Development of High-Performance Low-Dropout Regulators for SoC Applications

OR, Pui Ying

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Abstract

Recent development of power-management integrated circuits (ICs) provides revolutionary opportunities of energy usage for future Green and sustainable electronic devices. Advanced power converters including low-dropout regulator (LDO), switching-mode power converter and charge pump are the keys of power usage casting into the modern low-power IC systems. Among the afore-mentioned power converters, LDO is well-recognized to be the best candidate to provide power to the analogue and radio-frequency circuits in an IC system, as it can provide low-noise and ripple-free supply voltage to the supply- and noise-sensitive circuit blocks. In order to develop high-performance LDO for future IC applications, in this thesis, the power-supply rejection ratio (PSRR) and transient response are investigated.

A detailed analysis of PSRR of LDO is studied. It includes circuit modeling of a generic LDO with signal injection at its supply. Based on the modeling, the transfer function of PSRR is derived. Thorough analysis of the locations of poles and zeros obtained from the transfer function is carried out, and then recommendations to improve PSRR are given. The proposed model and the achieved results are verified by circuit simulations using BSIM models of a commercial CMOS 0.35-μm technology. The results reveal good agreement between the modeling and the PSRR property of a LDO.

Then, an output-capacitorless LDO with a direct voltage-spike detection circuit is presented in this thesis. The proposed voltage-spike detection is based on capacitive coupling. The detection circuit makes use of the rapid transient voltage at the LDO output to increase the bias current momentarily. Hence, the transient response of the

LDO is significantly enhanced due to the improvement of the slew rate at the gate of the power transistor. The proposed voltage-spike detection circuit is applied to an output-capacitorless LDO implemented in a standard 0.35-μm CMOS technology. Experimental results show that the LDO consumes 19 μA only. It regulates the output at 0.8 V from a 1-V supply, with dropout voltage of 200 mV at the maximum output current of 66.7 mA. The voltage spike and the recovery time of the LDO with the proposed voltage-spike detection circuit are reduced to about 70 mV and 3 μs, respectively, whereas they are more than 420 mV and 30 μs for the LDO without the proposed detection circuit.

Finally, a low-voltage fast-transient LDO compensated by an off-chip, low-ESR, nano-range output capacitor is reported. The proposed load-tracking impedance adjustment and the loop-gain boosting technique make the proposed LDO have fast response and small voltage spikes. The circuit is implemented by a commercial 0.35-μm CMOS technology. The chip area is 0.032 mm^2. The supply voltage ranges from 1.5 to 3 V. The regulated voltage is 1.2 V to provide 0 to 100 mA. The quiescent current in the no-load condition is 26 μA. A 100-nF low-ESR capacitor is sufficient to stabilize the proposed LDO. The measured voltage spike is 44.9 mV only, and the response time is less than 0.2 μs.

概要

電源管理集成電路近來發展迅速，爲未來一些主張省電的環保電子產品提供了一個電源供應的平台。這些能省電的電源管理集成電路主要包括了低電壓降穩壓器、切換式整流器以及電荷泵，而其中能有效阻隔雜訊的低電壓降穩壓器更被公認爲模擬集成電路和無線射頻系統的電源之最佳選擇。

在研發一些新的高質素的低電壓降穩壓器之前，了解電源抑制比和瞬態響應這兩個重要單位是不可缺少的一環。有關瞬態響應的報告在學術界中有很多，反而有關電源抑制比的深入討論卻寥寥可數。因此，在這論文中，首先探討的題目是電源抑制比的專題研究，根據模擬電路計算出其傳遞函數，再引申當中極點和零點之位置及其影響，最後針對這些影響提出相對的改善方法。

之後，論文會提出兩個提高低電壓降穩壓器性能的方案。第一個方案是爲了沒有輸出電容器的低電壓降穩壓器而設的，設計提供一個簡單的電路設計，及時提供額外電流予儀器，從而提高其瞬態響應。而第二個方案則爲連接輸出電容器的低電壓降穩壓器而提出的，其設計可令所需的輸出電容及其等效串聯電阻大大減少。這兩塊晶片都由 CMOS 350 nm (互補式金屬-氧化層-半導體 350 納米) 技術製成，由實驗結果證明其良好的瞬態響應。

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Journal Papers

1. **P. Y. Or** and K. N. Leung, "A Fast-Transient Low-Dropout Regulator with Load-Tracking Impedance Adjustment and Loop-Gain Boosting Technique," *IEEE Transactions on Circuits and Systems–II*, accepted for publication.
2. K. N. Leung, Y. K. Sun, L. K. K. Leung and **P. Y. Or**, "A Gain-Optimizing Regulated Charge Pump," *International Journal of Electronics*, accepted for publication.
3. K. N. Leung, F. K. M. Cheung, M. Ho, H. C. Poon and **P. Y. Or**, "A 1.9μW Transient-Enhanced Low-Dropout Regulator with Voltage-Spike Suppression," *Journal of Low Power Electronics*, Vol. 6, No. 1, pp. 126-132, Apr. 2010.
4. **P. Y. Or** and K. N. Leung, "An Output-Capacitorless Low-Dropout Regulator with Direct Voltage-Spike Detection," *IEEE Journal of Solid-State Circuits*, Vol. 45, No. 2, pp.458-466, Feb. 2010.

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1. **P. Y. Or** and K. N. Leung, "A Slew-Rate Enhancement Technique Based On Current Comparator and Capacitive-Coupled Push-Pull Output Stage for CMOS Amplifiers," *IEEE International Conference on Electron Devices and Solid-State Circuits*, Hong Kong, Dec. 2008.
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3. K. N. Leung, Y. S. Ng, K. Y. Yim and **P. Y. Or**, "An Adaptive Current-Boosting Voltage Buffer for Low-Power Low Dropout Regulators," *IEEE International Conference on Electron Devices and Solid-State Circuits*, Taiwan, Vol. I, pp. 485-488, Dec. 2007.
4. H. Y. Lo, **P. Y. Or**, K. N. Leung, L. L. K. Leung, C. S. Choy and K. P. Pun, "Design Challenges of Voltage Multiplier in a 0.35-um 2-Poly 4-Metal CMOS Technology for RFID Passive Tags," *IEEE International Conference on Electron Devices and Solid-State Circuits*, Taiwan, Vol. I, pp. 433-436, Dec. 2007.

Chapter 1

Background of LDO Research

Introduction

Low-dropout regulator (LDO) is a type of linear regulator which features a small input-output differential voltage [1]-[16]. Its stable, low-noise, fast-transient properties under different input-voltage and loading conditions, as well as temperatures, undoubtedly, provide outstanding supply to many analogue and RF circuits and systems. Thus, LDO is widely applied in many portable applications such as cellular phones, PDA handsets, especially the wireless multimedia devices.

1.1 Structure of a LDO

Fig. 1.1 shows the structure of a generic LDO. It basically consists of an error amplifier, a voltage buffer, a power transistor (M_P), a feedback resistor network (R_{F1} and R_{F2}) and a voltage reference (V_{REF}). The input and output voltage are denoted by V_{IN} and V_O, respectively, whereas R_L is used to model the load circuit. It is noted that C_{OUT} and R_{ESR} are the off-chip capacitor and its equivalent series resistance. Their function is to ensure the stability of the LDO based on dominant-pole frequency compensation with pole-zero cancellation. Moreover, C_{OUT} is used to provide transient current to the load when the LDO cannot respond to instantaneous change of the load current or the input voltage. The function of the voltage buffer is to drive the large gate capacitor of M_P so that slew rate at this node can be improved. In addition, the low output impedance can help to improve the stability of the LDO.

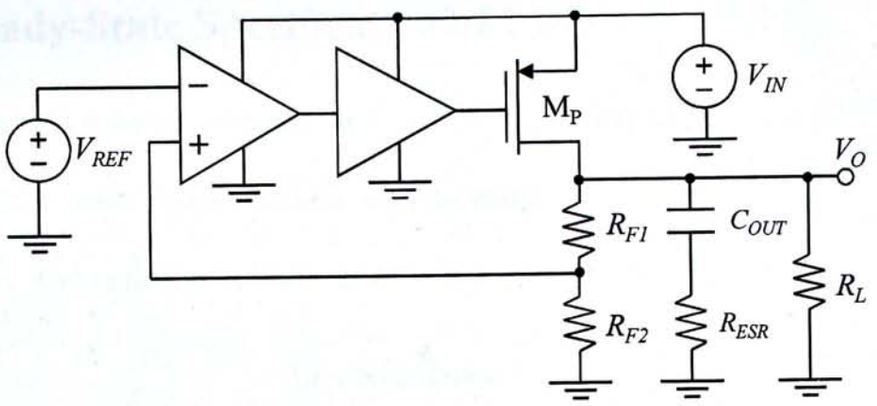

Fig. 1.1 Structure of a generic LDO.

1.2 Principle of Operation of LDO

The LDO structure shown in Fig. 1.1 reveals a feedback path [17]. The voltage regulation of V_O is therefore achieved by the feedback formed by the feedback network, the error amplifier, the voltage buffer and then the power transistor. The operation can be simply explained by the following example.

When the load current or the supply voltage changes, the LDO cannot respond the change instantaneously. As a result, V_O may increase or decrease. Assuming that V_O increases, the effect will be detected by the feedback network and appears at the non-inverting input of the error amplifier. By comparing with V_{REF}, the output of the error amplifier is then increased and the signal is propagated to the gate of the M_P through the voltage buffer. The reduction of V_{SG} of M_P causes the drain current being reduced so that less current is generated to the load and to charge the output capacitor. The resultant effect is that V_O drops accordingly. Similarly, when V_O drops below the preset voltage, the feedback takes control of the gate voltage of M_P by increasing its V_{SG} to provide more drain current to the load and C_{OUT}. This will make V_O increase to counter the effect. This mechanism repeats continuously to regulate V_O to a constant voltage.

1.3 Steady-State Specification of LDO

There are two specifications to measure the regulation ability of a LDO under the change of the input voltage and the loading current. They are line regulation and load regulation. The definition of line regulation is given by [1]

$$\text{Line Regulation} = \frac{\Delta V_O}{\Delta V_{IN}} \tag{1.1}$$

The unit of line regulation is mV/V. For load regulation, it is given by [1]

$$\text{Load Regulation} = \frac{\Delta V_O}{\Delta I_O} \tag{1.2}$$

where I_O is the loading current of the LDO circuit. The unit of load regulation is mV/mA. In fact, the relationship between the line and load regulations and circuit parameters has been extensively investigated in recent decade. It is found that higher loop gain achieved by a high-gain error amplifier improves both specifications [2].

1.4 High-Frequency Specification of LDO

Power supply rejection ratio (PSRR) is another important index to measure the ability of the LDO to suppress the noise from the input. The definition of PSRR is given by [15]

$$PSRR = 20\log\left|\frac{v_o(f)}{v_{in}(f)}\right| \tag{1.3}$$

Although many researchers have realized the importance of the PSRR of a LDO used for the future communication systems and they have proposed many effective LDO structures to reject high-frequency signal noise from the supply line, the fundamentals of the PSRR of a generic LDO has not been studied in detail. Therefore, PSRR is being analyzed in this thesis.

1.5 Dynamic Specification of LDO

In addition to steady-state and high-frequency specifications, dynamic specification such as load transient response is vital in LDO. Research focused on improving load transient response of a LDO has been extensively carried out in the past decade [1]-[14]. The researchers have been working hard to improve it for some LDO structures without and with the output capacitor. The main goal is to reduce the voltage spikes and shorten the recovery speed of the LDO output voltage.

1.6 An Advanced LDO Structure

Although the structure shown in Fig. 1.1 has been widely used for many years, it was found recently that a simpler LDO structure [14] based on flipped voltage follower [18], [19] can provide better performance. This structure is shown in Fig. 1.2.

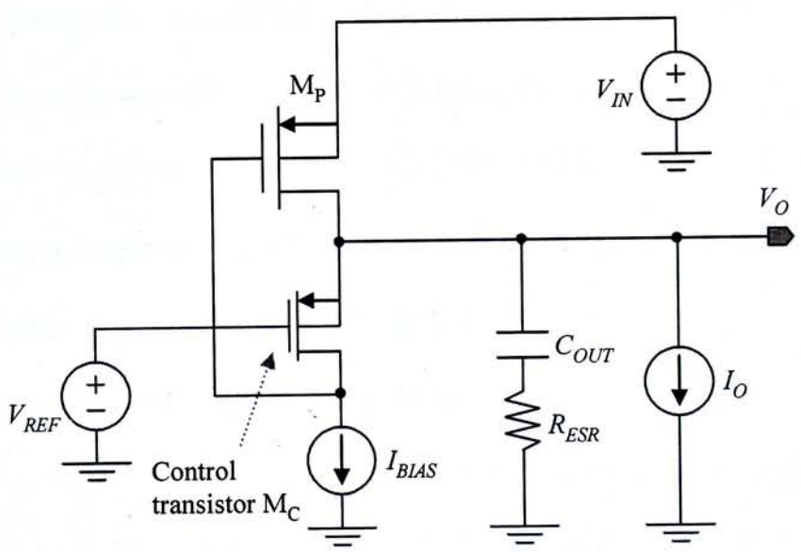

Fig. 1.2 Structure of the single-transistor-control LDO [14].

This circuit is regarded as single-transistor-control LDO which is suitable for SoC applications, and it has been analyzed by Man *et. al.* [14]. The LDO structure

basically consists of two basic transistors, with one being the power transistor (M_P) and the other being the control transistor (M_C). The power stage based on flipped voltage follower senses the change of the LDO output at the source of M_C, which the signal is compared with V_{REF} at the gate of M_C. An error voltage is then generated at its drain to change the gate voltage of M_P. Current via M_P is thus adjusted according to its source-to-gate voltage and regulates the LDO output. It is noted that this simple LDO structure needs a V_{TH}-compensated voltage reference to cancel the effect by M_C. This structure has many drawbacks such as slew-rate limited at the gate of M_P and inferior regulation ability. As a matter of fact, it is necessary to improve its performance by including some advanced circuit techniques which will be proposed in this thesis.

1.7 Contribution and Outline of the Thesis

Based on the foregoing background of LDO, it is known that the PSRR of a generic LDO has not been completely analyzed. Moreover, the transient response of the LDO structure, based on flipped voltage follower, without and with the output capacitor should be further improved by advanced circuit methods. Therefore, in this thesis, the contribution is focused on the following three aspects:

1. Chapter 2: PSRR analysis of generic LDO
2. Chapter 3: Improvement of the transient response of the LDO structure based on flipped voltage follower without the output capacitor
3. Chapter 4: Improvement of the transient response of the LDO structure based on flipped voltage follower with the output capacitor

The contributions of the research work are expected to be useful for future development of SoC applications [20].

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Chapter 2

PSRR Analysis

Introduction

Integrated power management is a promising approach to optimize function-rich SoC designs. The concept of integrated power management is to provide on-chip, locally optimized supply to power the system sub-blocks individually so that system performance can be enhanced and system power consumption can also be minimized simultaneously [1]. In the integrated power-management part, LDO is one of the power converters widely used for the analogue and RF parts of a SoC design, since it can provide low-noise, high-precision and ripple-free supply voltage [2]-[8]. Meanwhile, LDO is a good post-regulator as it can suppress high-frequency noise propagating from the supply lines through the LDO. Power-supply rejection ratio (PSRR) is used to measure the ability of signal suppression of a LDO, which is given by

$$\text{PSRR} = 20\log\left|\frac{v_o(f)}{v_{in}(f)}\right| \tag{2.1}$$

where $v_{in}(f)$ and $v_o(f)$ are the input signal and the output signal, respectively. The frequency range of interest was from DC to around 100 kHz in ten years ago due to the fact that the signal bandwidth of the former communication standard is not high. However, with rapid development of the communication standard, the signal bandwidth is being increased dramatically. One example is Worldwide Interoperability for Microwave Access (WiMAX). The signal bandwidth of WiMAX is scalable under different transmission conditions, ranging from 1.25 MHz to 28

MHz [9], [10]. As a result, when there is noise signal ranging from DC to 28 MHz appearing at the supply line, it must be suppressed by the supply-rejection property of a LDO. Otherwise, the noise signal will propagate into the communication circuits and is being up-converted to the frequency band of the communication standard (e.g. 2.3 GHz to 3.8 GHz for the WiMAX standard). The signal-to-noise ratio of the communication system will then be degraded seriously. For the above-mentioned application, it is known that the PSRR up to 28 MHz or even higher becomes very important for the future communication standards.

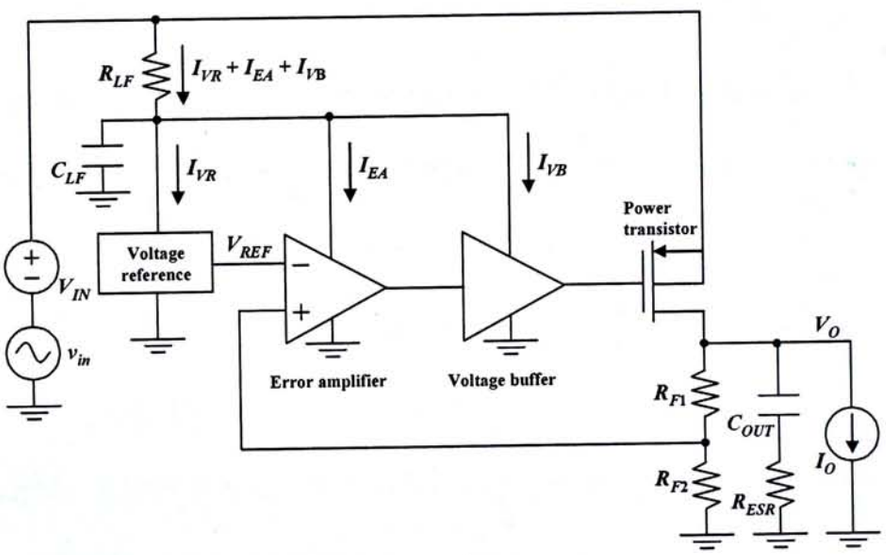
Although many researchers have realized the importance of the PSRR of a LDO used for the future communication systems and they have proposed many effective LDO structures to reject the high-frequency signal noise from the supply line (e.g. in [8], a LDO with PSRR of -56 dB at 10 MHz was reported), the fundamentals of the PSRR of a generic LDO has not been studied in detail. Typical understanding is to use cascode structure or NMOSFET power transistor to provide better isolation between the supply line and the output of the LDO. Some mentioned the importance of the loop bandwidth but did not discuss how much loop bandwidth is required to improve the PSRR up to a particular frequency range. Certainly, the material and quality of the off-chip output capacitor would affect the value of the equivalent series resistance (ESR), which is another key factor affecting PSRR at high frequency.

In fact, it is very important to understand the relationship between the circuit parameters and the PSRR of LDO so that the key design concepts can be extracted, before stepping further to develop more sophisticated LDO structures. Therefore, this chapter presents the circuit modeling of a LDO to investigate the PSRR in Section 2.1. Based on the modeling, the transfer function of PSRR is found and the poles and zeros are obtained for a detailed analysis. In Section 2.2, the circuit modeling is then

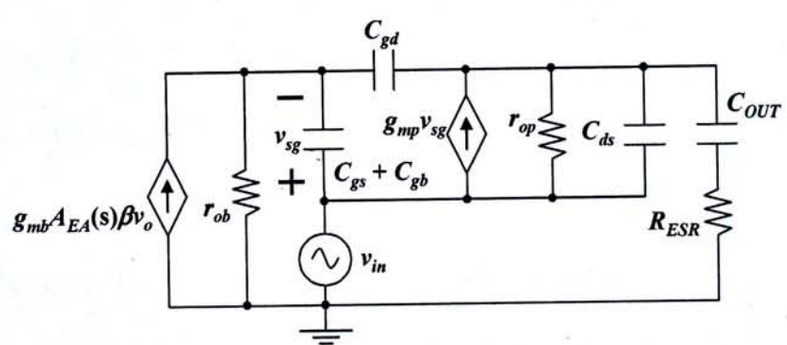
verified by a real LDO circuit operating in different conditions. By investigating the locations of the poles and zeros, some design recommendations to improve the PSRR are made and presented. Finally, the conclusion of this chapter summarizes the design recommendations to improve the PSRR of a generic LDO.

2.1 Modeling of the PSRR of LDO

The LDO structure under PSRR test is shown in Fig. 2.1(a), and the corresponding small-signal circuit is illustrated in Fig. 2.1(b).



(a)



(b)

Fig. 2.1 LDO under PSRR test (a) structure (b) small-signal circuit.

It is highlighted that

1. $A_{EA}(s) = G_{mEA}R_{OEA}/(1 + sC_{OEA}R_{OEA})$ is the transfer function of the error amplifier, where G_{mEA} and R_{OEA} are the transconductance and the equivalent output resistance of the error amplifier, respectively. Moreover, C_{OEA} is the equivalent output capacitance of the error amplifier.
2. g_{mb} and r_{ob} are the transconductance and the output resistance of the voltage buffer, where $r_{ob} \approx 1/g_{mb}$.
3. C_{gs}, C_{gb}, C_{gd} and C_{ds} refer to the parasitic capacitances of the power PMOS transistor.
4. C_{OUT} is much larger than the parasitic capacitances in the LDO.
5. The gain of the power transistor is negative and is equal to $g_{mp}r_{op}$, where g_{mp} and r_{op} are the transconductance and output resistance of the power transistor in saturation region.
6. R_{ESR} is the ESR of the off-chip capacitor of the LDO.
7. $\beta = R_{F2}/(R_{F1} + R_{F2})$ is the feedback factor.
8. The supply signal through the voltage reference, error amplifier and voltage buffer are neglected without losing accuracy as a simple *RC*-filter formed by R_{LF} and C_{LF} can be added to suppress the signal injection successfully. The *IR* drop across the added *RC*-filter can be ignored since the bias currents of the voltage reference, error amplifier and voltage buffer (i.e. I_{VR}, I_{EA} and I_{VB}) are in micro-amperes.

From Fig. 2.1(b), the transfer function of PSRR is given by

$$\frac{v_o(s)}{v_{in}(s)} \approx \frac{A_{LF}\left(1+\frac{s}{z_{ESR}}\right)\left(1+\frac{s}{z_1}\right)\left(1+\frac{s}{z_2}\right)\left(1+\frac{s}{z_3}\right)}{\left(1+\frac{s}{p_{ESR}}\right)\left(1+\frac{s}{Qp_o}+\frac{s^2}{p_o^2}\right)} \tag{2.2}$$

where $A_{LF} = \dfrac{1+g_{mp}r_{op}}{A_{EA}g_{mb}r_{ob}\beta g_{mp}r_{op}}$ is the low-frequency PSRR. From the transfer function, there are four zeros given by

$$z_1 = \frac{1}{C_{OEA}R_{OEA}} \tag{2.3a}$$

$$z_2 = \frac{1+g_{mp}r_{op}}{[C_{gs}+C_{gb}+C_{gd}(1+g_{mp}r_{op})]r_{ob}} \tag{2.3b}$$

$$z_3 = \frac{C_{gs}+C_{gb}+C_{gd}(1+g_{mp}r_{op})}{[C_{ds}(C_{gs}+C_{gb}+C_{gd})+C_{gd}(C_{gs}+C_{gb})]r_{op}} \tag{2.3c}$$

$$z_{ESR} = \frac{1}{C_{OUT}R_{ESR}} \tag{2.3d}$$

and a pair of complex poles, as well as a pole given by

$$p_o = \sqrt{\frac{G_{mEA}g_{mb}g_{mp}\beta R_{ESR}}{(C_{gs}+C_{gb}+C_{gd})C_{OEA}}} \tag{2.4a}$$

$$Q = \sqrt{\frac{A_{EA}g_{mb}g_{mp}\beta R_{ESR}C_{OEA}R_{OEA}}{C_{gs}+C_{gb}+C_{gd}}} \tag{2.4b}$$

$$p_{ESR} = \frac{1}{C_{OUT}R_{ESR}} \tag{2.4c}$$

It is found that the pole and zero created by C_{OUT} and R_{ESR} cancel each other. Since there is no C_{OUT} term in the expressions of the poles and zeros other than p_{ESR} and z_{ESR}, it can be concluded that C_{OUT} is not a factor affecting the PSRR. This is based on an assumption that C_{OUT} is larger than all parasitic capacitances in the circuit, which is always valid.

Based on equations, the typical PSRR plot is obtained and shown in Fig. 2.2. It is noted that the transfer function shown in (2.2) is accurate up to the frequency of z_3. In fact, it is hard to perform accurate analysis in the frequency domain after z_3 due to the complicated relationship interacted by the parasitic capacitances of the power

transistor and the control circuit. Therefore, the study of the PSRR of a LDO presented in this chapter is focused up to the frequency of z_3 only (i.e. the shaded region in Fig. 2.2), but it is sufficient for general wireless communication applications with signal bandwidth of about 10 MHz to 30 MHz. In the next section, detailed analysis of the PSRR of a LDO with different design parameters such as R_{OEA}, A_{EA}, R_{ESR} and I_O will be given.

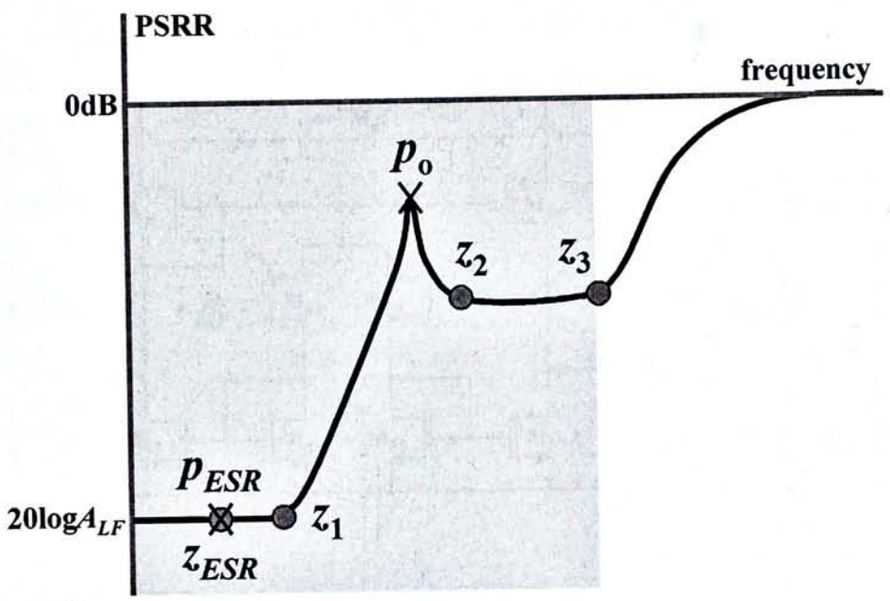


Fig. 2.2 Typical plot of PSRR vs. frequency of a generic LDO.

2.2 Analysis of LDO Circuit Using Proposed Modeling

In order to have a more realistic picture of the analysis, a circuit in the transistor level is used to verify and make conclusions of the analysis. The circuit implementation of the LDO under the PSRR test is illustrated in Fig. 2.3. The error amplifier and the voltage buffer are formed by M_{A1}-M_{A9} and M_{B0}-M_{B1}, respectively. The error amplifier is a current-mirror amplifier with a wide output swing. The voltage buffer is a source follower implemented by a PMOS transistor only with the bulk terminal connected to its source terminal to avoid signal injection from the supply via the bulk terminal. Moreover, the simulated signal injection is from an AC voltage source, v_{in},

so that the connection allows signal-injection-free voltage supplied to the error amplifier and the voltage buffer, and provides signal injection to the power transistor M_{PT} simultaneously. The LDO circuit is simulated using the BSIM3v3 models of austriamicrosystems (AMS) CMOS 0.35-μm technology (with V_{IN} = 3.3 V, V_O = 3 V, I_O = 100 mA, C_{OUT} = 10 μF and R_{ESR} = 0.1 Ω) to investigate the effects on the PSRR of the LDO under several conditions such as different R_{OEA}, A_{EA}, R_E and I_O.

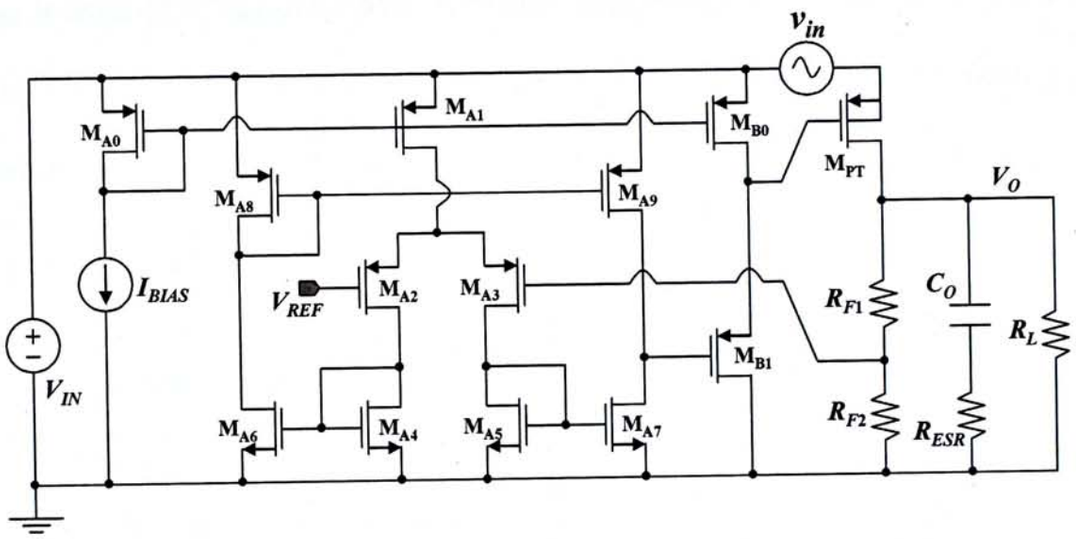


Fig. 2.3 A generic LDO used to investigate PSRR.

A. Impact of R_{OEA} towards PSRR

From (2.3a) and (2.4b), the value of R_{OEA} would affect the position of z_1 as well as the Q-factor of p_o. Certainly, the value of A_{LF} also closely relates to it. Based on this observation, some simulations with different R_{OEA} are carried out. The approach to change R_{OEA} is to have more parallel-connected transistors to M_{A7} and M_{A9} so that the bias current can be increased. According to the well-known relationship between the output resistance of a transistor (r_o) and drain current (I_D) given by $r_o \propto (I_D)^{-1}$, it is found that R_{OEA} can be altered by this approach. Certainly, the value of C_{OEA} will be changed as well, but it is less than the gate capacitance of M_{B1} in general situations and so the change can be neglected.

According to (2.3a) and (2.4b), when R_{OEA} is small, z_1 will be increased and shifted to higher frequency. The location of p_o will remain nearly unchanged, but with a smaller Q-factor which means that the sharpness of the frequency peak is reduced. It is noted that the effects to the Q-factor of p_o by R_{OEA} are not strong due to the square-root relationship.

The simulation result with two different R_{OEA} is shown in Fig. 2.4. The change of R_{OEA} is from 15.8 MΩ to 6.3 MΩ. A smaller R_{OEA} results in degraded A_{LF}, z_1 locating at higher frequency, and the reduced sharpness of the frequency peak, while p_o is located at about the same frequency. The results match with the said theory well.

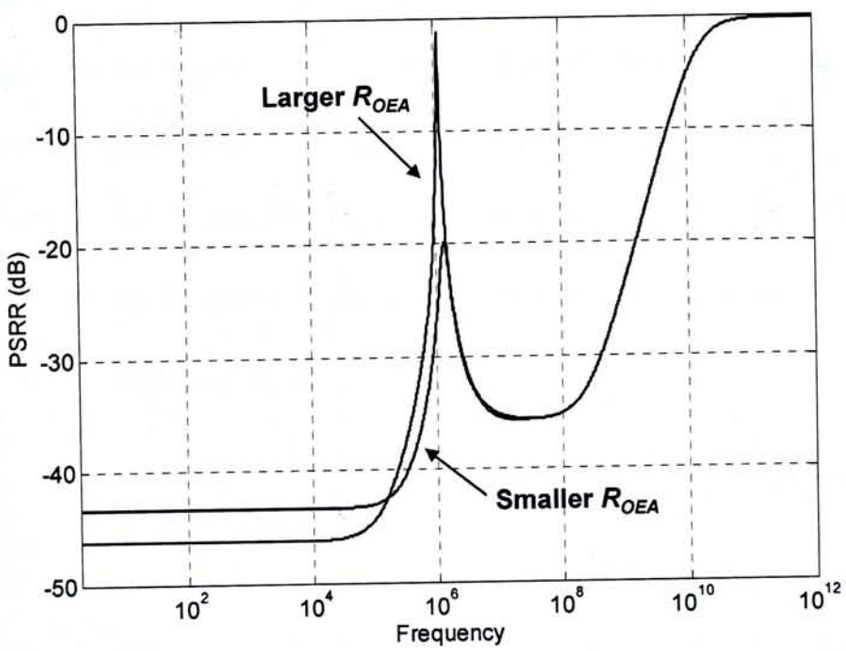


Fig. 2.4 PSRR with two different R_{OEA}.

From the study, as well as the simulation, it is found that a higher R_{OEA} undoubtedly provides a better PSRR at low frequency. However, the PSRR in the moderate frequency range (i.e. at about 1 MHz) is seriously degraded. In fact, from the simulation result, R_{OEA} does not cause a significant impact for gaining a better PSRR. Three critical parameters concerning PSRR will be discussed in the next sub-sections.

B. Relationship between PSRR and A_{EA}

After the study of R_{OEA} which is a parameter related to the error amplifier, the gain of the error amplifier is studied. To investigate the impact of the gain of error amplifier to the PSRR, one of the methods is to change the output voltage level of the error amplifier. Since V_{SG} of M_{PT} is fixed for a fixed output current, the change can be made by different V_{SG} of M_{B1}. Therefore, different bias current applied to M_{B1} can be used to study this phenomenon.

When the output voltage of the error amplifier is in the middle of the supply voltage, A_{EA} should be the highest since both M_{A7} and M_{A9} can have a large V_{DS} simultaneously. However, when V_{SG} of M_{B1} increases, M_{A7} will have smaller V_{DS} and so its conductance is increased. As a result, A_{EA} is decreased and this increases A_{LF}. The increased A_{LF} means the output of the LDO is more sensible to the change of the input voltage (i.e. the worse PSRR). As a result, A_{EA} is preferred to be large for getting a better PSRR from low to moderate frequency, which can be verified by the simulation results shown in Fig. 2.5.

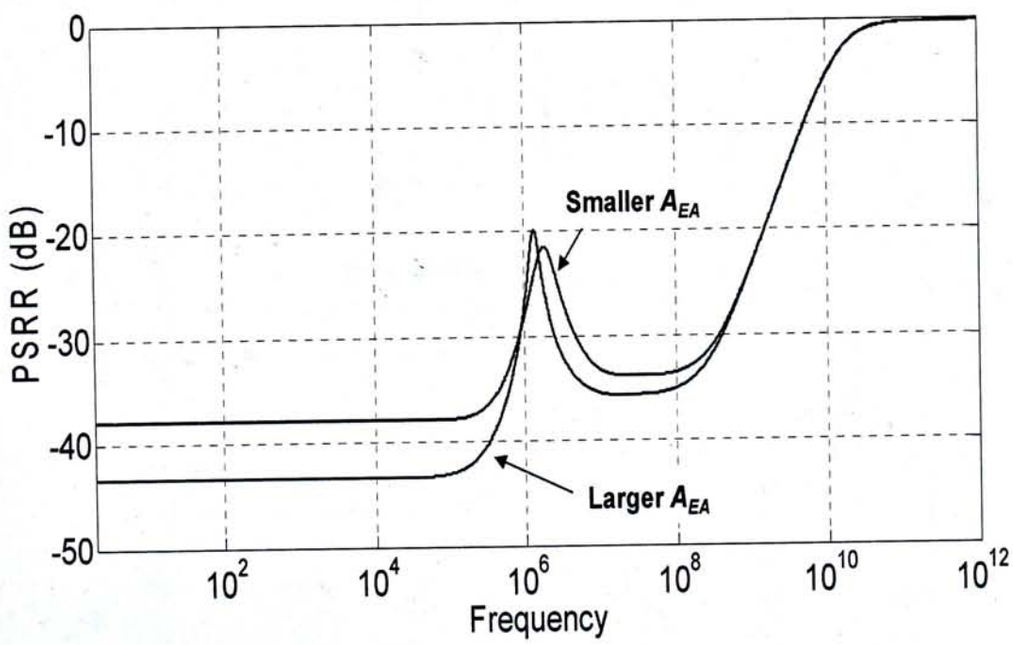


Fig. 2.5 PSRR under two different A_{EA}.

C. Influence of PSRR under different R_{ESR}

In this sub-section, the effect of the off-chip capacitor is studied. It is stated in Section 2.1 that both p_{ESR} and z_{ESR} cancel each other. As a result, the C_{OUT} term does not appear in (2.2). However, the R_{ESR} term seriously affect the PSRR, especially at high frequency.

Refer to (2.4a) and (2.4b), a larger R_{ESR} would cause p_o to higher frequency with a larger Q. This can be ascertained from the simulation result shown in Fig. 2.6. The curve with R_{ESR} of 0.3 Ω does have a sharper peak locating at higher frequency, when compared to that with a smaller R_{ESR} of 0.1Ω. Although a larger R_{ESR} benefits from pushing the complex poles to higher frequency, the larger Q-factor would cause a serious degradation in the PSRR of the LDO. Therefore, Q-factor should have a high priority over the location of p_o when choosing the R_{ESR}. In that case, a smaller R_{ESR} would be more favorable in obtaining a better PSRR. In addition to the smaller Q-factor, smaller R_{ESR} also demonstrated a better PSRR in the moderate to high frequency region.

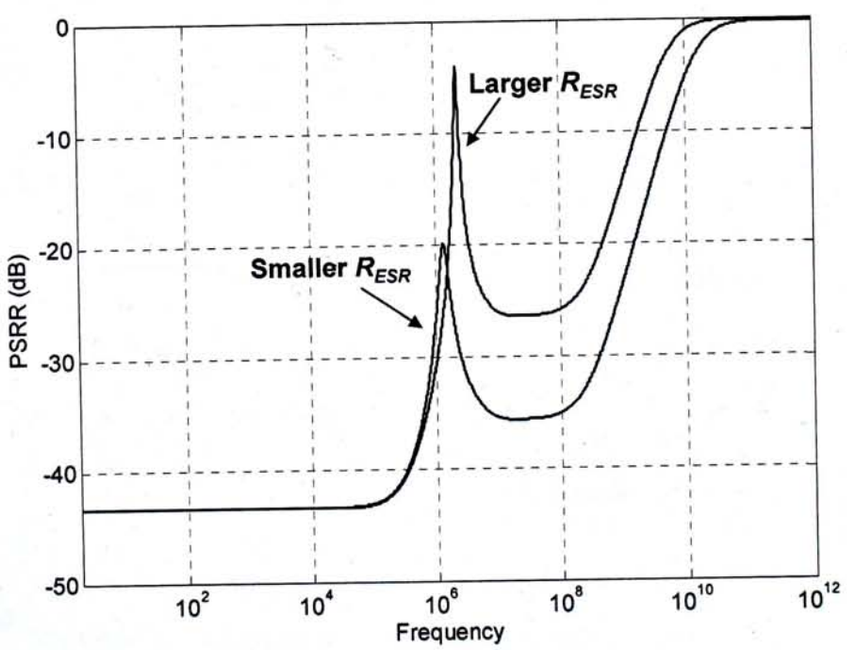


Fig. 2.6 PSRR under two different R_{ESR}.

D. Characteristic of PSRR under different I_O

Finally, the effect due to the power transistor is investigated. At low frequency, the impedance of the power transistor is extensively improved by the feedback loop. Therefore, the output voltage of a LDO is well-regulated. However, at moderate frequency, the feedback loop is no longer effective due to the finite loop bandwidth. It is not hard to understand that the high-frequency conductance of the power transistor is a dominant factor to affect the PSRR in the moderate frequency range. Since the size of the power transistor is determined by the maximum output current and IC technology, the output current alters the high-frequency conductance of the power transistor. From (2.4a) and (2.4b), when I_O decreases and g_{mp} is decreased, p_o will be shifted to a lower frequency than z_1, with a smaller Q to give a better PSRR.

The PSRR of the LDO at I_O = 0 A, 1 mA, 10 mA and 100 mA are simulated with results shown in Fig. 2.7. The worst PSRR happens at the maximum loading current, whereas the best case is at minimum loading current. When investigating PSRR of a LDO, the maximum loading case should be considered for the worst-case analysis.

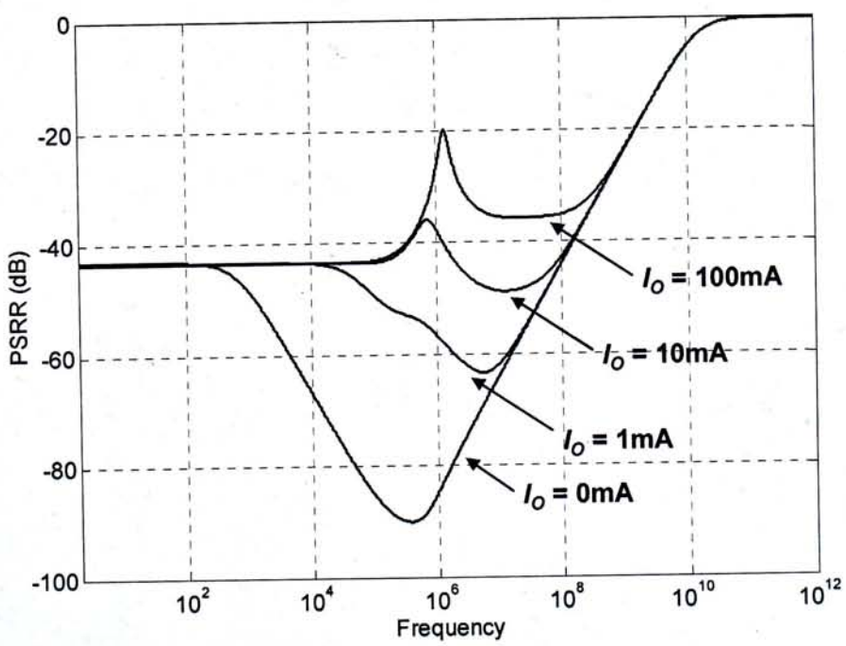


Fig. 2.7 PSRR under different I_O.

2.3 Conclusion of Chapter

The PSRR of a generic LDO has been analyzed in this chapter. The poles and zeros of the LDO have been investigated from the transfer function of the proposed modeling. In addition, several design parameters affecting the PSRR have been studied in detail. The conclusions made are

1. A higher R_{OEA} undoubtedly provides a better PSRR at low frequency. However, the PSRR in the moderate frequency range is degraded seriously.
2. A_{EA} and R_{ESR} take a significant role on improving the PSRR. A larger A_{EA} could gain a better PSRR at low to moderate frequency, while a smaller R_{ESR} could achieve PSRR enhancement at moderate to high frequency.

Finally, the worst PSRR happens at maximum I_O.

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Chapter 3[‡]

An Output-Capacitorless LDO with Direct Voltage-Spike Detection

Introduction

Transient response is a critical dynamic specification in LDO design. Both the amplitude of the voltage spike and the recovery time of the regulated output voltage affect its overall accuracy, which indirectly impacts the performance of the circuits supplied by the LDO. In fact, the transient response of a LDO is related to different design parameters such as the closed-loop stability, the loop bandwidth (BW_L) and the slew rate at the gate of the power transistor (SR_G) [1]-[5]. The closed-loop stability and BW_L are small-signal parameters related to the positions of the poles and the zeros in the feedback system, while SR_G is a large-signal parameter that depends heavily on the magnitude of the bias current [6]. Undoubtedly, typical measures to optimize the transient response of a LDO are to increase the output capacitance, use a low ESR capacitor, and increase the bias current of the error amplifier/voltage buffer [1]. However, in the SoC design, it is expected to place an on-chip output-capacitorless LDO adjacent to individual circuit blocks, so that the power supply of each circuit block can be optimized independently (i.e. accuracy, magnitude, power-supply rejection and noise) to improve the overall performance of the system [7]. The regulated power supplies are generated inside the SoC chip. Under this circumstance, in the SoC design, the generic approach using external capacitors is no longer useful to effectively reduce the voltage spike due to the

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non-zero bondwire inductance and the long power-line routings (i.e. RC delay). Therefore, more power is needed to increase both BW_L and SR_G of the LDO to suppress the voltage spike and reduce the recovery time.

Fig. 3.1 shows one reported LDO structure used in [8]-[10] to enable output capacitorless LDO. The LDO structure is basically based on the flipped voltage follower [11], which is a modified structure of the super source follower [6]. V_{IN} is the unregulated input voltage of the LDO. M_P is the power transistor, while M_{C1} and M_{C2} form a folded error amplifier in the common-gate configuration [10]. The source of M_{C1} detects the LDO output for comparing with a control voltage (V_{SET}) defined at the gate of M_{C1}. An error signal is then generated at the gate of the power transistor to achieve closed-loop voltage regulation by the negative feedback. The output impedance of the LDO is reduced drastically by the loop gain of the shunt feedback [6]. Since there is no large output capacitor in an output-capacitorless LDO, the shunt feedback can push the pole created at the LDO output away from BW_L [10]. Generally, BW_L is wide, as the dominant pole is a function of the gate capacitance of the power transistor (C_{par}), which is much smaller than the value of the output capacitance typically in the order of μF [8]-[10]. Thus, the transient response of the LDO shown in Fig. 3.1 is dominated by the SR_G limit.

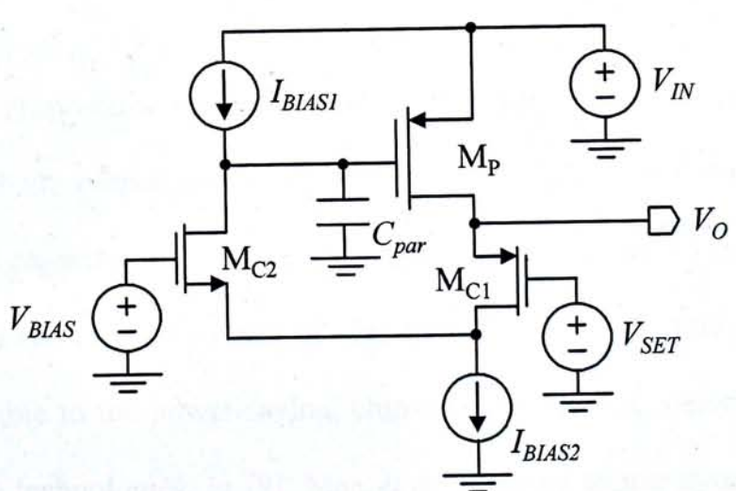


Fig. 3.1 An output-capacitorless LDO reported in [8]-[10].

There are several reported approaches to solve the problem, and the relationship between the output current and the quiescent current is shown in Fig. 3.2.

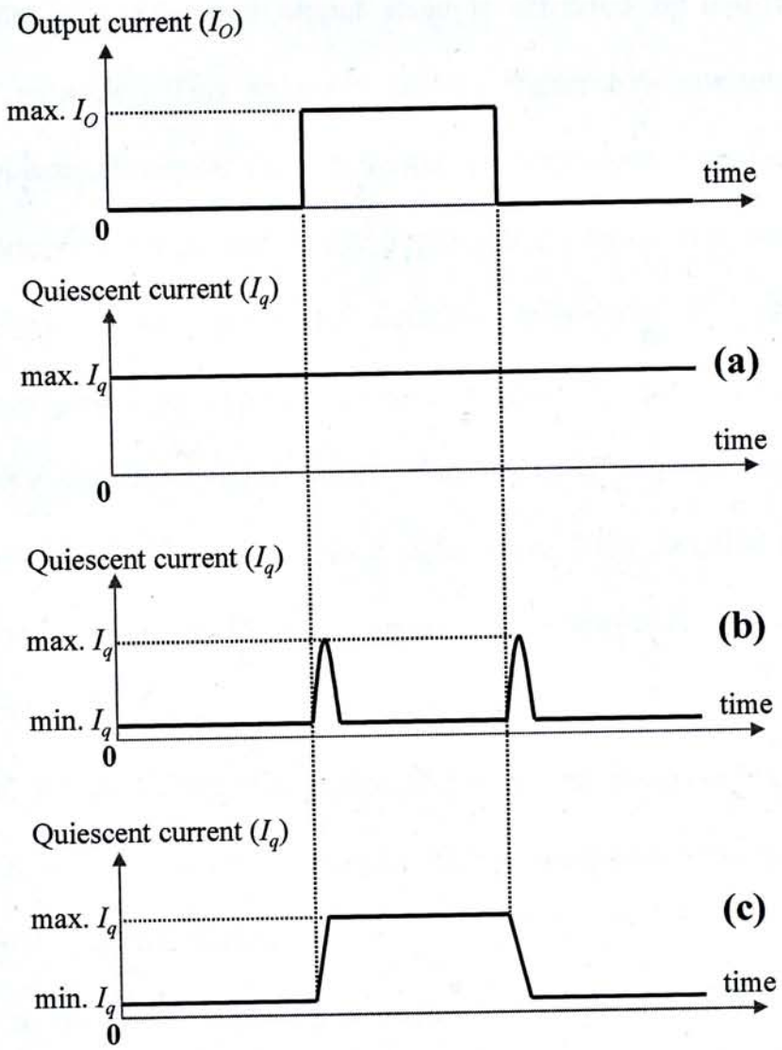


Fig. 3.2 Relationship between the output current and the quiescent current of the LDO (a) constant biasing [8] (b) dynamic biasing [9] (c) current-efficient current buffer [1], [12].

Hazucha *et al.* proposed to use heavy bias current of 6 mA, where the bias current is independent of the output current as shown in Fig. 3.2(a), and connect a 600-pF on-chip output capacitor to their LDO, implemented in CMOS 90-nm technology, to deliver a maximum output current of 100 mA [8]. However, this approach is not always applicable to the power-saving, chip-area-limited SoC designs implemented in inexpensive technologies. In [9], Man *et al.* reported to use dynamic biasing, so more bias current is used only at the transient instant when the output current is

changed, as shown in Fig. 3.2(b). The error amplifier has a push-pull output stage to inject and withdraw more current for charging and discharging C_{par} during the transient instant. The push-pull output stage is activated by a differential-input common-gate amplifier. This approach enables higher bias current to solve the SR_G-limit problem. However, the differential common-gate amplifier has limited input common-mode range and, most importantly, limited bandwidth. The fast changing voltage spike cannot be detected effectively by the differential common-gate amplifier. As a result, more power applied to the amplifier is needed in order to achieve significant improvement of the transient response. In addition, this approach is not applicable when V_O is a small value. This situation happens when providing an adaptive supply for a power-saving SoC design. Another approach is to increase the bias current according to the magnitude of the output current [1], [12], as shown in Fig. 3.2(c). This method is not as good as the adaptive-biasing technique reported in [9], as the bias current remains high in the steady state when the output current does not reach the minimum.

According to the brief review, it is obvious that the extra bias current is only needed during the transient instant to solve the SR_G-limit problem. It is not necessary to keep the bias current high in the steady state. The adaptive biasing technique reported in [9] enables this important advantage, but it suffers from the slow response and the limited input range of the differential common-gate input stage. To solve this problem, a simple and effective voltage-spike detection circuit applied to the LDO structure shown in Fig. 3.1 is proposed in this chapter. The proposed voltage-spike detection is based on capacitive coupling. The detection circuit makes use of the rapid transient voltage at the LDO output to increase the bias current momentarily. Hence, the transient response of the LDO can be significantly

enhanced due to the improvement of SR_G. Moreover, the small-signal response is also improved by the capacitive-coupling feature.

In this chapter, Section 3.1 presents the small-signal and large-signal responses of the output-capacitorless LDO. Section 3.2 introduces the proposed voltage-spike detection circuit and its design details [13]. Experimental results are presented in Section 3.3. Finally, the conclusion of this chapter is given.

3.1 Analysis of Output-Capacitorless LDO

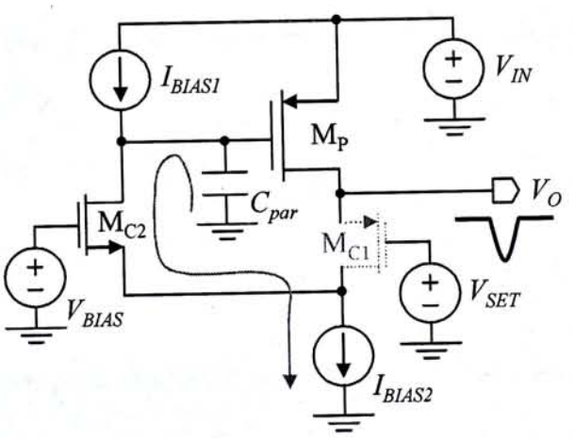
Referring to the output-capacitorless LDO shown in Fig. 3.1, when the output current of the LDO (I_O) suddenly increases (or decreases), the LDO cannot respond to the change for decreasing (or increasing) the gate voltage of M_P to increase (or decrease) its drain current instantaneously due to the finite BW_L of the LDO [1]-[5]. When the LDO is able to respond, the decrease (or increase) of the gate voltage of M_P is then constrained by the limited SR_G. Since an output-capacitorless LDO does not have a large off-chip output capacitor to provide charges to the load circuit (or accept the excess current from M_P) at the transient instant, V_O drops (or increases) dramatically and a large voltage spike is generated.

In fact, the closed-loop small-signal response of the output-capacitorless LDO is mainly determined by M_{C1}, since ΔV_O changes its V_{SG} to generate a small-signal current for voltage regulation. As a result, the transconductance of M_{C1} should be large in order to improve the small-signal response. This implies that more power is needed to apply to the LDO to achieve faster small-signal response.

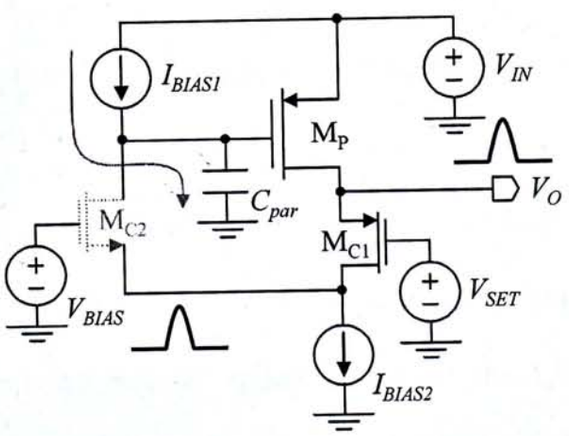
The output-capacitorless LDO undergoes large-signal response when there is rapid and large change of I_O. Fig. 3.3(a) and (b) shows the large-signal responses of the LDO when I_O suddenly increases and decreases, respectively. When I_O rapidly

increases, the LDO cannot change V_{SG} of M_P instantaneously to provide current due to the large C_{par}, and this situation causes V_O to drop. The drop of V_O reduces V_{SG} of M_{C1}, and it causes M_{C1} to cut off momentarily. Thus, $I_{BIAS2} - I_{BIAS1}$ is the discharging current of C_{par}.

Similarly, when I_O suddenly decreases, the LDO cannot reduce V_{SG} of M_P immediately and it makes V_O rise. The increase of V_O causes the drain voltage of M_{C1} to increase due to the property of the common-gate amplifier. Since the source terminal of M_{C2} has low resistance ($\sim 1/g_m$), the increase of the drain voltage of M_{C1} is nearly the same as the increase of V_O. This causes M_{C2} to cut off momentarily. Therefore, the charging current of C_{par} is I_{BIAS1}.



(a)



(b)

Fig. 3.3 Large-signal response of the output-capacitorless LDO (a) undershoot (b) overshoot.

From the above analysis, both I_{BIAS1} and I_{BIAS2} determine SR_G. Higher bias current does enhance the transient response of the LDO, but this approach consumes unnecessary power since there is no charge/discharge mechanism of C_{par} in the steady state. Moreover, the discharging current of C_{par} is $I_{BIAS2} - I_{BIAS1}$. Therefore, the discharging capability of C_{par} cannot be fully utilized by solely increasing I_{BIAS2}. Finally, the transistor size of M_P is very critical, since it determines the value of C_{par} or, in another point of view, the required amount of the bias current to solve the SR_G-limit problem. In 1-V or even sub-1V operation without low threshold-voltage devices, a larger transistor size is needed to compensate the low V_{IN} (the maximum allowable V_{SG} of M_P) for delivering a large I_O. Low and steady quiescent current is not possible to achieve fast transient response of the sub-1-V LDO since C_{par} is extremely large.

3.2 LDO with Proposed Voltage-Spike Detection Circuit [13]

The proposed voltage-spike detection circuit will be introduced in this section. The design and operation of the LDO with the proposed circuit will be discussed in detail.

A. Structure and principle of operation of the proposed voltage-spike detection circuit

Fig. 3.4 illustrates the concept of the proposed direct voltage-spike detection circuit. The main idea of the circuit is to momentarily increase the bias current of the control circuit of the LDO when voltage spikes appear at the LDO output in order to overcome the problem of the SR_G limit due to the large C_{par} of M_P. The circuit, in fact, is a simple current mirror formed by M_1 and M_2, where I_1 and I_2 are the input current and the output current of the current mirror, respectively. The major

modification to this current mirror is the addition of two passive components, R_1 and C_1 [14]. The voltage source V_{PULSE} is used to demonstrate the voltage spike for investigating the effect to the change of I_2.

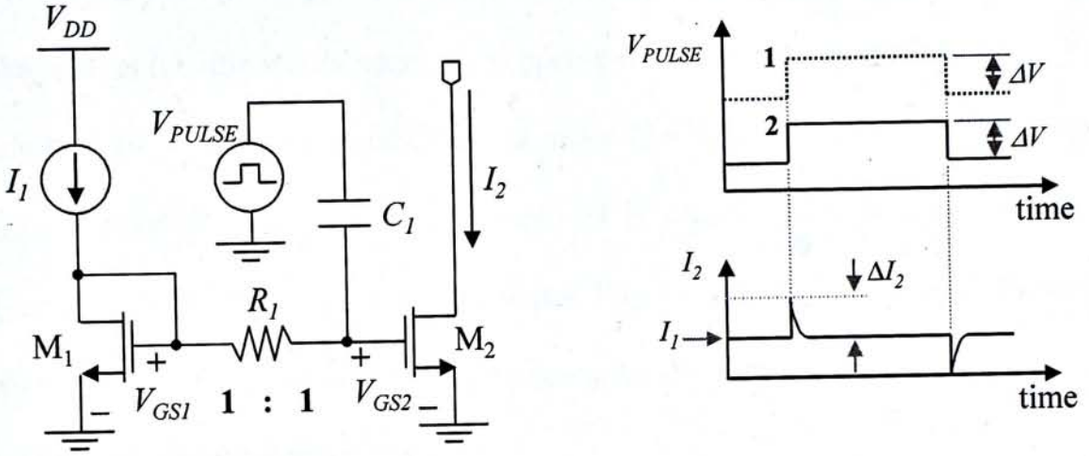


Fig. 3.4 Current mirror with high-pass *RC*-network to momentarily increase the bias current.

In the steady state, V_{PULSE} remains constant, and so V_{GS2} is defined by V_{GS1} to give $I_2 = I_1$. However, as shown by the timing diagrams in Fig. 3.3, when the amplitude of V_{PULSE} changes from low to high (ΔV) instantaneously, the rapid voltage change of V_{PULSE} is coupled to the gate of M_2 directly due to the high-pass property of C_1. In addition, R_1 is chosen to be large for better isolation between M_1 and M_2 during the change of V_{PULSE}. As a result, when C_1 is chosen to be larger than $C_{gs1} + C_{gs2}$, the gate voltage of M_2 is dominated by the coupled signal from C_1 in this instant, instead of the DC voltage provided by R_1. Thus, V_{GS2} is increased momentarily to increase I_2.

The extra current (ΔI_2) can be found from

$$\begin{aligned} I_2 + \Delta I_2 &= \frac{\mu_n C_{OX}}{2} \cdot \left(\frac{W}{L}\right)_{M2} \cdot \left(V_{GS2} + \Delta V - V_{TH}\right)^2 \\ &= \frac{\mu_n C_{OX}}{2} \cdot \left(\frac{W}{L}\right)_{M2} \cdot \left[\left(V_{GS2} - V_{TH}\right)^2 + \Delta V^2 + 2\Delta V\left(V_{GS2} - V_{TH}\right)\right] \end{aligned} \tag{3.1}$$

From (3.1), the magnitude of ΔI_2 is extracted and is given by

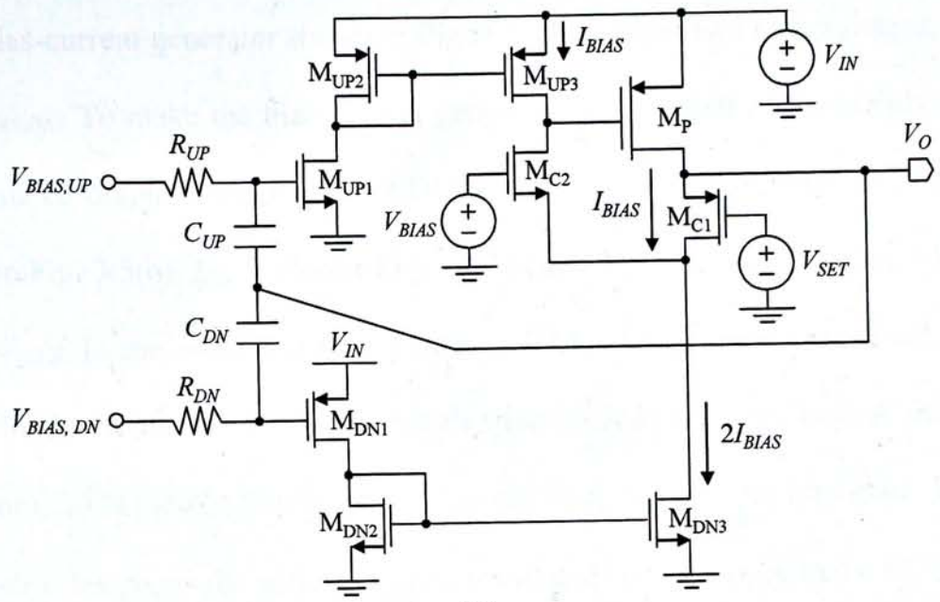
$$\Delta I_2 \approx \mu_n C_{OX} \cdot \left(\frac{W}{L}\right)_{M2} \cdot \left(V_{GS2} + \frac{\Delta V}{2} - V_{TH}\right)\Delta V \tag{3.2}$$

From (3.2), it is found that a larger W/L aspect ratio of the current mirror helps to increase ΔI_2 for injecting more transient current. When V_{PULSE} stays at a constant voltage level (i.e. the steady state), C_1 is open-circuited and R_1 dominates. Thus, V_{GS2} is defined by V_{GS1} in the steady state to make $I_2 = I_1$ once again. Similarly, when V_{PULSE} changes from high to low, the rapid ΔV is coupled through C_1 to the gate of M_2 and the coupled voltage signal decreases V_{GS2} to generate a smaller I_2. From the above analysis, the proposed direct voltage-spike detection circuit can provide auto shutdown of the bias-current boosting.

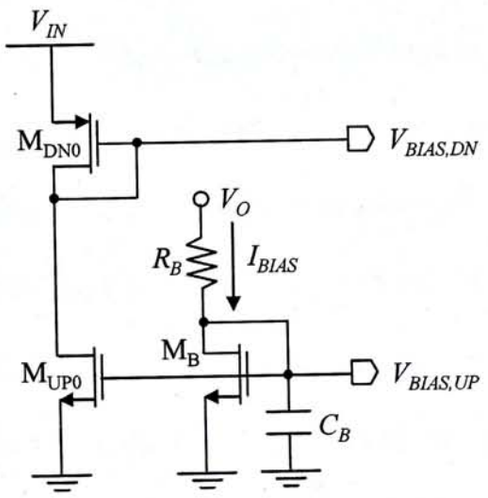
Finally, the coupling effect is independent of the DC value (but is limited by the breakdown voltage of the transistors) of V_{PULSE} (Curves 1 and 2 in Fig. 3.4) due to the high-pass characteristic of the capacitor. Therefore, the proposed detection method is suitable for detecting any output voltage level of the LDO.

B. LDO with the proposed voltage-spike detection circuit

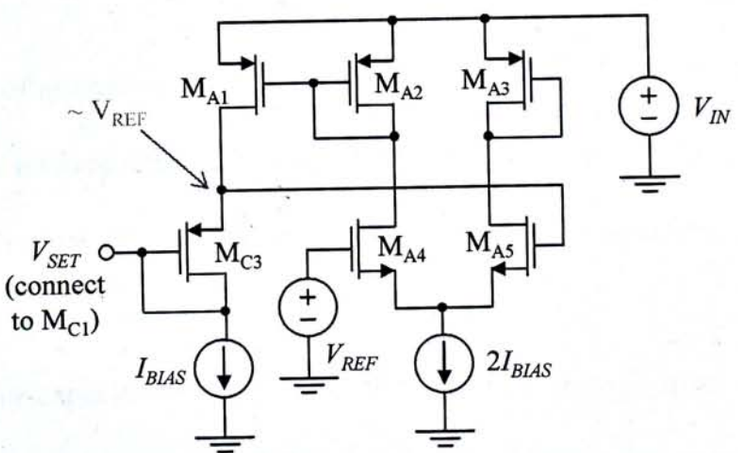
The LDO presented in this chapter is formed by the proposed voltage-spike detection circuit, a bias-current generator and a control-voltage generator [10]. Their circuit implementations are shown in Fig. 3.5. Fig. 3.5(a) shows the modified LDO structure based on the LDO shown in Fig. 3.1. M_{UP1}, M_{UP2} and M_{UP3} provide I_{BIAS1} to the LDO shown in Fig. 3.1, while M_{DN1}, M_{DN2} and M_{DN3} give I_{BIAS2}. The coupling capacitors, C_{UP} and C_{DN}, as well as two resistors, R_{UP} and R_{DN}, are included to the LDO to form the proposed voltage-spike detection circuit illustrated in Fig. 3.4. One of the two terminals of both C_{UP} and C_{DN} are connected to V_O to achieve direct detection of the voltage spikes created at the transient instant. Moreover, the voltage source V_{SET} is generated by the control-voltage generation circuit in Fig. 3.5(c).



(a)



(b)



(c)

Fig. 3.5 Full circuit diagram of the LDO with the proposed voltage-spike detection circuit (a) LDO core (b) bias-current generator (c) control-voltage generator.

The bias-current generator shown in Fig. 3.5(b) provides two bias voltages, $V_{BIAS,UP}$ and $V_{BIAS,DN}$. To make the bias-current generator independent of the supply voltage, the regulated output voltage of the LDO is used for the bias-current generation. As shown in Fig. 3.5(b), I_{BIAS} is formed by R_B, M_B and V_O, so that $I_{BIAS} = (V_O - V_{SG,B})/R_B$ where $V_{SG,B}$ is the source-to-gate voltage of M_B. Since V_O is regulated, I_{BIAS} is supply-independent as $V_{SG,B}$ is a constant when I_{BIAS} is once defined. A decoupling capacitor (C_B) is used to stabilize I_{BIAS}. The accuracy of C_B is not important. It is 2 pF only in this design, as the value of I_{BIAS} is small and is about 1 μA in the LDO design.

The control-voltage generator shown in Fig. 3.5(c) is basically an amplifier with negative feedback. It occupies nearly the same chip area as the error amplifier inside a generic LDO. A temperature- and supply-independent reference voltage (V_{REF}) is provided by a voltage-reference circuit. The source-to-gate voltage of M_{C1} ($V_{SG,C1}$) is connected at the output of the LDO, so that $V_O = V_{SET} + V_{SG,C1}$. Since $V_{SET} = V_{REF} - V_{SG,C3}$ where $V_{SG,C3}$ is the source-to-gate voltage of M_{C3}, $V_{SG,C1} = V_{SG,C3}$ is needed to achieve $V_O = V_{REF}$. As a result, the transistor sizes of M_{C1} and M_{C3} are the same and the current flowing through M_{C1} and M_{C3} are designed to be I_{BIAS}.

C. Principle of operation of the LDO with proposed voltage-spike detection circuit

This section includes the small-signal and large-signal analysis, as well as the design details of the LDO with the proposed voltage-spike detection circuit.

C.1. Small-signal response

For the output-capacitorless LDO with the proposed voltage-spike detection circuit shown in Fig. 3.5, the insertion of C_{UP} and C_{DN} (high-pass components) provides two quick paths and skip M_{C1} (a low-pass and bandwidth-limited component) to detect ΔV_O. The drop (or increase) of V_O is detected by C_{UP} to decrease (or increase) the

gate voltage of M_{UP1} and subsequently decrease (or increase) the gate voltage of M_P through the signal path formed by M_{UP2} and M_{UP3}. Similarly, C_{DN} also senses the drop (or increase) of V_O to decrease (or increase) the gate voltage of M_{DN1} and finally decreases (or increase) the gate voltage of M_P via the signal path formed by M_{DN2}, M_{DN3} and M_{C2}.

The selection of the values of C_{UP} and C_{DN}, as well as R_{UP} and R_{DN} can be done by investigating their corner frequencies and BW_L of the LDO. Fig. 3.6 shows a simple figure to illustrate the relationship. Since BW_L of the LDO is low-pass and limited while C_{UP} & R_{UP} and C_{DN} & R_{DN} are high-pass with the corner frequencies equal to $1/C_{UP}R_{UP}$ and $1/C_{DN}R_{DN}$, it is designed to make the corner frequencies lower than BW_L. This approach does virtually extend the loop-bandwidth of the LDO, and it makes sure that either the LDO itself or the proposed voltage-spike detection circuit responds to the small-signal changes of V_O. The typical BW_L of a LDO with 100-mA output capability is about 200 kHz to 1 MHz [1]-[5]. Assuming the corner frequency is set to be 100 kHz, the required C_{UP} (C_{DN}) and R_{UP} (R_{DN}) are 3 pF and 530 kΩ, respectively. The accuracy and the matching of the values are not important, and so C_{UP} and C_{DN} are implemented by poly-poly capacitor. They can be implemented by MOS capacitors to reduce chip area in triple-well technologies. R_{UP} and R_{DN} can be implemented by MOSFET or NWELL-resistor to reduce the chip area.

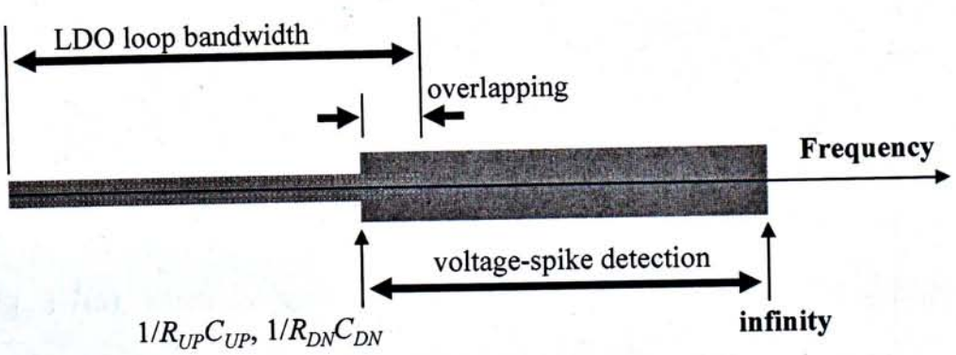


Fig. 3.6 Frequency range of operation of the LDO and the proposed voltage-spike detection circuit.

C.2. Large-signal response

The large-signal response is illustrated in Fig. 3.7, and the corresponding transient responses of the drain current of M_{UP3} and M_{DN3} are shown in Fig. 3.8.

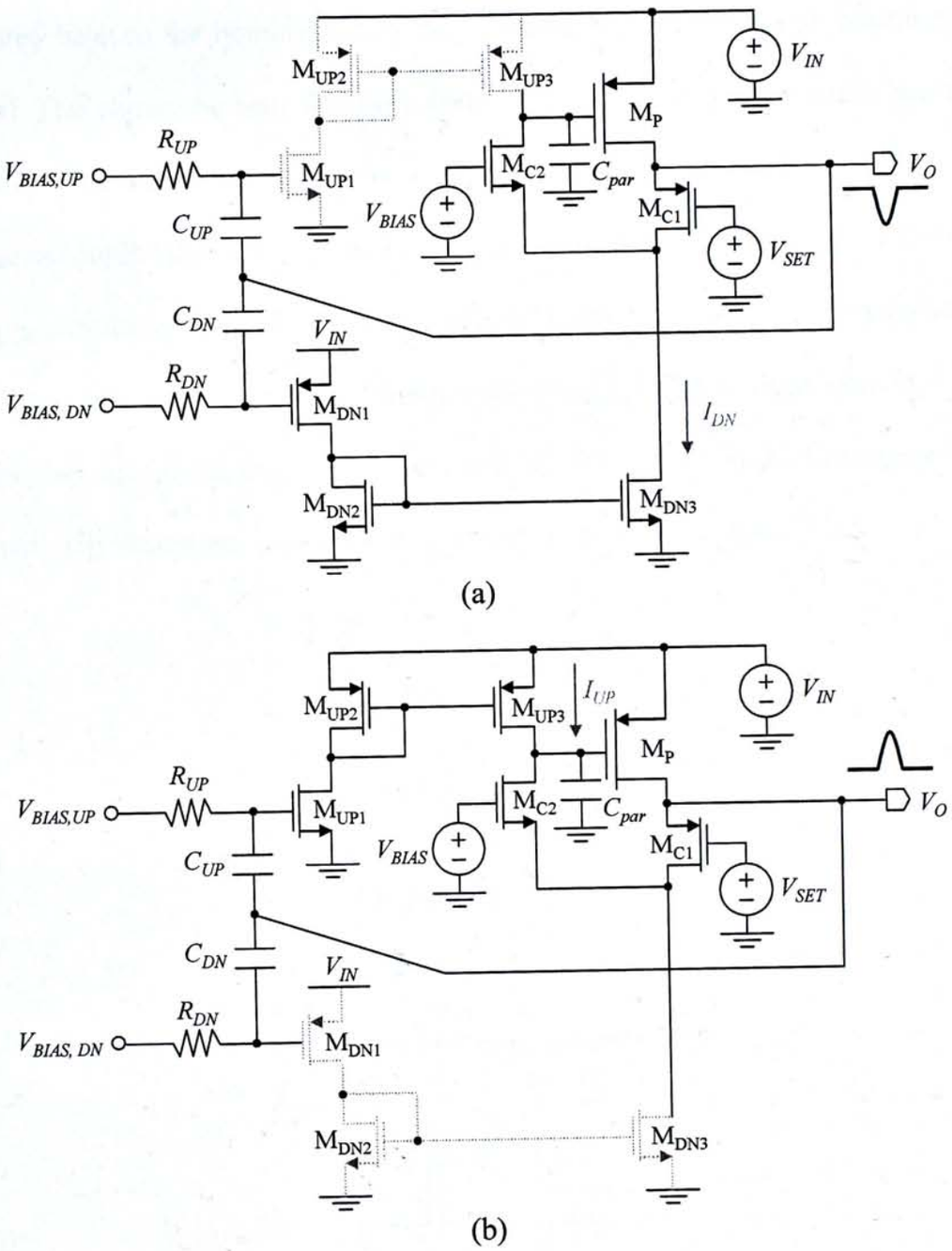


Fig. 3.7 Principle of operation of the proposed voltage-spike detection circuit (a) undershoot (b) overshoot.

In Fig. 3.7(a), when I_O increases suddenly, V_O drops rapidly. The change is then sensed by C_{UP} and C_{DN}, and is coupled to the gates of M_{UP1} and M_{DN1}. Due to coupling effect of C_{UP}, V_{GS} of M_{UP1} decreases, and thus the current of M_{UP3} is

reduced. At the same time, C_{DN} passes the change to the gate of M_{DN1}. It leads to a drastically and momentarily increase of V_{SG} of M_{DN1} to make I_{DN} increase. Therefore, a push-pull output stage is formed by M_{UP3} and M_{DN3} to discharge C_{par}. When V_O is regulated back to the nominal value, the bias condition of the circuit returns to the normal. This shows the auto-shutdown feature of the proposed bias-current boosting.

Similarly, as shown in Fig. 3.7(b), when I_O suddenly decreases, V_O increases. This change is coupled through C_{UP} and C_{DN} again to increase V_{GS} of M_{UP1} and reduce V_{SG} of M_{DN1} simultaneously. Therefore, a push-pull output stage is formed momentarily, since M_{UP3} provides more drain current while M_{DN3} gives less drain current. C_{par} is charged up to reduce the current provided by M_P to the load. The operation is automatically shut down again when V_O returns to the steady state.

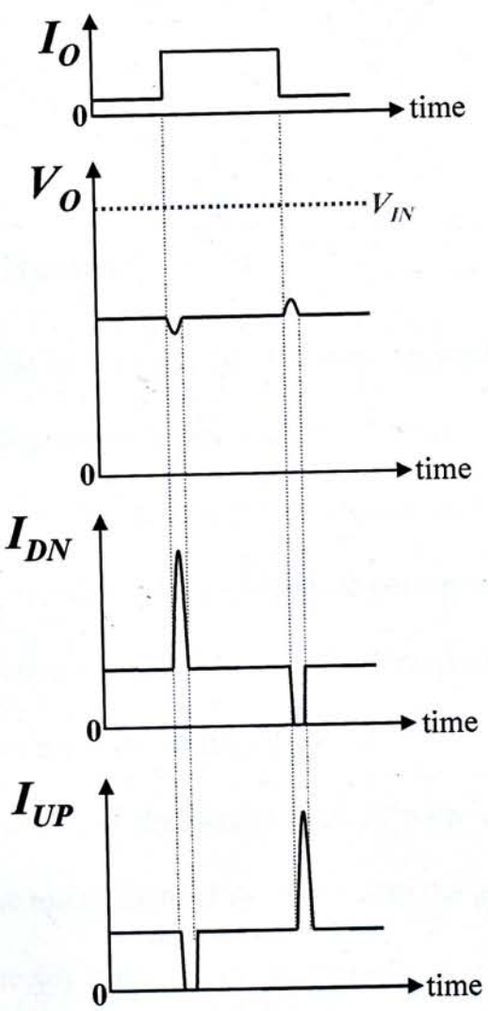


Fig. 3.8 Drain-current change of M_{UP3} and M_{DN3} during the load transient response.

Finally, as mentioned previously, C_B in Fig. 3.5(c) is used to maintain the bias current during large-signal response. In Fig. 3.9, a simulation shows the change of V_O not affecting I_{BIAS} much.

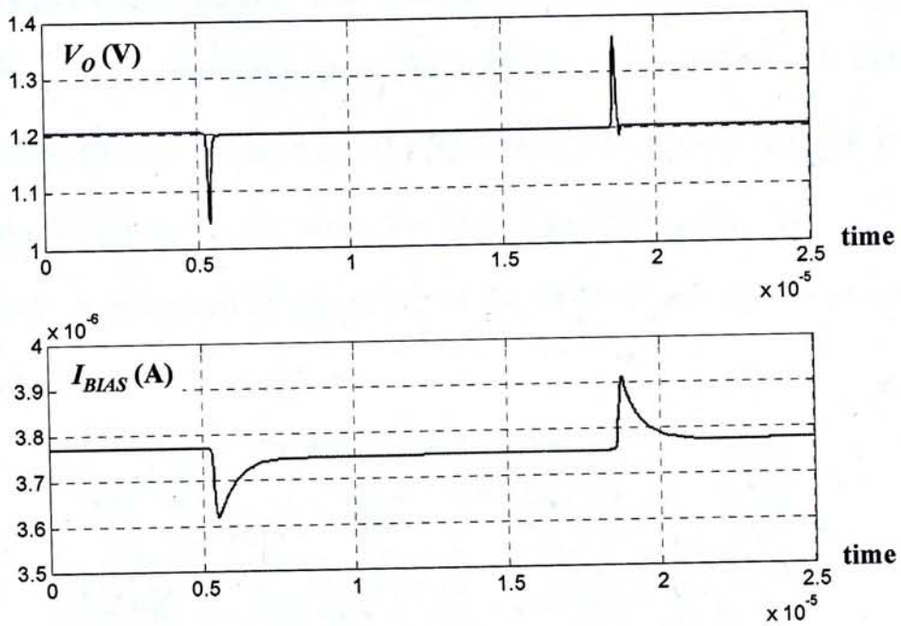


Fig. 3.9 Simulated change of I_{BIAS} under the change of V_O.

3.3 Experimental Results

The proposed voltage-spike detection circuit has been applied to a LDO design in Fig. 3.5 fabricated by austriamicrosystems (AMS) 0.35-μm CMOS process. The applications of the proposed LDO are for the analogue and RF parts in a SoC system. In order to make a fair comparison on the transient performance, a LDO without the proposed voltage-spike detection circuit is also implemented. The only difference is that both C_{UP} and C_{DN} are removed to disable the detection circuit, while the circuit structure, all transistor sizes and the bias current of both LDO designs remain the same. Fig. 3.10 shows the micrograph of the LDO with the proposed detection circuit. Table 3.1 summarizes the key information. The threshold voltages of the NMOSFET and PMOSFET are about 0.5 V and -0.65 V, respectively. Since the threshold

voltage of the PMOSFET is -0.65 V, the overdrive voltage is not high when the supply voltage is low (e.g. 1 V). Therefore, the required transistor size of M_P is 30000 μm / 0.35 μm to provide high I_O. The chip area is 597 μm × 260 μm, excluding the test pads. The chip area occupied by the control-voltage generator is less than 2% of the overall chip area. The transient responses of both LDOs are measured. Both LDOs do not need an off-chip capacitor to achieve stability. It is also found that the LDOs are stable when the output parasitic capacitance due to the power line, which is located at the output of the LDO, is non-zero (two cases are tested: 100 pF and 1 nF).

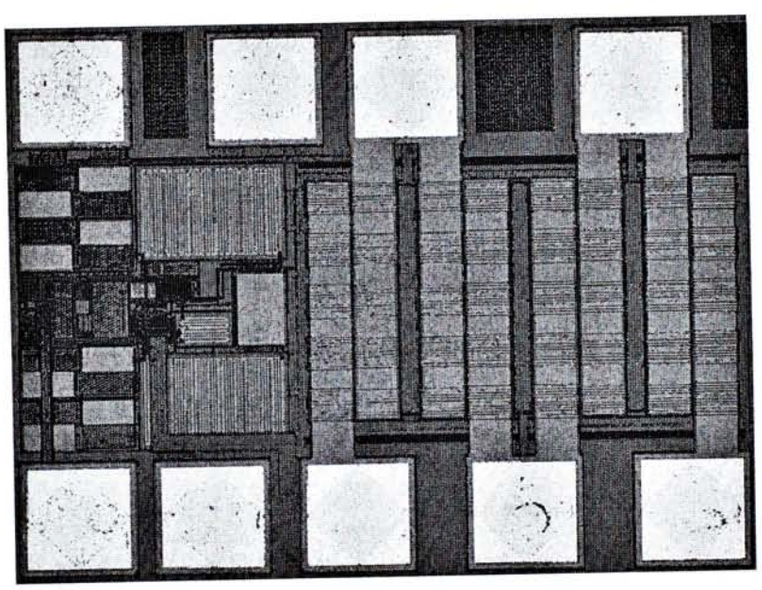


Fig. 3.10 Micrograph of the LDO with the proposed voltage-spike detection circuit.

Table 3.1 Summary of the design parameters.

Technology	AMS CMOS 0.35-μm 2P4M
V_{THN}	~ 0.5 V
V_{THP}	~ -0.65 V
Power-transistor size	30000 μm / 0.35 μm
Chip area	597 μm × 260 μm (excluding the test pads)
Output capacitor	Not required Stable even connected with a 100-pF or 1-nF capacitor

Fig. 3.11 shows the experimental setup to measure the load-transient response of both LDOs. The minimum output current ($I_{O(min)}$) is defined by R_{L1} connected between the LDO output and the ground, and so $I_{O(min)} = V_O/R_{L1}$. To define the maximum output current ($I_{O(max)}$), R_{L2} and an integrated NMOSFET (M_N) are used. The purpose to integrate M_N on the chip for the measurement is to minimize the associated parasitic capacitance and resistance for obtaining more accurate transient results in the range of micro- or nano-second. The gate of M_N is driven by a signal generator with a periodic square wave, so that M_N is turned on and off alternatively. By applying a large gate voltage to M_N (3.3 V is used in the measurement), the on-resistance of M_N is 55 mΩ, which is much smaller than R_{L2} (12.12Ω), and thus the effect from M_N can be ignored. Thus, the value of the current flowing through R_{L2} is $I_{O(max)} - I_{O(min)} = V_O/R_{L2}$. From Fig. 3.11, V_O is directly extracted and monitored by the scope, while I_O is obtained indirectly from the node voltage V_X. Since $V_X = V_O - I_O R_{L2}$, $V_X \propto -I_O$. Therefore, the extracted V_X is scaled and inverted by the scope to illustrate the transient change of I_O.

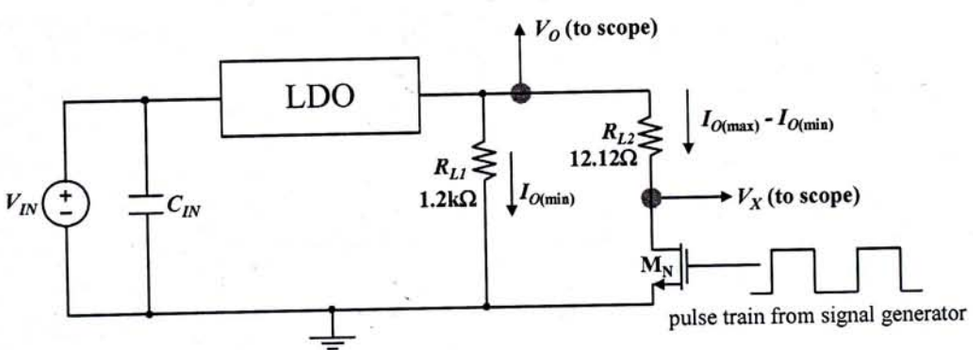


Fig. 3.11 Measurement setup to investigate the load-transient response.

Different combinations of the input voltage, the output voltage and the output current are tested. The measurement results are shown in Figs. 3.12, 3.13 and 3.14. The test cases are

1. $V_{IN} = 1.4$ V, $V_O = 1.2$ V and $I_{O(max)} = 100$ mA (Fig. 3.12)

2. V_{IN} = 1 V, V_O = 0.8 V and $I_{O(max)}$ = 66.7 mA (Fig. 3.13)

3. V_{IN} = 0.95 V, V_O = 0.7 V and $I_{O(max)}$ = 58.3 mA (Fig. 3.14)

The quiescent current and the current efficiency of each case are shown in Table 3.2. The reason for the difference of $I_{O(max)}$ at different V_{IN} and V_O is that the values of R_{L1} and R_{L2} are fixed in the measurement (as shown in Fig. 3.11). In fact, when the size of M_P is fixed, $I_{O(max)}$ is limited by V_{IN} (due to the maximum allowable V_{SG} of M_P) and it is also constrained by the dropout voltage (V_{IN} - V_O). Therefore, at V_{IN} = 0.95 V, the value of $I_{O(max)}$ is the lowest and the required dropout voltage is 0.25 V. Moreover, Fig. 3.5(c) shows that the quiescent current of the LDOs is a function of V_O. Therefore, the quiescent current at V_O = 0.7 V is the lowest among the three test cases. There is only 14 μA to drive the large C_{par} of M_P with size of 30000 μm / 0.35 μm. This implies the SR_G limit becomes more serious when V_O is lower. The above results demonstrate the impact of the lower quiescent current to the transient response of the LDOs with and without the proposed voltage-spike detection circuit.

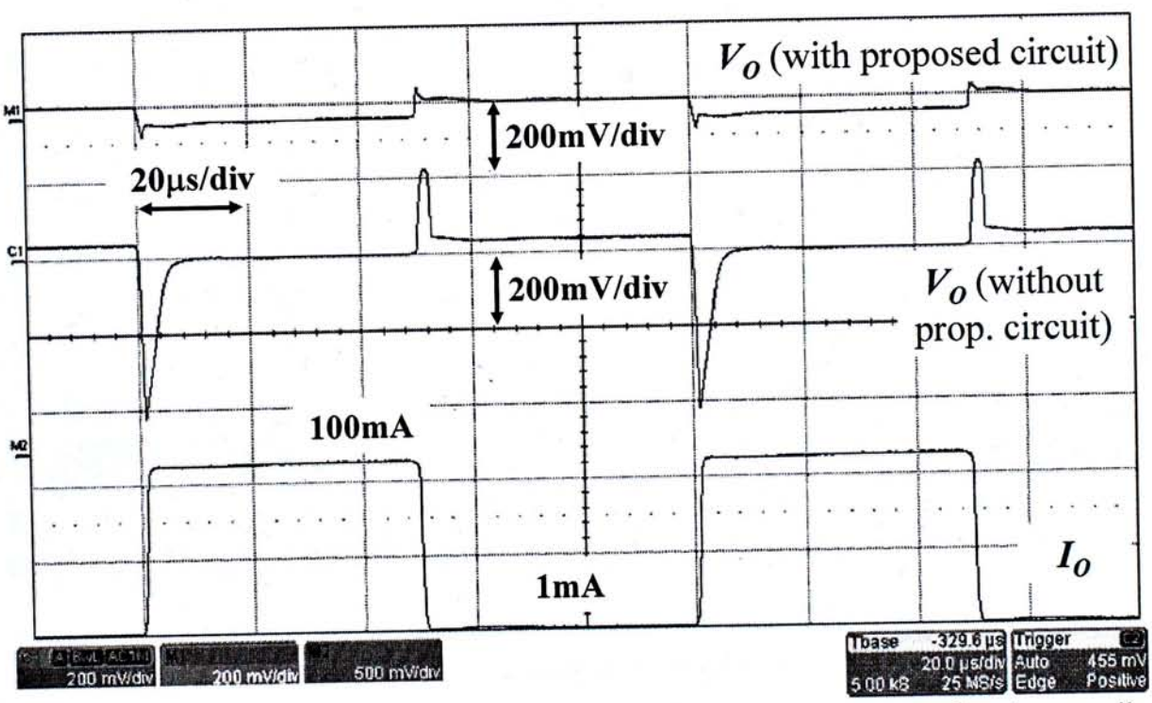


Fig. 3.12 Comparison of two LDOs with and without the proposed voltage-spike detection circuit, where V_{IN} = 1.4 V, V_O = 1.2 V, dI_O/dt = 99 mA/1 μs.

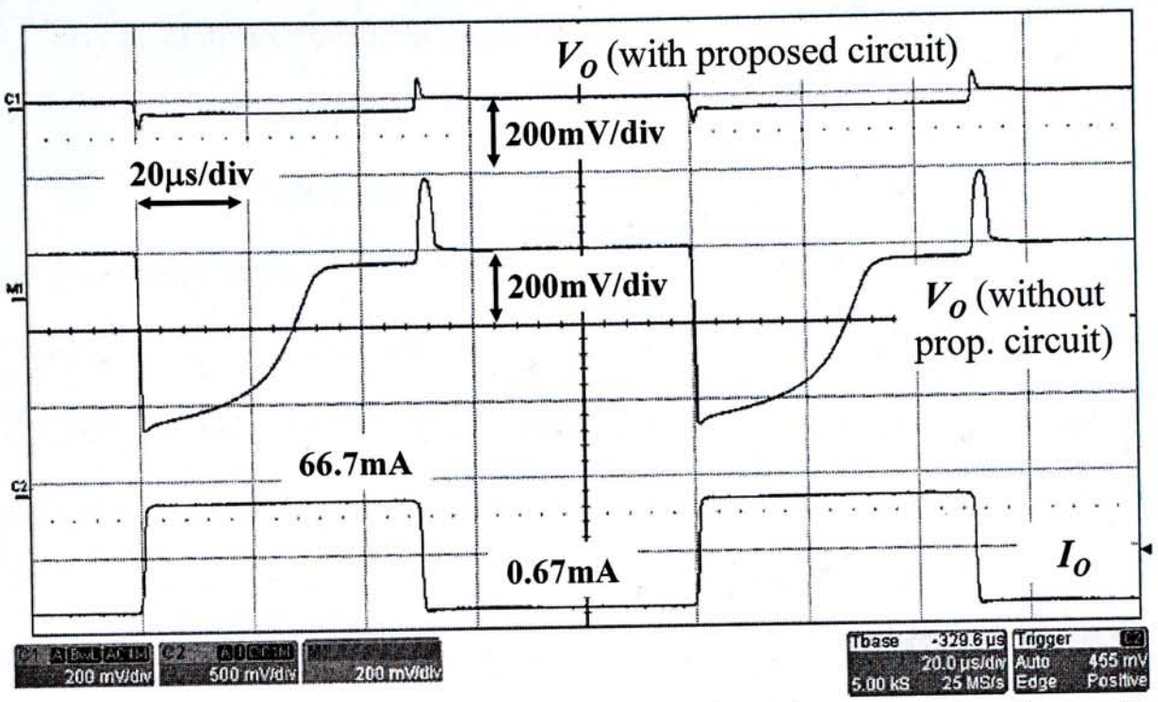


Fig. 3.13 Comparison of two LDOs with and without the proposed voltage-spike detection circuit, where V_{IN} = 1 V, V_O = 0.8 V, dI_O/dt = 66 mA/1 µs.

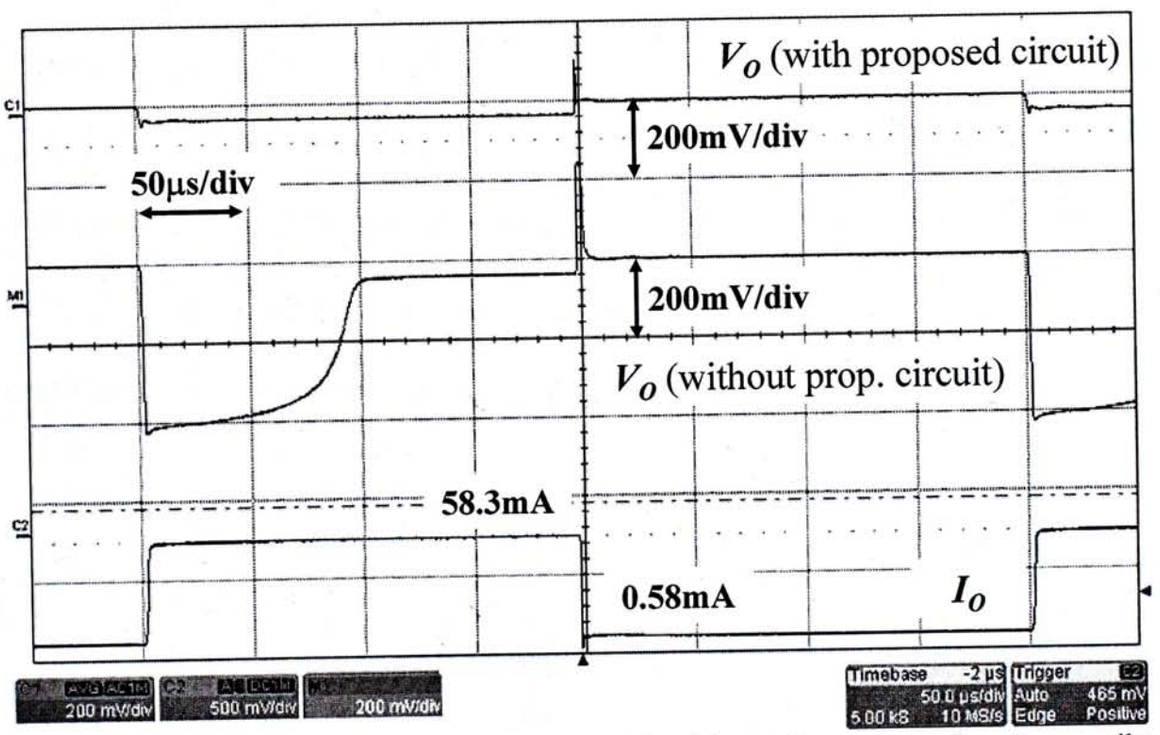


Fig. 3.14 Comparison of two LDOs with and without the proposed voltage-spike detection circuit, where V_{IN} = 0.95 V, V_O = 0.7 V, dI_O/dt = 57.7 mA/1 µs.

In Figs. 3.12, 3.13 and 3.14, the measurement results of the LDO with and without the proposed direct voltage-spike detection circuit at different V_{IN}, V_O and $I_{O(max)}$ are shown. There are three waveforms in each figure:

1. V_O of the LDO with the proposed voltage-spike detection circuit (top)
2. V_O of the LDO without the proposed voltage-spike detection circuit (middle)
3. I_O of both LDOs (bottom)

In all cases, I_O switches between the maximum and the minimum in 1 μs.

In Fig. 3.12, the measurement condition is V_{IN} = 1.4 V, V_O = 1.2 V and $I_{O(max)}$ = 100 mA. The quiescent current is 43 μA. The undershoot, the overshoot and the recovery time of the LDO without the proposed detection circuit are about 420 mV, 200 mV and 10 μs, respectively, while those of the LDO with the proposed circuit are about 70 mV, 70 mV and 3 μs only, respectively.

Similarly, in Fig. 3.13 (V_{IN} = 1 V, V_O = 0.8 V and $I_{O(max)}$ = 66.7 mA) and Fig. 3.14 (V_{IN} = 0.95 V, V_O = 0.7 V and $I_{O(max)}$ = 58.3 mA), the quiescent current in both cases is reduced to 19 μA and 14 μA, respectively. The SR_G-limit problem of the LDO without the proposed detection circuit becomes more obvious. The undershoot of V_O is about 420 mV, and the recovery time is more than 30 μs (Fig. 3.13) and about 100 μs (Fig. 3.14). However, the LDO with the proposed detection circuit at different conditions has no significant difference in the transient response.

Table 3.2 Summary of the measurement conditions of the LDO with the proposed voltage-spike detection circuit.

Input voltage V_{IN}	**Output voltage** V_O	**Max. output current** $I_{O(max)}$	**Quiescent current** I_Q	**Current efficiency** $I_O/(I_O + I_Q)$
1.4 V	1.2 V	100 mA	43 μA	99.957%
1 V	0.8 V	66.7 mA	19 μA	99.972%
0.95 V	0.7 V	58.3 mA	14 μA	99.976%

3.4 Conclusion of Chapter

This chapter presented a direct voltage-spike detection circuit to improve the transient response of the output-capacitorless LDO. The proposed detection circuit consists of two high-pass coupling capacitors, which are able to detect the fast-changing voltage spikes at the LDO output and adjust the bias current of the control circuit momentarily to improve both the small-signal and large-signal responses. The proposed circuit does not increase the quiescent current in the steady state, and it solves the narrow loop bandwidth and the slew-rate limit problems of the conventional LDO by applying a simple and effective modification to the LDO circuit. Moreover, the accuracy of the values of the added components is not important.

The measurement results have proven that the overshoot, the undershoot and the recovery time of the LDO have been improved significantly by the proposed voltage-spike detection circuit. Even though the threshold voltage of the power transistor is high, the input voltage of the LDO is lower than 1 V and the quiescent current is low.

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Chapter 4[†]

A LDO with Impedance Adjustment and Loop-Gain Boosting Technique

Introduction

Recently emerging low-voltage IC systems are driven heavily by rapid development of the semiconductor technology. However, power consumption of modern IC systems is not necessary to be low under a low supply voltage, since high chip density provides opportunities to include more and faster functionality into a chip. Hence, the power consumption, in contrast, is kept increasing. The growing trend of high power consumption of the modern IC systems working under low supply voltage implies that the current consumption is going to be large. When a LDO provides a regulated supply voltage to the low-voltage IC system, the high supply-current requirement makes the LDO design become extremely challenging since it is not easy to suppress the output voltage spikes (ΔV_O) of the LDO under rapid and large load transient changes (ΔI_T) during the switching between different operational modes of the IC system. General practice is to make use of a large off-chip capacitor at the LDO output (C_{OUT}) with low ESR (R_{ESR}), since a LDO has non-zero response time (T_r) which relates closely to the unity-gain frequency (UGF) of the LDO loop-gain response. A larger C_{OUT} is helpful to supply transient current to the load circuit when the LDO cannot respond to the rapid load changes. Moreover, a smaller RESR can reduce the transient voltage spikes significantly. In fact, the

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magnitude of the output voltage spike is approximately given by

$$\Delta V_O \approx \left(\frac{\Delta I_{OUT}}{C_{OUT}} \right) \cdot T_r + \Delta I_O R_{ESR} \tag{4.1}$$

Fig. 4.1 shows the typical load transient response of a LDO with a fixed C_{OUT}. The smallest voltage spikes among the three cases can be achieved by a faster LDO response and a smaller R_{ESR}. Moreover, the typical compensation strategy, as shown in Fig. 4.2, is dominant-pole compensation with single pole-zero cancellation. The zero (z_{ESR}) is generated by the ESR of C_{OUT} to cancel the non-dominant pole p_2 [1]. The dominant pole (p_{1A}) is inversely proportional to C_{OUT} [1]. When a larger C_{OUT} is used, the UGF is reduced and so the response time is degraded, since the dominant pole is shifted to a lower frequency (i.e. p_{1B}). As a result, including the concern of the cost and the physical size of the off-chip capacitor, C_{OUT} is suggested to be small to improve the response time, but it should be large enough to be able to achieve the stable closed-loop LDO operation simultaneously. In fact, when C_{OUT} is reduced, R_{ESR} has to be increased to generate the ESR zero at the same frequency to achieve an effective pole-zero cancellation (i.e. $z_{ESR} = 1/(C_{OUT}R_{ESR})$) [1]. It causes larger transient voltage spikes. Therefore, there is a contradiction between the stability and the transient-response improvement in the LDO design.

With regard to the above concerns, in this chapter, a 100-mA LDO compensated by an off-chip, low-ESR, nano-range output capacitor will be presented in Section 4.1. The goal of the design is to achieve a fast transient response with small voltage spikes. Section 4.2 will report the measurement results. Finally, a comparison with some recently reported LDO designs using a low-ESR capacitor will be given in Section 4.3.

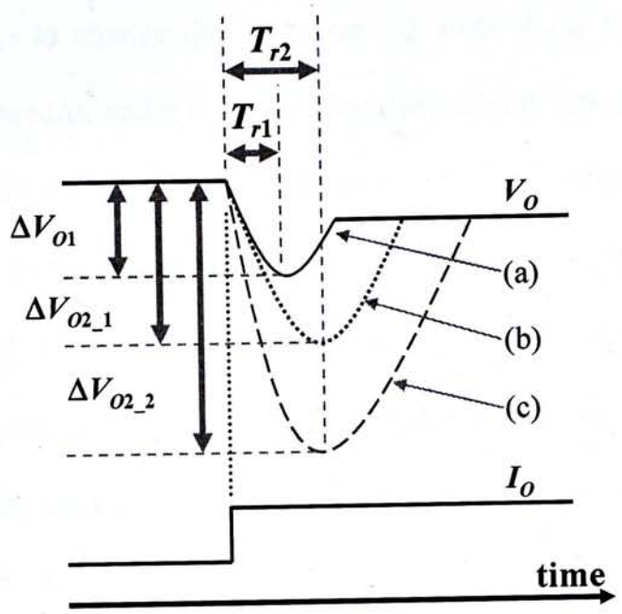


Fig. 4.1 Typical load transient responses of LDO (for a fixed C_{OUT}) with (a) a faster response and a lower-ESR capacitor (b) a slower response and a lower-ESR capacitor (c) a slower response and a larger-ESR capacitor.

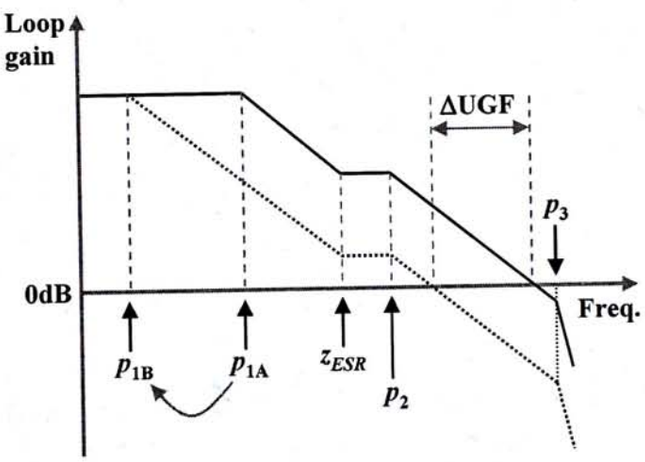


Fig. 4.2 Typical loop-gain responses with different output capacitances (the used ESR values in both cases are different to maintain the same z_{ESR} position).

4.1 Proposed LDO

The proposed LDO is shown in Fig. 4.3. It is formed by a LDO structure based on the flipped voltage follower, which has been analyzed in [5] in detail. In Fig. 4.3, M_{PT} is the power transistor, whereas M_{C1} is the common-gate error amplifier with a folded structure formed by M_{01}, M_{02} and M_{04} to have the output at node Y. This structure includes a load-tracking impedance adjustment circuit formed by the

diode-connected M_{07} to change the impedance at node Z for the use of low-ESR low-capacitance capacitor, and a loop-gain boosting circuit formed by M_{05} and M_{06}. Details of the proposed techniques will be analyzed later in this section. Similar to the design reported in [5], a control-voltage generator (i.e. to generate V_X to define the gate voltage of M_{C1}) is formed by M_{A1}–M_{A7} and M_{C2}. The simple setup composed of the reference voltage (V_{REF}), R_B and a diode-connected M_{B1} provides the bias current to the whole circuit. It is noted that C_B is a filtering capacitor to keep the bias current away from the effects of the coupling signals and noise.

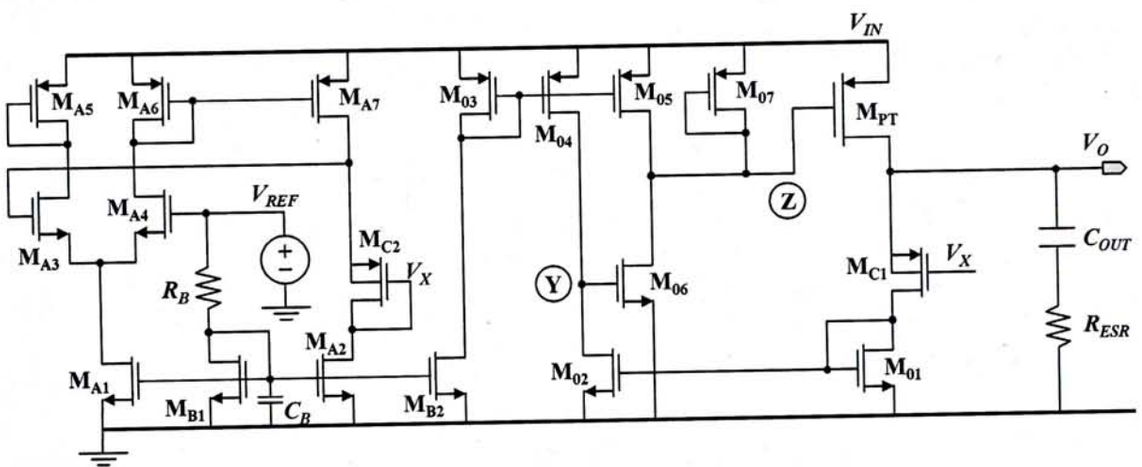


Fig. 4.3 Proposed LDO structure.

Based on the analysis reported in [5], there are totally three left-half-plane (LHP) poles and one LHP zero (the ESR zero). When referring to the ultimate goal to use a low-ESR capacitor for improving the transient response, one of the non-dominant poles and the ESR zero are located after the UGF due to the low ESR value, and so they can be neglected in the analysis. Finally, the dominant pole of the proposed LDO is given by [5]

$$p_1 = \frac{1}{C_{OUT}\left[\left(r_{oPT} \,//\, \frac{1}{g_{mC1}}\right)\right]} \tag{4.2}$$

where r_{oPT} is the drain resistance of M_{PT} and g_{mC1} is the transconductance of M_{C1}.

There is only one non-dominant pole left in the proposed design. It is given by [5]

$$p_2 = \frac{1}{\left\{C_{gsPT} + C_{gdPT}\left[1 + g_{mPT}\left(r_{oPT} \,//\, \frac{1}{g_{mC1}}\right)\right]\right\}\left(r_{o5} \,//\, r_{o6} \,//\, \frac{1}{g_{m7}}\right)} \tag{4.3}$$

where C_{gsPT} and C_{gdPT} are the gate-to-source and gate-to-drain parasitic capacitances of M_{PT}, respectively. Since M_{PT} is not small, both C_{gsPT} and C_{gdPT} cannot be neglected in the analysis. From (4.3), it is found that p_2 relates to the transconducatance of M_{07} (i.e. g_{m7}). When referring the connection of M_{07} in Fig. 4.3, it detects the source-to-gate voltage of M_{PT} directly. As a result, the drain current of M_{07} is proportional to I_O, and this makes p_2 located at a higher frequency when I_O increases.

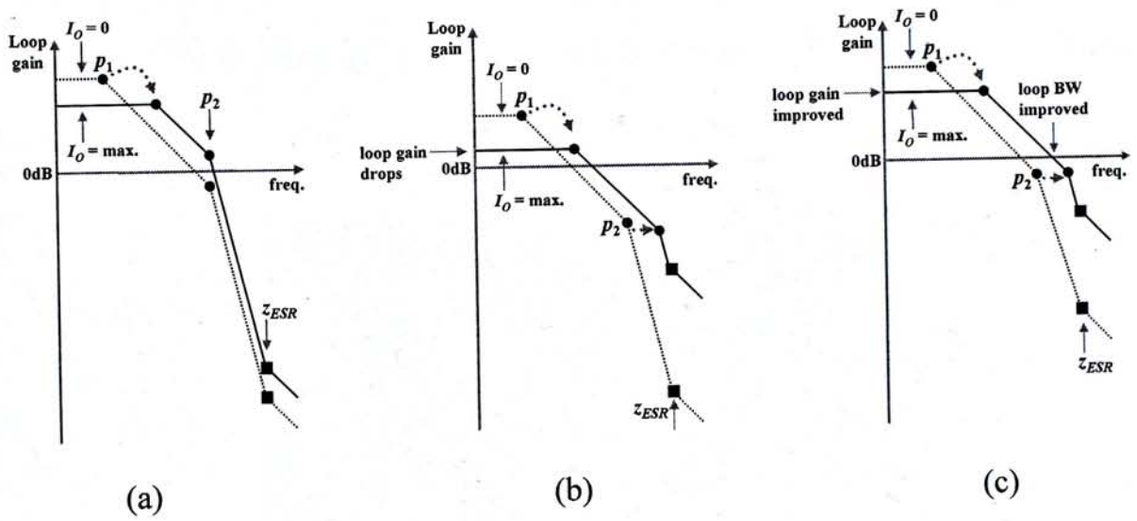
Fig. 4.4(a) shows the conceptual diagram of the loop-gain response without M_{07}. When I_O increases, the output resistance of the LDO decreases and so the loop gain is reduced for higher I_O. Moreover, according to (4.2), p_1 is shifted to a higher frequency, while p_2 remains unchanged if M_{07} is not included in the design. As a result, both p_1 and p_2 are located before the loop-gain UGF, and the LDO is not absolutely stable within the full range of I_O.

However, as shown in Fig. 4.4(b), the overall loop gain is dramatically reduced due to the impedance reduction by the diode-connected M_{07}. Thus, M_{05} and M_{06} are added to compensate the loop-gain loss. As a result, the loop gain is given by $-g_{mp}(r_{oPT}//g_{mC1}^{-1})g_{mC1}(r_{o2}//r_{o4})g_{m6}(r_{o5}//r_{o6}//g_{m7}^{-1})$, and so the UGF is given by

$$\text{UGF} = \frac{g_{mp}g_{mC1}g_{m6}\left(r_{o2} \,//\, r_{o4}\right)\left(r_{o5} \,//\, r_{o6} \,//\, g_{m7}^{-1}\right)}{C_{OUT}} \tag{4.4}$$

As shown in Fig. 4.4(c), both the loop gain and the UGF are improved. The condition to select the value of C_{OUT} is to ensure p_2 always locating after the UGF in the maximum I_O condition. The design of the gate size of M_{06} is important so that the

parasitic effect at node Y will not generate a pole locating before the loop-gain UGF. From a circuit simulation, it is found that r_{o2} = 2.19 MΩ, r_{o4} = 1.86 MΩ and C_{g6} = 38.84 fF. The pole at Y is located at 4.07 MHz which is higher than the UGF of about 1 MHz. This result shows that the pole created at node Y does not affect the phase margin of the loop gain.



(a) (b) (c)

Fig. 4.4 Conceptual diagrams of the loop-gain responses when (a) without M_{07} (b) with M_{07} and without M_{05} & M_{06} (c) with M_{05}, M_{06} and M_{07}.

Moreover, the large-signal response of the proposed LDO is not a limiting factor to the response speed in this design, since the slew rate at node Z (due to the large gate capacitance of M_{PT}) is not limited in this structure. When V_O is deviated from the preset value, the gate voltage of M_{PT} will be adjusted by the feedback. M_{05} and M_{06} are responsible to drive the gate capacitance of M_{PT} to achieve the adjustment. Since the pole created at node Y should be at a high frequency to ensure the closed-loop stability, the size of M_{06} is not large. However, the dynamic discharging current by M_{06} is not small, as it is now mainly determined by its gate-to-source voltage which has a dynamic range between $V_{IN} - V_{SD04(sat)}$ and $V_{DS02(sat)}$. Thus, the discharging of node Z is not a problem towards the response time of the proposed LDO. On the

charging side, the extra current from M_{07} does help the transient response at node Z. Due to the above considerations, the design of the steady-state bias current for M_{05} and M_{06} does not need to be high.

4.2 Experimental Results

The proposed LDO is implemented in austriamicrosystems (AMS) 0.35-μm 2-poly 4-metal CMOS Technology. The micrograph is shown in Fig. 4.5, and the chip area is 250 μm × 128 μm (0.032 mm^2), excluding the test pads.

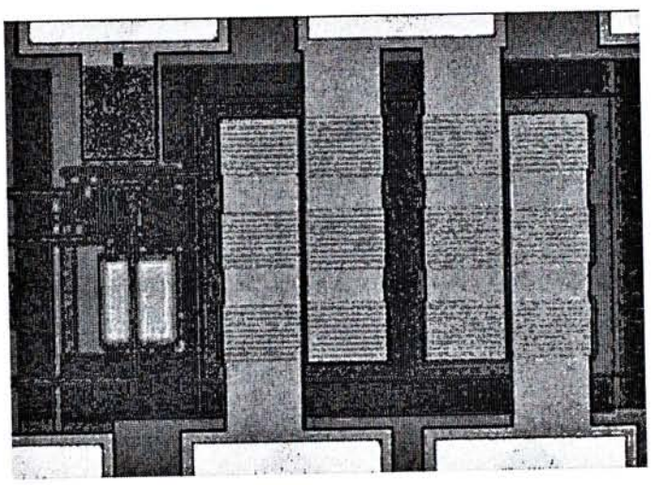


Fig. 4.5 Chip micrograph of the proposed LDO.

A summary of the LDO specifications is listed in Table 4.1. The threshold voltages of the NMOSFET and the PMOSFET in the used technology are about 0.5 V and -0.65 V, respectively. The LDO regulates the output voltage at 1.2 V from a supply ranging from 1.5 to 3 V, whereas the load current is from 0 to 100 mA. As will be proven by the measured load transient responses shown in Figs. 4.7 to 4.12, the proposed LDO is stable when C_{OUT} = 100 nF, and it is also stable in a wide range of C_{OUT} ranging from 100 nF to 10 μF. The ESR of the used capacitors are tabulated in Table 4.2 and are in the order of tens or several mΩ. This shows the stability of the proposed LDO does not need the help from the ESR zero.

Table 4.1 A brief summary of the proposed LDO specifications.

Technology	AMS CMOS 0.35-μm 2P4M
V_{THN}, V_{THP}	about 0.5 V, -0.65 V
Power-transistor size	9000 μm/0.35 μm
Chip area	250 μm × 128 μm
C_{OUT}	100 nF – 10 μF

Table 4.2 Measured stable range of C_{OUT} and ESR.

C_{OUT}	**Intrinsic ESR**	**Added ESR**
100 nF	23 mΩ	0.1 – 0.5 Ω
150 nF	15 mΩ	
200 nF	11.7 mΩ	
2.2 μF	5.1 mΩ	
4.7 μF	2.5 mΩ	
10 μF	2.4 mΩ	

Fig. 4.6 presents the quiescent current (I_Q) against the output current. In no-load condition, the LDO consumes 26 μA only. At the maximum output current (i.e. I_O = 100 mA), although a higher bias current is used for impedance reduction by M_{07}, I_Q remains below 70 μA.

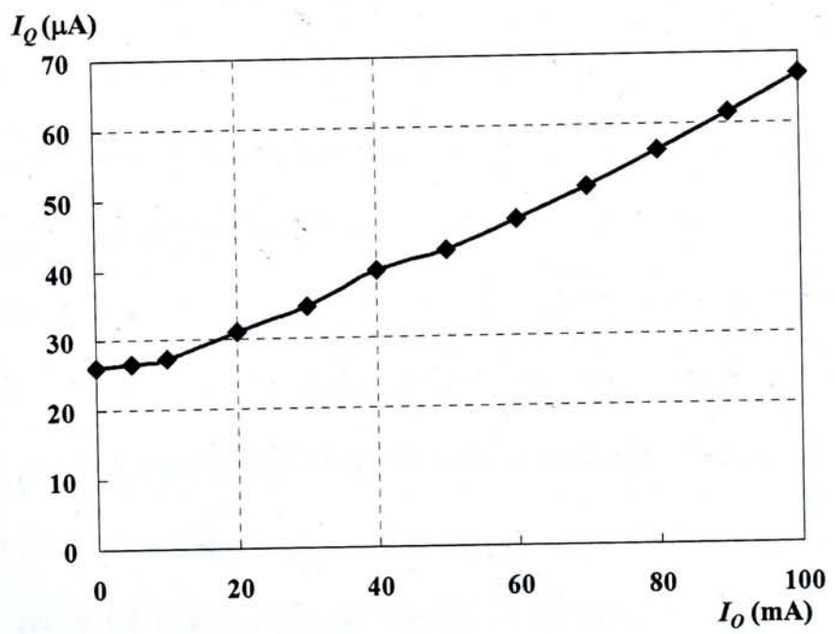


Fig. 4.6 Relationship between I_Q and I_O.

Some measured load transient responses of the proposed LDO are shown in Figs. 4.7 and 4.12. They are

1. Fig. 4.7: C_{OUT} = 100 nF, I_O = 0 – 100 mA
2. Fig. 4.8: C_{OUT} = 200 nF, I_O = 0 – 100 mA
3. Fig. 4.9: C_{OUT} = 4.7 μF, I_O = 0 – 100 mA
4. Fig. 4.10: C_{OUT} = 100 nF, I_O = 1 mA – 100 mA
4. Fig. 4.11: C_{OUT} = 200 nF, I_O = 1 mA – 100 mA
5. Fig. 4.12: C_{OUT} = 4.7 μF, I_O = 1 mA – 100 mA

Both cases of I_O = 0 – 100 mA and I_O = 1 mA – 100 mA are included, as load regulation cannot be accurately observed in the cases of I_O = 0 – 100 mA. The reason is that the overshoot of V_O causes C_{OUT} overcharged, but C_{OUT} is not able to be discharged by the LDO internally due to the low bias current. The cases of 1 mA – 100 mA are included to observe the load regulation of the design. Moreover, in all measurements, I_O is switched between 0 (or 1 mA) and 100 mA within 100 ns.

In Fig. 4.10, when the LDO is connected with a 100-nF output capacitor, it shows stable operation with response time faster than 0.2 μs. The undershoot and the overshoot of V_O are 30.3 mV and 44.9 mV, respectively. The load regulation is 8 mV/99 mV. The fast response time of 0.2 μs implies the loop-gain UGF is high, but it is the boundary condition of stability (since slight ringing is observed). When a 200-nF is used (Fig. 4.11), the response time is slightly more than 0.2 μs, but it shows better stability (no ringing). The voltage spikes are similar to the case using a 100-nF capacitor. This proves the design consideration for C_{OUT} stated in Section 4.1.

Fig. 4.9 and Fig. 4.12 are the transient responses when using a 4.7-μF capacitor. The voltage spikes are reduced to about 20 mV, as the larger capacitor provides more transient current to the load. However, a larger capacitor degrades the response time, as the loop-gain UGF is reduced significantly. The proposed design makes a 100-nF capacitor sufficient to achieve fast response and small voltage spikes simultaneously.

Finally, the stability of the proposed LDO is tested with an added ESR ranging from 0.1 to 0.5 Ω. It is verified that the LDO is perfectly stable in all cases. When C_{OUT} is small (i.e. 100 nF, 200 nF, etc.), the ESR zero locates after the loop-gain UGF. However, it still has slight effect to cancel p_2, and so, for the case of using a 100-nF capacitor, the slight ringing vanishes when the added ESR is ranging from 0.1 to 0.5 Ω. Moreover, when C_{OUT} is in the order of μF, the UGF is reduced so that the ESR zero does not affect stability since it is located far behind the UGF.

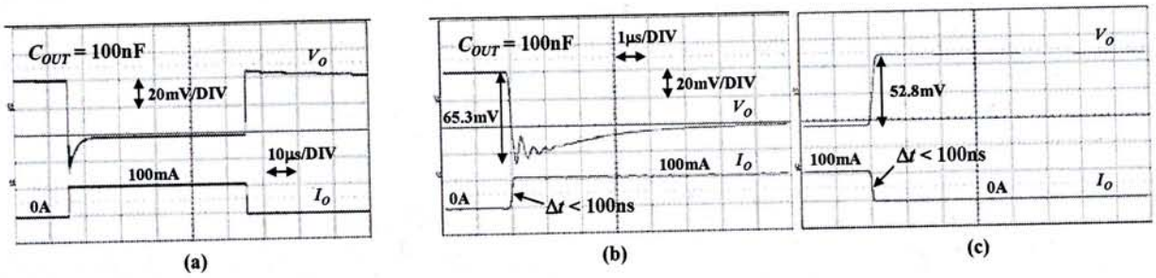


Fig. 4.7 Measured load transient response for V_{IN} = 1.5 V, V_O = 1.2 V, I_O = 0 to 100 mA, C_{OUT} = 100 nF, added R_{ESR} = 0 (a) full view (b) zoom-in view of the undershoot (c) zoom-in view of the overshoot.

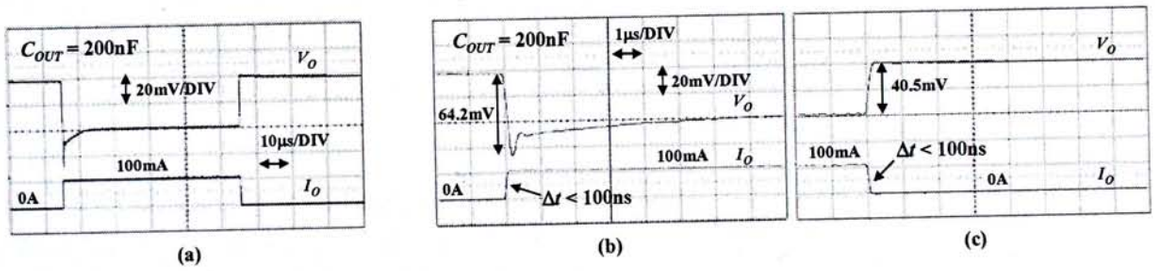


Fig. 4.8 Measured load transient response for V_{IN} = 1.5 V, V_O = 1.2 V, I_O = 0 to 100 mA, C_{OUT} = 200 nF, added R_{ESR} = 0 (a) full view (b) zoom-in view of the undershoot (c) zoom-in view of the overshoot.

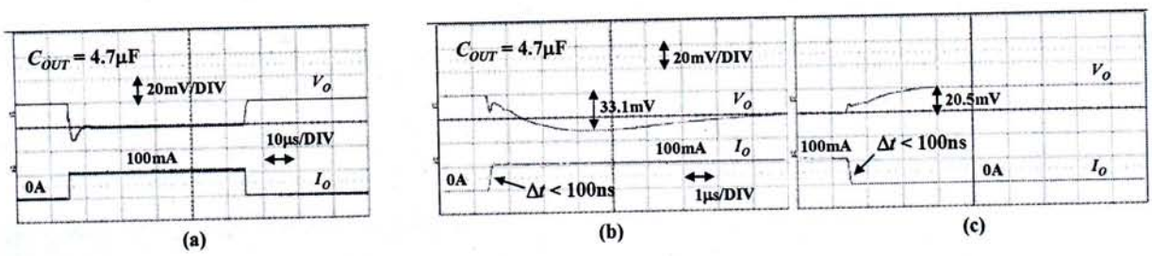


Fig. 4.9 Measured load transient response for V_{IN} = 1.5 V, V_O = 1.2 V, I_O = 0 to 100 mA, C_{OUT} = 4.7 μF, added R_{ESR} = 0 (a) full view (b) zoom-in view of the undershoot (c) zoom-in view of the overshoot.

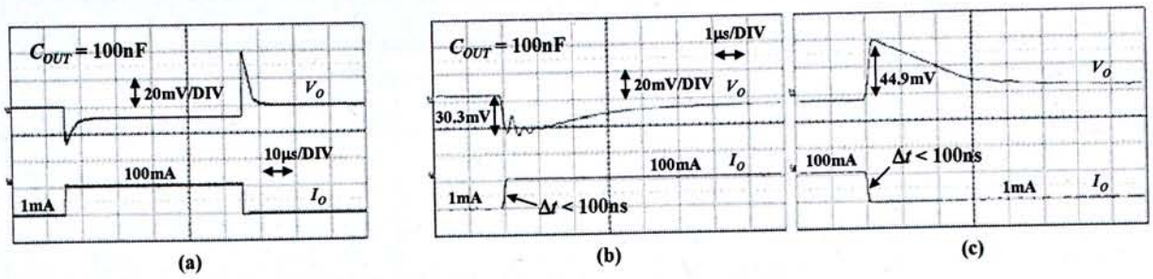


Fig. 4.10 Measured load transient response for V_{IN} = 1.5 V, V_O = 1.2 V, I_O = 1 mA to 100 mA, C_{OUT} = 100 nF, added R_{ESR} = 0 (a) full view (b) zoom-in view of the undershoot (c) zoom-in view of the overshoot.

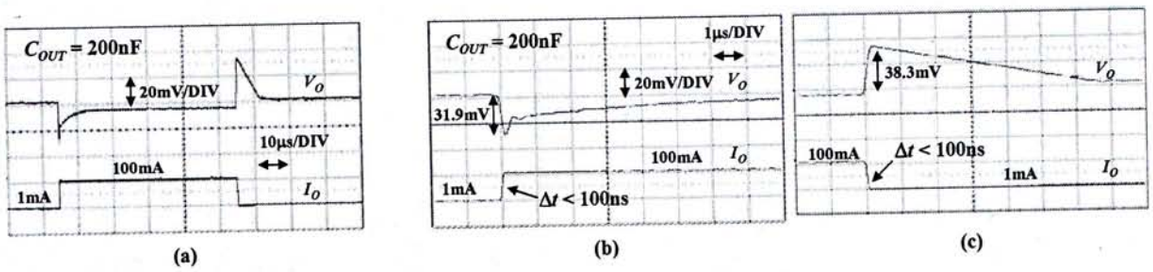


Fig. 4.11 Measured load transient response for V_{IN} = 1.5 V, V_O = 1.2 V, I_O = 1 mA to 100 mA, C_{OUT} = 200 nF, added R_{ESR} = 0 (a) full view (b) zoom-in view of the undershoot (c) zoom-in view of the overshoot.

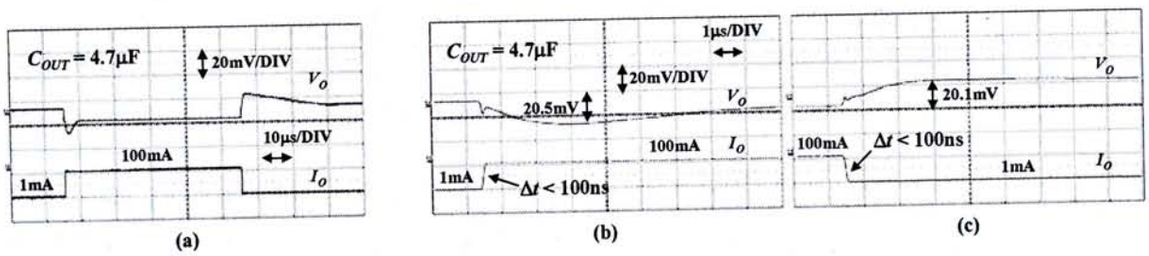


Fig. 4.12 Measured load transient response for V_{IN} = 1.5 V, V_O = 1.2 V, I_O = 1 mA to 100 mA, C_{OUT} = 4.7 μF, added R_{ESR} = 0 (a) full view (b) zoom-in view of the undershoot (c) zoom-in view of the overshoot.

4.3 Comparison

Some reported LDO designs utilizing low-ESR capacitor is summarized in Table 4.3. For the designs reported in [2]–[5], the minimum value of the off-chip capacitor is 1 μF, but the proposed LDO can be stabilized by a 100-nF capacitor. The quiescent current and the voltage spikes of the proposed design are not large when comparing to the others. Finally, the proposed LDO has the fastest response time of 0.2 μs.

Table 4.3 Comparison of some selected LDO designs using a low-ESR capacitor.

	[2]	[3]	[4]	[5]**	This work
Technology	CMOS 0.35-μm	CMOS 0.35-μm	CMOS 0.35-μm	CMOS 0.35-μm	CMOS 0.35-μm
V_{IN}	2 – 5 V	2 – 5.5V	2 V	1.2 – 1.5 V	1.5 – 3 V
I_Q	53 μA	20 μA	27 μA	95 μA	26 μA
C_{OUT}	1 μF	1 μF	1 μF	1 μF	0.1 μF
R_{ESR}	300 mΩ	low *	low *	16 mΩ	23 mΩ
ΔI_O	150 mA	200 mA	150 mA	50 mA	99 mA
ΔV_O	130 mV	54 mV	<70 mV	37 mV	44.9 mV
Measured T_r	~1.2 μs	NA ***	~0.4 μs	~0.8 μs	~0.2 μs

* The actual value is not available.

** Among the reported results in [5], C_{OUT} = 1 μF is the minimum capacitor value with low ESR to stabilize the LDO circuit.

*** Measured response time is not available.

4.4 Conclusion of Chapter

A low-voltage fast-response small-voltage-spike LDO with load-tracking impedance adjustment and loop-gain boosting technique has been presented in this chapter. It has been proven that it can be stabilized by an off-chip, low-ESR, nano-range capacitor. The design is suitable for low-voltage high-current applications.

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Chapter 5

Conclusion and Future Work

In this thesis, the PSRR of a conventional LDO and two proposed fast-transient LDOs for SoC applications has been introduced, analyzed and developed.

For the PSRR analysis, the poles and zeros of the LDO have been investigated from the transfer function of the proposed modeling. Several design parameters affecting the PSRR have been studied in detail. It is concluded that higher output resistance of the error amplifier provides a better PSRR at low frequency, but it would degrade the PSRR in the moderate frequency range seriously. In addition, a higher gain of the error amplifier and a smaller ESR can help improving the PSRR. To be more specific, a larger amplifier gain could obtain a better PSRR at low to moderate frequency, while a smaller equivalent series resistance could achieve PSRR enhancement at moderate to high frequency. It is also found from the analysis that the worst PSRR happens at maximum I_O.

After the PSRR discussion, the proposed LDO without an output capacitor has been discussed. The direct voltage-spike detection circuit has been introduced to improve the transient response of the output-capacitorless LDO. The simple detection circuit only consists of two high-pass coupling capacitors to detect the fast-changing voltage spikes at the LDO output and adjust the bias current of the control circuit momentarily to improve both the small-signal and large-signal responses. The proposed circuit does not increase the quiescent current in the steady state, and it solves the narrow loop bandwidth and the slew-rate limit problems of the conventional LDO by applying a simple and effective modification to the LDO

circuit. Moreover, the accuracy of the values of the added components is not important. The measurement results have proven that the overshoot, the undershoot and the recovery time of the LDO have been improved significantly by the proposed voltage-spike detection circuit. Even though the threshold voltage of the power transistor is high, the input voltage of the LDO is lower than 1 V and the quiescent current is low.

Finally, the proposed LDO with a low-ESR output capacitor is discussed. With the proposed load-tracking impedance adjustment, the gate of the power transistor decreases greatly which enables the use of small output capacitor with small ESR. Moreover, the loop-gain boosting technique has been added to raise the overall loop gain of the circuit and enhance the transient response. From the experimental results, it has been proven that the proposed LDO can be stabilized by an off-chip, low-ESR, nano-range capacitor.

The future work is to further investigate the gain-boosting technique on improving the stability of the LDO against process variations.