CMOS Power Amplifier and Transmitter Front-End Design in Wireless Communication

NG, Yuen Sum

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Abstract

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CMOS Power Amplifier and Transmitter Front-End Design in Wireless Communication

Submitted by **NG, Yuen Sum**

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In the recent years, radio-frequency (RF) front-end circuit design is a hot and challenging topic in both the industry and research. RF transceivers with different standards are integrated into a single chip. Different technologies, for example, SiGe bipolar or GaAs are chosen in some research works due to the high transition frequency, high breakdown voltage, high voltage supply and high DC current limitation. Nowadays, CMOS technology is another choice to implement RF front-end with the submicron or even the nano-scale channel length. Some of the RF front-end building blocks, such as low-noise amplifier (LNA) and mixer, can be implemented in CMOS technology due to the down-scaling of the channel length. Although CMOS technology suffers from higher threshold voltage, lower breakdown voltage, and lower supply voltage compared with the non-CMOS technologies mentioned above, CMOS is relatively inexpensive and more feasible to integrate the RF circuit with the digital part. Among other building blocks of the RF front-end circuit, power amplifier (PA) consumes the most power. In order to have high power efficiency, the PA is usually implemented by offchip active and passive components. However, this approach causes the production cost increase dramatically. Therefore, the development of on-chip PA is, so far, a proper choice to reduce the production cost.

In this thesis, the design consideration of PA and transmitter front-end circuit is outlined. A PA operating at 3 GHz under the supply voltage of 3.3 V is fabricated in a 0.18 μm RF CMOS technology. The PA can provide saturated power of 20 dBm with the input power of -12 dBm, according to measurement. Measured linear gain and power-added efficiency are 27.89 dB and 12%, respectively. The PA is also measured with IEEE 802.11a Wireless LAN and IEEE 802.16 WiMAX data. The measured EVM are -30.3 dB with an output power of 7.79 dBm and -26.4 dB with an output power of 8.73 dBm, respectively.

The transmitter front-end circuit for the WiMAX applications, including on-chip PA, has been fabricated by a 0.18 μm RF CMOS technology with the frequency band of 2.5 GHz. The transmitter is measured under 3.3 V for the power stage, 1.27 V for the driver stage and 1.5 V for the I/Q modulator. In the measurement, the circuit can provide output saturated power of 20 dBm, with linear gain of 24 dB and power-added efficiency of 14 %. This research work is tested using with 20-MHz bandwidth, 64-QAM-5/6-CTC WiMAX baseband signal corresponding to output power of 13 dBm associated with error vector magnitude of -30.52 dB.

概要

近年, 射頻前端綫路設計無論在工業還是科研都是一個熱門項目. 不同制式的射頻收發器建立在單晶片上. 不同工藝如 SiGe 三極管及 GaAs 可以用於射頻前端綫路, 因爲這些工藝都具有高過渡頻率高臨界極限, 高供電與高電承受能力. 近期, CMOS 工藝成爲了另一個射頻前端綫路設計的方法. 一些在接收器上的模組如低燥音放大器都有應用 CMOS 工藝生成. 雖然 CMOS 工藝的缺點有高限極, 低臨界極限, 低電流承受能力, 但 CMOS 工藝的價格較低與較容易同數碼世界結合. 而在眾多射頻前端的模塊中, 功率放大器是最消耗電能的. 所以功率放大器多是用外置電子零件來設計. 但是製造成本就會因此上升. 所以, 把功率放大器設計在 CMOS 工藝上是另一個可以節省成本的方法之一.

在這篇論文中, 會談及有關功率放大器以及發訊器的前端綫路設計. 首先, 一個以 3.3 V 作爲工作電壓及 3 GHz 爲工作頻律的功率放大器已經用 0.18 微米制程設計並且製造. 在測試中可以得知這個功率放大器可以發出 20 dBm 電能. 而它的綫性發大率爲 27.89 dB 以及附加功率效率爲 12 %. 同時也有用 IEEE 802.11a 無綫網路制式以及 IEEE WiMAX 制式測驗. 結果顯示在這兩個制式中, 這個功率放大器可以分別在發出 7.79 dBm 時 EVM 值是-30.3 dB 以及 8.73 dBm 電能時 EVM 值是-26.4 dB.

此外, 一個發訊器前端, 包括一個功率放大器, 也用了 0.18 微米制程設計並且製造. 這個發訊器前端是用於 2.5 GHz 頻帶 WiMAX 的應用上. 功率放大器的工作電壓爲 3.3 V, 前級放大器的工作電壓爲 1.27 V, 而 I/Q 混頻器的工作電壓爲 1.5 V. 在測試中, 這個發訊器前端可以提供 20 dBm 電能. 綫性放大率爲 24 dB 以及以及附加功率效率爲 14 %. 這個電路也有用 WiMAX 制式的基頻訊號測試, 結果以 20 MHz 64-QAM-5/6-CTC WiMAX 的基頻訊號中, 可提供 13 dBm 電能而 EVM 值是-30.52 dB

Acknowledgements

I want to specially thank to my supervisor, Professor Leung Ka Nang Alex, who provides me full support of my work. I am grateful for the help from Dr. Siu-Kei Tang who gave me a lot of guidelines on PCB layout techniques for the RF front-end circuit testing. In addition to the testing boards, I want to specially thank again Dr. Tang and Dr. Lincoln Lai Kan Leung who gave me a lot of technical advices on the circuit-level design and measurement skills. Furthermore, I want to specially thank Mr. Yeung Wing Yee who gave me a lot of technical supports on the all the simulation and layout CAD tools. Finally, I want to thank my colleagues in ASIC and Microwave Laboratories for their supports.

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1. Introduction

1.1 Motivation

Radio-frequency integrated circuit (RFIC) design becomes a hot topic on both the research and industry recently, because of the maturity of the sub-micron and nano-scale semiconductor technologies. Based on those technologies, there are many commercial products which were designed based on different standards to cater the consumer market. Some examples are GSM, Bluetooth, Wireless LAN and WiMAX, etc.

Regarding to the recent trend, some RF-front end circuits, either the receiver or the transmitter, are implemented by GaAs (Gallium arsenide), BiCMOS or silicon bipolar technologies. On the transmitter side, the front-end circuit including the power amplifiers and mixers are implemented by the afore-mentioned non-CMOS components due to high supply voltage and high breakdown voltage in order to deliver high output power. However, there are over 80 % semiconductor products manufactured by CMOS technology due to that fact that most of them are digital circuits. It is well-known that CMOS technology has many advantages such as low threshold voltage to enable low operational supply voltage. The low supply voltage can reduce the power consumption in the digital circuit. But it is not beneficial to the both the analog and RF IC design, as the voltage swing and output power delivery are limited and cascode structures may not be a good design technique. As a result, with GaAs, BiCMOS and SiGe bipolar technologies are better choice in implement analog and RF circuit as they have high supply voltage and current density limitation. However, these non-CMOS technologies are relatively much more expensive compared with the CMOS counterpart.

Therefore, most of the RF building blocks which can be analyzed in small signal domain, such as low noise amplifier (LNA), mixer, intermediate frequency (IF) filters and data conversion blocks, are designed using CMOS technology. Power Amplifier (PA), however, is required to deliver high output

power. It is not significantly benefited by the advanced sub-micron CMOS technology with the shortcomings mention above. As a result, special techniques are required to overcome these problems.

In addition to the supply voltage and current density limitation, CMOS technologies also suffer from poor quality factor of the monolithic passive components. The on-chip inductors generally have low the quality factor of about 8-10. The on-chip parasitic capacitance and resistance degrade their performance.

In the PA design, the output power, the efficiency and the linearity are the most important parameters. Switching PA could have good efficiency but poor linearity. Therefore, the communication standard with only phase and frequency modulation should use switching PA, e.g. GSM and Bluetooth. Nowadays, some new communication standards incorporate the orthogonal frequency division multiplexing (OFDM) is used for higher data rate transmission and multiple access, but the linearity requirement is high. IEEE 802.11 a/g wireless LAN, IEEE 802.16e Mobile WiMAX and Ultra-Wideband (UWB) are examples of using the OFDM scheme. All of them require the PA having good linearity, but the efficiency of a PA with good linearity is generally low.

This thesis would focus on the design in PA to provide high output power from a low supply voltage and high knee voltage in CMOS technology. In additional to the PA, the design of a transmitter front-end circuit with on-chip integrated PA is also discussed.

1.2 Specifications

Both the PA and transmitter front-end circuit are designed for the IEEE 802.16e Mobile WiMAX applications. It is based on OFDM in order to have high data rate transmission. OFDM system can also prevent inter-block interference (ISI). Mobile WiMAX incorporates orthogonal frequency division multiple access (OFDMA) which enable Multiple-Input-Multiple-Output (MIMO). In order to deliver optimum performance in channel bandwidth, the parameter in the physical layer is scalable. The

channel bandwidth is ranged from 1.25 MHz to 20 MHz [2]. The frequency bands [3] and the bandwidth requirement are shown in Table 1-1 and Table 1-2, respectively. WiMAX devices operates at 2.3-2.4 GHz, 2.305-2.320 GHz, 2.345-2.36 GHz, 2.496-2.69 GHz, 3.3-3.4 GHz, 3.4-3.8 GHz, 3.4-3.6 GHz and 3.6-3.8 GHz.

Table 1-1 Frequency bands for WiMAX standards [1]

Band Class Index	Frequency Range (GHz)	Channel Frequency Step (kHz)	Channel Bandwidth (MHz)	FFT sizes	Duplexing Mode
1	2.3-2.4	250	5	512	TDD
			10	1024	TDD
2	2.305-2.320 2.345-2.360	250	3.5	512	TDD
			5	512	TDD
			10	1024	TDD
3	**2.496-2.69**	**250**	**5**	**512**	**TDD**
			10	**1024**	**TDD**
4	3.3-3.4	250	5	512	TDD
			7	1024	TDD
			10	1024	TDD
5	3.4-3.8	250	5	512	TDD
			7	1024	TDD
			10	1024	TDD
	3.4-3.6	250	5	512	TDD
			7	1024	TDD
			10	1024	TDD
	3.6-3.8	250	5	512	TDD
			7	1024	TDD
			10	1024	TDD

As there are several frequency bands available in the standard, the design target is for specific frequency band that are needed to set first. The frequency band for Band Class Index 3 is chosen as the design target. It is because there are many publications [4] - [7] about the WiMAX applications for comparison.

Table 1-2 Bandwidth requirement of WiMAX standard [3]

Parameters	Values						
System bandwidth (MHz)	1.25	5	10	20	3.5	7	8.75
Sampling factor	28/25				8/7		
Sampling frequency (Fs MHz)	1.4	5.6	11.2	22.4	4	8	10
Sample time (1/Fs nsec)	714.3	178.6	89.3	44.6	250	125	100
FFT sizes	128	512	1024	2048	512	1024	1024
Subcarrier frequency spacing (kHz)	10.9375				7.8125		9.765625
Useful symbol time	91.4				128		102.4
Guard time	11.4				16		12.8
OFDMA symbol time	102.8				144		115.2

As WiMAX is an OFDM system, its linearity requirement is high. Switching PA is not a candidate for this application. PA is designed in the linear operation mode. The detailed analysis will be described in Chapter 2. The Error Vector Magnitude (EVM) is the major parameter in order to analyze the linearity of the OFDM system. The detailed definition will be shown in Chapter 2 also. The EVM requirement for the WiMAX system varies based on different modulations and coding schemes. Table 1-3 shows the EVM requirement needed. For the 64-QAM modulation with 5/6 coding, the EVM of the transmitter must be below 30 dB.

Table 1-3 Uplink modulation requirement

Modulation	EVM value required / dB
QPSK 1/2	<= -15
QPSK 3/4	<= -18
16-QAM 1/2	<=- 20.5
16-QAM 3/4	<=-24
64-QAM 1/2	<=-26
64-QAM 2/3	<=-28
64-QAM 3/4	<=-30
64-QAM 5/6	<=-30

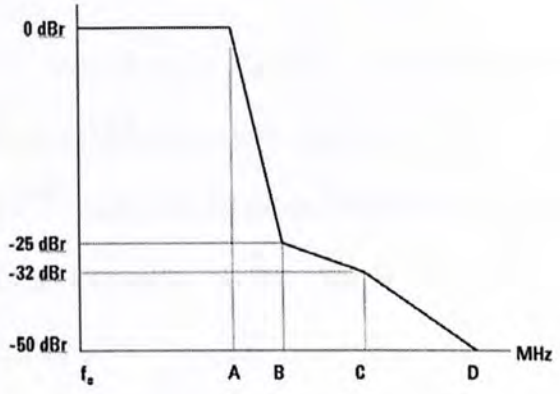
The Power Class requirement is shown in Table 1-4. There are 4 power classes in the WiMAX standards. For the low output power class, such as power class 1, it may be implemented by the CMOS

technology. For the higher output power, CMOS technology may not be a good candidate as power combining technique are required and it is quite hard to design. So, an offchip PA may be used.

Table 1-4 Power control requirement for WiMAX standard [2]

Class Identifier	Transmit Power (dBm) for 16-QAM	Transmit Power (dBm) for QPSK
Power Class 1	18 <= PTx,max < 21	20 <= PTx,max < 23
Power Class 2	21 <= PTx,max < 25	23 <= PTx,max < 27
Power Class 3	25 <= PTx,max < 30	27 <= PTx,max < 30
Power Class 4	30 <= PTx,max	30 <= PTx,max

In addition to the power and EVM requirement, the OFDM output spectrum should meet the spectrum mask requirement as shown in Fig. 1.2-1. The spectrum mask requirement depends on the channel bandwidth [9].



Channelization (MHz)	A	B	C	D
20	9.5	10.9	19.5	29.5
10	4.75	5.45	9.75	14.75

Fig. 1.2-1 Spectrum mask for different Channel bandwidth

As a result, this work will focus on the frequency band of 2.496-2.69 GHz. The center frequency is set to be 2.5 GHz. This work is implemented by a 0.18-μm RF CMOS technology. For the down-scaling technology, the supply voltage is quite low and there is only 3.3 V in the thick-oxide option in the

technology. Loadpull design technique can be applied to extract more output power from the low supply voltage. The design technique and effect would be discussed in Chapter 3 and Chapter 4.

1.3 Organization of the Thesis

This thesis will be presented in six chapters. In Chapter 2, the basic theory and the figure-of-merit of a PA would be discussed. In Chapter 3, a prototype PA is designed. Its center frequency is set to be 3-GHz. The loadpull technique would be addressed. All the design and the measurement result will be outlined. In Chapter 4, the design of a 2.5-GHz transmitter front-end circuit for WiMAX applications is presented. All the circuit-level design and measurement result would be given. Finally, the conclusion and the future work will be shown in Chapter 5 and Chapter 6, respectively.

1.4 References

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[8] Agilent, "WiMAX Concepts and RF Measurements.pdf".

2. Basic Theory of Power Amplifier and Transmitter Front-End

Unlike LNA which is a small-signal amplifier, PA operates in the large signal domain. PA cannot be designed using the small signal analysis method only. Traditionally, PA can be modeled by Volterra series, which models the weak non-linear effect of the transistor. However, it must be based on an accurate model. Parametric simulation is more suitable to design the PA. Another approach to design PA is based on that the PA is terminated with optimum output impedance location at the Smith chart where the PA can deliver highest amount of power. However, the transistor is needed to be fabricated, de-assembled and tested using large signal loadpull testing, which is very expensive. Therefore, most of the people may match the output of the transistor to a resistance value lower than 50 Ω. In this work, this approach is adopted.

As stated in Chapter 1, the design of PA depends on different modulation schemes. For the digital communication which adopts OFDM or involves amplitude modulation, PA should be designed in the linear mode. These PAs are classified by Class A, Class B, Class AB, Class C and Class F differentiated by the conduction angle. For the digital modulation which does not have amplitude modulation, for example GMSK in GSM, PA should be designed in switching mode (i.e. Class D and Class E), where amplitude modulation is not used and the linearity is not concern. The classification of the PA will be shown in the sub-section.

2.1 Classification of Power Amplifier

For a linear PA, the PA is classified based on the conduction angle. Due to the operation, the current waveform of the PA is shown below, where α is the conduction angle, I_{max} is the peak current. The average DC, the 1st harmonic and the nth harmonic current are [1]:

$$I_{dc} = \frac{I_{\max}}{2\pi} \frac{2\sin(\alpha/2) - \alpha\cos(\alpha/2)}{1-\cos(\alpha/2)} \tag{2.1}$$

$$I_1 = \frac{I_{\max}}{2\pi} \frac{\alpha - \sin\alpha}{1-\cos(\alpha/2)} \tag{2.2}$$

$$I_n = \frac{I_{\max}}{2\pi} \frac{\alpha - \sin\alpha}{1-\cos(\alpha/2)} \left[\frac{\sin(n+1)\frac{\alpha}{2}}{n+1} + \frac{\sin(n-1)\frac{\alpha}{2}}{n-1} - \frac{2}{n}\cos\frac{\alpha}{2}\sin\frac{n\alpha}{2} \right] \tag{2.3}$$

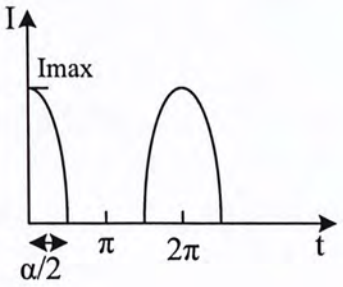

Fig. 2.1-1 Current waveform

With I_{max} normalized to 1, the current waveform with different harmonics versus the conduction angle could be plotted using (2.3) [1].

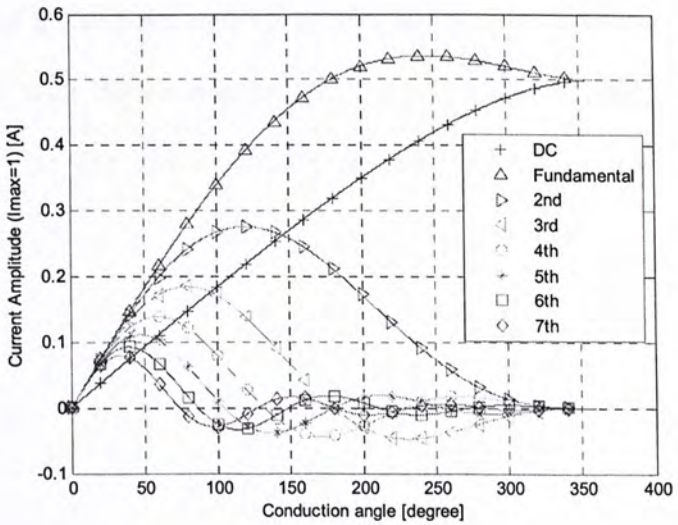

Fig. 2.1-2 Different harmonic current amplitude with different value of the conduction angle

Furthermore, the RF output power and the efficiency can be calculated based on the assumption that all the amplitudes are the same. Fig. 2.1-3 and Fig. 2.1-4 show the results. The efficiency of the amplifier approaches 100% when the conduction angle decreases, but the RF output power also approaches zero.

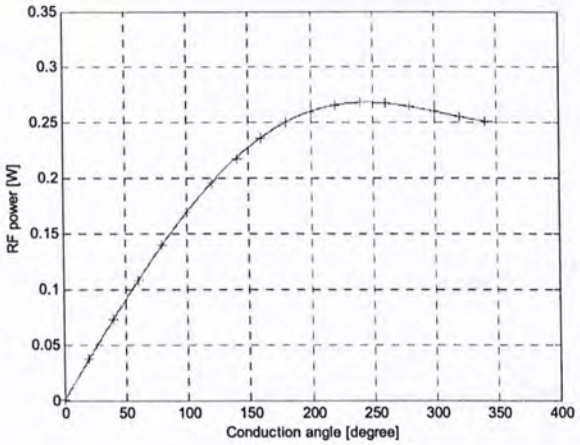

Fig. 2.1-3 RF power versus conduction angle

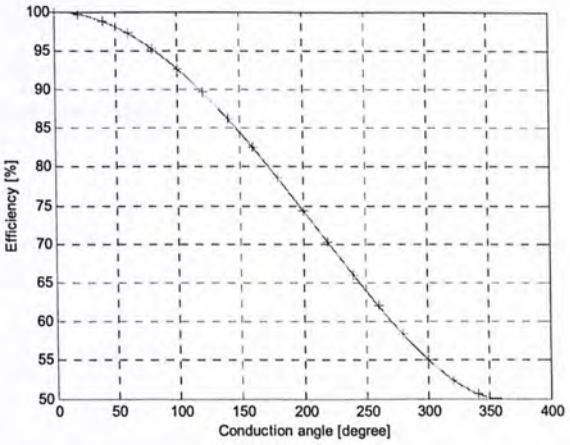

Fig. 2.1-4 Efficiency versus conduction angle

2.1.1Class A

In Class-A operation, $\alpha = 2\pi$, the transistor conducts current all the time over a cycle, as shown in Fig. 2.1-5. In Class-A mode, the transistor still operates in the small signal domain, with constant transconductance. Therefore, the amplifier has linear transconductance. From (2.8), it is known that the maximum efficiency η of a Class-A amplifier is 50%, in the case that the output voltage amplitude is equal to supply voltage, with the assumption that there is no knee voltage existed in the device, as shown in Fig. 2.1-4. From Fig. 2.1-2, there is no 2nd and higher harmonic generated when the conduction angle is 2π.

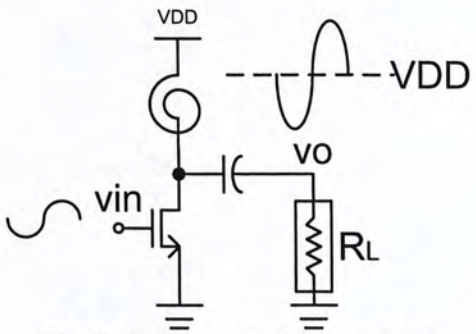

Fig. 2.1-5 Class A amplifier operation

$$I_{DC} = \frac{I_{\max}}{2} \tag{2.4}$$

$$I_1 = \frac{I_{\max}}{2} \tag{2.5}$$

$$P_o = \frac{1}{2}\frac{V_o^{\,2}}{R_L} \tag{2.6}$$

$$P_{DC} = \frac{V_{DD}V_o}{R_L} \tag{2.7}$$

$$\eta = \frac{V_o}{2V_{DD}} \tag{2.8}$$

2.1.2Class B

In Class-B operation, the conduction angle is π. The amplifier operation is shown in Fig. 2.1-6. The transistor only conducts current in half of the cycles. From (2.1) and (2.2) with $\alpha = \pi$, the DC, the 1st harmonic current, DC power and RF power are shown in (2.9)-(2.13). From (2.13), the efficiency is about 78% if the amplitude of the output waveform is equal to V_{DD} in the case that no knee voltage is present, as shown in Fig. 2.1-6. From Fig. 2.1-2, it is seen that the higher harmonics start to be generated due to the reduced conduction angle.

$$I_{DC} = \frac{I_{\max}}{2} \tag{2.9}$$

$$I_1 = \frac{I_{\max}}{\pi} \tag{2.10}$$

$$P_o = \frac{1}{2}\frac{V_o^2}{R_L} \tag{2.11}$$

$$P_{DC} = \frac{2V_{DD}V_o}{\pi R_L} \tag{2.12}$$

$$\eta = \frac{\pi}{4}\frac{V_o}{V_{DD}} \tag{2.13}$$

As the transistor conducts half of a cycle only, the overall output waveform can be generated out by combining RF current from another PA with 180° phase difference using transformer with the current from another half of cycle, as shown in Fig. 2.1-7.

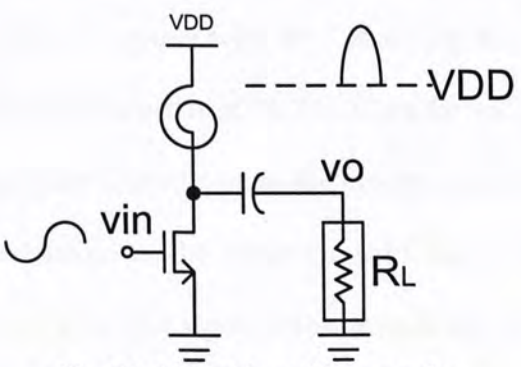

Fig. 2.1-6 Class B amplifier operation

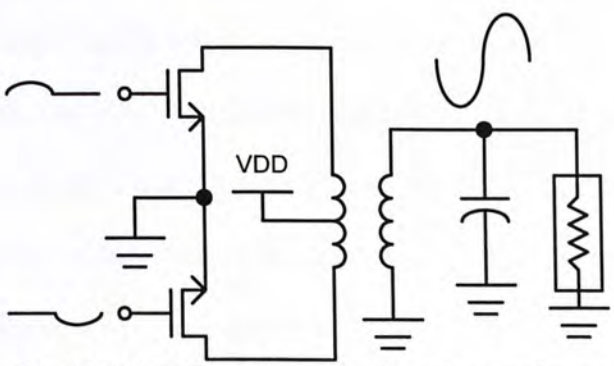

Fig. 2.1-7 Class B amplifier operation using transformer

2.1.3Class AB

The conduction angle of a Class-AB amplifier is between π and 2π. Although several harmonic components are generated, it has a small magnitude, as shown in Fig. 2.1-2. The voltage waveform is also shown in Fig. 2.1-8. From Fig. 2.1-2, the magnitude of the 2nd harmonic current waveform is generated rapidly, compared with other harmonics. However, the even harmonics can be suppressed by

using differential structure. As a result, differential Class-AB is the suitable candidate of the PA design in OFDM system, as it maintains the linearity with acceptable efficiency. The efficiency of a Class-AB amplifier is between 50% (class-A) and 78.5% (class-B).

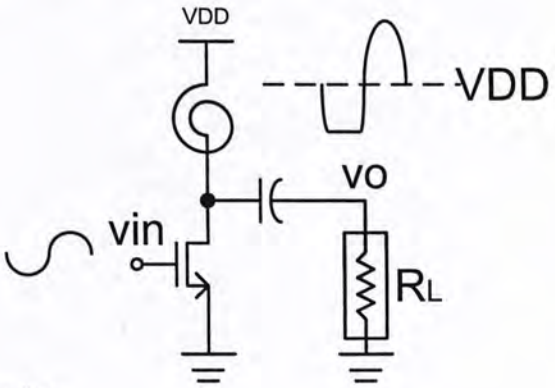

Fig. 2.1-8 Class AB amplifier operation

2.1.4Class C

The conduction angle of a Class-C amplifier is between 0 and π. As the conduction angle is further reduced, higher-order harmonics are generated with a large magnitude, but the efficiency is improved. The voltage waveform of a Class-C amplifier is shown in Fig. 2.1-9. The RF power generated is smaller compared with the Class A, Class AB and Class B counterparts, as shown in Fig. 2.1-3. The efficiency is between 78.5% (Class B) and 100%. However, it is almost impossible to achieve 100% in the Class C operation, as the voltage waveform is nearly a pulse in a very short duration. The amplitude modulation can be applied to the Class-C amplifier by applying drain modulation. This is an approach to apply an AM signal at the drain of the transistor in the Class-C amplifier.

Both the Class-C and Class E amplifiers, which will be described in the other section, are the candidates in the system using constant envelope modulation. The major difference between them is the amplitude relationship between the input and the output waveforms. In a Class-C amplifier, the output waveform still follows the input waveform, although a lot of higher-order harmonics are generated. However, it is not the case for the Class-E amplifier, as the transistor is a switch only.

Most of the publications reported that the design of the Class-E amplifier rather than Class-C amplifier as CMOS technology is good in implementing switch.

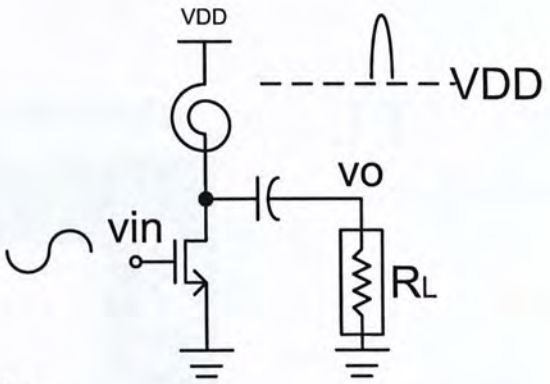

Fig. 2.1-9 Class C amplifier operation

2.1.5Class D

In a Class D amplifier, the transistor operates as a switch. The input signal should be large enough to drive the transistor as a switch. Fig. 2.1-11 shows the implementation of a Class-D amplifier. The complementary switch drives the resonator. The input signal is large enough to approximate it as a square wave. The resonator filters output high-order harmonics so the output waveform is sinusoidal wave.

In the operation of the Class-D amplifier, the voltage at the switch node V_{SW} does not overlap with the drain current waveform. Therefore, no DC power is dissipated at the switch. As a result, the efficiency is 100% theoretically. However, the finite gate-source and source-drain capacitance of the CMOS switch make it differ from the ideal switch. Thus, power is dissipated by the parasitic capacitance [2].

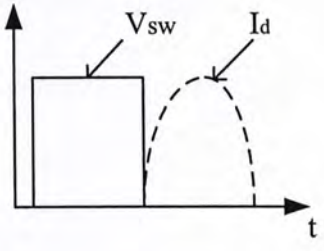

Fig. 2.1-10 Voltage and current waveforms in class-D operation

Fig. 2.1-12 shows a simple Class-D amplifier implemented in the CMOS technology. The transistors are driven as a pair of complementary switches. A feedback resistor is used to obtain high gain.

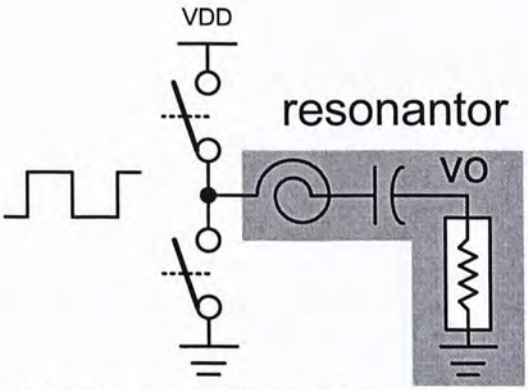

Fig. 2.1-11 Class D amplifier operation

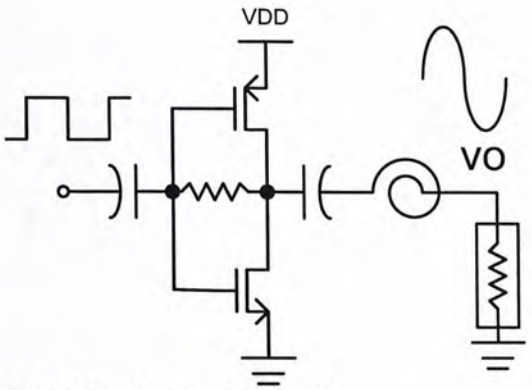

Fig. 2.1-12 Another class D amplifier

2.1.6Class E

The Class-E amplifier is another type of switching mode amplifier [7]. Similar to the class-D operation, the ideal efficiency is 100%. As it operates in switching mode, the on-resistance of the transistor should be as small as possible. The large drain-source capacitance of the CMOS devices can be incorporated in the Class-E amplifier design, as shown in (2.14). To make on-resistance R_{ON} small, the gate voltage of the CMOS devices should be large and the aspect ratio $\frac{W}{L}$ should also be large. Sometimes, the aspect ratio can be above 1000. However, the large parasitic drain-source capacitance can be incorporated into class-E amplifier design.

$$R_{ON} = \frac{1}{\mu_N C_{OX} \frac{W}{L}(V_{GS} - V_t)} \tag{2.14}$$

In the Class-E operation, there are two conditions needed to fulfill:

$$V_{SW} = 0 \text{ at } t = t_1 \tag{2.15}$$

$$\frac{\partial V_{SW}}{\partial t}\Big|_{t=t_1} = 0 \tag{2.16}$$

In order to achieve the above conditions given by (2.15) and (2.16), the inductance and capacitance values are carefully chosen. The simplified resultant voltage and current waveform is shown below:

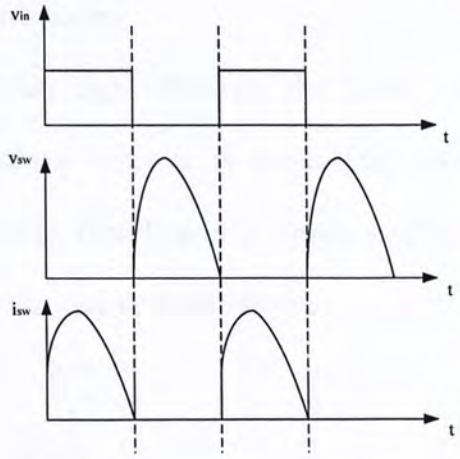

Fig. 2.1-13 Waveform of class-E operation. (top) switching voltage (center) drain voltage at transistor. (bottom) drain current of transistor

The design equation of the Class-E operation is developed under the condition that there is no loss in the inductors and capacitors. The simplified Class-E amplifier circuit is shown in Fig. 2.1-14. The design equation is shown as follows [7]:

$$R = \frac{2}{\frac{\pi^2}{4}+1}\frac{VDD^2}{P} \tag{2.17}$$

$$L = \frac{Q_L R}{\omega} \tag{2.18}$$

$$C1 = \frac{8}{\pi(\pi^2+4)}\frac{1}{2\omega R} \tag{2.19}$$

$$C2 = \frac{1}{\omega^2 L}\left(1+\frac{1.42}{Q_L - 2.08}\right) \tag{2.20}$$

where R is the loading resistance

P is the output power

Q_L is the quality factor of the output filter

The peak voltage V_{SW} is approximately equal to 3.56 times of V_{DD}. Another approach to analyze the Class-E operation is using state-space equation [2]. All the parasitic resistance of the loading inductor and output inductor are taken into account.

Although the Class-E amplifier has high efficiency, the linearity is poor. It cannot be used in the amplitude modulation applications as there is no relationship between the amplitudes of the input waveform and the output waveform. Therefore, it is widely used in GSM and Bluetooth system since the constant envelope modulation is used in those systems.

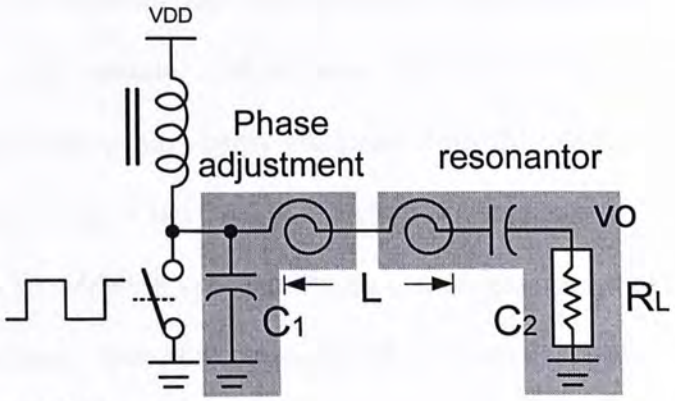

Fig. 2.1-14 Class E amplifier operation

The linearity problem of the Class-E amplifier can be improved by using the drain modulation technique. The RF signal can be decomposed into the amplitude and phase signals. The phase signal is applied to the Class-E amplifier, as it is only interested in the frequency. The amplitude signal is applied to the drain of the Class-E amplifier. The supply voltage of the Class-E amplifier changes according to the amplitude of the AM signal. However, it may have the misalignment problem between AM and PM signals. It is hard to implement the drain modulator, as it needs to supply high DC current with sufficient wide bandwidth [2].

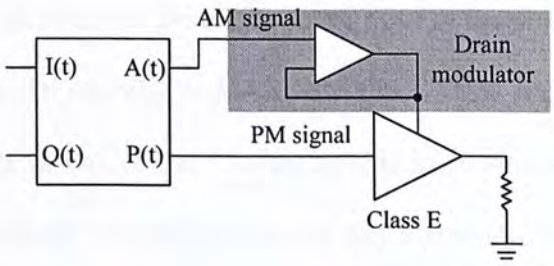

Fig. 2.1-15 Drain modulation

2.1.7Class F

In the Class-F operation, the transistor can work as both the voltage controlled current source or switch. However, the amplifier uses resonator with different harmonics to the fundamental. The transistor is biased to the Class-B operation to have better efficiency. Only the odd-harmonics can pass through the harmonics filters. The efficiency of the Class-F operation can approach to 100% if the infinite numbers of odd harmonics filters are added. It is because there is no overlapping between the waveforms of the drain voltage and drain current. One of the examples of the Class-F amplifier is shown in Fig. 2.1-16.

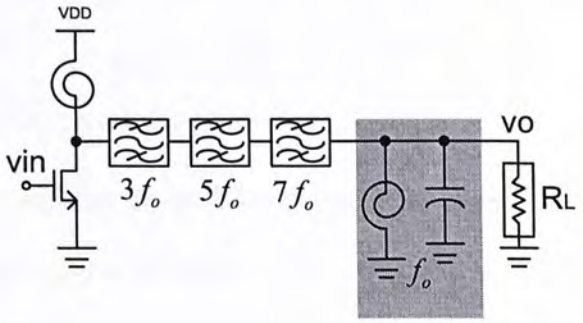

Fig. 2.1-16 Class F amplifier

2.2 Figure-of-Merit of Power Amplifier

The functionality and performance of a PA should be verified by three analyses. They are small signal analysis, large signal analysis and modulation analysis. Although PA is a large signal circuit, its small signal response is still needed to find out in order to ensure the PA function properly in both the small signal and large signal domains. Finally, PA is the one of the major components in the RF transmitter,

which operates in different standards. In the recent years, most of the new standards, for example, IEEE 802.11a/b/g/n and IEEE 802.16 Mobile WiMAX, use the OFDM modulation scheme. Its linearity requirement is high. In order to ensure the PA can operate in these standards, modulation tests with differential modulated RF signals, for the PA test, or modulated baseband signal, for the transmitter test, are required.

2.2.1 Small Signal Analysis

2.2.1.1 *S*-parameter

The small signal response of a PA can be verified by measuring its *s*-parameter. Although the linear PA is large signal circuit, its small signal response should be investigated. In order to test its small signal response, the PA should operate in the condition of low input and output power. For a single-end PA, the *s*-parameter is 2-port. However, when the PA is a differential structure, the common mode and differential *s*-parameter are needed to be measured. These *s*-parameters can be calculated from the 4-port *s*-parameter. The small signal power gain and stability measure can be found out using *s*-parameter.

2.2.1.2 Gain and Stability

The power gain of the RF amplifier depends on both the input and output matching. There are three definitions of the power gain under different input and output termination conditions [3]. They are listed below:

Transducer power gain

$$G_T = \frac{P_L}{P_{AVS}} \tag{2.21}$$

Power gain (operational power gain)

$$G_P = \frac{P_L}{P_{IN}} \tag{2.22}$$

Available power gain

$$G_A = \frac{P_{AVN}}{P_{AVS}} \tag{2.23}$$

where

P_L is power delivered to the load

P_{IN} is power input to the network

P_{AVS} is power available from the source

P_{AVN} is power available from the network

A simple microwave amplifier diagram is shown in Fig. 2.2-1. With the definition of return coefficient, the power gain definition can be rephrased as follows:

$$G_T = \frac{1-|\Gamma_S|^2}{|1-\Gamma_{IN}\Gamma_S|^2}|S_{21}|^2\frac{1-|\Gamma_L|^2}{|1-S_{22}\Gamma_L|} \tag{2.24}$$

$$G_P = \frac{1}{1-|\Gamma_{IN}|^2}|S_{21}|^2\frac{1-|\Gamma_L|^2}{|1-S_{22}\Gamma_L|} \tag{2.25}$$

$$G_A = \frac{1-|\Gamma_S|^2}{|1-S_{11}\Gamma_S|^2}|S_{21}|^2\frac{1}{1-|\Gamma_{OUT}|^2} \tag{2.26}$$

Under the condition that no transistor feedback exists (i.e. $S_{12} = 0$), the transducer gain G_T can be described as unilateral power gain G_{TU} [4]. Under the condition that S_{12} cannot be neglected, using the operational power gain G_P and available power gain G_A are more convenient to carry out analysis. The power gain or the operational power gain G_P is used when either input or output of the amplifier is assumed to be perfectly matched. It can be used for the design of a PA. As in the PA, loadpull technique is used and the transistor may not be conjugate matched at the output. The available power gain G_A is used when the output is assumed to be perfectly matched. It can be used to represent the low

noise amplifier (LNA). As in LNA, the input may need to perform noise match to reduce input referred noise.

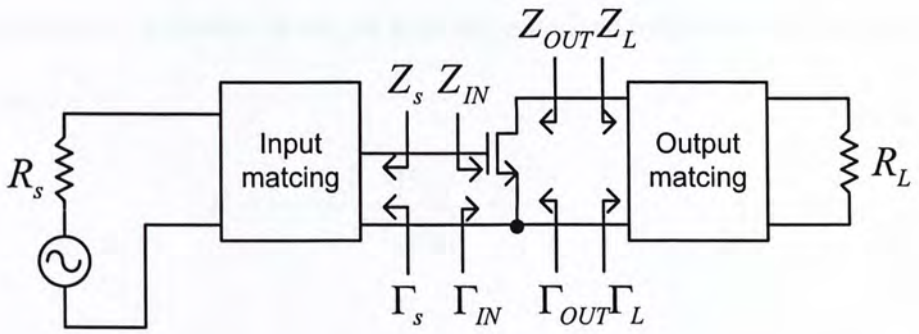

Fig. 2.2-1 Simple microwave amplifier diagram

In addition to the small signal power gain, the stability is another major concern. The amplifier may oscillate if there is a parasitic feedback path, and both the amplifier and feedback path fulfill the condition of oscillation. For high frequency applications, the parasitic gate-drain capacitance of the transistor is the one of the parasitic feedback path to make the amplifier unstable. Therefore, the amplifier should be terminated by appropriate impedance at both the input and output to maintain stability. In terms of the reflection coefficients, the conditions for the unconditionally stable are listed below:

$$|\Gamma_S| < 1 \tag{2.27}$$

$$|\Gamma_L| < 1 \tag{2.28}$$

$$|\Gamma_{IN}| = \left| S_{11} + \frac{S_{12}S_{21}\Gamma_L}{1 - S_{22}\Gamma_L} \right| < 1 \tag{2.29}$$

$$|\Gamma_{OUT}| = \left| S_{11} + \frac{S_{12}S_{21}\Gamma_S}{1 - S_{11}\Gamma_S} \right| < 1 \tag{2.30}$$

The input and output reflection coefficients in (2.26) and (2.27) are less than 1. It means the incident wave is larger than the reflected waves at both the input and output ports. From (2.29) and (2.30), Γ_{IN} and Γ_{OUT} depend on the load and source reflection coefficient simultaneously. As it is too complicated to calculate, a Rollett factor, or K-factor is defined to measure the stability. The definition is listed as follows:

$$K = \frac{1-|S_{11}|^2-|S_{22}|^2+|\Delta|^2}{|2S_{21}S_{12}|} \tag{2.31}$$

and

$$\Delta = S_{11}S_{22} - S_{12}S_{21} \tag{2.32}$$

The necessary and sufficient conditions for unconditionally stable are listed below:

$$K > 1 \tag{2.33}$$

$$\Delta < 1 \tag{2.34}$$

There is another parameter B_1 to measure the stability. The unconditionally stable conditions are K>1 and

$$B_1 = 1+|S_{11}|^2-|S_{22}|^2-|\Delta|^2 > 0 \tag{2.35}$$

2.2.2 Large Signal Analysis

PA is a large signal device due to the large input and output voltage swing. These behaviors cannot be modeled using small signal analysis. In most cases, the output voltage swing must be represented by fundamental, the 2nd harmonic and 3rd harmonics. Higher harmonics are neglected as they are small in magnitude, according to

$$y(t) = \alpha_1 x(t) + \alpha_2 x^2(t) + \alpha_3 x^3(t) + \ldots \tag{2.36}$$

There are several figure-of-merits to analyze the large signal response of a PA.

2.2.2.1 1-dB compression point

The 1-dB compression point is defined as the point that the input level causes the linear gain decreased by 1 dB [5]. If a signal $x(t) = A\cos\omega t$ is applied to the system, harmonics are produced due to the nonlinear gain of the PA. Then, the output voltage will be

$$y(t) = \alpha_1 A\cos\omega t + \alpha_2{}^2 A^2\cos^2\omega t + \alpha_3{}^3\cos^3\omega t \tag{2.37}$$

$$= \frac{\alpha_2 A^2}{2} + \left(\alpha_1 A + \frac{3\alpha_3 A^3}{4}\right)\cos\omega t + \ldots \tag{2.38}$$

If α_1 and α_3 are out of phase, the constant $\left(\alpha_1 A + \frac{3\alpha_3 A^3}{4}\right)$ is decreased when the signal amplitude is increased [5].

$$20\log\left|\alpha_1 + \frac{3}{4}\alpha_3 A^3\right| = 20\log|\alpha_1| - 1 \tag{2.39}$$

$$\rightarrow A = \sqrt{0.145\left|\frac{\alpha_1}{\alpha_3}\right|} \tag{2.40}$$

2.2.2.2 Third-order intermodulation point

The third-order intermodulation point (IP_3) is another figure-of-merit to analyze the linearity of the PA. However, the output signal is being distorted and cannot be used in amplitude modulation when the amplitude of the input signal swing approaches the 1-dB compression point. Therefore, IP_3 is not an important parameter to examine the linearity of PA.

If the input signals are two tones and close in frequency (i.e. $x(t) = A_1\cos\omega_1 t + A_2\cos\omega_2 t$), the fundamental output swing are given by

$$y(t) = \alpha_1(A_1 \cos\omega_1 t + A_2 \cos\omega_2 t) + \alpha_2{}^2(A_1 \cos\omega_1 t + A_2 \cos\omega_2 t)^2 \quad (2.41)$$
$$+ \alpha_3(A_1 \cos\omega_1 t + A_2 \cos\omega_2 t)^3$$

The following intermodulation products are generated

$$\text{For } 2\omega_1 - \omega_2 : \frac{3\alpha_3 A_1{}^2 A_2}{4} \quad (2.42)$$

$$\text{For } 2\omega_2 - \omega_1 : \frac{3\alpha_3 A_2{}^2 A_1}{4} \quad (2.43)$$

Those intermodulation products are close to the fundamental, the signal may be corrupted. The third-order intercept point (IP_3) is defined as the point where the power of fundamental is equal to the power of the intermodulation. If the amplitudes of two signals are equal ($A_1 = A_2$) , then IP_3 can be calculated as follows:

$$|\alpha_1| A_{IP3} = \frac{3}{4}|\alpha_3| A_{IP3}{}^3 \quad (2.44)$$

$$A_{IP3} = \sqrt{\frac{4}{3}\left|\frac{\alpha_1}{\alpha_3}\right|} \quad (2.45)$$

The graphical representation of the 1-dB compression point and IIP3 is shown in Fig. 2.2-2

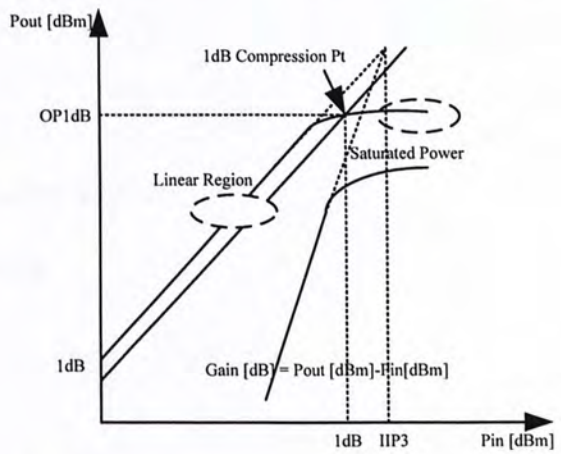

Fig. 2.2-2 Graphical illustration of 1-dB compression point and IIP3

2.2.2.3 Power Gain

The power gain is defined below:

$$G = \frac{P_{OUT}}{P_{IN}} \tag{2.46}$$

where P_{OUT} is power delivered to the load

P_{IN} is power provided by the source

In the power amplifier design, the power gain is not the most important parameter. Most of the power stages of the PA do not have high gain as conjugate match is not used in the PA output stage in order to extract high output power from the supply. Therefore, the gain of power stage is not optimized. In order to have high gain, several gain stages are added before the power stage. In some advanced transceivers, the gain stage can be programmable controlled.

2.2.2.4 Drain Efficiency and Power Added Efficiency

The efficiency is another important parameter in the PA design. There are two definitions for the efficiency. They are listed below:

$$DE = \frac{P_{OUT}}{P_{DC}} \tag{2.47}$$

where P_{OUT} is power delivered to the load

P_{DC} is DC supply power

$$PAE = \frac{P_{OUT} - P_{IN}}{P_{DC}} \tag{2.48}$$

where P_{OUT} is power delivered to the load

P_{IN} is power available from the source

P_{DC} is DC supply power

2.2.2.5 AM-AM and AM-PM conversion

As PA is a nonlinear device, it usually has band-pass frequency response. Assume that PA is memoryless and nonlinear and a modulated signal $x(t)$ is applied to the PA,

$$x(t) = A(t)\cos[2\pi f_o t + \phi(t)] \tag{2.49}$$

the output signal $y(t)$ is given by

$$y(t) = f[A(t)]\cos\{2\pi f_o t + \phi(t) + g[A(t)]\} \tag{2.50}$$

where $f[A(t)]$ is the nonlinear gain (AM-AM conversion)

$g[A(t)]$ is the amplitude-to-phase conversion (AM-PM conversion)

Both the amplitude and phase signal will be corrupted by the nonlinearity of the PA.

2.2.3 Modulation Analysis

2.2.3.1 Constellation Diagram and Error Vector Magnitude

The modulation analysis is used to test the modulation accuracy of the PA or the transmitter. In the digital communication using OFDM, the data symbol is modulated to different modulation types, such as quadrature phase shift keying (QPSK) or M-ray quadrature modulation (M-ray QAM), for example 16-QAM or 64-QAM. After the digital modulation, the fast Fourier transform (FFT) is applied to the data stream and then a time-varying waveform is produced. This waveform is transmitted by the transmitter. The transmitted waveform will be distorted if the transmitter is highly nonlinear. The FFT is applied to the data stream and then the data stream will be demodulated on the receiver side. The error vector magnitude (EVM) is defined as the mean square error between the samples of the actual and the ideal signals, normalized by the average power of the ideal signals [8].

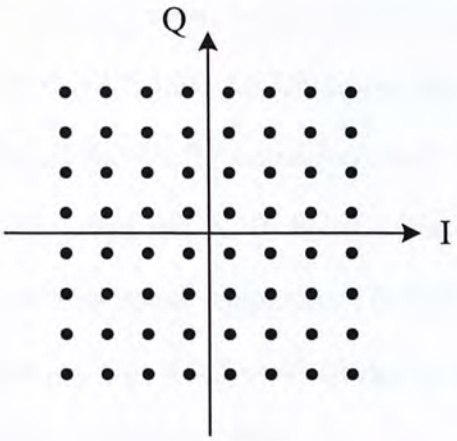

Fig. 2.2-3 64-QAM Constellation diagram

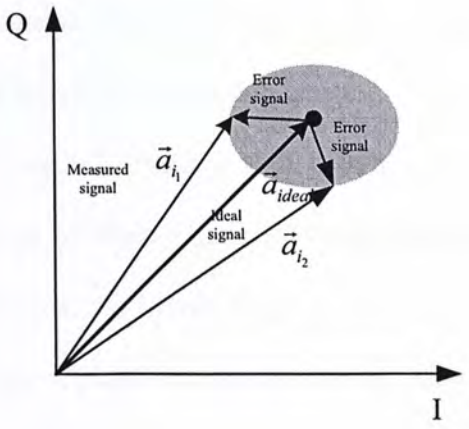

Fig. 2.2-4 Error vector magnitude

$$EVM(\%) = \left[\frac{\sum \left\{ \left| \vec{a}_i - \vec{a}_{ideal} \right|^2 \right\}}{\sum \left\{ \left| \vec{a}_{ideal} \right|^2 \right\}} \right]^{\frac{1}{2}} * 100 \tag{2.51}$$

The EVM calculated (2.51) is the root mean square value. It can be represent by the in dB form as follows

$$EVM(dB) = 10\log(EVM(\%)) \tag{2.52}$$

2.3 Reference

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3. Circuit Design of Power Amplifier

3.1 Introduction

In Chapter 1, it is clear that the requirement of Power Class Index I for WiMAX applications is about 18 dBm to 20 dBm. Therefore, the required output power is set to about 20 dBm. As WiMAX is an OFDM system, the PA cannot operate in the switching mode, so that PA is designed to operate in the linear mode. In order to have high linearity with acceptable efficiency, Class AB topology is chosen. However, this PA is a design prototype, so that the center frequency is set to 3 GHz, which PA has best performance at this frequency band.

In this chapter, the design technique of the PA will be discussed. The PA works under the supply voltage of 3.3 V. The design challenge is that the PA functions under a relatively low supply voltage compared with the SiGe bipolar or GaAs technologies. Therefore, the PA is not terminated with a 50-Ω load if the output power is needed to be high. In Section 3.2, the topology of the PA is addressed. Afterwards, both the simulation and layout consideration are shown in Section 3.3 and 3.4. The measurement result of the PA will be reported in Section 3.5.

3.2 Topology of the Power Amplifier Design

Fig. 3.2-1 shows the overall structure of the proposed PA. It consists of a driver stage, a power stage and an output matching network. The power stage provides adequate output power to the load. As the transistor sizes in the power stage are large, the driver stage is added to drive the large gate capacitance. The gain of the PA is controlled by the transconductance of the driver stage and the quality factor (Q) of its resonant tank. The output matching network is used to transform the 50-Ω load to the optimum resistance R_{OPT}.

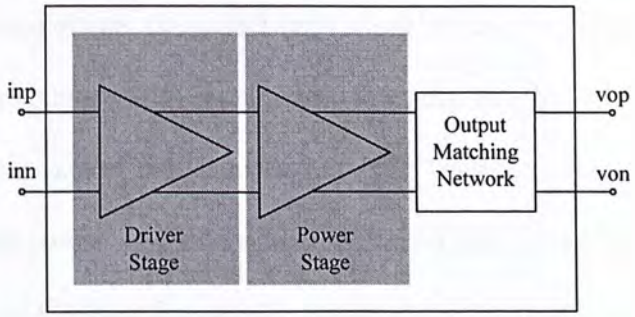

Fig. 3.2-1 Block diagram of power amplifier

3.3 Design in Power Amplifier

3.2.1Power Stage

The design of the power stage involves the selection of appropriate output matching network and transconductance in the power transistors. In order to achieve high output power from low supply voltage because of down-scaling of the CMOS technology, the output resistance should be smaller than 50 Ω. The optimum output resistance R_{OPT} can be roughly found by a technique called load-line match method [1] as follows:

$$R_{OPT} = \frac{V_{DD} - V_K}{I_{\max}} = \frac{V_{DD} - V_K}{2I_{DD}} \tag{3.1}$$

where V_{DD} is the supply voltage and V_K is the knee voltage and I_{max} is the peak output current.

With a high knee voltage, the transistor falls into the linear or even weak inversion region easily with high voltage swing. The overall gain will, thus, be significantly affected. The *W/L* ratio of the power transistor is the limiting factor of the knee voltage since the minimum v_{ds} is proven by

$$v_{ds\min} = \sqrt{\frac{2I_{\max}}{\mu C_{OX}\frac{W}{L}}} \tag{3.2}$$

In order to reduce the knee voltage, the aspect ratio should be high in order to reduce v_{dsmin}. However, this increases the gate capacitance at the same time. v_{dsmin} can also be reduced by decreasing I_{max}. Yet, the power gain and output power will then be reduced. Therefore, R_{OPT}, I_{DD} and output power are closely related. The output power should be optimized by varying I_{DD} and R_{OPT}, with fixed W/L ratio. The optimization is done in Cadence Spectre-RF by observing the relationship between the output 1-dB compression point (OP1dB) and R_{OPT} with ideal resistive loads and fixed W/L ratio, as shown in Fig. 3.3-1. An optimum output resistance can be found for each supply current. The curve I_{DD} = 250 mA is used in the design due to the limitation on the DC current through the drain inductors.

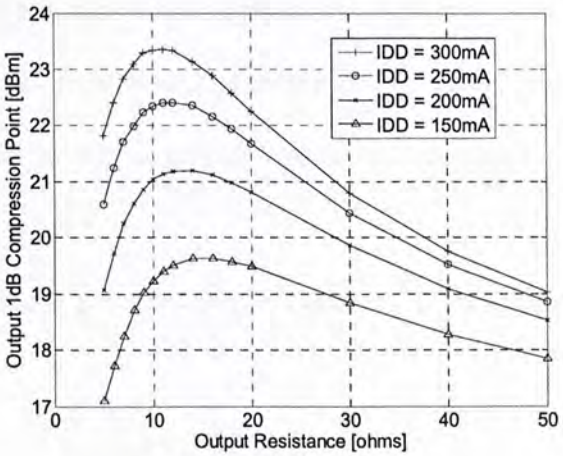

Fig. 3.3-1 OP1dB vs R_{OPT}

Although the sizes of the transistors should be large, the upper limit of the size of transistors is dependent on the available size of on-chip inductors at the previous stage. In this case, the previous stage is the driver stage, which will be mentioned at the next section. The on-chip inductors of the driver stage are needed to resonance out the gate capacitance of the transistors at the power stage. However, the on-chip inductors with fixed number of values are provided by the foundry design kit. In order to provide sufficient power gain and minimize loss, the on-chip inductors with highest Q-factor are needed to be used.

The on-chip inductor with inductive value of 1.21 nH with the width of 20 μm has the highest Q-factor, which is used in both the power stage and driver stage.

When the transistors sizes are further increased, the gate capacitance will also increased. A small inductor is required to resonance out the gate capacitance. However, the inductors with values smaller 1 nH, it may be greatly suffered from the process variation. In addition, it may also reduce the power gain of the overall PA, as the power gain depends on the Q-factor of the resonator.

When R_{OPT} is determined, the output matching network is designed to transform the 50-Ω load to R_{OPT} The ratio of the 50-Ω load and R_{OPT}, is the transformation ratio of the output matching network. It is shown in [2] that high transformation ratio degrades the efficiency and output power. Therefore, R_{OPT} should not be smaller than 10. In addition, as shown in Fig. 3.3-1, with a supply current of 250 mA, OP1dB attains the highest value with an output resistance of around 12Ω. This is, therefore, chosen as the optimum resistance.

Fig. 3.3-2 and Fig. 3.3-3 show the two output matching topologies. In Fig. 3.3-3, the R_L can be transformed to R_S by

$$R_L = (Q_T^2 + 1)R_S \approx Q_T^2 R_S \tag{3.3}$$

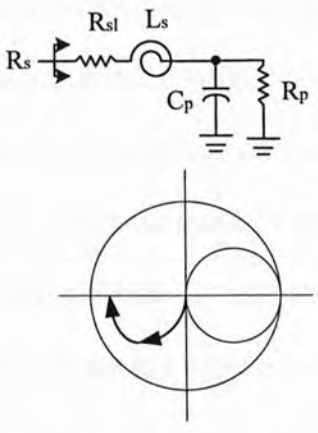

Fig. 3.3-2 Output matching network with series inductor and shunt capacitor

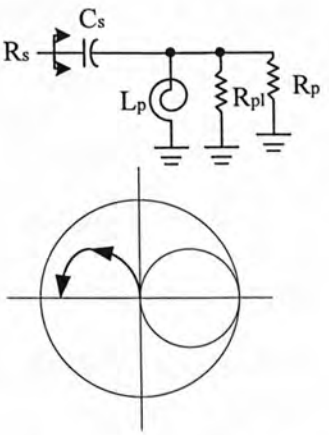

Fig. 3.3-3 Output matching network with series capacitor and shunt inductor

Assuming the R_{sl} is the parasitic resistance in the on-chip inductor L_S. The change in resultant resistance due to the parasitic resistance in the on-chip inductor is

$$\Delta R_S = (R_S + R_{sl}) - R_S = R_{sl} \tag{3.4}$$

In the case of Fig. 3.3-3, the L_P has the same Q-factor as L_S in Fig. 3.3-2, with the following definition

$$Q_L = \frac{\omega L_S}{R_{sl}} = \frac{R_{pl}}{\omega L_P} \tag{3.5}$$

With the present of the parasitic resistance in the on-chip inductor in the parallel form, the Q-factor of the whole output matching network is the following:

$$Q_T = \frac{R_{pl} // R_L}{\omega L_P} \tag{3.6}$$

By using the (3.3), the overall series resistance in the output matching network is

$$R_S' = \frac{(\omega L_P)^2}{R_{pl} // R_L} \tag{3.7}$$

Finally, the change in series resistance due to the parasitic resistance

$$\Delta R_S = R_S' - R_S = \frac{R_{pl}}{Q_L^2} = R_{sl} \tag{3.8}$$

Therefore, the change in resistance due the parasitic resistance in the on-chip inductor is the same in the case of series-inductor-shunt-capacitor and series-capacitor-shunt-inductor. However, the series-inductor-shunt-capacitor configuration is a low-pass filter but the series-capacitor-shunt-inductor is a high-pass filter. The series-capacitor-shunt-inductor cannot filter out the high order harmonic. However, the series-capacitor-shunt-inductor can provides a DC block and the shunt inductor gives lower energy coupling to the substrate as one terminal is grounded [2]. In addition, the series-capacitor-shunt-inductor configuration can relieve the flicker noise upconverted by the upconversion mixer.

The series-capacitor-shunt-inductor topology is chosen for the output matching network. The design equation is set as follows:

$$Q_T = \sqrt{\frac{R_L}{R_S} - 1} = \sqrt{m-1} \tag{3.9}$$

$$L_P = \frac{R_L}{\omega Q_T} \tag{3.10}$$

$$C_S = \frac{1}{\omega R_S Q_T} \tag{3.11}$$

where m is the transformation ratio, R_L is the loading resistance, R_S is the required optimum resistance and Q_T is the quality factor of the output matching network.

Fig. 3.3-4 shows the overall schematic of the power stage including the output matching network. A supply voltage of 3.3V is used in the power stage. Cascode transistors are used, which are biased by the self-biasing cascode technique as mentioned in [3]. The cascode transistors can extend the breakdown voltage and the PA is more reliable.

In the power stage, the sources of the transistors are connected to ground. The large signal differential drain currents are show as follows:

$$\Delta I_D = \frac{1}{2}\mu_N C_{OX}\frac{W}{L}(V_{GS1} + V_{GS2} - 2V_T)(V_{GS1} - V_{GS2}) \tag{3.12}$$

By keeping V_{GS1} and V_{GS2} constant, the differential current can be kept linear under the differential voltage. However, the nonlinearity of the CMOS differential amplifier comes from the nonlinear capacitance within the device, so that CMOS differential amplifier is still nonlinear even this topology is used.

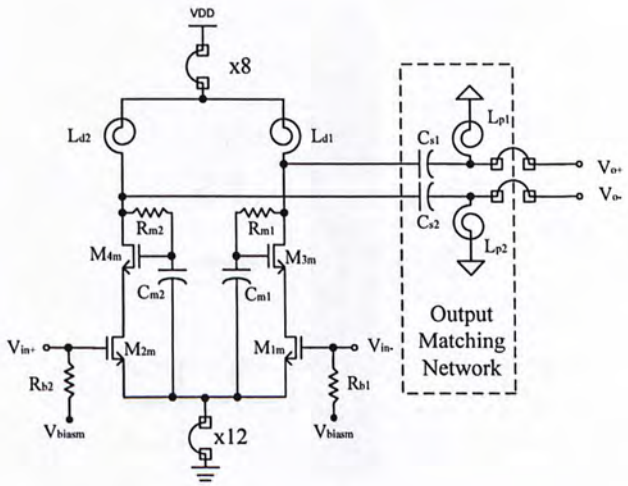

Fig. 3.3-4 Power Stage

The transistors sizes and other component values are listed as follows:

M_{1m}	840μ/0.18μ	M_{2m}	840μ/0.18μ	M_{3m}	840μ/0.18μ	M_{4m}	840μ/0.18μ
R_{m1}	2.56 kΩ	R_{m1}	2.56 kΩ	R_{b1}	2.56 kΩ	R_{b2}	2.56 kΩ
L_{d1}	1.21 nH	L_{d2}	1.21nH	L_{p1}	1.654 nH	L_{p2}	1.654 nH
C_{m1}	10.45 pF	C_{m2}	10.45 pF	C_{s1}	3.09 pF	C_{s2}	3.09 pF

In addition, on-chip loading inductors L_{d1} and L_{d2} are used. The on-chip inductors suffer from relatively large parasitic resistance compared with the bondwire inductor. The parasitic resistance may reduce the output voltage swing and affect the output power level. However, the differential matching of bondwire inductors are poor as it is hard to produce two bondwire inductors with little or no difference. The poor differential matching at the loading inductors may lead to common mode oscillation shown below

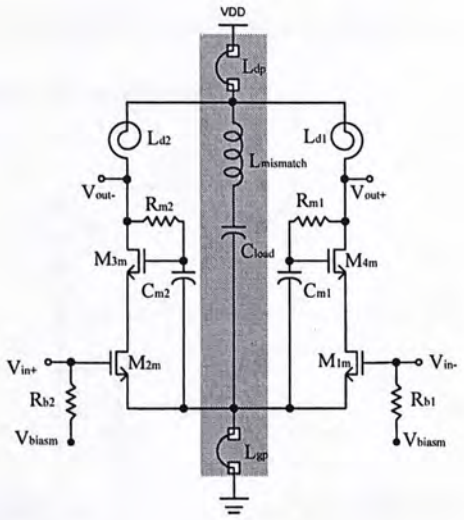

Fig. 3.3-5 Parasitic common mode oscillation

The common mode oscillation frequency due to the resonator at the power supply is given by

$$f = \frac{1}{2\pi\sqrt{(L_{dp} + L_{gp} + L_{mismatch})C_{load}}} \tag{3.13}$$

The common mode oscillation may occur at the desired frequency. In order to prevent the oscillation, two methods may be used. One method is to add a damping resistor in series with the C_{load}. The other method is to reduce the L_{dp} and L_{gp} by using more bondwires. The resonator may be unstable at higher frequency but the gain is insufficient to trigger oscillation.

3.2.2Driver Stage and Input matching

Input signals will be reflected back when the gate capacitance of the power stage is too large and the PA is connected to the input source directly. Thus, a driver stage, as shown in Fig. 3.3-6, is added to drive the power stage. The gate capacitance in the power stage is resonated by the drain inductors (L_{d3} and L_{d4}). The biasing current in the driver stage can be tuned in order to adjust the gain of the whole PA. A supply voltage of 1.8 V is sufficient to provide the necessary gain. Cascode structure is still used

to provide better stability in the high-gain driver. Similar to the power stage, the cascode transistors are also biased by the self-biasing cascode technique.

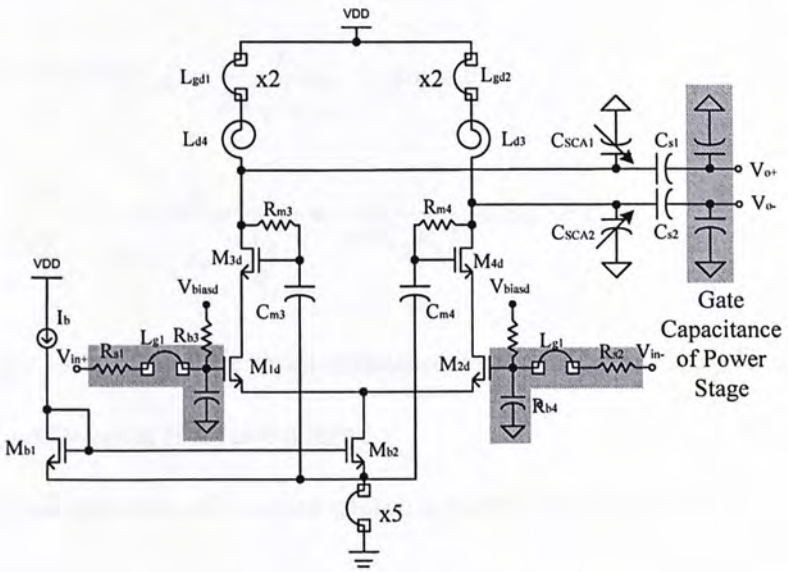

Fig. 3.3-6 Driver stage

The lists of transistor sizes and values of components are as follows:

M_{1d}	210μ/0.18μ	M_{2d}	210μ/0.18μ	M_{3d}	210μ/0.18μ	M_{4d}	210μ/0.18μ
R_{m3}	2.56 kΩ	R_{m4}	2.56 kΩ	R_{b3}	2.56 kΩ	R_{b4}	2.56 kΩ
L_{d3}	1.21 nH	L_{d4}	1.21nH	C_{s1}	5.047 pF	C_{s2}	5.047 pF
C_{m1}	10.45 pF	C_{m2}	10.45 pF	M_{b1}	125/0.18	M_{b2}	1000/0.18

At the input port, a series resonator is formed by bondwire inductors L_g, gate capacitance C_g, source resistance R_S and resistive biasing resistor R_B. This resonator shown in Fig. 3.3-7 controls the input reflection coefficient of the PA.

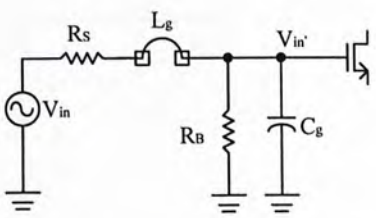

Fig. 3.3-7 Series resonator at input port

The resonator forms a potential divider and the ratio $\frac{Vin'}{Vin}$ is shown in (3.14).

$$\frac{Vin'}{Vin} = \frac{1}{j\omega\left(C_g R_S + \frac{L_g}{R_B}\right) + 1 + \frac{R_s}{R_B} - \omega^2 L_g C_g} \tag{3.14}$$

$\frac{Vin'}{Vin}$ at the resonant frequency $f_o = \frac{1}{2\pi\sqrt{L_g C_g}}$ is given by

$$\frac{Vin'}{Vin} = \frac{1}{j\omega\left(C_g R_S + \frac{L_g}{R_B}\right)} \approx \frac{1}{j\omega(C_g R_S)} \text{ as } R_B >> L_g \tag{3.15}$$

To reduce the voltage loss, C_g and the series resistance R_S should be reduced. However, common mode oscillation due to L_g may occur if R_S is too small.

The CMOS differential pair with tail current source is used in the driver configuration. The large signal response is given by

$$I_{D1} - I_{D2} = \frac{1}{2}\mu_N C_{OX}\frac{W}{L}(V_{in1} - V_{in2})\sqrt{\frac{4I_{SS}}{\mu_N C_{OX}\frac{W}{L}} - (V_{in1} - V_{in2})} \tag{3.16}$$

From (3.16), it can be shown that driver is more nonlinear compared with the source-grounded differential pair in power stage. However, it can have better common mode rejection.

The overall gain of the PA depends on the shunt resonator, consisting of the drain inductors (L_{d3} and L_{d4}), switched capacitor network (C_{sca1} and C_{sca2}), gate capacitance of the power stage (C_g) and coupling capacitors (C_{s1} and C_{s2}). Its resonant frequency, determined by (3.17) can be tuned by changing the value of C_{sca}.

$$\omega = \frac{1}{\sqrt{L_d\left(C_{sca} + \frac{C_s C_g}{C_s + C_g}\right)}} \tag{3.17}$$

3.4 Simulation Result on Power Amplifier

The design is simulated using Cadence Spectre-RF simulator. In the pre-layout simulation, some shunt capacitor is added to model the parasitic capacitance of metal wires. The simulation schematic is shown below

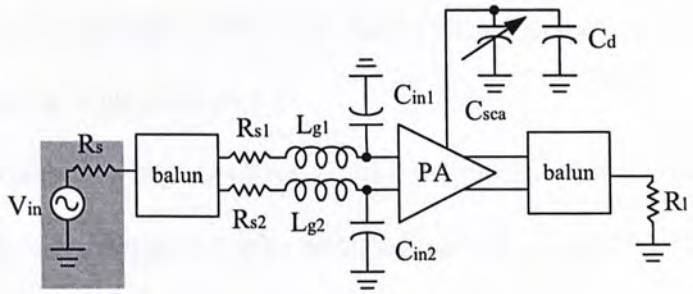

Fig. 3.4-1 Simulation schematic

As the PA is differential, two baluns with no loss are added at both input and output port. The L_g and R_s are the inductor and resistor for input matching. C_{in} models the parasitic capacitance of metal wires at the input port, and C_d model the parasitic capacitance at the node between driver stage and power stage. C_{sca} model the switched capacitor array at the circuit.

Both the pre-layout and post-layout simulation result is shown as follows. In the pre-layout simulation, C_{in} is set to 200fF to model the on-chip metal wires. The circuit is measured at 3 GHz center frequency with different values of L_g, C_{in} and C_{sca}.

Table 3-1 Pre-layout and post-layout simulation result at 3 GHz

	Pre-layout @ 3G	Post-layout @3G
Psat [dBm]	24.0762	24.7746
P1dB [dBm]	-11.9796	-12.1258
OP1dB [dBm]	19.054	21.2942
linear gain [dB]	32	34.4
gain @ P1dB [dB]	31.0338	33.42
PAE @ P1dB [%]	11.06946	18.253
PAE @ Psat [%]	36	34
DR power [W]	66.4m	65.5m
PW power [W]	615m	611m
Cin / fF	200	1
Lg / nH	4.5	3.5
Cd / F	2p	1f
code	b'111'	b'000'

3.5 Layout consideration

The layout is implemented in 1P6M UMC 0.18 μm RF CMOS technology. The top metal is thick metal with 20 kA. The layout of PA is very important. The parasitic resistance should be minimized as the drain current is very high. The power transistor cluster should place near to the power ground pads in order to reduce the parasitic resistance; otherwise, the transconductance of the power stage is reduced and the output voltage swing is also reduced.

The loading inductor should have high *Q*-factor in order to minimize the loss due to parasitic resistance. The inductor from the foundry design kit with metal wire of 20 μm wide is chosen. From the foundry information, the top-metal wires can withstand 5.32 mA per μm, so that this on-chip inductor can withstand DC currents of 100 mA.

Due to the limitation of the chip areas, the output matching network is placed in between the power stage and the driver stage. The floorplan of the PA is shown below.

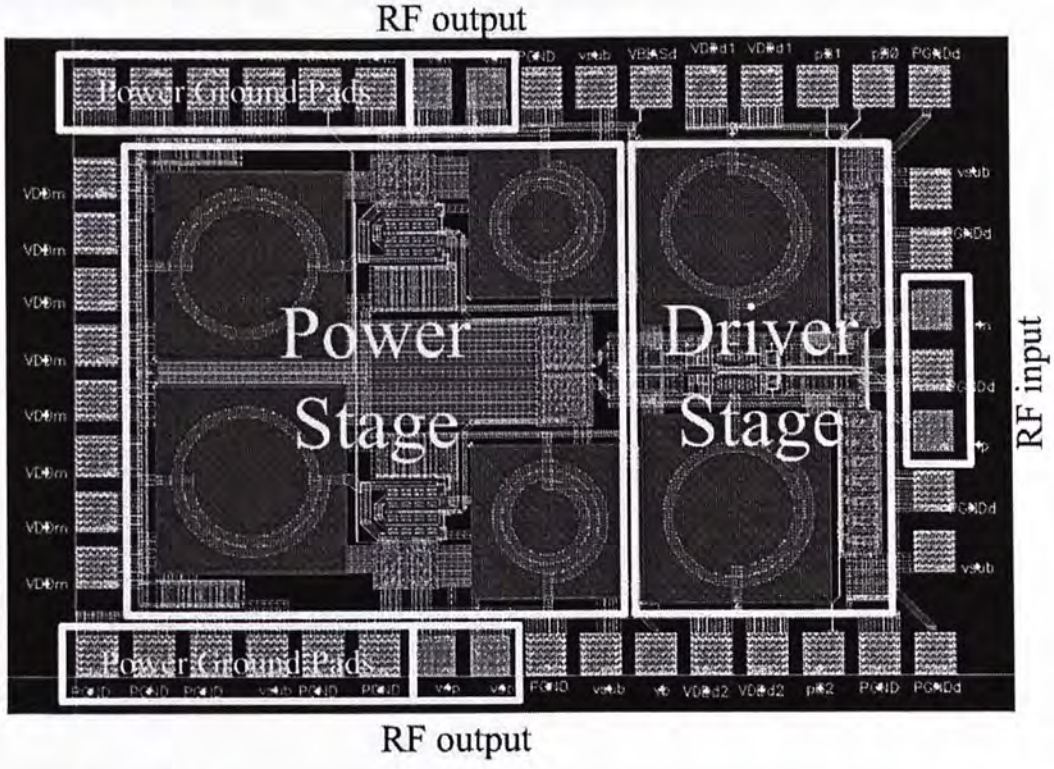

Fig. 3.5-1 Floorplan of the PA

In the layout, M6 is used for RF signal to minimize the parasitic capacitance. The power transistors are placed close to the power ground metals. In order to reduce the parasitic resistance of power ground metals, two metal lines M4 and M5 are used. As a result, the power transistor clusters is not placed closed to each other. It may introduce larger mismatch but it can minimize the cross-coupling and reduce source resistance. In the driver stage, the transistors are placed close to each other to minimize mismatch.

3.6 Measurement Result on Power Amplifier

The two-stage PA was fully integrated and implemented in the 0.18-μm CMOS technology. It is measured at 3 GHz with 1.8 V supply voltage in the driver stage and 3.3 V supply voltage in the power stage. The chip micrograph is shown in Fig. 3.6-1. The die size is 1850 × 1400 μm^2. The driver and power stage consist of 2 and 8 sets of transistors with W/L = 105 μm/0.18 μm each. Series resistors are added at the input to model the impedance of the resonant tank in the upconversion mixer. They are only used for measurement purpose.

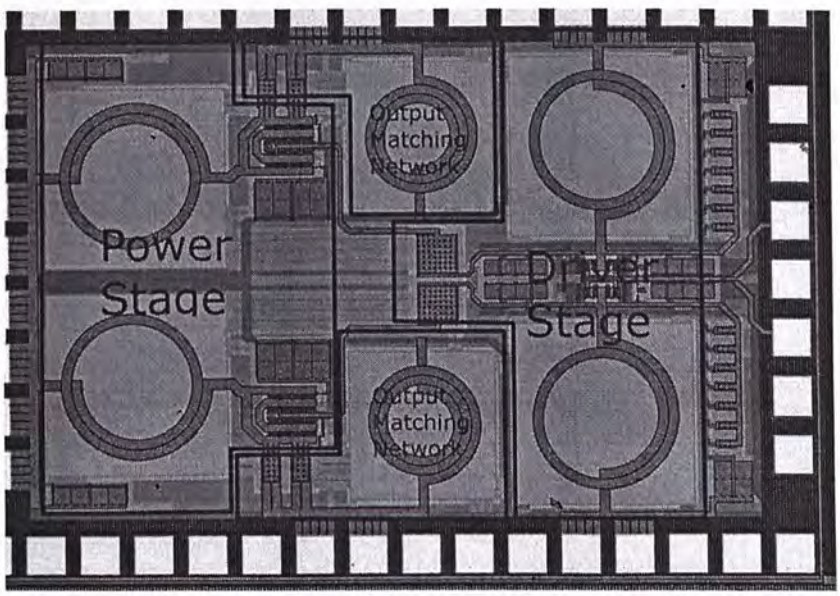

Fig. 3.6-1 Chip Photo

As shown in Fig. 3.6-2, the die is mounted on a PCB by silver epoxy and then the die is wire-bonded to the PCB. As the circuit is differential, so that two 180° hybrid couplers are used. The power loss of the cables and the insertion loss of the couplers are calibrated before the measurement. Two resistors with 20 Ω are connected at the input ports.

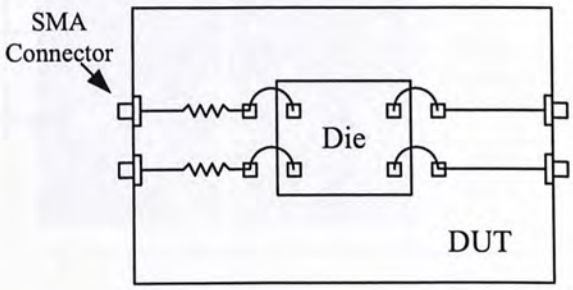

Fig. 3.6-2 Testing board configuration

3.4.1 Small signal measurement

The small signal response of the PA is measured assuming a small input power entering the input port of the PA. Fig. 3.6-3 shows the block diagram of the measurement. The *s*-parameter is measured by Agilent E5071A ENA Series RF Network Analyzer. Both the *s*-parameter of the common mode and differential mode of the PA are measured and are shown in Fig. 3.6-5 to Fig. 3.6-10.

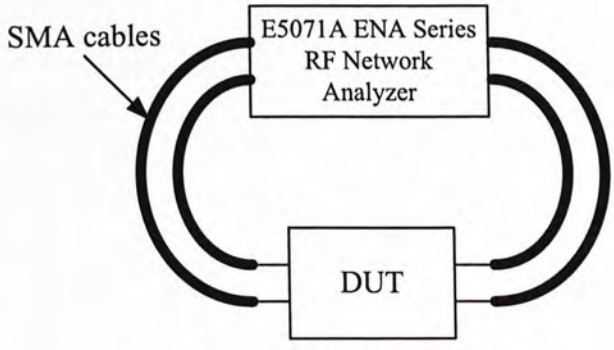

Fig. 3.6-3 Small signal measurement configuration

Fig. 3.6-4 shows the port arrangement in the small signal measurement. Port 1 and Port 2 are defined as input port and Port 3 and Port 4 are defined as output port. All the ports are connected through semi-rigid SMA cables.

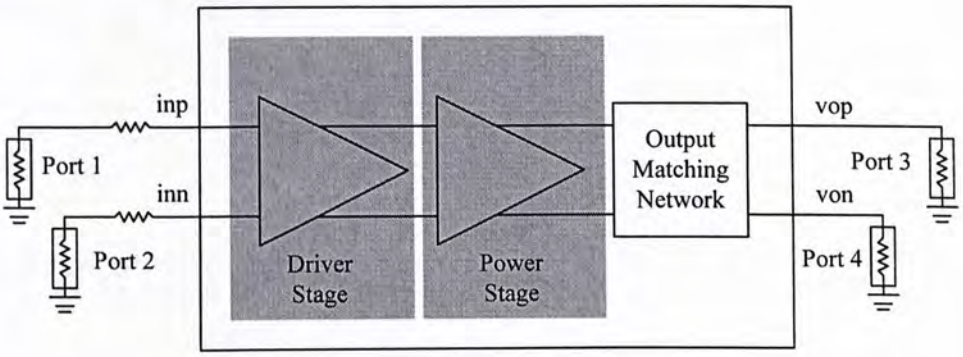

Fig. 3.6-4 Port arrangement in the 4-port s-parameter measurement

The common mode return loss in the input (S_{11} and S_{22}) and output (S_{33} and S_{44}) of the PA are shown in Fig. 3.6-5 and Fig. 3.6-6 respectively. The forward and reverse voltage transmissions (S_{31} and S_{42} for forward, S_{13} and S_{24} for reverse) of the PA in common mode are shown in Fig. 3.6-7 and Fig. 3.6-8 respectively. In Fig. 3.6-9, the return loss of differential input (S_{d11}) and output (S_{d22}) is shown. The forward and reverse voltage transmission of the PA (S_{d21} and S_{d12}) is shown in Fig. 3.6-10.

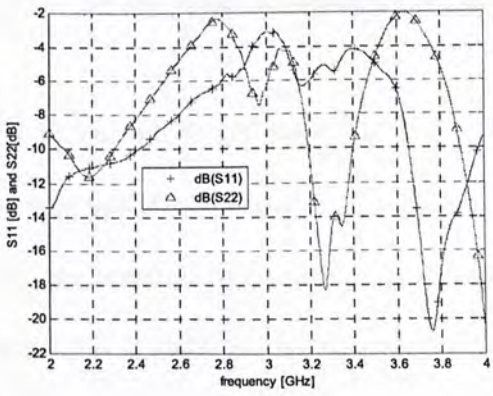

Fig. 3.6-5 Common mode return loss at input

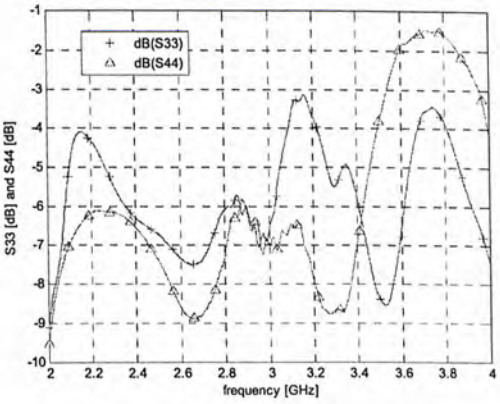

Fig. 3.6-6 Common mode return loss at output

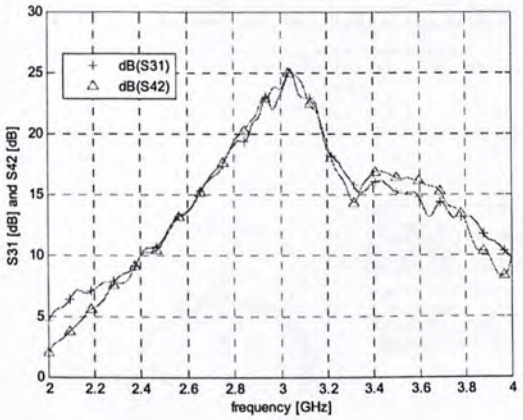

Fig. 3.6-7 Common mode gain

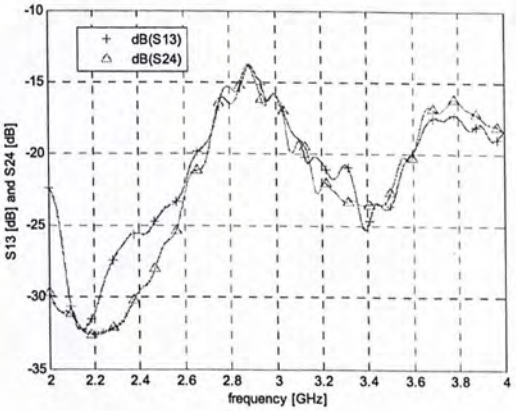

Fig. 3.6-8 Common mode isolation

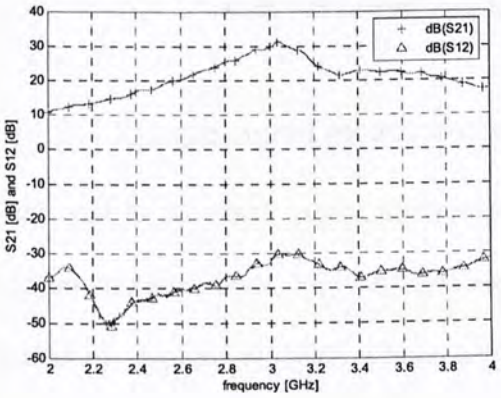

Fig. 3.6-9 Differential mode gain and isolation

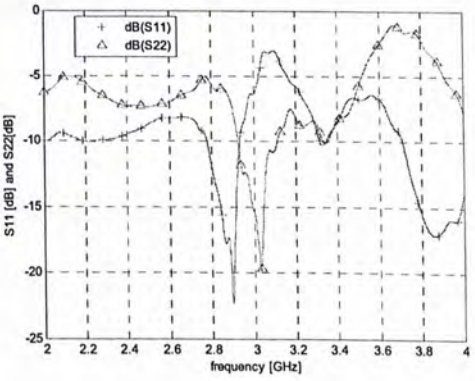

Fig. 3.6-10 Differential mode return loss at input and output

The K-factor and Δ are shown in Fig. 3.6-11. By (2.31) to (2.34), it can be shown that the PA is potentially unstable. Therefore, the stability depends on the input and output termination. From the Fig. 3.6-11, the location of S_{11} and source stability circle and the location of S_{22} and load stability circle show that PA is stable in this input and output termination.

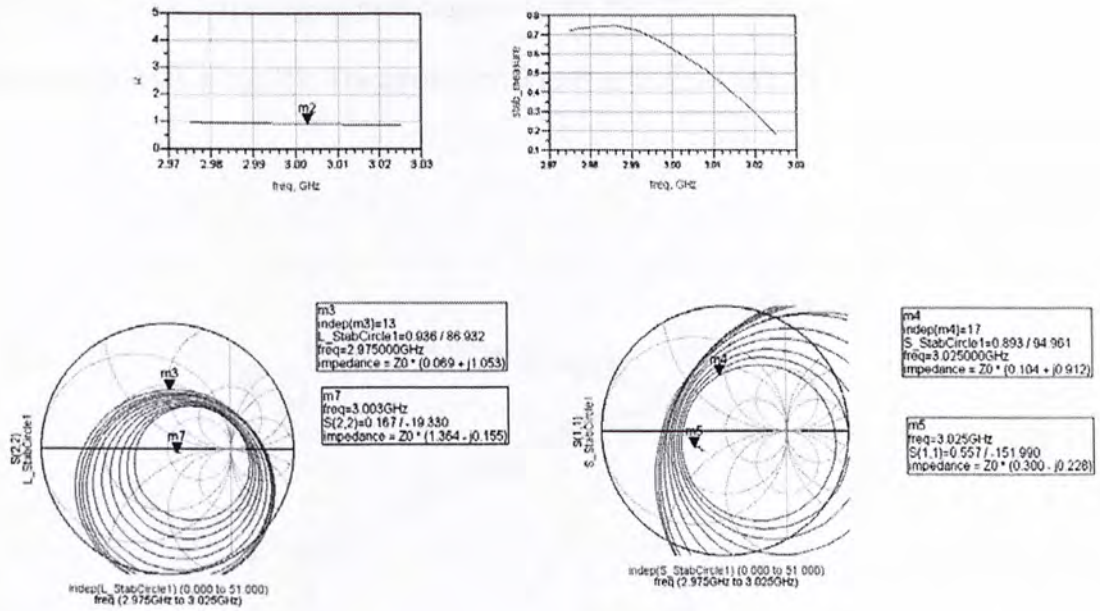

Fig. 3.6-11 Stability analysis (top left: K-factor, top right: Δ, bottom left: output reflection coefficient and load stability circuit, bottom right: input reflection coefficient and source stability circuit

3.4.2Large signal measurement

In additional to the small signal measurement, the PA is tested with fixed frequency tone of 3-GHz with different power level. Fig. 3.6-12 shows the measurement setup in the tone test. The input signal is generated by Agilent N5182A vector signal generator. The input signal is split by offchip balun. Another offchip balun is used at the output to combine differential signal into the single-end signal. As mentions before, all the power loss of the cables and the offchip baluns are calibrated before the measurement.

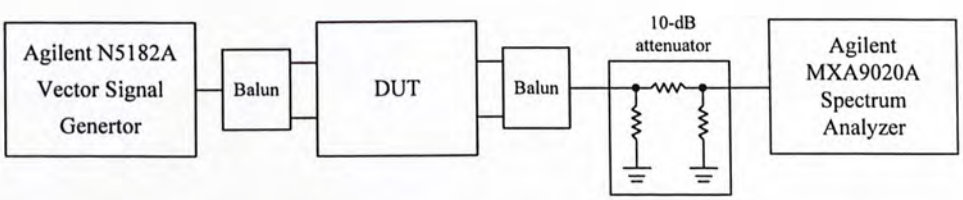

Fig. 3.6-12 Large signal measurement configuration

Fig. 3.6-13 shows the large-signal performance of the PA. The PA delivers a saturated power P_{SAT} of 20.6 dBm with a PAE of 12.7%. The small-signal gain is 27.9 dB and the OP1dB is 14.72 dBm.

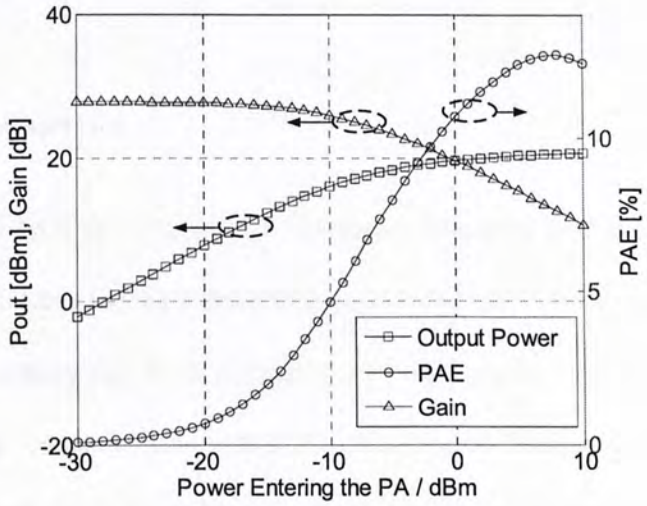

Fig. 3.6-13 Large signal performance

3.4.3Modulation measurement

The PA was also tested with IEEE 802.11a, (WLAN) 54 Mbps, 64-QAM-OFDM signals and IEEE 802.16e (Mobile WiMAX) 64-QAM-OFDM signals. The block diagram of the measurement setup is shown in Fig. 3.6-14. The modulated RF signal is generated Agilent N5182A vector signal generator which is controlled by Agilent N7615B signal studio software for 802.16 WiMAX and N7617 for 802.11a at 3-GHz.

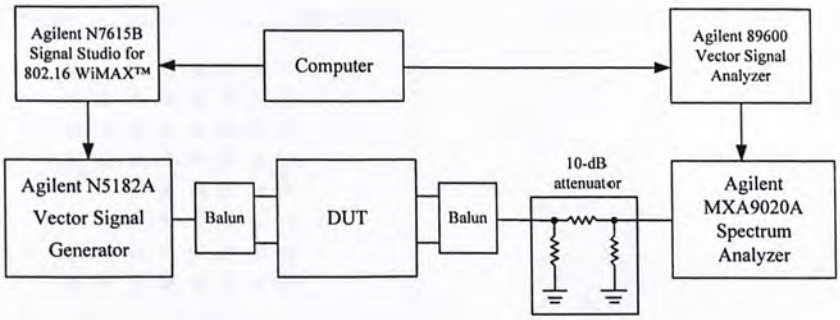

Fig. 3.6-14 Modulation Test configuration

Fig. 3.6-15 and Fig. 3.6-16 show the output frequency spectrum and constellation diagram of the WiMAX and 802.11a Wireless LAN modulated signals captured with the Agilent 89600 vector signal analyzer. The output frequency spectrum complies with the specified spectral mask in both standards. The maximum tolerable constellation errors in WLAN and WiMAX are -25 dB and -30 dB, respectively. The measured EVM of WiMAX and WLAN at the output of the implemented PA are -30.3 dB with an output power of 7.79 dBm and -26.4 dB with an output power of 8.73 dBm, respectively.

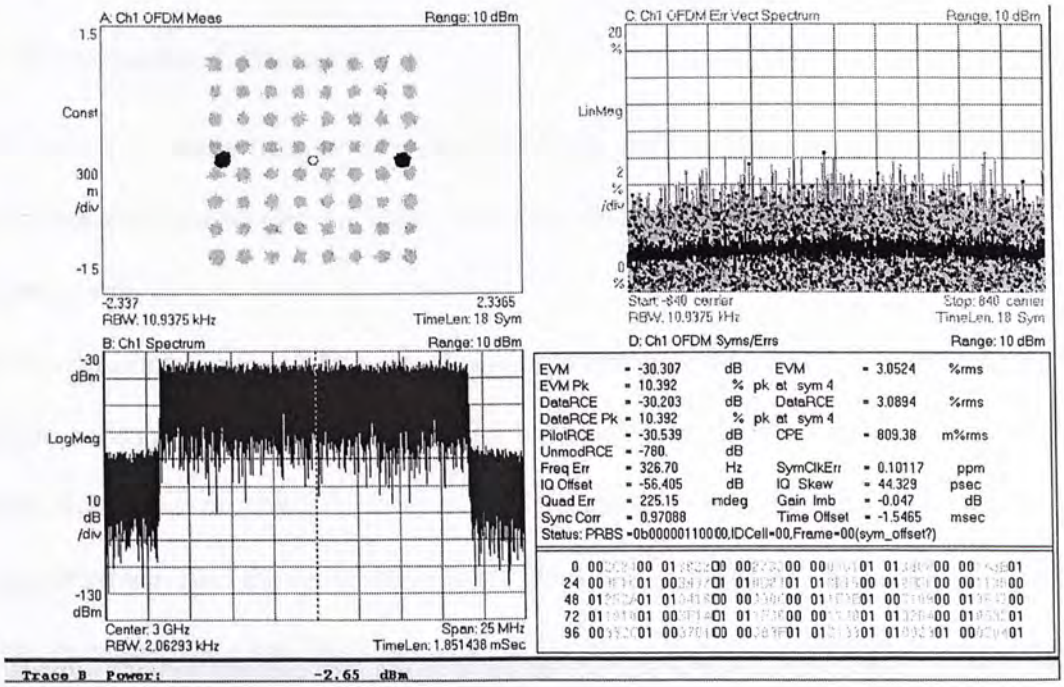

Fig. 3.6-15 Constellation Diagram and Output Spectrum of the WiMAX output RF signal

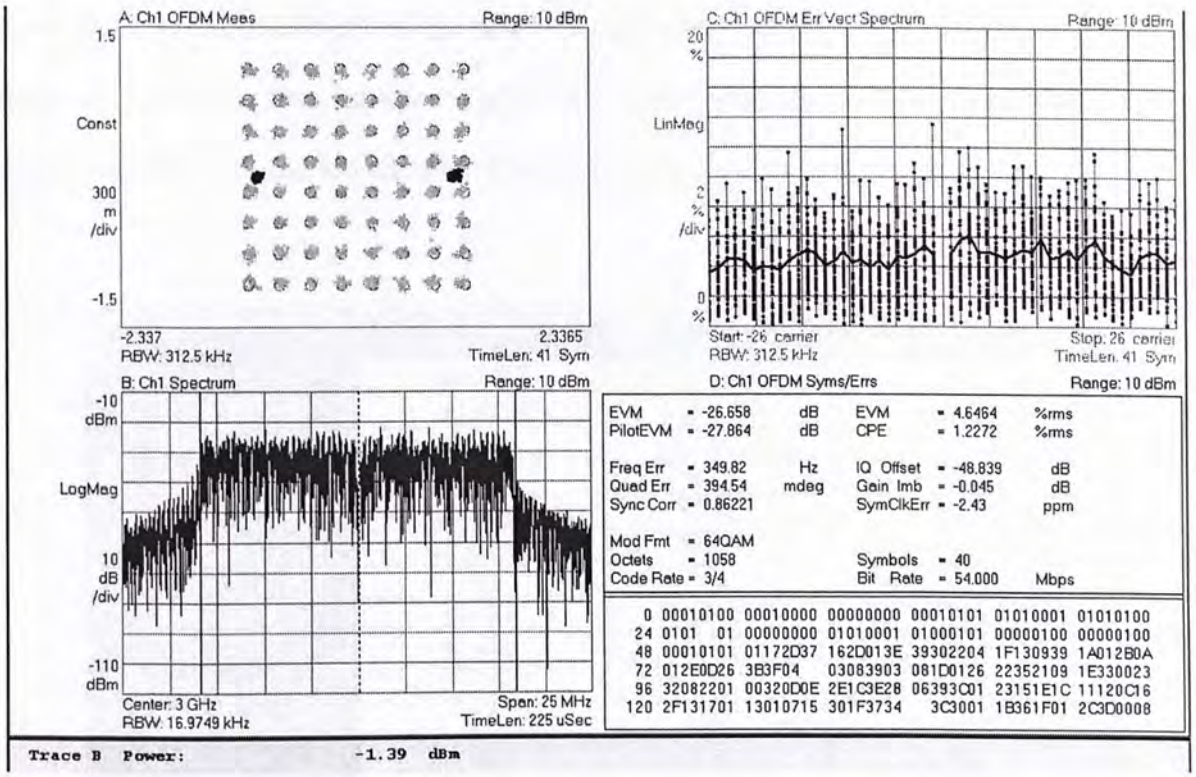

Fig. 3.6-16 Constellation Diagram and Output Spectrum of the IEEE 802.11a output RF signal

3.7 Performance Summary

Table 3-2 show the comparison between the simulation result and measurement. The pre-layout and post-layout measurement results are close. However, there is difference between the post-layout and measurement result.

There are some reasons to the difference. One of the reasons is that the PA is mounted on PCB board. The parasitic resistance along the transmission line may degrade the output power. In addition, the transmission lines may transform the termination impedance to other position in the smith chart, which has less output power. And the input match is not good in order to minimize the return signal.

In addition, there may be some process variation that the parasitic source resistance is larger than the case in the post-layout simulation. During the measurement, the power ground voltage is about 200 mV.

However, there is only 1.578 mV at the source of the power transistor. The parasitic resistance along the metal wires is larger than expected. The ground metal is still not enough to minimize the parasitic resistance even both M4 and M5 are used. The ground wires should be wider or thicker.

Table 3-2 Comparison between the pre-layout, post-layout simulation and measurement result

	Pre-layout @ 3G	Post-layout @3G	Measurement @ 3G
Psat [dBm]	24.0762	24.7746	20
P1dB [dBm]	-11.9796	-12.1258	-12
OP1dB [dBm]	19.054	21.2942	14.72
linear gain [dB]	32	34.4	27.89
gain @ P1dB [dB]	31.0338	33.42	26.72
PAE @ P1dB [%]	11.06946	18.253	3.43
PAE @ Psat [%]	36	34	12.67
DR power [W]	66.4m	65.5m	54m
PW power [W]	615m	611m	808m
Cin / fF	200	1	N.A.
Lg / nH	4.5	3.5	N.A.
Cd / F	2p	1f	N.A.
code	b'111'	b'000'	b'010'

3.8 Reference

[1] S.C. CRIPPS, *RF Power Amplifier for Wireless Communications,* 1st ed. 685 Canton Street, Norwood, MA 02062, Boston, U.S., Artech House, Inc.

[2] I. Aoki *et al.*,"Distributed active transformer-a new power-combining and impedance-transformation technique," *IEEE Trans. Microw. Theory Tech.*, vol. 50, no. 1, pp. 316-331, Jan. 2002.

[3] Tirdad Sowlati and D. M. W. Leenaerts:, "A 2.4 GHz 0.18-μm CMOS Self-Biased Cascode Power Amplifier," *IEEE J. Solid-State Circuit*, Vol. 38, No. 8, pp 1318-1324, Aug. 2003.

4. Circuit Design of Transmitter Front-End

4.1 Introduction

Mobile WiMAX (IEEE 802.16e-based standard) is a new broadband wireless communication standard based on orthogonal frequency division multiplexing (OFDM). This standard enables long transmission distance, high data rate and multiple accesses [1]. As mentioned in Chapter 1, the frequency bands of the WiMAX standard are ranged from 2.3 GHz to 3.8 GHz with different band classes and power classes, as well as with scalable bandwidth requirement in between 1.25 MHz and 20 MHz [2]. This outstanding standard is believed to be a very promising wireless communication standard in the next decade.

However, recent research works on the WiMAX standard such as the designs reported in [3]–[6] only focus on the receiver design and the transceiver design but not including the power amplifier (PA). General approach is to use off-chip passive components or non-CMOS devices such SiGe BiCMOS devices to implement the PA [7]. They have higher transition frequencies compared with CMOS devices, but much more expensive. Undoubtedly, PA implemented in the CMOS technology is a challenging design topic. It needs to achieve high output power and high efficiency under limited DC current density, low supply voltage and low breakdown voltage in the CMOS technology. Under the low supply voltage, conjugate matching is not a suitable approach to have high output power. Therefore, an optimum output resistance is required to be determined carefully. Furthermore, the output should be connected to a single-end antenna. However, most of the circuit blocks implemented in the CMOS technology are differential structures for sake of suppressing the even harmonic, common mode noise and more than 3-dB power gain. Differential output mismatches due to bondwire effect can hardly be cancelled out if off-chip balun is used. An on-chip differential-to-single-end output matching network is therefore essential.

In Chapter 3, a power amplifier prototype is designed and measurement. It is known the layout of the ground wires, location of the power transistors and the all the signal port should be critical to the measurement. The location of the output port of the PA cause difficulty in design test PCB. And the effect of off chip balun cannot be taken into account. These problems are addressed in this design.

In this chapter, a fully integrated CMOS transmitter front-end circuit, including a CMOS RF main amplifier with on-chip LC balun, is proposed. The frequency band is ranged from 2.496 GHz to 2.69 GHz, which is Band Class 3. The work is tested with LO of 2.5 GHz under the large signal measurement. In addition, WiMAX baseband signal with different input power and bandwidth are also measured.

4.2 Topology of the Transmitter Front-End Design

A transmitter is composed of PA, mixer, channel selection filter and digital-to-analog convertor. There are several architectures to implement the transmitter. The most common used architecture in the integrated circuit is the direct conversion architecture as shown in Fig. 4.2-1.

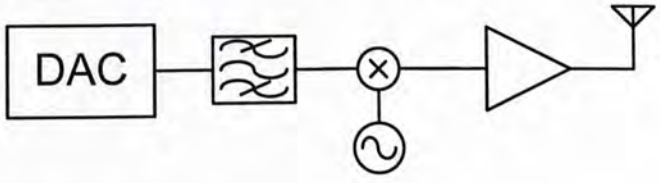

Fig. 4.2-1 Simple direct conversion transmitter

The advantage of the direct converstion transmitter architecture is that no high-quality bandpass filter is required. The order of those filter is more than 2 and it is impossible to implement in semiconductor technology. As a result, a direct-conversion architecture is chosen for the design of the proposed transmitter front-end design, as shown in Fig. 4.2-2. Although this architecture suffers from the problem of LO feedthrough, it is not a critical issue in the OFDM scheme, as the DC subcarrier is not

used. All the on-chip components, including the I/Q modulator, driver and main amplifier, operate in differential modes to suppress the LO feedthrough and even harmonics. In addition, in the direct conversion transmitter, the number of gain stage required is less than other architecture such as low-IF conversion and superheterodyne architecture. The transmitter is more linear if less gain stage is used under the following condition.

$$\frac{1}{IIP3_T} \approx \frac{1}{IIP3_1} + \frac{A_1}{IIP3_2} + \frac{A_1 A_2}{IIP3_3} + \ldots \tag{4.1}$$

where $IIP3_i$ is the 3-order input referred intermoduation product of i stage

A_i is the gain of i stage

The baseband signal is firstly up-converted by the I/Q modulator, and then the signal is sent out by the RF driver and PA. Parallel resonator is added as loading between the I/Q modulator and the driver stage, and between the driver stage and the power stage. The resonator can filter out the higher harmonics generated along the transmission path and improve the power gain of the whole circuit.

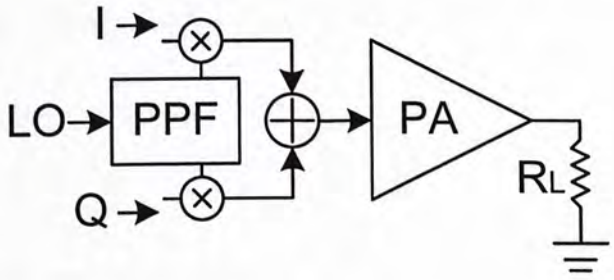

Fig. 4.2-2 Proposed on-chip direct conversion transmitter

Suppose a complex baseband signal (4.2) is being up-converted. As the direct conversion architecture is chosen, the I and Q baseband signals (4.3) and (4.4) are directly upconverted to that complex LO frequency.

$$x(t) = A(t)e^{j\theta(t)} = A(t)\left[\cos(\theta(t)) + j\sin(\theta(t))\right] \tag{4.2}$$

$$I(t) = A(t)\cos(\theta(t)) \tag{4.3}$$

$$Q(t) = A(t)\sin(\theta(t)) \tag{4.4}$$

$$A(t) = \sqrt{I^2(t) + Q^2(t)} \tag{4.5}$$

$$\theta(t) = \tan^{-1}\frac{Q(t)}{I(t)} \tag{4.6}$$

$$v_{LO}(t) = A_{LO}e^{j2\pi f_{LO}t} = A_{LO}(\cos 2\pi f_{LO}t + j\sin 2\pi f_{LO}t) \tag{4.7}$$

The upconverted real and imaginary parts are shown in (4.9) and (4.11). The upper sideband signal (4.12) is generated by substracting real part with the imaginary parts.

$$v_{RFI}(t) = A_{LO}A(t)\cos(2\pi f_{LO}t)\cos(\theta(t)) \tag{4.8}$$

$$= \frac{1}{2}A_{LO}A(t)\left[\cos(2\pi(f_i + f_{LO})t + \theta'(t)) + \cos(2\pi(f_i - f_{LO})t + \theta'(t))\right] \tag{4.9}$$

$$v_{RFQ}(t) = A_{LO}A(t)\sin(2\pi f_{LO}t)\sin(\theta(t)) \tag{4.10}$$

$$= \frac{1}{2}A_{LO}A(t)\left[\cos(2\pi(f_i - f_{LO})t + \theta'(t)) - \cos(2\pi(f_i + f_{LO})t + \theta'(t))\right] \tag{4.11}$$

$$v(t) = v_{RFI}(t) - v_{RFQ}(t) = A_{LO}A(t)\cos(2\pi(f_i + f_{LO})t + \theta'(t))$$

$$= A_{LO}A(t)\left[\cos(2\pi(f_i + f_{LO})t + \theta'(t))\right] \tag{4.12}$$

where $\theta(t) = 2\pi f_i t + \theta'(t)$

But the flick noise at the baseband signal is also upconverted to the desired frequency band. Fortunately, the WiMAX is an OFDM system so that the DC subcarrier is not used. Fig. 4.2-3 shows the signal flow in the frequency domain. The complex baseband signal is first convoluted with the complex LO signal under the single-sideband mixer. The complex resultant RF signal is formed. The real signal is formed at the node that the real and imaginary parts are added together.

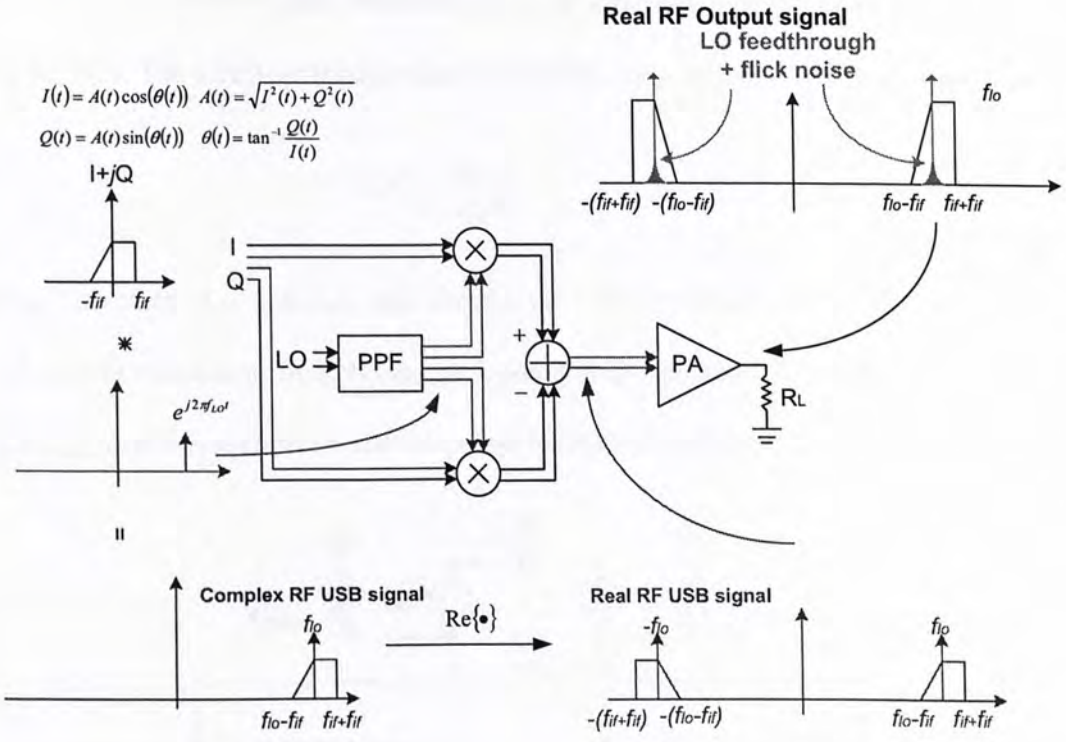

Fig. 4.2-3 The signal flow graph of the transmitter front-end circuit

4.3 Design in transmitter front-end circuit

4.2.1I/Q Modulator

The mixer should have high linearity requirement with sufficient gain, as it should not be saturated before the PA saturates. Therefore, the I/Q modulator is composed by two active mixers, rather than passive mixers. Four-phase LO signals are needed and they are generated from differential LO signals by a three-stage polyphase filter. The differential LO is generated by an offchip balun, which is a ratrace hybrid coupler. It is noted that the polyphase filter is used for measurement purpose only. In the single-chip transceiver, the signals are provided by a frequency synthesizer.

Fig. 4.3-1 shows the schematic of the proposed I/Q modulator. The linearity of the mixer is improved by the degeneration resistor R_b but the gain is degraded. By (4.1), the linearity can be improved if the

gain of the 1st stage is not too high. However, the gain cannot be too low since the output noise of the mixer may be high. The effective transconductance of M_{5a}, M_{5b}, M_{6a} and M_{6b} is shown below

$$G_m = \frac{g_m}{1 + g_m R_b} \tag{4.13}$$

The loading inductors (L_{d1} and L_{d2}) can double the output voltage swing. It can also improve the linearity of the I/Q modulator. In addition, the loading inductors and the switched capacitor array (SCA) C_{SCA1} and C_{SCA2} form a resonator to filter out other higher harmonics.

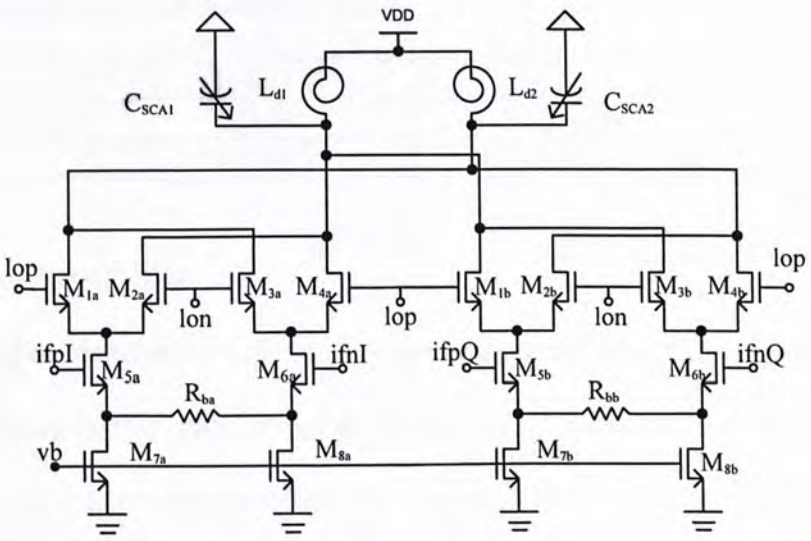

Fig. 4.3-1 I/Q Modulator

The list of the transistor sizes and components values are shown as follows:

$M_{1a,b}$	100μ/0.18μ	$M_{2a,b}$	100μ/0.18μ	$M_{3a,b}$	100μ/0.18μ	$M_{4a,b}$	100μ/0.18μ
$M_{5a,b}$	150μ/0.36μ	$M_{6a,b}$	150μ/0.36μ	$M_{7a,b}$	200μ/0.36μ	$M_{8a,b}$	200μ/0.36μ
$R_{ba,b}$	712.2 Ω	$L_{d1,2}$	1.654 nH				

The three-stage polyphase filter is shown in Fig. 4.3-2. The four-phases LO signals are created from the differential LO signals. The filter is for measurement purpose only when a quadrature VCO is available.

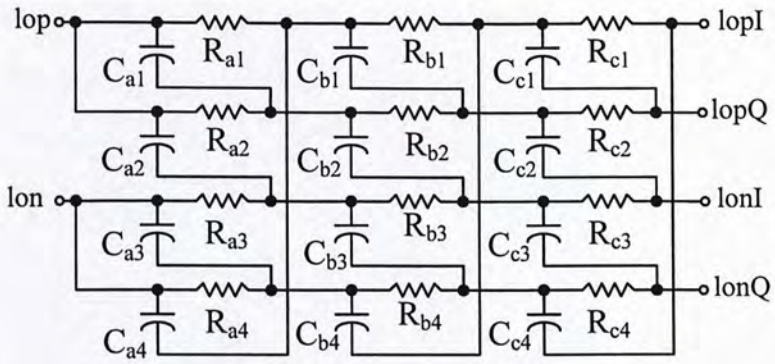

Fig. 4.3-2 3-stage polyphase filter

The values of the components are listed as follows

$R_{a1,2,3,4}$	188 Ω	$C_{a1,2,3,4}$	229.5 fF
$R_{b1,2,3,4}$	273 Ω	$C_{b1,2,3,4}$	229.5 fF
$R_{c1,2,3,4}$	397 Ω	$C_{c1,2,3,4}$	229.5 fF

4.2.2Power Amplifier

The power stage of the transmitter front-end circuit is designed using the methodology introduced in Chapter 3. The output power is highly dependent on the output matching, supply voltage and the supply current. However, the supply voltage, breakdown voltage and DC current density limit are decreasing under the scaling down technology.

In order to have higher output power, the power stage transistors are terminated with a resistance lower than 50 Ω. Furthermore, in order to eliminate the offchip balun at the output port, a on-chip *LC* balun is built in the chip.

As there is a large parasitic capacitance is introduced by a large *W/L* ratio of transistors in the power stage. Thus, a driver stage is added between the I/Q modulator and the main amplifier. The driver stage also provide the power gain. The overall schematic of the PA is shown below.

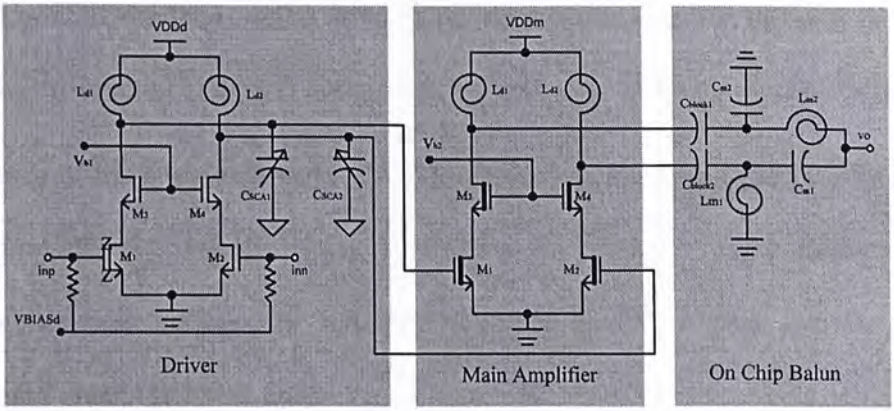

Fig. 4.3-3 Overall schematic of PA

The output of the driver stage connects to the input of the power stage directly. The configuration can minimize power loss between two stages. The biasing voltage of the power transistors at the power stage is adjusted through the supply of the driver stage. Therefore, one bond pad is saved.

The main amplifier is composed of a differential cascode amplifier, an on-chip power combining balun and gate-controlled circuit (GCC), as shown in Fig. 4.3-5. In the power stage, the thick-oxide transistor is used to withstand 3.3-V supply voltage. The thick-oxide transistor has high threshold voltage and breakdown voltage. Although the knee voltage is increased due to higher threshold voltage, the voltage swing can be enhanced because of higher breakdown voltage and it has more reliable. However, the thick-oxide transistor suffers from larger gate capacitance and lower transition frequency. The transconductance of the transistors is degraded, but it is still acceptable in this application. The loading inductors at the driver stage is smaller to resonate out the large gate capacitance. And the power gain of the driver stage is reduced

A gate-controlled circuit (GCC) is used to tune out the process variation at the cascode transistors M_3 and M_4. The GCC adjust the gate voltages of M_3 and M_4 to control the drain current through them. L_{d1} and L_{d2} are used on-chip to have better differential matching. As the sources of the power transistors

are connected to ground, the large signal differential current is the same as those in (3.12). By keeping V_{DDd} constant, the differential current is linear with the change of different input voltage.

As the gate voltage of the cascode transistors at the power stage is larger than the nominal voltage of the technology provided (i.e. 1.8 V), so that the GCC is also designed using thick-oxide transistor to withstand the high supply voltage. By varying the voltage reference V_{BIAS_m} in the GCC, the drain current at the power stage can be varying.

A LC lattice-type balun is implemented on-chip for differential power combining, as reported in [9]. The on-chip balun can have better efficiency when comparing with the LC loadpull matching. The LC balun will be discussed in the next secion. Beside the design of LC balun, the optimum output resistance value is needed to be found. It is found out by using the parametric simulation with Cadence Spectre-RF simulator. The transistor size is fixed at the simulation. As the gate capacitance of the power transistors increase if the aspect ratio increase. Although a driver stage is added, the gate capacitance cannot be too large; otherwise, the loading inductors at the driver stage cannot resonate out the gate capacitance at the desired center frequency. On-chip inductors with small inductance values are easily affected by the process variation. The on-chip inductos should not be smaller than 1nH.

As the on-chip inductors at the foundary design kit may not be suitable to be used for the power amplifier design, the inductors may need to be tailor-designed by either using metal 5 and metal 6 stack together or enlarge the width of the inductors. Both of the design methods need 3-D electromagnetic (EM) simulation. Extra time is needed to study the 3-D EM simulation and one more run of wafer is required to test the inductors. Therefore, the on-chip inductors from the foundry are used eventually.

The simulation result is shown below.

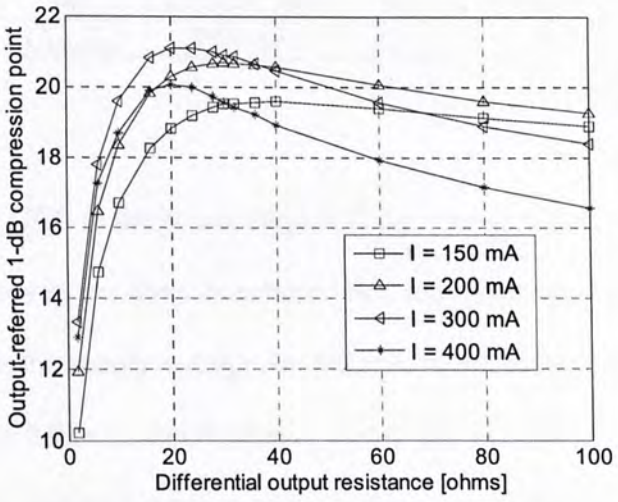

Fig. 4.3-4 Parametric simulation of 1-dB compression point versus differential output resistance

It is shown in the above figure that the power stage can deliver largest amount of power with drain current of 400 mA. However, the technology cannot withstand too high DC current. Finally, the drain current of 200 mA is choosn according to the limitation listed by the foundary, and the optimum output resistance is set to around 15 Ω.

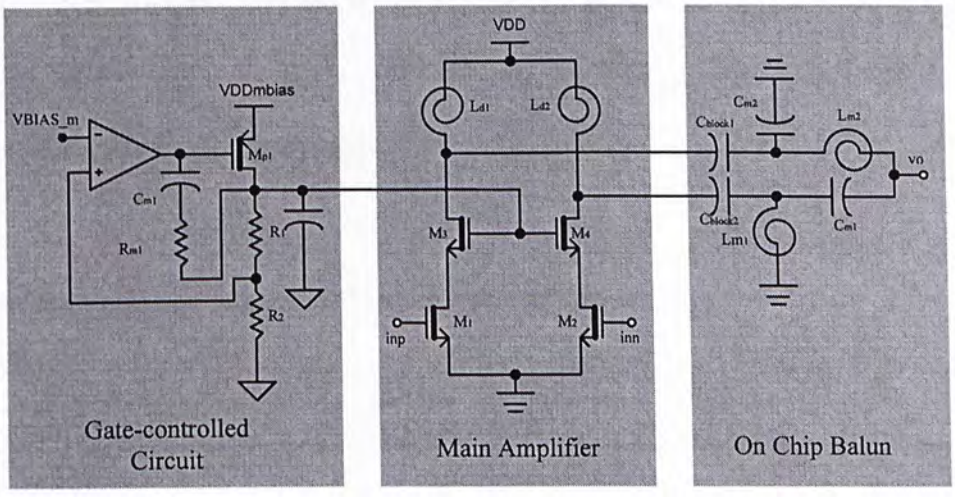

Fig. 4.3-5 Power Stage with on-chip balun and gate-controlled circuit

The transistors sizing and components values of the main amplifier and on-chip balun are listed as follows:

M_1	1200μ/0.34μ	M_2	1200μ/0.34μ	M_3	1200μ/0.34μ	M_4	1200μ/0.34μ
$L_{d1,2}$	1.21 nH	$C_{block1,2}$	39.4 pF	$L_{m1,2}$	2.469 nH	$C_{m1,2}$	1.643 pF

The full schematic of the GCC at the power stage is shown in Fig. 4.3-6. As the output common mode voltage range does not cover the input common mode voltage range, and it is only about 300 mV difference compared with the supply voltage, so that a PMOS transistor is added to form low dropout regulator (LDO) topology. Miller compensation is used to provide enough phase margin to stabilize the circuit. In order to provide required common mode voltage, the supply of the GCC is set to be 3.6 V.

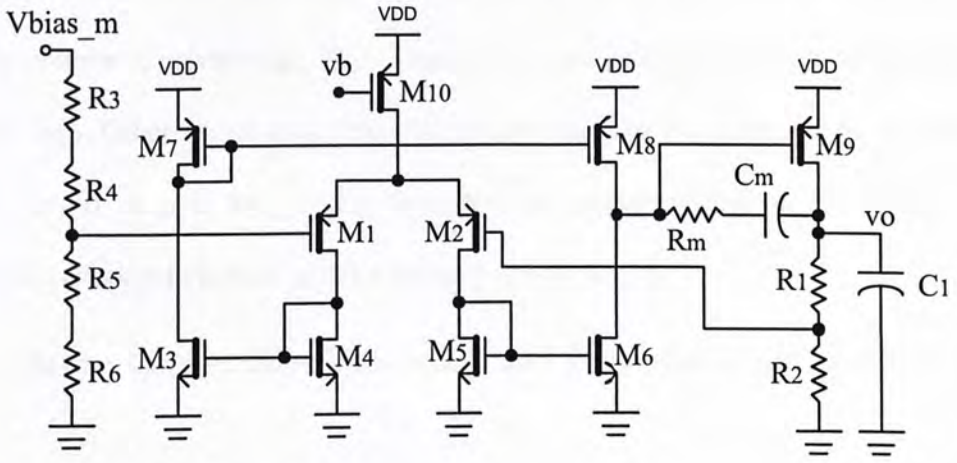

Fig. 4.3-6 Full schematic of gate-controlled circuit in power stage

The transistors sizes and components values are listed as follows:

$M_{1,2}$	60μ/1μ	M_3-M_6	8μ/1μ	M_7-M_8	24μ/1μ	M_9	10μ/0.34μ
M_{10}	96μ/1μ	R_m	20.1 kΩ	R_1-R_6	105.824 kΩ	C_1	10.4 pF
C_m	4 pF						

The driver stage is shown in Fig. 4.3-7. It is added to drive the large gate capacitance of the power transisors at the power stage. In addition, the driver stage provide gain. The power gain depends on the Q factor of the resonator formed by the C_{SCA}, C_{G_PW} and L_d.

$$f = \frac{1}{2\pi\sqrt{L_d\left(C_{SCA} + C_{G\_PW}\right)}} \tag{4.14}$$

where C_{SCA} is the capacitance at the SCA

C_{G_PW} is the gate capacitacne of the power transistors at the power stage

L_d is the loading inductor at the driver stage

The driver stage consists of both the source-grounded differential amplifier and the GCC. As discussed in the previous section, the source-grounded is more linear with constant V_{GS1} and V_{GS2} compared with the differential amplifier with tail current source, with the limitation of poor common mode rejection. As the supply voltage of driver stage V_{DDd} is used to bias the power transistors at the power stage, V_{DDd} cannot be too high. Otherwise it may drive the power transistor to linear region. Although the supply voltage at the driver stage is low, on-chip inductors are added as loading. The voltage swing can be doubled with the on-chip inductors and the linearity is maintained.

The voltage reference V_{BIAS_d} could be adjusted to control the effective G_m of the differential pairs (M_1 – M_4).

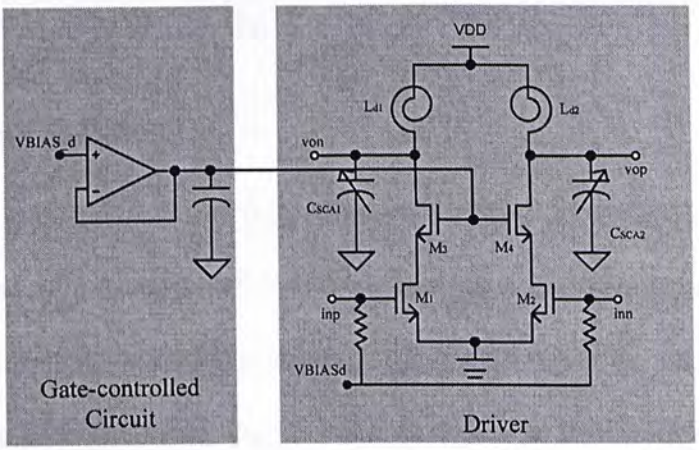

Fig. 4.3-7 Driver Stage and the Gate-controlled Circuit

The transistor sizing and the component values are shown as follows:

M_1-M_4	600μ/0.18μ	$L_{d1,2}$	955.4 pH	$R_{bias1,2}$	2.56 kΩ		

The full schematic of the gate-controlled circuit at the driver stage is shown in Fig. 4.3-8. A current-mirror amplifier is used as the OTA in unity-gain configuration. A loading capacitor C_1 is used to provide dominant compensation to the gate-controlled circuit. The GCC is work under the supply voltage of 1.8 V. As the output voltage required is about 1.27 V, so that this GCC does not need to be designed using thick-oxide transistor.

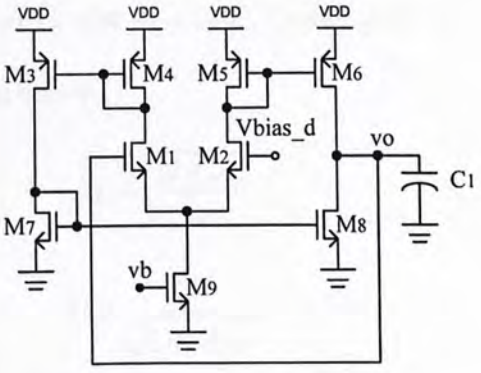

Fig. 4.3-8 Full schematic of gate-controlled circuit in driver stage

The transistor sizes and the component values are shown as follows:

M_1-M_2	5.2μ/0.5μ	M_3-M_6	42μ/0.5μ	M_7-M_8	5.2μ/0.5μ	M_9	10.4μ/0.5μ

4.2.3On-chip LC Balun

As the supply voltage is only 3.3 V, the output power is limited by the load resistance. More output power can be delivered if it is terminated with output resistance less than 50 Ω. The impedance transformation can be implemented by *L*-match or *LC* balun. However the output of a transmitter is an antenna which is single-end. Therefore, the *LC* balun is chosen in this design because it can eliminate the usage of the off-chip balun and provide impedance transformation. The ideal on-chip *LC* balun is shown as follow.

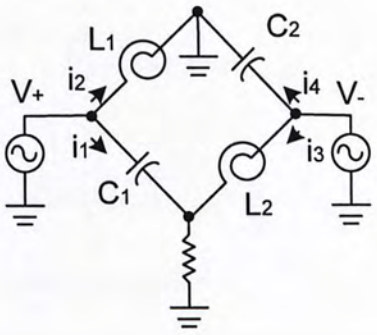

Fig. 4.3-9 LC balun

To ensure the phase difference of V_+ and V_- is 180°, L_1 should be equal to L_2 and C_1 should be equal to C_2. The design equation is listed below.

$$L = \sqrt{\frac{2R_L Z_i}{\omega^2}} \tag{4.15}$$

$$C = \frac{1}{\sqrt{2R_L Z_i \omega^2}} \tag{4.16}$$

However, the Q-factor of the on-chip inductor is typically around 8-10, so that the model of the LC-balun is needed to modify to model the loss.

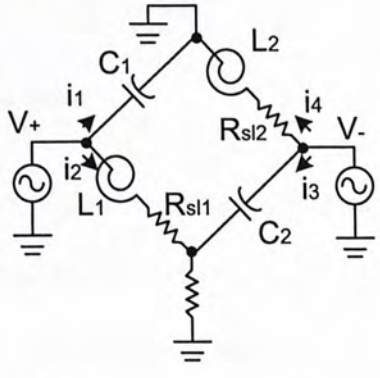

Fig. 4.3-10 LC balun model including loss in inductor

The resonant frequency is shifted to lower frequency due to the parasitic resistance at the on-chip inductor. The condition is given by

$$C = \frac{L}{R_{sl}^{\ 2} + (\omega L)^2} \tag{4.17}$$

$$f_o = \frac{1}{2\pi}\sqrt{\frac{1}{LC}\frac{Q_L^{\ 2}}{1+Q_L^{\ 2}}} \tag{4.18}$$

where Q_L is the quality factor of the on-chip inductor

From (4.18), if the quality factor is too low, the resonant frequency, f_o is shifted to lower frequency.

4.4 Simulation Result of the Transmitter Front-End Design

The design is simulated using Cadence Spectre-RF simulator which is efficient for simulating the RF circuit. The output 1-dB compression point (O1PdB), saturated power (P_{SAT}), linear gain, and power-added efficiency (PAE) can be found out by using the periodic steady-state analysis. The simulation schematic is shown below.

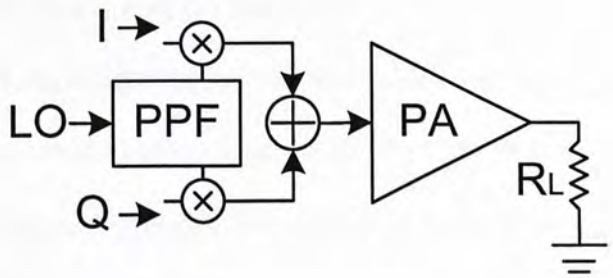

Fig. 4.4-1 Simulation schematic of the transmitter

All the inputs of *I* channel, *Q* channel and LO signals are differential signals. In the tone simulation, the IF frequency is set to 5 MHz and the LO signals is set to 2.5 GHz. The frequency of output signal is 2.505 GHz. The image of the output signal is about 2.495 GHz.

The LO feedthrough and sideband suppression can be found out by using transient analysis and then perform fast fourier transform. A quadrature error of 3 degrees at baseband is introduced at the pre-layout and post-layout simulation to model the mismatch. The simulation result is shown in Table 4-1.

Table 4-1 Comparison between the pre-layout and post-layout simulation result

	Pre-layout	Post-layout
P_{sat} [dBm]	23.5	21.65
P1dB [dBm]	-6.42669	2.01796
OP1dB [dBm]	22.0534	21.6013
linear gain [dB]	29.48	20.648
P_{gain} @ P1dB [dB]	28.46	19.58334
PAE @ OP1dB [%]	19.866	17.81
PAE @ Psat [%]	25.7	17.9
mixer_power [mW]	27.4	27.4
DR_power [mW]	53.4	53.4
PW_power [mW]	620	622
LO feedthrough [dBc]	-72.05	-61.8
sideband suppression [dBc]	-35.8	-37.3

4.5 Layout consideration

In Chapter 3, the floorplan of the PA is not good due to chip-area limitation. In this design, the area restriction is less. Therefore, the ground wire is widened to about 40 μm with M4 and M5 layer. Therefore, the parasitic resistance is further minimized.

In addition, all the circuit components are in differential mode, so that the components are needed to keep in the axis of symmetry. In the power stage and driver stage, the on-inductor should be the widest, which is 20 μm to have the highest Q-factor. The number of ground pads should be as many as possible to minimize the parasitic resistance and inductance along the bondwires.

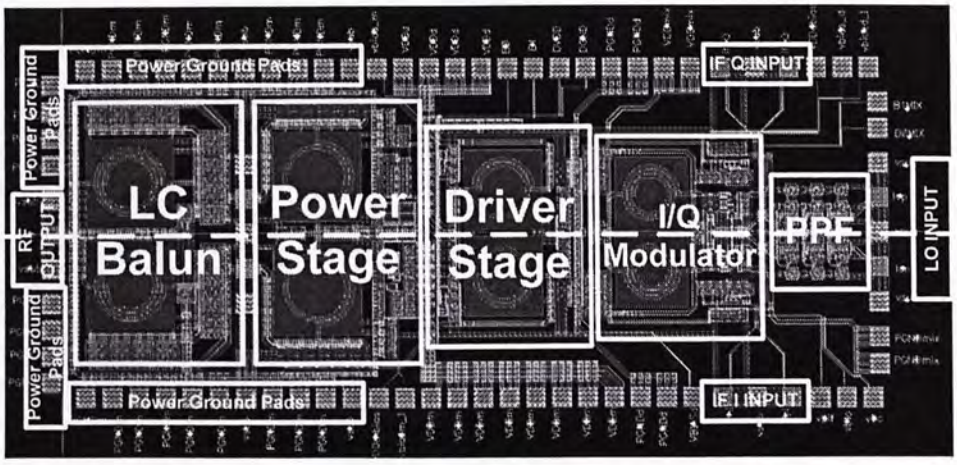

Fig. 4.5-1 Floorplan of the transmitter front-end circuit

The output port is in GSG pads configuration. The differential LO ports are in GSGSG configuration and the differential IF ports are in SGS configuration. They are used for the probing. In addition, the RF signal should flow in one direction only. From Fig. 4.5-1, the LO signal enter the chip from the right hand side and then mixed with the IF components and then output at the left hand side. Therefore, the PPF is placed at the right-hand sides, followed by I/Q modulator, driver stage, power stage and finally the *LC* balun at the left hand side.

In this layout, the numbers of ground pads is about 26 in order to reduce the bondwires inductance to prevent self-oscillation during start up. The power transistors are placed next to the power ground wires in order to reduce the source resistance.

4.6 Measurement Result of the Transmitter Front-End Design

The 2.5-GHz Mobile WiMAX transmitter front-end was fabricated in UMC 1P6M 0.18-μm CMOS process. Fig. 4.6-1 shows the micrograph. The die size is 3734 μm × 1581 μm, including the bonding pads. The transmitter front-end circuit is measured at supply voltages of 1.5 V for the I/Q modulator, 1.27 V for the RF driver and 3.3 V for the RF main amplifier. The differential main amplifier consumes 217 mA. The supply current is less than 100 μA in both GCCs.

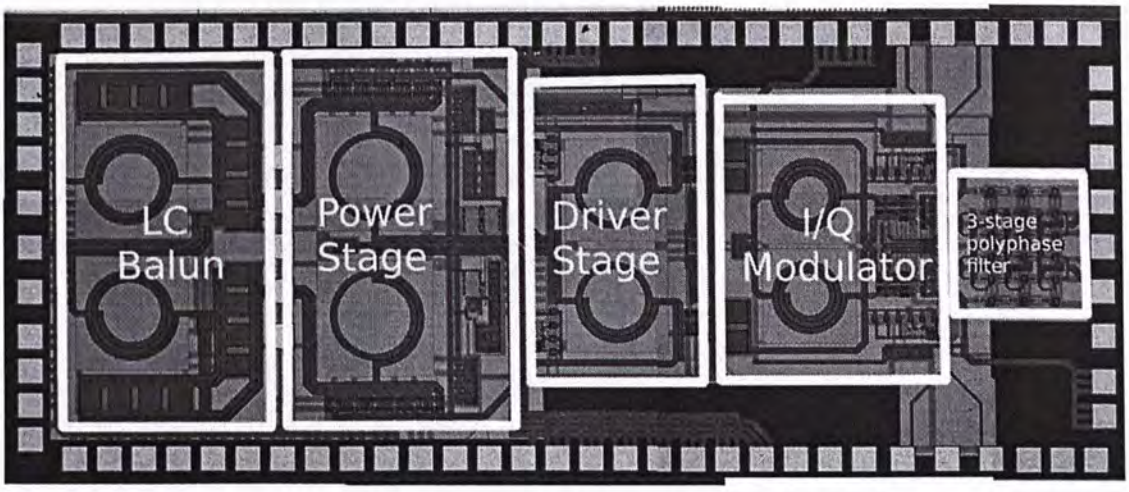

Fig. 4.6-1 Chip Photo

4.4.1. Transmitter Front-End Measurement

4.4.1.1 Output Reflection coefficient

As the transmitter front-end circuit includes a RF power amplifier, the stability issue is the major concern. Since there is a frequency conversion existed in the circuit, so that the *K*-factor cannot be used to determine the stability. One of the methods to study the stability is to investigate the output reflection coefficient (S_{11}), if S_{11} is larger than 1, then the circuit is potentially unstable.

This 1-port *s*-parameter can be measured in the following measurement setup shown in Fig. 4.4.1-1. All the LO and IF input ports are 50-Ω terminated. The 1-port *s*-parameter is measured by Agilent E5071A RF network analyzer.

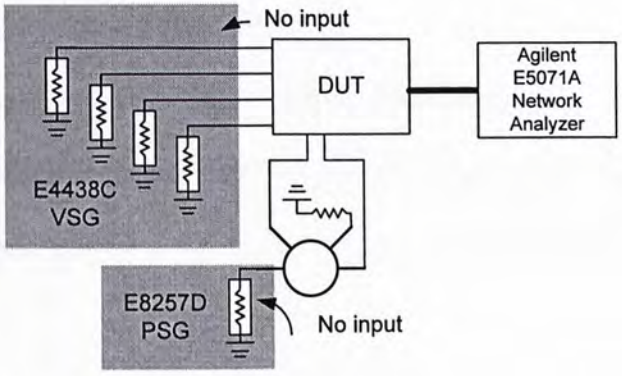

Fig. 4.4.1-1 Measurement setup for reflection coefficient at the output.

Fig. 4.4.1-2 shows the magnitude of output reflection coefficient in dB. As the value is negative within the band of interest, it is proven to be stable. Both the cases which the LO signals is on or off are shown in Fig. 4.4.1-2. There is a LO feedthrough at the 2.5 GHz frequency at the case of LO on.

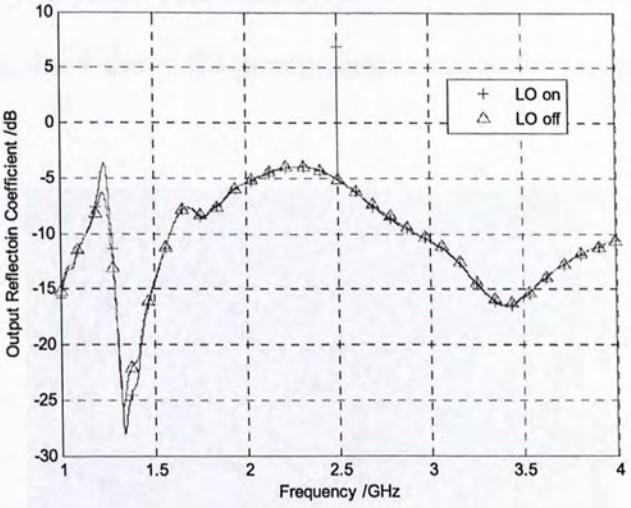

Fig. 4.4.1-2 Output reflection coefficient

4.4.1.2 Large Signal Measurement

This work was measured using Agilent PSA E4400 spectrum analyzer with 10-dB attenuator. The 4-phase quadurate baseband signals are generated by Agilent E4438C ESG Vector Signal Generator. The differential LO signal is generated by a 180° hybrid coupler with the source from Agilent E8257D PSG Analog Signal Generator.

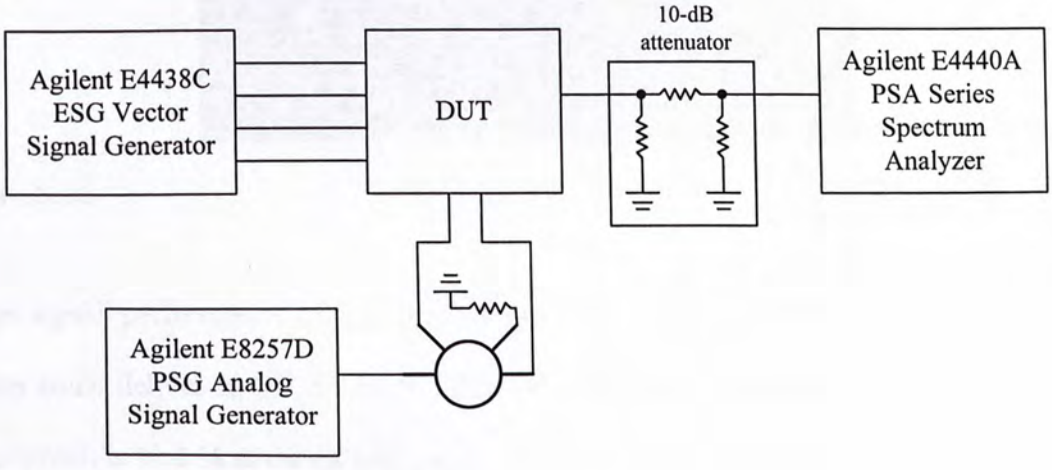

Fig. 4.6-2 Measurement setup for the tone measurement

The die is mounted on a gold-plated FR4 PCB by silver epoxy, and the design is measured in probe station. Fig. 4.6-3 and Fig. 4.6-4 shows the measurement setup in the test bench and the probe station, respectively.

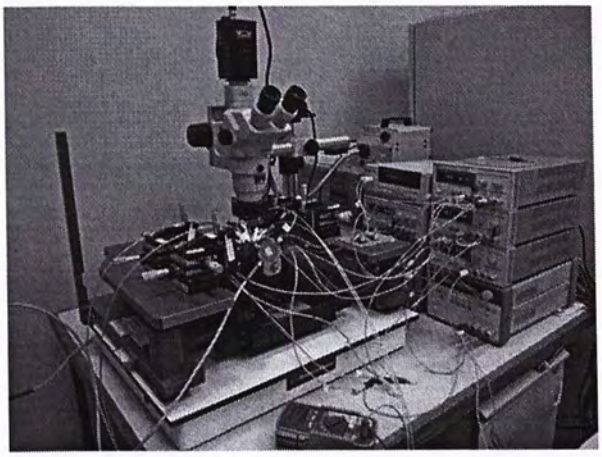

Fig. 4.6-3 Measurement setup in the test bench

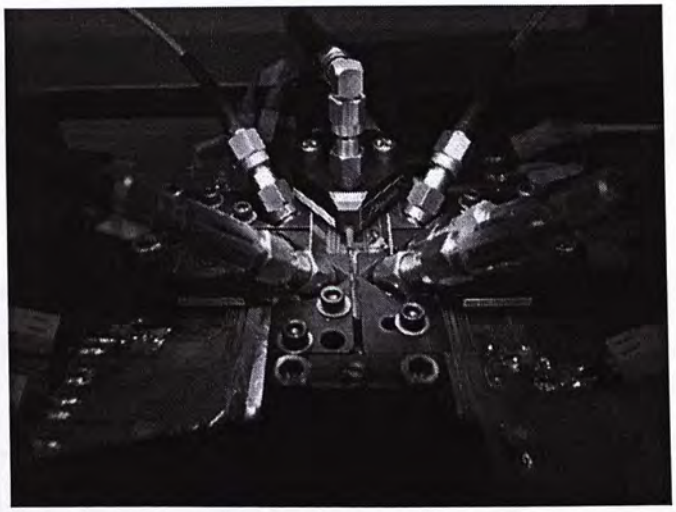

Fig. 4.6-4 Probe station

The large-signal performance of the transmitter at LO of 2.5 GHz is shown in Fig. 4.6-5. The transmitter could deliver an OP1dB of 18 dBm and small-signal power gain of 24 dB. The PAE of the front-end circuit is 10.5 % at the OP1dB point.

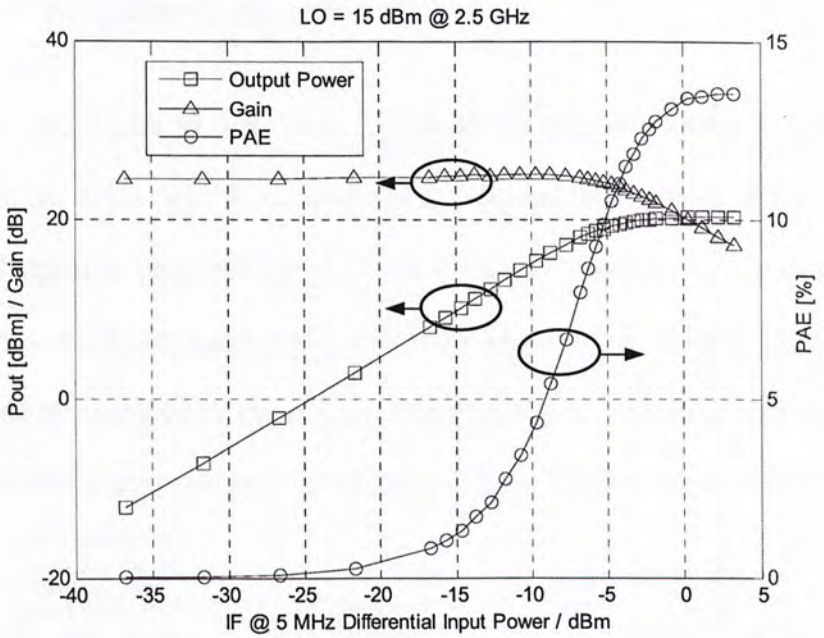

Fig. 4.6-5 Large Signal Performance

Fig. 4.6-6 shows the output spectrum at the 2.5-GHz band. Without any calibration circuit, the measured sideband and LO feedthrough suppression with LO power of 15 dBm are -38.98 dBc and -43.04 dBc, respectively.

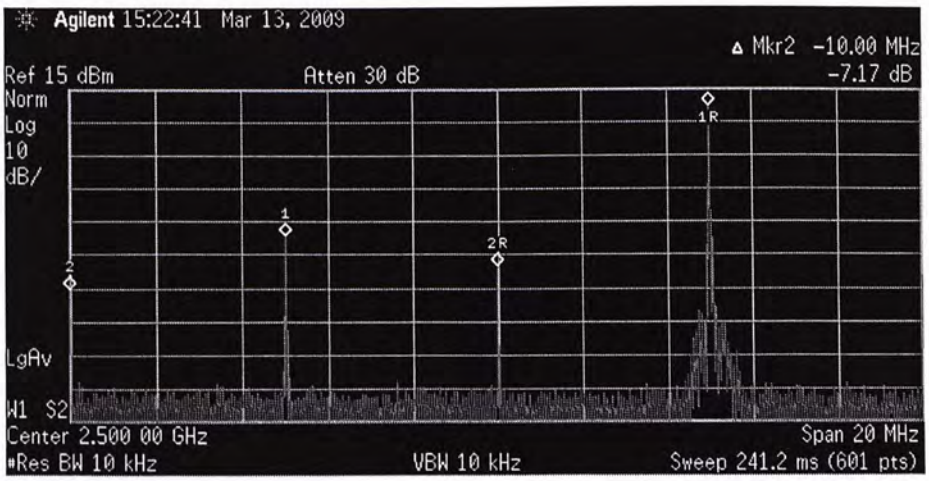

Fig. 4.6-6 LO feedthrough and carrier suppression

4.4.1.3 Modulation Measurement

This work was also tested with 64-QAM-5/6-CTC WiMAX modulated signals with bandwidths of 10 MHz, 20 MHz and 28 MHz. Fig. 4.6-7 shows the measurement setup in the modulation test. The WiMAX baseband signal is generated by the Agilent E4438C ESG vector signal generator, which is controlled by the host computer using Agilent N7615B signal studio for 802.16 WiMAX. The output RF modulated signal is measured by the Agilent E4440 PSA series spectrum analyzer. The signal read in the spectrum analyzer is analyzed by Agilent 89600 vector signal analyzer software.

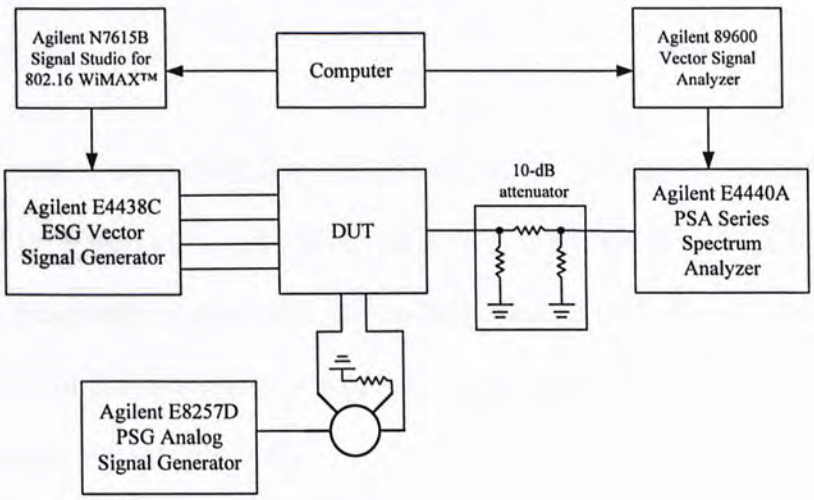

Fig. 4.6-7 Measurement setup for the modulation test

With differential IF input power of -11.7 dBm, the measured EVM are -30.53 dB, -30.52 dB and -30.59 0dB, respectively. Fig. 4.6-8 shows the result of EVM versus IF differential input power. This work fulfills the EVM requirement of -30 dB as shown in [8] with input power less than -11.7 dBm.

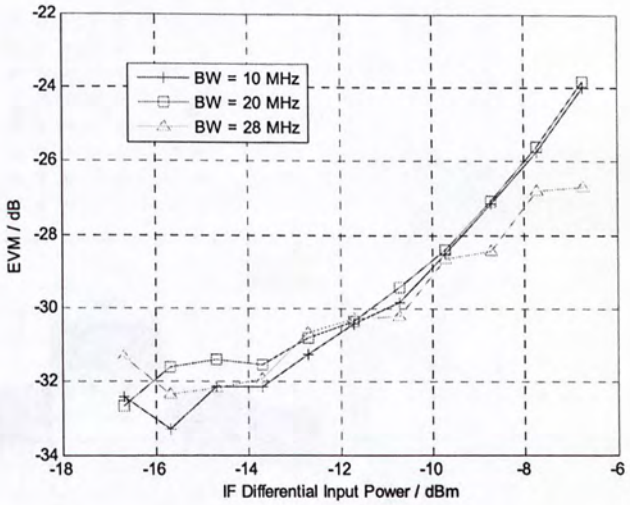

Fig. 4.6-8 EVM vs. IF differential input power

Error! Reference source not found., Fig. 4.6-10 and Fig. 4.6-11 show the constellation diagrams and output spectrum of the transmitter front-end circuit with WiMAX baseband input signal of 10 MHz, 20 MHz and 28 MHz bandwidth respectively. The demodulated data in grey and frame control header in black [10] is shown in the constellation diagram. The center symbol is shown since the zone is demodulated without active subcarrier [11].

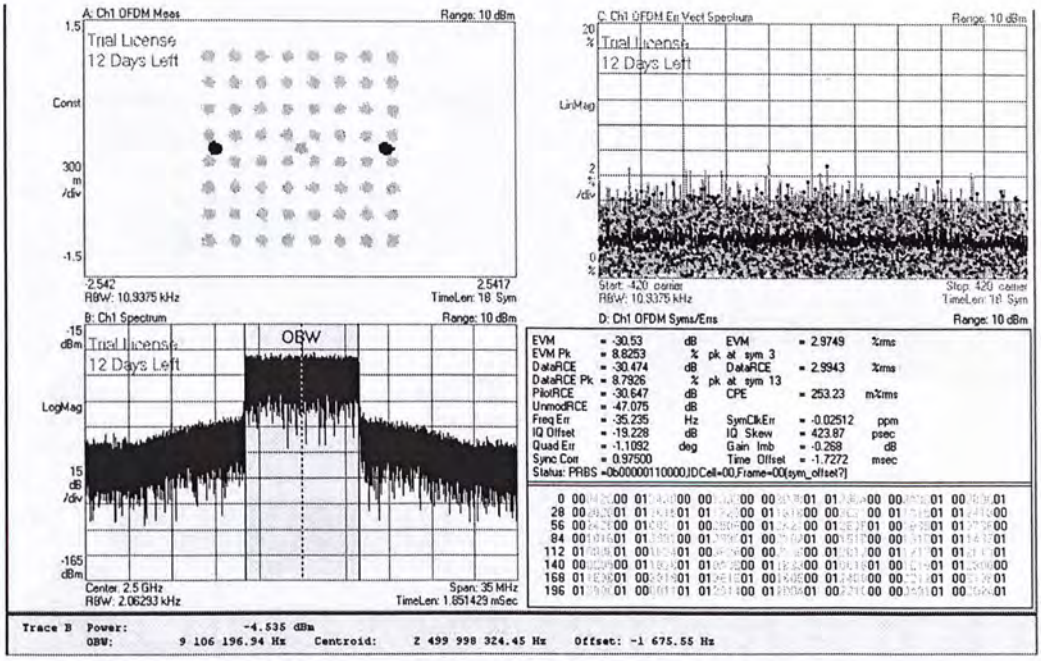

Fig. 4.6-9 WiMAX modulation test with 10-MHz baseband signal

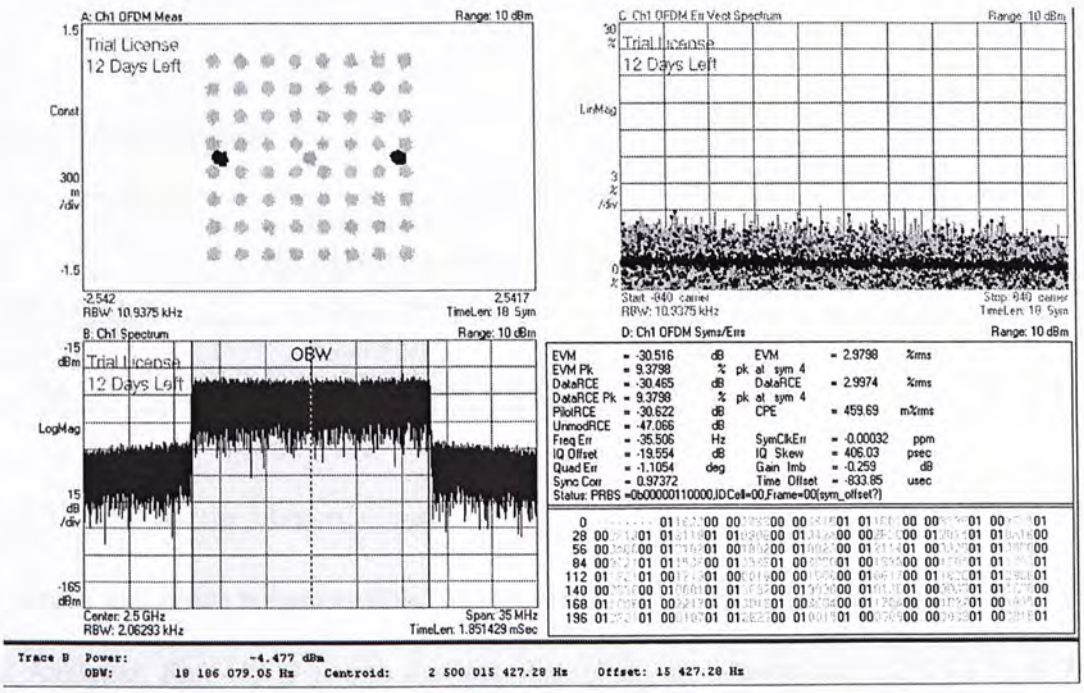

Fig. 4.6-10 WiMAX modulation test with 20-MHz baseband signal

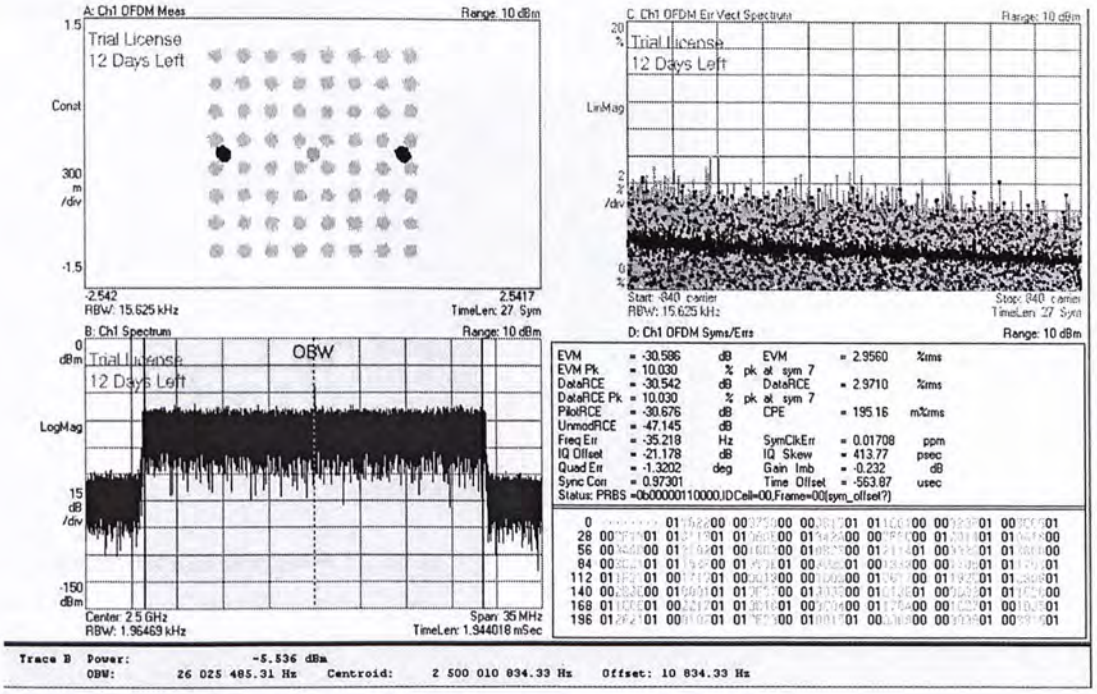

Fig. 4.6-11 WiMAX modulation test with 28-MHz baseband signal

DC current consumption

	Pre-layout simulation result	Post-layout simulation result	Measurement result
I/Q modulator	18.25 mA	18.25 mA	7.59 mA
Driver	42.09 mA	42.09 mA	44 mA
PA	188.5 mA	188.6 mA	217 mA

4.4.2. LC Balun Measurement

The magnitude and phase response of the on-chip *LC* balun is measured by Agilent E5071A RF 4-port Network Analyzer. Fig. 4.6-12 shows the testbench of the measurement. Fig. 4.6-13 and Fig. 4.6-14 shows the magnitude response, $|S_{13}|$ and $|S_{23}|$, and the phase response, $\angle S_{13}$ and $\angle S_{23}$ of the *LC* balun. Fig. 4.6-15 shows the amplitude and phase mismatches of the on-chip balun. The measured phase mismatch is only 2.9°. Moreover, the measured amplitude mismatch is less than 2 dB. It shows that the

on-chip balun has good differential power combining capability and it has less phase mismatch compared with an off-chip balun.

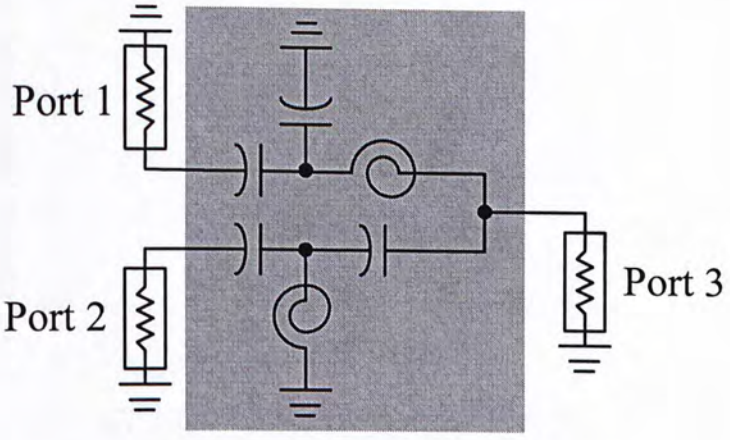

Fig. 4.6-12 S-parameter measurement in LC balun

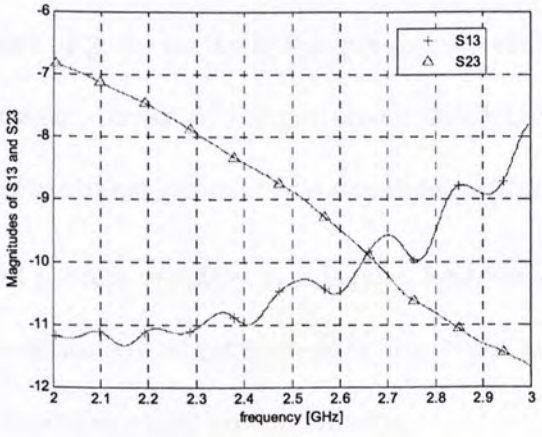

Fig. 4.6-13 Magnitude response of the LC balun

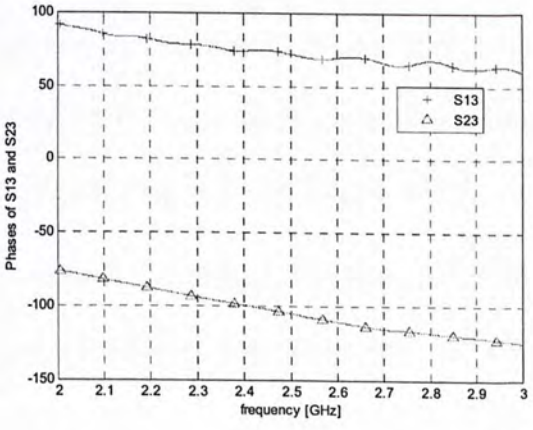

Fig. 4.6-14 Phase response of the LC balun

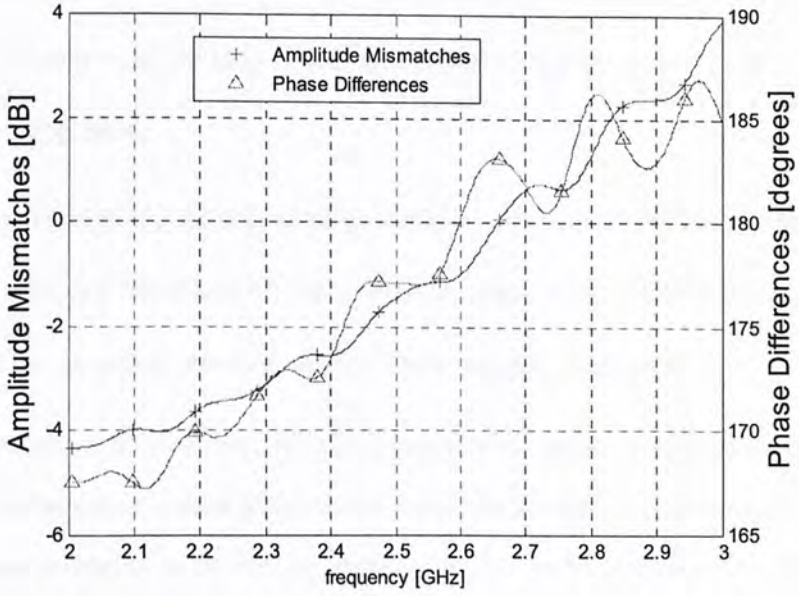

Fig. 4.6-15 Amplitude and phase mismatch of the LC balun

4.7 Performance Summary of the transmitter front-end circuit

Table 4-2 shows both the pre-layout, post-layout simulation result and measurement result. The saturated power of the pre-layout simulation result is larger than that of the post-layout simulation because of the ground resistance at the power stage and voltage drop within the signal wires.

And process variation is existed at both the parasitic resistance model and inductor model. Therefore, the measured output power is less than the post-layout simulation. The bondwires resistance also reduces the output power delivery.

For the linear gain, the measured result is larger than the post-layout simulated result, but smaller that the pre-layout simulation result. As the power gain depends on the transconductance of all the stages, which is also depend on the drain current of all the stages. The post-layout extraction may not model the parasitic resistance accurately.

The values of the efficiency obtained from the pre-layout and post-layout simulation are similar, but its measurement result is not. It may be degraded by the parasitic resistance within the probe station. Also,

the loss within the metal wires is also higher than expected. The parasitic model of the inductor and metal wires may not match with the chip. Furthermore, the power gain is suffered as the quality factor of the inductor is also degraded.

In the mixer power consumption, the measured power consumption is only half of the simulation result. It may also be the process variation of the transistor, especially the current source of the mixer. Therefore the V_{GS} of the g_m cell is reduced and the drain current is reduced.

For the sideband suppression, all the pre-layout, post-layout simulated and measured result are similar. It is shown that the quadrature error at the baseband input is about 3 degrees. For the LO feedthrough, no LO mismatch is introduced in the pre-layout and post-layout simulation, so that the LO feedthrough are too realistic and not close to the measured result.

Table 4-3 summarizes the performance of the transmitter front-end. Table 4-4 is the comparison table. It shows that this work can deliver similar output power level when comparing with the bipolar counterpart in [6]. Moreover, this work has larger OP1dB and the saturated power (P_{SAT}) compared with [2] – [5]. In addition, this work provides the largest band power among the works reported in [2]-[5].

Table 4-2 Simulation and Measurement Result

	Pre-layout	Post-layout	Measurement
P_{sat} [dBm]	23.5	21.65	20.6
P1dB [dBm]	-6.42669	2.01796	-5.22
OP1dB [dBm]	22.0534	21.6013	18
linear gain [dB]	29.48	20.648	24
P_{gain} @ P1dB [dB]	28.46	19.58334	17
PAE @ OP1dB [%]	19.866	17.81	10.6
PAE @ Psat [%]	25.7	17.9	14
mixer_power [mW]	27.4	27.4	11.4
DR_power [mW]	53.4	53.4	55.9
PW_power [mW]	620	622	716
LO feedthrough [dBc]	-72.05	-61.8	-43.04
sideband suppression [dBc]	-35.8	-37.3	-38.98

Table 4-3 Transmitter performance summary

Technology	UMC 1P6M 0.18μm CMOS
Supply Voltage	1.5 V (Mixer) 1.27 V (RF driver) 3.3 V (main amplifier)
Radio Frequency	2.5 GHz
Tx small signal gain	24 dB
OP1dB P_{SAT}	18 dBm 20 dBm
PAE @ OP1dB	10.5 %
LO feedthrough @ P_{SAT}	-43.04 dBc
Sideband Suppression @ P_{SAT}	-38.98 dBc
EVM @ P_{IN} = -11.7-dBm	-30.53 dB @ BW = 10-MHz -30.52 dB @ BW = 20-MHz -30.59 dB @ BW = 28-MHz
Power comsumption	716 mW (Power stage) 55.88 mW (Driver stage) 11.39 mW (I/Q modulator)

Table 4-4 Comparison Table

	Technology	**Band (GHz)**	**Supply (V)**	**OP1dB (dBm)**	**EVM**
This work	**CMOS 0.18** μm	**2.5**	**1.5 1.27 3.3**	18 / 20(P_{SAT})	**-30.52-dB (20MHz) @ 5.52 dBm**
[3]	CMOS 0.13 μm	2.3– 2.7	1.2 ,2.5	9.6	-36.6 dB @ -5dBm, 2.3 GHz
[4]	SiGe BiCMOS 0.25 μm	2.3 –2.7	2.8	2.5	1.5 % @ 2.5 dBm
[5]	CMOS 90 nm	2.5	1.2, 2.9	12	N.A.
[6]	CMOS 0.18 μm	2.3-2.7	1.8, 2.5	N.A.	-38 @ 0 dBm
[7]	SiGe BiCMOS 0.18 μm	5.8	3.2 – 3.6	21 (P_{SAT})	N.A.

4.8 Reference

[1] WiMAX Forum, "WiMAX Technology," available at http://www.wimaxforum.org/resources/documents/technical/release1.5.

[2] WiMAX forum, "WiMAX Forum® Mobile System Profile, Release 1.0 Approved Specification, (Revision 1.7.1: 2008-11-07)".

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[5] D. Yamazaki *et al.*, "2.5-GHz fully-integrated WiMAX transceiver IC for a compact, low-power-consumption RF module," in *Proc. 2008 RFIC Symp.*, Jun. 2008, pp. 109-112.

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[9] Agilent, "WiMAX Concepts and RF Measurements.pdf".

[10] Agilent, "IEEE 802.16e WiMAX OFDMA Signal Measurements and Troubleshooting".

5. Conclusion

In this thesis, a CMOS Class-AB RF power amplifier and a CMOS RF transmitter front-end circuit are designed and fabricated using a 0.18-μm CMOS technology. The power amplifier functions at the 3-GHz frequency band. As the supply voltage is low, the PA is terminated with an optimum output resistance to extract the most amount of power from the supply. The optimum output resistance is found out by parametric Cadence Spectre-RF periodic steady-state simulation. The output matching network is designed to transform the load resistance to optimum output resistance.

In this work, there are some drawbacks in the design. The ground wires are too thin and the parasitic resistance is larger than expected. The signal wires are also not wide enough to reduce the parasitic resistance. The distance between the power transistors should be close to the power ground. The transconductane and the output voltage swing are reduced also. The output power is loss. The RF signal should flow in one direction only.

A transmitted front-end circuit for WiMAX application has been presented. The drawbacks at the previous work are addressed. Both the ground wires and signal tracks are widened, especially the output stage. The power transistors are placed next to the power ground wires. All the signal ports can be probed using the probe station in order to lessen the parasitic components at all the ports. In addition, the offchip balun at the output stages can also be eliminated. The proposed front-end circuit operates in Frequency Band Index 3 of the WiMAX standard. The circuit has been measured under the center frequency of 2.5 GHz and the results have been reported. The output signal is single-ended by using the on-chip *LC* balun with low LO feedthrough and good sideband suppression. This work delivers the highest output power among other reported CMOS transmitters or transceivers. Finally, this work does also provide similar output power level as the counterpart implemented in BiCMOS technology.

6. Future Work

In this thesis, all the on-chip inductors are provided by the foundary design kit. Although those inductors have accurate model, it is not desired to be used in the power amplifier design. It is because their Q-factor is quite low and the metal width of the inductors cannot withstand high current densities. As a result, inductors should be tailor-designed in the future.

The output power is still not high enough compared with other state-of-the-art PAs. The output power can be improved by using the different power combining technique. There are many techniques, for example, transformer coupling. The output power is provided by 2 or more power amplifier cells.

In the transmitter side, the gain can also be designed to be programmable. In the new wireless communication standard, the gain step is strictly controlled. Therefore, the power gain of the driver stage can be adjusted to fulfill the requirement. The gain can be controlled by changing the drain current flow though the driver. It can change the transconductance of the driver stage.