A Quaternary Current Mode Bus Driver and Receiver Circuits

CHEUNG, Cheuk Kit

A Thesis Submitted in Partial Fulfillment
of the Requirements for the Degree of
Master of Philosophy
in
Electronic Engineering

The Chinese University of Hong Kong

August 2009

Abstract

Abstract of thesis entitled:

A Quaternary Current Mode Bus Driver and Receiver Circuits

Submitted by **CHEUNG Cheuk Kit**

for the degree of **Master of Philosophy** in **Electronic Engineering**

at **The Chinese University of Hong Kong** in June 2009

This thesis presents a new current-mode low-swing interconnect driver and receiver circuits which consist of a gated cascode current mirror as a transmitter and a custom design sense-amplifier as a receiver. The new sense-amplifier uses gated transistors to isolate the cross-coupled inverter from the differential pair to reduce the parasitic capacitance at the drain terminals of the input differential pair. As a result of this improvement, the new sense-amplifier has smaller kick-back noise, power consumption and delay than conventional designs.

We have designed and fabricated two test systems to verify the new design, one is the new quaternary current mode driver and receiver circuits and the other one is a conventional inverter chain driver and receiver circuits. Both test systems drive a 500 μm long and 1 μm wide metal wire. The measurement results indicate that the new design operates faster and has smaller power consumption and area at high speed. However, the

new design loses the power consumption advantage at low speed operation because of the added circuit complexity of the new design.

摘要

本論文展示了一種新型的電流模數位信號互連。此新型的信號互連有別於傳統的二位元，可在一條連接電路中進行四位元的信號傳輸。這信號互連由一個閘控堆疊電流鏡作為傳送器，而接收端則由等效二極管電晶體與感測放大器所組成。

為了減低由感測放大器耦合至互連電路上的突波回授雜訊，我們捨棄了傳統的感測放大器，並以之為參考，在差動對電晶體之上加上一對電晶體以收阻隔電壓急速改變之效。此改動能有效減低感測放大器的突波回授雜訊、信號延遲與功耗。

我們分別設計了兩種信號互連，一是上述的電流模信號互連，另一個是傳統的鏈狀電型模信號互連。它們均連接著長 500 微米，闊 1 微米的連接電路。從仿真及而實驗數據得知，本論文所展示的電流模信號互連於高數據率的情況下比傳統的電壓模信號互連更省電。但在低數據連中會失掉此優勢。

Acknowledgements

I would like to take this opportunity to express my gratitude to my supervisor, Professor Chan Cheong Fat, for his patient guidance and fruitful discussions in these two years. I have gained much invaluable opinions on my research through the discussions.

Then I would like to thank for Mr. Yeung – laboratory technician. He helped me solve the problem in CAD tools and measurement equipments. Finally, I would like to thank for my colleagues who has worked with me within this two years

Table of Contents

Abstract 1

摘要 2

Acknowledgements 3

Table of Contents 4

List of Figures 9

1. Introduction 12

1.1. Research Motivation 12

1.1.1. Global and Intermediate Interconnects 12

1.1.2. Constraints of Repeater Insertion Techniques 13

1.2. Research Objective 13

1.3. Reference 14

2. Voltage Mode and Current Mode Circuits 16

2.1. Introduction 16

2.2. Voltage Mode Circuit 16

2.3. Current Mode Circuit 18

2.4. Power Consumption 19

2.5. Latency 20

2.6. Summary 20

3. Transmitter Design 22

3.1. Introduction 22

3.2. Multi-level Signaling 22

3.3. Gated Current Mirror 23

3.4. Power Consumption 24

3.5. Summary 24

3.6. Reference 25

4. Receiver Design 26

4.1. Introduction 26

4.2. Conventional Latched-typed Sense Amplifier 27

4.3. Sense Amplifier with Isolated Differential Pair 29

4.4. Power Consumption, Latency and Kick-back Noise Comparison between Different Designs 30

4.4.1. Comparison on Power Consumption 30

4.4.2. Comparison on Latency 31

4.4.3. Comparison on Kick-back Noise 33

4.5. Summary 34

4.6. Reference 34

5. Inverter Chain 36

5.1. Introduction 36

5.2. Inverter Chain Based 36

5.3. Summary 38

5.4. References 38

6. Layout Techniques 39

6.1. Introduction 39

6.2. Two-Dimensional Common Centroid Layout Technique 39

6.3. Dummy Devices 40

6.4. Summary 42

6.5. References 42

7. Simulation Results 43

7.1. Introduction 43

7.2. Simulation of Different Aspect Ratios of Differential Pair 43

7.3. System Level Simulation with Different Sense-amplifiers 46

7.4. System Level Simulation at Different Data Rate 47

7.5. Summary 49

8. Measurement Results 50

8.1. Introduction 50

8.2. Experimental Setup 50

8.2.1. Testing Chips 50

8.2.2. Equipments Setup 52

8.3. Measurement Results 53

8.4. Summary 56

9. Conclusion 57

9.1. Author's Contributions 57

9.2. Future Works 58

10. Appendix 59

List of Figures

Fig. 2.1 Models of voltage mode transmitter 16

Fig. 2.2 Models of current mode transmitter 18

Fig. 3.1 Schematic of gated current mirror transmitter with self-cascode architecture 23

Fig. 3.2 Illustration of the input and output of the quaternary current more transmitter .. 24

Fig. 4.1 Receiver circuit 26

Fig. 4.2 Conventional sense amplifier 28

Fig. 4.3 Kick-back noise from conventional sense amplifier 28

Fig. 4.4 Sense amplifier with isolated differential pair 29

Fig. 4.5 Comparison of conventional sense amplifier and the one with isolated differential pair 30

Fig. 5.1 Inverter chain based interconnect 36

Fig. 6.1 Illustration of two-dimensional common centroid layout 40

Fig. 6.2 Schematic of a differential pair with dummy devices 41

Fig. 6.3 Example of two-dimensional common centroid layout 42

Fig. 7.1 Power consumption simulation of different aspect ratios 44

Fig. 7.2 Latency simulation of different aspect ratios 45

Fig. 7.3 Kick-back noise level simulation of different aspect ratio 46

Fig. 7.4 Power consumption simulation result of system with different sense amplifier under different data rate 47

Fig. 7.5 Power consumption simulation result of two interconnect system under different data rate 48

Fig. 8.1 Interconnect using conventional sense amplifier as comparator 51

Fig. 8.2 Interconnect using sense amplifier with isolated differential pair as comparator 51

Fig. 8.3 Interconnect using inverter chain 52

Fig. 8.4 Block diagram of measurement setup 52

Fig. 8.5 Power consumption measurement of quaternary current mode interconnect..... 53

Fig. 8.6 Measurement result of relationship between power consumption and data rate. 55

Fig. 10.1 Complete schematic of the current mode transmitter 59

Fig. 10.2 Complete schematic of the conventional sense amplifier (A) and sense amplifier with isolated differential pair (B) 59

Fig. 10.3 Transient Waveform of the Clock Signal 60

Fig. 10.4 Transient Waveforms of the Drain of Differential Pairs 60

Fig. 10.5 Transient Waveforms of the Drain of Clock Transistors 61

Fig. 10.6 Transient Waveform of the Outputs 61

Fig. 10.7 Transient Waveform of Kickback Noise of the Conventional Sense Amplifier 62

Fig. 10.8 Transient Waveform of Kickback Noise of the New Sense Amplifier 62

Fig. 10.9 Complete schematic of the proposed current mode interconnect..... 63

Fig. 10.10 Complete schematic of the inverter chain based reference interconnect..... 63

1. Introduction

1.1. Research Motivation

1.1.1. Global and Intermediate Interconnects

As advance in technology, the feature size of transistor is shrinking. However, wire interconnects do not scale as the same rate of transistor because of current density, metal migration and propagation delay [1, 2]. Specially, long global routing wires are becoming a speed bottle neck for advanced submicron technologies.

As early as 1977, ACM Turing Award winner John Backus has predicated this phenomenon called Von Neumann bottleneck, which indicates that the major limitation of performance is the transmission speed of the buses between processor and memory. The processor must wait until the data to be transferred. Caches memory has been used to relief this bottleneck; however, from 1986, the improvement in memory access time has lagged significantly compared to the advancement of the operating speed of processor. This phenomenon is known as Memory Wall, which is a major limitation to the overall system performance and can be more significant in multi-core and SOC design [3].

1.1.2. **Constraints of Repeater Insertion Techniques**

In the lumped model of a wire, the $R_{wire}C_{wire}$ time delay increases 4 times if the wire length doubles. Since the increase of delay and power consumption with respect to the wire length is quadratic, typically designers insert repeaters in between the interconnects to improve the latency and power consumption. There have been different repeater insertion optimization schemes, which focus on different aspects of the design parameters such as delay, power and area optimization.

However, using the repeater technique to drive long interconnects requires very large driver transistor size, transistor sizes range from 40x to 200x of the minimum inverter size are reported [4]. These large drives consume large area and power. Moreover, placing these large drivers is becoming a difficult design issue especially in large design, because designers usually cannot place the repeaters at the optimal locations due to other design constrains. Therefore, special floor-planning software is usually required to place and route the repeaters [3].

1.2. Research Objective

The objective of this research is to develop an on-chip or off-chip transmission system which can improve the power efficiency in long wire transmission.

The remaining part of this thesis is organized as follows. Chapter 2 discusses the differences between voltage mode circuit and current mode circuit. The design of the new transmitter is explained in chapter 3. Chapter 4 shows the design and working principle of the receiver. Chapter 5 analyzes the behavior of inverter chain based interconnect. The layout consideration is discussed in chapter 6. The simulation and measurement results are reported in chapter 7 and 8, respectively. Finally, chapter 9 is the conclusion.

1.3. Reference

[1] Sylvester, D. and Keutzer, K., "A global wiring paradigm for deep submicron design," IEEE Trans. Computer-Aided Design Integr. Circuits Syst., vol. 19, no. 2, pp. 242–252, Feb. 2000.

[2] Ho, R. Mai, K.W. and Horowitz, M.A., "The future of wires," Proc. IEEE, vol. 89, no. 4, pp. 490–504, Apr. 2001.

[3] P.G. Emma and E. Kursun, "Is 3D chip technology the next growth engine for performance improvement?," IBM Journal of Research and Development, vol. 52, no. 6, Nov. 2008.

[4] Song Chen, "Floorplanning with Consideration of White Space Resource Distribution for Repeater Planning," Sixth International Symposium on Quality of Electronic Design, pp. 628-633, Mar. 2005.

2. Voltage Mode and Current Mode Circuits

2.1. Introduction

This chapter discusses the differences between voltage mode and current mode circuits. First of all, their characteristics will be introduced. Then the power consumption and latency will be compared.

2.2. Voltage Mode Circuit

A typical voltage mode transmitter is shown in Fig. 2.1, where r_n and r_p model the on-resistance of the channel of the NMOS and PMOS transistors respectively, r_{int} is the interconnect resistance, C_{int} is the interconnect capacitance and C_{LOAD} is the load capacitance at the receiver side. In this work, we are using a "L" model to model the wire.

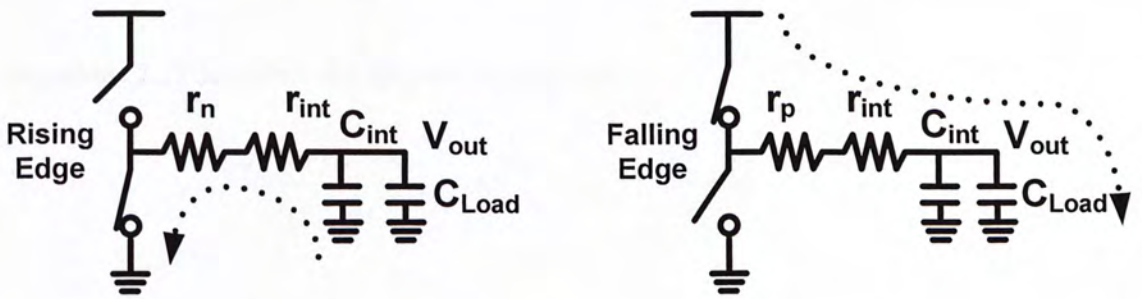

Fig. 2.1 Models of voltage mode transmitter

To minimize the loading effect in voltage mode circuit, the input impedance should be large (C_{Load}, which refers to the gate capacitors of the receiver side inverter) and the output impedance (r_n and r_p) should be small.

The information carrier of voltage mode signaling is the nodal voltage. The transmitter (inverter) works as a switch to connect the load C_{Int} and C_{Load} to V_{dd} or V_{ss} so that the power supply can charge up the capacitors or the ground can discharge the capacitors.

Equation (2.1) and (2.2) show the transient response corresponding to a rising edge input and a falling edge input, respectively and the voltage swing of V_{out} is from V_{dd} to V_{ss}.

Equation (2.1) describes the output discharging state.

$$\frac{V_{out}(t)}{r_n + r_{int}} = -(C_{int} + C_{Load})\frac{dV_{out}(t)}{dt} \tag{2.1}$$

Equation (2.2) describes the output charging state.

$$\frac{V_{out}(t) - Vdd}{r_p + r_{int}} = -(C_{int} + C_{Load})\frac{dV_{out}(t)}{dt} \tag{2.2}$$

2.3. Current Mode Circuit

Fig. 2.2 shows one of the models of a current mode transmitter, where r_o represents the channel resistance of the switching transistor, I_{bias} and I_o are two current sources, which are equivalent to V_{dd} and V_{ss} in voltage mode design.

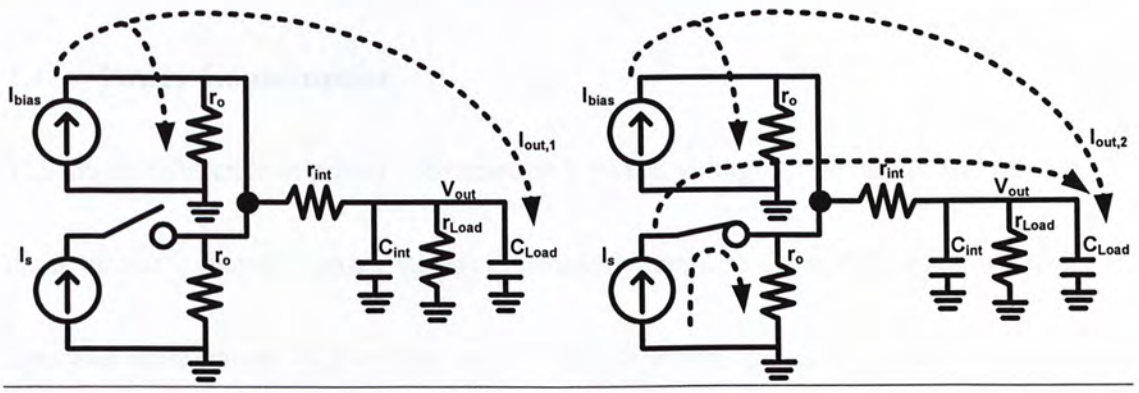

Fig. 2.2 Models of current mode transmitter

The information carrier of current mode signaling is the branch current, the output DC current is determined by equations (2.3) and (2.4).

$$I_{out,1} = \frac{r_o}{r_o + (r_{int} + r_{Load})} I_{bias} \tag{2.3}$$

$$I_{out,2} = \frac{r_o}{r_o + (r_{int} + r_{Load})} (I_{bias} + I_s) \tag{2.4}$$

The output DC voltage is given by equations (2.5) and (2.6).

$$V_{out,1} = r_{Load} \left[\frac{r_o}{r_o + (r_{int} + r_{Load})} I_{bias} \right] \tag{2.5}$$

$$V_{out,2} = r_{Load} \left[\frac{r_o}{r_o + (r_{int} + r_{Load})} (I_{bias} + I_s) \right] \tag{2.6}$$

The voltage swing is given by equation (2.7), it can be kept low.

$$\Delta V_{out} = V_{out,2} - V_{out,1} \tag{2.7}$$

The transient response of a current mode circuit is given by equation (2.8).

$$I_{out} = \frac{V_{out}(t)}{r_{Load}} + (C_{int} + C_{Load})\frac{d\,V_{out}(t)}{dt} \tag{2.8}$$

2.4. Power Consumption

The major difference in power consumption between voltage mode circuit and current mode circuit is that the former mainly consume dynamic power and the latter mainly consume static power. In a voltage mode circuit as shown in Fig. 2.1, power is required to charge up the interconnect capacitor and load capacitor to V_{dd} so the power consumption can be estimated as:

$$P \approx (C_{int} + C_{Load})V_{dd}{}^2 f \tag{2.9}$$

This well-known equation reveals that the power consumption of a voltage mode circuit is proportional to the operating frequency.

However, the major power consumption of a current mode circuit is static power, which is independent of the operating frequency so the power consumption is equal to:

$$P \approx I_{avg}V_{dd} \tag{2.10}$$

2.5. Latency

The latency can be simplified as the time needs to charge or discharge a capacitor to certain voltage level. It is determined by equation (2.10),

$$\Delta t = \frac{C\,\Delta V}{I_{avg}} \tag{2.10}$$

where ΔV is the voltage swing of the output node and I_{avg} is the average current charging or discharging the node. In voltage mode circuit like an inverter, the voltage swing is determined by the power supply rail. Comparing to a voltage mode circuit, the voltage swing of a current mode circuit is flexible. As shown in equation (2.5) – (2.7), the voltage swing of a current mode circuit can be kept very low, while the current swing can be kept at a large level. This can be accomplished by reducing the loading impedance. The small voltage swing of a current mode circuit reduces the charging and discharging time.

2.6. Summary

This chapter analyzes the difference between voltage mode circuit and current mode circuit. We have compared the transient response, power consumption and latency of these two different designs. The dynamic power consumption of a voltage mode circuit is controlled by frequency, loading and supply voltage which a designer has very little control. However, the static power consumption of a current mode circuit is a function of

the branch current, which a designer can changed to optimize the performance of the design.

3. Transmitter Design

3.1. Introduction

A multi-level current-mode transmitter is designed to replace a conventional inverter driver. This transmitter can convert two binary bit voltage inputs into 4 different level output currents. The new quaternary current mode transmitter reduces the number of wires by half, which will have a significant impact on area and power consumption on designs with a large bus.

3.2. Multi-level Signaling

In conventional binary signaling, 2 voltage levels, usually V_{ss} and V_{dd}, are used to represent 0 and 1. One way of increasing the data rate without increasing the channel bandwidth is to use coding.

The symbol rate in binary signal is equal to the data rate; however, it is possible to map 2 data bits into one symbol to achieve 4-level signaling. Consequently, the symbol rate is less than the data rate, thus, we have doubled the data rate at the same channel bandwidth

.

3.3. Gated Current Mirror

The driver is a gated current mirror as shown in Fig. 3.1. The driver consists of three current mirrors connected in parallel, which generates two separate I_{ref} currents and a 2X I_{ref} current. It sources static bias current I_{ref} through M2 and M3 to keep the diode-connected transistor at receiver side active. When bit0 (bit1) is low, V_{g1} (V_{g2}) is driven to V_{bias}, M4 (M6) and M5 (M7) source I_{ref} (2 I_{ref}). While bit0 (bit1) goes high, V_{g1} (V_{g2}) is connected to V_{dd}, no current flows through M4 (M6) and M5 (M7) [1]. The output current steps of I_{out} are I_{ref}, 2 I_{ref}, 3 I_{ref} and 4 I_{ref} as shown in Fig. 3.2. The complete schematic diagram of the transmitter is shown in Fig. 10.1 in Appendix.

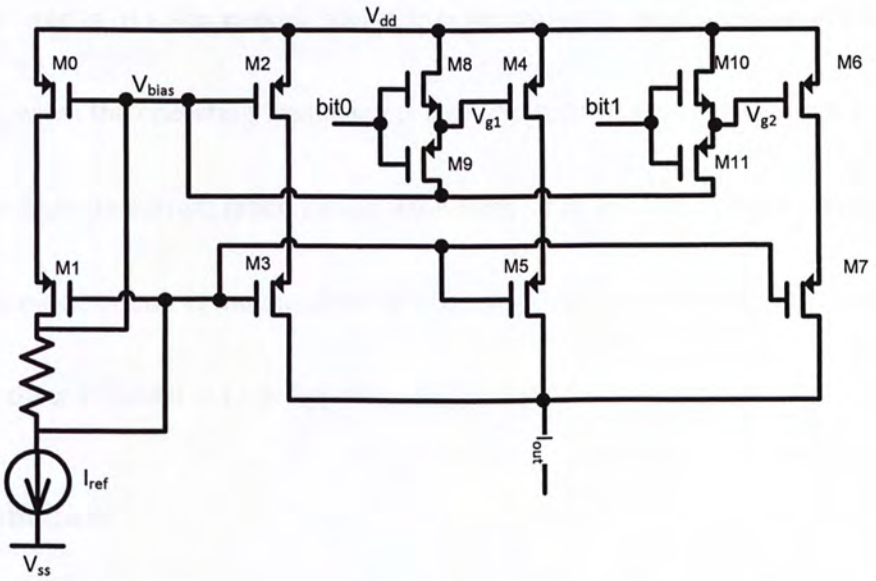

Fig. 3.1 Schematic of gated current mirror transmitter with self-cascode architecture

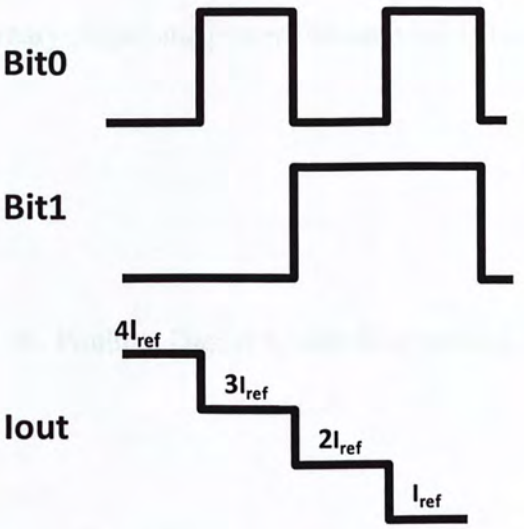

Fig. 3.2 Illustration of the input and output of the quaternary current more transmitter

3.4. Power Consumption

The major power consumption of this current mode transmitter is static power rather than dynamic power as in voltage mode transmitter according to the discussion in chapter 2. Therefore, when the operating frequency is low, the voltage mode transmitter consumes less power than the current mode circuit. However, since the static power consumption of the current mode circuit is independent of frequency, thus, the current mode transmitter becomes power efficient at high operating frequency [2].

3.5. Summary

This chapter has presented the schematic design and operation principle of the proposed gated current mirror, which will be used as a transmitter. The major advantages of the

new design are the quaternary output and power consumption is independent of frequency [2].

3.6. Reference

[1] W. J. Dally and J. W. Poulton, Digital System Engineering. Cambridge University Press, 1998.

[2] Akira Tanabe, "0.18-μm CMOS 10-Gb/s multiplexer/demultiplexer ICs using currentmode logic with tolerance to threshold voltage fluctuation", IEEE J. Solid-State Circuits, vol. 36, issue 6, pp. 988 – 996, Jun. 2001.

4. Receiver Design

4.1. Introduction

This chapter proposes a new current mode receiver design as shown in Fig. 4.1. This receiver is composed by 4 diode-connected NMOS transistors as current-to-voltage converters and three sense amplifiers (comparators). The sense amplifiers are responsible for distinguishing the 4 different current levels and convert the quaternary current signal back into voltage signal. This chapter will explain the operation principles of the sense amplifier and compare the differences between a conventional design and the design of this work which uses an isolated differential pair.

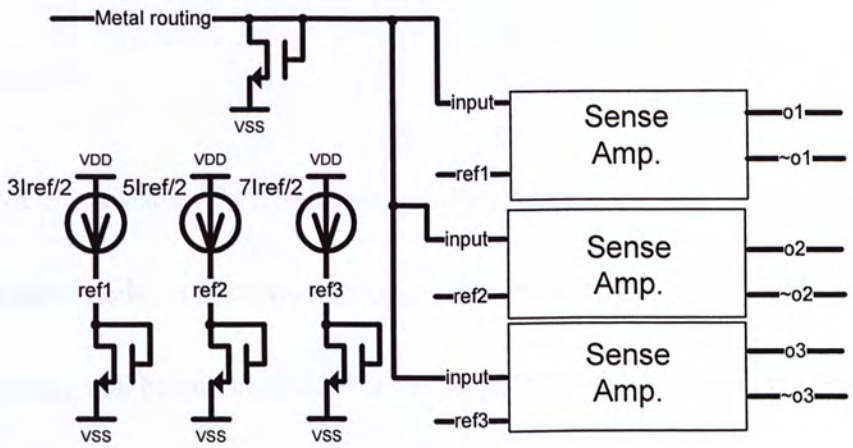

Fig. 4.1 Receiver circuit

4.2. Conventional Latched-typed Sense Amplifier

Besides memory applications and logic designs [1], [2], sense amplifiers are also widely used in Flash ADC designs [3]. Fig. 4.2 illustrates the operation principle of a sense amplifier. This type of sense amplifier has two phases. In the RESET phase, differential outputs are reset to V_{dd}. In the SET phase, differential output is evaluated.

When the clock is LOW the comparator is off, and the differential outputs are charged to V_{dd} by M7 and M8. This is the RESET phase of the sense amplifier. The SET phase occurs when the clock is HIGH. As both outputs are charged to V_{dd}, both M3 and M4 are on. The two input transistors (M5, M6) act as two voltage control current sources, which start to discharge the two output nodes. The difference between INPUT and Ref voltages causes different discharging currents. Thus, one of the outputs will discharge at a higher rate than the other.

The two PMOS transistors (M1, M2) are initially off because of the HIGH outputs. When one of the output nodes is discharged to V_{dd}-V_{thp} so that $V_{gsp}>V_{thp}$, the corresponding PMOS transistor will be switched on. For example, if INPUT is larger than Ref, OUTPUT will reach V_{dd}-V_{thp} before ~OUTPUT, which causes M2 to switch on. The

positive feedback across couple inverters latches the outputs [1,2]. In the example above, OUTPUT is LOW and ~OUTPUT is HIGH.

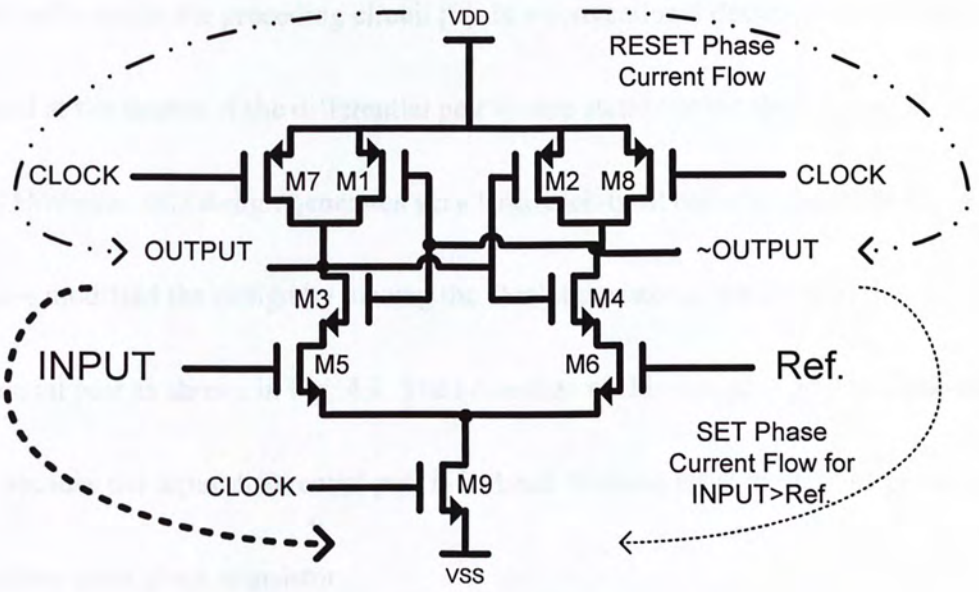

Fig. 4.2 Conventional sense amplifier

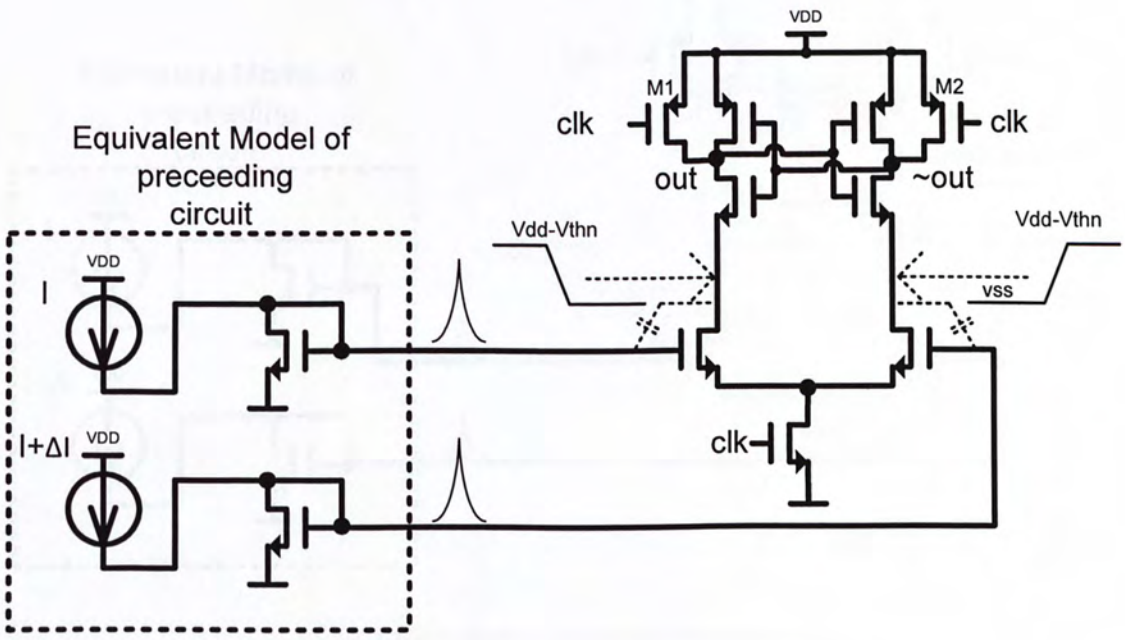

Fig. 4.3 Kick-back noise from conventional sense amplifier

4.3. Sense Amplifier with Isolated Differential Pair

Fig. 4.3 illustrates how the kick-back noise is generated in a conventional sense amplifier [4] and reflected to the preceding circuit [5]. In a conventional design, a clock transistor is placed at the source of the differential pair to stop static current flow during the RESET phase. However, this design generates very large kick-back noise as shown in Fig. 4.3. We have modified the design by placing the clock transistor at the drain of the differential pair as shown in Fig. 4.4. The advantage of this design is smaller kick-back noise because the input differential pair is isolated from the large drain voltage swing at a cost of one extra clock transistor.

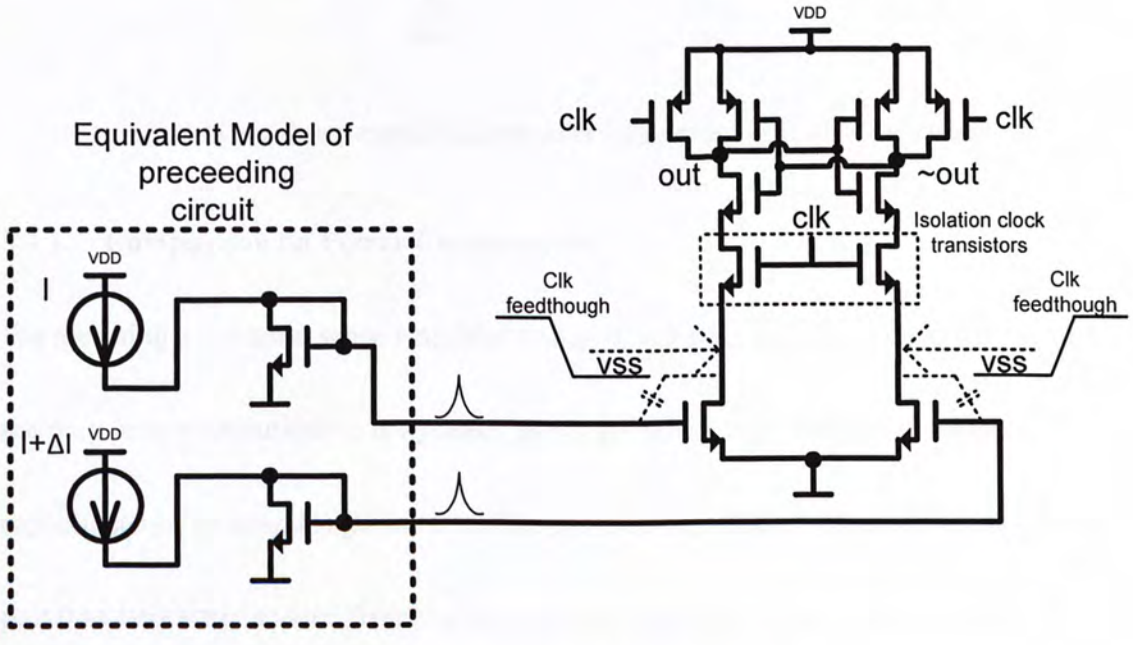

Fig. 4.4 Sense amplifier with isolated differential pair

4.4. Power Consumption, Latency and Kick-back Noise Comparison between Different Designs

Fig. 4.5 illustrates the parasitic capacitors of a conventional sense amplifier and the new design with isolated differential pair. Only half of the circuit is shown in Fig. 4.5 for simplicity because the other half is an exact mirror image of the other half.

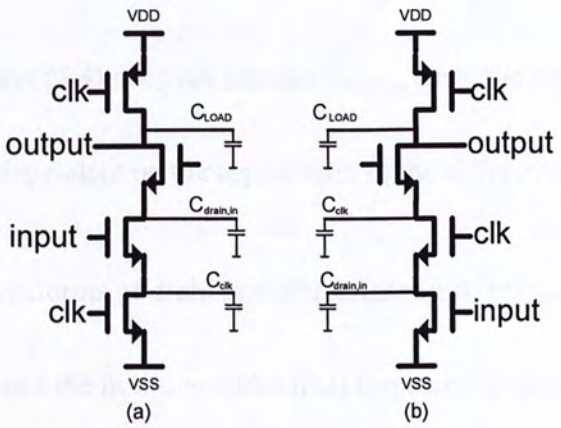

Fig. 4.5 Comparison of conventional sense amplifier and the one with isolated differential pair

4.4.1. Comparison on Power Consumption

We are using a dynamic sense amplifier design which does not consume any static power, the only power consumption is dynamic power [6] which is a function of parasitic capacitance. The new design has a smaller parasitic capacitance because the differential pair transistors are isolated from the cross-coupled inverter by the clock transistor. As illustrated in Fig. 4.5, the isolation clock transistor shields the parasitic capacitors $C_{drain,in}$

of the differential pair from being charged up during the RESET phase. The total capacitance of a conventional design in RESET phase is shown in equation 4.3, and the total capacitance of the new design is shown in equation 4.4. The new design has less capacitance than a conventional design.

$$C_{total} = 2(C_{Load} + C_{drain,in}) + C_{clk} \quad (4.3)$$

$$C_{total} = 2(C_{Load} + C_{clk}) \quad (4.4)$$

Moreover, since equation (4.4) does not contain $C_{drain,in}$ term, the power consumption of the new design is less dependent on the aspect ratio of the differential pair.

Fig. 10.4 shows the waveforms of drain of differential pair of the conventional sense amplifier (dotted line) and the new one (solid line) respectively. From this figure, it is showed that the voltage variation at the drain is isolated in the new design. On the other hand, from Fig. 10.5, the voltage variation at the drain of the isolation clock transistor is significantly larger than that of the conventional design. It can be concluded that the small-sized isolation clock transistor isolates the large voltage variation so that the power consumption required to pre-charge the circuit is significantly reduced.

4.4.2. **Comparison on Latency**

When the sense amplifier is at SET phase, the sensing delay is determined by the current difference between the left and the right half of the differential pair. Since the transistors

of the differential pair are operating in the saturation region during the SET phase and longer channel transistors are used to reduce short channel effect. Therefore, we can model the drain current with a simple square law as shown in equation 4.5

$$I = \frac{1}{2}\mu_n C_{ox}\frac{W}{L}(V_{gs} - V_{thn})^2 \tag{4.5}$$

From equation (4.5), we can reduce the latency by using larger differential pair. However, large differential pair will increase the parasitic capacitance, which will compensate the effect. We have solved this design paradox problem by placing the clock transistors between the cross-coupled inverter and the drains of the differential pair. As stated earlier, the clock transistors shield the parasitic capacitance of the differential pair during the RESET phase. Therefore, increasing the size of the differential pair will increase the drain current and reduce the latency. We can further demonstrate this point by calculating the total charges store at these two circuits at the end of RESET phase. The total charge accumulated in the conventional sense amplifier illustrated in Fig. 4.5a is shown in equation 4.6

$$q_{total} = 2C_{Load}V_{dd} + 2C_{drain,in}(V_{dd} - V_{thn}) + C_{clk}V_{clk} \tag{4.6}$$

, where V_{clk} is the voltage at the drain of the clock transistor C_{clk} .

The total charges stored in the sense amplifier with isolated differential pair shown in Fig. 4.5b is shown in equation 4.7, which is smaller than the conventional design and independent of the size of the differential pair.

$$q_{total} = 2C_{Load}V_{dd} + 2C_{clk}(V_{dd} - V_{thn}) \quad (4.7)$$

Fig. 10.6 verifies the above analysis that the latency of the new sense amplifier (solid line) is shorter than that of the conventional one (dotted line).

4.4.3. **Comparison on Kick-back Noise**

Fig. 4.3 illustrates the origin of the kick-back noise in a conventional sense amplifier. In the RESET phase, two reset switch transistors M1 and M2 precharge the two outputs to V_{dd} and the drain of the two input transistors to $V_{dd} - V_{thn}$. In the SET phase, one of outputs discharges to V_{ss}. The large voltage swing at the output node will be coupled back to the input though the parasitic capacitor. This disturbance will reduce the accuracy of sense amplifier.

The new design isolates the load and driver of the differential pair. There is no large voltage swing at the drains of the differential pair so that the kick-back noise is reduced. The only kick-back noise is the clock feed-through appeared at the drain terminals, which

couples to the input as shown in Fig. 4.4. The clock feed-through signal is voltage divided by the parasitic capacitors and is much smaller than V_{dd}.

The kickback noise transient waveform of the conventional sense amplifier is shown in Fig. 10.7 and that of the new design is shown in Fig. 10.8. They verify that the kickback noise generated from the new sense amplifier is much less than that generated from the conventional design.

4.5. Summary

This chapter introduces the design and the operation principles of the receiver and the sense amplifiers. We have also analyzed the performance difference between a conventional sense amplifier and the new design with isolated differential pair. The isolation clock transistors act as shields for the differential pair, which prevents the differential pair from charging at the RESET phase to reduce kick-back noise. The new design also solved the paradox problem between driver size, parasitic capacitance and speed of the sense amplifier.

4.6. Reference

[1] Chun-Lung Hsu, and Mean-Horn Ho, "High-speed sense amplifier for SRAM applications," IEEE Asia-Pacific Conference, vol. 1, pp. 577–580, Dec. 2004.

[2] Do Anh-Tuan, Kong Zhi-Hui, and Yeo Kiat-Seng, "Hybrid-Mode SRAM Sense Amplifiers: New Approach on Transistor Sizing," IEEE Trans. Circuits Syst. II, Exp. Briefs, vol. 55, no. 10, pp. 986–990, Oct. 2008.

[3] Behzad Razavi, Principle of Data Conversion System Design. IEEE Press, 1995.

[4] T. kobayashi, K. Nogami, and T. Shirotori, Y. Fujimoto, "A current-controlled latch sense amplifier and a static power-saving input buffer for low-power architecture," IEEE J. Solid-State Circuits, vol. 28, pp. 523–527, May 1993.

[5] Figueiredo, P.M. and Vital, J.C., "Kickback noise reduction techniques for CMOS latched comparators," IEEE Trans. Circuits Syst. II, Exp. Briefs, vol. 53, no. 7, pp. 541–545, Jul. 2006.

[6] B. Wincht, Current Sense Amplifier for Embedded SRAM in High-Performance System-on-a-Chip Designs. Springer, 2003.

5. Inverter Chain

5.1. Introduction

In order to compare the performance of the new design, we have built a commonly used bus driver circuits as a reference. We will discuss the pros and cons of the inverter chain circuits in the following sections. In this chapter, lumped approximation of distributed RC wire proposed by [1] is used to model an interconnect.

5.2. Inverter Chain Based

A reference circuit which is based on cascading inverter chain is shown in Fig. 5.1. In this design, the interconnect is modeled by distributed model, where n is the number of stage and k is the scaling factor. The principle of inverter chain based interconnect driver is that the size of inverter gradually increases with the same scaling factor until the last inverter is capable of driving the long wire load at certain rise and fall time.

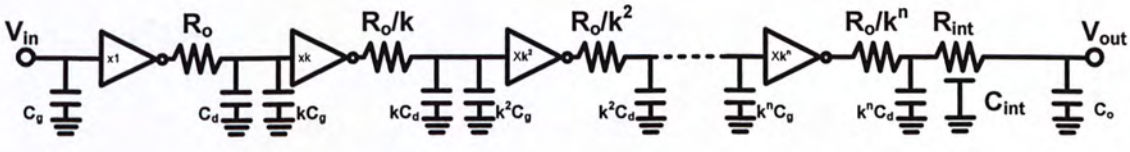

Fig. 5.1 Inverter chain based interconnect

From [1] and [2], the propagation delay of a wire driven by an inverter can be approximately calculated as:

$$\tau_o = 0.4R_{int}C_{int} + 0.7(R_oC_{int} + R_oC_L + R_{int}C_L) \tag{5.1}$$

where R_{int} and C_{int} are the resistance and capacitance of whole length of interconnect. R_o and C_L are the output resistance an inverter and loading capacitance respectively.

From equation (5.1), the total delay can be written as:

$$\begin{aligned}\tau_{total} = {} & \left[0.7R_o(C_d + kC_g) + 0.7\frac{R_o}{k}(kC_d + k^2C_g) + 0.7\frac{R_o}{k^2}(k^2C_d + k^3C_g) + \cdots \right. \\ & \left. + 0.7\frac{R_o}{k^{n-1}}(k^{n-1}C_d + k^nC_g)\right] \\ & + \left\{0.4R_{int}C_{int} \right. \\ & \left. + 0.7\left[\frac{R_o}{k^n}C_{int} + \frac{R_o}{k^n}(k^nC_d + C_o) + R_{int}(k^nC_d + C_o)\right]\right\}\end{aligned} \tag{5.2}$$

Since the loading capacitance C_o is usually approximately equal to C_g, and is much less than k^nC_d, it can be ignored. And hence, equation (6.4) can be simplified to:

$$\begin{aligned}\tau_{total} = {} & [0.7(n-1)R_o(C_d + kC_g)] \\ & + \left\{0.4R_{int}C_{int} + 0.7\left[\frac{R_o}{k^n}C_{int} + \frac{R_o}{k^n}(k^nC_d) + R_{int}(k^nC_d)\right]\right\}\end{aligned} \tag{5.3}$$

The optimum scaling factor for standard CMOS technologies is between 3 – 4.

5.3. Summary

Inverter chain based interconnect method is introduced. From equations (5.2) and (5.3), it is found that the inverter chain based technique does not reduce the time constant. Therefore, both latency and power consumption increase quadratically with the length of the wire. We will use the inverter chain driver circuit as a reference circuit to gage the performance of the new design, because it is much easier to emulate a long bus driver and receiver system with this technique.

5.4. References

[1] Sakurai, T., "Approximation of wiring delay in MOSFET LSI," IEEE J. Solid-State Circuits, vol. 18, issue. 4, pp. 418–426, Aug. 1983.

[2] H.B. Bakoglu, Circuits, Interconnections and Packaging for VLSI. Addison Wesley, 1990.

6. Layout Techniques

6.1. Introduction

Layout is a critical step in the design because it will affect the performance of the circuit. We use many modified sense amplifiers in this design, proper matching of the left and right half of the differential amplifier is required to reduce the offset error.

6.2. Two-Dimensional Common Centroid Layout Technique

In order to reduce the effect of thermal and process linear gradients to the critical circuit such as differential pair, common centroid layout technique is widely applied.

There are four rules of common centroid layout [1]:

1. Coincidence

   The centroids of the matched devices should coincide at least approximately.

2. Symmetry

   The array should be symmetric around both X- and Y-axes.

3. Dispersion

   The segments of each device should be distributed throughout the array uniformly.

4. Compactness

   The array should be as compact as possible.

In the case of a differential pair shown in Fig. 6.1, the two transistors A and B need to be matched very well. Each transistor is divided into two halves and they are placed diagonally across a central point.

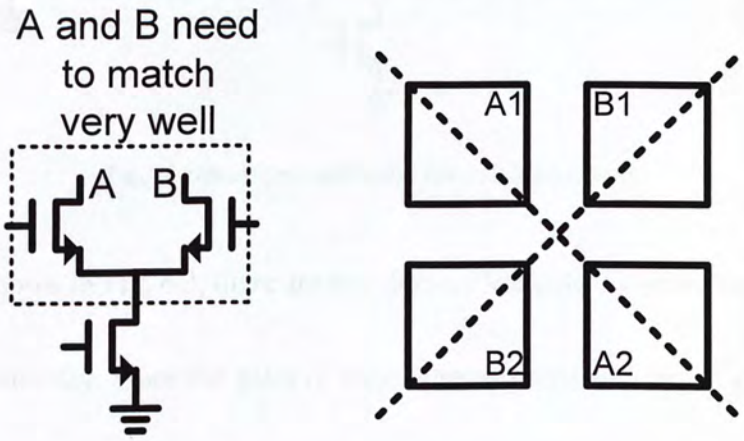

Fig. 6.1 Illustration of two-dimensional common centroid layout

Fig. 6.3 shows the layout of Fig. 6.1. The source terminals of transistor A and B are connected together, which are routed through the centre of the layout. In order to reduce the overlap parasitic capacitance, tilting routings are used in the gate and drain connections.

6.3. Dummy Devices

To reduce the over-etching effect during fabrication, it is recommended to place dummy devices around the transistors [2]. Fig. 6.2 shows the schematic of a differential pair with both two-dimensional common centroid technique and dummy devices. There are eight

dummy transistors required in a common centroid layout as illustrated in Fig. 6.1. Each quarter requires two dummy transistors, one at each end.

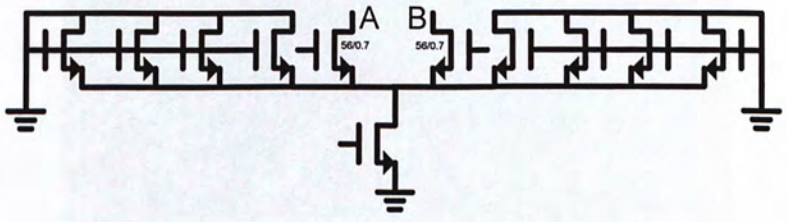

Fig. 6.2 Schematic of a differential pair with dummy devices

In the layout shown in Fig. 6.3, there are two dummy transistors connected to the two ends of each transistor. Since the gates of these dummy transistors are all grounded, they do not affect the overall aspect ratio. However, the dummy transistors do increase the total parasitic capacitance.

By extraction, the additional parasitic capacitance of each sense amplifier is 2.58 fF. This causes 40 ps additional latency for the new sense amplifier.

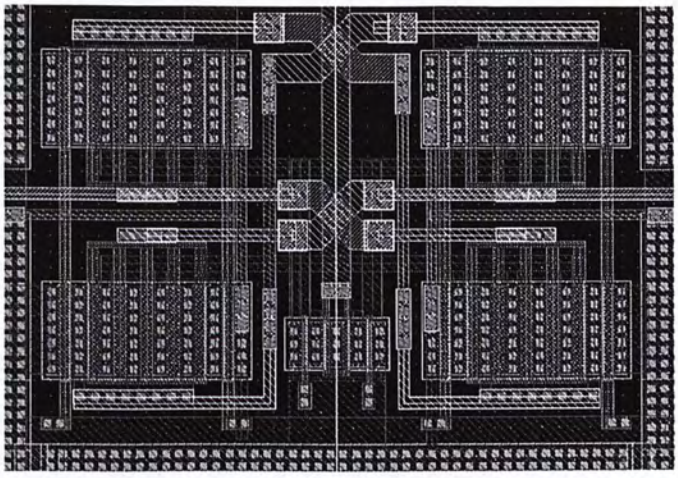

Fig. 6.3 Example of two-dimensional common centroid layout

6.4. Summary

By using common centroid layout technique and dummy devices, the effects of thermal, process gradient and over etching are reduced.

6.5. References

[1] Alan Hastings, The Art of Analog Layout 2nd Edition. Pearson Prentice Hall, 2006.

[2] Christopher Saint and Judy Saint, IC Mask Design Essential Layout Techniques. McGraw – Hill, 2002.

7. Simulation Results

7.1. Introduction

We have performed a number of different simulations to verify the design. All the simulations were simulated with a 3.3V 0.35-μm CMOS at 1.8V power supply. We will present three groups of simulation results. The first group looks at the performance of the sense-amplifier. The second group is a whole system simulation of quaternary current mode system with conventional and new sense-amplifier designs. The third group is a whole system simulation which compares the performance of the new quaternary current mode interconnect against the invert chain based interconnect.

7.2. Simulation of Different Aspect Ratios of Differential Pair

In this section, we will present the power, delay and kick-back noise simulations of the sense amplifier under 100 MHz clock frequency. A conventional design shown in Fig. 4.2 is used as a reference to gage the performance of the new sense-amplifier with isolated differential pair. A simplified schematic diagram of the new sense amplifier is shown in Fig. 4.3 and a complete schematic diagram with all the aspect ratio of the transistors is shown in Fig. 10.2 in Appendix.

Fig. 7.1 is the power simulation at different aspect ratios. As we have discussed in Chapter 4, the new design isolates the parasitic capacitance, which reduces the power consumption at large aspect ratio. The simulation results demonstrate that the power consumption of the new design has a very small dependence on the aspect ratio, while the conventional design is linearly dependent to the aspect ratio.

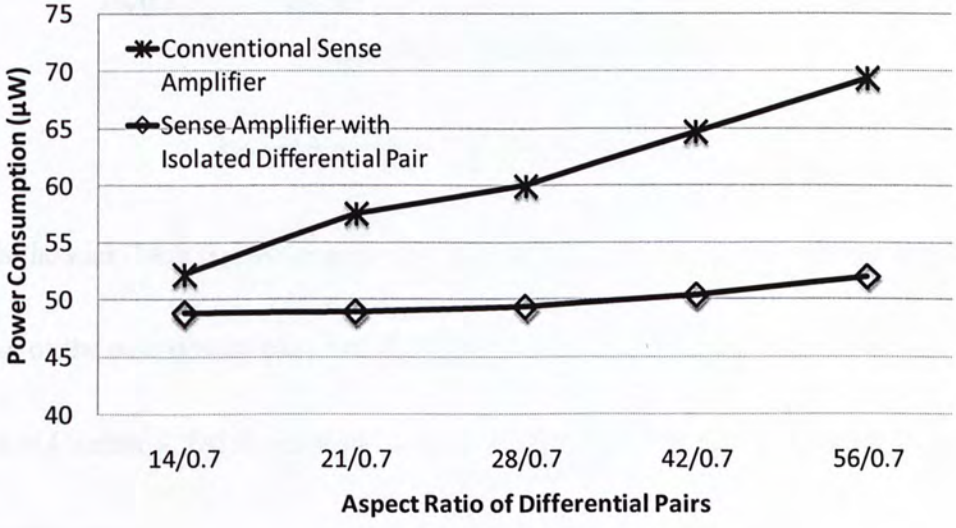

Fig. 7.1 Power consumption simulation of different aspect ratios

From the latency simulation results shown in Fig. 7.2, it is found that the latency of both sense amplifiers decrease as the aspect ratio of the differential pair increase. The simulation result also shows that the latency of the new sense amplifier is shorter than the conventional one because of the smaller parasitic capacitance.

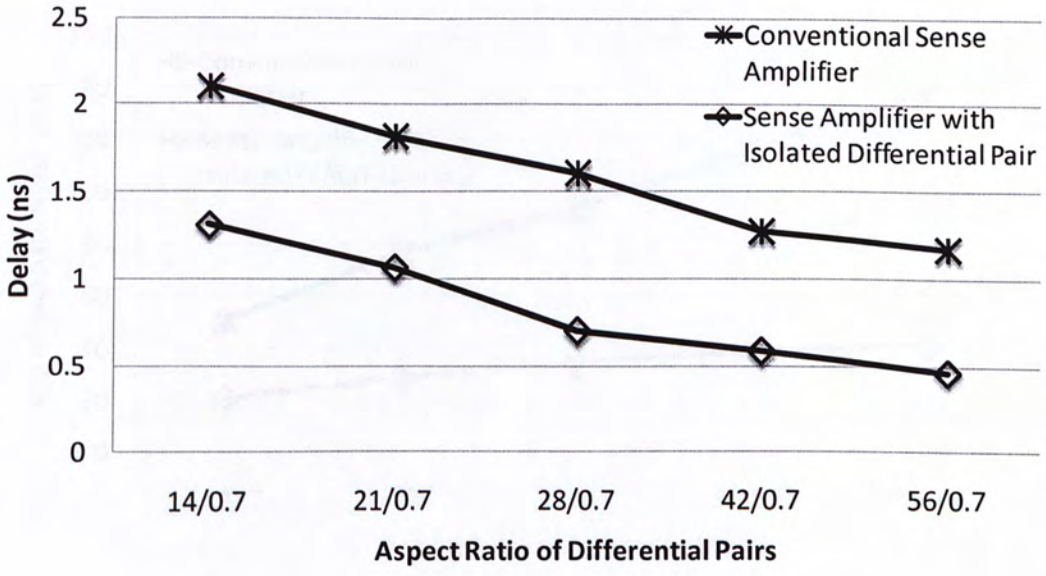

Fig. 7.2 Latency simulation of different aspect ratios

Fig. 7.3 is the kick-back noise simulation at different aspect ratios, which shows the kick-back noise of the new design has a smaller dependence on the aspect ratio as we have discussed in Chapter 4. On the contrary, the conventional design has a linear dependence on the aspect ratio.

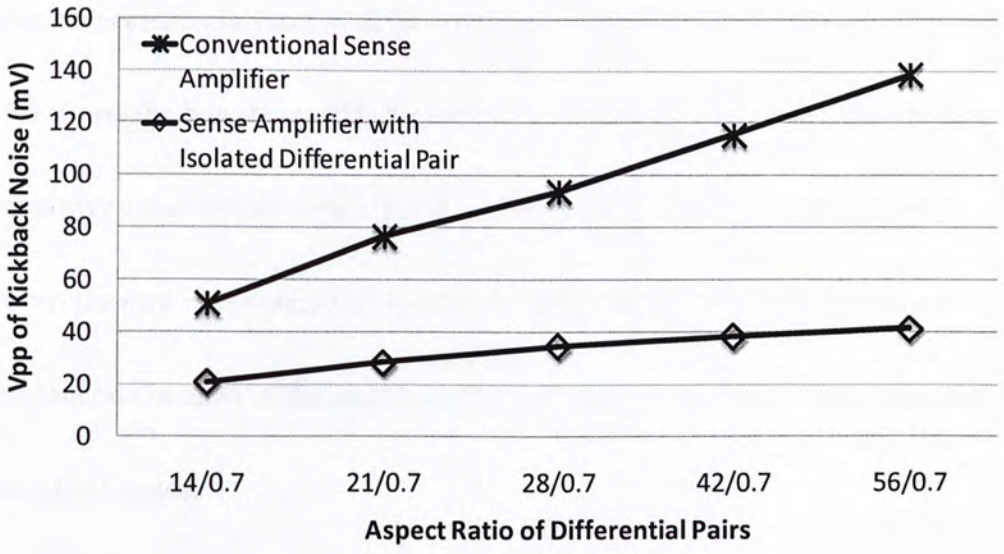

Fig. 7.3 Kick-back noise level simulation of different aspect ratio

The above simulations results verify the theoretical analysis in section 4.4 that the isolation clock transistors effectively shield the differential pair from charging at the RESET phase and prevent a large voltage variation at the drain terminals of the differential pair.

7.3. System Level Simulation with Different Sense-amplifiers

We have preformed system level simulation of the quaternary current mode bus driver and receiver system. This simulation is to verify the performance and maximum operating speed of the design. Two different systems are simulated, one with conventional sense-amplifier and one with the new sense amplifier design. A 500 μm long wire is used as the bus, which is modeled with a distributed π-model. The

complete schematic diagrams of these two systems are shown in Fig. 10.9 in Appendix. Fig. 7.4 shows the power simulation results of these two systems, both systems have shown power consumption which increases linearly as a function of the data rate. However, the new sense-amplifier system consumes less power and operates under higher data rate because of the shielding effect of the isolation transistors, which we have discussed in Chapter 4.

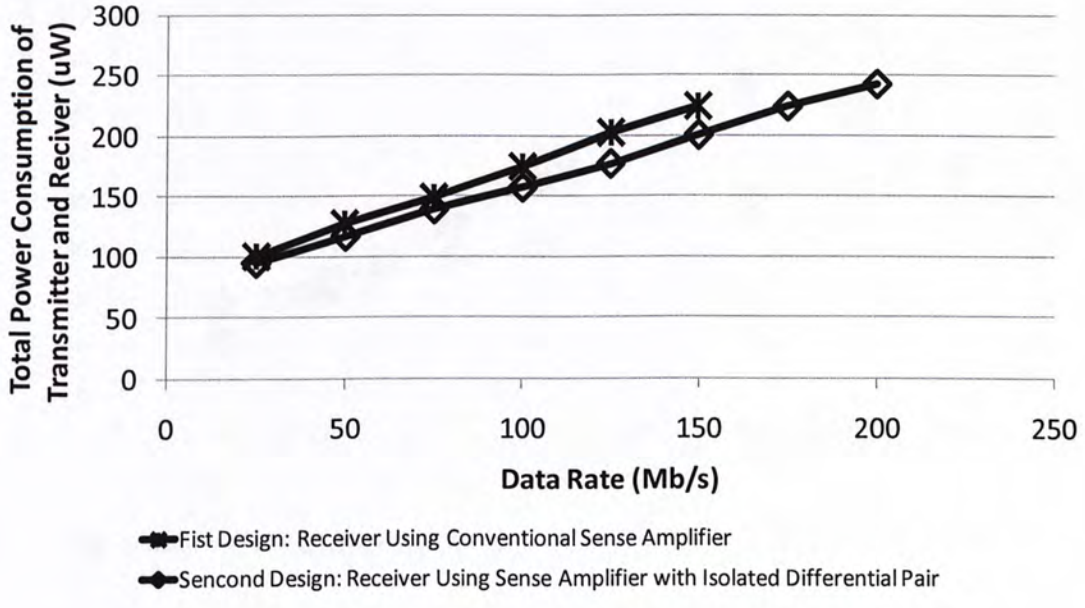

Fig. 7.4 Power consumption simulation result of system with different sense amplifier under different data rate

7.4. System Level Simulation at Different Data Rate

Two different systems are simulated: one is a conventional inverter chain driver system which is used as a reference and the other one is the new quaternary current mode system.

The schematic diagram of the inverter chain test system is shown in Fig. 10.10 in Appendix and the quaternary current mode system is the same as the one with isolated differential pair sense amplifier. Since the inverter chain driver system is binary, we have to multiply the simulated power consumption by 2 to match the data rate of the quaternary current mode system.

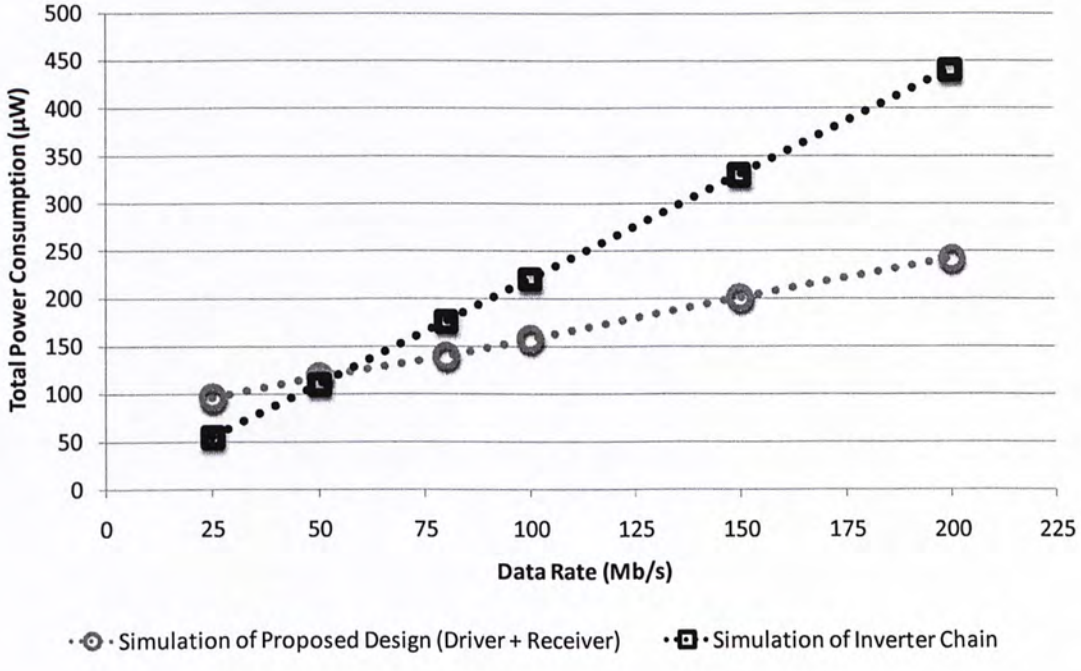

Fig. 7.5 Power consumption simulation result of two interconnect system under different data rate

The simulation results shown in Fig. 7.5 indicate that the new design is more power efficient at high data rate as we have predicated in Chapter 4. At 200 Mb/s, the new design consumes around 40% less power than the conventional inverter chain system.

7.5. Summary

The simulation results have demonstrated that the new sense-amplifier design has a significant improvement on power consumption, speed and kick-back noise compared to the conventional design. Moreover, system level simulation results indicate that the new quaternary current mode system is more power efficient when operating at high data rate.

8. Measurement Results

8.1. Introduction

We have designed and fabricated three test chips to verify the new design. The simulation results of the three test chips are presented in Chapter 7 and the schematic diagrams are listed in Appendix. All the test chips were fabricated with a 3.3V 0.35-μm CMOS process at Austria Microsystems.

8.2. Experimental Setup

8.2.1. Testing Chips

The three test chips are: quaternary current mode using conventional sense -amplifier, quaternary current mode using isolated differential pair sense-amplifier, and conventional inverter chain driver. The microphotographs of these three test chips are shown in Fig. 8.1-8.3. All three test chips have a Metal 1, 1 μm wide and 500 μm long wire connected the driver and receiver. The two quaternary test chips have identical transmitter, which occupies an area of 50 μm × 40μm. The receiver of first chip, which uses conventional sense amplifier as comparator has an area off 155 μm × 155 μm and the receiver of second chip, which uses the new sense amplifier has an area of 160 × 155 μm.

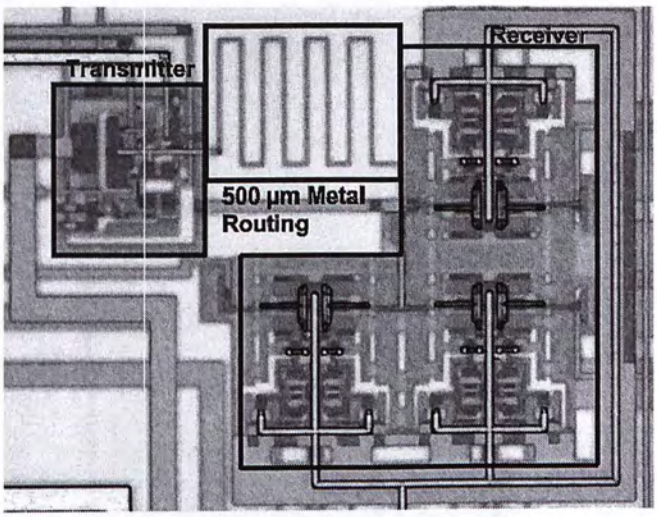

Fig. 8.1 Interconnect using conventional sense amplifier as comparator

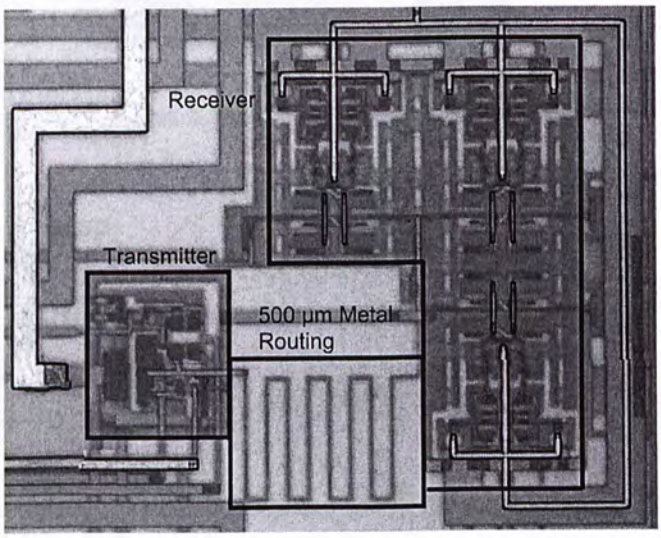

Fig. 8.2 Interconnect using sense amplifier with isolated differential pair as comparator

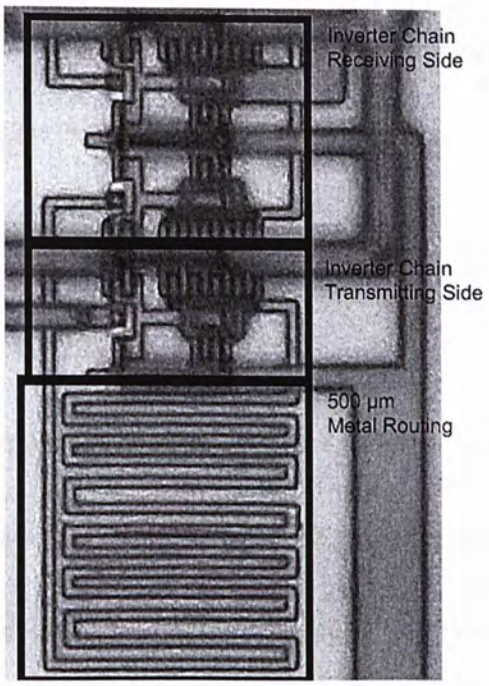

Fig. 8.3 Interconnect using inverter chain

8.2.2. **Equipments Setup**

Agilent Technologies 16720A Pattern Generator was used to generate binary inputs to the test circuits and LeCroy Waverunner 6100A 1GHz Oscilloscope was used to monitor the outputs of the receiver. Fig. 8.4 illustrates the block diagram of the measurement setup.

Fig. 8.4 Block diagram of measurement setup

All the measurements were performed at a 1.8V voltage supply. The reference current I_{ref} is 12 μA and the four internally generated current steps are 12 μA, 24 μA, 36 μA, and 48 μA.

8.3. Measurement Results

The measured power consumption (transmitter and receiver) of the two quaternary current mode test chips are shown in Fig. 8.5. The measured results agree quite well with the simulation results presented in Chapter 7. Table 8.1 summarized the measurement results of these two test chips.

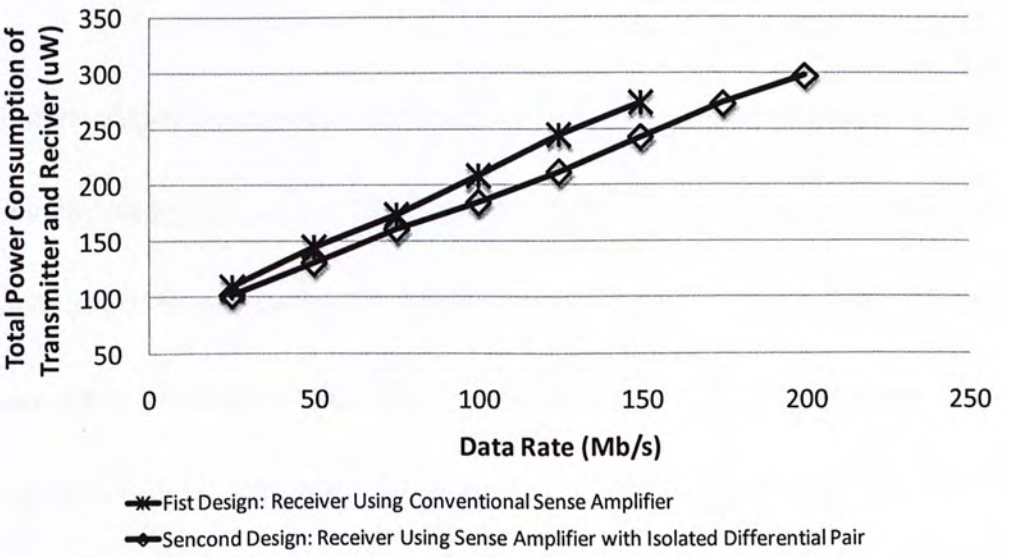

Fig. 8.5 Power consumption measurement of quaternary current mode interconnect

TABLE 8.1 Measurement Results

	First Design	Second Design
Process	3.3V 0.35 μm	3.3V 0.35 μm
Power Supply	1.8 V	1.8 V
Maximum Data Rate	150 Mb/s	200 Mb/s
Transmitter Power Consumption at 150 Mb/s	78 μW	75 μW
Receiver Power Consumption at 150 Mb/s	195 μW	167 μW
Total Power Consumption at 150 Mb/s	273 μW	242 μW
Delay (Including Output Buffer by measurement)	6 ns	5.3 ns
Delay (Excluding Output Buffer by Subtraction)	1.8 ns	1.1 ns

The first test chip with conventional sense amplifier has a maximum data rate of 150 Mb/s and the second test chip with the new sense-amplifier has a maximum data rate of 200 Mb/s. The 25% increase in data rate is a result of the new isolated differential pair sense-amplifier, which reduces the kick-back noise and latency. This is because the sense amplifier with isolated differential pair in the second chip provides better kick-back noise isolation that that in the first chip. Moreover, the test chip with the new sense-amplifier also has lower power consumption and delay.

The second measurement compares the power consumption of the new quaternary current system with an inverter chain reference circuits. The measured propagation delay of the new quaternary current system is 1.1ns and that of the inverter chain based one is 1.3ns. The measured results shown in Fig. 8.6 agree with the simulation shown in Fig. 7.5. The new quaternary current mode system is more power efficient at high data rate than the reference system.

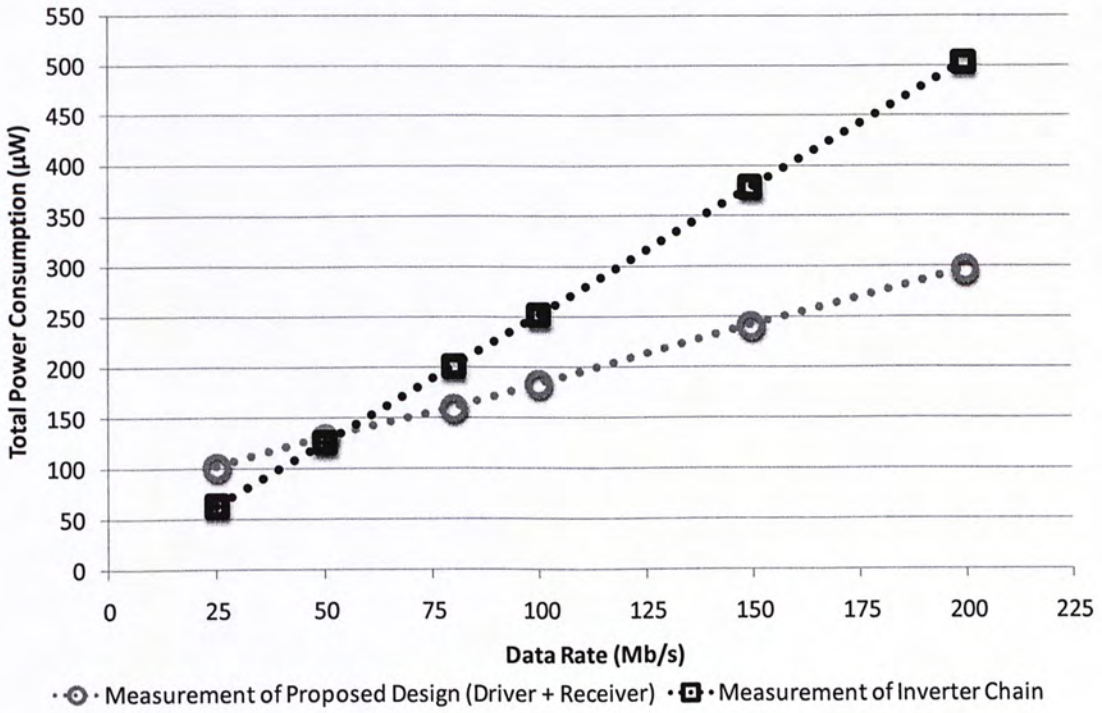

Fig. 8.6 Measurement result of relationship between power consumption and data rate

8.4. Summary

The measurement results agree quite well with the simulation results presented in Chapter 7. We can conclude that the new quaternary current mode system using the new sense - amplifier design is more power efficient to drive long interconnect at high data rate.

9. Conclusion

9.1. Author's Contributions

This thesis presents the design of a new quaternary current mode bus driver and receiver circuits. One of the main features of this design is to reduce number of interconnection wires by half using quaternary logic.

We have designed and fabricated three test systems to verify the new design. The measurement results indicated that the new sense amplifier is more efficient than conventional sense-amplifier. It generates less kick-back noise and consumes less power than the old design. Moreover, the new sense-amplifier design has increased the data rate from 150Mb/s to 200 Mb/s.

We have also designed and built a conventional inverter chain driver and receiver circuits as a reference to benchmark the performance of the new design. The measurement results indicate that the new design consumes less power at high speed. However, the new design loses the power consumption advantage at low speed operation because of the added circuit complexity of the new design.

9.2. Future Works

We have demonstrated in this work that there are significant advantages of using quaternary logic in bus driver and receiver circuits. It will be interesting to carry this research to a higher multi-level logic such as six or eight levels.

10. Appendix

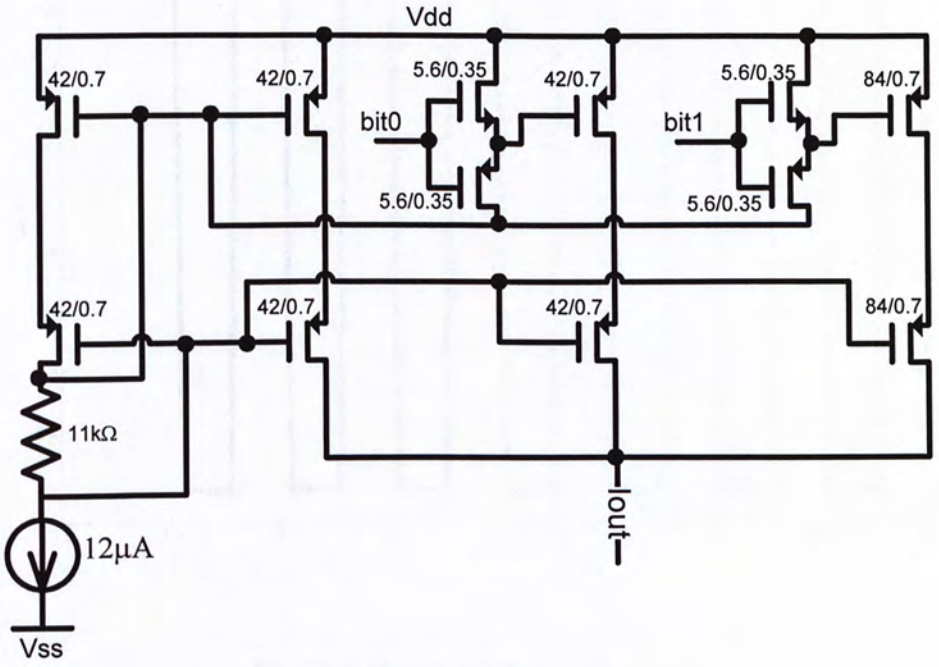

Fig. 10.1 Complete schematic of the current mode transmitter

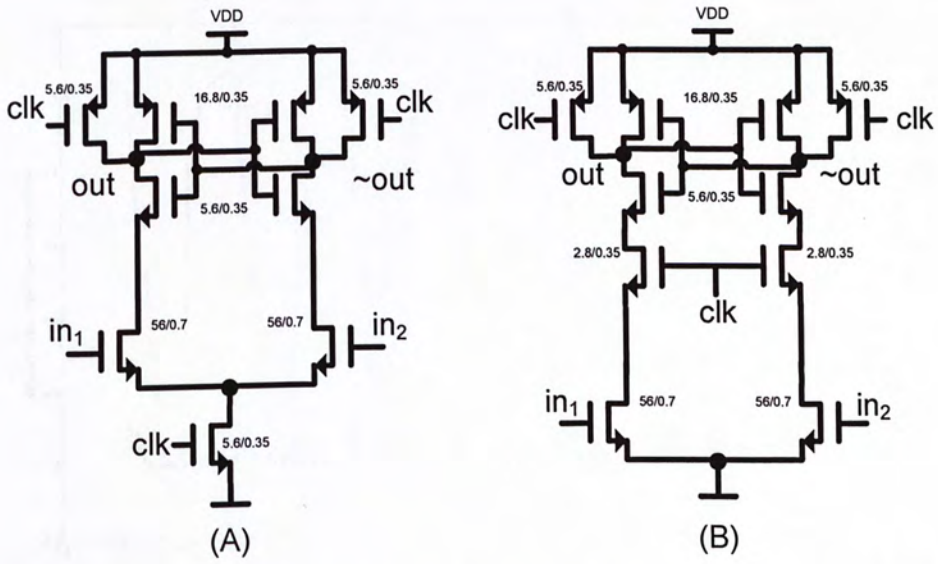

Fig. 10.2 Complete schematic of the conventional sense amplifier (A) and sense amplifier with isolated differential pair (B)

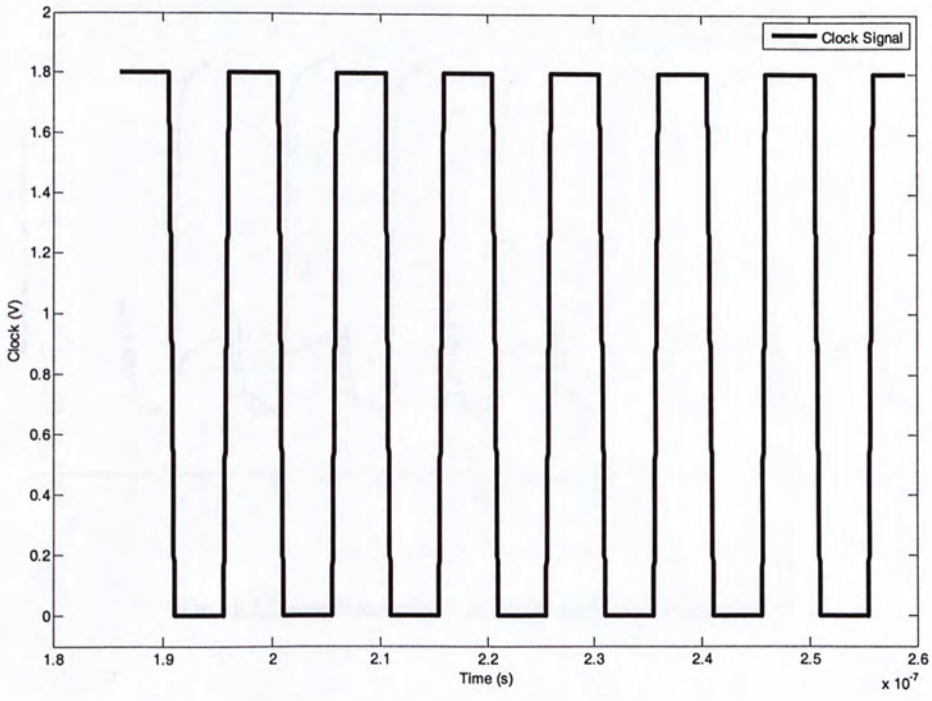

Fig. 10.3 Transient Waveform of the Clock Signal

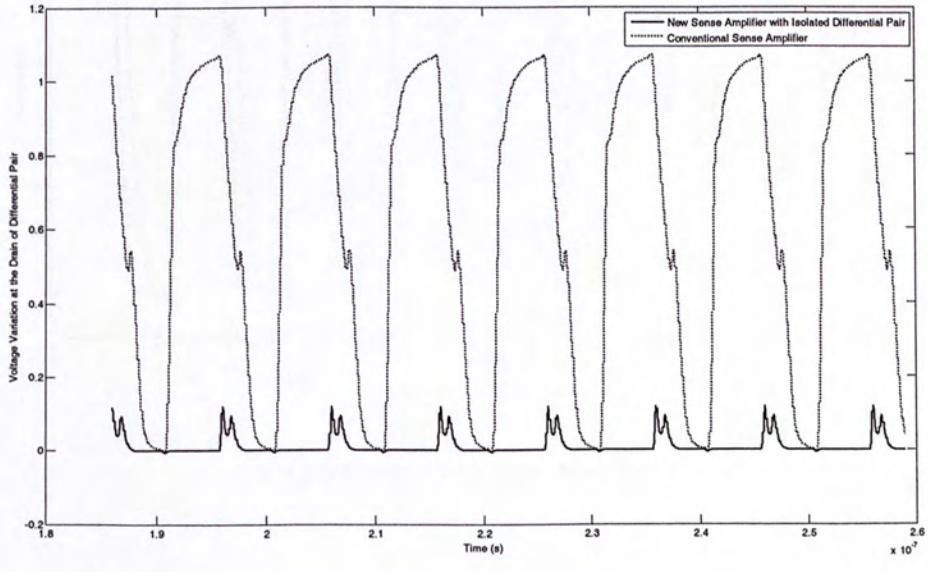

Fig. 10.4 Transient Waveforms of the Drain of Differential Pairs

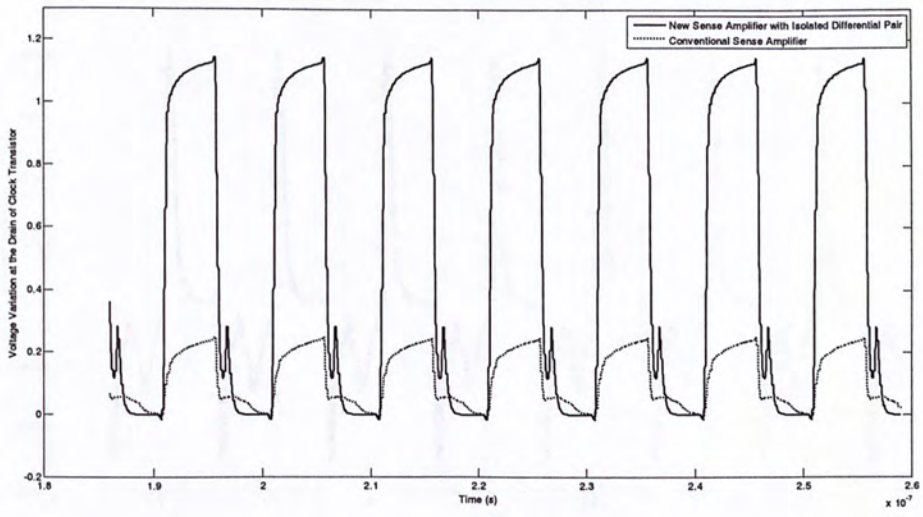

Fig. 10.5 Transient Waveforms of the Drain of Clock Transistors

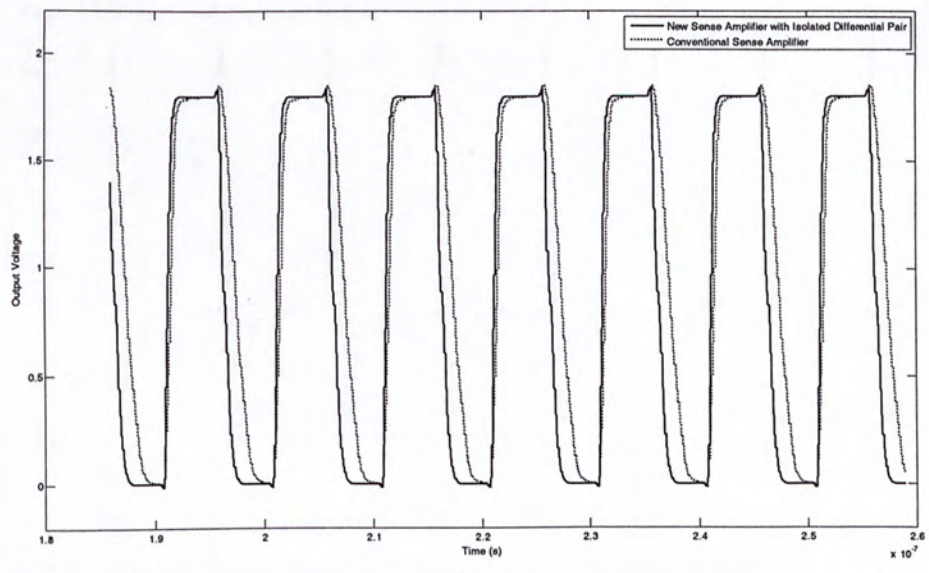

Fig. 10.6 Transient Waveform of the Outputs

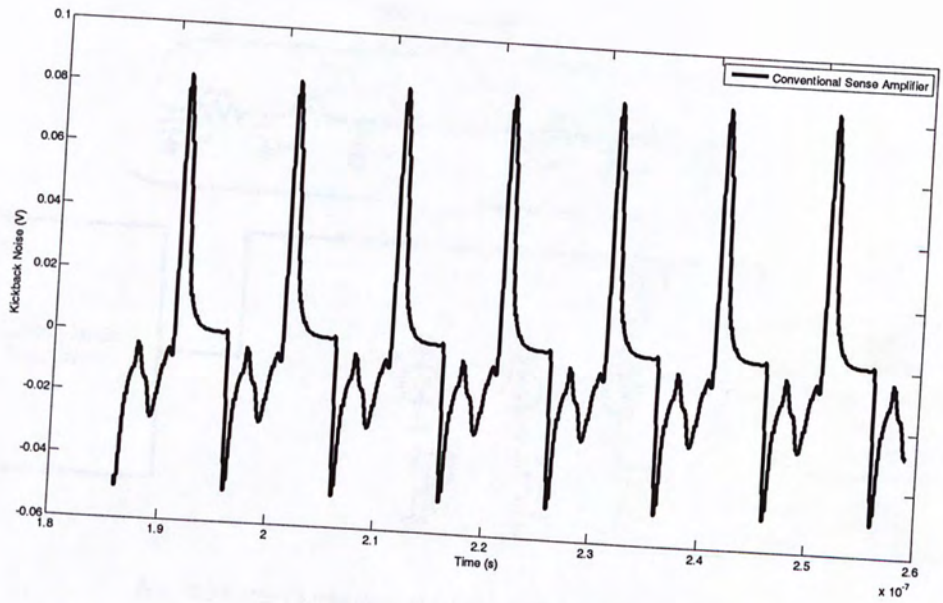

Fig. 10.7 Transient Waveform of Kickback Noise of the Conventional Sense Amplifier

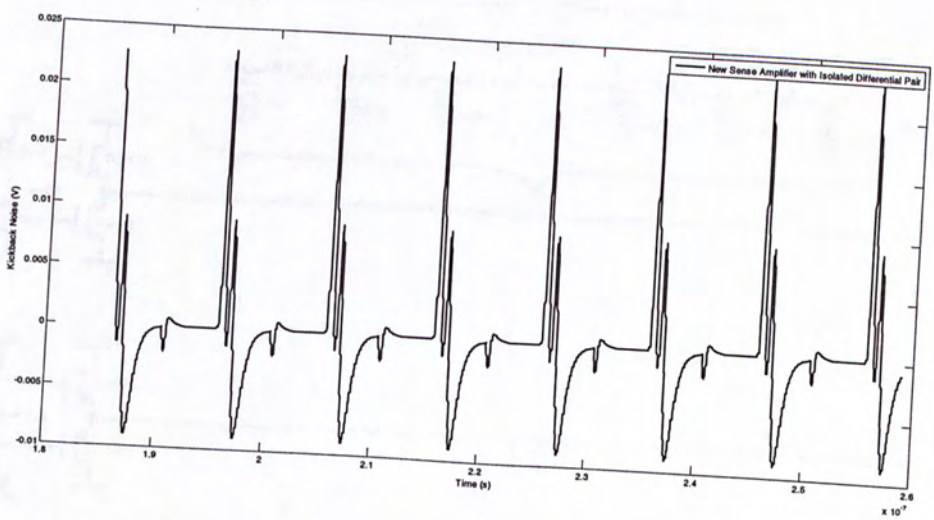

Fig. 10.8 Transient Waveform of Kickback Noise of the New Sense Amplifier

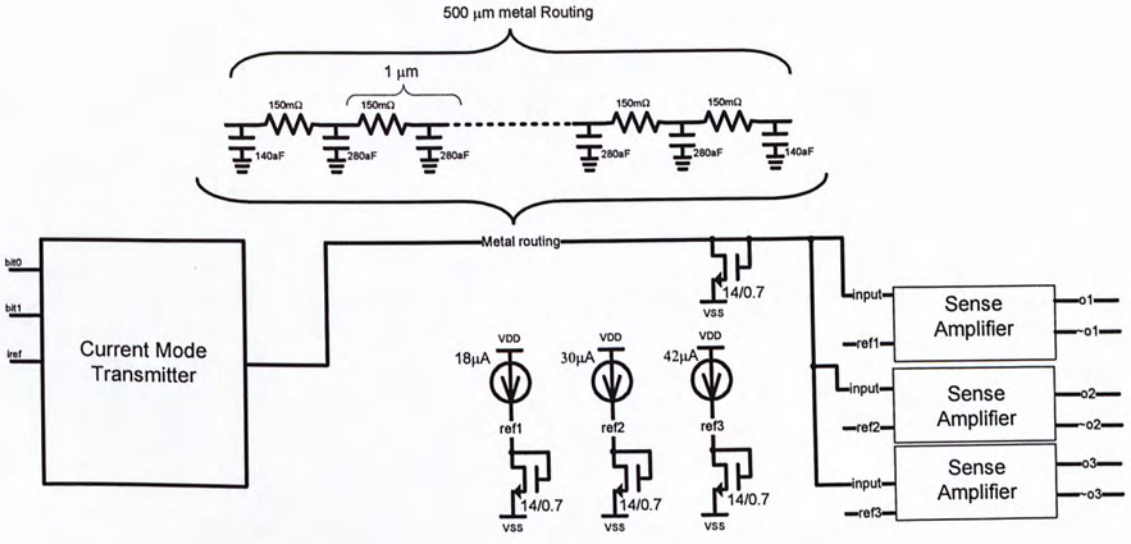

Fig. 10.9 Complete schematic of the proposed current mode interconnect

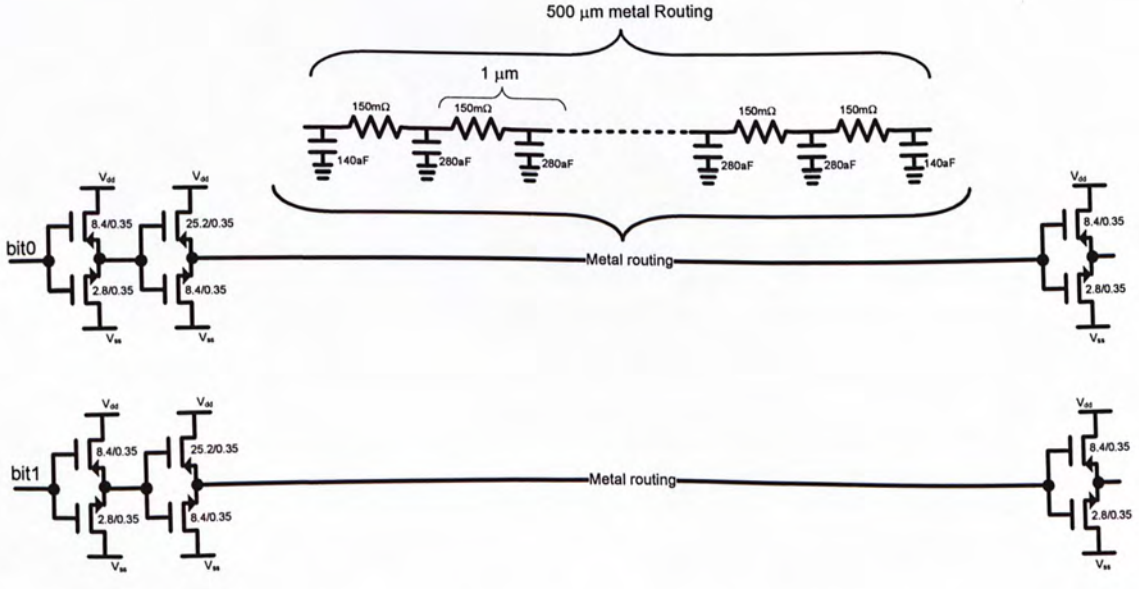

Fig. 10.10 Complete schematic of the inverter chain based reference interconnect