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Misfit strain relaxation and dislocation formation in supercritical strained silicon on virtual substrates

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Relaxation of strained silicon on 20% linear graded virtual substrates was quantified using high resolution x-ray diffraction and a defect etching technique. The thickness of strained silicon was varied between 10 and 180 nm. Relaxation was observed in layers below the critical thickness but increased to only 2% relaxation in the thickest layers even with annealings up to 950 °C. Cross-sectional transmission electron microscopy revealed stacking faults present in layers thicker than 25 nm, and nucleated 90° Shockley partial dislocations forming microtwins in the thickest layer. These features are implicated in the impediment of the relaxation process. © 2007 American Institute of Physics. [DOI: 10.1063/1.2769751]

Tensile strained silicon used in the channel region of transistors has been demonstrated to produce an improvement in the charge carrier transport properties above that of bulk silicon.¹ The most widely used method of fabricating globally strained silicon for device processing employs SiGe virtual substrates as growth templates. In order to be acceptable for use in industry, strained layers must ideally be defect free and maintain strain during device processing.

Due to relaxation processes of the virtual substrate, threading dislocations are grown into the strained silicon layer. Relaxation of the layer will proceed by the strain-induced glide of these threading dislocations, forming misfit dislocations at the strained interface.² The critical thickness of strained silicon is therefore described by the Matthews and Blakeslee mechanical equilibrium theory³ for relaxation via preexisting dislocations. For the case of silicon on 20% Ge content virtual substrates, the critical thickness is approximately 13 nm.

Linearly graded virtual substrates of 20% Ge composition were grown using low pressure chemical vapor deposition. The SiGe was graded at a rate of 10% μm^{-1} with a 2 μm final constant composition layer. Each virtual substrate was capped with strained silicon in the range of 10–180 nm at 700 °C. An accurate measurement of the thickness of the strained silicon layers was obtained by cross-sectional transmission electron microscopy (XTEM).

Reciprocal space maps using high resolution x-ray diffraction (HRXRD) around the (224) and (004) reflections were employed to ascertain the relaxation of the strained silicon layers. The relaxation of the final constant composition layer of the virtual substrates and their exact Ge contents were also determined, which dictates the amount of strain the strained silicon layers are subjected to. The results of the strained silicon relaxation are shown in Fig. 1. The relaxation is shown to saturate at around 2%, and is overall very low, compared to the relaxation of compressively strained SiGe layers under the same degree of strain.⁴

HRXRD reciprocal space maps display peak broadening of the strained silicon peak due to mosaicity⁵ caused by the

presence of misfit dislocations at the strained silicon interface, which warp the diffraction planes. The effect is more pronounced in thicker samples, where the misfit dislocation density (MDD) is greater. Peak broadening limits the accuracy for determining strain (this gives the error bars in Fig. 1). For the thinner strained silicon layers, detectable x-ray intensities are close to the background noise level, making resolution of the peak even more prone to error. Scans were conducted over a 22 h period to maximize the signal-to-noise ratio, but the technique still only yields sufficient x-ray intensity for layers thicker than 15 nm.

Annealing of strained silicon layers is known to induce Ge diffusion from the virtual substrate,⁶ which will reduce its thickness. In order to determine a suitable range of temperatures over which to conduct annealings, secondary ion mass spectroscopy (SIMS) performed a 32 nm strained silicon layer in the as-grown state and after it had been subjected to annealings for 1 h at 750, 850, and 950 °C (Fig. 2). The Ge concentration gradient into the strained silicon layer does not deviate much from the as-grown state for the 750 and 850 °C annealings. Relaxation measurements performed using these annealing conditions assumed the layer thickness to be unchanged.

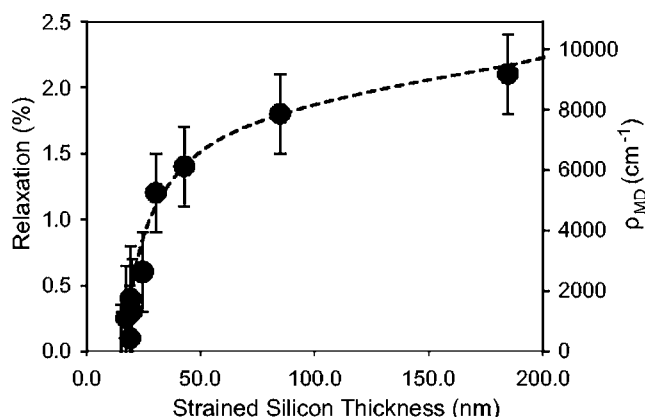


FIG. 1. Measured relaxation of strained silicon layers using HRXRD from 15 to 180 nm.

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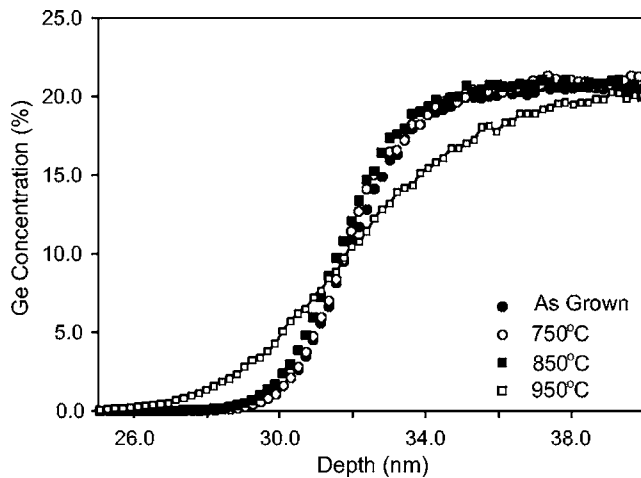


FIG. 2. SIMS profile for a 32 nm strained silicon layer in the as-grown state, and annealed at 750, 850, and 950 °C for 1 h.

Misfit dislocations at the strained silicon/virtual substrate interface were revealed with a dilute Schimmel etchant.⁷ The etched surface could then be imaged using a differential interference contrast microscope which images an area of $75 \times 100 \mu\text{m}$. The etch rate was found to be 5 nm s^{-1} in silicon layers and 20 nm s^{-1} in 20% SiGe layers from step measurements.⁸ Each sample was exposed to the etchant for 10 s to reveal dislocations at the strained interface and not from deeper in the structure. Figure 3 shows a magnified section of a typical etch image, revealing the additional presence of extended stacking faults in the layers.

The total plastic strain relief δ in an (etched) image area can be determined by measuring the misfit dislocation line density ρ_{MD} (total length of misfit dislocations per unit area). For strained silicon, dislocations are typically of 60° type. Relaxation is therefore given by⁹

$$\delta = \frac{a_{\text{Si}}}{2\sqrt{2}} \rho_{\text{MD}}, \quad (1)$$

where a_{Si} is the lattice constant of bulk Si.

In materials under tensile strain, it is known that strain can dissociate 60° perfect dislocations into 90° and 30° Shockley partial dislocations.¹⁰ For sufficiently large strain, the 90° partial will break away from the 30° , creating an

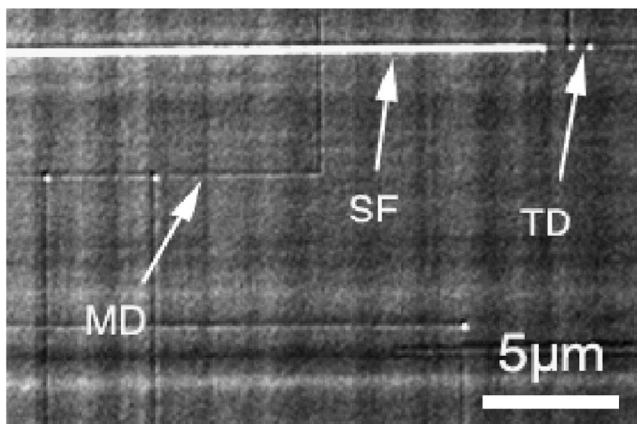


FIG. 3. Close-up of a typical etch image from a 20 nm strained silicon layer, showing misfit and threading dislocations and extended stacking faults.

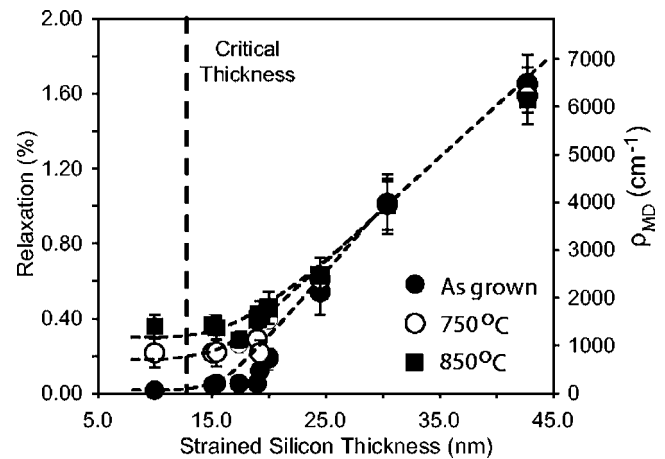


FIG. 4. Strained silicon relaxation variation with thickness and anneal. Lines are for guidance only. Errors are determined by standard deviation of the averaged results.

adjoining stacking fault. As the 90° partial leads, the relaxation of the line density of stacking faults ρ_{SF} in the considered area is given by

$$\delta = \frac{a_{\text{Si}}}{3\sqrt{2}} \rho_{\text{SF}}. \quad (2)$$

HRXRD results for the residual strained state of the underlying virtual substrate and its exact Ge fraction gives the maximum amount of strain each silicon layer is subjected to, allowing δ to be expressed as a percentage.

The MDD of each etched sample was determined by measuring the total length of misfit dislocations in $75 \times 100 \mu\text{m}$ image areas and averaging over ten different images randomly taken from the sample surface. Using this data combined with HRXRD measurements on the virtual substrate composition and relaxation, the relaxation of the strained silicon could be determined as a function of thickness using Eqs. (1) and (2) (Fig. 4). This analysis was performed on each sample before and after annealing at 750 and 850 °C for 1 h in nitrogen ambient.

The threading dislocation density (TDD) was evaluated to be $2(\pm 1) \times 10^5 \text{ cm}^{-2}$ for all the layers up to 20 nm. Stacking fault densities (SFD) remained at $5(\pm 1) \text{ cm}^{-1}$ for thicknesses up to 20 nm, and increased sharply to $400(\pm 30) \text{ cm}^{-1}$ as the thickness exceeded 25 nm. The increase in SFD was accompanied by an expected rise in TDD, but only to $3(\pm 1) \times 10^5 \text{ cm}^{-2}$. No increases in TDD or SFD were observed after annealing.

Defect etch analysis was found to be useful only for layers up to 50 nm thick. Thicker layers exhibited a rapid rise in SFD, which made the accurate assessment of TDD and relaxation impossible. The stacking fault trenches become wider as the layer gets thicker, which increases the likelihood of these broader features masking other dislocation structures. This has profound implications for the material quality of thicker layers; as such a rise in SFD is accompanied by an increase in TDD.

Misfit dislocations (and low levels of relaxation) are observed even below the critical thickness, an anomaly that has been noted previously.⁹ As expected, the annealing process creates misfit dislocation segments by initiating glide of threading dislocations. This effect seems to be more pronounced in the thinner layers; samples below 20 nm show a

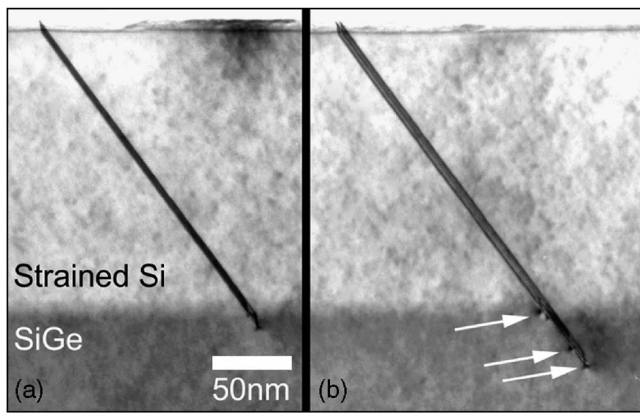


FIG. 5. Cross-sectional TEM image of a 180 nm strained silicon layer showing (a) a stacking fault and (b) a microtwin. Nucleated 90° Shockley partial dislocations are arrowed.

clear increase in relaxation with increasing annealing temperature. Minimal increases in relaxation in layers thicker than 20 nm are observed after annealing.

The overall relaxation implied by defect etching agrees to within the experimental uncertainty of the HRXRD results (Fig. 1). An explanation for the apparently limited relaxation has been offered by Freund through a mechanism of dislocation blocking¹¹ where the glide of threading dislocations is impeded by preexisting orthogonal misfit dislocations. Studies conducted into dislocation blocking have been mostly confined to compressively strained SiGe/Si heteroepitaxy,¹² where relaxation is observed to progress to a much higher degree.⁴ There is evidently a difference in the relaxation behavior between the compressive and tensile strained cases. It is thought that extended stacking faults, which only form in layers under tensile strain, play a much larger role in dislocation blocking than misfit dislocations,¹³ leading to lower levels of relaxation.

XTEM analysis confirms the presence of stacking faults in the strained silicon layers (Fig. 5). In the 180 nm layer microtwins were also observed, which can form in tensile strained layers when the strain energy is sufficiently large.¹³ 90° partial dislocations nucleate from the surface and glide as half-loops to the strained interface. The nucleation of a

second 90° partial dislocation on the same glide plane will repel the initial partial dislocation into the virtual substrate. Additional nucleation events will force other partial dislocations deeper into the structure, forming a microtwin.

The existence of microtwins in the 180 nm layer shows that the strain is no longer being sufficiently relieved by the glide of preexisting threading dislocations, and higher energy dislocation nucleation processes occur. This trend is expected to increase as the layers become thicker, with the eventual nucleation of perfect 60° dislocations around the critical thickness derived by People and Bean.¹⁴

In conclusion, strained silicon layers on virtual substrates many times the critical thickness have been shown to exhibit limited levels of relaxation, even after high temperature annealing. The possibility of stacking faults impeding dislocation glide in thicker layers is offered as an explanation for the apparent disparity between relaxation of compressive and tensile strained layers, which will be subject to further study. Despite the low levels of relaxation and TDD, the rapid increase in SFD and nucleation of microtwins in thicker layers may compromise the performance of electronic devices.

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