GaAs Optoelectronic Logic Devices

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" A thesis presented to the Chinese University of Hong Kong in partial fulfillment of the Degree of Master of Philosophy "

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1994

This thesis is dedicated to my Mother, who always give me her full support

Abstract

Careful design of logic circuits incorporated with Metal-Semiconductor-Metal photodiodes or photoconductive switches can be used to build optoelectronic logic devices. This approach offers the advantages of fast response and the possibility of monolithic integration with other optoelectronic and electronic circuits. In this research, an OR gate, an exclusive-OR gate, an exclusive-NOR gate and a 2 to 4 decoder have been demonstrated using a device structure consisted of a composite pair of GaAs photodetectors. The area of the active region is 10 μm x 40 μm. With an input optical energy less than 1 pJ, the output electrical signal has a FWHM of a few hundred picoseconds, which is among the fastest that have been reported. In addition, the electrical signal has been used to drive laser diodes to obtain the desirable optical output. Owing to the limited bandwidth of some amplifiers used in the setup, the response of the optical signal is not optimized. A FWHM of 850 ps with an on-off contrast ratio of 17 dB has been obtained. On the other hand, special input pulse trains have been constructed to test the functionality of the logic devices. Besides, a 3 to 8 decoder and a serial full adder have been proposed. All these devices will find important applications in optical computing and optical signal processing.

Acknowledgments

I would like to express my sincere gratitude to my supervisor, Dr. C. T. Shu, for his guidance and invaluable advice throughout the project. I would also like to thank my godfather, Dr. N. C. Poon, for his continuous encouragement and support. I am also indebted to Miss H. S. Choy for her help in the fabrication of devices. In addition, I would like to thank W. T. Hui for his support in mask production. Special thanks is given to K. W. Ho for preparing the experimental set-up used in gain-switching of laser diodes, and K. C. Tam for his valuable discussion on logic devices. Provision of the MQW laser from Dr. H. K. Tsang is gratefully acknowledged. Furthermore, the assistance and encouragement given by W. S. Chan, S. K. Chan, K. S. Choi, Y. C. Lee, K. S. Lee, L. M. Cheung, B. C. Lui and L. Y. Chan is highly appreciated. Last but not least, I have to thank God for His blessings throughout my study.

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1 INTRODUCTION

1.1 The Rise of Optical Computing

1.1.1 Limitation of conventional Von Neumann electronic computing

Nowadays, computer is indispensable to our daily life. Nearly all computers available are based upon VLSI circuits, etched in silicon. They run sequential programs that specify what to do at each step and are usually termed as Von Neumann electronic computers.

The limited interconnections between memory and processing elements, together with the interactions among electrons prevent the possibility of supporting multichannel communication through a single bus and of reducing the propagation delay of the electronic devices via miniaturization [1]. Because of this interconnection issue, there are some cases where the speed performance of the Von Neumann electronic computers cannot live up to requirements. These cases usually involve great masses of computation, such as image processing and large-scale simulation problems.

There are two proposed solutions to solve this problem. One is to incorporate artificial intelligence with logic programming [2]. Another deals with parallel computing. From the latter, optical computing arouses great interest owing to the inherent parallelism of optics.

1.1.2 Advantages of optical computing over electronic computing [2]

1. *Direct image processing*

   Images can be processed directly by specific optical systems, so there is no need for sampling, quantization, etc. Consequently, optical systems can operate faster with better resolution.

2. *High propagation speed*

   Electronic signals propagate two orders of magnitude slower than light. The reason is that electronic conductor has a capacitance that has to be charged and discharged. Therefore the propagation time increases with the length of connection. On the other hand, light transmission needs not suffer from this problem.

3. *Large bandwidth and Massive parallelism*

   Data channels, each with a greater bandwidth than of any electronic link, can operate in parallel owing to the fact that photons do not interact with each other. This massive parallelism and connectivity allows for much higher speed in data processing.

4. *Immunity to Electromagnetic Interference (EMI)*

   The intrinsic nature of photons make it not susceptible to EMI.

1.2 Present Status of Optical Computing

Roughly speaking, there exists three types of classification of optical computers. They are :

1. *analog* versus *digital*
2. *special purpose* versus *general purpose*
3. *all-optical* versus *hybrid*

It can be said that special purpose analog optical computer is relatively well developed. Optical processors for synthetic aperture radar imaging are one of the applications currently in wide use [2]. The realization of other special purpose analog optical processors depends on the resolution of dynamic range and space-bandwidth problems.

On the contrary, general purpose digital optical computer is still at a very early stage of development. It is expected that additional developments, especially in optical interconnections and material technology, will be needed to pave the road towards the implementation of an all-optical computer, or a hybrid electronic optical machine that can perform better than the electronic computer.

Owing to the supreme accuracy performance of digital system, nowadays more and more systems are digitized. The success of electronic computing has inspired the idea of making a similar optical counterpart to achieve higher speed. An electronic processor usually consists of many logic circuits which in turn compose of numerous logic gates. Thus, this is highly desirable for the development of optical computing if high

performance optical logic gates, which will be used as the building blocks for an optical processor, can be achieved.

1.3 Choice of Logic System

There exists two major logic systems for digital optical computing : *binary* logic and *multilevel* logic. Multilevel system has the advantage of allowing for more information in a basic unit. This increases effective data rates and storage densities. However, more elementary values have to be distinguished. It results in higher complexity and is more sensitive to noise. The main attractive feature of the binary system is its simplicity. It is also the well-developed system that has been utilized by nearly all electronic computers.

In this research, we are mainly interested in the binary logic devices.

1.4 Representation Scheme

There exists different kinds of representation scheme for a binary digital system. In electronic systems, the most well known schemes include on-off keying (OOK), frequency-shift keying (FSK) and phase shift keying (PSK). For optical systems, we can also have time shift keying (TSK), polarization encoding, spatial encoding and the combined use of polarization and intensity encoding. The common representation schemes for the optical binary digital systems are introduced below.

1.4.1 On-off keying

This is the most popular scheme for electronic as well as optical systems. For most cases, bright true logic is adopted. That is, the presence of light represents the logic "1" and the absence of light represents the logic "0". Simplicity is its main advantage. However, it involves creation and destruction of energy and results in thermal and fanout problems. The unique characteristics of light has not been utilized in this representation scheme.

1.4.2 Time-shift keying

There exists a clock time window in time-shift keying. The existence of a pulse within the clock time window corresponds to a "1". When the pulse is out of the clock time window, we get a logic "0". Special materials and mechanisms have to be employed to produce the necessary time delay of pulse for this scheme. Moreover, a correlator may be needed to differentiate the two states.

1.4.3 Spatial encoding

Under this scheme, a binary number is represented by a spatially coded optical pattern which is composed of two areas, A and B, with complementary intensity. When the beam is at A, no light will be at B and this pattern can be defined as logic "1". On the other hand, when the beam is deflected to illuminate B, A will be dark and this pattern will be defined

as "0". Its problem is the difficulty of introducing sufficient deflection such that miniaturization of devices can be achieved.

1.4.4 Polarization encoding

Light has the property of possessing different polarizations. In implementing binary logic devices, the vertical and horizontal polarizations has always been used to represent the two logics. Thus, switching from one state to other causes no loss of energy, which is highly desirable for cascading. However, the polarizations of the input beams have to be maintained carefully.

1.4.5 Intensity and polarization encoding

In addition to the intensity used in OOK, polarization is also included in this scheme. As a result, we can have four possible combinations representing 2-bit patterns. Referring to Fig. 1-1, no light stands for 00, horizontal polarization for 01, vertical polarization for 10 and both horizontal and vertical polarization for 11.

The main advantage of this scheme is that more information can be encoded. However, its cascadability is in doubt as one of its possible output (1,1) is not a legitimate input logic.

In this research, the simplest encoding scheme, OOK is adopted with a bright true logic.

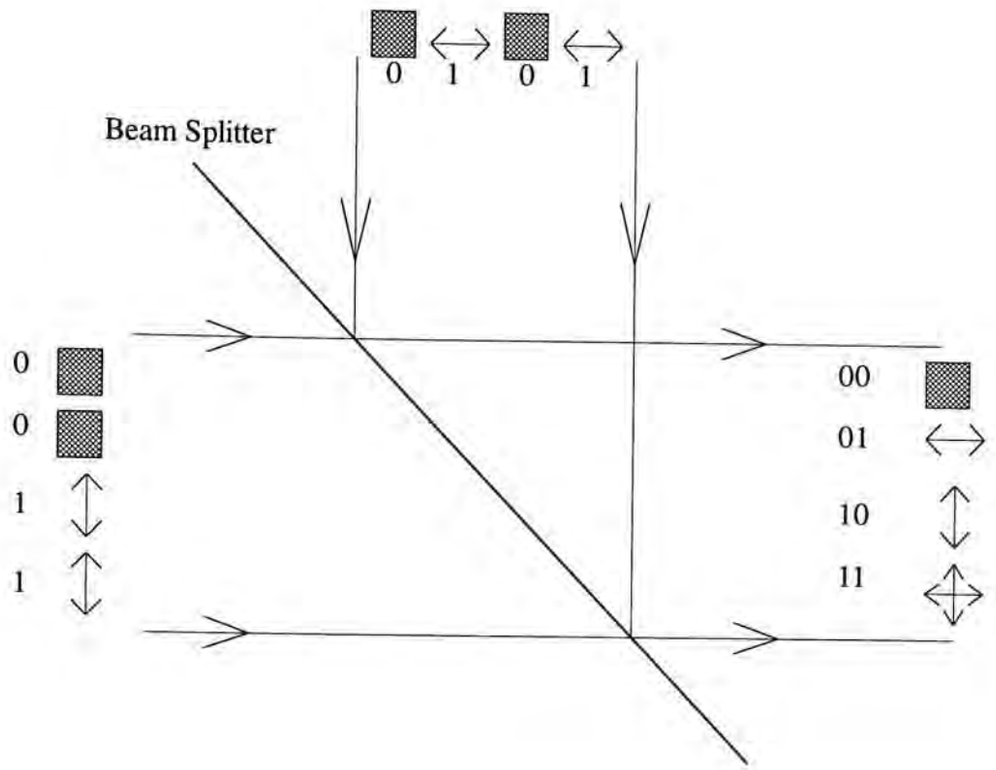


Fig. 1-1 Intensity and polarization encoding scheme

1.5 Binary Logic Elements

It is well known that all Boolean functions can be obtained by cascading NOR gates together. Thus, it seems that the simplest method to construct logic devices would be to demonstrate a cascadable NOR gate and then use it to build all the logic devices. However, optical computers should not be built by merely replacing electronic devices with optical devices. Implementing an optical logic system requires the optimum design of each logic device for trading off gate count and interconnection complexity. Different designs can lead to new architectures for logic systems and make optical implementations attractive where electronic implementations would not be practical [3].

In **Section 6**, it is seen that OR gates and exclusive-OR (XOR) gates are useful in constructing full adder which is an indispensable element in the arithmetic logic unit of a computer. Because of this, the implementations of these basic logic gates are reported.

With the design of the XOR gate, it is ready to find out that its complementary function, exclusive-NOR (XNOR) can be demonstrated in a similar manner. This function is particularly useful in code matching which is essential in parity checking.

Based on the XOR and the XNOR gates, a 2 to 4 optoelectronic decoder has been designed and demonstrated. A 2 to 4 decoder is a decision-making logic device with two inputs and four outputs. Depending on the actual binary value of the inputs, one and only one of its outputs would be turned on. With some modifications, a 3 to 8 optoelectronic decoder has been proposed as well. As their electronic counterparts have found important applications in the construction of the central processing unit, it is believed their development will also be crucial to digital optical computing.

A serial full adder has also been designed. A full adder is a three-input/two-output combinational logic circuit. At the i th bit location, it adds two binary digits, Ai and Bi, and a carry-in from the (i-1)-bit position, Ci-1. The proposed structure consists of two optoelectronic XOR gates and a carry generator. In its operation, the two input pulse trains are launched to the adder in a serial manner. The ability to function as a multi-bit binary adder may be its most prominent advantage.

1.6 Content of this Thesis

In **Section 2**, different approaches that have been used to implement binary optical logic devices are reviewed. A comparison of all-optical approach with optoelectronic approach is also made.

The core element in our logic devices, photodetector, is discussed in **Section 3**. Two types of high speed photodetectors have been used in this research. They are the photoconductive switches and MSM photodiodes. Design of simple logic gates with high speed photodetectors is also presented.

In **Section 4**, an account of the design, fabrication and mounting of the basic structure used in the logic devices is given. In addition, characteristics of the structure, such as single gap response, are investigated.

Details of the experimental environment and technique is presented in **Section 5**. First of all, the experimental procedure is listed. Next, light sources for providing the input logics as well as generating the output are introduced. Then elaborations are made on topics such as lock-in technique and optical path delay control. The automation of instrument control and data-acquisition is also discussed.

All the logic devices that have been designed and demonstrated using high speed GaAs photodetectors will be discussed in **Section 6**. Basic logic

gates that have been demonstrated includes OR, exclusive-OR and exclusive-NOR. For more complex logic device, we have a 2 to 4 decoder.

Finally, possible improvements and extensions of this project are discussed in **Section 7.** A serial full adder and a 3 to 8 decoder have been proposed. The conclusion is given in **Section 8**.

2 REVIEW OF OPTICAL LOGIC

2.1 All Optical

1. Shadow Casting Logic (SCL)
2. Soliton Dragging Logic Devices
3. Nonlinear Threshold Logic Devices
4. Liquid Crystal Light Valve (LCLV) Logic Gates

2.2 Optoelectronic / Hybrid

1. Directional Coupler Switches
2. Self-Electrooptic Effect Devices (SEEDs)
3. Phototransistors / Photothyristors integrated with Light Emitting Diode (LED) / Edge-Emitting Laser (EEL) / Vertical Cavity Surface Emitting Laser (VCSEL)
4. Logic Circuits implemented on Metal-Semiconductor-Metal (MSM) Photodetectors / Photoconductive (PC) Switches

2.1.1 Shadow Casting Logic (SCL)

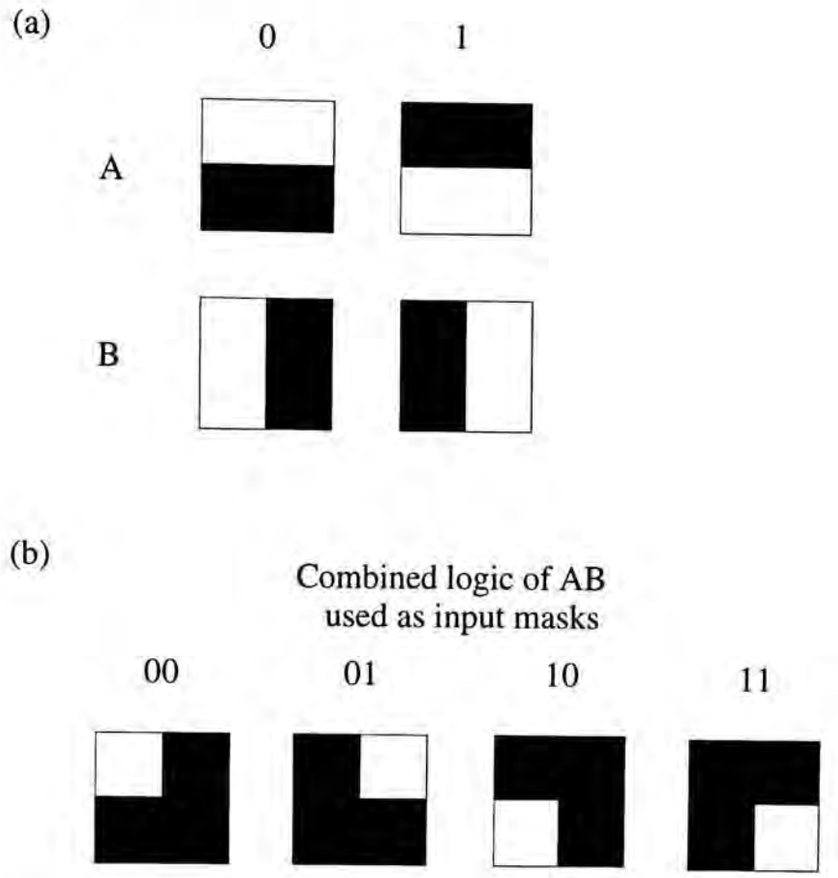


Fig. 2-1 (a) Coding of the two binary inputs of shadow casting logic
(b) Combinations of the two inputs superimposed on each other

In an optical shadow casting system, a two-dimensional spatially encoded pattern is used as data input. To produce the output, the pattern is illuminated by some combinations of 4 Light-Emitting Diodes (LEDs). Each LED will cast a shadow in a slightly different direction, and the shadows are interlaced to give out the output pattern [4,5]. Fig. 2-1 shows the shadow casting logic and Fig. 2-2 shows the configuration of the setup. Originally, the input pattern is represented by vertical and horizontal stripes of opaque and transparent bars. With this arrangement, all 16 binary logic functions can be performed. Later, polarized codes are

introduced such that more complex logic units like full adder can be realized [6,7].

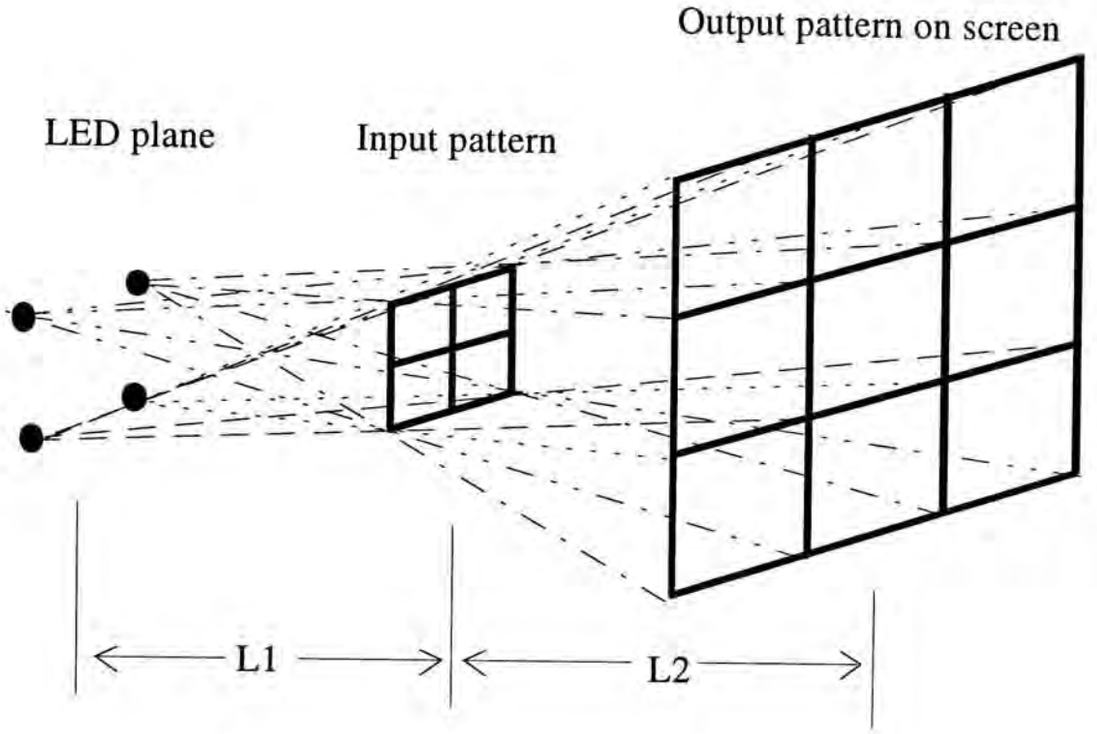


Fig. 2-2 Configuration of a shadow casting system

Advantages :

1. It is optically simple because no lens or nonlinear devices are needed.
2. It is flexible as all 16 binary functions can be performed without any changes to the system configuration, only the number of LEDs used needs to be changed.
3. Once the inputs are encoded, the computation speed is limited only by the speed with which light travels from the input plane to the output plane [8].

Problems :

1. It is difficult to encode the inputs. This also makes direct cascading of gates impossible.

2. Problem of spreading of the output pixel arises due to the use of divergent point source.

2.1.2 Soliton Dragging Logic Devices

In soliton dragging, two pulses in a fiber interact through cross-phase modulation and results in a chirp in frequency. The frequency shift is converted to a time shift by propagating in a dispersive delay line. The output is then read out by the time-shift-keyed format. A schematic diagram showing the demonstration of a NOR gate is shown in Fig. 2-3 [9]. It consists of two birefringent fibers connected through a polarizating beamsplitter with the output filtered by a polarizer. The fiber length is trimmed so that in the absence of signals A or B, pulse C can arrive within the clock window and corresponds to a "1". When either or both signals are incident, they interact with pulse C through soliton dragging and pull C out of the clock time window. Input signals A and B are polarized orthogonal to C and are blocked by the polarizer at the output.

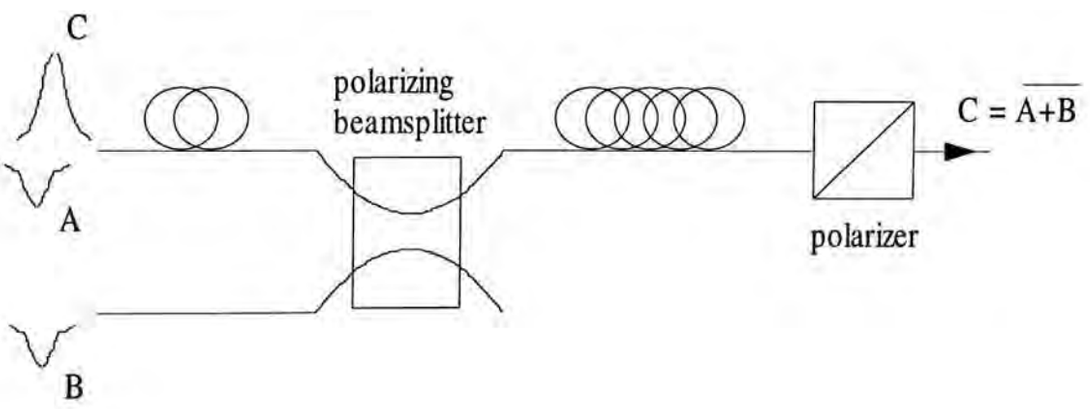


Fig. 2-3 A schematic diagram showing a soliton dragging NOR gate

Besides NOR, logic functions such as OR, AND, XOR and NOT have also been demonstrated [10,11]. Moreover a generalized exclusive-OR (GEO) module has been proposed which can be used to build more complex logic devices including decoders, demultiplexers and counters [12].

Advantages :

1. The switching energy is low, only a few pJ.
2. High speed of operation possible : hundreds of GHz.
3. It is cascadable with gain.

Problems :

1. Soliton has to be used.
2. The time-shift-keyed format output signal is not compatible with most available devices.

2.1.3 Nonlinear Threshold Devices

This type of nonlinear devices usually consists of a threshold level at some input level. There is no output when the input is below threshold. Otherwise, a constant output can be obtained. The inputs are always fed to this kind of devices simultaneously. The kind of logic functions implemented can be determined by the level of the threshold. For example, if the threshold is set to a level such that any one input can pass it, then the output function will be OR. If it is set in a way that requires the presence of both inputs to pass it, then the output function will be AND. The concept is illuminated in Fig. 2-4.

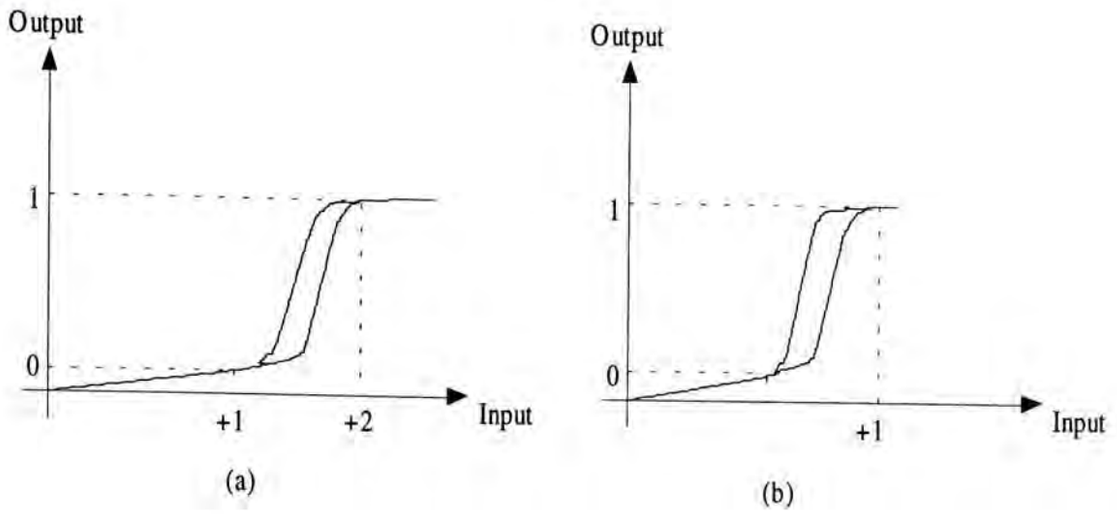


Fig. 2-4 IO characteristics of the nonlinear threshold (a) AND, (b) OR gate

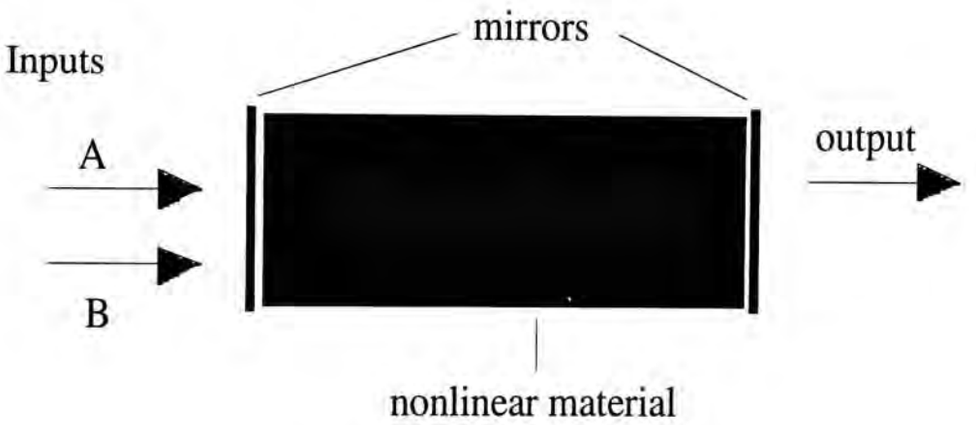


Fig. 2-5 A Fabry-Perot etalon

Logic functions including NOR, NAND, XOR, OR, AND and XNOR have been achieved with a Fabry-Perot etalon [13,14]. This resonator, as shown in Fig. 2-5, consists of two mirrors separted by some nonlinear material. This material has some nonlinear dispersive or absorptive characteristics such that the refractive index of the material can be changed with the incident light intensity. This in turn changes the path length and affects the

transmittance of the cavity. Speed ranges from μs to ps [15] have been reported, depending on the recovery time of the nonlinear material.

Advantages :

1. It is cascadable with gain.

Problems :

1. The threshold level places a lower limit on the power needed. To solve this problem, a hold beam may be used to set the operation level just below threshold. However it incurs another problem of critical biasing of the hold beam.
2. Materials with a large nonlinear optical effect and a fast response time are required for its success.

2.1.4 Liquid Crystal Light Valve (LCLV) Logic Gates

LCLVs can be viewed as controlled polarization changing mirrors and the binary logic values are represented by the two orthogonal linear polarizations of light. In operation, the inputs are made to shine onto the LCLVs before a read beam is reflected by them. The reflection of the read beam is accompanied by a change of polarization that depends on the intensity of the inputs. In this way, the inputs can influence the polarization of the reflected beam. A polarizer is then used to read the polarization state of the reflected read beam as the output. A schematic illustration of the operation of the light valve is shown in Fig. 2-6 [16].

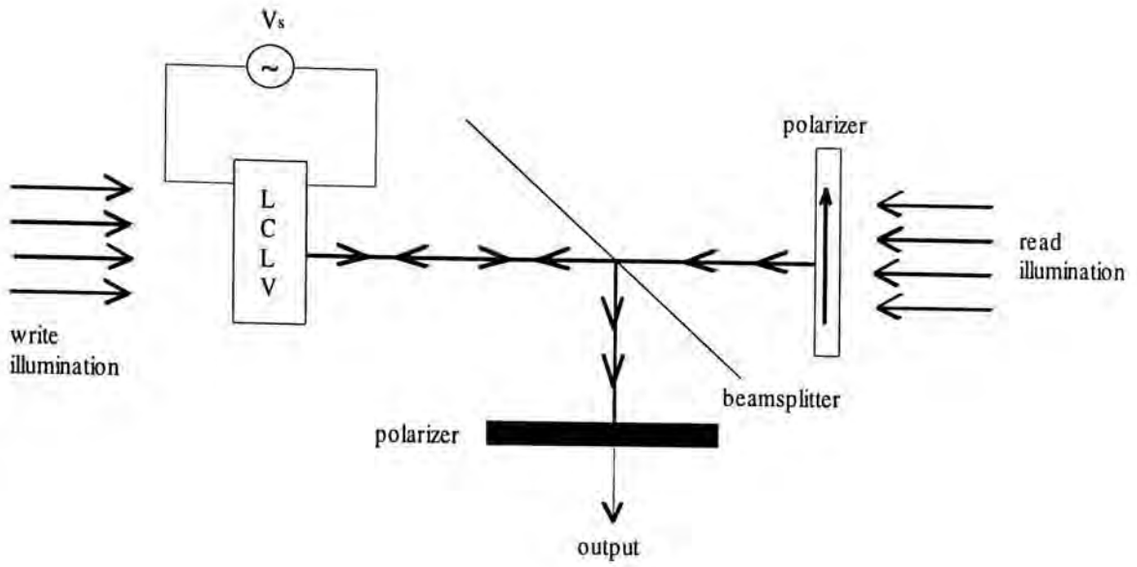


Fig. 2-6 An illustration showing the operation of a LCLV

All 16 boolean logic functions of two binary inputs have been demonstrated [17]. A simpler configuration to achieve the XOR and XNOR functions have also been reported [18]. Optical implementation of various types of flip-flop and their use in the design of shift registers and accumulators have been proposed [19]. Recently, two-dimensional operations are suggested to be performed by logic gates using ferroelectric LCLVs to build an optical digital processor [20].

Advantages :

1. It makes use of commercially available devices.
2. It enjoys the advantages of polarization logic as discussed in **Section 1**.

Problems :

1. It has slow response time, in the range of ms.
2. It is cascadable but with no gain.
3. It is optically complex.

2.2.1 Directional Coupler Switches

As shown in Fig. 2-7, when two waveguides are close together, energy periodically exchange between them as a function of distance. Based on this coupled mode theory, switching function can be achieved with a proper design of the waveguides. The distance separating the waveguides, the interaction length L and the refractive indexes of the materials can all affect the degree of coupling. By applying a bias voltage across a waveguide, its refractive index can be changed. Thus, the degree of coupling can be monitored with this electro-optic effect.

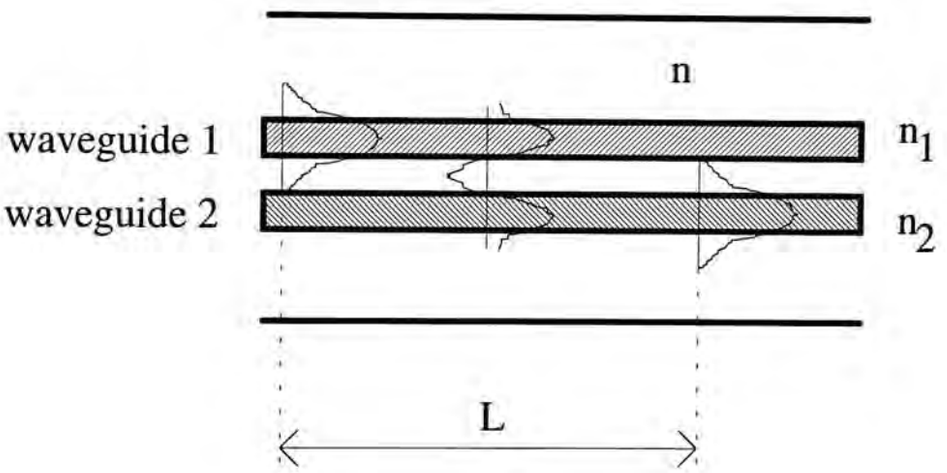


Fig. 2-7 Operating principle of the directional coupler

Fig. 2-8 depicts the operation of a simple directional coupler switch [21]. Optical input signals A and B are routed through the directional coupler switch and produce the ouputs D and E. C is the electrical control signal. But an optical implementation of C is also possible, which is also shown in the figure. When C is "1", D = A and E = B. When C is "0", D = B and E

= A. Thus the output is either in the bar state or cross state, depending on the control signal.

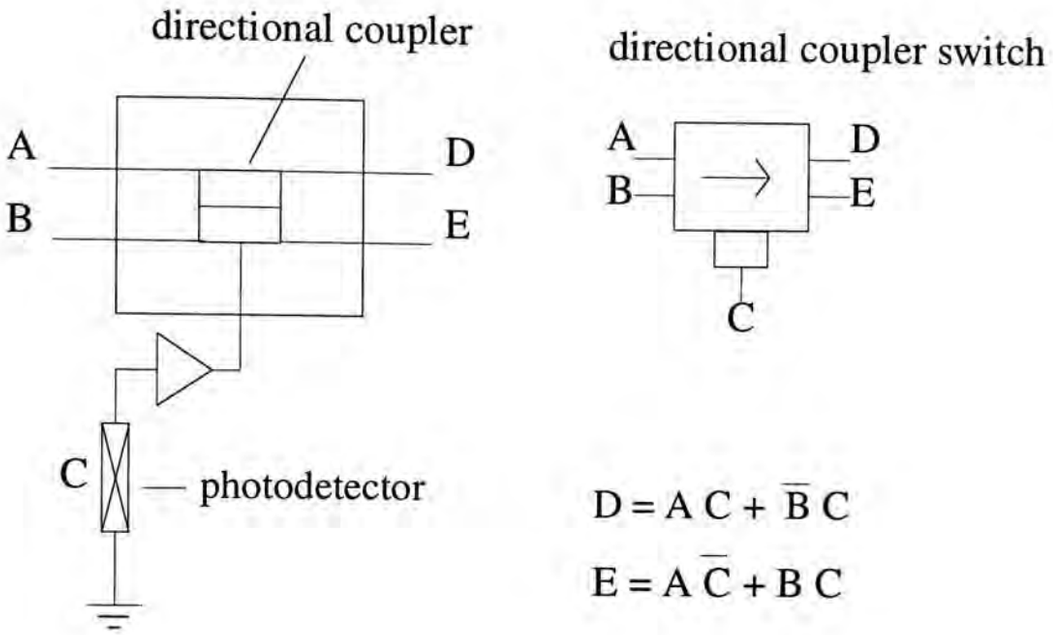


Fig. 2-8 Operation of a simple directional coupler switch

With this directional coupler switch, logic functions including AND, OR, NOT, 2-in-1-out multiplexing, 1-in-2-out demultiplexing can be implemented [22]. A 100 MHz counter has also been demonstrated [23]. Moreover, a bit-serial digital optical computer using $LiNbO_3$ directional couplers as logic elements and fiber-optic delay lines as memory elements have been proposed [22].

Recently, based on Kerr effect, nonlinear directional coupling has been investigated. Moreover, logic gates including AND, OR and XOR have been numerically demonstrated [24]. Since the switching of the signals

between the waveguides is now achieved by controlling the intensity level of the input signal, it in fact adopts an all-optical approach.

2.2.2 Self-Electrooptic Effect Devices (SEEDs)

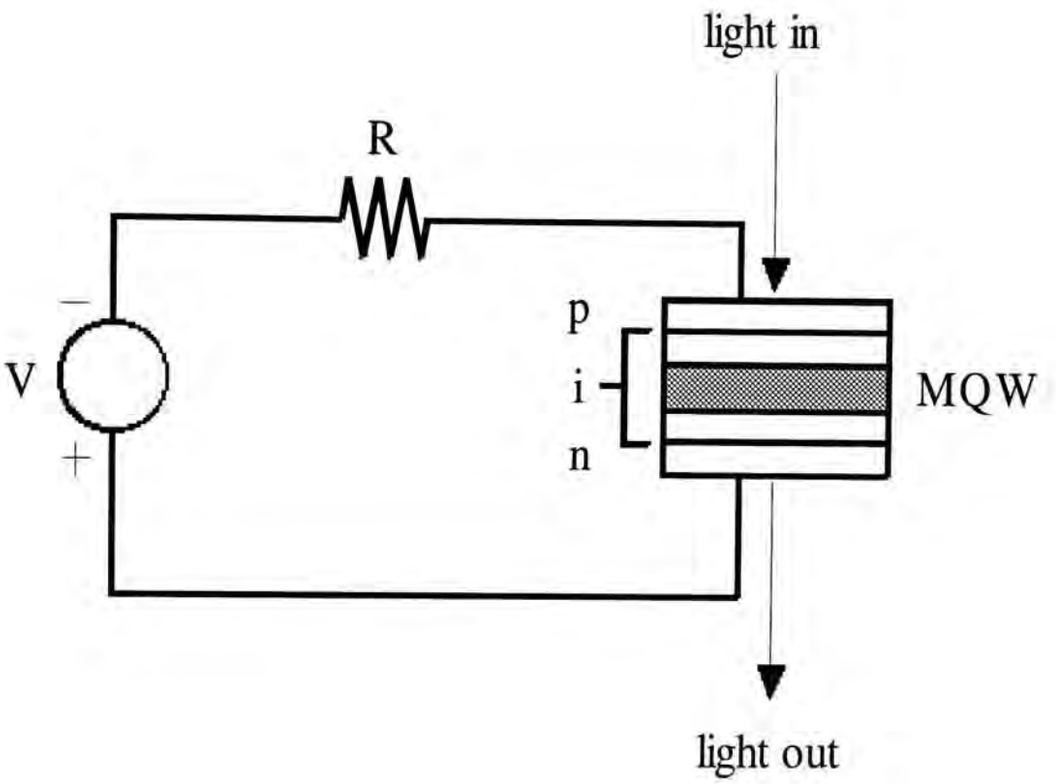


Fig 2-9 A digram showing the operation of a SEED device

The electric field-induced absorption changes in a MQW p-i-n diode are enhanced by the Quantum-Confined Stark Effect (QCSE) to produce a large change in the transmission or reflection of an external light source [25]. Devices that operate with this principle are called SEEDs. A simple SEED device is shown in Fig. 2-9. The SEED usually requires an optical bias and an external light source. It can have a time sequential optical gain which is important for its cascadability [26]. However the optical contrast

is relatively low. Optical logic functions such as AND, OR, NAND, NOR and XOR have been demonstrated [27]. A circuit demonstrating the NOR function using SEEDs is depicted in Fig. 2-10. In addition, memory devices such as S-R flip-flop, ring counters and shift registers have been built [28]. Large-scale integration has also been used in the system demonstration of a multistage interconnection network [29] and an optical digital processor consisting of four arrays of symmetric SEEDs has been demonstrated [30]. It is the most successful approach so far in building complex logic circuits. This may be a direct consequence of its low energy requirement and its high gain cascadability.

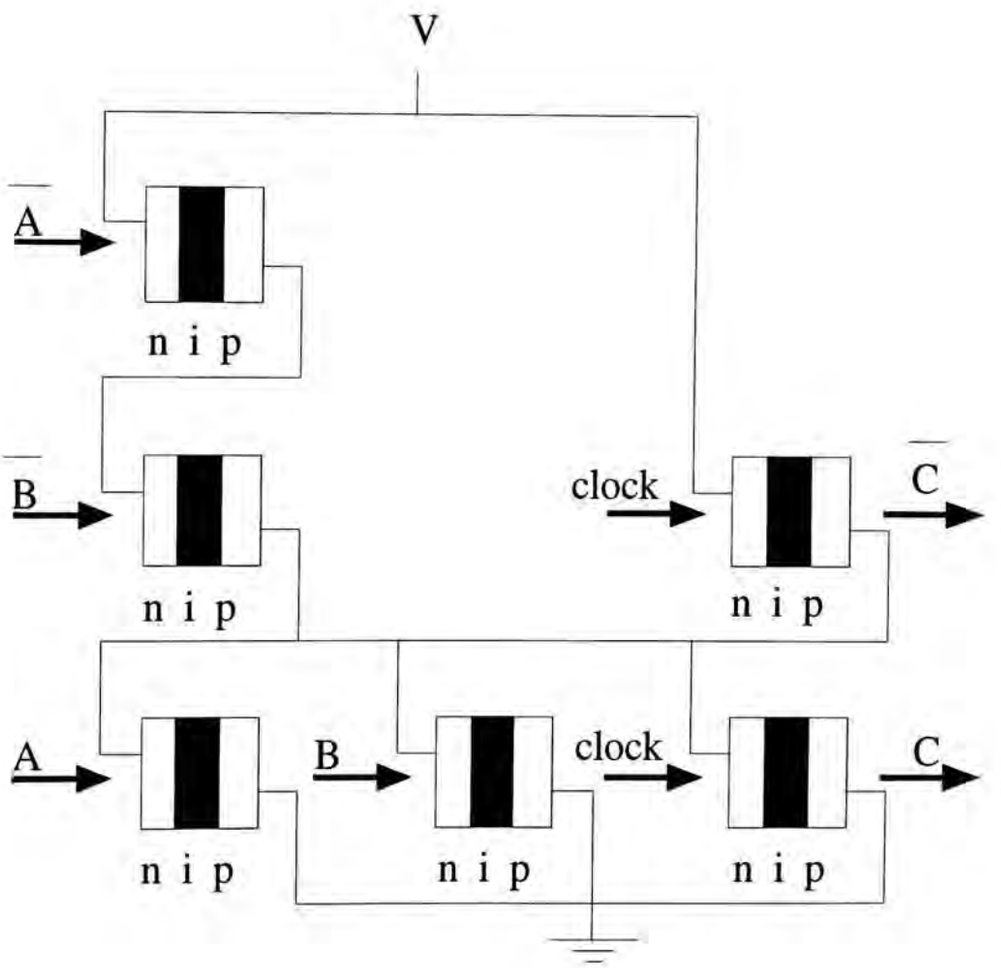


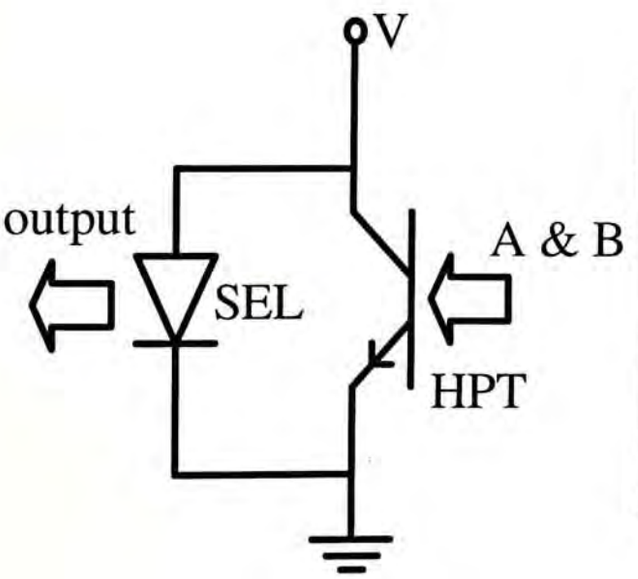
Fig. 2-10 A schematic diagram of a Logic-SEED NOR gate

While a single SEED device can operate at a fast switching speed of 33 ps [31], the demonstrated logic functions can only reach the μs range owing to the stringent requirements in fabricating fast SEEDs. Moreover, it can be seen from Fig. 2-10 that the implementation of a simple logic function NOR involves a total of six SEEDs. This means that intelligent design is required to perform the various logic functions. In addition, the operation of these devices depends upon a shift in the exciton resonance. Consequently, they require a tunable, narrow wavelength laser source or/and a strict control of active layer thickness. It is believed that their success will highly depend on the future development of material science and fabrication technology.

2.2.3 Phototransistors / Photothyristors with Light Emitting Diode (LED) / Edge-Emitting Laser (EEL) / Vertical Cavity Surface Emitting Laser (VCSEL)

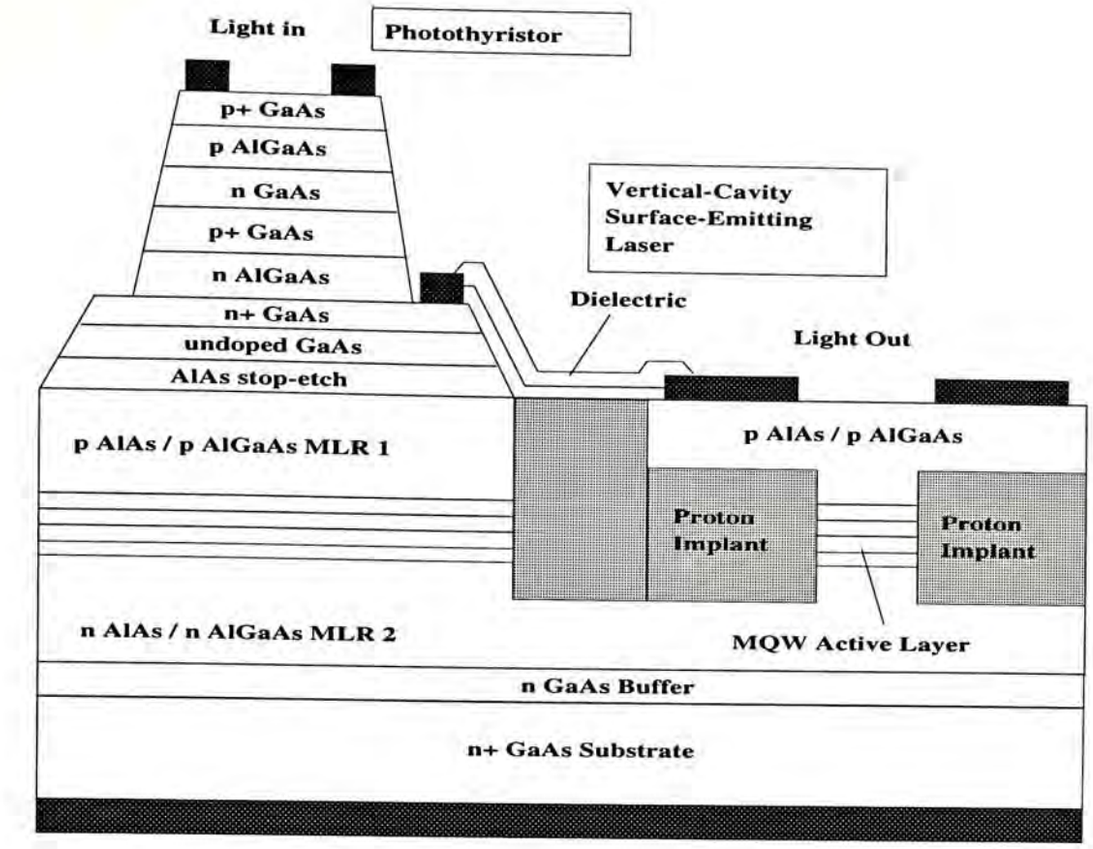
This class of devices use phototransistors [37,39] or photothyristors [42,43] for light detection and use LEDs [37], EELs [47] or VCSELs [41,42,43] to generate the optical outputs. Fig. 2-12 shows the epitaxial structure of a monolithic optical switch integrating a VCSEL with a photothyristor. Although the high gain of phototransistors or photothyristors can effect in a lower switching energy, these gain-bandwidth product governed detecting devices all suffer from the problem of large emitter junction capacitance and results in a low speed. The highest speed obtained is of tens of μs [38].

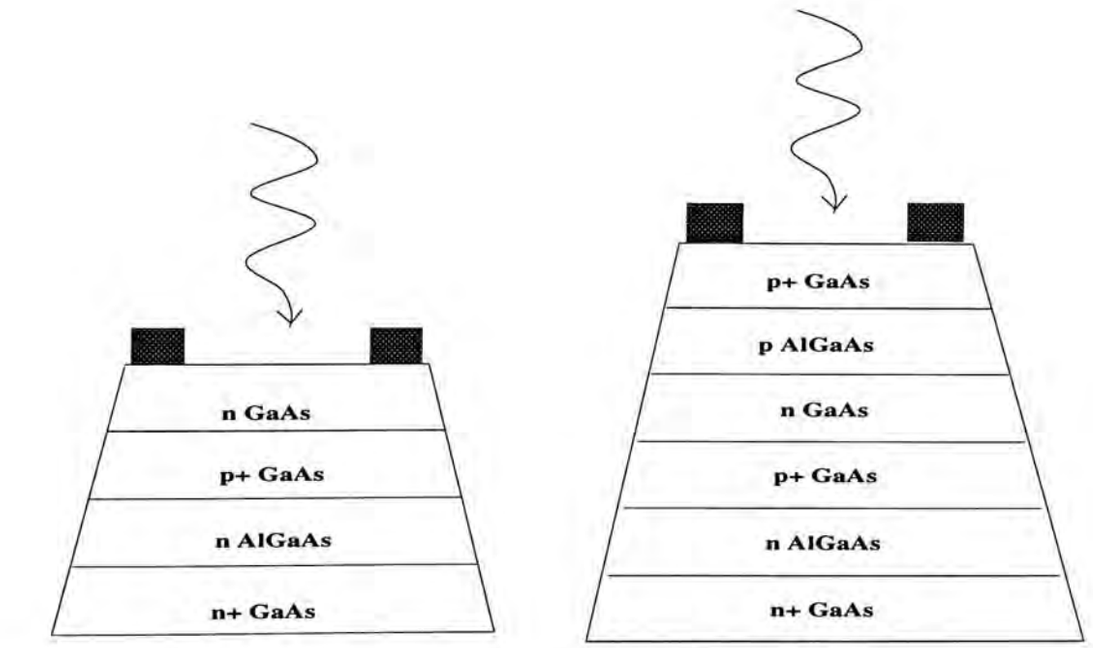
LED-based structures are power-inefficient with a high drive current, a low optical output power and a low optical gain. On the other hand, EELs are not compatible with a two-dimensional optical architecture. As a result, recent development focuses on VCSELs which performs far better in many aspects than the above two sources, such as lower drive current, lower beam divergence, the possibility of monolithic integration and suitability for two dimensional optical architectures. The logic functions demonstrated so far include AND [35,40,44], OR [40,44], NOR [33,38,45], NAND [34,45], XOR [36,37,40], NOT [32,45], simple switching nodes [48] and comparator [46]. Fig. 2-11 describes a NOR circuit and the corresponding truth table using the VCSEL logic. The use of VCSEL logic in forming two/three-dimensional arrays of smart pixels is particularly attractive in wide range of applications such as optical computing, optical interconnect, visual displays, optical memory and laser printing.



A	B	A NOR B
0	0	1
0	1	0
1	0	0
1	1	0

Fig. 2-11 A schematic diagram of the NOR circuit and the corresponding truth table





(a) Heterojunction Phototransistor

(b) Photothyristor

Fig. 2-12 Epitaxial structure of a monolithic optical switch integrating a VCSEL with a photothyristor

2.2.4 Logic Circuits with Metal-Semiconductor-Metal (MSM) Photodiodes / Photoconductive (PC) Switches

Logic devices with the highest speed are obtained with this approach. This is due to the fast response of the MSM photodiodes and the photoconductive switches. The details of these photodetectors will be discussed in **Section 3**.

With proper design of circuits incorporating these photodetectors, logic functions including AND [49], XOR [50] and an optoelectronic half-adder [51] have been demonstrated. However, the 2 pairs of photodiodes involved in the XOR device have to be isolated by a trench and this imposes additional complexity in the fabrication. On the other hand, the sum unit of the half-adder generates electrical signals of both positive and negative polarities. This means that its outputs have to be further processed before they can be useful in a cascading environment. Although this approach may not be as well-developed as SEEDs and lacks the ease of achieving two-dimensional array structure as surface-emitting laser logic, it is still very attractive in optical signal processing applications owing to its high speed operation, relative simple fabrication and possibility to integrate monolithically with other electronic or optical devices.

The logic devices investigated in this project will be focused on this approach.

2.3 Comparison of the Two Approaches in Implementing Digital Logic Devices

In all-optical approach, the characteristics of light, such as intensity, polarization and phase are of primary interests. However, these properties are not easy to modulate and thus information is difficult to be encoded or decoded by all-optical means. Although nonlinear optics seems to provide a solution, the high power required limits its usage. That explains why the present research effort is mainly on the exploration of new nonlinear material, not the implementation of systems. In addition, to lower the energy requirement, the size of the materials used should be as small as possible. Thus, a mature technology of micro-optics is also essential [52]. On the other hand, since all-optical process can involve no speed limited devices, the processing speed is definitely superior than the optoelectronic approach. Furthermore, optical signals can be in the form of two-dimensional images and process in parallel through lenses, prisms, etc. This means that the inherent parallism of optics can be better employed. While this property has already been proven successful in optical analog prosessing, its potential in digital processing are still waited to be explored.

The optoelectronic approach involves the conversions from optical signals to electrical signals and vice versa. Since these EO and OE conversions take time, the speed achieved may not be as fast as those all-optical devices. The energy efficiency would also be degraded. However, with the advanced development of semiconductor technology, Opto-Electronic Integrated Circuit (OEIC) has been realized [53]. Both p-i-n photodiode and SEEDs have been successfully integrated monolithically with Field

Effect Transistors (FET) [54,55]. As a result, this approach can combine the advantages of optics with the well-developed technology of digital electronics. Thus, it is believed that it will be promising in optical digital signal processing.

3 HIGH SPEED PHOTODETECTORS APPLIED IN OPTOELECTRONIC LOGIC DESIGN

3.1 Photoconductive Switch

3.1.1 General of the photoconductive switch

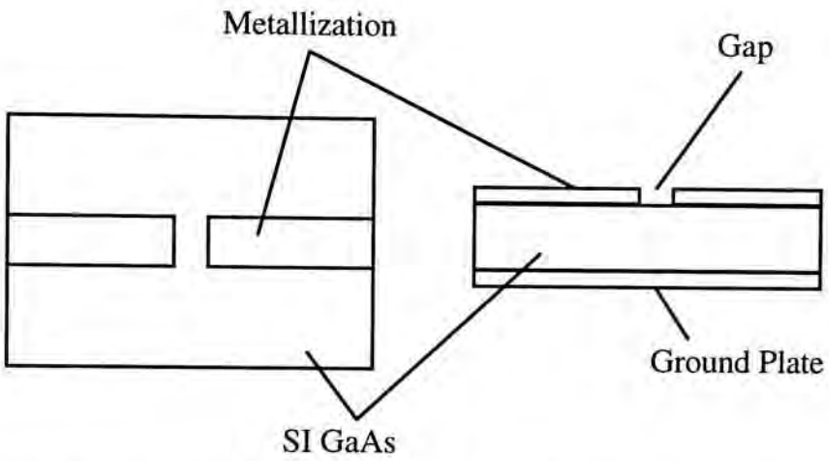


Fig. 3-1 Top and side view of a photoconductive switch fabricated on a GaAs substrate

Consider the photoconductor as shown in Fig. 3-1. When the gap is illuminated, absorption of photons takes place in the semiconductor. A photon with an energy greater than the bandgap energy of the semiconductor can cause an electron to transfer from the bound state to the free state, thus creating a free electron-hole pair. The electron-hole plasma generated connects the gap and so an electrical signal can propagate along the transmission line. The steady-state current that flows due to the photoinduced conductivity for a biased semiconductor is given by

$$I_{ph} = \eta e \frac{P}{h\nu} \frac{V}{L^2} (\mu_n \tau_n + \mu_p \tau_p) \qquad \text{Eqn. (3-1)}$$

where η is the external quantum efficiency,

P is the incident optical power,

$h\nu$ is the photon energy,

μ_n and μ_p are the electron and hole mobilities,

τ_n and τ_p are the electron and hole lifetimes,

V is the bias voltage, and

L is the gap length

This expression assumes uniform fields and ohmic contacts. From this equation, it can be seen that the magnitude of the photocurrent depends linearly on the optical input power and the bias voltage, and inversely proportional to the square of the gap length. However, in the experiment, the linearity of the photocurrent to the bias voltage is not truely observed. The reason for this discrepancy is saturation. The photo-excited carriers have reached the saturation velocity and so further increase of the bias voltage has negligible effect on the output signal.

For picosecond photoconductivity, the photoconductive gain, defined as the number of charges crossing the photoconductor per second divided by the number of photons absorbed per second, is given by [56]

t_p/τ_t for $0 < t < t_p$ Eqn. (3-2)

$(t_p/\tau_t)e^{-t/\tau_e}$ for $t > t_p$ Eqn. (3-3)

where t_p is the pulse width,

τ_e is the lifetime of free electron, and

τ_t is the transit time of the carriers, which is given by

$\tau_t = L^2/\mu V$ Eqn. (3-4)

where μ is the mobility of the carrier

The rise time of the photoconductive signal is the same as the rise time of the optical pulse, and from Eqn. (3-3), the fall time depends on the carrier

lifetime. To maximize the gain, from Eqns. (3-2) and (3-3), the transit time τ_t has to be small. Hence, from Eqn. (3-4), a switch with a small gap should be used. However, the bias voltage must not be too high for small gap switch owing to the problem of breakdown. In fact, to hold off voltage, the material should process a high dark resistivity and a high intrinsic breakdown field.

The width of the electrical pulse generated depends on the duration of the optical pulse used to create free carriers, the carrier lifetime of the photoconductive material, and the intrinsic bandwidth of the transmission line into which the photoconductive material is integrated. To obtain fast switching time, amorphous, polycrystalline, and radiation-damaged semiconductor have been used. They have high defect density and therefore reducing the carrier capture time into picosecond domain. However, these materials have low mobility, making it inadequate for generating electrical pulses of reasonable voltage levels.

The output voltage V_o is given by [56] :

$$V_o = V Z_o / (2Z_o + R) \qquad \text{Eqn. (3-5)}$$

where Z_o is the characteristic impedance of the line, and

R is the resistance of the gap which can be expressed as [56]

$$R = L^2 / Ne\mu \qquad \text{Eqn. (3-6)}$$

where N is the total number of photoinduced charged carriers which is proportional to the optical energy of the pulse.

To ensure a large linear dynamic range, we see from Eqn. (3-5) that R should be much larger than $2Z_o$. It is not difficult to achieve as Z_o is always chosen to be 50 Ω.

3.1.2 Advantages of the photoconductive switch [56]

1. It allows jitter free switching.
2. It has ultrafast rise time, usually the rise time of the optical pulse.
3. It also has ultrafast fall time when materials with picosecond carrier lifetimes are used.
4. It possesses large dynamic range.
5. It can be integrated monolithically with microelectronic devices.

3.1.3 Disadvantages of the photoconductive switch :

1. From Eqns. (3-2) and (3-3), a large carrier lifetime is desirable for a large gain. However, it would lower the speed of the detector. Thus, the gain and bandwidth are physically linked and cannot be optimized at the same time. For our application, a large bandwidth is obtained at the expense of a lower gain.
2. The dark current results from random motions of carriers in the dark can decrease the signal-to-noise ratio. The magnitude of the noise is larger in photoconductive switch when compared with other photodetectors owing to the presence of ohmic contacts. The magnitude of the noise is directly proportional to temperature and dark conductance. Thus, low-temperature operation with lighter doping is desirable.

3.1.4 Applications of the photoconductive switch :

1. On-wafer time-domain characterization of ultrafast devices.
2. Millimeter-wave generation and detection [56].

3.2 Metal-Semiconductor-Metal (MSM) Photodiode

3.2.1 General of MSM photodiode

A MSM photodiode is formed when a layer of metal is deposited onto semiconductor to produce two Schottky contacts with a gap separating them. For most cases, this Schottky contact structure is highly symmetric and consists of interdigitated metal fingers. The schematic diagram of a simple MSM photodetector is shown in Fig. 3-2. It detects photons by collecting electrical signals generated by photo-excited electron-hole pairs in the depleted semiconductor gap that drift under the electric field applied between the two metallic electrodes.

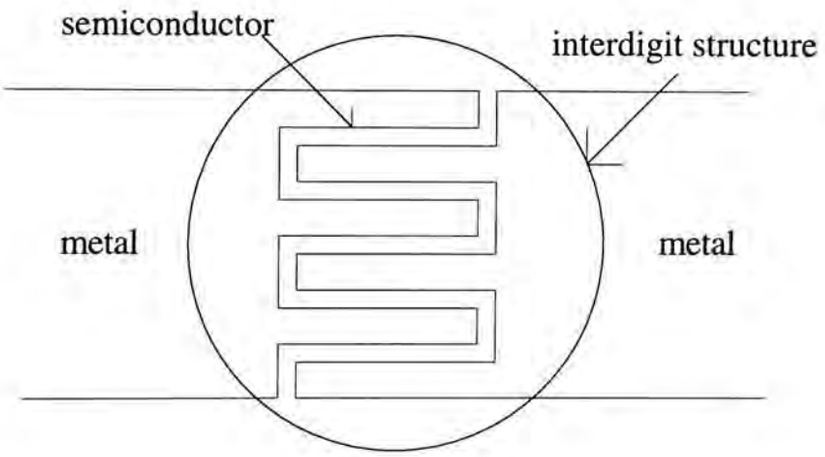


Fig. 3-2 A schematic diagram showing a MSM photodetector with interdigitated fingers

Before a carrier is emitted into the metal over the Schottky barrier, it has to pass through the depletion region in the semiconductor. The carrier motion within the depletion region is governed by the drift and diffusion processes, while its emission into the metal is determined by the density of

available states in the metal. The two processes are essentially in series, and the one that causes the larger impediment to the carrier flow determines the current. In high mobility semiconductors like GaAs, the current is limited by thermionic emission over the barrier [57]. Thus the mechanism of GaAs MSM photodetector can be understood with the thermionic emission theory [58].

The response of MSM photodetector is limited by carrier transit time and RC charging times of external circuit. The capacitance of a lithographically defined interdigitated electrode structure with an active area of 10 x 10 μm^2 amounts to 1 to 8 fF depending on the finger separation and width. Thus the RC-charging time for such a detector with a 50 Ω load is less than 400 fs. The response of device with similar area is then dominated by carrier transit times which can be minimized by choice of a small distance between the Schottky contacts. Such a geometry permits rapid carrier collection after photoexcitation [59].

Although the use of interdigital electrode structures can decrease the transit time and offer lower on-state resistance, the responsivity is reduced owing to the metal finger shadowing. Since the MSM photodetectors used in this research is not interdigitated, the influences of finger spacing and finger width to device response will not be considered.

3.2.2 Advantages of MSM photodetectors :

1. Faster response than photoconductors because of internal field and reduced capacitance.

2. Because of the planar structure, fabrication is relatively easy. Moreover, it is highly compatible with large-scale planar integrated circuit technology. Thus, monolithic integration and the use of standard GaAs FET process is possible.

3. Small dark current (< 10 nA) owing to the presence of the potential barrier. From Eqn. (3-7), this diminishing current noise can result in a higher bandwidth for the same minimum detectable power [60].

$$q\eta P_{min}/h\nu = \sqrt{2qI_dB} \qquad \text{Eqn. (3-7)}$$

where η is the quantum efficiency,

P_{min} is the minimum detectable power,

I_d is the dark current, and

B is the bandwidth.

4. Symmetrical Schottky contact structure allows a bias application in either polarity [60].

3.2.3 Disadvantages of MSM photodetectors

1. A larger contact resistance may limit the dynamic range.

3.2.4 Applications

1. As receiver in multi-gigabit optical communication systems.
2. High speed sampling.
3. Optical control of monolithic microwave integrated circuits.
4. High speed chip-to-chip connection.

3.3 Design of Simple Logic Gates with Photodetectors

3.3.1 Boolean function AND

Truth table of logic function AND :

A	B	A • B
0	0	0
0	1	0
1	0	0
1	1	1

Table 3-1 Truth table of AND

Design of the optoelectronic AND gate :

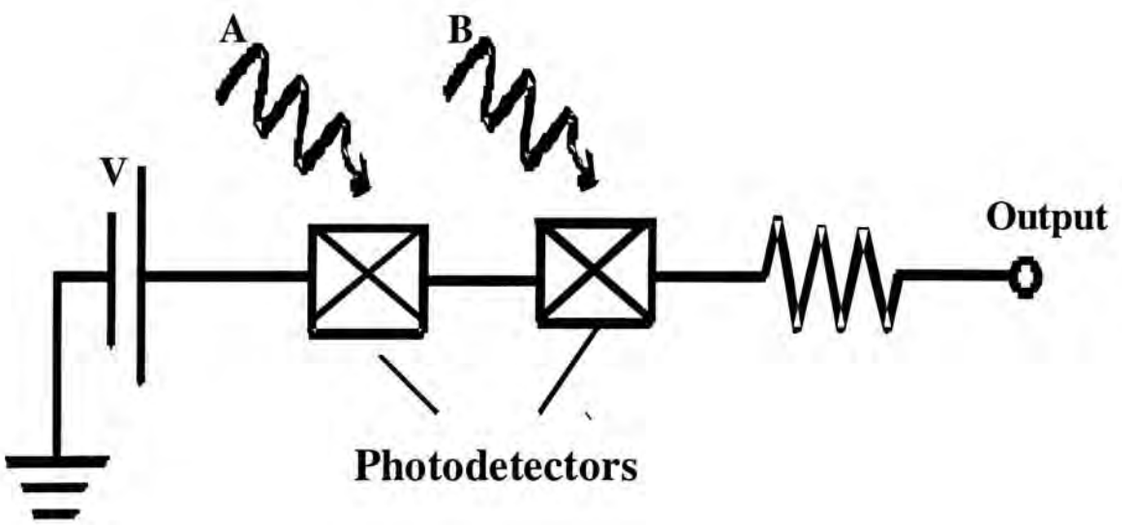


Fig. 3-3 Circuit design of logic function AND

Discussion :

1. The output signal for this circuit is small. It is because the two photodetectors are connected in series. The second switch is only biased at the output voltage of the first switch, which is smaller than the bias voltage of the first switch.

2. A suitable time delay has to be maintained between the two input beams for the proper functioning of the gate. This time delay should be equal to the propagating time needed by the photo-carriers generated from the first switch to travel to the second switch. Consequently, this time delay can be made negligibly small if the distance between the photodetectors is minimized.

3.3.2 Boolean function NOR :

Truth table of logic function NOR :

A	B	$\overline{A+B}$
0	0	1
0	1	0
1	0	0
1	1	0

Table 3-2 Truth table of NOR

Design of the optoelectronic NOR gate :

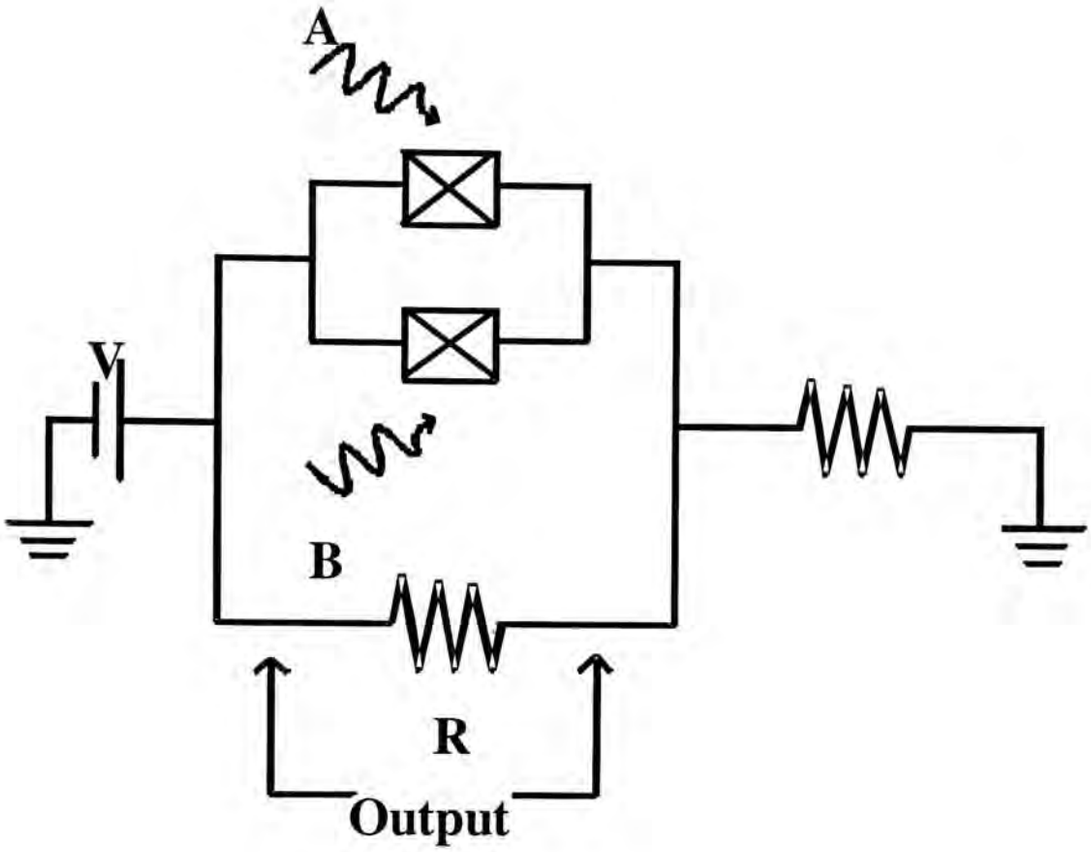


Fig. 3-4 Circuit design of logic function NOR

Discussion :

1. Output is taken as the potential difference across resistor R.
2. To obtain a good on-off contrast ratio, the resistance of R should be much smaller than the dark resistance of the parallel photodetectors and much larger than their illuminated resistance. As discussed in **Section 4**, the dark resistance of the photodetectors is in the order of tens of mega-ohms. And the illuminated resistance is in the order of hundreds of kilo-ohms. Consequently, R may take a value of a few mega-ohms.

3.3.3 Boolean function NAND

Truth table of logic function NAND :

A	B	$\overline{A \bullet B}$
0	0	1
0	1	1
1	0	1
1	1	0

Table 3-3 Truth table of NAND

Design of an optoelectronic NAND gate :

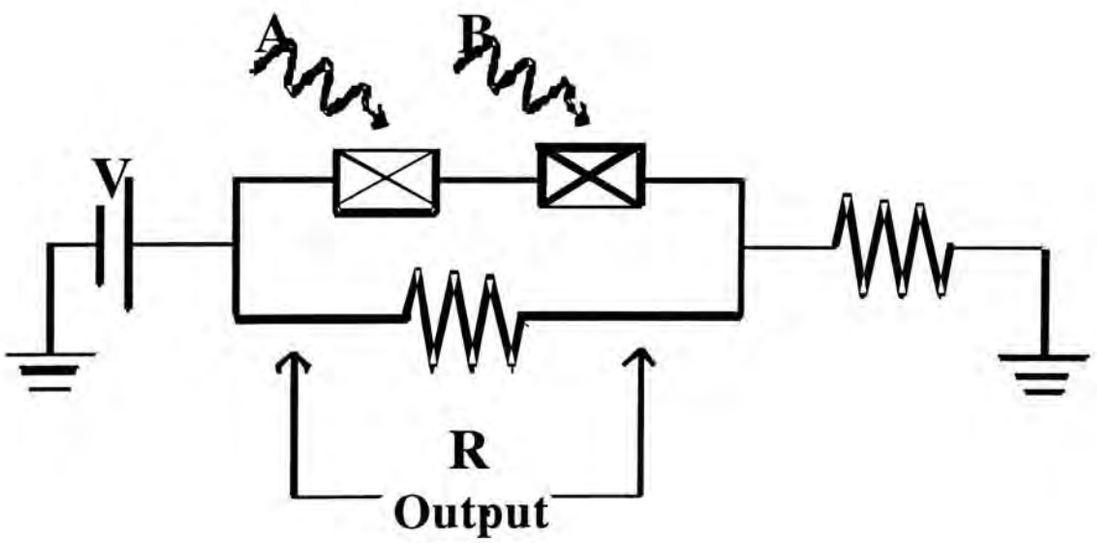


Fig. 3-5 Circuit design of logic function NAND

3.3.4 Boolean function NOT

Truth table of logic function NOT :

A	$\overline{A}$
0	1
1	0

Table 3-4 Truth table of NOT

Design of an optoelectronic NOT gate :

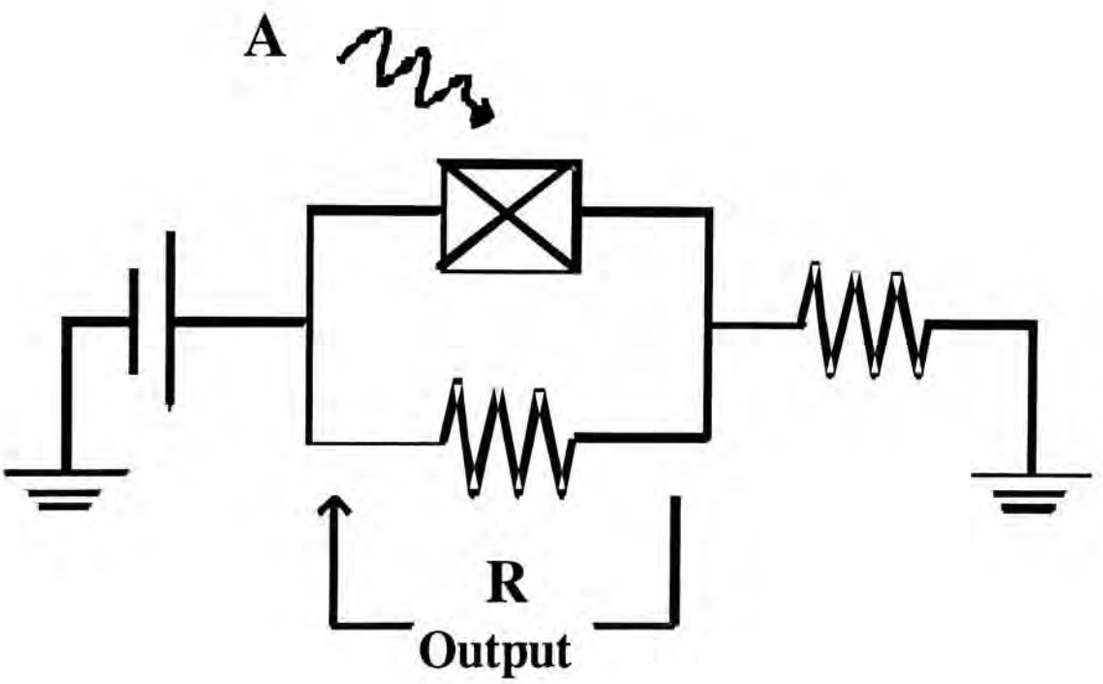


Fig. 3-6 Circuit design of logic function NOT

4 DEVICE FABRICATION AND CHARACTERIZATION

4.1 Design of the Basic Structure

4.1.1 Schematic layout of the basic structure

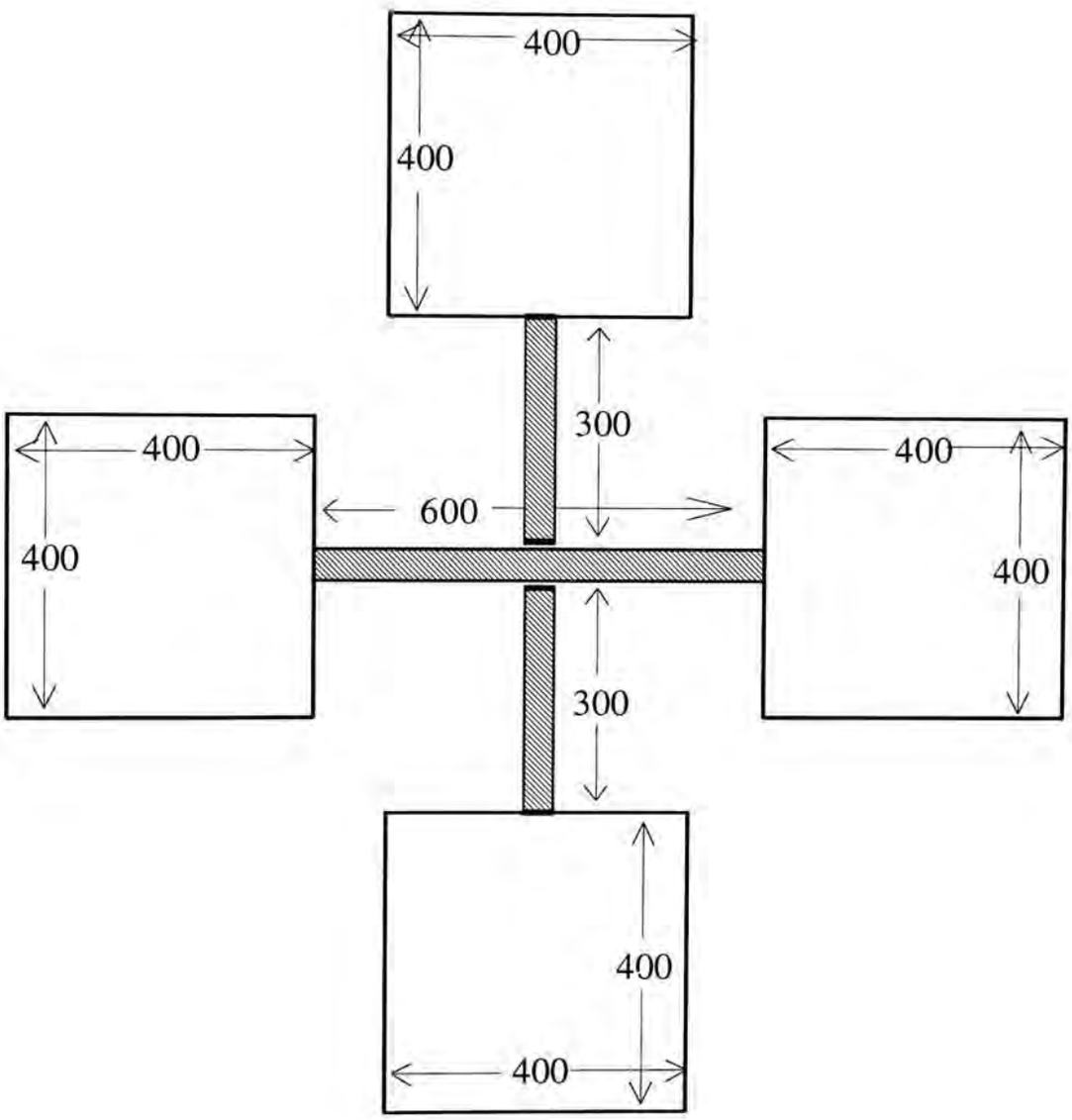


Fig. 4-1 Schematic diagram of the basic structure

The schematic diagram of the basic structure for the logic devices is shown in Fig. 4-1. The central hatch portions are the metallic transmission lines. The linewidth is 40 μm. The two vertical lines form two gaps with the horizontal lines with a gap length of 10 μm. The two gaps will be the active area of the devices. The four squares adhering to the transmission lines are the ground planes which will be the ports for external electrical connections. The whole structure will be fabricated as a single layer of metal depositing on a semiconductor substrate.

4.1.2 Origin of the basic structure

Similar structure is originally used in making electronic autocorrelation measurements of the electrical signals produced by picosecond photoconductors [61]. The essential feature of the electronic autocorrelation technique is to use one photoconductor as a pulse generator and the other as a sampling gate. A variable delay is introduced by varying the relative timing of the optical pulses absorbed at each photoconductor. The average output signal as a function of relative time delay is measured to obtain an autocorrelation trace which can be used to investigate the response of the photoconductive switches or estimate the FWHM of the input optical pulse.

4.1.3 Design Considerations

Gap length :

As discussed in **Section 3**, the photoresponse increases inversely with the square of the gap length for a photoconductive switch. Thus, a smaller gap

length is favoured for a larger output signals. Moreover, a smaller transit time can be achieved to get a faster response for the MSM photodiodes. On the other hand, the active area would decrease with a shorter gap length. This means that a tighter alignment will be required. Also, the capacitance of the gap would increase and results in a larger RC time constant. In addition, it is easier to get breakdown as the electric field across the gap increases for the same bias voltage. Owing to the limitation of fabrication resolution, a gap length of 10 μm is chosen.

Linewidth :

This parameter is less critical to the performance of the device. Smaller linewidth may result in a smaller dark current. Moreover, the capacitance of the gap increases with the linewidth. On the other hand, a larger linewidth means a larger active area, and so a larger photoresponse. But as fast response is the main concern in this research, the linewidth is minimized in the design. The dimension used is limited by mask-making.

It should be noted that the two gaps are separated only by the linewidth of the horizontal transmission line. Thus, in order to prevent both gaps being illuminated by a single beam unexpectedly, the width of this line cannot be too short. But in our case, the limitation set out by mask-making already overrides this consideration.

Line length :

The length of the transmission should not be long as it will introduce unnecessary time delay, dispersion, and loss of the electrical signals propagating on it. In addition, a longer transmission line also means a

larger device, which is not desirable in terms of cost and reliability. However, a minimum length has to be ensured to minimize the reflection of signals at the interface of the transmission lines and the ground planes.

Size of ground planes :

Since wire-bonder is not available at the time of design, the size of these ground planes are made large enough for the application of silver paste for external electrical connections. Otherwise, an area of 150 μm x 150 μm will be sufficient for 2 mil bonding wire. As the ground planes contribute most of the area of the structure, their reduction in size can save material and increase the yield.

Symmetric shape :

The symmetric shape provides a large flexibility in using the structure. Once a gap is illuminated, the input beam can be easily adjusted to illuminate another gap. Thus, the performance of the structure can be verified quickly. In addition, both gaps are terminated by the main horizontal transmission line and reflections are minimized. On the other hand, as some of the logic operations involve the cancellation of pulses generated from the two gaps, a highly symmetrical structure is preferred for a more complete cancellation.

4.2 Fabrication

4.2.1 Semi-Insulating Gallium Arsenide (SI-GaAs) substrate wafer

GaAs is used extensively in optoelectronics despite the availability of the well-developed silicon technology. It is because GaAs is a direct bandgap material and thus has a much better quantum efficiency than the indirect bandgap Si. In addition, in developing high speed devices, GaAs has a definite advantage over Si owing to its higher electron mobility. However, GaAs also has its limitations. It is fragile and more efforts have to be paid to obtain surface passivation when compared with Si. Moreover, its cost is much higher.

For compensation of the unintentionally doped shallow donors Si contributed from the crucible material during the growth process, deep acceptors are doped near bandgap middle and forms the SI-GaAs. This material has an additional advantage of larger dark resistance. However, it is difficult to contact with low-resistance non-rectifying contacts.

Properties of SI-GaAs are given in **Appendix II**.

4.2.2 Fabrication procedure

1. Clean the semi-insulating undoped GaAs wafer with TCE (1,1,1-Trichloroethane).
2. Clean the wafer with acetone by ultrasonic for five minutes.

3. Repeat the above step with IPA (iso-propyl-alcohol).
4. Clean the wafer with deionized water.
5. Dry the wafer with oxygen blower for about three minutes.
6. Place the wafer in an oven for five minutes at 80°C.
7. Apply photoresist (AZ 1450J) on the wafer by a spinning machine at 4000 rpm for 45 seconds.
8. Prebake the wafer by putting it in an oven for thirty minutes at 80°C to stabilize the photoresist.
9. Allow the wafer to cool down for a few minutes.
10. Place the mask on the wafer using a maskaligner.
11. Expose the wafer with mask under ultra-violet light for thirty seconds.
12. Use chlorobenzene to stabilize the photoresist for five minutes.
13. Blow away the chlorobenzene staying on the devices by a suction pump. No chlorobenzene should stay on the devices before developing.
14. Develop with AZ 351 (1:5 H_2O) for one minute.
15. Rinse the wafer with deionized water and dry it.
16. Post-bake the wafer by putting it in an oven for twenty minutes at 80°C to stabilize the photoresist.
17. Place the metallization on the devices by thermal evaporation.
18. Lift-off the unwanted metallization by putting the wafer in acetone using ultrasonic until the pattern is clearly seen.
19. Immerse the wafer in IPA to remove the acetone.
20. Clean the wafer with deionized water and dry it.

4.2.3 Metallization

Gold-germanium eutectic (88% Au , 12% Ge) is used in fabricating photoconductive switches. Its melting point is about 360 °C . Nickel is added to inhibit the balling up of AuGe owing to the difference of their lattice constants. Subsequently thermal anneal is applied to form alloyed ohmic contact. The thickness of the transmission lines is 0.16 μm.

Both aluminium and gold have been deposited onto SI-GaAs substrate to form Schottky barrier MSM photodetectors. The thickness of the metal layer is 0.2 μm. For these metals, rectifying contacts are formed due to the barrier potential between the metals and the semiconductor (0.9 eV for Au and 0.8 eV for Al). Au is used in most cases because Al suffers from the problem of electromigration which greatly reduces the reliability and lifetimes of the devices [62].

4.3 Mounting of Device

4.3.1 Mounting procedure

1. The processed semiconductor wafer is diced into separate pieces with the help of a pair of forceps and scriber, each piece containing one device.
2. Each device is fixed onto a processed circuit board with some thermal paste.
3. Then silver paste is used to make electrical connections between the device and the transmission lines on the circuit board.

4. When the silver paste has been dried, the conductivity between the device and the circuit board is verified. Up to this step, the device has been mounted on a circuit board such that it can be handled easier and safer.

5. To provide a convenient means to test the devices, a microwave circuit testbox is used to facilitate the external electrical connections of the circuit board. The testbox is a brass mount supplied with adjustable connector/mounting plate assemblies and SMA-RIM microstrip launchers as shown in Fig. 4-2. The connector contacts provide the external contacts of the board circuitry. The area of the testbox is 15 mm x 22 mm.

6. A schematic diagram of the whole testbox is shown in Fig. 4-3. It is then fastened onto a three-dimensional precision stage to facilitate subsequent alignment.

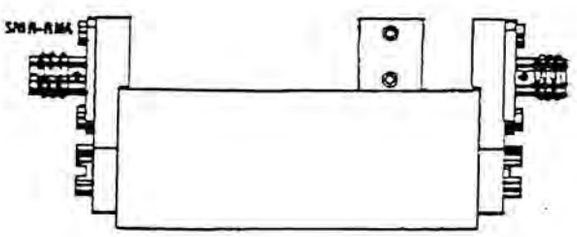


Fig. 4-2 Microwave circuit testbox

4.3.2 Circuit board pattern description

The layout and dimensions are shown in Fig. 4-4. The hatch regions are the transmission lines for external connections. It can be noted that they are

present only on the top and bottom sides of the board. They are absent on the two vertical sides of the board to reserve space for the focusing objectives which have a working distance of only 11 mm. This space is critical in the case where two beams are focused onto the device. Four transmission lines are present on the board. For our purpose, three are sufficient. Two are for connections of positive and negative bias voltages and another is for output. The remaining one can be viewed as a spare unit.

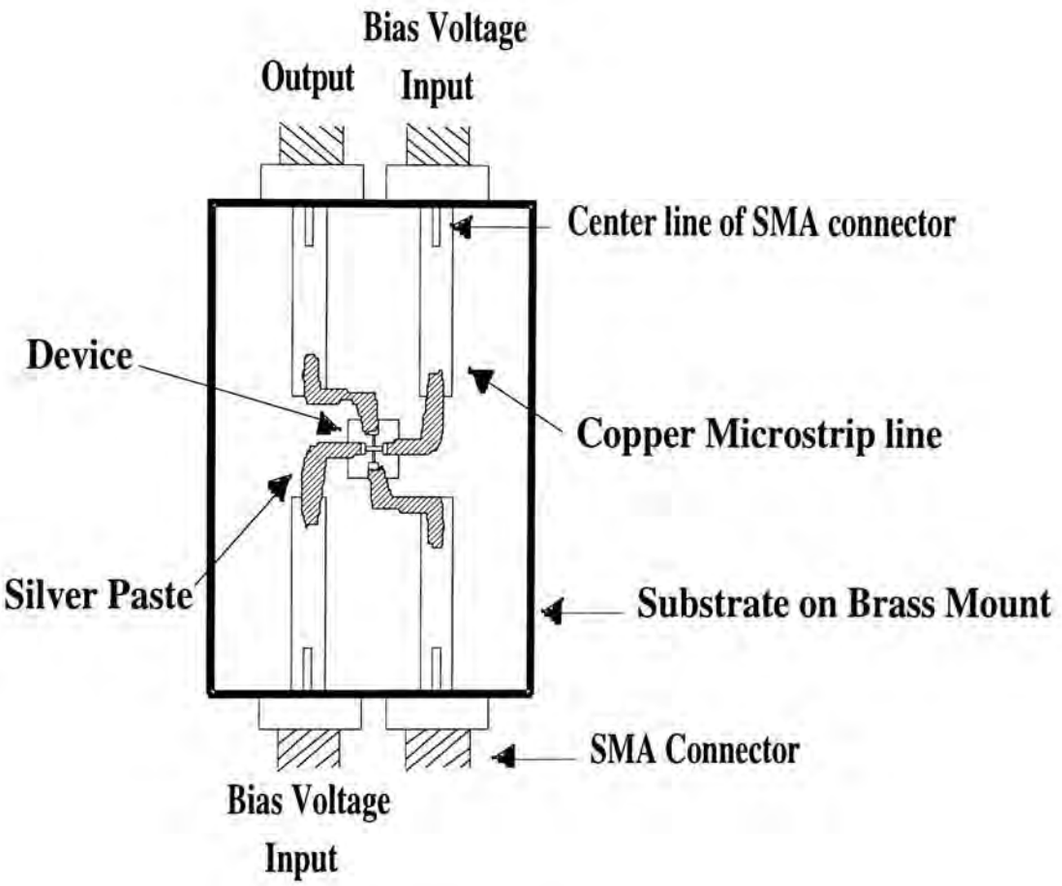


Fig. 4-3 A schematic layout of the whole testbox

4.3.3 Steps of circuit board preparation

1. Transfer the pattern required onto a red membrane with the help of a cutter.

2. Use the red membrane as the mask and carry out the *photoresist processing steps* to transfer the pattern onto a plain circuit board.

3. Cut the processed board into the size needed to be mounted onto the brass mount and make sure that the transmission lines terminating at the edges of the board make no contact with the brass.

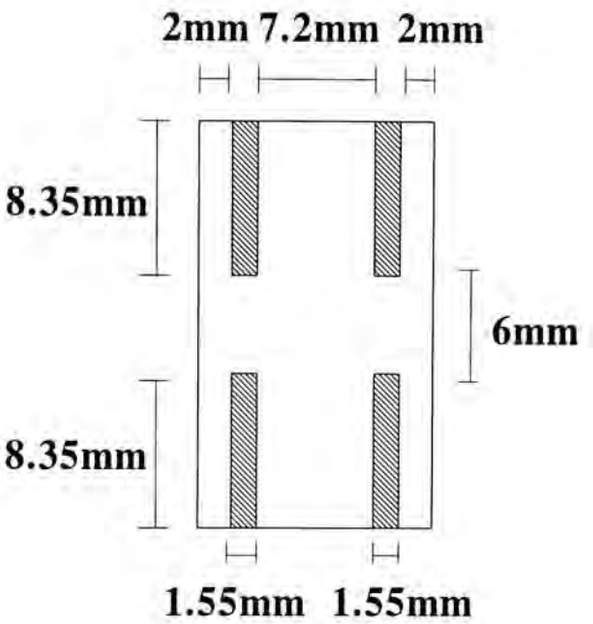


Fig. 4-4 Schematic layout of the circuit board

Photoresist processing steps :

1. Coating with Photoresist

   Apply viscous positive photoresist (AZ1450J) to previously cleaned and dry board. Both the thickness and smoothness of this layer of photoresist are important in obtaining a good etching. It should be thin and even. This may be achieved with the help of a spinner.

2. Prebaking

   Bake for 20 minutes at 80 ^{o}C.

3. Mask Alignment

Since the resolution and the position are not critical, the mask is put over the circuit board by hand.

4. Exposure to ultraviolet

First of all, the board with the mask is pressed by a glass plate to get a flat surface. At the same time, two mercury lamps are switched on for three minutes to allow them to reach steady state. After that, the board is exposed under the lamps for ten minutes.

5. Developing

The board is rinsed in an appropriate developer until the pattern comes out. For our case, sodium hydroxide (NaOH) solution is used. This dissolves the exposed positive photoresist but does not affect the exposed regions. Then the board is washed and dried.

6. Postbaking

Bake for 20 minutes at 100 ^{o}C to toughen the remaining photoresist.

7. Etching

Iron(III) chloride solution ($FeCl_3$) is used to etch away those parts of the board where the photoresist has been dissolved. This process takes five to ten minutes, depending on the concentration and temperature of the solution.

8. Stripping

Finally, the remaining photoresist is removed with acetone and the circuit board is cleaned with deionized water.

4.3.4 Specifications of the circuit board

Dielectric substrate material	:	RT-Duroid 6002 microwave laminate
Dielectric constant	:	2.94 ± 0.04
Dielectric thickness	:	25 mil

Conducting material	:	copper on both side
Bandwidth	:	up to and beyond 20 GHz

4.3.5 Transmission Line Structure

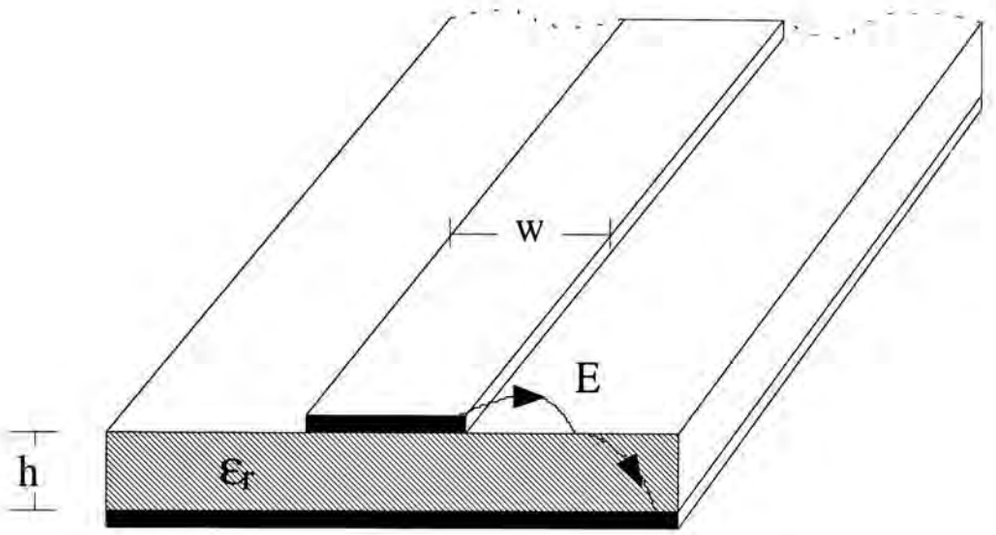


Fig. 4-5 Configuration of a microstrip line

Fig. 4-5 shows the microstrip line that is used as the transmission line structure for the circuit board. It is used because it has a very simple geometric structure that can be fabricated easily by photolithography techniques and the mode of propagation is almost TEM. In addition, it has a good range of characteristic impedance from 20 to 125 Ω, determining by w, h and ε_r [63]. The microstrip line structure is designed to have a 50 Ω characteristic impedance such that the pulse can be launched to a standard SMA connector with minimum reflection and pulse broadening. The design is carried out with HP 85150B Microwave Design System (MDS) running on the DEC workstation. From simulation, the parameters for the

circuit board are : w = 1.55 mm, h = 0.625 mm and ε_r.= 2.94. When these values are verified with Wheeler's method [63] using Fig. 4-6, the characteristic impedance is around 38 Ω. This reflects that the dimensions obtained are acceptable.

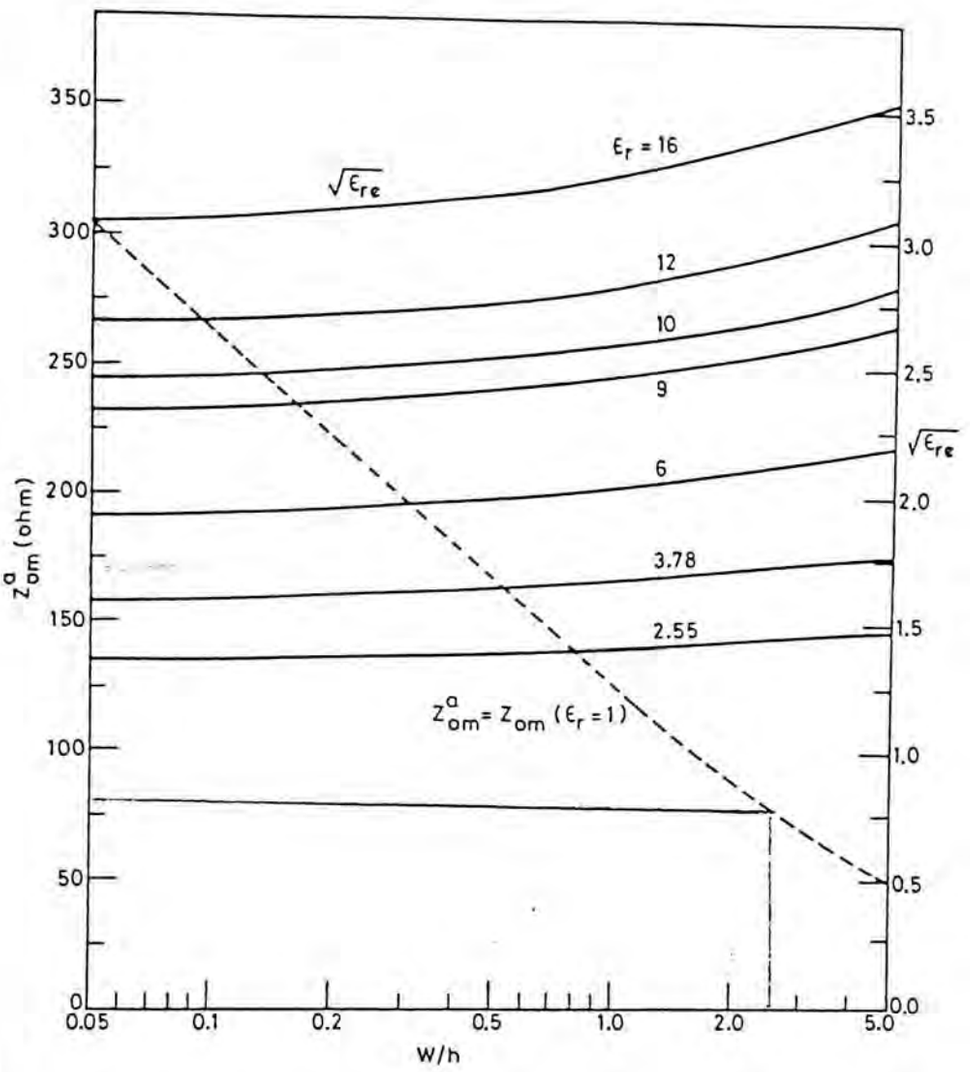


Fig. 4-6 Characteristics impedance for different dimensions of microstrip line

4.4 Characterization

4.4.1 Single gap response of the basic structure

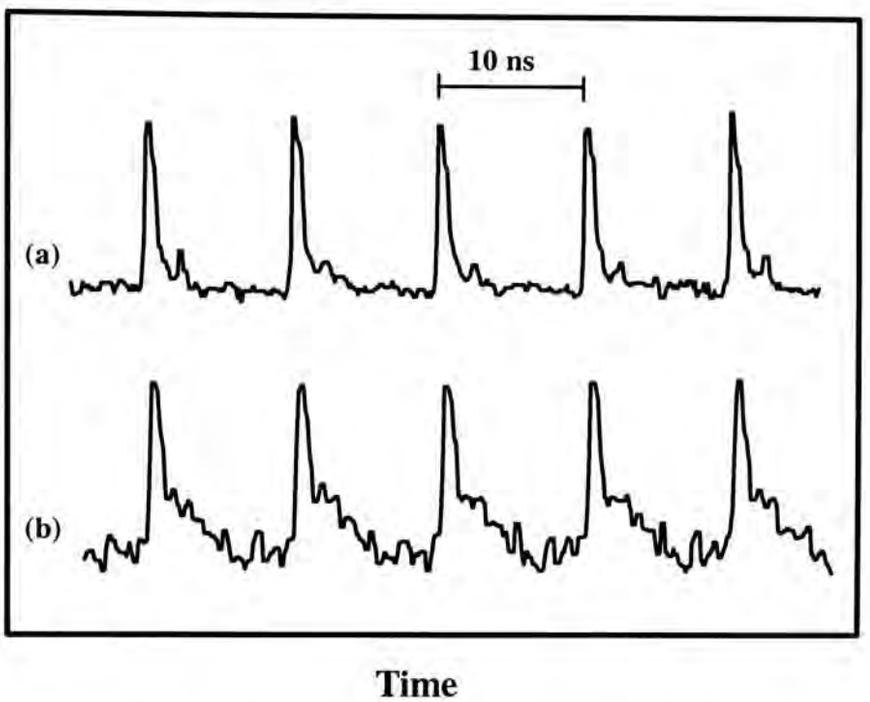


Fig. 4-7 Gap response of the basic structure

Single gap response of the structure is depicted in Fig. 4-7. The metallization is achieved by depositing 0.2 μm of gold onto the SI GaAs substrate. Profile (a) shows an input pulse train at 0.83 μm with a repetition rate of 100 MHz. The pulse width is 250 ps as measured by the New Focus photodetector. This input source is prepared by driving an AlGaAs/GaAs MQW laser diode at 19 mA dc bias with an 8 dBm ac signal. Profile (b) displays the electrical output when the beam is focused onto one of the two identical MSM photodetectors. The pulse width increases to 690 ps. The device response is limited by parasitics arising from the mounting fixture for external electrical connections.

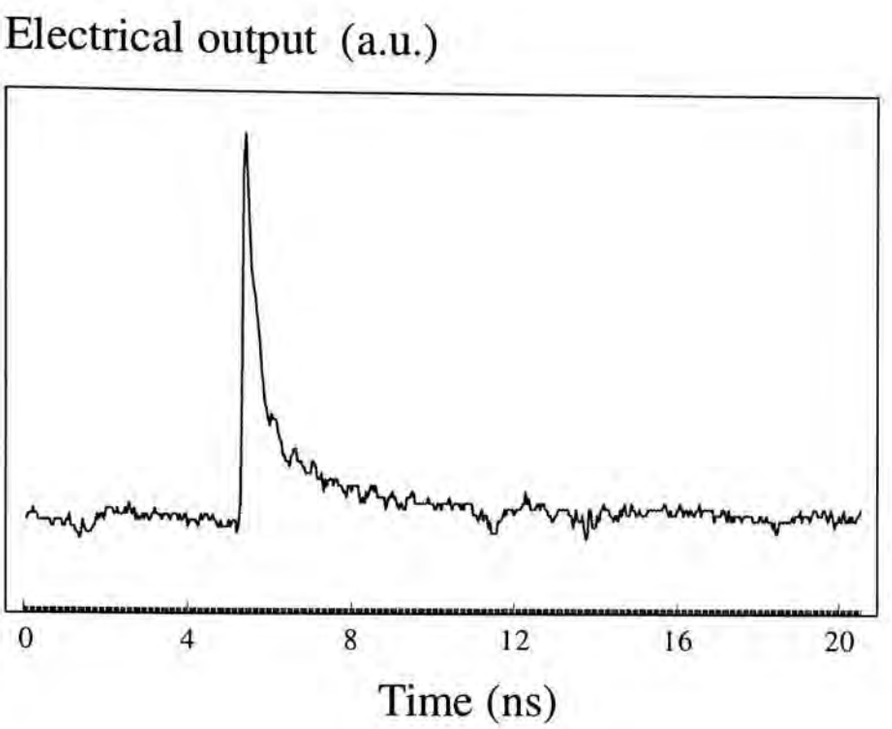


Fig. 4-8 Gap response of the basic structure with positive bias voltage

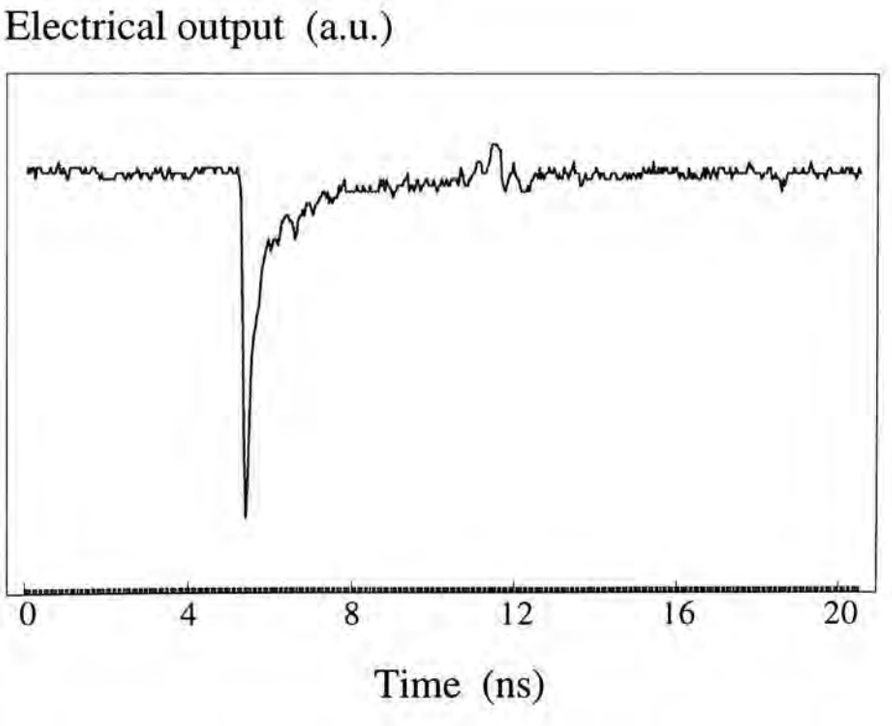


Fig. 4-9 Gap response of the basic structure with negative bias voltage

Fig. 4-8 and Fig. 4-9 show the single gap responses of the basic structure with bias voltages of different sign. The input optical beam is provided by the PPL50M module diode laser. The measured average power of the input pulse is 75 μW. The bias voltages are ± 20 V. The output pulse has a FWHM of 250 ps and a peak amplitude of 22 mV for both bias voltages.

It can be observed from Fig. 4-10 and Fig. 4-11 that the peak amplitude of the output pulse increase linearly with the power of the beam for the range concerned, regardless of the sign of the bias voltage. This desirable feature will be useful in the realization of the logic functions.

For positive bias voltage

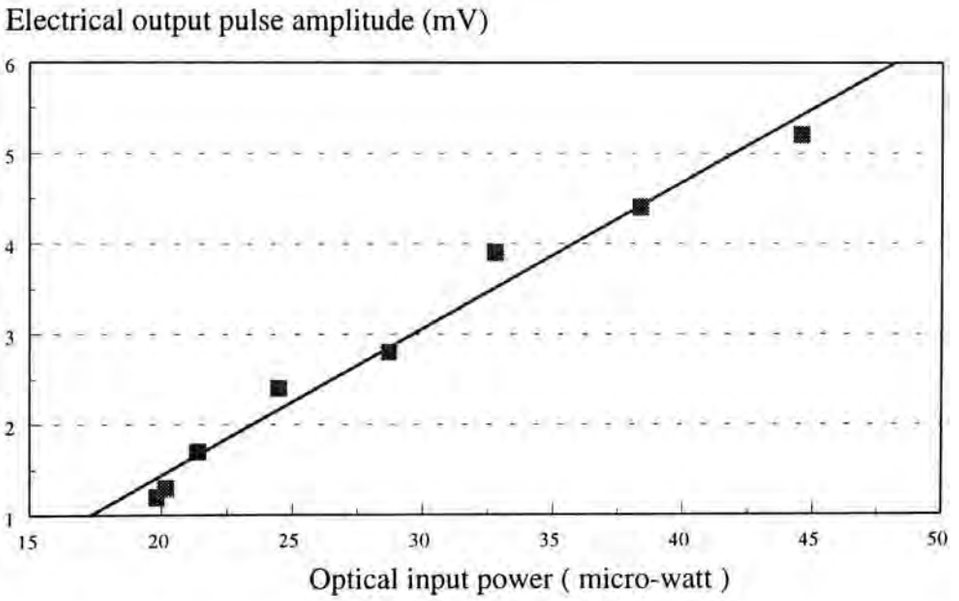


Fig. 4-10 Electrical output pulse amplitude against optical input power with positive bias voltage

For negative bias voltage

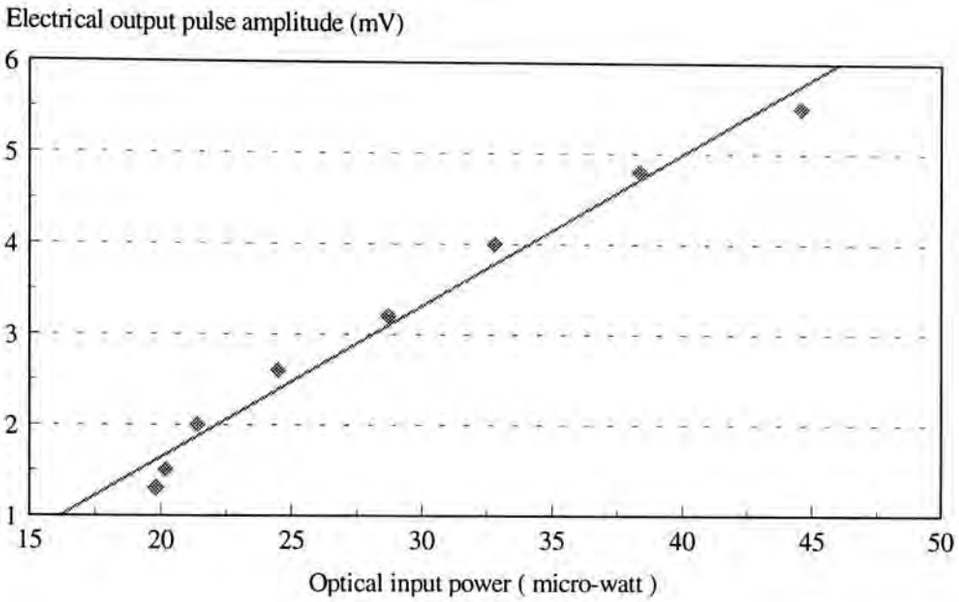


Fig. 4-11 Electrical output pulse amplitude against optical input power with negative bias voltage

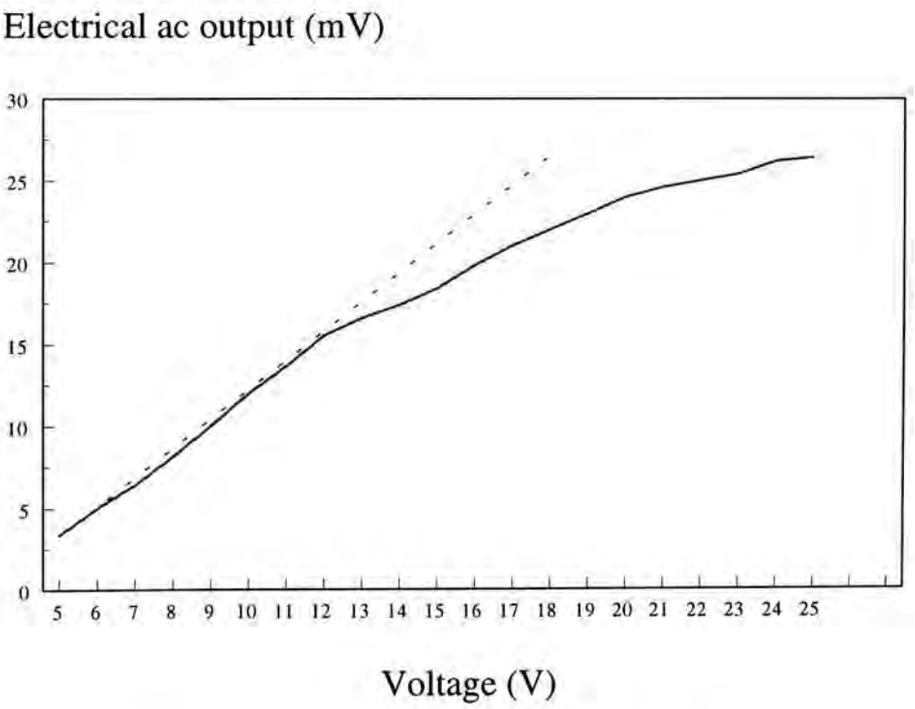


Fig. 4-12 Electrical ac output against bias voltage

Fig. 4-12 shows a plot of electrical ac output against the bias voltage. Gold is used for the metallization of the structure. PPL50M diode laser provides the input beam with a measured power of 70 μW. It can be observed that the ac output increases linearly with the bias voltage V_b for V_b less than 12 V. When V_b is further increased, the ac output begins to saturate. This saturation may be the result of some photo-induced carriers reaching the saturation velocity.

Since $V_d = \mu E$

where V_d is the drift velocity of the photo-induced carrier,

μ is the carrier mobility, and

E is the electrical field across the gap,

so at a bias voltage of 12 V, we get a drift velocity of 6500 cm^2/Vs x $(12V/10^{-3}cm) = 7.8 \times 10^7$ cm/s for electron. The value of the saturation drift velocity for GaAs is also in the order of 10^7 cm/s. Thus, the electrons should have reached the saturation drift velocity.

The saturation does not flat off immediately. It is because the hole carrier, with a much smaller mobility, has not reached their saturation drift velocity.

4.4.2 Autocorrelation measurement

In order to estimate the intrinsic response of the device, an optoelectronic autocorrelation measurement is made [56]. The measured FWHM of the autocorrelation curve is 260 ps. Assuming a

Gaussian profile, the result corresponds to a single gap response of 184 ps. However, owing to the use of MSM photodetectors, this figure is only an upper limit of the true value. This is because the optically generated ac bias for the sampling gap is relatively small. It slows down the gap response and results in a broadened autocorrelation trace.

4.4.3 Resistance of the gap switch

When an optical beam with an average power of 70 μW from the PPL50M module laser diode is illuminated onto the MSM photodetector, it is measured that the resistance of the gap drops from 60MΩ dark resistance to less than 1 MΩ. It has also been verified that the resistance is necessarily independent on the bias voltage, no matter what the polarity is.

4.4.4 Breakdown field of the gap switch

It is found that the gap breaks down at a bias voltage of 50 V. Since the gap length is 10 μm, it is calculated that the breakdown field is $5x10^4$ V/cm. The breakdown field for GaAs is $4x10^5$ V/cm. Thus, the measured value is one order of magnitude less than the expected one. This discrepancy is acceptable because it can be caused by the non-uniformity of the transmission lines which results in some high field regions.

5 EXPERIMENTAL TECHNIQUE

5.1 Measurement Procedure

I. Fix the device-mounted circuit board onto the microwave testbox. Verify the connections between the board transmission lines and the SMA connectors.

II. Settle the testbox on a three-dimensional precision stage to allow the fine adjustment of the position of the device.

III. Apply the dc bias voltages to the device. Usually, ten volts are used for both polarities.

IV. Connect the output of the device to the lock-in amplifier.

V. Feed the collimated input beam directly onto the device with the help of an infrared viewer. To get the largest photoresponse, the beam should be normal to the surface of the device.

VI. Chop the input beam with an optical chopper and prelimarily align the input beam with the lock-in amplifier until an optimum reading is obtained.

VII. Subsequently, include an objective lens to focus the parallel input beam onto the device. At this step, both the device and the fiber coupler holding the input beam should stay at their aligned positions tuned at **step VI**.

Only the precision stage holding the objective lens is adjusted to do the alignment.

VIII. When the lock-in reading is maximized, a bias-tee network is used to extract the ac signal from the device. Remove the chopper and feed the ac signal to the CSA 803 sampling oscilloscope.

IX. Further align the systems until the ac signal is maximized on the sampling oscilloscope.

X. When two beams have to be focused onto the device, repeat the above procedure with another input beam. The only difference is that the first beam should make an angle of approximately 45 degrees with the surface of the device to allow space for the second input beam.

5.2 Optical Sources

5.2.1 Description of PPL50M module

This source is a 850 nm diode laser in a microwave circuit made to pulse at a fixed repetition rate of 50 MHz. The multimode optical output is via a 50/125 core/clad Corning fiber fitted with an ST style optical connector.

Specifications :

Nominal Wavelength (nm)	Wavelength Tolerance (nm)	Spectral Width (nm)	FWHM (ps)	Peak Power (mW)
850	10	4	47	40

Fig. 5-1 depicts the optical pulse produced by the diode laser as measured by the New Focus photodetector. The measured pulse width is 55 ps.

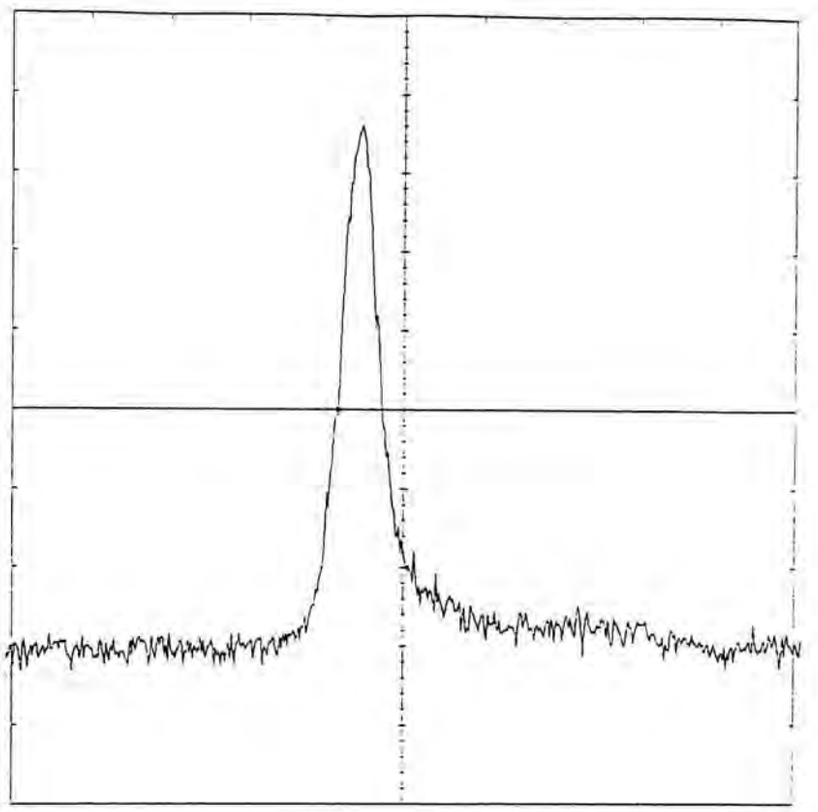


Fig. 5-1 Optical pulse from PPL50M module diode laser

5.2.2 Characteristics of OKI OL350A-4 laser diode

This laser is in a DIP module package with single-mode fiber pigtail. The emission wavelength is 1300 nm.

Fig. 5-2 shows the P-I plot of the laser diode. The threshold current of this laser is 19 mA and the output power is in the range of hundreds of μW for input current below 30 mA. The external quantum efficiency is 45 μ W/mA.

Power-Current characteristic :

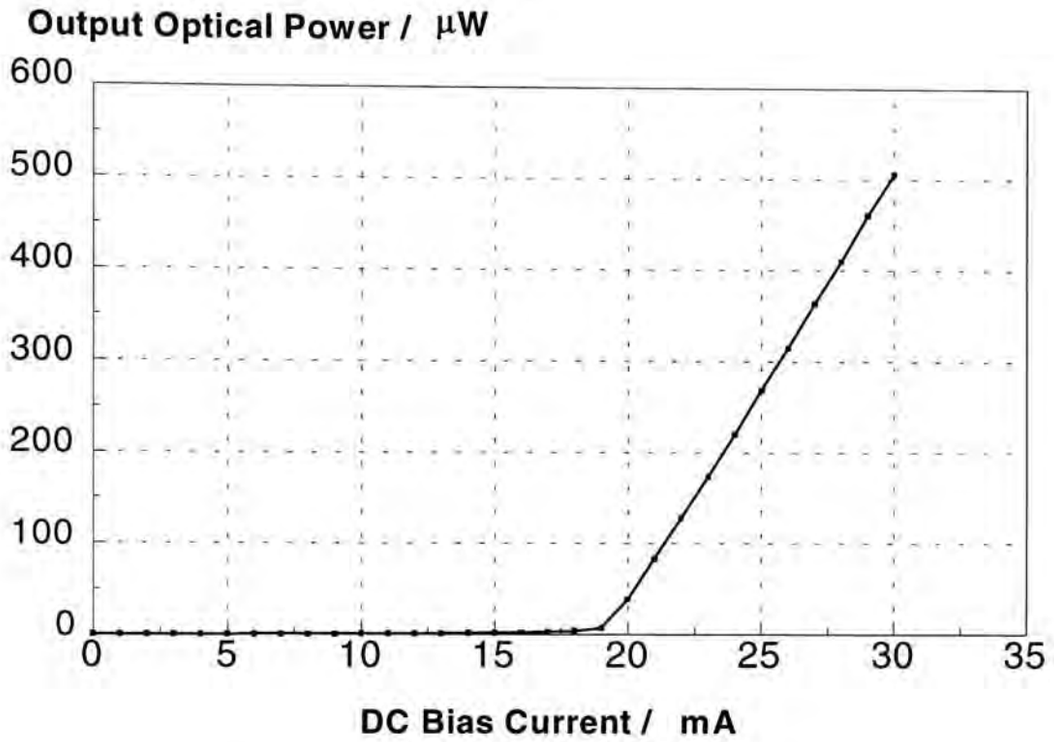


Fig. 5-2 Output power of OKI laser diode against input current

Gain-switching characteristic :

Gain-switching is a simple technique for producing short optical pulses from semiconductor lasers. It has the advantages of requiring no external cavity and the feasibility of producing light pulse at controllable repetition rates [64]. To generate ultrashort light pulses, picosecond electrical pulses are needed to drive a pre-biased laser diode. In our setup, the picosecond electrical pulses are provided by comb generators which accept a sinusoidal signal and generate a negative pulse whenever the input signal goes from a positive to a negative cycle. Fig. 5-3 shows the experimental setup used in the gain-switching of this laser. Signal generator HP 8657A provides a 0 dBm 100 MHz sinusoidal signal. The signal is amplified by a 24 dB gain

amplifier before it is used to drive the HP 33002A 100 MHz comb generator. The resulting electrical pulse train, which is depicted in Fig. 5-4, has a repetition rate of 100 MHz and a pulse width of 130 ps FWHM. A dc bias of 4 mA, provided by LDX-3412 precision current source, is coupled with this picosecond electrical pulses through a microwave bias-tee. The output is then used to drive the laser. The gain-switched laser pulse is monitored with the New Focus photodetector and the result is shown in Fig. 5-5. The pulse has an amplitude of 12 mV and a pulse width of 97 ps.

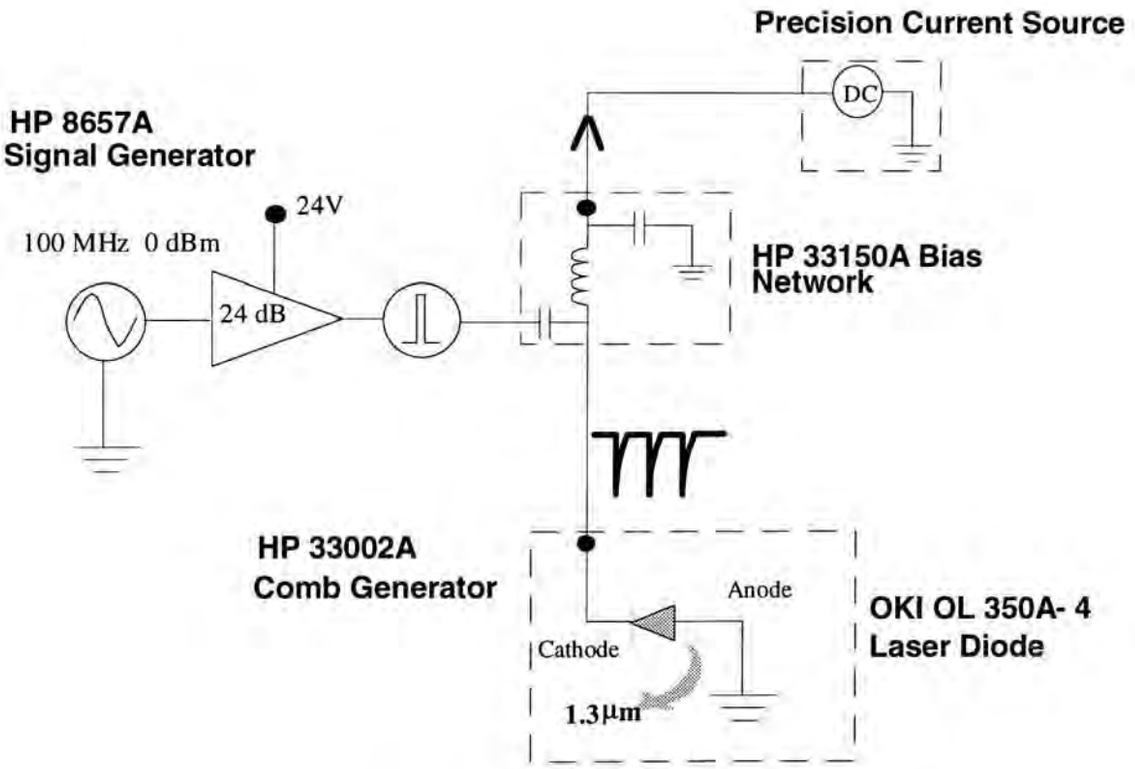


Fig. 5-3 Schematic diagram of the gain-switching setup

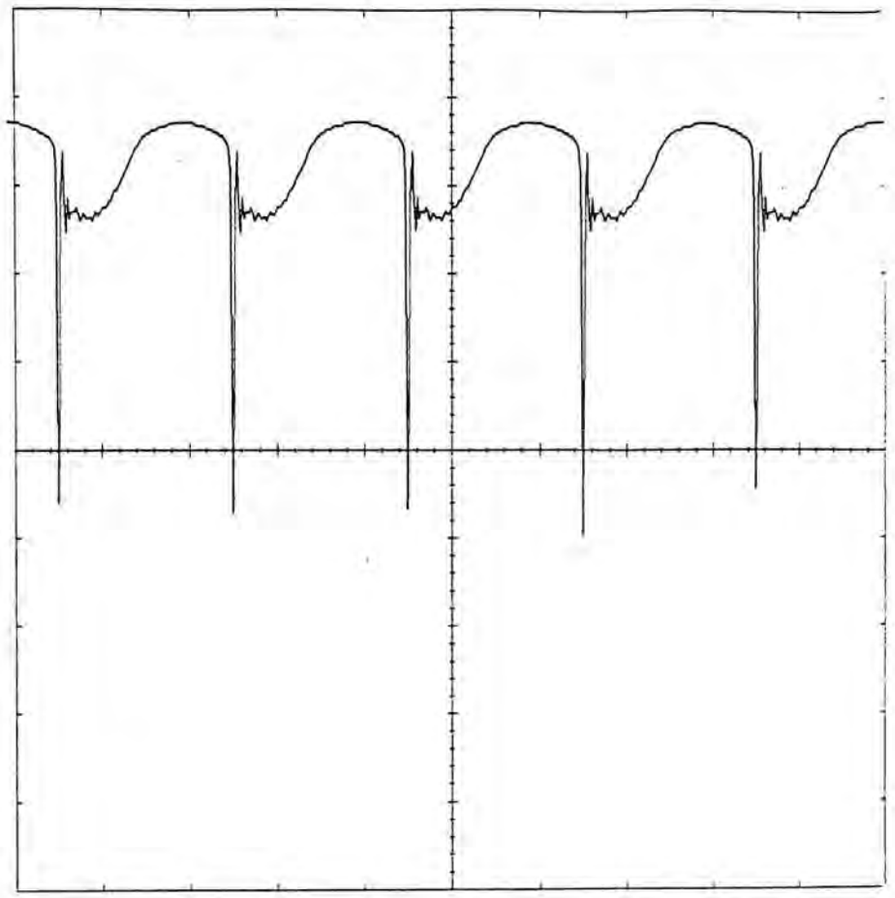


Fig. 5-4 Electrical pulses generated by the comb generator

As expected, the pulses generated by comb generator are negative. They get an amplitude of 1 V after being attenuated by 20 dB. This attenuation is needed to protect the sampling head of the CSA 803 sampling oscilloscope.

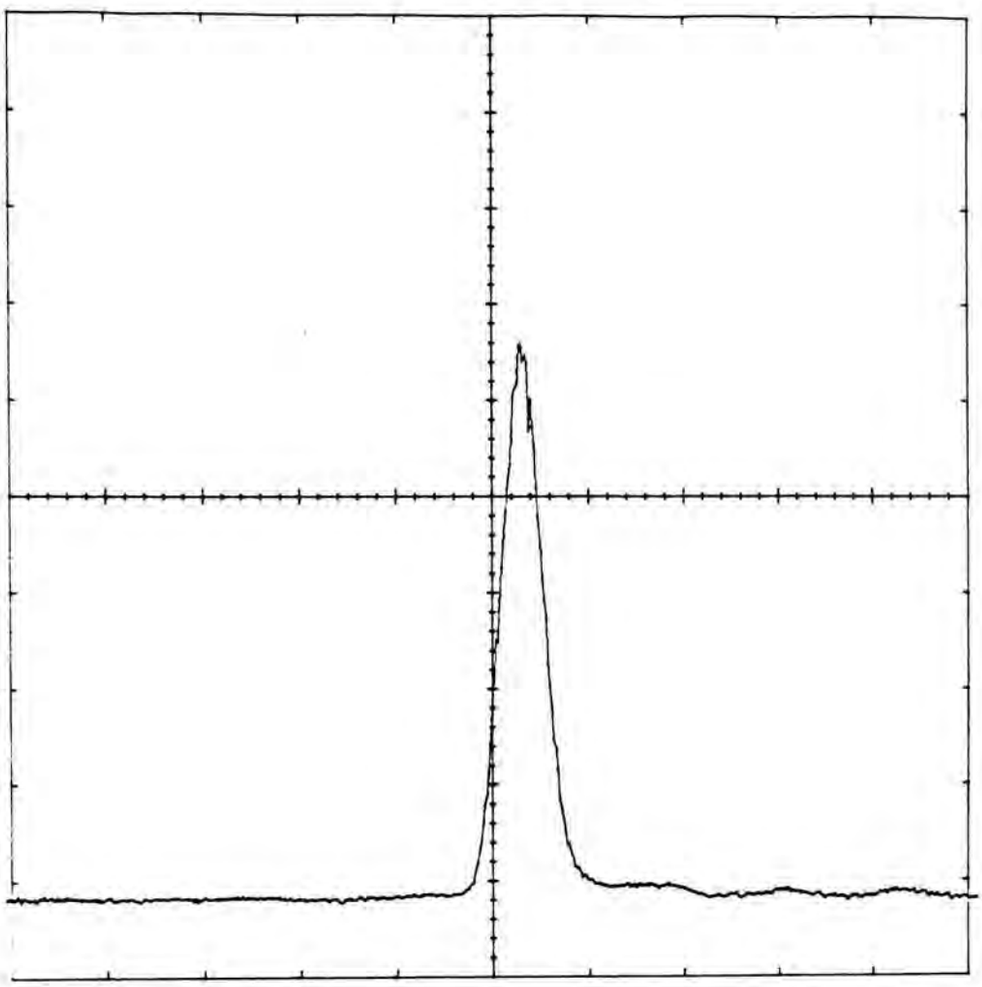


Fig. 5-5 Gain-switched pulse from OKI OL 350A-4 laser diode

5.3 Optical Alignment

5.3.1 Collimation and focusing of laser beam

The experimental arrangement for the collimation and focusing of a laser beam is shown in Fig. 5-6. Since the beam diverges quickly after coming out from a fiber (the divergence angle ranges from 23° to 35°) , the fiber is usually fitted into a fiber coupler in which an objective lens is incorporated to collimate the beam. Objective lens with large numerical

aperture is preferred because it can receive more light owing to its larger acceptance angle. Normally, a 20X objective lens is used. The degree of collimation of the beam is checked with a Newport F-IRC1 infrared sensor card. Then another objective lens is used to focus this collimated beam. The beam needs to be focused because the active area of our devices are very small, in the order of tens of micrometer.

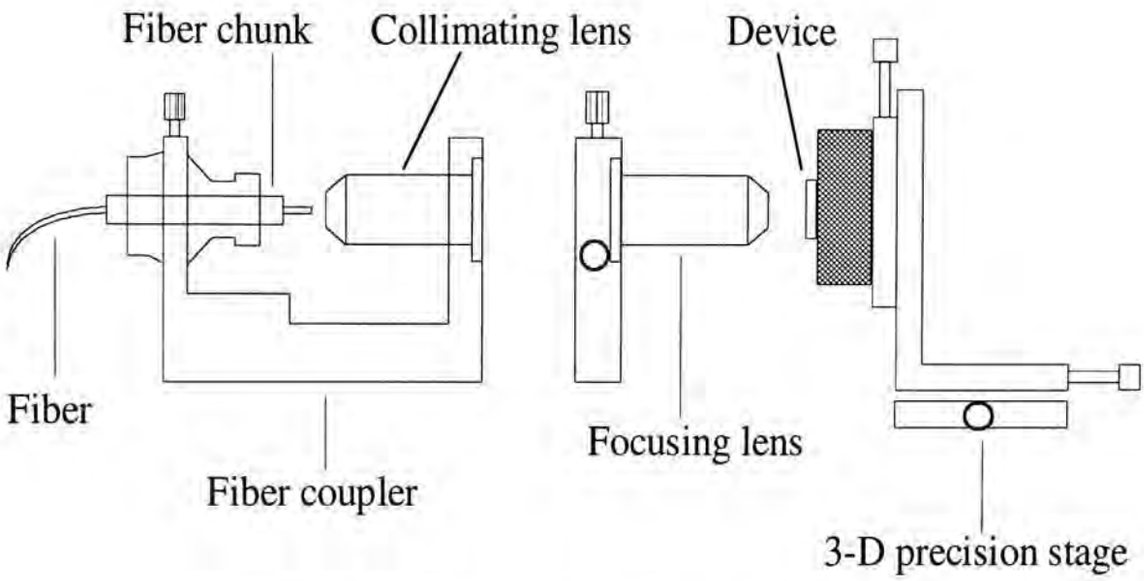


Fig. 5-6 Collimation and focusing of laser beam

In the experiment, two types of multimode fibers have been used :

<u>For ST connectorized fibers :</u>

Fiber coupler : Newport F-91-C1-T

Chuck : Newport FPH-CA

<u>For pigtail fibers :</u>

Fiber coupler : Newport F-915T

Chuck : Newport FPH-DJ

Connectorized fibers have the advantage of easy and effective coupling to the PPL50M laser source and to other connectorized fibers. Pigtail fibers provide more flexibility in tailoring the fiber length and are cheaper.

5.3.2 Use of lock-in amplifier and optical chopper

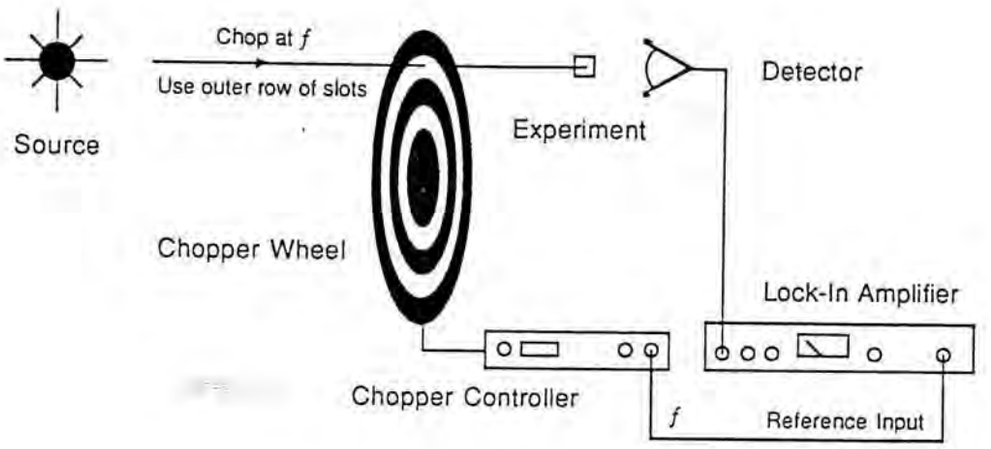


Fig. 5-7 Experimental setup of lock-in technique

To allow us to achieve an accurate alignment, a lock-in amplifier and an optical chopper is used. The lock-in technique enables us to measure very small ac signals, even when the signals are obscured by noises which may be a thousand times larger. This technique requires that the experiment be excited at a fixed frequency in a relative quiet part of the noise spectrum. The lock-in then detects the response from the experiment in a very narrow bandwidth at the excitation frequency [65]. The standard setup is shown in Fig. 5-7. The output from the testing device is fed to the lock-in amplifier.

To apply the lock-in technique, an optical chopper chops the input optical beam illuminating on the device. At the same time, the chopper controller informs the lock-in amplifier about the chopping frequency. In this way, the amplifier would average only those signals with frequencies that fall within the narrow bandwidth around the chopping frequency. The alignment is tuned in a way such that the lock-in reading is maximized.

5.3.3 Use of sampling oscilloscope to optimize the alignment

After the lock-in reading is maximized, a sampling oscilloscope is used to display the ac signal from the device. This ac signal can be obtained with the help of a bias-tee network. Owing to photovoltaic effect, the alignment position where the lock-in reading is a maximum need not be the same position where the ac signal is maximized. As a result, we need to further align our system by observing the ac signal on the oscilloscope. In other words, the lock-in technique only allows us to find an ac signal. The optimization has to be done with an oscilloscope.

5.4 Control of Optical Path Delay

5.4.1 The needs to control optical path delay

In doing the optoelectronic autocorrelation experiment to characterize the intrinsic response of the devices, the time delay between the light beams illuminating on the biasing gap and the sampling gap has to be monitored continuously such that the total sampled charge as a function of relative time delay can be obtained.

In addition, input beams have to be focused onto the testing device simultaneously in nearly all demonstrations of the logic devices. In other words, a zero time delay between the beams is needed for the logic operations.

Owing to the above applications, the need of a precise control on the time delay of the beams arises.

5.4.2 Experimental method to control optical path delay

The use of a stepping motor allows us to have a fine and accurate control on the relative time delay between the optical beams. The experimental setup is shown in Fig. 5-8.

One of the input beams is focused onto the device directly. The other beam is reflected twice by a pair of mirror mounted on a stage propelled by a stepping motor before it is focused onto the device. By adjusting the

position of the stage with the stepping motor controller, the time delay can be altered.

The resolution of the stepping motor is 1 μm. Thus, the minimum time delay adjustment is 2 μm, corresponding to 6.67 fs. This resolution is well above our need as the typical pulse width of the light pulse is around a hundred picoseconds.

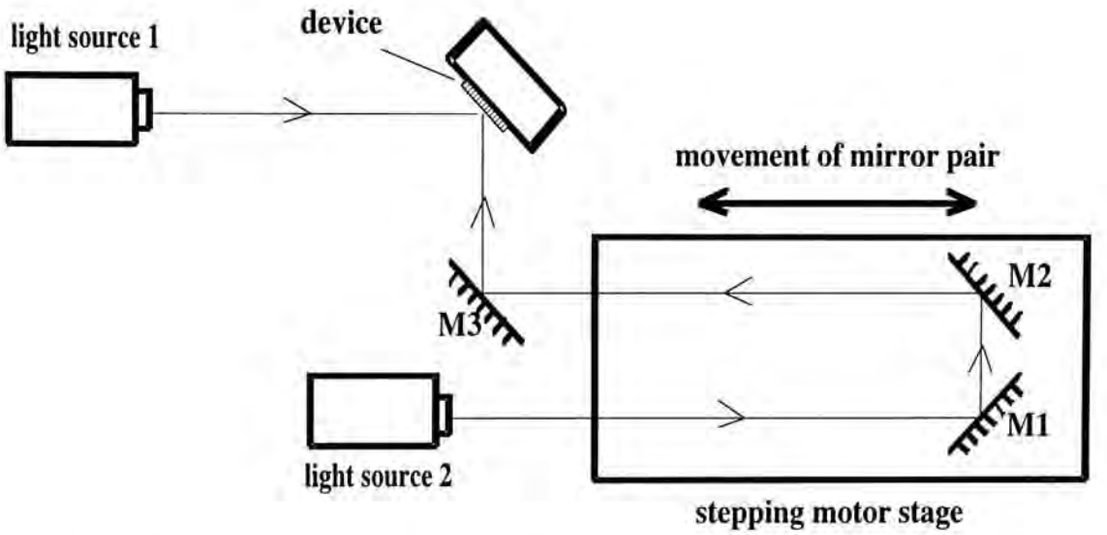


Fig. 5-8 Experimental setup to control the time delay between the input beams

5.5 Measurement Automation

To achieve automation of instruments and data acquisition by computer, a software package LabVIEW for Windows is used to develop a control system. LabVIEW is a graphical programming system for :

1. data acquisition and control,
2. data analysis, and
3. data presentation.

It offers an innovative programming methodology in which graphical software modules called virtual instruments (VIs) are graphically assembled. By using this application software package, the system development time can be reduced and the system is easier to modify and maintain.

In LabVIEW, a VI actually consists of three parts :

1. Front Panel :

This panel has knobs, slides, switches, graphs, strip charts, and so on. It serves as an interactive interface for supplying inputs to and observing output from the instrumentation system. This panel can be designed easily since creating a panel in LabVIEW is as simple as drawing a picture. It only needs to select a variety of controls and position them to build up the user interface.

2. Block Diagram :

This is the actual program that controls the VI. However, other than the conventional cumbersome text-based programming, it is a block diagram programming language. The functional blocks in the block diagram range from simple arithmetic functions to advanced acquisition and analysis routines.

3. Data Flow :

The functional blocks are connected by data paths and the data can flow in and out of the blocks through these paths. This type of data flow programming eliminates the constraints set out by the linear architecture of text-based languages.

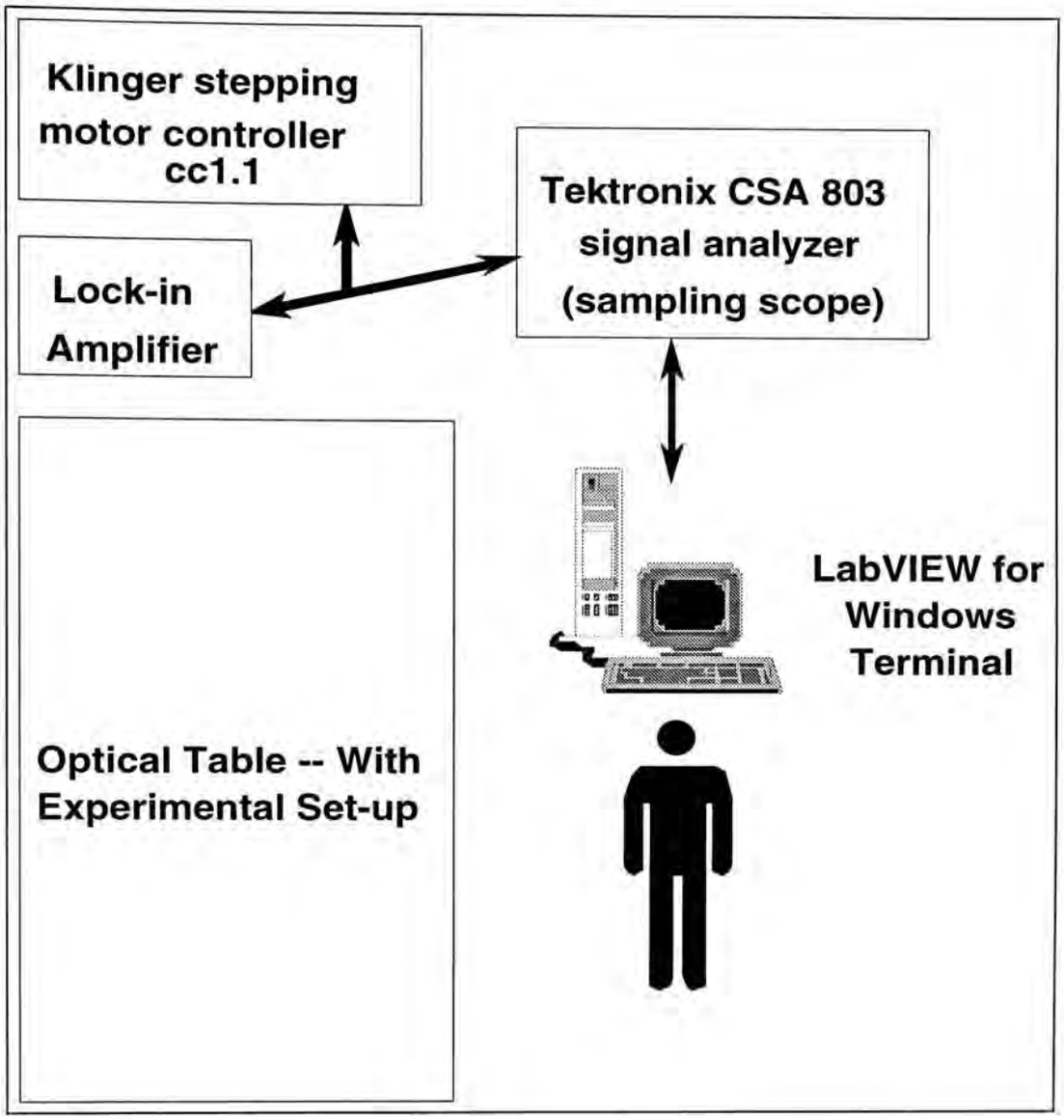


Fig. 5-9 A schematic diagram showing the automated control syste

In this project, I build up the VIs for the synchronization of the SR530 lock-in amplifier and the CC1.1 stepping motor controller. These VIs would be useful in doing the autocorrelation measurement. This measurement is needed to investigate the intrinsic response of the devices. The VI of CSA 803 signal analyzer is also used to take data into the computer. Fig. 5-10 depicts the front panel of the signal analyzer VI. The LabVIEW terminal is connected to the sampling oscilloscope, the stepping motor and the lock-in amplifier simultaneously through the IEEE-488

cables. Fig. 5-9 illustrates the setup of the automated control system. With this setup, the three systems can be controlled easily while doing the experiment on the optical table.

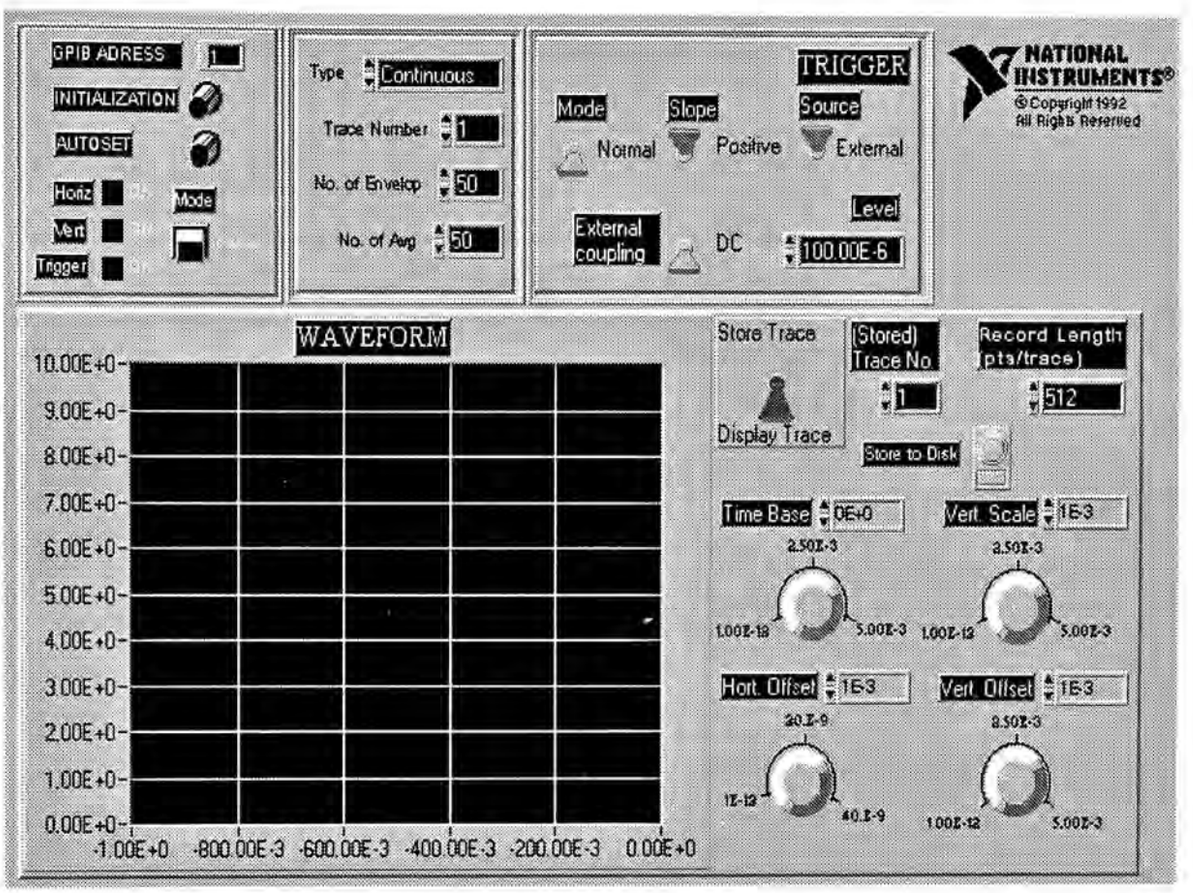


Fig. 5-10 Virtual instrument front panel for the sampling oscilloscope

6 DEMONSTRATION OF OPTOELECTRONIC LOGIC DEVICES

6.1 Optoelectronic OR Gate

6.1.1 Introduction

Truth table of logic function OR :

A	B	A + B
0	0	0
0	1	1
1	0	1
1	1	1

Table 6-1 Truth table of OR

The output of an OR circuit is on if as least one of the inputs is present as given in Table 6-1. Optoelectronic implementation of this function has been reported more than once [27,40,44]. However, the response of these devices is no better than the electronic logic gates available today. The fastest one is in the range of microsecond. In this work, a high speed optoelectronic OR gate, which makes use of a composite pair of ultrafast MSM photodetectors, is reported. The response time obtained is below 300 ps.

6.1.2 Design of the optoelectronic OR gate

Fig. 6-1 shows the circuit configuration of the device and the experimental set-up used for the logic gate operation. Gold is deposited onto undoped semi-insulating GaAs substrate to obtain the structure described in **Section 4**. When the inputs A and B are "0", no electrical signal can be obtained because of the large dark resistance of the MSM photodetectors. Otherwise, an electrical signal will be generated along the center transmission line owing to the closing of one or both gaps.

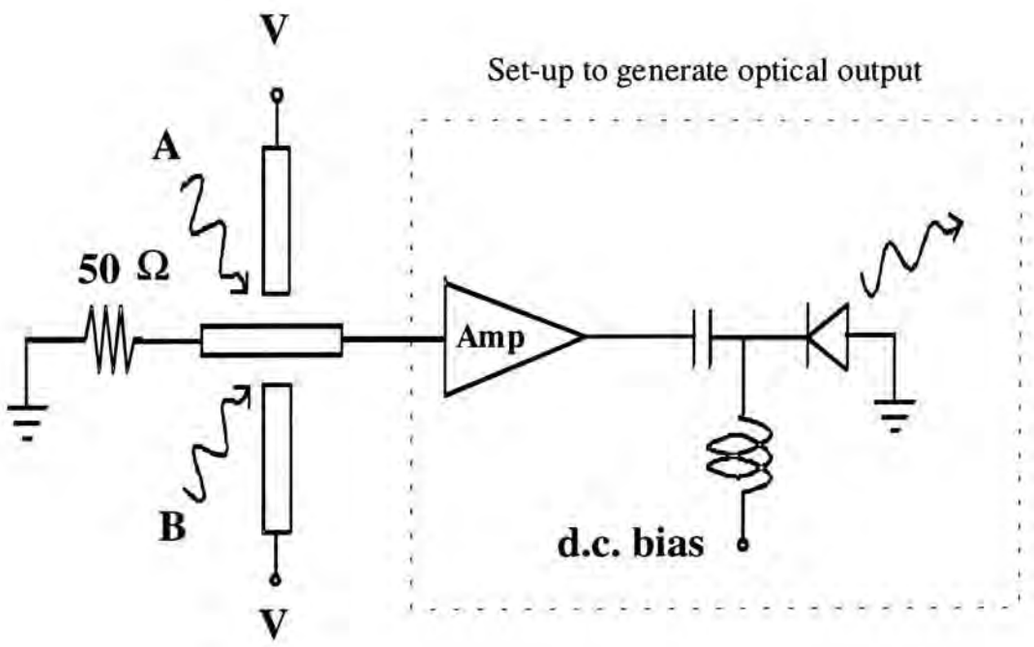


Fig. 6-1 Circuit configuration of the optoelectronic OR gate and a schematic representation of the experimental set-up

6.1.3 Experiment and Result

Optical inputs to the OR gate are provided by splitting the pulse train from the PPL50M laser diode. The measured average power of each beam is 33 μW and the switching pulse energy is 0.6 pJ.

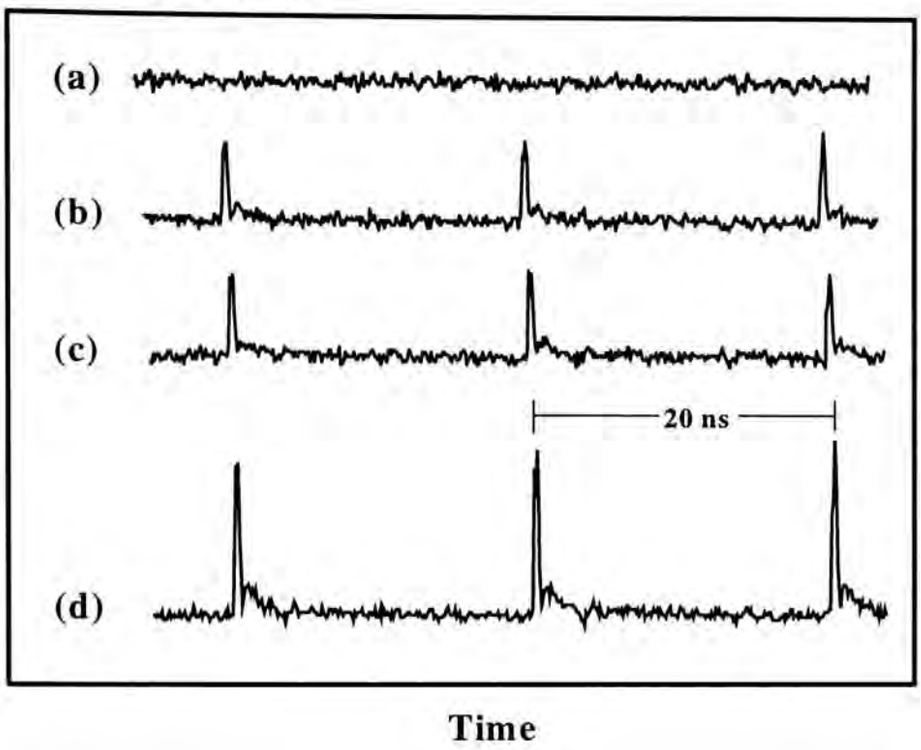


Fig. 6-2 Electrical outputs from the optoelectronic OR gate
(a) (0,0) (b) (0,1) (c) (1,0) (d) (1,1)

Output electrical signals from the device for different input logics are measured with a digital sampling oscilloscope and displayed in Fig. 6-2. Pulse width of the signals is below 300 ps. It can be observed that the amplitude of the electrical output for the case (1,1) is approximately double that of cases (0,1) / (1,0). This difference is expected as the presence of both inputs close both gaps and the larger number of carriers reaching the center transmission line gives rise to a larger signal. The on-off contrast ratio is limited by cases (0,1) / (1,0) and is found to be 13.7 dB.

6.1.4 Discussion

The input beams have to be illuminated onto the circuit simultaneously. Otherwise, two output pulses would come out in the case of input logics

(1,1). However, when the zero time delay of the two beams is ensured, the output signal for case (1,1) is double that for cases (0,1) / (1,0). This problem has to be solved in cascading applications.

An optical output can be obtained by amplifying the electrical pulses and using them to drive a pre-biased laser diode as depicted in the dotted part of Fig. 6-1.

Although this simple demonstration of logic function OR suffers from the problem of unequal outputs, the parallel branch concept involved in the design of the OR gate is useful in implementing more complex logic devices such as full adder. The Carry generator of the proposed serial full adder has made use of the configuration reported here to carry out the OR function of two AND operations. The problem above does not exist in the generator because the outcome of the two AND operations are mutually exclusive. In other words, case (1,1) does not exist for the OR operation in the generator. Details of the serial full adder will be discussed in **Section 7.2**.

6.1.5 Summary

An optoelectronic OR gate has been demonstrated using a composite pair of GaAs MSM photodetectors. It shows a fast response with an electrical output of pulse width less than 300 ps. The on-off contrast ratio is better than 13 dB. However, it suffers from the problem of unequal output. This may hinder its usefulness in cascading applications.

6.2 Optoelectronic Exclusive-OR (XOR) Gate

6.2.1 Introduction

Truth Table of XOR :

A	B	A⊕B
0	0	0
0	1	1
1	0	1
1	1	0

Table 6-2 Truth table of XOR

The following equations are two useful ways to express the XOR function :

$$A \oplus B = \overline{AB}(A + B) \qquad (6\text{-}1)$$

$$A \oplus B = A\overline{B} + \overline{A}B \qquad (6\text{-}2)$$

Optoelectronic XOR gates based on these two equations have been reported. Fig. 6-3 shows the circuit based on Eqn. (6-1) [50]. In this design, two MSM photodetectors are used for each optical input. There are three bias voltages V1, V2 and V3, where V1 and V3 are positive and V2 is negative. In case no light is launched onto the photodetectors, no conducting path exists and the output is "0". When either input is "1" and another is "0", say A is "1" and B is "0", the branches connecting to V2 and V3 will still be open. However, there is a conducting path from V1 to the output port. Therefore, an output can be obtained. The same situation is found when A is "0" and B is "1". When both A and B are present, all photodetectors are activated. Since V2 is of the opposite sign to V1 and V3, it is possible to obtain an output "0" for some suitable value of V2.

Thus, it can be seen that the path connecting the output to V2 performs the function ~(AB) and the paths connecting the output to V1 and V3 performs (A+B).

Since each input beam is used to illuminate two photodetectors, a trench is etched between them to provide a good isolation. Otherwise, crosstalk will become a problem. This requirement inevitably complicates the fabrication process.

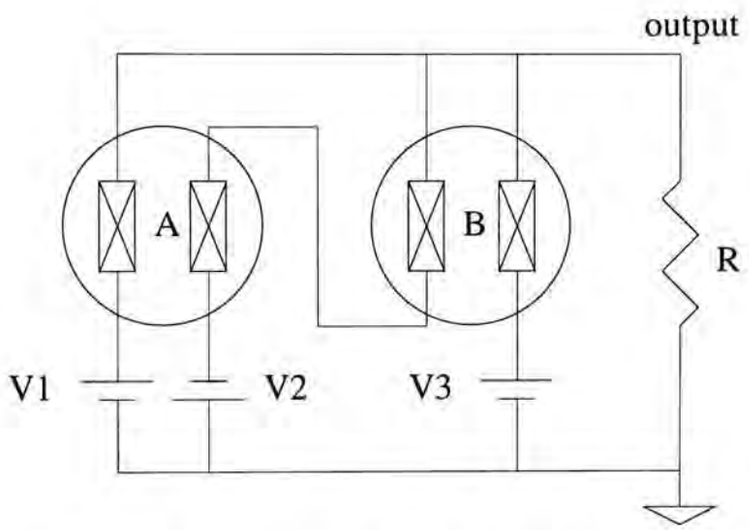


Fig. 6-3 Schematic representation of an XOR gate based on Eqn. (6-1)

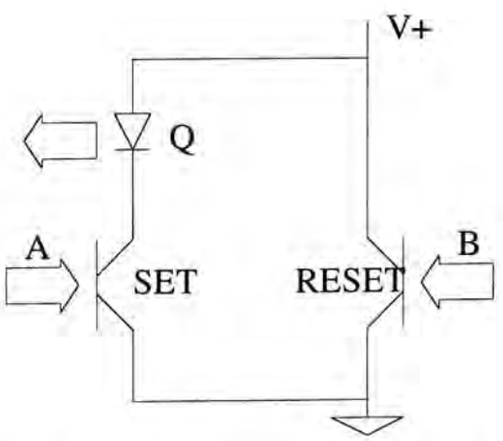


Fig. 6-4 Schematic diagram showing a circuit demonstrating the function (A AND ~B)

Fig. 6-4 shows the design based on Eqn (6-2) [37]. It performs the minterm (A AND ~B). Let Q, the initial state, be "0". Q would remain "0" for any pulse illuminating on RESET HPT. Once a pulse is launched onto SET HPT, a conducting current flows through the LED and thus Q is turned ON to give a "1". When both light beams are present on the HPTs, Q would be turned off because the voltage applied to the RESET HPT is higher than that to the SET HPT owing to the turn-on voltage of LED. As a result, the current flows through the RESET HPT. With a similar circuit performing the function (B AND ~A) and their output coupled together, the XOR function can be achieved.

However, due to the use of latching devices, there exists some flaw in operation [36]. When the LED has been latched ON, it can only be reset by either illuminating the RESET HPT or toggling the electrical bias. Thus, if the next input bit is "0", problem arises in resetting the LED to the required "0" output.

The above designs require two pairs of photo-sensitive devices for light detection. This not only increases fabrication and alignment complexity, but also requires higher input energy. Consequently, new design with only one pair of light-detection element is highly desirable. It is then found that this can be achieved if the output is generated in the optical domain [40]. However, the device demonstrated uses phototransistors for light detection and the response time is slow, in the order of microseconds. In this work, a high speed optoelectronic XOR gate is demonstrated using only a pair of GaAs photoconductive switches.

Applications of this logic function :

1. *As an inverting or non-inverting gate :*

When one input of the XOR function is permanently connected to a logic "1", it can be seen from Table 6-2 that the output would always give an inverted version of the input. Similarly, if the input is fixed to a logic "0", the input will appear non-inverted at the output.

2. *As a comparator :*

Whenever the inputs are equal, the output of XOR is "0". The output goes to logic "1" only when the inputs are unequal. This property makes it useful in matching application.

3. *Constructing parity generator and detector :*

To detect errors in transmitted digital data, a technique called parity checking has been employed. It compares the number of "1" bits in the transmitted word with the number of "1" bits received. To do this, an additional bit of data, called parity bit, is needed. This parity bit tells the receiver system whether the transmitted binary word contains an even or odd number of "1" bits. Consequently, if the number of "1" bits in the data word changes from odd to even or vice versa in the transmission, this parity bit will be able to tell that an error has occurred.

An even parity generator is shown in Fig. 6-5. Even parity means that the parity bit always adjusts the total number of "1" transmitted to an even number. For example, if the transmitted word is "1101", the parity bit would be "1". If the word is "1100", the parity bit would be "0". It can be

seen that the even-parity generator is constructed from three XOR gates. An odd parity generator can be constructed from the combinations of XOR and XNOR gates. It will be discussed in details in later section.

An even parity detector is shown in Fig. 6-6. In fact, it consists of the even parity generator (XOR gates 1 to 3) which generates an even parity bit from the data word received. A fourth XOR gate is then used to compare this bit with the parity bit of the original data word that have been transmitted. In fact, this comparing function can be done by an XNOR gate as well. The only difference is the definition for good parity. For the XOR gate, parity fault is indicated by an output "1". While for the XNOR gate, it would be "0".

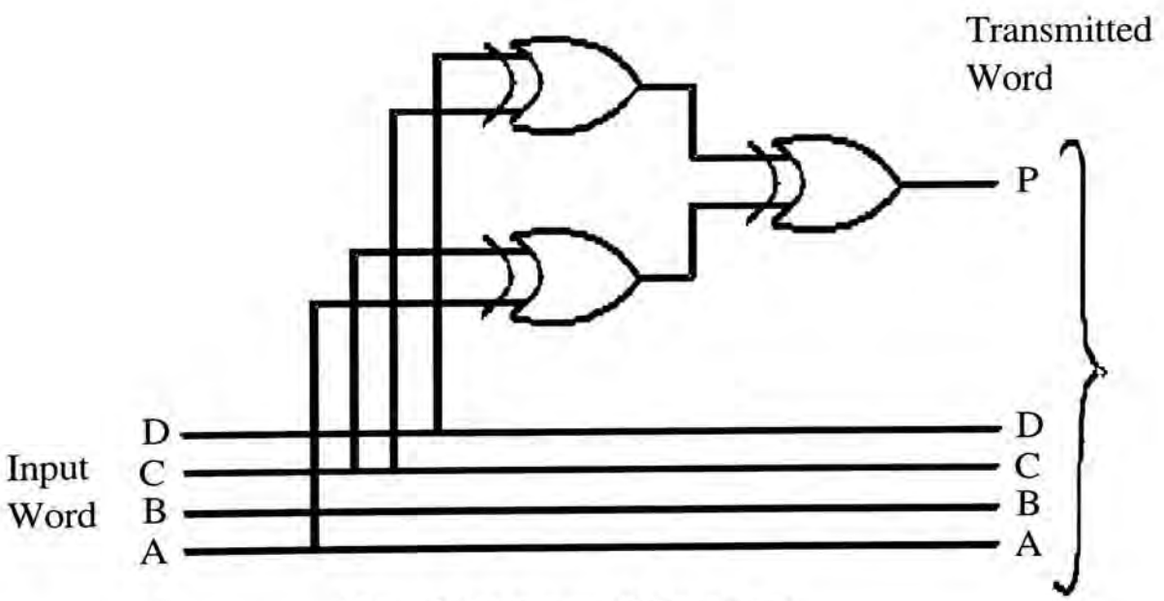


Fig. 6-5 An even-parity generator

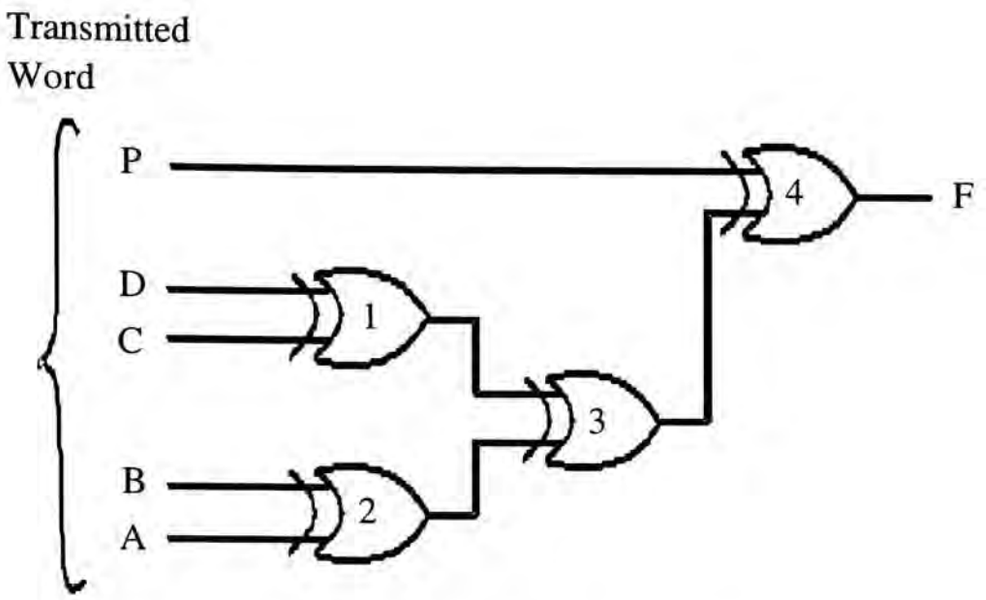


Fig. 6-6 An even-parity detector

4. *Generating the SUM bit in an adder :*

Truth table of an adder with no previous carry

A	B	SUM	CARRY
0	0	0	0
0	1	1	0
1	0	1	0
1	1	0	1

Table 6-3 Truth table of an adder with no previous carry

In view of Table 6-3, the SUM bit can be generated by applying the XOR operation on the two inputs while the CARRY bit can be obtained with the AND operation. Accordingly, the XOR function is useful in implementing an adder.

6.2.2 Design of the optoelectronic XOR gate

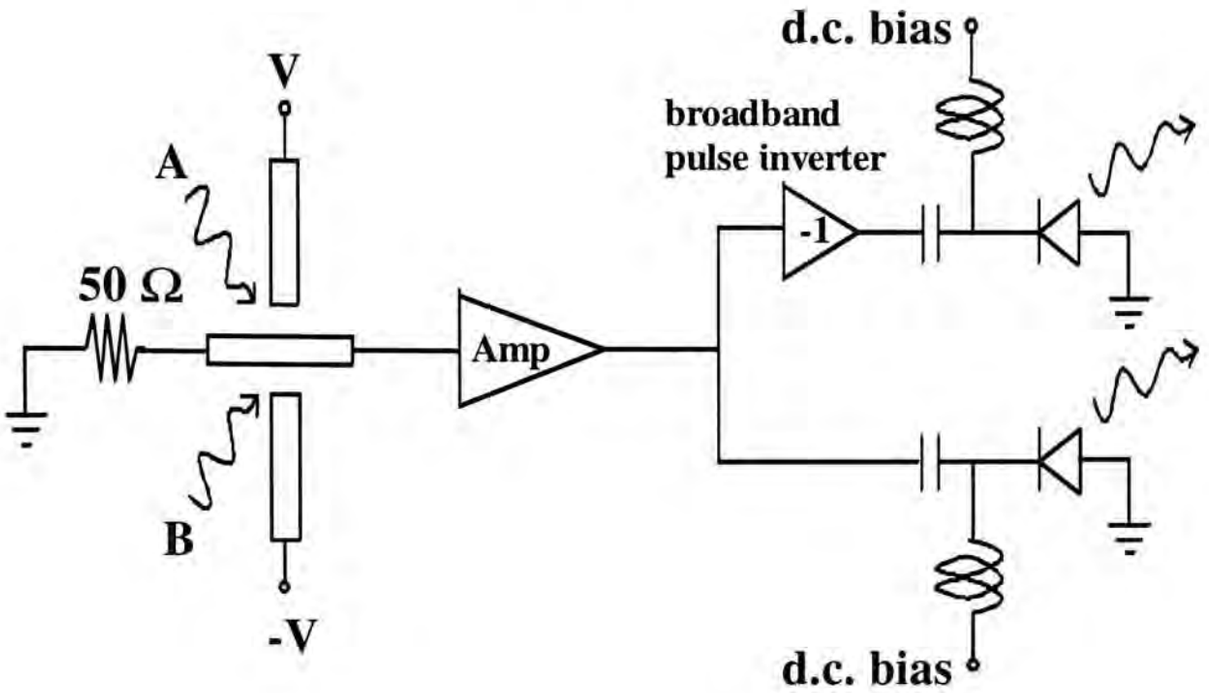


Fig. 6-7 Circuit configuration and experimental set-up of the optoelectronic XOR gate

Fig 6-7 shows the circuit configuration of the device and the experimental set-up used for the logic gate operation. Gold/Germanium/Nickel is deposited onto undoped semi-insulating GaAs substrate. The devices are then thermally annealed to form alloyed ohmic contacts. The structure of the devices has been discussed in details in **Section 4**. When the inputs A and B are "0", no electrical signal is generated along the center transmission line. When both inputs are "1", electrical signals from the two photoconductive switches will cancel each other as a result of the opposite bias voltages. If only A or B alone is "1" and the other is "0", a positive or negative electrical pulse signal will be generated. This electrical signal is then used to gain-switch an auxiliary laser diode and generates an optical output.

6.2.3 Experiment and Result

Optical inputs to the XOR gate are provided by splitting the pulse train from the laser diode PPL50M. The measured average power of each beam is 33 μW and the switching pulse energy is 0.6 pJ.

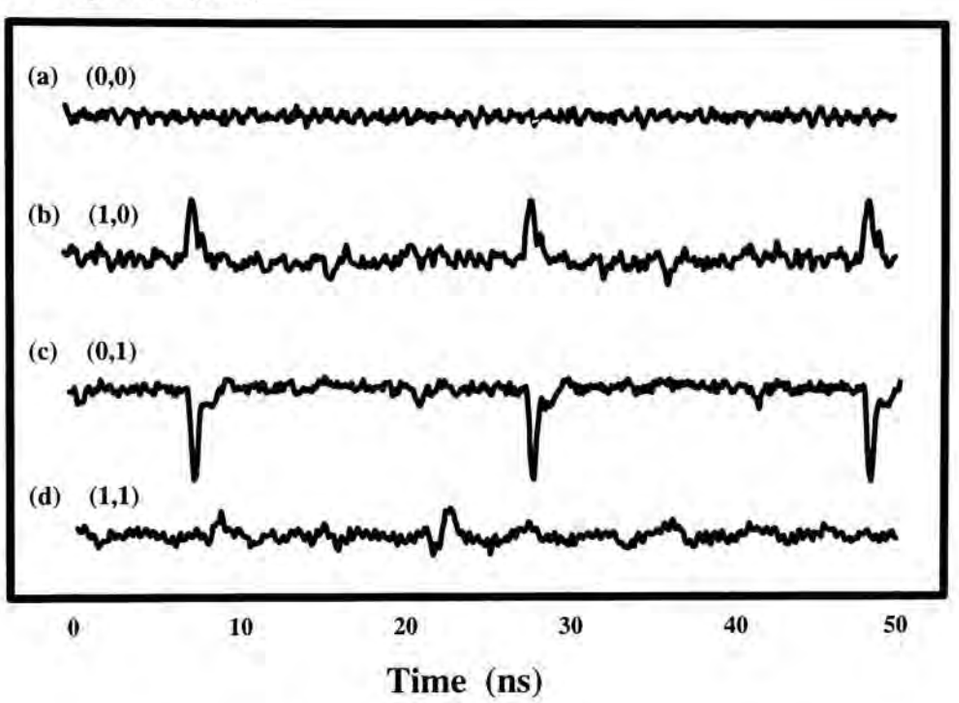


Fig. 6-8 Electrical output from the XOR device

Output electrical signals from the device are amplified and measured with a digital sampling oscilloscope. The results are displayed in Fig. 6-8 with various input logics. Pulse width of the signals is below 500 ps and the amplitude is above 1 V. As is shown in profile (d), cancellation of the signals is not complete when both inputs are "1". This is caused by slightly different pulse energy of the two beams. However, these undesirable residual signals will be suppressed in the optical output obtained from the gain-switched laser diode.

The OKI laser diode is used for generating the optical output. A dc bias of 12 mA is coupled with the amplified electrical signals from the XOR gate through a microwave bias-tee. The output is then used to drive the laser. The gain-switched laser pulse is monitored with the New Focus photodetector. The signal is then observed on the sampling oscilloscope. Results for the beam pulses are displayed in Fig. 6-9.

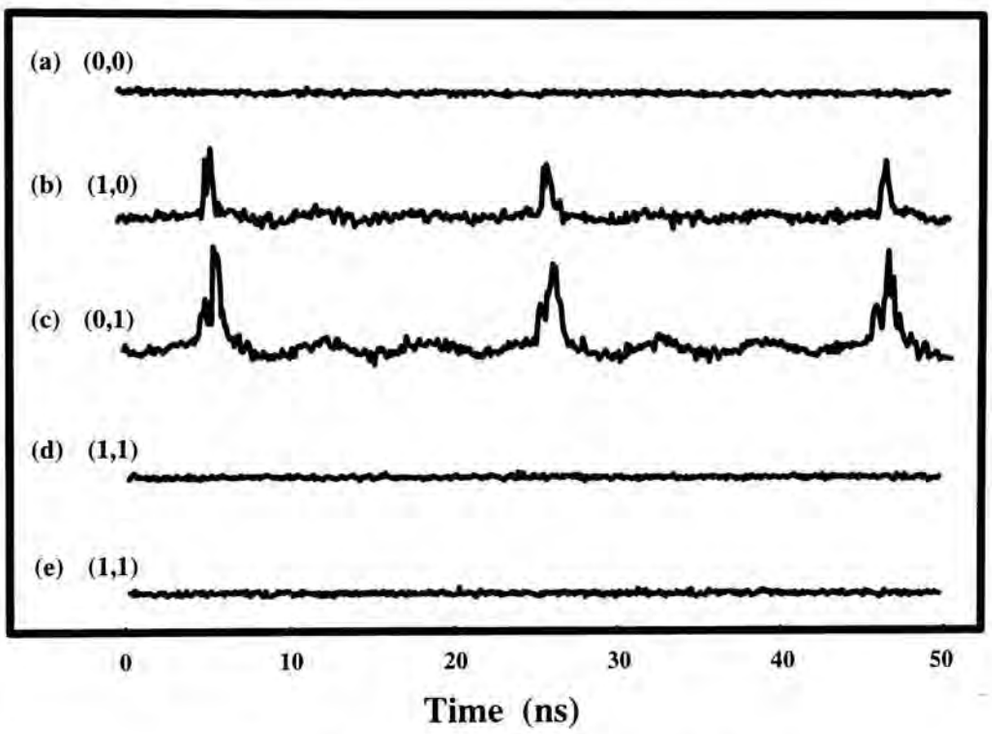


Fig. 6-9 Optical output from the device

When the electrical output from the XOR gate is of opposite sign to the dc bias, a broadband pulse inverter with a risetime of 20 ps is used to flip the ac signal. The main concern here is whether the amplified residual electrical signal would be large enough to drive the laser diode and causes undesirable output when both optical inputs are present. The optical outputs for the (1,1) case with and without the pulse inverter, which

corresponds to two opposite sign of pulse input, are displayed in profiles (d) and (e) of Fig. 6-9. No observable optical pulse is generated. The on-off contrast ratio is observed to be higher than 19 dB. The output optical power of the case (1,1) is less than 1 μW, which is about the same to the case when there is no input. For the cases (1,0) and (0,1) with desired optical output, a 13 μW power is obtained. In the experiment, signal pulse width less than 400 ps has been achieved.

To investigate the optical energy required to change the logic states, we adjust the attenuation of one of the input beams in the case (1,1). It is observed that there remains no output signal as long as the input power of the beams is kept below the ratio 2.5 : 1. This means that a good contrast ratio can be easily achieved even when there is fluctuation in the input optical power. When the power of the input beams is in the ratio 6 : 1, the output amplitude increases to half of the value for a logic "1".

6.2.4 Discussion

Owing to the limited bandwidth of some amplifiers used in the set-up, optimum performance of this device has not been achieved. As the wavelength of the input beams is close to the absorption edge of GaAs at 0.89 μm, the density of generated carriers and hence the photocurrent is small. Shorter wavelength can be used to increase the absorption coefficient and results in a larger photoresponse. It follows that a smaller signal amplification will be needed.

This design of the logic gates allows a large flexibility in the output wavelength. If the gain-switched laser diode is replaced by one operating at the input wavelength, the output of this gate can serve as an input to another. This cascadability is particularly important for its usage in more complex logic devices such as an adder. On the other hand, the two gain-switched laser diodes can be chosen to operate at different wavelengths. When the two input signals are matched (0,0) or (1,1), there will be no output. But when the signals are different, we can determine which of the input beam pulses is present from the wavelength of the output signal. This information will facilitate subsequent processing with the outputs.

A serial comparator can also be implemented with this logic gate. It serves to compare the magnitude of two data words. Instead of combining the output of the two lasers, they are arranged to illuminate two different photodetectors. The MSB of the words are fed to the gate first. If the bits are the same, there would be no output and the next bit pair is compared. Once a bit pair is different, their relative magnitude can be determined from the photodetector outputs. The comparison stops either when two input bits are found to be different (one word is found to be larger than another) or the LSB pair has been processed (the two words are equal).

6.2.5 Summary

In summary, a high speed optical-in optical-out exclusive-OR (XOR) gate based on GaAs photoconductive switches has been demonstrated. The output response time is shorter than 400 ps. On-off contrast ratio better than 19 dB has been achieved. The processing of the device is relatively

simple. It can be made cascadable and will be a promising device in applications such as optical signal processing and optical computing.

6.3 Optoelectronic Exclusive-NOR (XNOR) Gate

6.3.1 Introduction

Truth table of XNOR :

A	B	$\overline{A \oplus B}$
0	0	1
0	1	0
1	1	0
1	0	1

Table 6-4 Truth table of XNOR

This function is complementary to XOR. It can be expressed in the two following forms :

$$\overline{A \oplus B} = AB + \overline{A}\,\overline{B} \qquad (6\text{-}3)$$

$$\overline{A \oplus B} = (\overline{A} + B)(A + \overline{B}) \qquad (6\text{-}4)$$

This logic function, to the best knowledge of the author, has not been reported using the optoelectronic approach. In electronic computing, it is usually achieved by cascading other logic gates.

Applications of this logic function :

1. *As an inverting or non-inverting gate.*

It can perform these tasks in the way as the XOR function. It is inverting when one of its inputs is fixed to "0" and non-inverting when is fixed to "1".

2. *As an equality function :*

From Table 6-4, this function gives an output logic "1" only if the input logics are identical. As a result, it is also useful in the matching applications. For example, a number of them can be used simultaneously to program a machine to do certain functions whenever the counter reaches some specified sets of numbers.

3. *As a parity generator and detector :*

Similar to that done by the XOR function, only the definition of parity is different. Its usage is particularly important in implementing odd-parity circuits. As shown in Fig. 6-10, the odd-parity generator is similar to the even-parity generator, only that the third XOR gate is replaced by an XNOR gate.

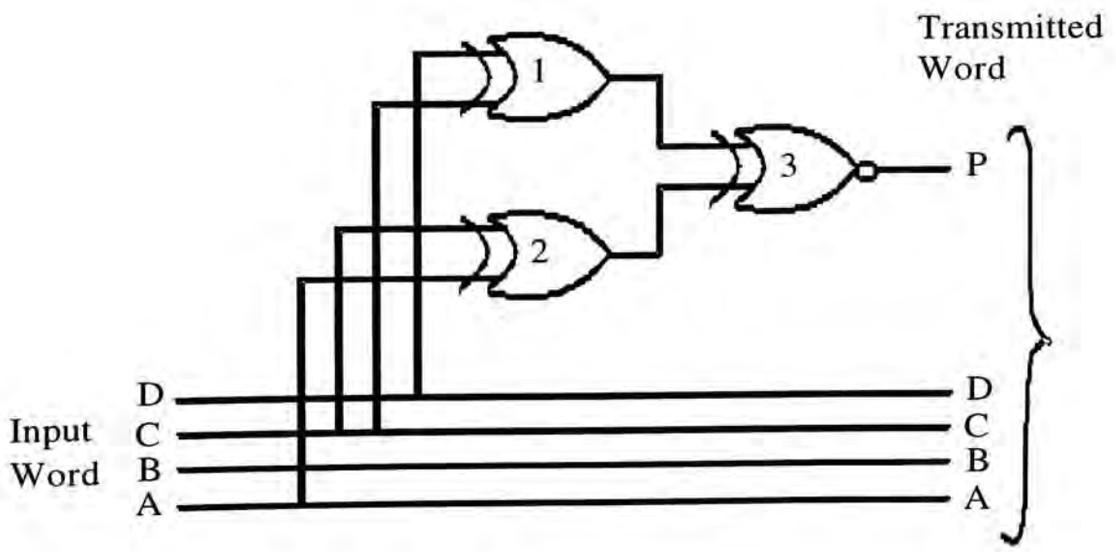


Fig. 6-10 An odd-parity generator

4. *Generating the SUM bit in an adder :*

Truth table of an adder with previous carry bit "1"

A	B	SUM	CARRY
0	0	1	0
0	1	0	1
1	0	0	1
1	1	1	1

Table 6-5 Truth table of an adder with previous carry bit "1"

In view of Table 6-5, the SUM bit can be generated by applying the XNOR operation on the two inputs while the CARRY bit can be obtained with the OR operation. Accordingly, the XNOR function can also be useful in implementing an adder.

6.3.2 Design of the optoelectronic XNOR gate

Fig. 6-11 shows the circuit configuration of the device and the experimental set-up used for the logic gate operation. The metallization is processed by depositing gold onto undoped semi-insulating GaAs substrate. To implement the XNOR operation, two input logic beams, A and B, are combined and focused onto a MSM photodetector. The other photodetector is illuminated by an enable beam with the same pulse energy. The enable beam is needed because XNOR gate is a normally-on device. When the inputs A and B are "0", a positive electrical pulse signal will be generated. If only A or B alone is "1" and the other is "0", electrical signals from the two MSM photodetectors will cancel as a result of the

opposite bias voltages. When both inputs A and B are "1", a negative electrical pulse signal will be generated since the combined optical power of the signal beams is double that of the enable beam.

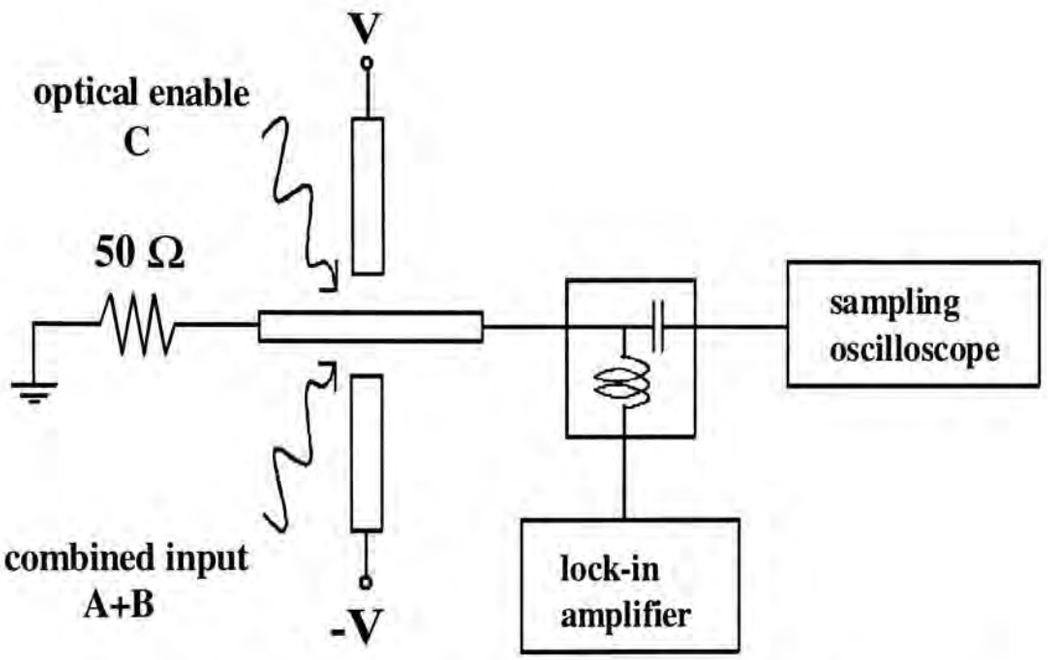


Fig. 6-11 A schematic representation of the optoelectronic XNOR gate

6.3.3 Experiment and Result

As shown in Fig. 6-12, optical inputs to the XNOR gate are provided by splitting and recombining the pulse train from a AlGaAs/GaAs MQW laser diode operating at 100 MHz. A and B are the two input logic beams. C is the enable beam with optical pulses at roughly 200 MHz. In the experiment, only a fixed length of fiber is used as the delay line to demonstrate the logic. With a proper delay, repetition rate at exactly 200 MHz can be achieved. Average power of this beam is 13 μW and the optical pulse energy is thus 65 fJ. Beam D is the signal beam representing the combined input of A and B. The beam consists of two pulses of different

amplitudes. They follow one another alternatively at the same repetition rate of 100 MHz. The larger pulse has an amplitude double that of the smaller pulse. It represents the presence of both A and B input signals (1,1). The input logic (1,0) or (0,1) is represented by the smaller pulse which has an amplitude equal to that of the enable beam.

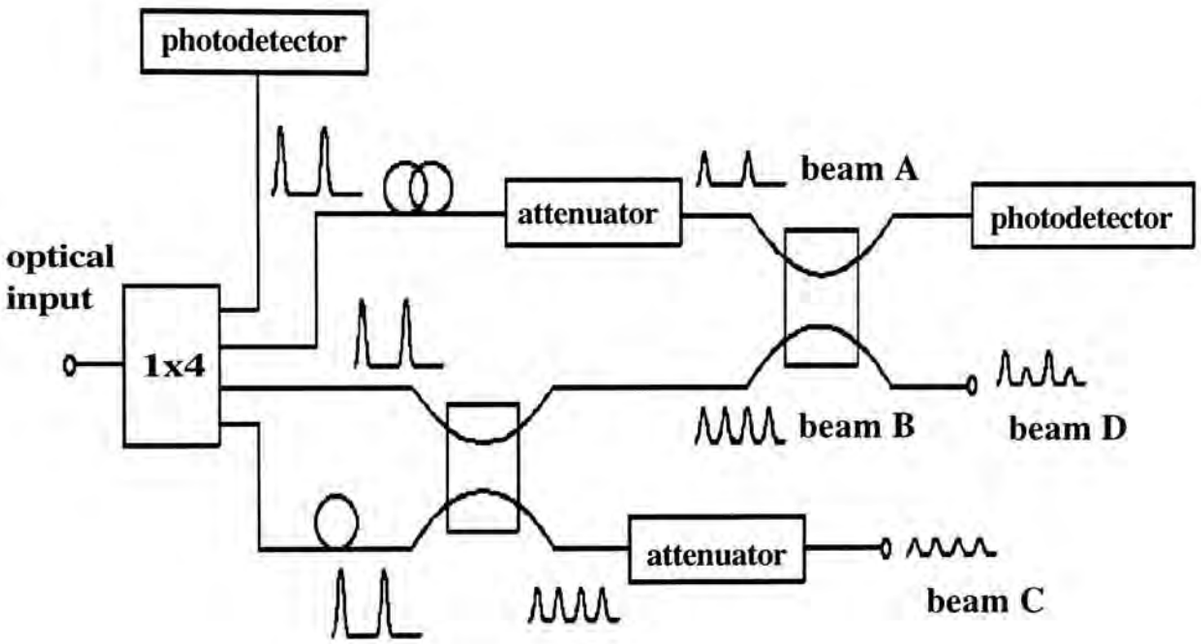


Fig. 6-12 Layout for the arrangement of the optical inputs

Fig. 6-13 depicts the response of the positively biased MSM photodetector to beams C and D. The uneven baselines are caused by signal reflections from the mounting parasitics. The 200 MHz signals are not equally spaced because the delay line used in constructing these signals does not give an exact 5 ns time delay. A slight difference in pulse amplitudes is detected from beam C, indicating that the splitting ratio of the 3 dB couplers is not exactly 1 : 1. Response of the photodiode to beam D shows two pulses of

different amplitudes. Their ratio is 2 : 1 which is expected from the linear response of the device to the optical power.

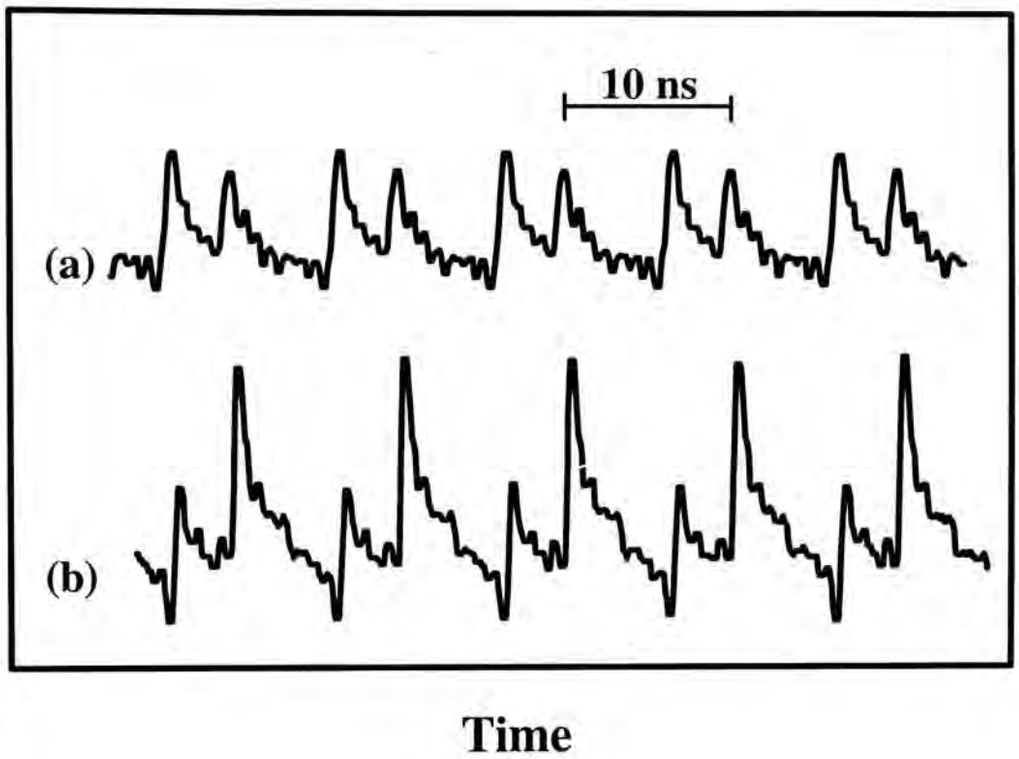


Fig. 6-13 Photodetector response to the optical beams
(a) Enable beam C (b) Combined input beam D

Electrical output from the XNOR gate is measured with the digital sampling oscilloscope. The results are displayed in Fig. 6-14. Profile (a) shows the output when both enable beam C and combined signal beam D are present on the respective gap. Owing to a difference in pulse energy, the electron-hole pairs generated from the larger pulses of beam D are more than that generated from the enable pulses. Thus, there is a net flow of electrons to the center detector electrode. A negative electrical pulse is then generated. In other words, an output logic "1" is obtained when the input is (1,1). At the moments when the smaller pulse of beam D is present, no output can be

observed as the signals are completely cancelled by the equal-magnitude enable pulses. In order to obtain a positive output signal, a broadband pulse inverter with a risetime of 20 ps is used to flip the output pulses. The result is shown in profile (b). A slight degradation in the signal amplitude is observed. Operation of the XNOR gate for input logic (1,0), (0,1) and (1,1) have been demonstrated. To implement the input logic (0,0), we simply remove the signal beam so that only the enable beam is focused onto a MSM photodetector. The output is shown in profile (c). It is observed that a pulse signal exists when the input logic beams are absent. The signal has a FWHM of 736 ps.

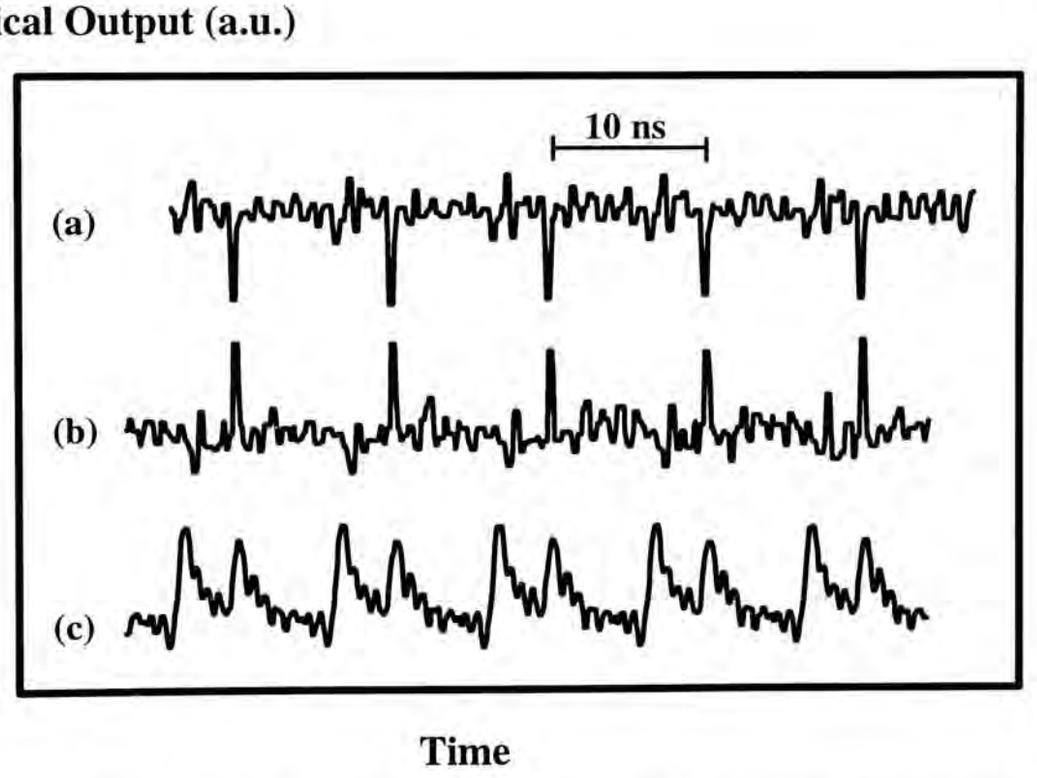


Fig. 6-14 Electrical output from the device (a) Both beams C and D are present (b) Same as (a) but with the use of a pulse inverter (c) Only beam C is present

While the electrical outputs for (0,0) and (1,1) are "1" and "-1", respectively, they can be made identical in the optical domain. To realize

the transformation, the electrical signal is split into two branches and one of them is allowed to pass through a pulse inverter. Each branch is then used to drive a pre-biased laser diode, which will emit light in the presence of a negative pulse. In this way one of the laser diode will produce an optical output regardless of the original sign of the electrical signal. Outputs from the two laser diodes can be coupled into a single fiber to give the desirable XNOR output. Similar operation has been done for the function XOR.

The on-off contrast ratio is determined from the amplitudes of the output for different input logics. From profile (a), the contrast ratio between (1,1) and (0,1) / (1,0) is measured to be 9.9 dB. In the case when a pulse inverter is used to flip the output, the ratio reduces to 6.2 dB. On the other hand, the contrast ratio between (0,0) and (0,1) / (1,0) is determined from profiles (b) and (c) to be better than 7 dB.

An interesting observation is that the output pulse width in profile (b) appears to be shorter than that in profile (c). This phenomenon is caused by a partial cancellation of the positive and negative tails in the pulse signals. While the peak amplitude is linearly dependent on the optical power, the tail appears to have the same magnitude. It suggests that some non-ideal factors such as thermal re-emission of carriers from the trap energy levels may play a role in determining the tail characteristics.

6.3.4 Discussion

In system application, no output should be generated in the absence of the enable beam, regardless of what the inputs are. This is not the case for the

operation of our device. To meet the goal, another MSM photodetector can be fabricated onto the detector electrode of the device. This photodetector is also activated by the same enable beam with a proper time delay. It will impose a large resistance to the signals generated by the inputs when the enable is absent. Alternatively, the device can be biased with an ac electrical clock signals synchronized with the enable beam. This will ensure that no output is generated when the enable beam is absent. For a proper functioning of the XNOR gate, it should be noted that the enable signal and the logic inputs must be synchronized. It may be done most conveniently with the system clock signals.

6.3.5 Summary

In summary, a high speed optoelectronic exclusive-NOR (XNOR) gate based on a composite pair of GaAs MSM photodetectors has been demonstrated. Output response time shorter than 800 ps has been achieved with an on-off contrast ratio better than 6.2 dB. The logic gate structure is relatively simple and is ready for monolithic integration with other optical and electronic devices. It will find important applications in bit pattern matching for optical signal processing and optical computing.

6.4 Optoelectronic 2 to 4 Decoder

6.4.1 Introduction

Truth table of 2 to 4 decoder :

INPUTS		OUTPUTS			
A	***B***	**1**	**2**	**3**	**4**
0	0	**1**	0	0	0
0	1	0	**1**	0	0
1	0	0	0	**1**	0
1	1	0	0	0	**1**

Table 6-6 Truth table of 2 to 4 decoder

In electronic computing, much of the information is handled in a highly encoded form. In an instruction, an n-bit field may be used to denote 1 out of 2^n possible choices for the action to be taken. To perform the desired action, the encoded instruction must first be decoded [66]. A decoder is a circuit which permits one of 2^n possible outputs to be selected, where n is the number of bits in a binary word specifying the selected output. A 2 to 4 decoder is a logic device with two inputs and four outputs, i.e. n = 2. At each time, depending on the two-variable input logics, only one of its four outputs would be active.

6.4.2 Design of the 2 to 4 optoelectronic decoder

To implement this function, two pairs of MSM photodetectors have been deployed. Fig. 6-15 shows the schematic layout of the optoelectronic decoder consisting of two circuits 1 and 2. The input beams A and B are each split into two equal parts such that the MSMs of both circuits are able to receive the logics carried by them. In circuit 1, beams A and B are focused onto two different photodetectors in a symmetric manner, which are biased at equal and opposite voltages. While for circuit 2, both beams A and B are illuminated onto the same photodetector. Another photodetector with an equal and opposite bias is illuminated by a clock beam. Electrical outputs from the circuits are amplified and are split into two branches. One branch from each circuit is allowed to pass through a pulse inverter. The electrical signals are then connected to several pre-biased laser diodes, which will emit light in the presence of a negative pulse. In this way, one and only one laser diode will be activated depending on the logics of the input beams A and B.

When the inputs A and B are "0", no output will be generated from circuit 1 while a positive electrical pulse signal will result from circuit 2 owing to the presence of the clock beam. Accordingly, only laser diode 00 will be activated. If only A or B alone is "1" and the other is "0", electrical signals from the two photodetectors of circuit 2 will cancel as a result of the opposite bias voltages. On the other hand, a pulse will be generated from circuit 1 with its polarity determined by whether A or B is present. Consequently, either diode 10 or diode 01 will emit light. When both inputs A and B are "1", no signal will be produced from circuit 1 because

the photodetectors are biased equal and opposite. A negative pulse signal will be generated from circuit 2 since the combined optical power of the signal beams is double that of the clock beam. As the device has a linear response in this range of optical power, the negative pulse will have the same amplitude as the positive signal in the case of (0,0). This negative electrical signal is then used to drive the laser diode 11 to generate an optical output. In other words, the four laser diodes serve as outputs of the decoder and each input logic will lead to the activation of one and only one of them. The electrical and optical outputs for different input logics are summarized in Table 6-7.

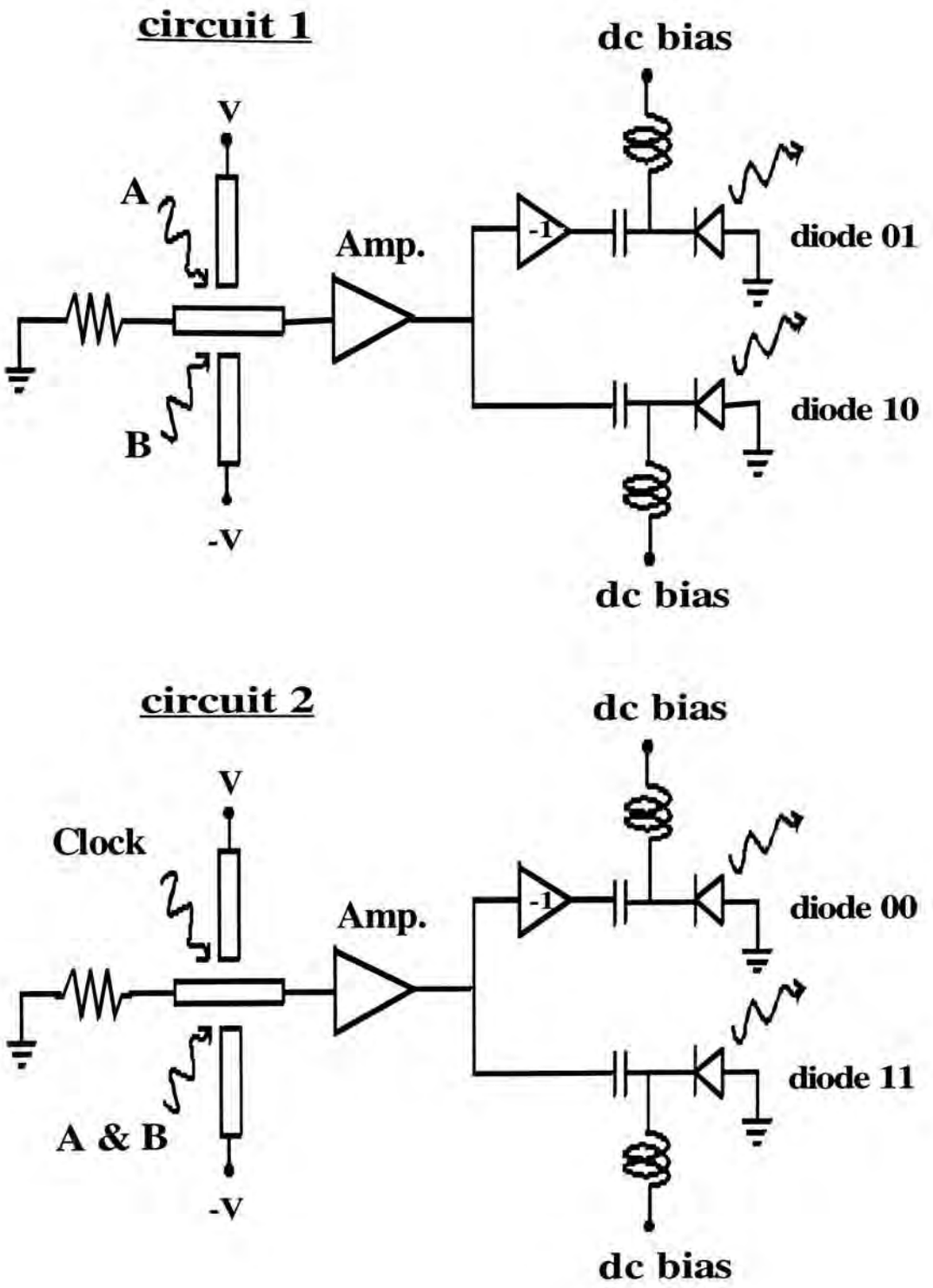


Fig. 6-15 Schematic representation of the 2 to 4 optoelectronic decoder

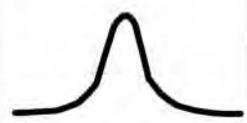
Input code	(0,0)	(0,1)	(1,0)	(1,1)
Electrical output from circuit 1				
Electrical output from circuit 2				
Optical output from laser diode 01				
Optical output from laser diode 10				
Optical output from laser diode 00				
Optical output from laser diode 11				

Table 6-7 Operation concept of the 2 to 4 decoder

6.4.3 Experiment and Result

In the experiment, optical inputs to the decoder are provided by the laser diode PPL50M. The average power of each beam is about 33 μW, except for the case of input logic (1,1). The bias voltages on the MSM photodetectors are ± 10 V. The device is fabricated by depositing 0.2 μm gold onto undoped semi-insulating GaAs substrate using the lift-off photolithography technique. The dimensions of the structure has been discussed in **Section 4**.

Electrical signals from the photodetector pairs are displayed in Fig. 6-16. The pulses obtained has an amplitude of 3 mV, a width of 370 ps, and an on-off contrast ratio of 10 dB. Note that there is no output from circuit 1 when circuit 2 produces a signal and vice versa. This ensures that one and only one laser diode would be activated at a given time. To achieve a good contrast ratio, optical pulse energy of the input beams and the clock beam should be the same. Otherwise, the cancellation will not be complete and it will result in some residual signals. In addition, the input signals should also be synchronized to guarantee a good cancellation. Electrical outputs as demonstrated for the case (1,1) are weaker due to a smaller incident optical pulse energy. It will be explained in more detail later.

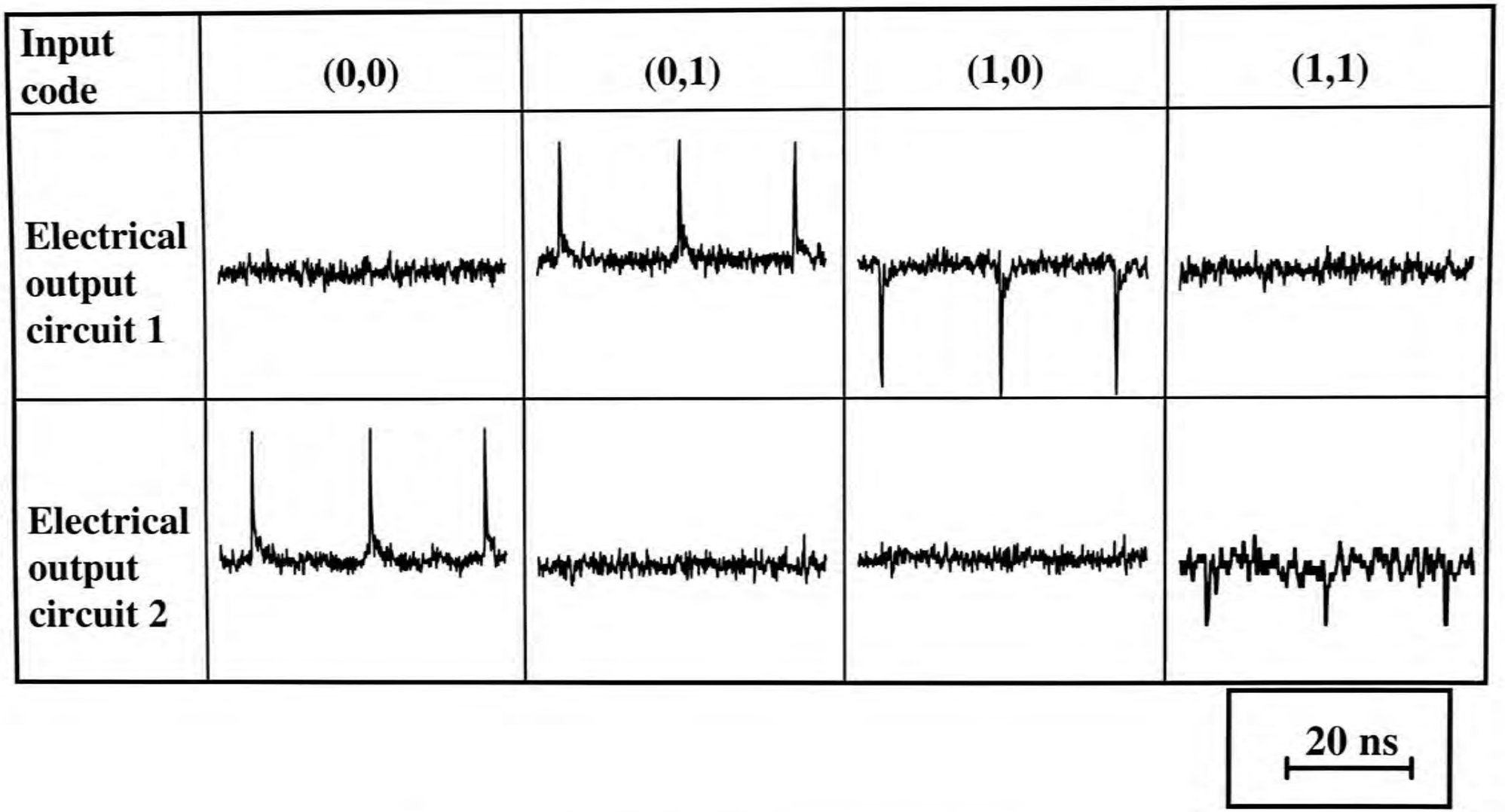


Fig. 6-16 Electrical output from the optoelectronic 2 to 4 decoder

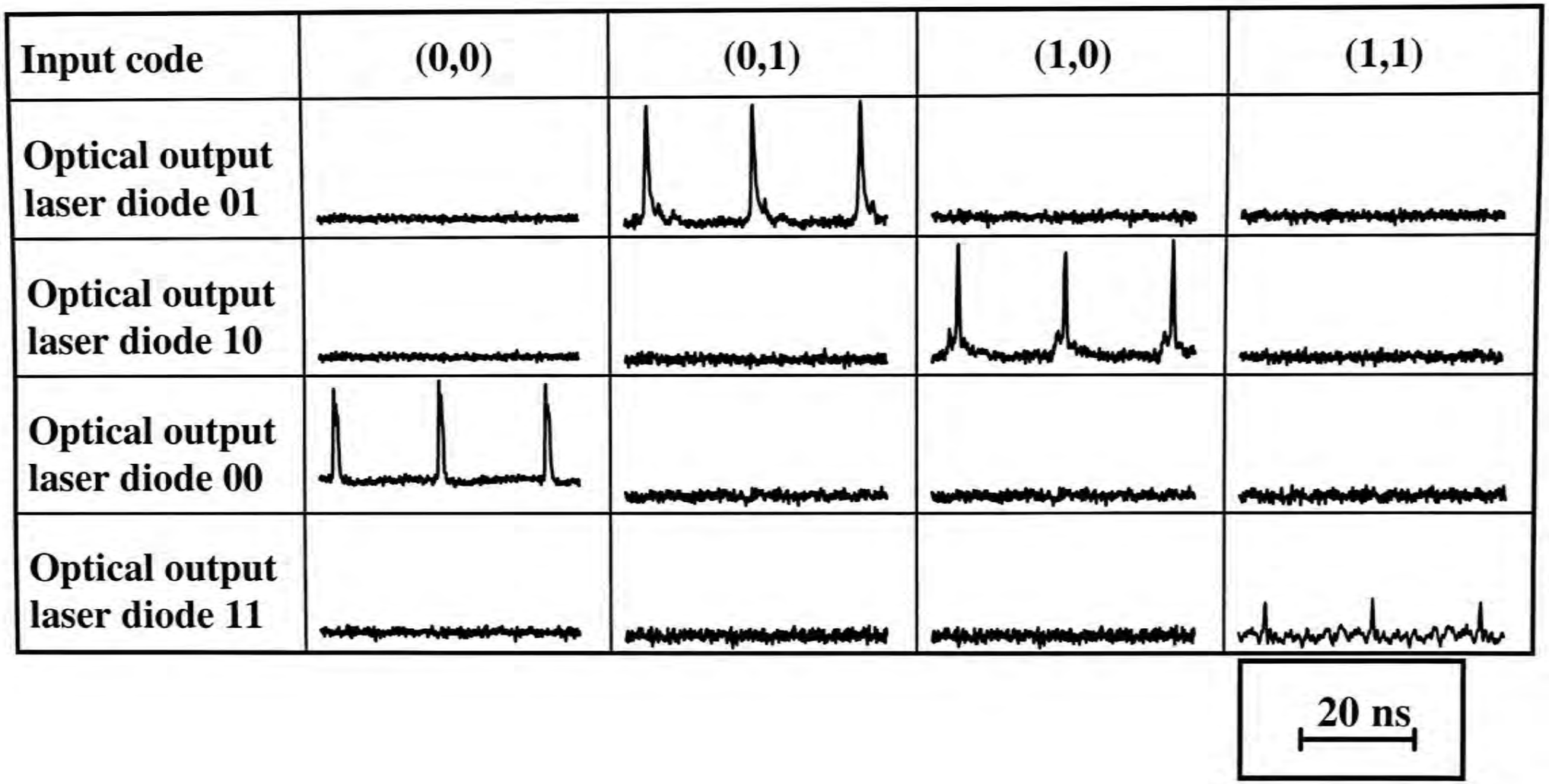


Fig. 6-17 Optical output from the optoelectronic 2 to 4 decoder

The electrical signals are amplified and are used to drive one of the several pre-biased AlGaAs/GaAs laser diodes to generate the decoder optical output. A dc bias of 38 mA is coupled with the amplified electrical signals from the photodetector pairs through a microwave bias-tee. The broadband pulse inverters in the circuits have a risetime of 20 ps. An output emission wavelength at 0.83 μm is obtained from the laser diodes. The light emitted is monitored with a high speed photodetector and a digital sampling oscilloscope. The results are displayed in Fig. 6-17. A striking improvement on the on-off contrast ratio is observed and is measured to be 17 dB. The pulses obtained have a width of 842 ps. The improvement in the contrast ratio is explained by the threshold characteristic of the lasing mechanism. On the other hand, broadening in the pulses is caused by the use of amplifiers with a limited bandwidth in the circuit. The amplified electrical signals have a width of about 850 ps after a total gain of 48 dB. When these broadened pulses are used to modulate the laser diodes, the optical pulses generated get a larger width than the original electrical signals.

For the cases of input logics (0,0), (0,1) and (1,0), three or fewer input beams are sufficient to demonstrate the results on the circuits. However, to investigate the response for the input logics (1,1), all the photodetectors have to be illuminated. Thus, a total of five input beams are needed. Subsequently the original laser beam has to be split one more time to provide enough inputs. As a result, the optical power is approximately half of the other logic inputs. It explains why the amplitude of the electrical and optical output signals are smaller for the case of (1,1). Owing to the linear response of the photodetectors in this range of optical power, the electrical signal is observed to be about half less than the other cases. The optical output, however, does not obey such linearity and the amplitude is found to

be much smaller. In practical applications, the input pulse energy should of course be identical for all combinations of the logics. The electrical and optical outputs for (1,1) will then have the same amplitude as the other cases.

6.4.4 Discussion

Although the two circuits are mounted separately in the experimental demonstration, they can in fact be fabricated monolithically onto a single substrate. The circuits are mounted apart in this work to facilitate optical alignment in providing the four input logic beams. When the circuits are fabricated on the same substrate, the reliability, the yield, and the compactness of the device are expected to improve significantly. An added advantage of using MSM photodetectors lies on their integrability with a variety of field-effect-transistors, which can then provide on-chip amplification of the signals and enhances the sensitivity of the decoder.

Owing to the combined effects of the intrinsic response of the output laser diodes, the limited bandwidth of some amplifiers used in the setup, and the parasitics of the decoder mounting fixture, optimum performance of this device has not been achieved. By using laser diodes with higher frequency bandwidth, shorter optical pulse signals can be produced. As discussed in **Section 6.2**, the number of amplifiers can be reduced by operating an input laser with a shorter wavelength to increase the photoresponse. Together with the incorporation of interdigitated MSM photodetectors [67] and better packaging, pulse width below 100 ps should be achievable.

The optoelectronic decoder is a cascadable device. Its optical output can serve as an input to other devices and circuits. It can be used as a

controller to determine which subsequent circuit is to be activated for further processing of the signals. The outputs are space-differentiated when the decoder is operated in this manner. On the other hand, they can be wavelength-differentiated by having the output laser diodes operating at different wavelengths. In this way, the output of all lasers can be coupled together into a single fiber and transmits over a long distance before it is used as an input to some wavelength-sensitive devices. Lastly, time-differentiated outputs can be achieved by coupling the signal from all output laser diodes into a single fiber with a pre-determined time delay between them. With such flexibility in the output wavelength and operating mode, its usage in optical signal processing, such as high speed optical addressing, will be highly desirable.

6.4.5 Summary

In summary, a cascadable high speed 2 to 4 optoelectronic decoder is demonstrated using two composite pairs of GaAs MSM photodetectors. Output response time shorter than 850 ps has been achieved with an on-off contrast ratio of 17 dB. The structure of our decoder is relatively simple and is ready for monolithic integration with other optical and electronic devices.

7 DISCUSSION

7.1 Improvements

1. Devices can be incorporated with coplanar waveguide structure to reduce dispersion of signals.

2. A layer of antireflection coating can be applied on top of the active regions to increase the amount of incident light absorbed by the photodetectors. The increased photoresponse can further improve the on-off contrast ratio.

3. Semiconductor substrate with smaller recombination lifetime, such as LT-GaAs, can be used to fabricate photoconductive switches to obtain faster response.

4. Interdigitated structure MSM photodetectors can be incorporated to decrease the response time of the logic devices. It is because the distance needed to be travelled by the photo-induced carriers decreases and results in a shorter transit time.

5. The size of devices can be reduced to decrease the energy requirement. In addition, miniaturization can reduce the capacitance and hence a smaller RC time constant. Moreover, small size also favours integration.

6. Instead of using silver paste, gold wire bonding should be used to achieve a better mounting to reduce the parasitics. Consequently, the response of the logic devices can be improved.

7. Bit generator can be used to generate random input bit pattern to facilitate the demonstration of the logic functions.

8. An input source with a shorter wavelength can be used to increase the photoresponse. The details have been discussed in **Section 6**.

7.2 Extensions of this Project

7.2.1 *Design and demonstration of a serial full adder*

Truth table of an adder

Without Carry :

Inputs		Outputs	
A	B	Sum (XOR)	Carry (AND)
0	0	0	0
0	1	1	0
1	0	1	0
1	1	0	1

With Carry :

Inputs		Outputs	
A	B	Sum (XNOR)	Carry (OR)
0	0	1	0
0	1	0	1
1	0	0	1
1	1	1	1

Table 7-1 Truth table of a full adder

An optoelectronic half-adder has been demonstrated by K. Nakajima et al [51]. It is an optical-input electrical-output circuit. The key element is two GaAs MSM photodetectors. The circuit is redrawn in Fig. 7-1.

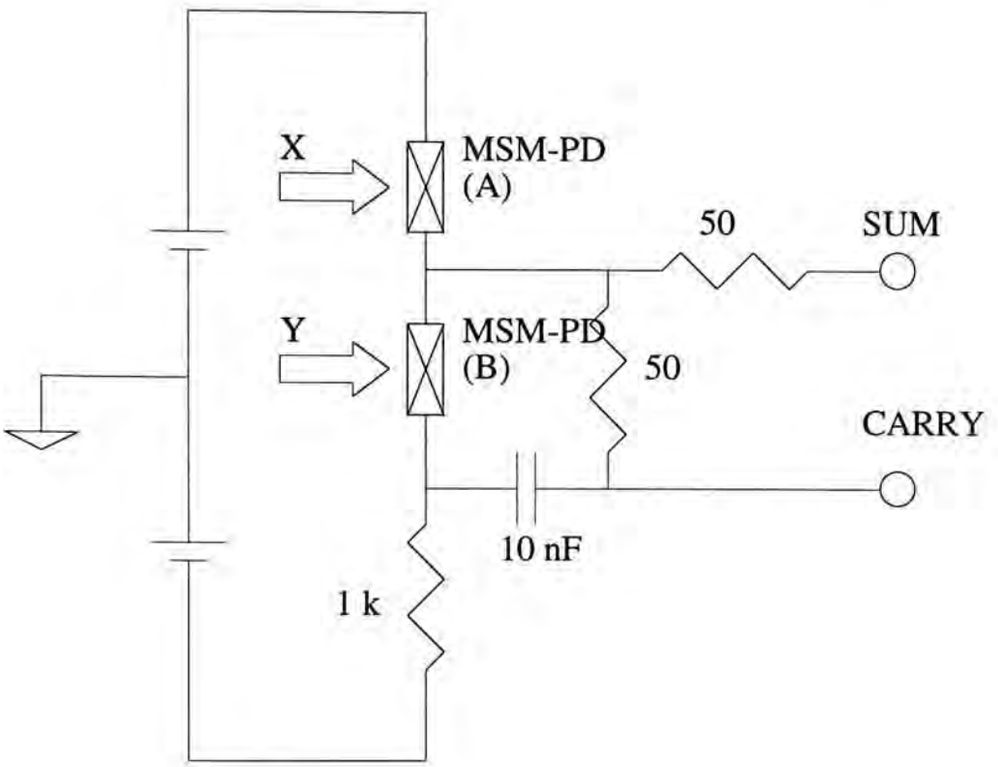


Fig. 7-1 Schematic diagram of a half adder

When a light pulse is launched at MSM-PD A, a positive pulse appears at both SUM and CARRY ports. When a light pulse is launched at MSM-PD B, a negative pulse is generated at the SUM port while a positive pulse at the CARRY port. While both positive and negative pulse are regarded as "1" for SUM, the threshold for CARRY is determined in a way such that a "1" is obtained only when both A and B are "1".

When there is no input, both SUM and CARRY will be "0". When A is "1" and B is "0", there will be a positive pulse at SUM which means "1", and a positive pulse at CARRY which is not high enough to be "1", and will be taken as "0". On the other hand, when B is "1" and A is "0", there would be a negative pulse at SUM which also represents "1", and a positive pulse at CARRY which is also not high enough to be "1" and is again taken as

"0". In the case when both A and B are "1", the positive pulse would be cancelled by the negative pulse which leads to a "0" at the SUM port. At the CARRY port, the addition of both small-amplitude pulses generates a large enough pulse which is regarded as "1". Thus 1 + 1 = 10.

Since the output logics for both SUM and CARRY are determined in a unique way in this design, the cascadability of this device is low.

A parallel adder has been proposed by H. Kamiyama et al. [50]. In the scheme, optical feedback is applied. The algorithm of this adder is shown below in Fig. 7-2.

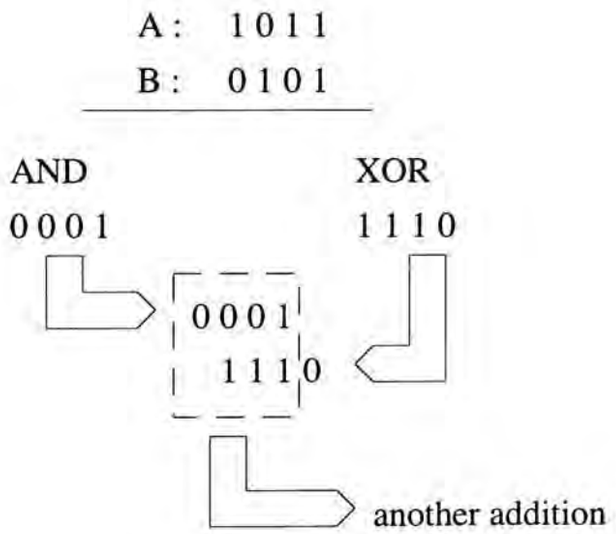


Fig. 7-2 Algorithm for a parallel adder

Referring to Fig. 7-2, it is assumed that the two inputs are 4-bit number. At the beginning, these two numbers are gone through two arrays, AND and XOR array. From output of the AND array, CARRY information is obtained and from output of the XOR array, SUM information is obtained. According to the principle of addition, the CARRY is left-shifted and then

added to the SUM. Therefore another addition is needed. This addition is performed again by this parallel adder by optical feedback. For 4-bit data, five feedbacks are required to produce a 5-bit results (4 for SUM and 1 for CARRY).

The schematic diagram of this parallel adder is shown in Fig. 7-3.

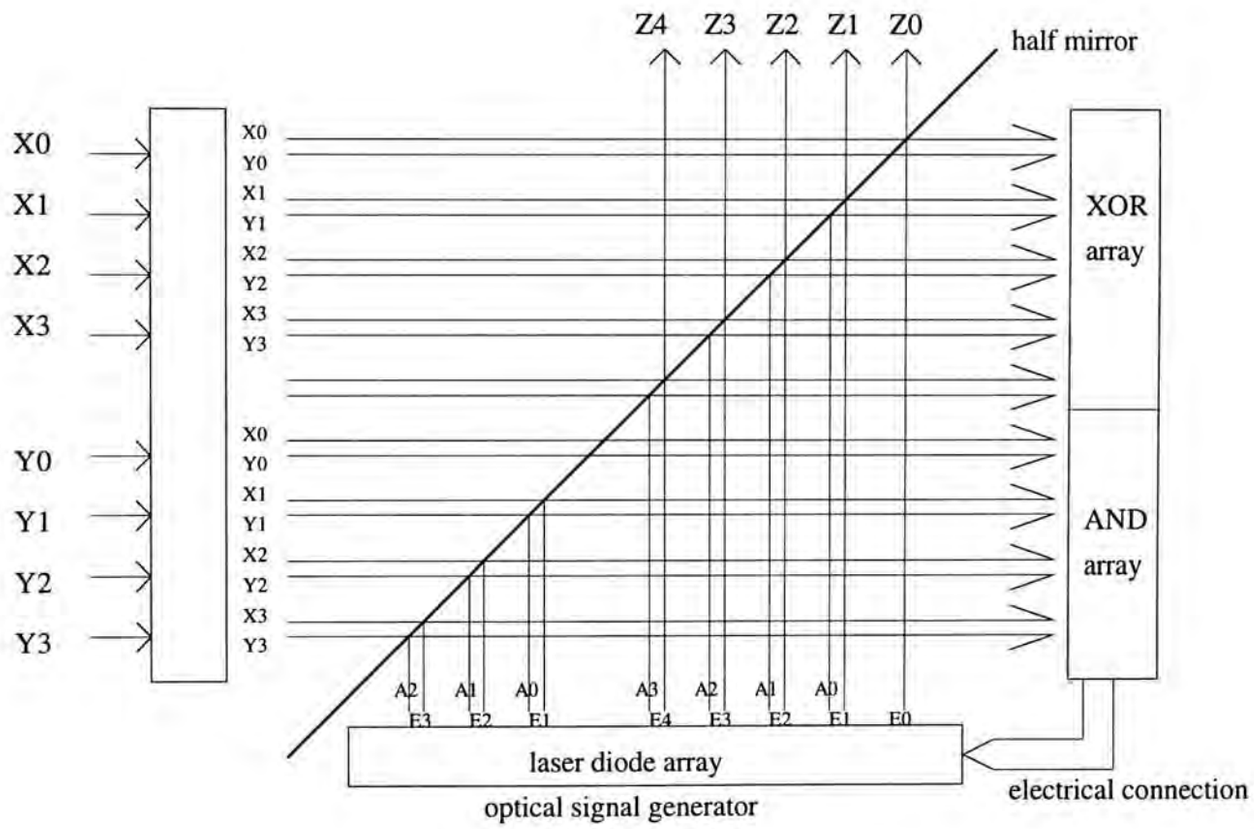


Fig. 7-3 Schematic diagram of the parallel adder

This adder is not cascadable. This means that a 16-bit addition cannot be realized by simply cascading four 4-bit adders. It is because this design takes no account of a CARRY IN signal. Since it is not cascadable, the number of element needed would be large when it is required to perform a more bit addition. For example, in a 16-bit addition, 16 AND gates, 17 XOR gates and

33 laser diodes are needed. As a result, it is not favourable to larger system implementation [68].

Here, a serial full adder is proposed. The concept and design are shown in Fig. 7-4 and Fig. 7-5, respectively. The adder consists of three circuits. They are the Sum-without-carry generator, the Carry generator and the Sum generator.

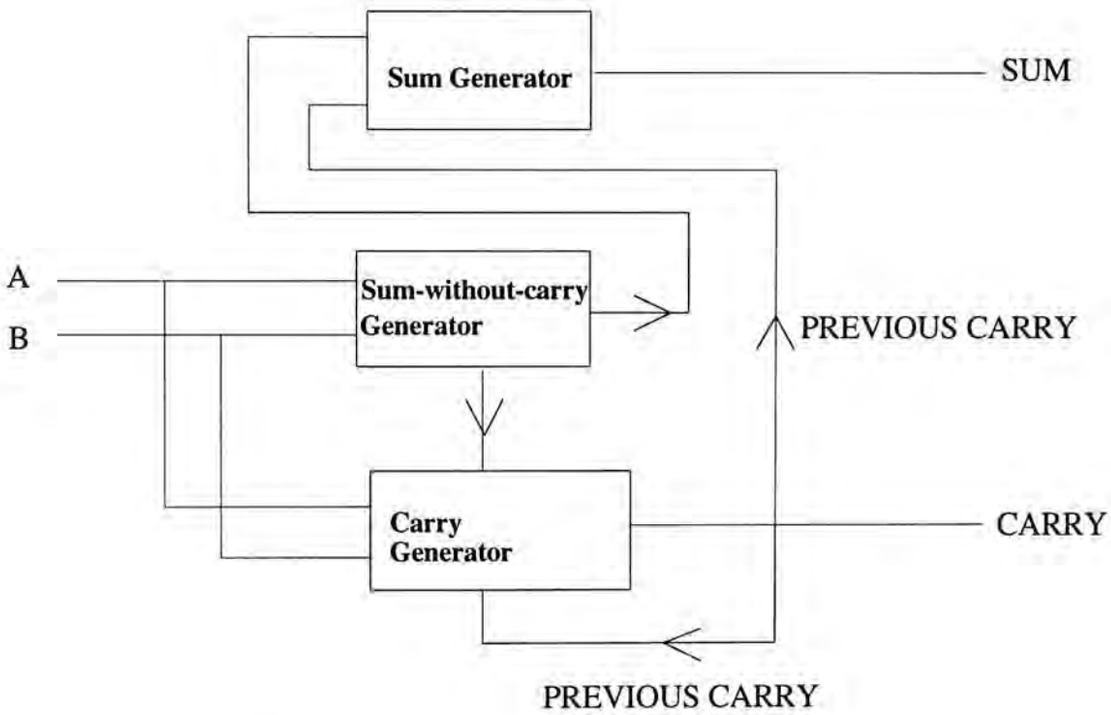
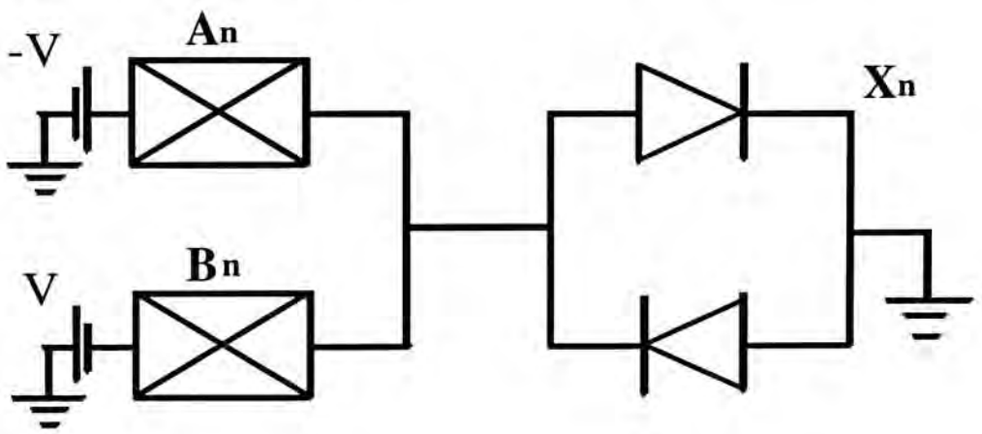


Fig. 7-4 Concept of the proposed serial full adder

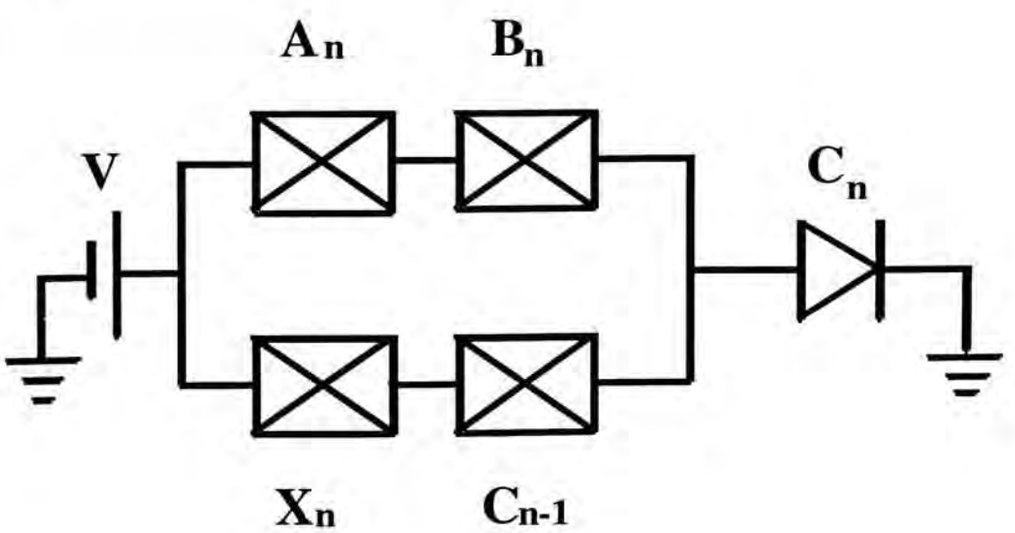
The Sum-without-carry generator is trivial. As shown in Table 7-1, it is essentially the XOR gate. For the Carry generator, it in fact performs the OR function of two AND operations. From table 7-1, a carry is generated either when *both* A and B are present or one of them is present *with* the previous Carry bit being "1". As a result, we have one branch performing $A_n \bullet B_n$ and another branch performing $X_n \bullet C_{n-1}$. It should be noted

that X_n is "1" only when A_n or B_n alone is "1". Then these two AND branches are connected together with an OR configuration. Finally, to take in consideration of the previous Carry bit C_{n-1} in determining the Sum bit X_n, the Sum generator has to be included such that the Sum bit will be inverted when the previous Carry bit is "1". This is because when the Sum of A_n and B_n is originally "0", the presence of the previous Carry will add the Sum to "1". On the other hand, when the Sum of A_n and B_n is originally "1", the addition of the previous Carry "1" will turn the final Sum to "0".

Sum-without-carry generator :



Carry generator :



Sum generator :

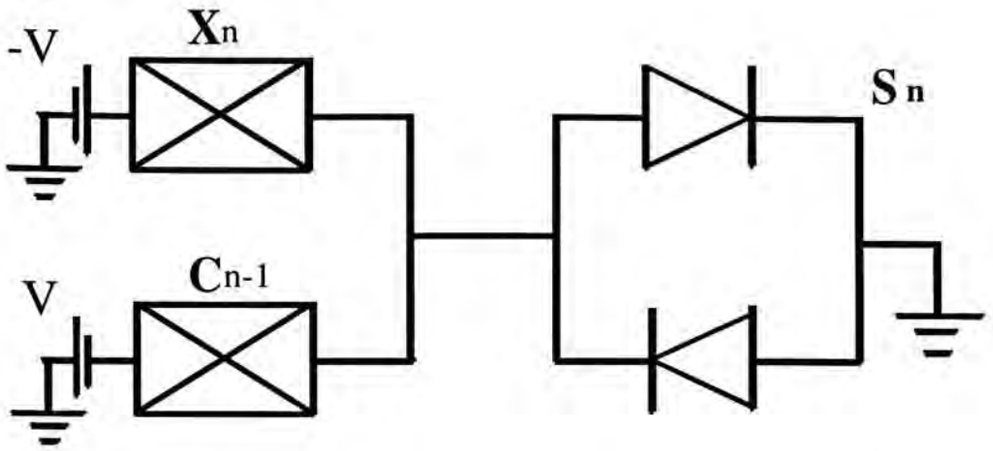


Fig. 7-5 Schematic representation of the circuits of the proposed serial full adder

For the carry generator, a larger amplification of the electrical output is required than the sum generators in producing the optical output. It is because the electrical signals generated from the carry generator originate from the photo-conductance of the two serial photodetectors, instead of one.

Since both C_{n-1} and X_n are required for the determination of C_n and S_n, careful feedback and clocking of the signals is needed. In addition, special algorithm is essential to extract the final Carry bit out to form the SUM with S_n's.

When compared with the parallel adder, this serial architecture has the advantage of involving a much smaller number of gates. This in turn suggests that the space required is also smaller. Moreover, in principle, it can perform addition of two words of any bit length. In other words, no change is needed in hardware implementation when the length of the input words is varied.

Since the area occupied by the proposed serial adder is much smaller, it can in fact perform some kind of parallelism. Several serial adders may be integrated into an array. The adder array can be arranged to process simultaneously under well control [68].

7.2.2 *Design and demonstration of a 3 to 8 decoder*

INPUTS			**OUTPUTS**							
A	***B***	***C***	**1**	**2**	**3**	**4**	**5**	**6**	**7**	**8**
0	0	0	**1**	0	0	0	0	0	0	0
1	0	0	0	**1**	0	0	0	0	0	0
0	1	0	0	0	**1**	0	0	0	0	0
1	1	0	0	0	0	**1**	0	0	0	0
0	0	1	0	0	0	0	**1**	0	0	0
1	0	1	0	0	0	0	0	**1**	0	0
0	1	1	0	0	0	0	0	0	**1**	0
1	1	1	0	0	0	0	0	0	0	**1**

Table 7-2 Truth table of 3 to 8 decoder

The 2 to 4 optoelectronic decoder discussed in **Section 6.4** can be modified to become a 3 to 8 decoder with some alterations in the circuit design.

First, the electrical outputs from each of the two circuits are split into four instead of two branches. One branch from each pair is allowed to pass through a pulse inverter. Each branch is then used to drive a pre-biased laser diode as before. One branch pair has a resistor R in series with it. Another branch pair, which is in parallel with the preceding one, has an additional MSM photodetector in series. The circuit modification and the truth table are shown in Fig. 7-6 and Table 7-2, respectively. Beam C is the third input to both circuits 1 and 2. It is split in the same manner as beams A and B. It controls the state of the third MSM photodetectors present in both circuits. These additional photodetectors act as selectors to route the amplified electrical signals to alternate pairs of laser diodes. When C is "0", the output will be generated from the laser diodes which are in series with the resistors R. When C is "1", the operating laser diodes will shift to those in series with the additional MSM photodetectors. A total of eight laser diodes serve as outputs of the device and only one of them will be activated at a given time.

To ensure a good contrast ratio, R should be chosen to be much smaller than the dark resistance of the additional photodetector but substantially larger than the detector resistance when it is illuminated. Since 3 to 8 decoder plays a very important role in electronic digital computing, it is believed that its development in the optoelectronic regime would also be crucial to optical computing.

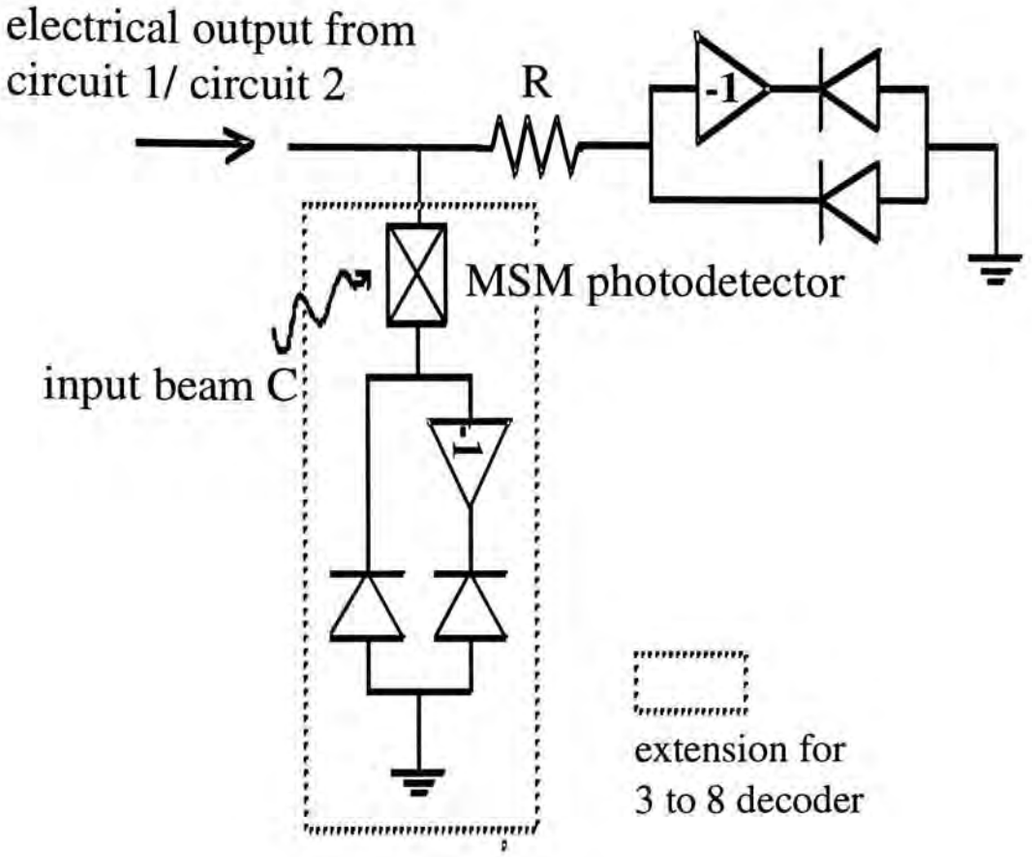


Fig. 7-6 Circuit modification for 3 to 8 optoelectronic decoder

7.2.3 *Design and demonstration of Memory Devices*

Having dealt with optical logic gates and being interested in binary optical computing, it is logical to consider flip-flops. In considering flip-flops, it is natural to develop the different types shown to be useful for various application in electronic circuitry [19]. For example, memory devices such as shift registers and counters are constructed from JK flip-flops. To implement these bistable devices, some kind of feedback has to be provided. As a result, special attention has to be paid to the timing of the beams and the fanout problem.

Processing of digital data often requires the capability to shift and rotate the data. A simple mechanism for realizing both operations is to devise a register whose content may be shifted, to the right or left, one bit position at a time. On the other hand, counters are useful in realizing ordinary counting functions as well as generating control and timing signals [66]. Since the ultimate goal to develop the logic devices is to implement an optical computer, the development of these memory logic devices is essential.

7.2.3 *Integrated interdigitated MSM photodetectors with VCSELs to perform logic devices*

This may be the most promising optoelectronic approach to implement an optical computer. It combines the advantages of the fast response of MSM photodetectors and also the inherent parallel, two dimensional optical access offered by VCSELs. The gain needed to drive the surface emitting lasers can be provided by field-effect transistors integrated monolithically with the MSM photodetectors and also the VCSELs.

7.3 Prospects and Limitations of this Approach

Although the devices demonstrated show very fast response, the use of electronic amplifiers have limited their speed and introduced time delay. This will ultimately make the devices face the problems of their electronic counterparts.

In order to eliminate the need of the speed-limiting amplifiers, we need light detection devices with large enough gain. Phototransistors and photothyristors have been used for this purpose. However, their speed performance has to be improved before they can be useful. Another possible candidate is avalanche photodiode. But the integration of the photodiodes with lasers is no easy task. As a result, significant progress in the fabrication technology has to be made for this approach to be practical.

8 CONCLUSION

In this research, a number of optoelectronic logic devices have been designed and demonstrated using high speed GaAs photodetectors for light detection. Two types of photodetectors have been employed. They are photoconductive switches and MSM photodetectors. Time response of the logic devices with them are similar, in the order of hundreds of picosecond. The speed demonstrated is among the fastest in the reported optical logic devices. Moreover, the devices also have a good contrast ratio, ranges from 6 dB to 19 dB. With an active area of 10 μm x 40 μm, the input energy is less than one pJ.

Apart from having a superior performance, the design of the devices is simple and results in a relatively simple fabrication. Logic gates including OR, XOR and XNOR have been achieved with the same basic structure. This favours batch fabrication and the cost can be lowered.

On the other hand, more complex logic devices have also been studied. A novel 2 to 4 optoelectronic decoder is designed and demonstrated. It will be useful in high speed addressing. In addition, a 3 to 8 optoelectronic decoder and a serial full adder have been proposed. They will be the essential elements in implementing an optical computer.

Although the demonstrated devices show a response time of hundreds of picosecond, fast switching below 100 ps should be able to achieve. It has been found that the signals have been broadened by low bandwidth

amplifiers from 250 ps to over 800 ps. These amplifiers can be removed from the setup using an input laser with a shorter wavelength that can produce a larger photoresponse. Thus, together with the incorporation of interdigitated photodetectors and better mounting, the response time can be substantially improved.

This approach of implementing logic elements has the advantage of allowing the devices to be monolithically integrated with other optoelectronic devices as well as the well-developed electronic circuits. For example, the devices can be integrated with field effect transistors to obtain signal gain. In this way, the amplified output can be used to drive vertical cavity surface emitting laser which is ideal in two-dimensional parallel processing.

On the other hand, these devices would ultimately face the same limitations of their electronic counterparts owing to the presence of amplifiers. As a result, light detection devices with large enough gain should be incorporated to eliminate the need of amplifiers.

In conclusion, the optoelectronic logic devices designed and demonstrated will be important in the development of optical computing and optical signal processing.

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Appendix I

List of Instruments

1. Lock-in Amplifier
   Standford Research Systems
   Model SR530

2. Optical Chopper
   Standford Research Systems
   Model SR540

3. Picosecond Fiberoptic System
   Opto-electronics Inc.
   Model PPL50M Pulse Diode Laser
   Model PFC50 Optical Fiber Coupler

4. Stepping Motor
   Klinger
   Model CC1.1

5. Optical Picowatt Power Meter
   Newport
   Model 835

6. High Speed Photodetector
   New Focus
   Model 1404
   Bandwidth : > 20 GHz

7. Communication Signal Analyzer
   Tektronix
   Model CSA 803
   Sampling Head SD-26
   Bandwidth : 20 GHz
   Sampling Head SD-30
   Bandwidth : 40 GHz

8. Electronic Infrared Viewer
   Optical Systems Inc.
   Model Find-R-Scope

9. Precision Current Source
   ILX Lightwave Corporation

Model LDX-3412

10. Dual Tracking DC Power Supply
Wembley
Model TPS-4303

11. Autoranging Multimeter
Keithley
Model 175A

12. Bias Tee
Picosecond Pulse Labs.
Model 5540
Bandwidth : 44 GHz

13. Bias Tee
Picosecond Pulse Labs.
Model 5555
Bandwidth : 17 GHz

14. Bias Tee
Hewlett Packard
Model 33150A
Bandwidth : 0.1 - 18 GHz

15. Inverting Transformer
Picosecond Pulse Labs.
Model 5100
Risetime : 20 ps

16. Broadband Amplifier
MITEQ
Model AFS4-00102000-65-LN
Bandwidth : 0.1 - 20 GHz
Gain : 16 dB

17. Amplifier
Mini-Circuits
Model ZFL-1000
Bandwidth : 0.1 - 1000 MHz
Gain : 17 dB

18. Variable Gain Amplifier
Mini-Circuits
Model ZFL-1000GH

Bandwidth : 10 - 1200 MHz
Gain : 17 dB

19. Compensated Attenuator
Newport
Model 925B
Aperture : 0.5 in. (12.7 mm)
Attenuation Range : 0.01- 3.0 ND
Attenuation Resolution : 0.02 ND
Wavelength Range : 440-690 optimal
400-1500 with reduced maximum transmittance
Safe Energy Level : 75W/cm^2 CW
10mJ/cm^2 pulsed

20. Objective Lens
Newport
Model-5X
Focal length : 25.5 mm
Working Distance : 15.0 mm
Numerical Aperture : 0.1
Model-10X
Focal Length : 14.8 mm
Working Distance : 6.0 mm
Numerical Aperture : 0.25
Model-20X
Focal Length : 8.3 mm
Working Distance : 1.9 mm
Numerical Aperture : 0.4

21. Long Working Distance Objective Lens
Olympus
Model ULWD MSPlan 20
Working Distance : 11 mm
Numerical Aperture : 0.4

22. 2x2 Multimode Fiber Coupler
Canstar
Model MR4

23. Three-axis precision stage
Klinger
Model

Appendix II

Properties of Semi-Insulating Gallium Arsenide (SI-GaAs)

(All values at 300K)

1.	Bandgap energy	: 1.43 eV
2.	Cutoff wavelength	: 870 nm
3.	Dielectric constant	: 13.2
4.	Melting point	: 1238 °C
5.	Resistivity	: 10^8 Ω-cm
6.	Thermal conductivity	: 0.46 W/cm-°C
7.	Mobility of electron	: 6500 cm^2/V-s
8.	Surface reflectivity	: 0.34
9.	Photosensitivity	: 0.25 A/W
10.	Quantum efficiency	: 35% at 850 nm
11.	Saturation elecron drift velocity	: 1x10^7 cm/s
12.	Absorption coefficient	: 3.6 x 10^4 cm^{-1}
13.	Absorption depth	: 0.28 μm
14.	Intrinsic carrier concentration	: 2 x 10^6 cm^{-3}

LIST OF ACCEPTED AND SUBMITTED PUBLICATIONS DURING THE PERIOD OF STUDY

[1] T. C. She, and C. Shu, "High speed optoelectronic exclusive-OR gate", *Electron. Lett.*, **30**, pp. 81-82, 1994.

[2] C. Shu, H. S. Choy, and T. C. She, "Optical control of polarity in short electrical pulses generated from coplanar waveguide metal-semiconductor-metal photodetectors", *J. Appl. Phys.*, **75**, pp. 8228-8230, 1994.

[3] T. C. She, and C. Shu, "Optoelectronic exclusive-NOR gate operating at 200 Mbit/s", *IEEE Photon. Technol. Lett.* (accepted for publication).

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[5] T. C. She, and C. Shu, "Optoelectronic logic devices implemented on GaAs photodetectors", *1994 Hong Kong Electron Devices Meeting*, **HKEDM'94**, July, Hong Kong (accepted for presentation).

[6] T. C. She, and C. Shu, "A high speed optoelectronic decoder", *IEEE J. Quantum Electron.* (submitted).