

AN INTEGRATED BROADBAND
CONCENTRATION/DISTRIBUTION NETWORK
FOR MULTIMEDIA APPLICATION COMPATIBLE
WITH THE HYBRID FIBER-COAX (HFC)
ARCHITECTURE

By

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A THESIS

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Abstract

A simple, low-cost, broadband (100-Mb/s) multimedia network is proposed for residential subscribers for provisioning of multimedia services over the existing tree-architecture coaxial cable CATV distribution system. A Fast Polling Protocol is employed to provide collision-free media access in the Media Access Control (MAC) layer. The protocol is based on the Binary Exponential Backoff Polling (BEBP) algorithm to improve the throughput efficiency and to guarantee the performance of connection-oriented isochronous services. The protocol is compatible with the Hybrid Fiber-Coax (HFC) architecture, which is a very promising architecture for bringing broadband services to the residential subscribers. Experimental demonstration has been performed based on the TAXI chip datalinks, and the performance in throughput, fairness and network access delay have been demonstrated satisfactorily. The proposed network can be used as a low-cost ATM traffic concentrator at the hub.

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Chapter 1

Introduction

Network has become part of our daily life. As Internet continues to grow exponentially in recent years in access speed, number of servers and number of subscribers, the information superhighway is no longer a dream. Internet access may be as simple as telephone access in a few years. But the network alone cannot provide everything, it needs a partner - multimedia information. Many multimedia information services has been provided on Internet in recent years, from simple still pictures to full multimedia documents with motion video and sound.

As in many other industries, the existing information infrastructure cannot satisfy every desire of the customers. Most of the existing networks cannot support multimedia services. In a campus or office environment, most of the available LAN solutions such as Ethernet and Token Ring can only provide around 10- to 20-Mbps of bandwidth. Network access for residential users is even worst. Most of them can only use a 14.4 Kbps modem line to retrieve information. There is a large market force to develop a low cost highspeed

network access for the end users.

1.1 Multimedia Network Requirement

The first requirement for multimedia services is large bandwidth. Most of the images, video and voice in multimedia service consume a lot of bandwidth. Although many compression algorithms have been developed successfully [1, 2, 28], the bandwidth required is still very large. For example, 1.5Mbps is required for MPEG-I, px64 Kbps is required by H.261 video conferencing for p frames per second. Experiments show that the existing Ethernet cannot support more than four MPEG-I simultaneously.

Another important requirement for multimedia service is real time guarantee. Services like video conferencing require the voice and video data to arrive in real time. Excessive delay will result in packet loss. CCITT specifies that the delay for voice cannot be larger than 25ms. Thus, the delay guarantee for real time packets is one of the major concerns in the design of a high speed multimedia network.

1.2 100-Mbps Network Proposal

Many high-speed network proposals have been suggested, such as the FastEthernet, ATM LAN [3, 4], Demand Priority MAC Protocol (IEEE 802.12) [5, 6], FDDI/CDDI[7], etc. Some are extensions of existing protocols, and some are new proposals.

FastEthernet (also called 100BaseT Ethernet) is the 100-Mbps version of

10BaseT Ethernet. It was designed to run on existing UTP Cat.5 cable plant without having to rewire the network. Although the specification for Cat.5 cable is 100m, only 50m can be reached in most FastEthernet products. Since the protocol still uses the CSMA/CD protocol, it cannot provide a guaranteed delay.

CDDI is the modified version of FDDI, which can run on copper wires. Both FDDI and CDDI follow the Timed Target Token Protocol. The protocol is more suitable for the provisioning of guaranteed service, but the delay can only be bounded to a relatively large value and the throughput performance depends on the round trip delay time of the network. This is the major drawback of using FDDI for multimedia services.

ATM provides a high-end and complete solution for multimedia networking. The small packet (53 bytes) can provide a very short network delay, but it creates a large protocol overhead. ATM was first suggested by telecommunication companies. As bandwidth scalability was the major concern, a large number of network vendors have designed ATM switching networks rather than shared media networks as have been done in most of the LAN environments. On one hand, switched networks can fully increase the bandwidth utilization of the network, on the other hand, it is not very compatible with Internet which is a connectionless network more suitable for shared media network. As a result, a lot of extra work has to be done to run IP and ARP on ATM [37, 38, 39].

The IEEE 802.12 Demand Priority MAC Protocol for the 100BaseVG - Any-LAN can run 100 Mbps on the existing UTP cable plants of 10BaseT Ethernet. Four pairs of wires have to be used to transmit the 100-Mbps traffic, so as to reduce the bandwidth required in each single pair of wires. Since the bandwidth

is shared by every node, it is difficult to guarantee a very small delay. So, different priorities are assigned to different connections. Higher priority traffic is served first in order to reduce the delay for real time services.

However, none of these proposed schemes is capable to work with the CATV tree architecture or the hybrid fiber-coax (HFC) architecture, which is a very promising architecture for bringing broadband services to the residential subscribers.

1.3 Broadband Network on HFC Architecture

There is a strong interest in the study of Hybrid Fiber-Coax (HFC) architecture for local loop distribution recently [8, 9]. First, the HFC architecture has abundant bandwidth which can also be made compatible to the existing analog TV system, thus allowing a graceful evolution and introduction of broadband services while supporting existing CATV customers. Second, the split and branch HFC architecture naturally serves as a traffic concentrator, reducing the number of cabling wires going into the hub offices of the service providers. Third, broadband interactive multimedia services can be provided on the HFC architecture very cost-effectively by subcarrier multiplexing. As such, the unification of this multimedia LAN proposal with the HFC architecture provides a low-cost, evolvable solution to the broadband, local distribution problem.

It is very important both technically and commercially to develop a new 100-Mb/s multimedia LAN standard that can work with a tree architecture so that residential end users can enjoy the broadband services through their existing cable.

1.4 The BEBP MAC Protocol

Based on the above consideration, a new multimedia LAN (Fast Polling MAC protocol) is proposed. It is compatible with the existing CATV network architecture and physical media. In order to improve the polling deficiency when the number of active nodes are small compared to the total number of nodes, a binary exponential backoff polling (BEBP) algorithm is proposed. Using such an algorithm, a high throughput and guaranteed delay multimedia LAN can be easily implemented over the existing CATV cable or the hybrid fiber-coax (HFC) architecture.

1.5 Scope of the Thesis

This thesis is separated into six chapters. Chapter 2 will go through all the important concepts and protocols of the proposed network. This include the fast polling MAC protocol, the BEBP algorithm and the Protocol Data Unit. A simulation evaluating the performance of the BEBP algorithm is presented in Chapter 3. Major factors affecting the performance of BEBP will be covered and evaluated in this chapter.

Chapter 4 will talk about the network architectures for the MAC protocol. Since BEBP is very flexible, it can be implemented on star, bus or ring networks with different physical media. Most of the issues in the chapter is on the compatibility of BEBP with the existing network wiring. Chapter 5 covers the design and implementation issues of the network. All the design of different layers will be covered in details, including the physical layer, MAC layer, network interface card, and software driver. The design of the hub and its integration with the

higher hierarchy network will also be found in this chapter. Finally, some of the testing results of the prototype will be reported. The final chapter will conclude this thesis.

Chapter 2

The MAC Protocol

In this section, the MAC protocol of the proposed multimedia network will be discussed. First, we describe various existing MAC protocols. Then we describe the proposed Fast Polling protocol which is a collision-free protocol that can guarantee real-time services over arbitrary network architecture.

Existing solutions on MAC protocol can be divided into three categories: random access, token passing and polling. The first random access MAC protocol was the Aloha proposed by the University of Hawaii [10]. It was then further developed to become the well-known Ethernet [11]. Additional algorithms, like “Carrier Sensing”, “Collision Detection” and “Truncated Binary Exponential Backoff” was later added to improve the throughput of the protocol, which is also called CSMA/CD. CSMA/CD provides a very simple and low cost solution for LAN connection, but it is never a good MAC protocol for high speed network. Collisions occur frequently at heavy traffic so it is difficult to guarantee service quality under those circumstances. This is also why CSMA/CD has a network access delay that is unbounded.

Token passing is another very popular MAC protocol. It can be implemented on a ring network like the FDDI[40] and the IEEE 802.5 Token Ring[32], or on a bus network such as the IEEE 802.4 Token Bus[31]. Fair access can be guaranteed even under high traffic, and the maximum delay is bounded. On the other hand, the protocol will become very inefficient when the number of active nodes is small. The token has to pass through all the inactive nodes before the active node gets the token to transmit. Another drawback of the token passing network is its large delay under high traffic. For example, the network access delay of FDDI can be as high as 8 ms, which is not suitable for multimedia traffic.

Polling is different from the above two MAC protocols for its centralized control over distributed control of the media. In a polling system, a central master called the hub control all the activities in the physical media. Polling systems have been used in many electronic systems for a long time, especially in the design of computer networks, and have been extensively studied by many researchers [12] [13]. However, there are two major limitations of the polling system.

First, a polling system requires very intensive communication between the hub and the nodes. The hub has to send out a lot of polling commands in order to control the traffic in the network. The polling commands are not very complicated but they have to be transmitted at all times. Most of the existing transceivers are not suitable for handling such short-length messages effectively. For example, in the Ethernet transceivers, 7 bytes of preamble has to be added in front of every packet in order to provide enough time for the receiver's PLL to lock onto the signal. If polling commands of only 10-bit length are used, then

a lot of bandwidth will be wasted on the preamble. Unless we can handle short-length polling commands effectively, polling system has a rather poor efficiency.

Second, traditional polling systems (such as the round-robin polling systems) share the same drawback as token passing systems. When the number of active nodes is small compared to the total number of nodes connected, the protocol will become very inefficient. The active nodes have to wait for the hub to poll all the inactive nodes before they are polled.

In the following section, we shall discuss a very effective polling system which can be implemented on the MAC layer with very high throughput efficiency. By using the state-of-the-art transceivers, short polling commands can be sent very effectively. Then we propose a new polling algorithm called the Binary Exponential Backoff Polling (BEBP) algorithm, which will provide a fair and efficient media access even when the number of active nodes is small compared to the total number of nodes.

2.1 Fast Polling Protocol

The Fast Polling Protocol is based on hub-polling to guarantee collision-free access. It is a simple “master-slave” protocol: the hub acts as the master which broadcast commands to every nodes, while the nodes act as slaves which respond to the commands accordingly.

For a general LAN architecture, we can assume the hub to have access and control of two shared media, one for uplink and one for downlink. The two media serve as concentrator and distributor of traffic respectively. This assumption is sufficiently general, because it covers the case of switched architectures as well

as multi-access architectures. The two shared media can be multiplexed onto the same physical media, for compatibility with architectures that employ only one single cable. Alternatively, half-duplex operation can be employed similar to IEEE 802.12.

For downlink, the hub simply broadcast any data packet and control messages to all the nodes. No scheduling issue has to be considered in the downlink transmission because the hub is the only sender. But in the uplink transmission, many senders may want to send their packets at the same time. So, a scheduling algorithm is required to resolve the multiple access problem.

Many polling algorithms can be implemented at the hub. However, the complexity and efficiency can be very different. First, we shall describe a very common and simple round-robin polling algorithm. Since the simple round-robin polling algorithm suffers from a poor throughput efficiency when the number of nodes in the network increases, therefore, we propose the Binary Exponential Backoff Polling (BEBP) algorithm to improve both the throughput efficiency and delay performance. Furthermore, the algorithm can also guarantee the service time of a connection-oriented isochronous service, which is very important for multimedia networks.

2.1.1 Round Robin Polling

Figure 2.1 and Figure 2.2 illustrate the polling events and timing for four nodes. Each node is assigned a unique polling address, node 0 to node 3. A data transfer cycle is started by the hub sending a "Poll Node 0" command to the downlink. If Node 0 does not have any packet to send, it simply ignores the command. Node 1 to node 3 will also ignore this command because the poll command is

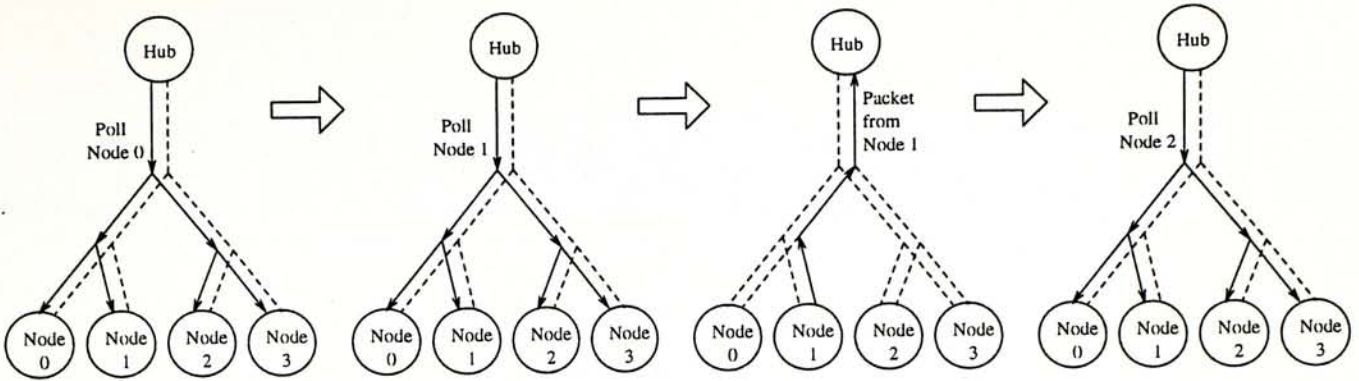


Figure 2.1: Polling Events of the Round Robin Polling

not addressed to them. Since the hub does not receive any data after a certain period t_{gu} , called the guard time, it can go ahead to poll the next node, which is node 1.

A “Poll Node 1” command is sent to the downlink. Now node 1 has a packet to send out, so it responds to the polling command by sending the data packet through the uplink immediately. This time the hub detects a packet arrival before the guard time has elapsed, so it will wait for the entire packet to be received completely. Thus it will wait for a packet transmission time plus the guard time ($t_{pkt} + t_{gu}$) before polling the next station, node 2. The same polling procedure applies to all nodes on a round-robin basis, before the polling comes back to node 0 again.

2.1.2 Binary Exponential Backoff Polling

As the number of nodes in the network increases, the efficiency of round-robin polling may be very low. This deficiency can be improved by the Binary Exponential Backoff Polling (BEBP) algorithm. The polling procedure is same as the round-robin polling, but the polling frequency depends on the activity of each node. An active node will receive more polls than those inactive nodes.

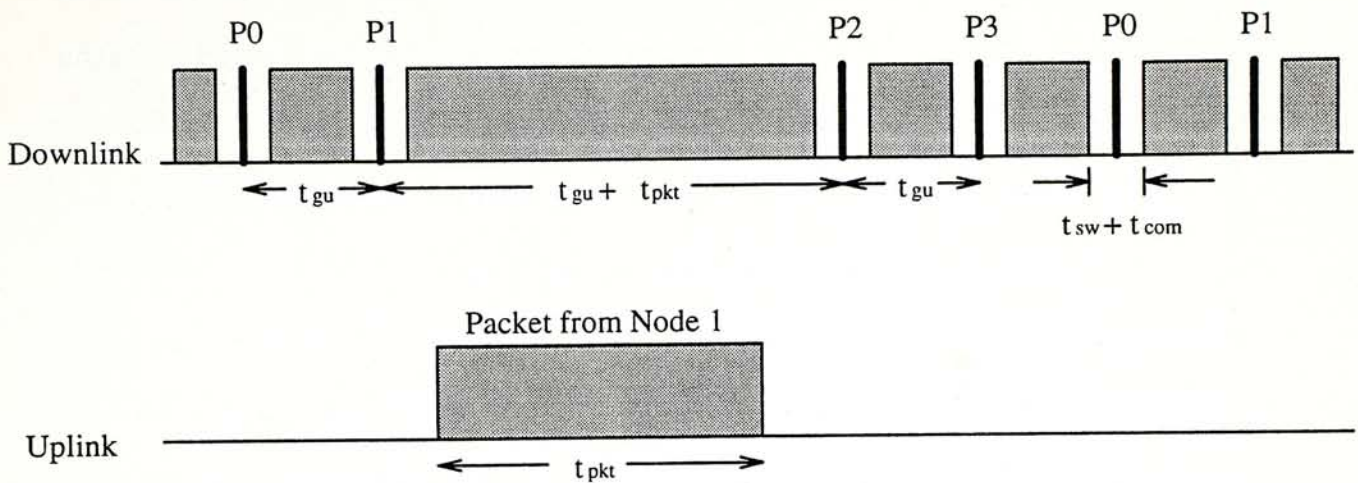


Figure 2.2: Timing of the Polling Events on the Downlink and Uplink

The BEBP algorithm is inspired by the truncated binary exponential backoff algorithm used in Ethernet and IEEE 802.3. However, unlike the latter, BEBP is collision-free, and only the polling frequency of a node depends on its activity in a binary exponential backoff manner. Only the master node (hub) needs to keep track of the activity information, all the other nodes (slaves) simply responds to the poll command as in the round-robin polling case.

The hub keeps two counters for each attached node, the wait level counter (WL) and the count down to poll counter (CDTP). In the beginning of a cycle, all the CDTP counters will decrease by 1. Those nodes with zero CDTP counter value will be polled in this cycle. The hub will send "Poll Node xxx" in the downlink for those nodes with zero CDTP counter value sequentially. According to the response from node xxx, the hub will update its counters. If no packet is sent back, the node's WL counter will be increased by one fold (binary exponentially increasing). If a packet is sent back by the node, the node's WL counter will be reset to the initial value, 1. In both case, the CDTP counter will change to the same value as the WL counter. The same procedure goes on for

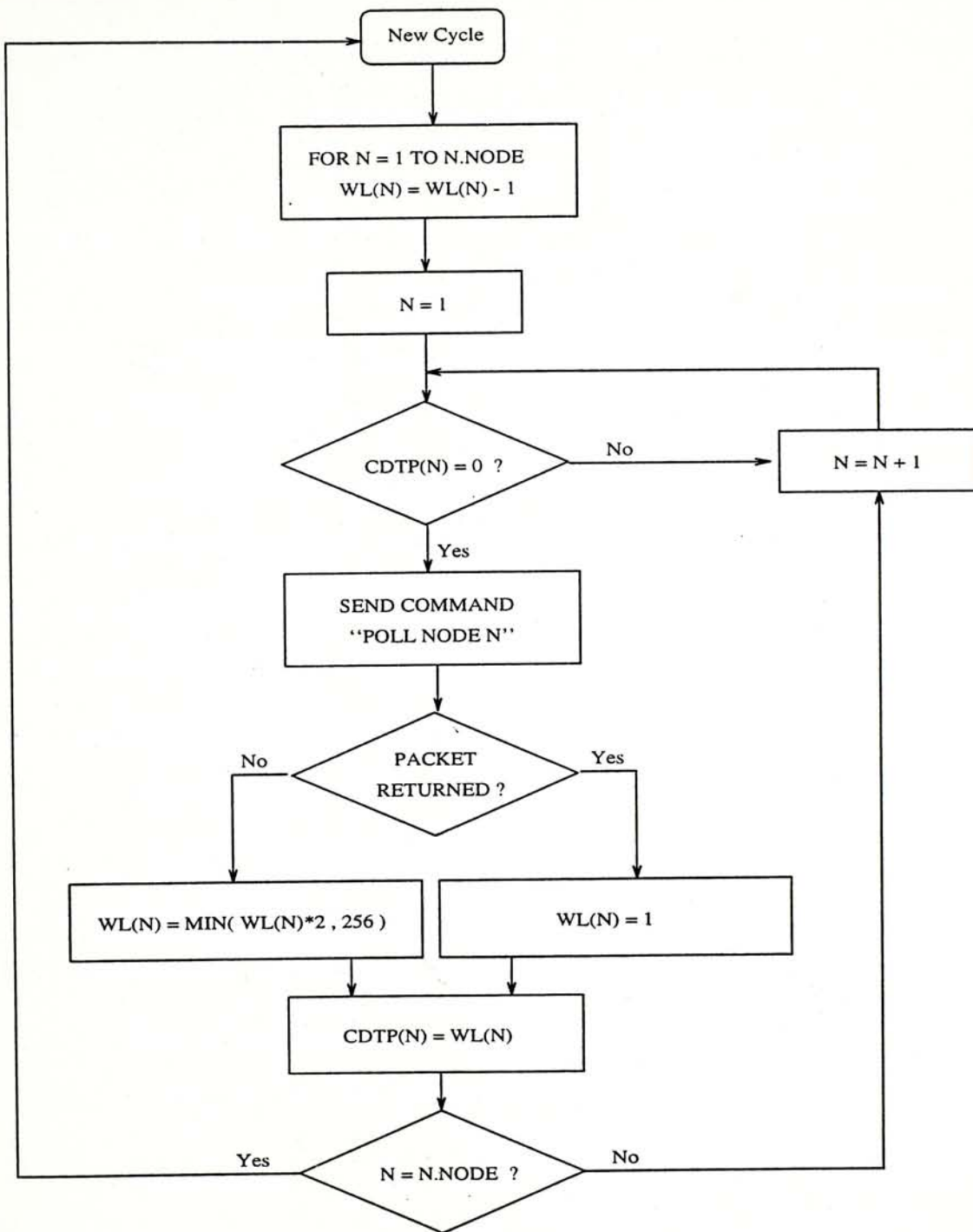
every nodes with zero CDTP counter value, then a new cycle starts. The flow chart in Figure 2.3 summarizes the procedure.

With this algorithm, if a node is active in the current cycle (i.e., the node has sent a packet), it will be guaranteed to be polled in the next cycle. On the other hand, if a node does not respond to a poll in one cycle, it will be skipped by the hub in the next cycle. If the node continues to ignore the poll addressed to it for n times, the hub will skip polling the node for 2^n cycles until a maximum number (e.g. 256) is reached. This algorithm also guarantees that an isochronous connection will be served in a definite period of time independent of the bandwidth of the connection.

The performance analysis of the round-robin polling and BEBP algorithm will be discussed in the next chapter.

2.2 Protocol Design

After an efficient MAC layer is built, the next task is to interface the MAC layer with the network layer. To simplify our demonstration, we choose to support only the most common network protocol, the Internet protocol, rather than providing the most generic design to support all possible network protocols. Thus, the design of the MAC layer supports IP packets directly. In order to have a better understanding of our MAC layer design, we will go through the MAC design of IEEE 802 LAN and Ethernet first.



N.NODE = Number of Node in the Network
 WL(N) = Wait Level Counter of Node N
 CDTP(N) = Count Down To Poll Counter of Node N

Figure 2.3: Flow Chart of the BEBP Algorithm

2.2.1 Lessons learnt from IEEE 802 LAN and Ethernet

Figure 2.4 shows the IEEE 802.2 LLC layer [29] and 802.3/4/5 MAC layer [30] [31] [32] Encapsulation. All the 3 different MAC protocols use the same LLC layer for compatibility. The design of the LLC is based on HDLC, which is a very reliable MAC layer protocol.

There are two reasons for splitting the MAC layer into two sublayers. First, it provides the flexibility for the users to choose different media for the network (different MAC) but sharing the same interface to the higher network layer (same LLC). Another benefit is to simplify the design of bridges among different 802 LAN. Bridges can operate in the LLC layer rather than in the network layer as most of the gateways do. The standard is widely accepted and has already been used by other LAN/MAN standard, e.g. FDDI.

Ethernet is a variant of the IEEE 802.3 and it can be compatible to IEEE 802.2 LLC. However, Ethernet is not equivalent to IEEE 802.3. As shown in Figure 2.5, Ethernet is different from 802.3/802.2 for the MAC layer encapsulation. The complete MAC layer header of 802.3/802.2 consists of 22 bytes (14 in MAC and 8 in LLC), while there are only 14 bytes in the Ethernet MAC layer. Both standards are accepted by the Internet Community as RFC1042 [36] and RFC 894 [35] respectively. Although the 802.3/802.2 encapsulation is well defined, the Ethernet encapsulation is most commonly used. Detailed description can be referred to the two RFC documents.

Direct encapsulation of IP over Ethernet becomes so common that the LLC has seldomly been used. In most cases, the IP packet is directly encapsulated by the Ethernet header (usually called the hardware header). As a result, the IEEE 802 bridge cannot work on the LLC layer because Ethernet does not use

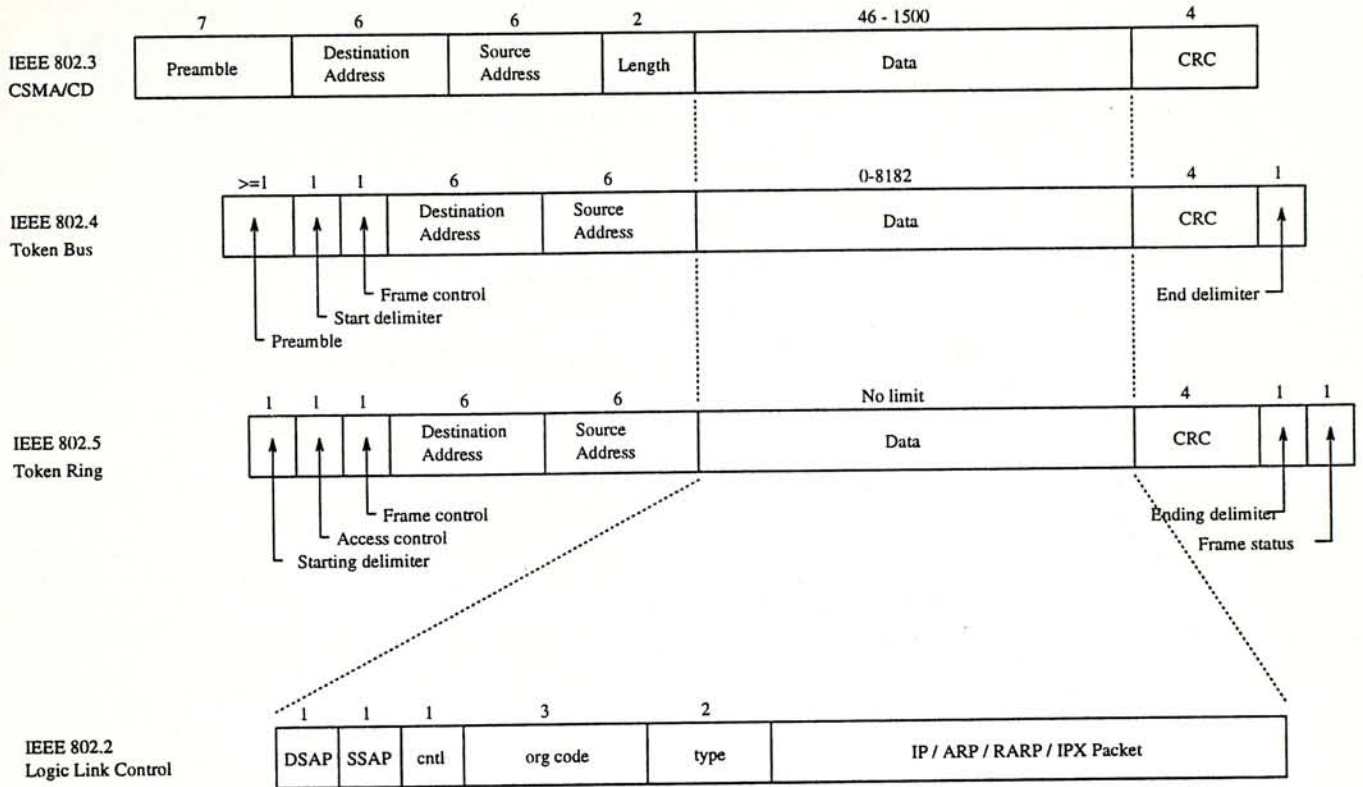


Figure 2.4: Encapsulation of the IEEE 802.2 and 802.3/4/5

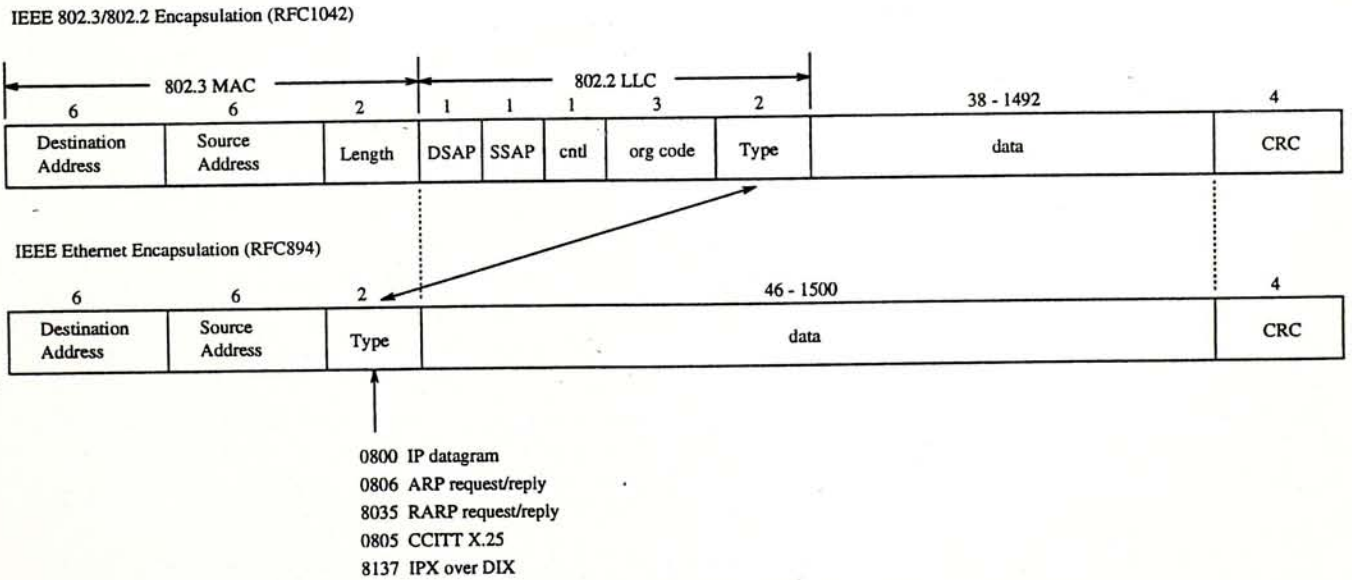


Figure 2.5: Ethernet and 802.2/802.3 Encapsulation

the 802.2/802.3 encapsulation. Bridging between two LANs (where one of the LANs is Ethernet) is usually done in the network layer by the IP gateway. The common LLC becomes an overhead to the 802 LAN.

There is a big lesson learned from the story of Ethernet and IEEE 802.2 / 802.3. First of all, the splitting of the MAC layer may not be necessary. Second, a simple MAC layer is very reliable in a LAN environment. Third, careful inspection of the Ethernet header will discover that the source address in the hardware header is never used. The protocol can work without this field.

2.2.2 Protocol Data Unit

In the design of the MAC layer based on BEBP, the following requirements are in mind:

- The protocol should be as simple as possible, so as to reduce the overhead.
- The MAC and physical layers are very reliable, with BER less than 10^{-9} .
- Only IP packets are carried in the network.
- The IEEE 802.2 LLC is not supported.

In order to have an efficient MAC layer, we choose to use fixed size packet. Fixed size packet can provide a better management in the polling, because the hub can always wait for the same time interval for a packet to return from the node before polling another. Also the length field used in the Ethernet header can be discarded. As discussed in the previous section, the source address is usually not used for routing, so the protocol data unit (PDU) does not contain the source address in the header.

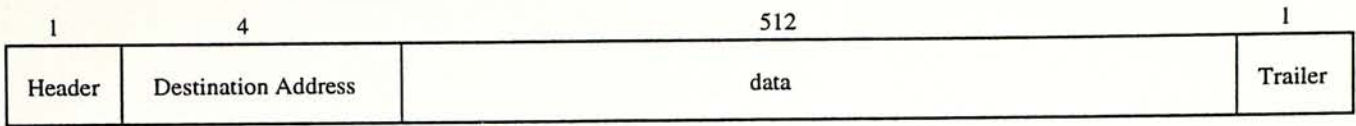


Figure 2.6: The BEBP 512+6 Byte Packet

Since only IP packets are carried in the network, the TYPE field like that in the Ethernet header will not be needed in the PDU header. With only IP packets, different hardware address and IP address become a redundant design. So, we use the unique 4-byte IP address to replace the hardware address. As a result, ARP is no longer necessary in our network design.

The PDU is shown in Figure 2.6. The DATA field is set to be a fixed size of 512 bytes, but different sizes can be used. Further discussion on the packet size will appear in Section 3.6. Together with a one-byte HEADER, a 4-byte DESTINATION ADDRESS and a one-byte TRAILER, the complete packet size is 512+6 bytes.

The design of the 512+6 byte packet format is fully compatible with the CUMLAUDE NET designed by the Chinese University of Hong Kong [15] [16]. The integration of the hub design with the CUMLAUDE NET will be discussed in Section 5.4.1.

Chapter 3

Performance Analysis

In order to have a better understanding of the BEBP algorithm, a simulation is performed to study the performance. The simulation is based on the Simscript simulation language [43]. A detailed description of the simulation model and the program will be covered in the first section. Then the performance of the round robin polling and BEBP will be compared. Afterward, the performance of BEBP with different number of nodes connected (at different network size) will be analyzed. Finally, the different system parameters that affect the BEBP performance will be discussed: including the TxFIFO size, the host bus transfer time and the packet size.

3.1 The Simulation

In the simulation, N nodes are connected to the hub, of which some are idle and some are active. The network data rate is 100 Mbps, and the packet size is assumed to be 518 bytes.

The Simscript source code of the simulation is attached in Appendix B. The program consists of PREAMBLE, MAIN and 6 processes. Declaration and initialization is done in PREAMBLE and MAIN. Two of the processes, STOP and INFO.COLLECT, are used for the collection and presentation of the simulation results. The other four processes will be described in the following sections. In the following description, a character string enclosed by [] represents the variable used in the Simscript program.

PACKET.GENERATOR Process

The packet generation algorithm tries to emulate a UNIX machine transmitting IP packets. The IP packet generation by the host machine is assumed to follow an exponential distribution with deviation equals to 1. Arrival statistics for other special application, like an MPEG video connection, FTP, or a WWW connection can also be simulated, but they will not cover in this thesis.

When the UNIX workstation has a packet waiting to be sent, the IP layer will call the network device driver (for detailed operation please refer to Section 5.5). The driver will first check the status of the transmit FIFO [PACKET.QUEUE] (TxFIFO) in the Network Interface Card (NIC). If the TxFIFO has already been filled by packet(s), the driver will reject the call from the IP layer. The IP layer will then buffer the unsuccessfully transmitted packet in its kernel buffer (mother board RAM) [IP.BUFFER]. It will then retry periodically every 50 μ s [IP.POLL.TIME] until the IP packet has been successfully transmitted. The kernel buffer [MAX.IP.BUFFER] is assumed to be able to store 200 packets, then it will kill any extra in-coming packets.

PACKET.TRANSFER Process

If the TxFIFO is not full, whenever the driver is called by the IP layer, a packet will be transferred from the kernel memory to the TxFIFO. The time required by this transfer is called the host bus transfer time [PACKET.TRANSFER.TIME], which is a very important factor in the actual system behavior. Unless the packet has completely arrived at the TxFIFO, it is not allowed to leave the NIC even if the node has received a poll. This is to guarantee the continuity of the packet burst in the link (see Section 5.3).

NODE Process

After the packet has been completely passed to the TxFIFO, it will be queued in the NIC according to a First-In-First-Out basis. It has to wait for all the packets in front of it to leave the NIC before it gets a chance to leave. The time between when the packet first entered the TxFIFO and when it arrived at the top of the TxFIFO is called the FIFO queuing delay [QUEUE.DELAY]. When a node gets a poll, the packet at the top of the queue will be transmitted and the packet will disappear from the simulation. The time between when the packet arrived at the top and when it actually left the NIC is called the network access delay [ACCESS.DELAY]. Figure 3.1 gives a more clear illustration.

HUB Process

The BEBP algorithm described in the previous chapter is implemented in this process. For each nodes, the hub will keep a Wait Level Counter [WAIT.LEVEL] and Count Down to Poll Counter [WAIT.COUNT]. If no packet is returned, the hub will wait for t_{gu} [POLL.SHORT.INTERVAL]. If a packet is returned before

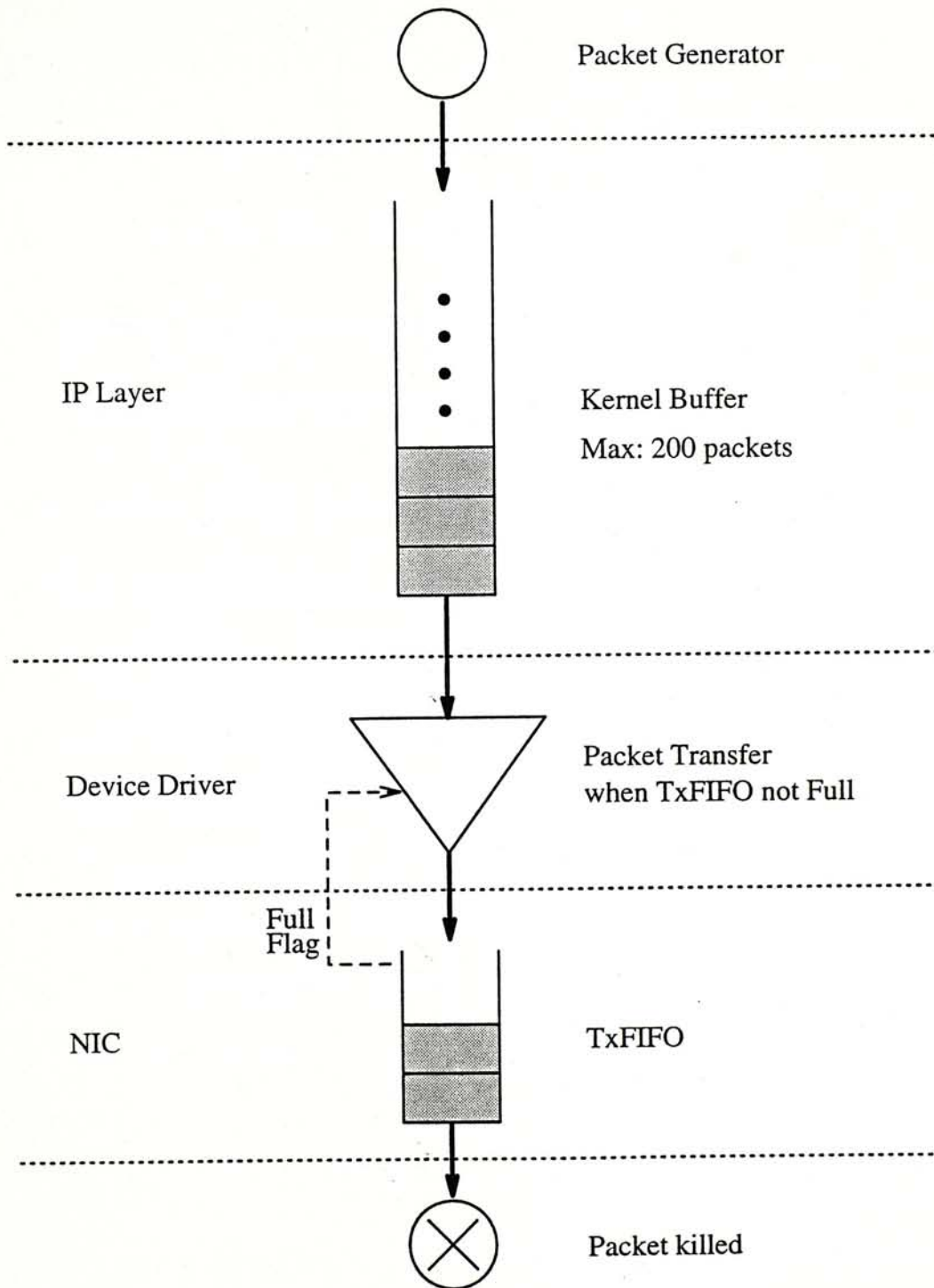


Figure 3.1: Diagram illustrated the Packet Generation Model

t_{gu} elapsed, the hub will wait $t_{gu} + t_{pkt}$ [POLL.LONG.INTERVAL] before polling the next node.

PREAMBLE and MAIN Routine

Input parameters to the simulation include:

- The number of nodes connected [N.NODE],
- The number of active nodes [NUM.ACTIVE.NODE],
- The offered load [OFFERED.LOAD],
- The host bus transfer time for one packet [PACKET.TRANSFER.TIME],
- The Tx FIFO size [FIFO.SIZE].

The offered load is defined to be the ratio of the total traffic arrival rate from all active nodes relative to the total network capacity. For example, if the network capacity is 100 Mb/s, an offered load of 1 means that the total data arrival rate from all the active nodes is 100 Mb/s. Host bus transfer time is assumed to be zero, while the Tx FIFO is assumed to be 1K bytes, which can buffer one 518-byte packet. Simulation time [END.TIME.SEC] is 1 second, which corresponds to about 15 minutes of running time in a Sun Sparc 10 machine.

Other system parameters include:

- the sampling time for the collection of statistics [SAMPLING.TIME],
- the packet size [PACKET.SIZE],
- the maximum throughput of the network [MAX.THROUGHPUT],

- the maximum value of the Wait Level Counter [MAX.WAIT.LEVEL],
- the maximum IP buffer size [MAX.IP.BUFFER],
- the IP layer retry period [IP.POLL.TIME].

The raw simulation results with different parameters are attached in Appendix C. They are summarized in the following sections.

3.2 Round Robin vs. BEBP

In the simulation, we assume that the average distance between the hub and all the nodes is 100 m, which corresponds to a round-trip delay time of 1 μ s. A guard time t_{gu} of 2 μ s would be very safe. The processing delay at the hub and node must also be considered. Usually, it is less than 1 μ s. Assuming the packet size to be 518 bytes, the packet transmission time t_{pkt} is 41.44 μ s in a 100-Mb/s network.

Throughput Analysis

The simulation result of the round robin polling is show in Figure 3.2. As shown in the figure, the total throughput of the network can be very high (95%) when all 64 nodes are active. This figure can be easily verified by simple calculation. If every node has a packet to be transmitted in every poll, the total throughput is:

$$throughput_{best} = \frac{t_{pkt}}{t_{pkt} + t_{gu}} = 95\%$$

But in actual practice, the number of active node is usually much less than the total number of nodes, in which case the efficiency would be very low. In the

worst case, when there is only one station transmitting packets in the uplink, the active node has to wait for the hub to poll all the other 63 nodes after sending one packet before it receives another poll again. So, the throughput of the uplink is equal to:

$$throughput_{worst} = \frac{t_{pkt}}{t_{pkt} + 64 \times t_{gu}} = 24\%$$

For the downlink, the polling protocol only affects the bandwidth minimally. In the worst case, when there is no packet to be transmitted, a polling command has to be sent every $2 \mu s$, the guard time. To insert a command in the downstream data, the hub has to switch off the downstream data temporarily by buffering the packet. The switching time (t_{sw}) is typically less than 200 ns for High speed CMOS / TTL technology. Another 100 ns for command transmission (t_{com}) is required to transmit the one byte command. Therefore the worst case efficiency for the downlink is about:

$$throughput_{down} = \frac{t_{gu} - t_{sw} - t_{com}}{t_{gu}} = 85\%$$

For the BEBP, the result is shown in Figure 3.3. As shown, nearly all the curves approach the ideal curve with all the 64 nodes are active. Even with only one single node is active, throughput of over 70% still can be reached. BEBP eliminates the major drawback of polling system: the same throughput can be retained even when the number of active nodes is small. Comparing with the traditional CSMA/CD, BEBP is superior. There is no collision over the media, all the resources (bandwidth) are scheduled on demands. Overhead occurs only in the propagation delay (the guard time), which has been shown to be smaller than a few percent of the total bandwidth. But in the CSMA/CD,

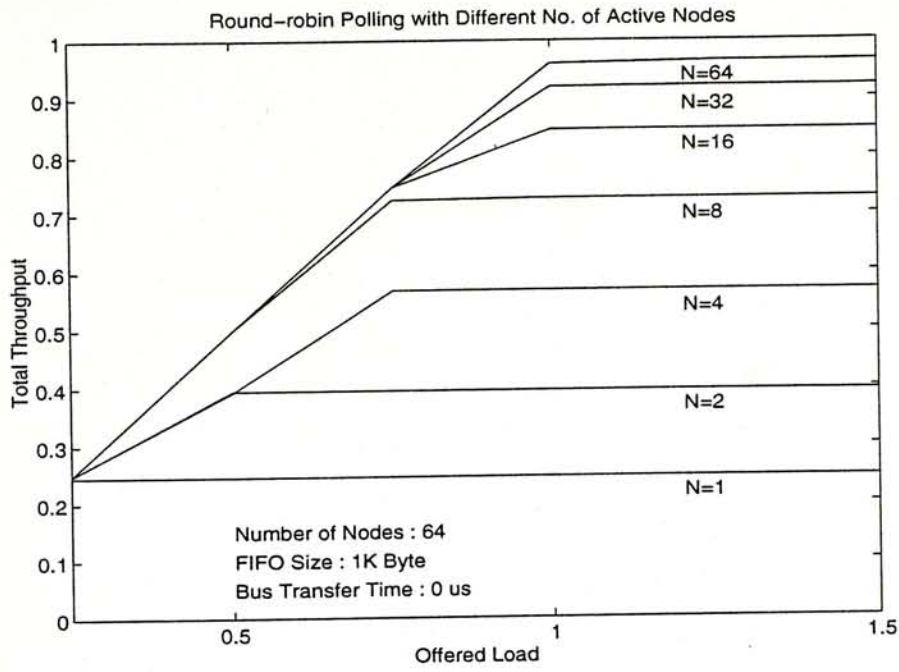


Figure 3.2: Throughput of the Round Robin Polling Algorithm

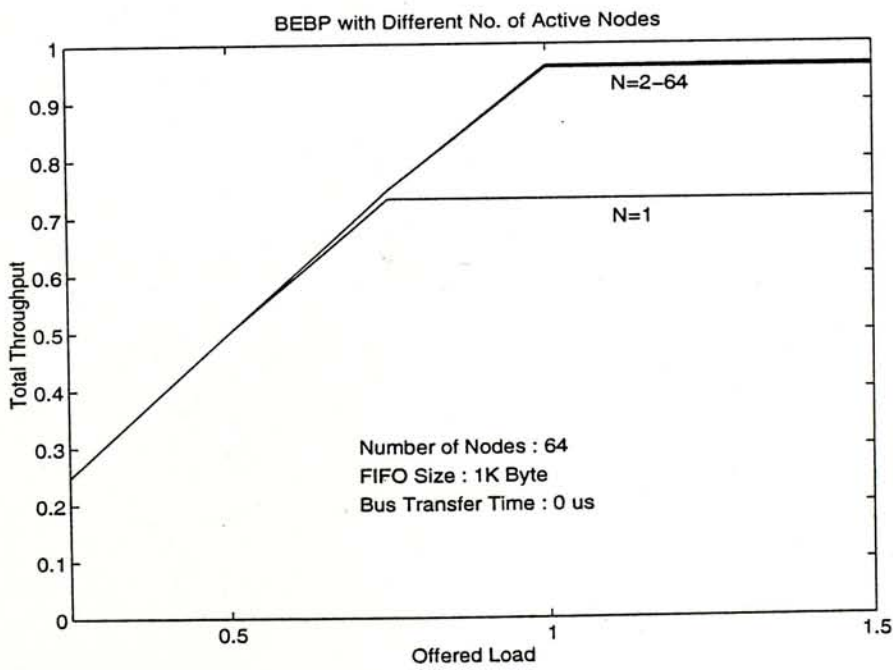


Figure 3.3: Throughput of the BEBP Algorithm

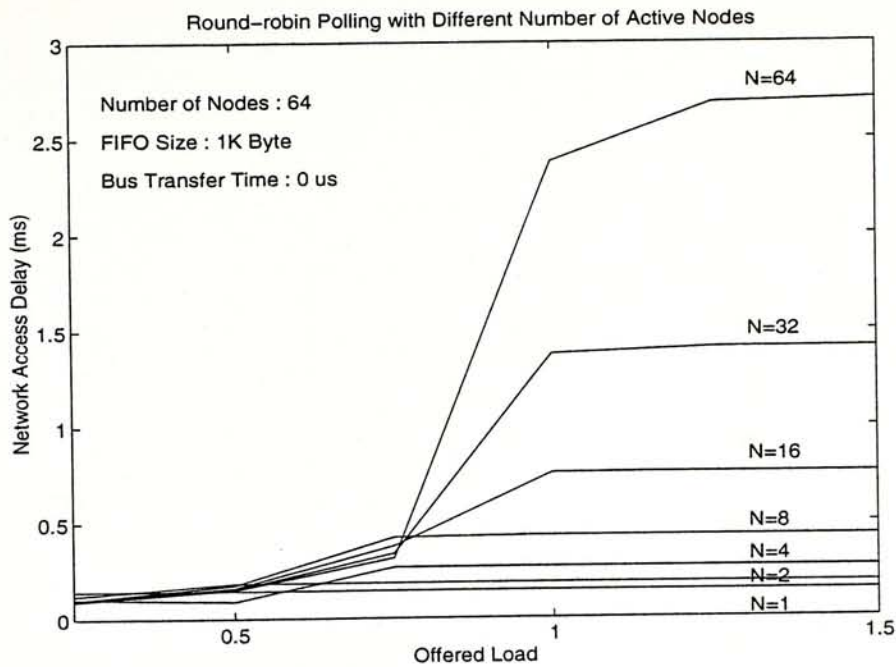


Figure 3.4: Access Delay of the Round Robin Polling Algorithm

the throughput drops significantly when the offered load and number of station increases

Network Access Delay Analysis

It is also very important to provide guaranteed network access delay for multimedia networks. Delay in round-robin and BEBP algorithm is fair and guaranteed since every node suffers the same delay. The simulation results for round-robin and BEBP showing the average network access delay of a packet is presented in Figure 3.4 and Figure 3.5 respectively. No significant difference found between the two algorithms.

Under normal traffic (offered load < 1), the access delay is below 1 ms even many nodes are active (32 or more). Under overloaded traffic (offered load > 1), the access delay is still less than 1 ms when the number of active nodes N is small (say 8 to 16). But when N grows large, the access delay increases and

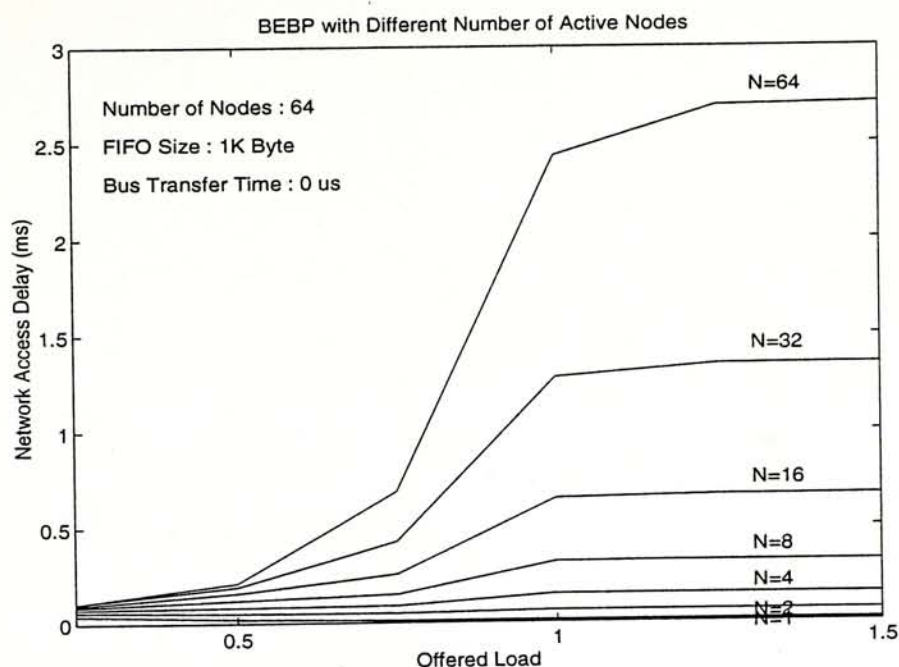


Figure 3.5: Access Delay of the BEBP Algorithm

finally saturates at 2.5 ms.

A network access delay of less than 1 ms is very competitive comparing with many 100 Mbps LAN proposal (Table 3.1). With such a small delay, BEBP can be used for real-time multimedia network applications. For example, CCITT G.164 recommends that the overall delay for a voice packet should be kept less than 25 ms. BEBP can comfortably meet this requirement.

The worst case delay is bounded to be less than 2.5 ms, which is also quite promising when compared to unbounded delay of protocols like CSMA/CD. Depending on applications, this 2.5 ms delay may be too long for some extremely delay sensitive packets. This deficiency can be overcome by using priorities. One of the possibilities is to assign priority to different connections, as in the IEEE 802.12 Demand Priority[5]. Another suggestion is to reduce the packet size, as in the ATM. The performance of BEBP for different packet size can be found in the last section of this chapter.

	BEBP	FDDI/ CDDI	IEEE 802.12	ATM LAN	Fast Ethernet
Native Network Architecture	Any	Dual Ring	Star	Star	Star
Native Physical Layer	Any	MMF/UTP	UTP	Any	UTP
Network Access Delay	<1ms (L=1)	8ms (worst)	0.5-0.8ms (high priority)	0.8ms (queuing delay)	unbounded
Support Tree Distribution Architecture?	Yes	No	No	No	No
Support Bus Network Architecture?	Yes	No	No	No	No
Support Star Network Architecture?	Yes	Yes	Yes	Yes	Yes

Table 3.1: Comparison of Different 100Mbps Network

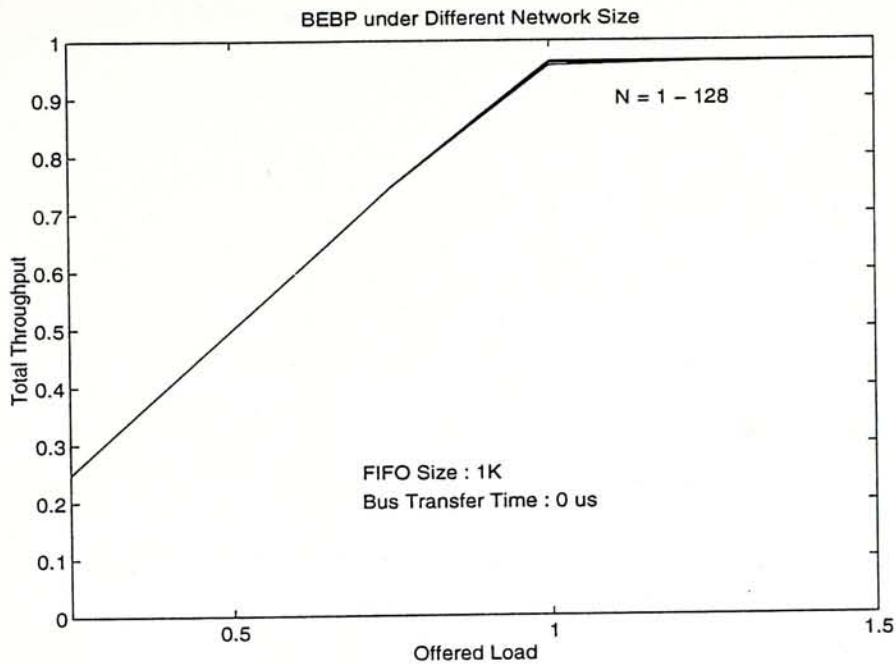


Figure 3.6: Throughput of BEBP with Different Network Size

Fairness Analysis

Fairness is not a problem at all in polling systems. The hub does not distinguish one node from another. Every node suffers the same delay, and receives the same bandwidth allocation. All the resources are allocated according to the activity of the node. Therefore, both the bandwidth allocation and network access delay are fair to each node.

3.3 Size of BEBP Network

In the simulation, different number of nodes (N) are connected to a hub ($N = 1, 2, 4, 8, 16, 32, 64, 128$). All the nodes are assumed to be active. The simulation result is shown in Figure 3.6 and Figure 3.7. For throughput, no significant difference is found. BEBP works with very high efficiency for different network size. On the other hand, the network access delay increases with the number of

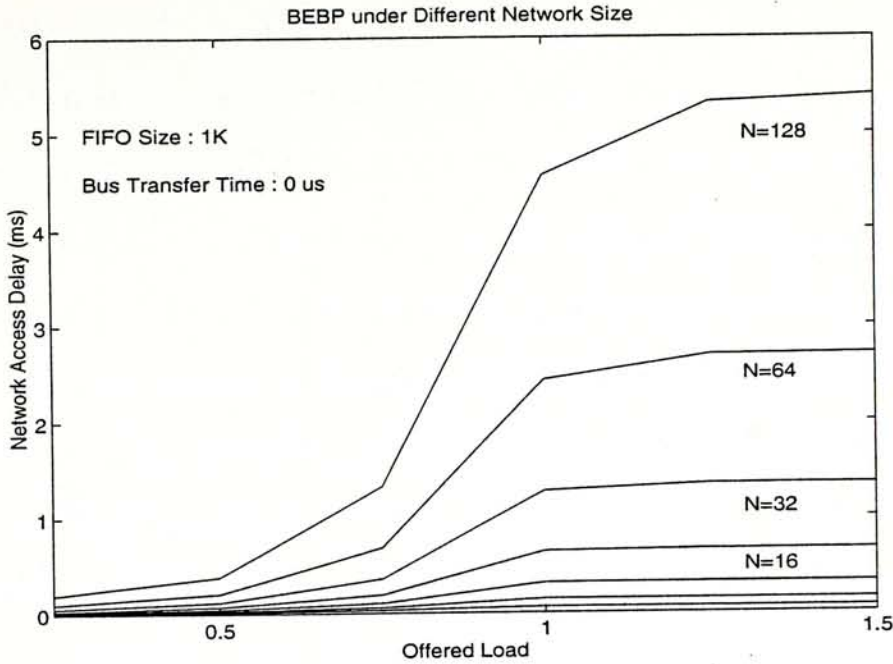


Figure 3.7: Network Access Network of BEBP with Different Network Size

network nodes.

If the network is small ($N < 16$), network access delay can be kept smaller than 1 ms even under the overloaded condition. But when N is large, network access delay is higher (1.3ms for $N=32$, 2.7ms for $N=64$ and 5.4ms for $N=128$). Therefore, when the network grows too large, it would be better to separate the network into smaller groups by using more hubs connected to a backbone network (see Section 5.4.1).

3.4 BEBP with Different Tx FIFO Size

The simulation results shown in Figure 3.8 and Figure 3.9 on throughput and network access delay do not indicate any difference when different Tx FIFO size is used. Both throughput and network access delay of BEBP is completely independent on the Tx FIFO size.

On the other hand, the TxFIFO size does affect the FIFO queuing delay of BEBP, as shown in Figure 3.10. With 1K FIFO, which can only hold one single packet, there is no queuing delay at all. The FIFO queuing delay increases as the FIFO size increases. This is very natural, since a longer queue means the packets have to wait for a longer time to arrive at the top. Such an indication does not mean that a small FIFO introduce smaller delay, because the packets still have to wait in the IP buffer in the case of small FIFO. The overall queuing delay does not vary too much.

In addition to better FIFO queuing delay, there are two more advantages for using small FIFOs. The first advantage is cost, and the second advantage is better management by the host machine. By being able to buffer the packet in the kernel, the host machine can easily manage where the packet should go. For example, time-outed packets can be killed, and a higher priority can be given to real time packets that arrived later at the queue. As a result, a 1K-Byte TxFIFO is used in our NIC design.

3.5 Limitation of the Host Bus Transfer Rate

The host bus is the interface bus between the NIC and the host machine. Since we are using Intel processors (486 or P5), the choice of the host bus for the NIC design includes:

1. PC Bus (XT Bus): 8 bits, 2 MBps (MAX)
2. ISA Bus (AT Bus): 16 bits, 8 MBps (MAX)
3. EISA: 32 bits, 8 MBps (Normal), 33 MBps (DMA)

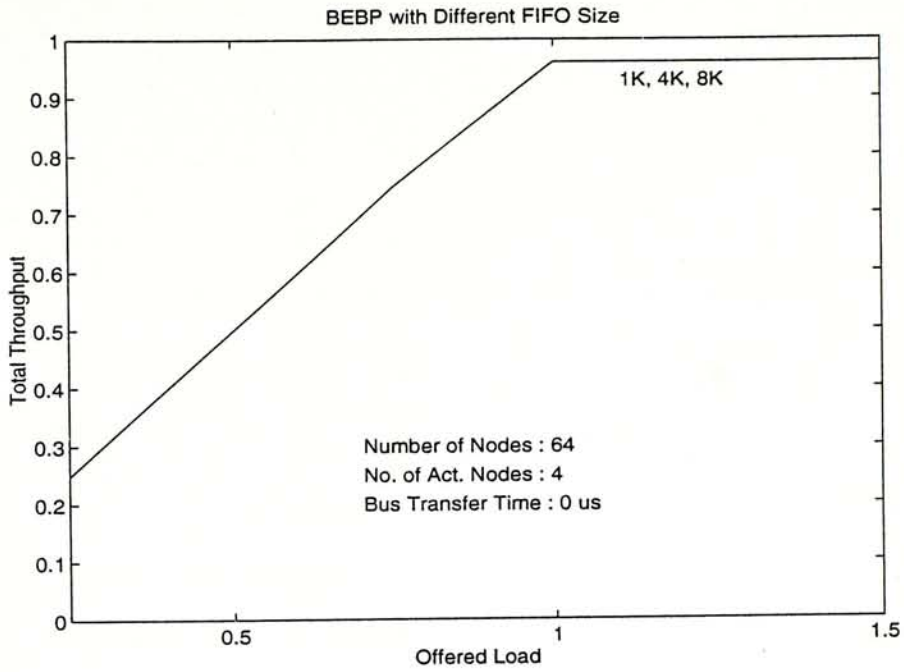


Figure 3.8: Throughput of BEBP with Different FIFO Size

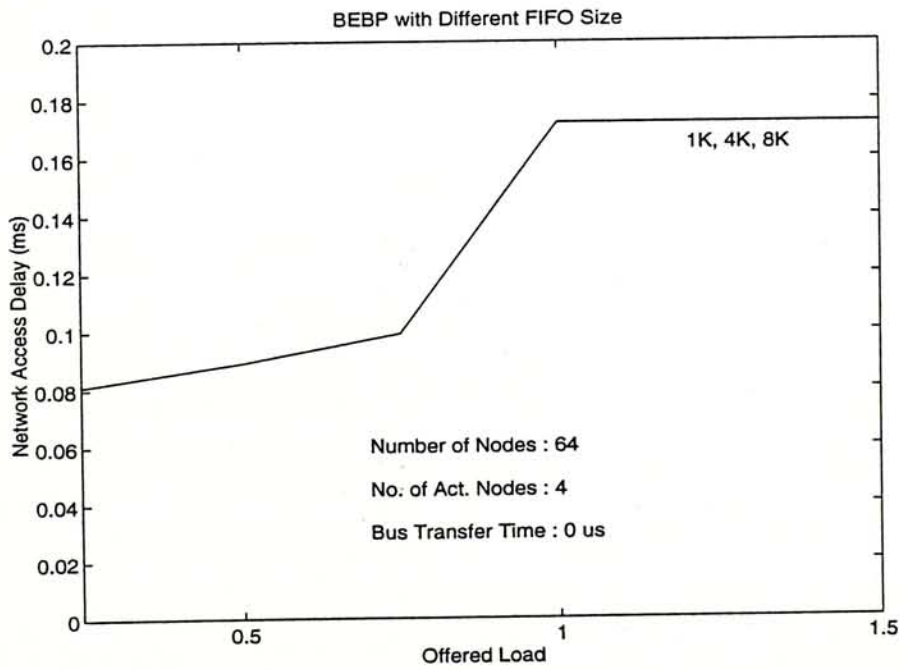


Figure 3.9: Network Access Network of BEBP with Different FIFO Size

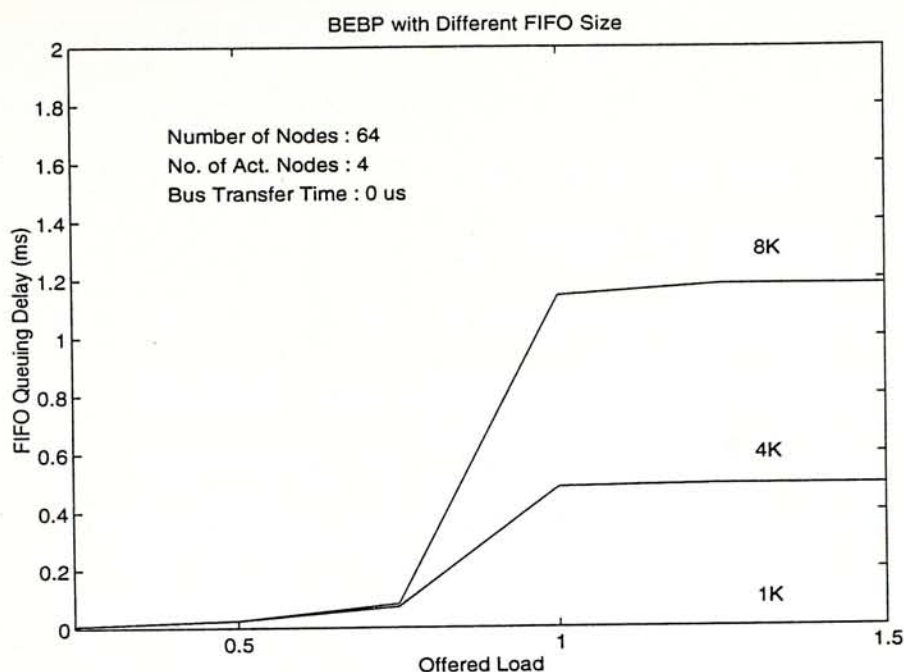


Figure 3.10: FIFO Queuing Delay of BEBP with Different FIFO Size

4. VESA Local Bus: 32 bits, 44 MBps (Normal), 132 MBps (Burst)
5. PCI: 32 bits, 66 MBps (Normal), 132 MBps (Burst)

The transfer rate of the above interface buses are obtained from [17]. For an actual system, the above stated theoretical transfer rate is always difficult to achieved. For example, we can only achieve about 1 MBps transfer rate using the PC Bus in our existing NIC design because of multiple IOs required per packet transfer.

A suitable choice of the host bus is very important in designing a heavy-traffic network adapter card, such as the NIC. The cost effectiveness is the first factor to consider. For example, in an Ethernet adapter, an ISA Bus's transfer rate is already faster than the network, so it may not be necessary to use a PCI bus for Ethernet. Secondly, as the CPU processing time is always faster than the interface bus, it is a waste of the CPU time when transferring heavy traffic over

a slow interface bus. For example, more than 5 wait states have to be added in an ISA bus transfer. Even for VL-Bus, one wait state is still required. A faster bus can reduce the waste of CPU time used in data transfer.

Figure 3.11 shows the simulation result of BEBP throughput against different host bus transfer time. The packet size is assumed to be 518 bytes. As shown in the figure, if the transfer time is less than 100 μ s, ideal performance (zero transfer time) can be achieved.

In the first BEBP prototype, we choose to build the NIC on the 8-bit ISA Bus for simplicity (Section 5.3). The transfer rate achieved was only about 1 MBps, which corresponds to 555 μ s per packet as indicated in the diagram. This is our major bottleneck of the prototype NIC. Although the theoretical throughput of the BEBP network is very high, it is limited by the NIC interface bus. The true capacity of the BEBP network cannot be shown by this version of NIC.

The next version of NIC is being prototyped. In order to eliminate the bottleneck of the previous version, the bus transfer time should be less than 100 μ s which corresponds to 5.18 MBps. Most of the 32-bit buses can handle such a transfer rate, all of the EISA, VL-Bus and PCI buses can be used. We believe the PCI bus is better for two reasons.

First, PCI is a CPU independent interface bus. Other than its originator - Intel, most of the large computer companies have already joined the PCI Special Interest Group. PCI has already worked on the Intel P5 and Dec Alpha machines. PCI on Macintosh and Power PC platforms will soon be available in the market. A single PCI board can work on different platforms without have to be redesigned for a specific bus. Such an attractive compatibility drives us to consider building the next generation NIC on PCI platform.

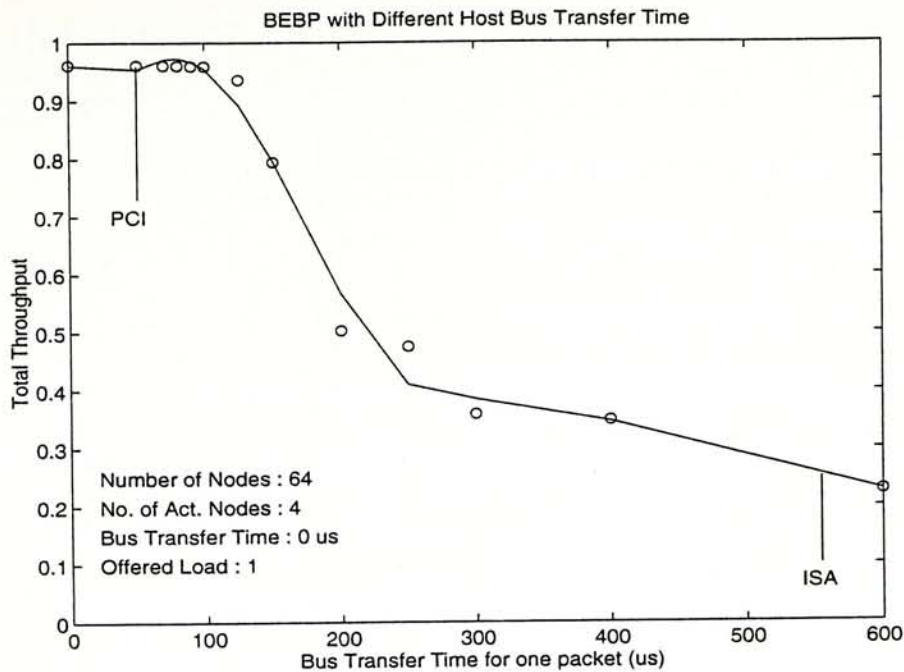


Figure 3.11: BEBP Throughput Performance against Host Bus Transfer Time

Second, PCI perhaps is the most well-defined interface bus ever occurred in the computer history. It makes use of the state-of-the-art technology because it is started from ground zero. Both EISA and VL-Bus have to consider the compatibility problem with the conventional ISA Bus. The specification of PCI [42] is very clear and well-defined for the designer to follow easily.

Hopefully, the PCI version NIC will be finished by the end of 1995. At that time, the actual throughput of the BEBP algorithm can be observed and evaluated.

3.6 Performance with Different Packet Size

In this section, the performance of BEBP with different packet size is analyzed. The simulation result is summarized in Figure 3.12 and Figure 3.13.

BEBP becomes very inefficient when the packet size is too small. For normal

loading ($L < 1$), throughput can be retained at its saturated value even when the packet is as small as 128 bytes. When the network is overloaded, the throughput begins to decrease when the packet size decreases to around 400 bytes, and finally drops dramatically when the packet size is smaller than 100 bytes.

The network access delay, on the other hand, depends on the packet size more linearly. Under normal traffic, the network access delay is more or less the same for any packet size. In the overloaded condition, the network access delay increases as the packet size increases.

The simulation results are very natural and reasonable. A small packet size can result in a low network delay, but the throughput is also low. On the other hand, large packet size can provide higher throughput but large delay network. A suitable packet size have to be chosen to balance these two factors.

First of all, the packet size should never be smaller than 100 bytes for worst case network efficiency. Second, a network access delay of over 3ms is too high, so the packet size should not be larger than 700 bytes. Therefore, the range of possible choice should be between 200 to 600 bytes per packet.

In the actual system, there are two more factors affecting the analysis of the throughput efficiency. First is the hardware header overhead which will be a very significant factor if the packet size is small (as in the case of ATM). Second is the processing overhead on fragmentation and reassembly of packets by the upper layer, in particular, the TCP layer. The IP layer have to fragment and reassemble the received message from the TCP/UDP layer according to the MTU specified by the network. The processing time spent in the transport layer will significantly increase if the packet size is too small.

In the existing BEBP, we set the packet size at 518 bytes, with a 512-bytes

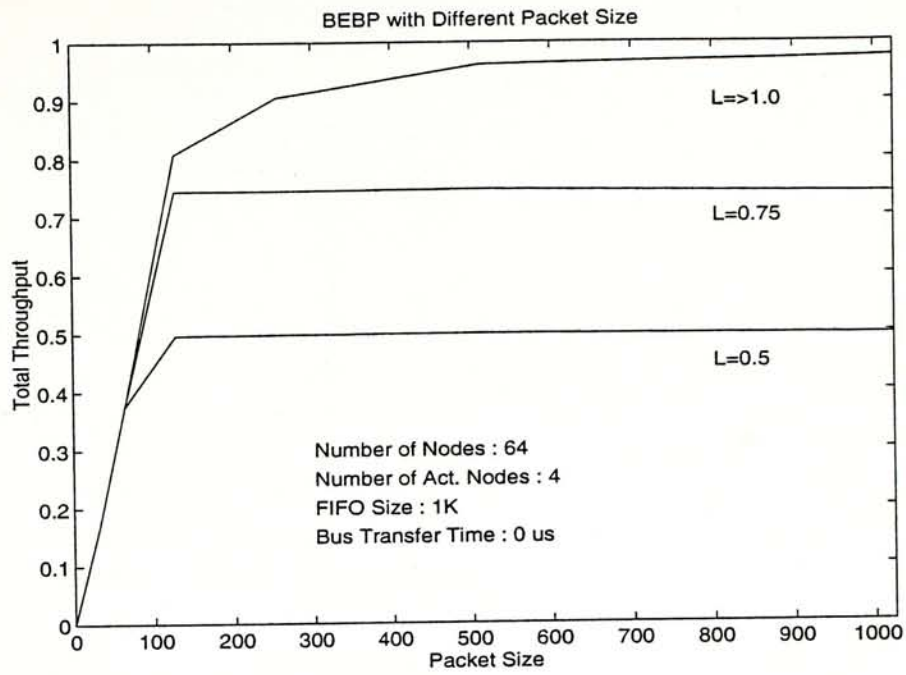


Figure 3.12: BEBP Throughput Performance against Packet Size

data field. A packet size of 262 bytes with 256 bytes data field is also possible, but the packet size should not be as small as 53 bytes used in the ATM.

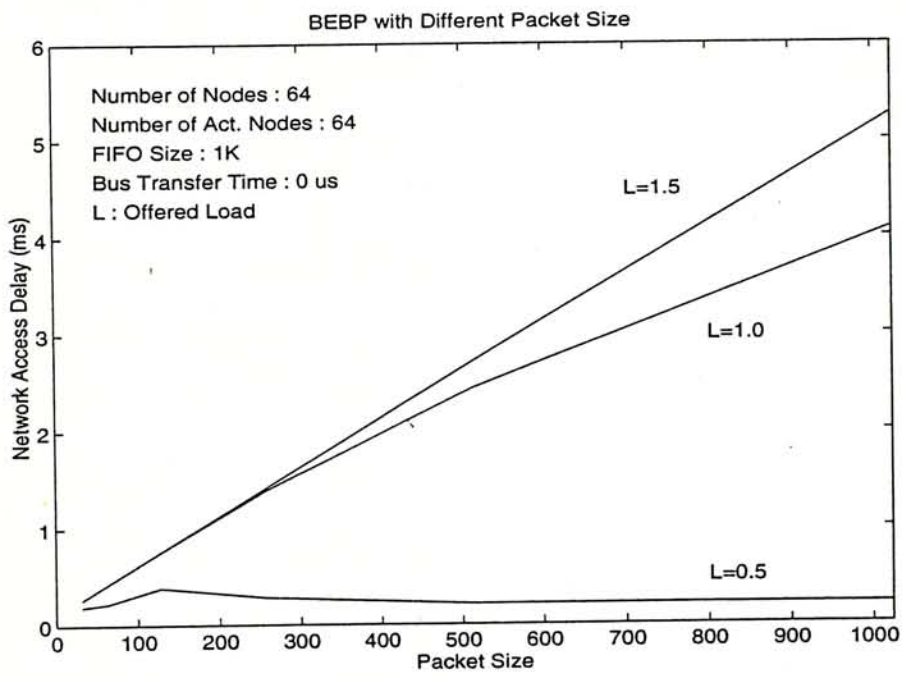


Figure 3.13: BEBP Network Access Delay Performance against Packet Size

Chapter 4

Network Architecture

As we have discussed in the Chapter 2, the hub is assumed to have access and control of two shared media, one for uplink and one for downlink. This assumption is sufficiently general, because it covers the case of switched architectures as well as multi-access architectures. Below, we illustrate how the BEBP can be implemented for bus architectures as well as for star architectures. Then we will show how BEBP can be implemented on the most common existing network cable plant: 10BaseT Ethernet, 10Base2 Ethernet, and CATV distribution network, without having to rewire any installed cables.

4.1 Dual Bus Network Architecture

In the dual bus architecture, one bus is used for the downlink while the other bus is used for the uplink. Access scheduling on the uplink is controlled by the hub through the Polling Commands at the downlink. A node will turn on its transmitter only after it has received a polling command from the hub via the

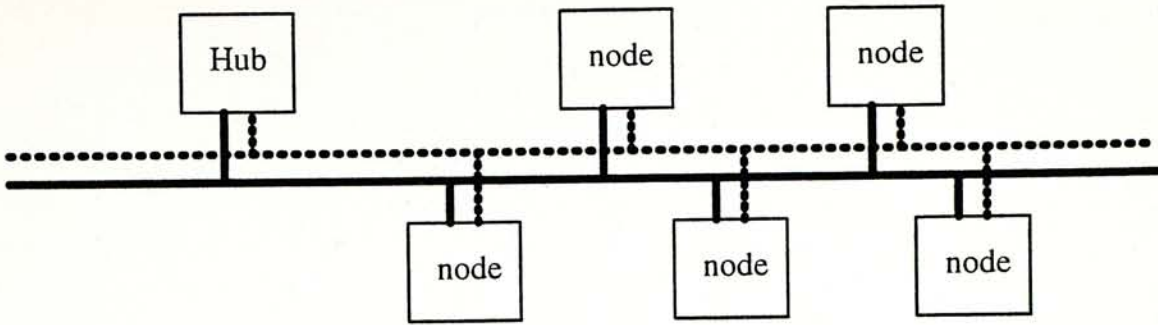


Figure 4.1: BEBP on Dual Bus Network Architecture

downlink. After one packet is completely transmitted, a node will automatically turn off its transmitter (completely isolated from the bus). This kind of transceivers is called burst mode transceiver [18]. For burst mode transceivers, the preamble used for synchronization should be minimized so as to minimize the bandwidth used in signaling.

4.2 Star Network Architecture

In star architectures, each node is connected to the hub by two links, uplink and downlink, and the protocol can be implemented either in burst-mode (similar to the dual-bus implementation) or in a continuous mode. For the latter, every link is synchronized at all time, so no bandwidth is required for synchronization establishment. The bandwidth required for signaling can also be very small. Packet is transfer through the synchronous link asynchronously. We have used the TAXI chip [44] to demonstrate the synchronous data link (continuous mode) implementation and signaling.

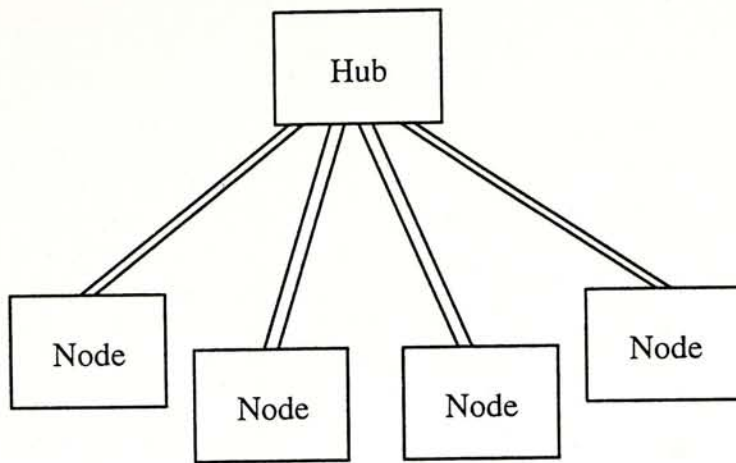


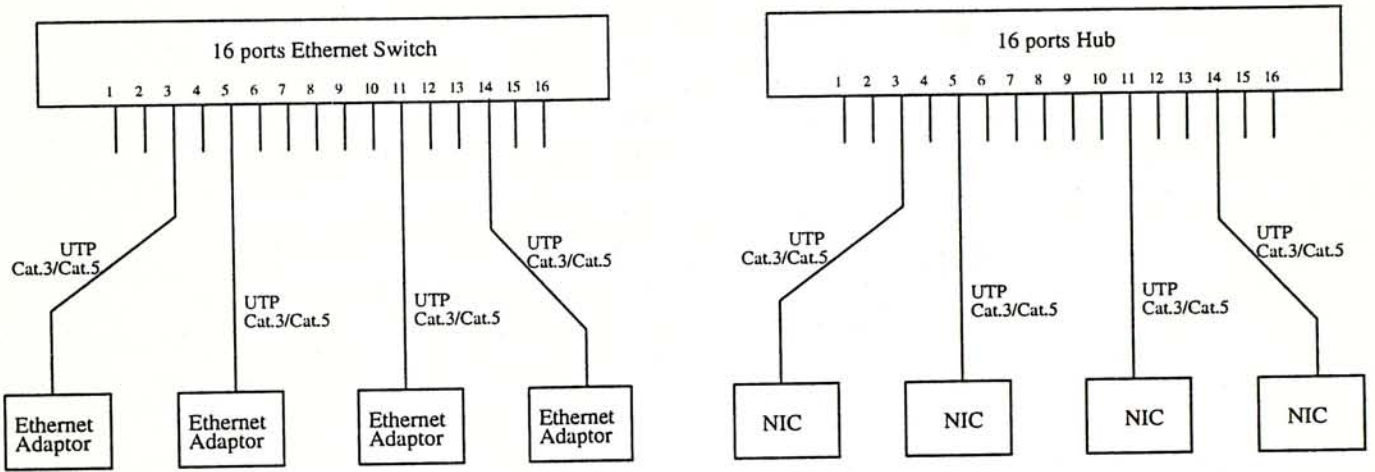
Figure 4.2: BEBP on Star Network Architecture

4.3 Compatibility with Existing Networks

The existing networks can be classified into three categories: bus, tree, and star architecture. For example, the 10Base2 Ethernet is bus, while 10BaseT is star, and the CATV system is tree. None of the existing networks can support all these architectures. Different networks are usually designed for one kind of architecture in mind which is very difficult to be used with other architectures (see Table 3.1). Our network proposal is an attempt to provide a multimedia protocol that can be used with all these different network architectures. We will show how BEBP can support different existing network architecture.

4.3.1 Compatibility with 10BaseT UTP Star Network

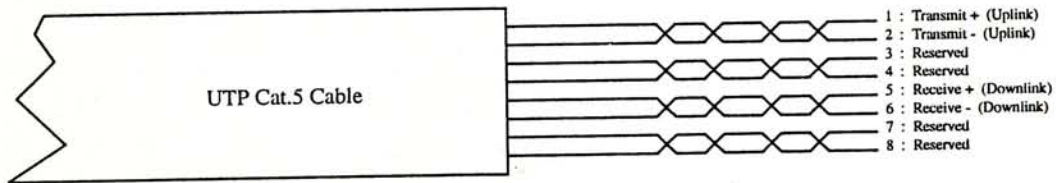
10BaseT Ethernet [34] is one of the most popular network in office and campus environment. Every 10BaseT Ethernet adapter card is connected to the concentrator, called Ethernet Switch, through a UTP cable. The UTP cable contains at least two pairs of cables (there are 4 pairs in UTP Cat.5 cable), one pair for transmitting data from the Ethernet Switch to the adapter and the other in the



The 10BaseT Ethernet Configuration



The BEBP Configuration



Pin Assignment of BEBP on UTP Cat.5 Cable

Figure 4.3: BEBP on 10BaseT UTP Cable Plant

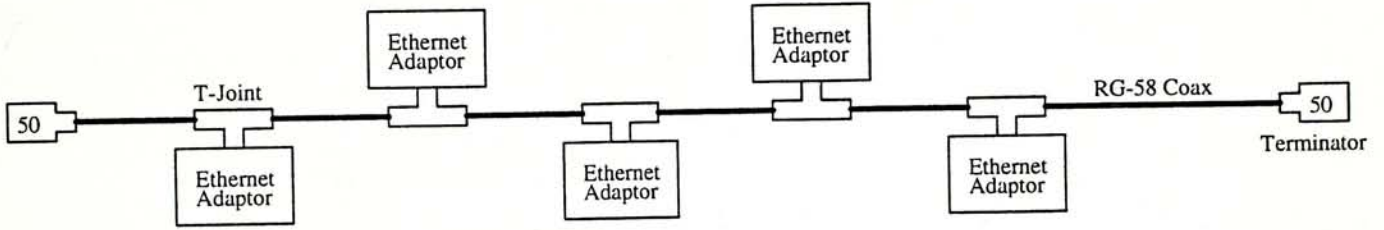
reverse direction.

BEBP can be implemented on the 10BaseT Ethernet by replacing the Ethernet Switch and Adapter with the hub and NIC respectively. Continuous mode implementation using TAXI on the 10BaseT UTP network have been demonstrated. The protocol runs without major difficulties, problems occurs only on the physical layer - the UTP cable. The physical link becomes very unstable when it is longer than 20 meters. Although the UTP Cat.5 cable claims to be able to carry 100 Mbps traffic over 100 meters, our experiment does not support it. Part of the reasons may be due to the improper connection between the cable and the device. More discussion on the physical layer will be found in Section 5.1.

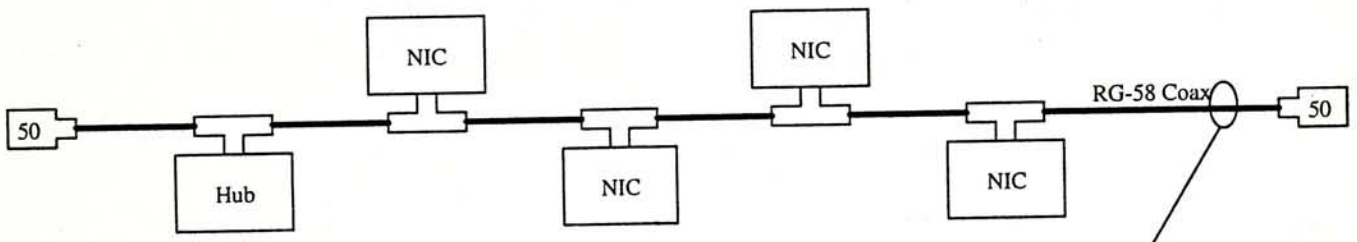
4.3.2 Compatibility with 10Base2 Coax Bus Network

In 10Base2 Ethernet [33], each network adapter is connected to a shared coax cable by inserting a T-joint in the cable. BEBP can be implemented on such a shared media by replacing the Ethernet adapter with the NIC. The hub can be placed anywhere within the cable. The scheduling of the multiple access is controlled by the hub. Burst mode implementation can be used in the RG-58 cable. No burst mode transceivers are commercially available in the market, so a burst mode version of the TAXI chip is implemented. Detail is found in Section 5.2.2

The dual channel required by the BEBP can be implemented on a single cable system by two ways: (1) frequency multiplexing, (2) bridge circuit. In frequency multiplexing, the two channels are carried at different frequencies so a single cable can provide dual channel communication. This is a more expensive



10 Base 2 Ethernet Configuration



BEBP Configuration

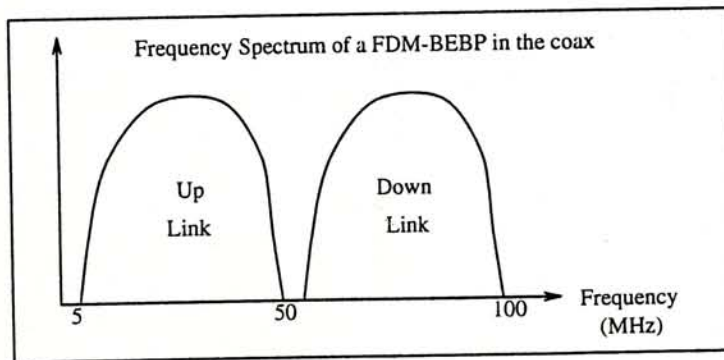


Figure 4.4: BEBP on 10Base2 Coax Ethernet

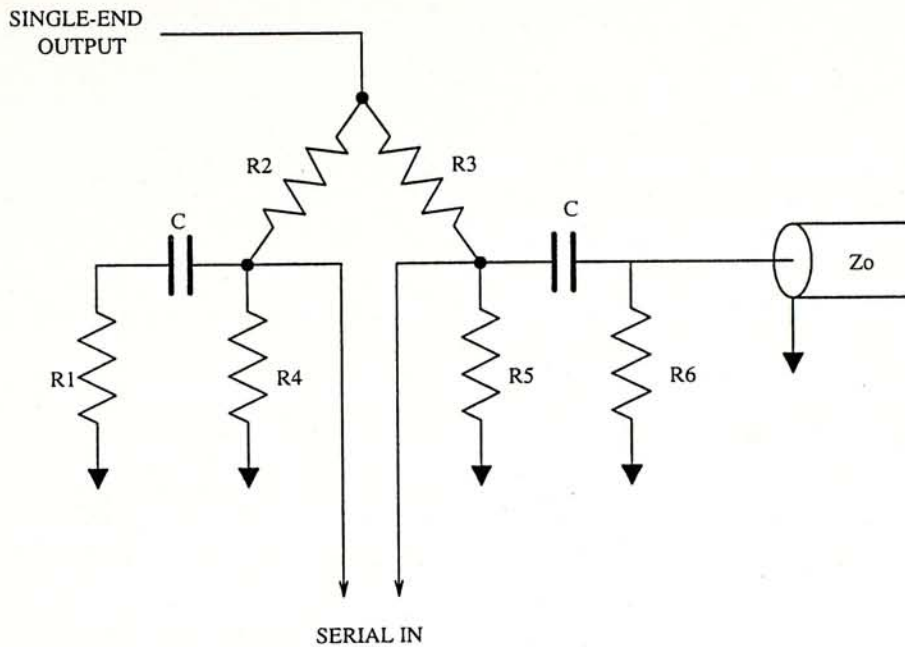


Figure 4.5: Bridge circuit for bi-directional link (from AMD TAXI TIP No.89-09, Ref.12330D-41)

solution but it provides a very reliable channel.

Another method to achieve bi-directional communication over a single cable is to use a bridge circuit, as shown in Figure 4.5. For the bridge circuit, the transceiver device should be able to drive differential signal output. Most of the highspeed (over 100 Mbps) transceivers, like TAXI [44], SONET OC-3 [45], 100BaseT Transceivers [46], or Hotlink [47] are already designed to drive differential pair output.

In the bridge circuit, the +ve SERIAL OUT pin drives a bridge circuit in which the impedance of the cable and its termination is balanced by a resistive load R_1 . The top two resistors (R_2 and R_3) are chosen to equal the cable impedance. R_3 serves as part of the impedance matched termination for the cable, while R_2 balances the bridge for both AC and DC signals originating at the top of the bridge. Resistors R_4 and R_5 serve as both part of the coax

termination networks, and as part of the bias network to set levels for the receiver inputs. Resistor R6 is a large value bleeder resistor to remove any accumulated DC voltage from the line, and is not intended for the cable termination.

Input to the bridge is single ended for signals which originate at the junction from the coaxial cable, while the SERIAL IN receives differential signal from the bridge. Signals originated from the cable are referenced against the load presented by R1 (constant), which produce differential input signals to the SERIAL IN. If the signals are originated from SERIAL OUT at the top of the bridge, both SERIAL IN pins will act simultaneously. This is called the common mode input, which is functionally equivalent to the idle in a differential input pins.

Such a bridge circuit design can provide bi-directional communication over signal cable but the trade-off is that only the single-ended signal of the differential signal is used, which result in a 50% lower power budget. The feasibility have been shown by AMD [48]. A 100-ft, 125MHz bi-directional data link using RG-58 coaxial cable as the media has been reported to operate successfully.

4.3.3 Compatibility with the HFC Coax Tree Network

The most important feature of the Fast Polling Protocol based on BEBP is that it can run on the existing CATV tree distribution network. Hybrid Fiber Coax (HFC) architecture is believed to be one of the most promising solutions to bring broadband services to the home. The coax part of the HFC system is basically the conventional CATV distribution system, consisting of taps and splitters/combiners.

The key difficulty to provide interactive broadband services over CATV coax system is the multiple access contention over the uplink. Conventional protocol

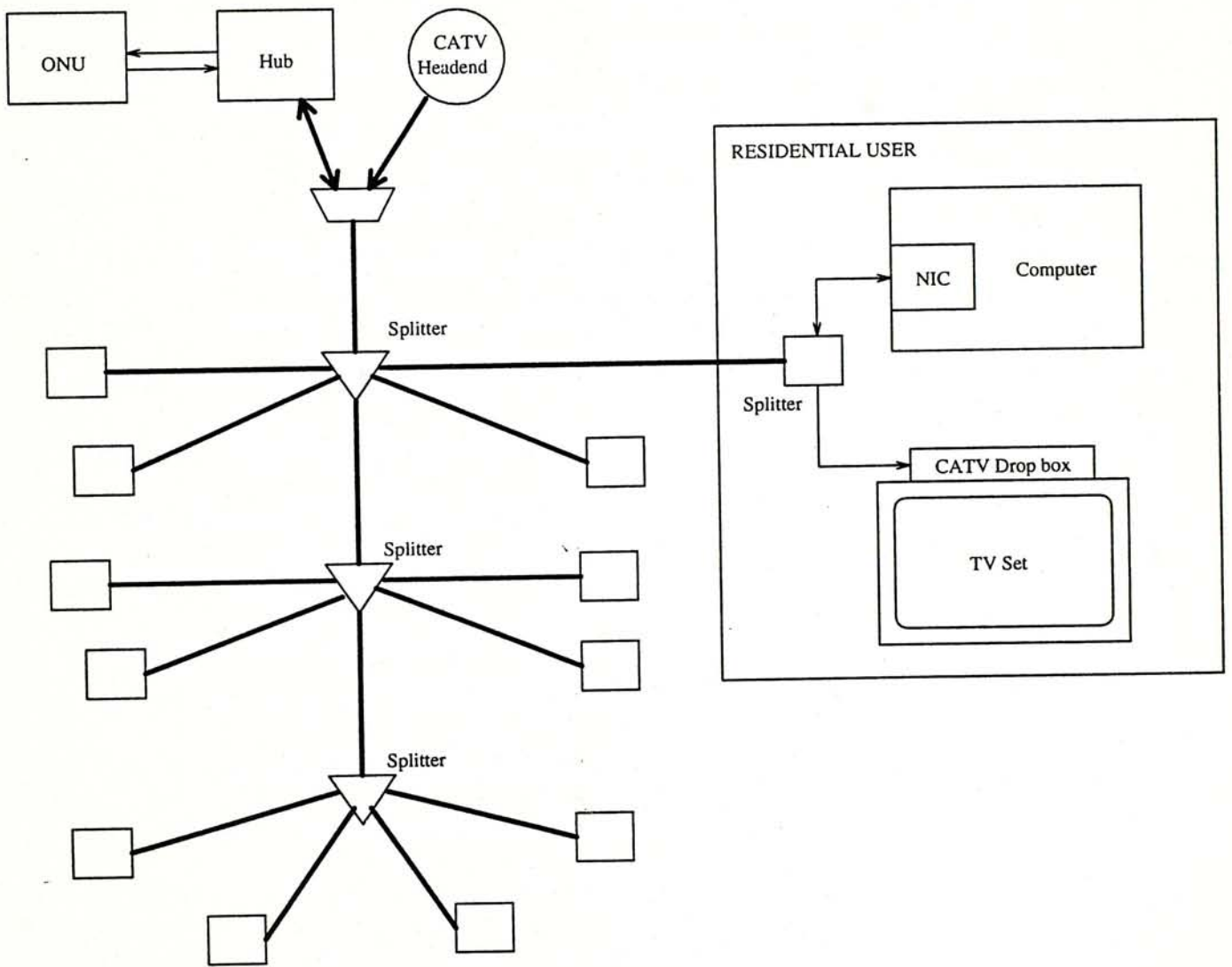


Figure 4.6: BEBP in HFC Distribution Network

like CSMA/CD is not applicable to CATV system, for the signaling in one branch cannot propagate to another branch. Many proposals are suggested to resolve this multiple access problem, like TVNet [19] and Homenet[20]. All these suggestions are based on circuit switch channel assignment or reservation, which is not suitable for data communication. Other suggestions like the Two-hop CATV Data Networks [21] and SWIFT [22] are packet switched networks which are more suitable for data communication, but the efficiency of bandwidth utilization is not satisfactory.

The Fast Polling Protocol with BEBP is especially suitable for a Hybrid Fiber-Coax system. First, the protocol provides an efficient and fair multiaccess mechanism for multimedia communication in the local access coax system. Second, the central controller / hub provides a very convenient access point to the fiber network. Thus, the proposed network can be easily installed in a HFC system, by placing a high-speed optical network access unit at the hub in the local distribution headend, and a network Interface Controller (NIC) in every home. Third, since all the intelligence of the network is located at the hub, the design of the drop box in every home is very simple and low cost.

BEBP can be implemented on the CATV tree-structure single coax systems. We can use the burst-mode design as discussed above because the signals are either broadcast downlink or transmitted uplink directly to the hub, so unlike Ethernet, signaling between any two nodes are not required. The splitters/combiners existed in a tree network will not affect the protocol. A tree network is logically equivalent to a bus network under BEBP.

Chapter 5

Implementation

In this section, the design and implementation issues will be covered. First, different physical layer is tested and evaluated. Then more details on the TAXI chips will be described. Afterward, the design of the major component - the NIC and hub will be discussed in the third and forth section. Finally, more issues on the software will be covered.

5.1 Physical Layer

For 100 Mbps link, several physical layers can be used. Table 5.1 shows the performance of different physical layers. Only a rough comparison has been done. The physical layer is tested by the TAXI chip. TAXI provides an indication in the receiver called the violation (VLTN), which will be active when it decodes an illegal bit pattern from its serial data. If the power budget is not enough, bit error may occur in the serial data which results in a violation. "Distance before violation" means the maximum distance that can be reached before a

	RG-58 coax	RG-59 coax	UTP	STP	MMF
Impedance (Ω)	50	75	100	150	–
Attenuation at 100MHz (db/100m)	16	12	28	16	0.04
Distance before violation (m)	50	100	20	50	1000

Table 5.1: Comparison of Different Physical Layers

single violation occurred within the test time.

As shown in the table, UTP Cat 5 cable can only reach 20 m. STP and RG-58 coax have similar performance of about 50 m while broadband RG-59 coax can reach about 100 m. If MMF with LED is used, distance before violation can reach 1 km.

The performance is not very satisfactory, especially for the UTP. Both the cable and connectors limit the distance. The frequency spectrum of TAXI spans from 5MHz to 50MHz with its 4B5B plus Manchester line coding. Since the attenuation of RG-58 cable at 100MHz is very high (16db/100m), the theoretical maximum distance to provide enough sensitivity for the TAXI receiver is only 80m. Thus it is not surprising that only 50m is reached in our test.

Both UTP and STP claim to be able to carry 100 Mbps over 100 m, so the worst performance in our test is mainly due to the NEXT and FEXT effect in the connectors. In our experiment, conventional twist-pair cable connectors (DB-9 or RJ-45) are used, both are not suitable for high speed communication. If high-end connectors (shielded RJ-45, or shielded DB-9) are used, better results may be obtained.

This does not mean that the UTP Cat 5 cable has no problem. Although Cat 5 is designed for 100 Mbps application, not a single vendor claims that they

can let 100-Mbps signals run over a 100-m Cat 5 cable.

Alternatively, many solutions are suggested to run high speed signal over Cat 5 cables. Suggestions can be categorized into 3 groups. First is on line coding, ref. [23] summarizes the current work on that. Suggestions include the NRZ adopted by ATM Forum [41], MLT3 for CDDI [24] and SONET [25], and the three-level “partial-response” codes BPR1 and BPR4. The second solution is to make use of the “spared” pairs of wires in the Cat. 5 cable, like IEEE802.12 [5]. That is, each pair of wires actually only carries part of the 100 Mb/s. Other people also think that the STP can be further improved to shield each single wire independently. As a result, every wire behaves like a coax, which can highly increase the bandwidth of the cable. Such kind of cables is called the Foiled Twisted Pair (FTP), but this suggestion requires the re-wiring of cables.

If 100-Mbps data communication can be reliably run on the UTP cable plant, it is surely a better media in office and campus environment than coaxial cable. Dual channels can be easily obtained by twisted pair cables, but FDM or bridge circuit have to build on coax to achieve this. If dual coax is used, the cost will be higher. Also the laying of twist paired cable is far easier than coaxial cables.

5.2 MAC Layer

In this section, we will show an implementation example of the MAC protocol discussed in Chapter 2. We will describe the datalink of our prototype, TAXI, first. Then we will show how the MAC protocol can be implemented on the TAXI datalink.

5.2.1 Continuous Mode Datalink

In our network, we use the TAXI transceiver chips from AMD [44] as the datalink layer. TAXI stands for Transparent Asynchronous Xmitter-Receiver Interface. The transmitter is basically a parallel to serial MUX, plus a 4B5B encoder, and the receiver is a 4B5B decoder plus a serial to parallel DEMUX. One of the special features of the TAXI chips is its method of synchronization. When it is not transmitting data, the TAXI transmitter will automatically generate a special SYN pattern in the serial link, while the TAXI receiver can adjust its phase locked loop to get a better locking. TAXI is a byte-oriented protocol. After a byte (8-10 bit) of data is strobed into the TAXI transmitter, it will automatically encode, serialize and send into the serial link. The TAXI receiver automatically recovers the "encoded-byte" in the serial data.

Other 100Mbps datalink layers are available, like SONET [45], Hotlink [47], Fast Ethernet Transceiver (100BaseT) [46]. We choose TAXI for its convenience to sent burst data packet over synchronized link. Much of the bandwidth used in synchronization can be saved. Another reason is to compatible with ATM physical layer, works have been started to integrate the BEBP with ATM.

5.2.2 Burst Mode Datalink

A burst mode modification of the TAXI link has been implemented, which is shown in Figure 5.1. A ECL buffer is inserted in front of the TAXI serial output. Before a packet is sent, the ECL buffer will be opened first. But doing this, a preamble is added before the packet, which may increase the bandwidth wasted in signaling.

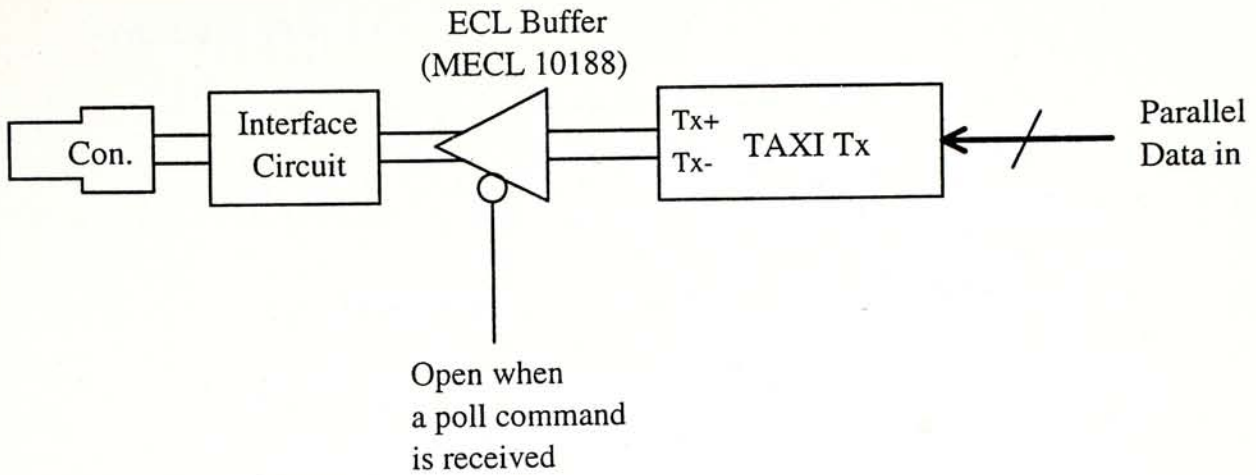


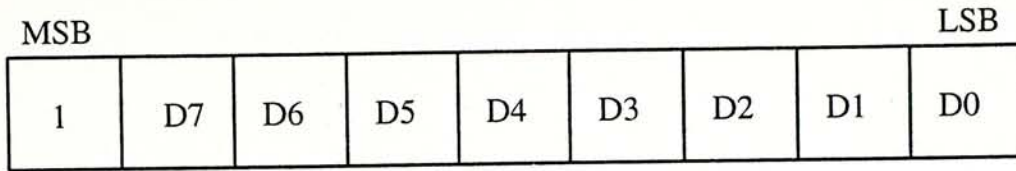
Figure 5.1: Block Diagram of Burst Mode TAXI

5.2.3 The 9-bit Polling Commands

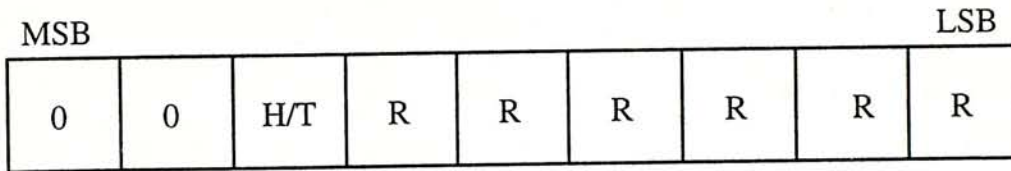
One of the major concern is the efficiency of handling signaling in polling system. In order to minimize the bandwidth used for signaling, the commands are designed to be very short - only 1 byte long. Furthermore, we have designed the protocol such that whenever the hub wants to send a command, it simply inserts the command anywhere in the downstream data without having to wait for the idle time interval between two downstream packets. This reduces the polling time required substantially. We have demonstrated this signaling capability by on TAXI datalink.

There are two methods to insert the one-byte polling commands into the TAXI datalink. Since TAXI employs the 4B5B line coding, there are some serial words which are not used by any data pattern. TAXI provides a special feature called the Command Transmission to make use of these "unused" codes. The hub can make use of these "unused" code to send the polling commands, which will not confused with normal data byte. Such an implementation have been tried by the other network, like METANET [14].

NORMAL DATA BYTE



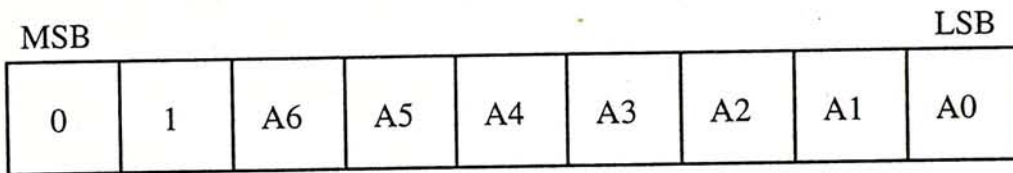
HEADER/TRAILER BYTE



0: TRAILER

1: HEADER

FAST POLLING COMMAND



← POLLING ADDRESS →

R: RESERVED

Figure 5.2: The Definition of the 9-bit Byte

We choose to use another special feature of TAXI to implement the protocol - the 9 bit mode. TAXI chip set provides 8 bit, 9 bit and 10 bit mode operation. For normal packet operation, 8 bit operation is sufficient. In order to distinguish between the control byte and normal data byte, we choose to use the 9-bit mode of TAXI. Normally, the 9th bit is set. If it is a control byte, then the 9th bit will be equal to 0. For command byte, the 8th bit is used to distinguish between packet header/trailer and the Fast Polling protocol. The definition of the “9-bit Byte” is shown in Figure 5.2.

Since the control byte have a special bit pattern, it can be easily recognized, filtered out whenever necessary. Every node will recognize its own poll command, and ignore any other poll commands. At the same time, it can filter those control bytes from normal data byte. The control bytes therefore is not necessary to place in between the idle time of two packets, it can be placed anywhere in the datalink.

The use of the 9-bit mode of TAXI provides an extra convenience on packet synchronization. Every packets are encapsulated by a special pattern packet header and packet trailer, which provide an easy way to isolate corrupted packets (see Section 5.3). But on the other hand, it wastes part of the bandwidth of the datalink. For example, in our case, the serial bit rate of the TAXI transceiver is set at 110 Mb/s for the 9-bit mode, the actual data rate is only 80 Mb/s. 3 bits are waste out of 11 bits for the 4B5B + 5B6B line coding, and the extra bit used for control byte.

5.3 Design of the NIC

The block diagram of the NIC is shown in Figure 5.3. TAXI Tx and TAXI Rx stand for the AMD7968 and AMD7969 respectively. FIFO stands for First-In-First-Out Memory, in our design, Am7202A (1K x 9bit) or Am7205A (8K x 9bit) from AMD is used [49]. FIFO is a special function RAM which supports asynchronous and simultaneously read/write port accesses. Parallel data are strobed into the FIFO through the input bus by the write strobe. The parallel data can be retrieved from the output bus by strobing the read pin. In 72xx family FIFO, three flags are supplied by the IC indicating the statues of the

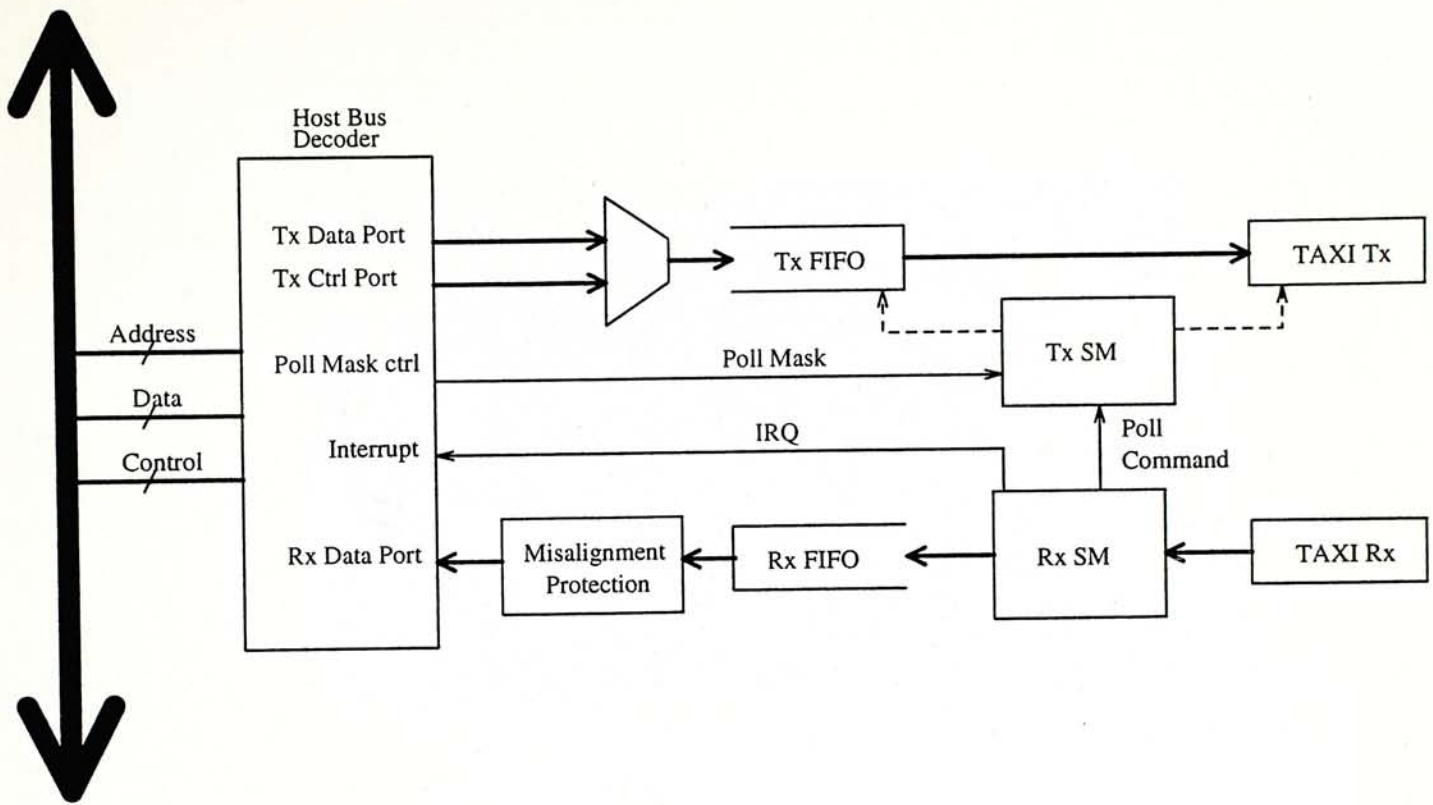


Figure 5.3: Block Diagram of NIC

FIFO. They are the Empty, Half-full and Full Flag, which will be set when the FIFO is empty, half-full and full respectively.

In order to simplify the design, Programmable Logic Device (PLD) is used in the NIC. We select the ispLSI family from Lattice, which stands for “In-System Programmable Large Scale Integration” [50]. The 84-pin PLCC ispLSI-1032 with 64 I/O pin is used. Most of the logic design described in the following sections are implemented inside the ispLSI. One of the special and convenient features of the ispLSI is its “isp”, which means that we can change the logic inside the ispLSI without plugging out or even power-down the system. This can largely reduce the hardware design return time. Since the I/O of the ispLSI is not enough to decode the address bus of the PC-AT Bus, a GAL20V8 is used for the base address decoding.

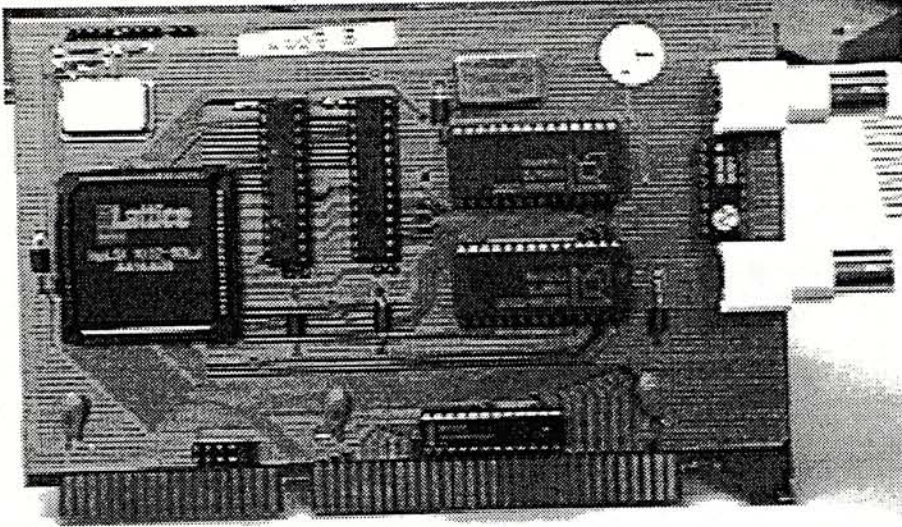


Figure 5.4: Photograph of the NIC

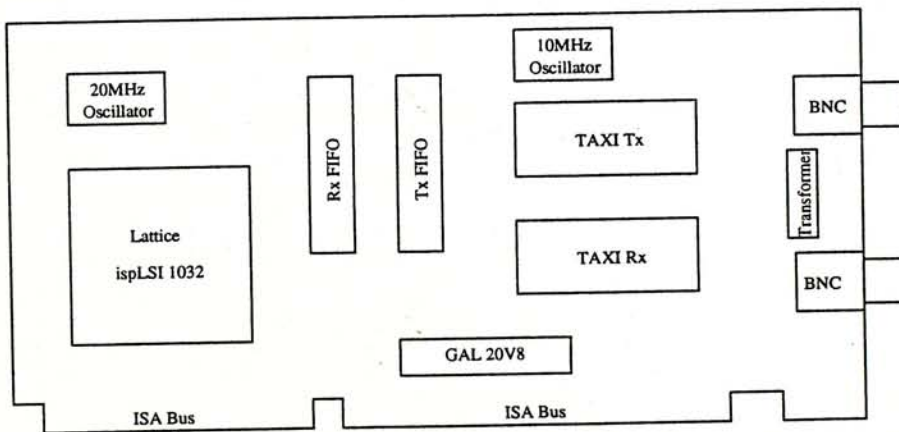


Figure 5.5: Components on board of the NIC

As a result, the board size and the number of component count can largely reduce. There are only 6 components: 2 FIFO, 2 TAXI, 1 ispLSI and 1 GAL. And the board size can reduce to only 4 inches by 6 inches, as shown in the Figure 5.5. The circuit diagram of NIC is attached in Appendix D.1. The CUPL program and the LDF program for the GAL and ispLSI are also attached in Appendix E.1 and Appendix E.2 respectively.

The following subsections will discuss the design of the transmitter and receiver modules of the NIC in detailed.

5.3.1 Transmitter Modules

The transmit FIFO (TxFIFO) is used to buffered the out-going packet. For flow control, the host machine will observe the status of the TxFIFO before transferring a packet to the TxFIFO. One of the possible way is to monitor the full flag of the TxFIFO, but it is not a very good scheme. Available space in the TxFIFO may not enough to occupy a complete packet, so if the host machine start to transfer the packet whenever the FIFO is not full, part of the packet may be lost. Such a corrupted packet will cause a lot of problem in routing. So the half full flag of the FIFO is used instead. When the host machine has a packet to send, the host machine will check the half full flag of the TxFIFO first. If the TxFIFO is not half-full, the packet will be transferred, otherwise, the host machine will buffer it softwarely or just discard it.

Control and Data Port

According to the protocol, every byte is 9 bits. The ninth bit (D8) is set to zero for packet start/end and is set to one for the normal data. Such a special

signaling can be implemented on a 8-bit PC-XT Bus, by using two independent I/O ports. If the data is written into the Tx FIFO by the Control Port (Figure 5.3), D8 will automatically set to zero. If it is written through the Data Port, D8 will be one.

Transmitter State Machine

A transmitter state machine logic (TxSM) is placed in between the Tx FIFO and the TAXI transmitter. The major function of the TxSM is to transfer the packet in the FIFO to the TAXI, but it will do that unless both of the following conditions are satisfied: (1) a complete packet is found in the Tx FIFO, (2) a poll command addressed to it is received. The first condition is necessary because the transfer rate of the host machine bus may not be faster than the TAXI Tx. (But if the host bus is faster, as in the PCI, this condition is no more required.) If the TxSM starts before a complete packet is ready, the packet will not be in a burst, many idle times are inserted in the middle of the packet. In order to guarantee the burst of packet, a PollMask flag is added which is controlled by the host machine. Before the host starts to send a packet, it will set the PollMask. The TxSM will not respond to any poll commands if the PollMask is set. So it will ignore all the poll between the time where the packet is transferred from the host machine to the FIFO. The timing is shown in Figure 5.6 .

Under such a scheme, the packet transfer to the TAXI can be guaranteed to be a burst, but the first packet in the FIFO will suffer greater network access delay in case the poll originally dedicated to it may be masked out by the second up-coming packet. It is really the case observed in the ISA Bus system, where the packet transfer time requires as long as 555 μ s. But such a worry will be completely

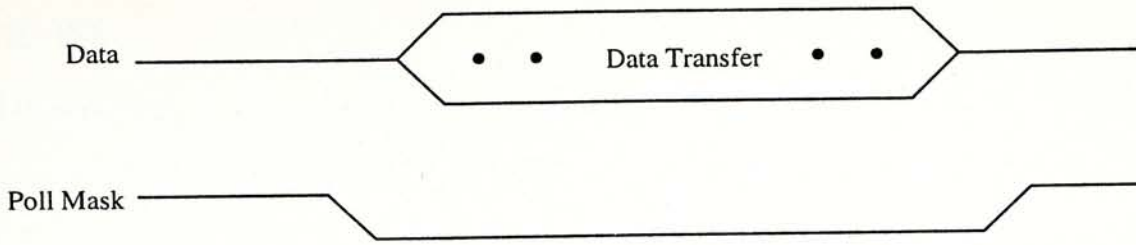


Figure 5.6: Operation of the Poll Mask in Tx SM

removed under PCI Bus System, experiment shows that the packet transfer time can be less than $50 \mu\text{s}$, which is faster than the TAXI transfer rate. Under such a fast bus, the TxSM has only need to consider whether the TxFIFO is empty, if it is not and it receives a poll command, it will start the transfer. No idle time will be inserted in between the packet, even the PCI bus transfer and the TAXI transfer start at the same time.

5.3.2 Receiver Module

As in the transmitter module, there is a TAXI receiver and a FIFO connected to the host machine bus in the receiver modules. A Receiver State Machine (RxSM), and a misalignment protection circuit is used to control the receiver module.

Receiver State Machine

Data received from the TAXI receiver will not directly put into the Receive FIFO (RxFIFO), RxSM is placed in between the FIFO and TAXI as in the transmitter modules. First of all, the RxSM will filter out all the poll commands from normal packet. If the poll commands is addressed to this node, it will generate a signal to the TxSM. Also a packet filter is implemented in the TxSM which will filter out the packet with correct IP address or broadcast address and put them into

the RxFIFO.

Depending on the destination address of a packet, the RxSM will decide whether to kill or forward the received packet. A five stage shift register which shift by a normal data byte, and reset by the packet-head is used to implement the packet filter circuit. If all the four address bytes in the first four stage are matched, either matched with the IP or the broadcast 255.255.255.255, the fifth stage register will be set and will not change till the packet-end. Depending on the fifth stage output of the shift-register, data received from the TAXI is either ignored or written into the RxFIFO. Packet written into the RxFIFO will have no header, but the packet-end is intentionally retained, which is very important in the misalignment protection circuit.

Interrupt

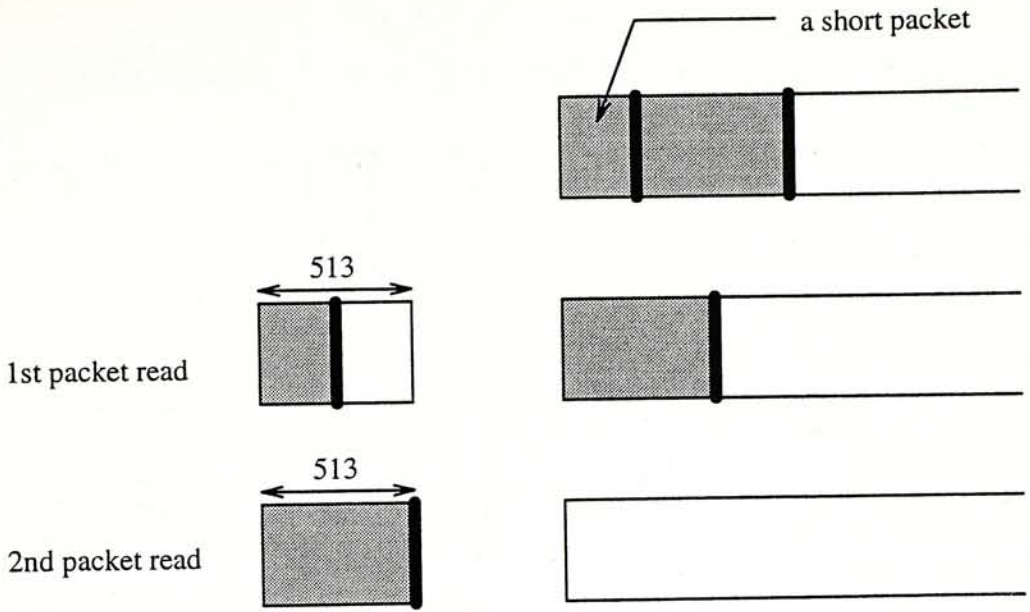
A successfully received packet (written into the RxFIFO) will generate an interrupt (IRQ) to the host machine. The host machine will response to the IRQ by reading out one packet from the RxFIFO. Under normal traffic, such a mechanism is capable to handle the packet one by one. But under high traffic, the context switch of the host machine may not be fast enough to handle every packet. A second interrupt may arrive while the host machine is still handling the first packet. It will than miss the second interrupt, which in turn will miss the second packet. Little tricks can be added in the host machine's driver software to solve the problem. Every time the host machine receives an IRQ, it will not only read one packet from the RxFIFO. Instead, it will read packets one by one, until the RxFIFO is empty. As a result, several packets can be read in a single context switch, which can reduce the time used in context switching.

Misalignment Protection

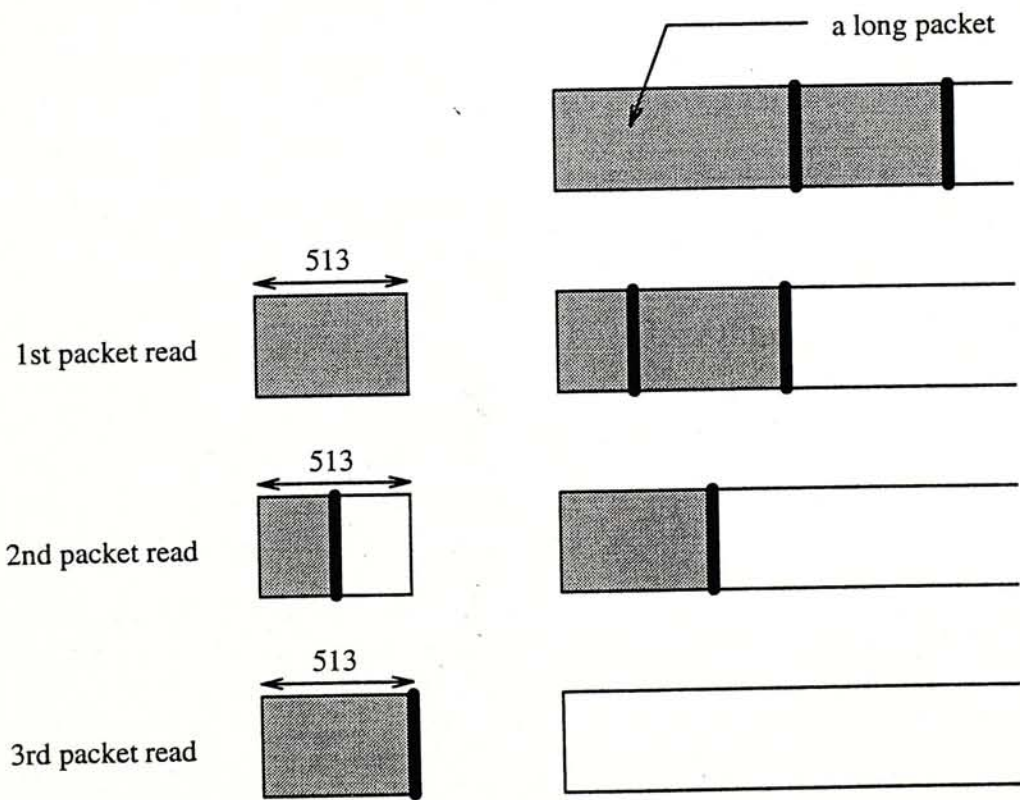
In between the RxFIFO and the host machine bus, there is a misalignment protection circuit. Misalignment will be happened anywhere and any time in the network. It may be an accidentally one byte added-in in between a packet, or it may be a missing of any number of bytes in the packet. Without misalignment protection, a single byte-misalignment may cause a large number of packet lost.

The misalignment protection can be implemented because every packet is separated by a packet-end, which has a distinct bit pattern from other data byte. The host machine will continue to read fixed-amount of bytes (512+1 Bytes) from the RxFIFO, but the FIFO will stop pouring data out whenever it observed that a packet-end has been read. Under normal condition, that is the packet is exactly 513 byte long, no special things will happen. But if the packet is shorter, e.g. 500 bytes, the FIFO will stop pouring out data after the 500th byte, but the host machine will continue to read even there is no one responding it. The host machine will check whether the last byte is matched with the pattern of the packet-end, an incorrect matched will cause the host machine to discard the packet. In this case, the shorter packet just read will be discarded, and the next packet is aligned again. Similar case occurred in a longer packet, where the first two packets read by the host machine will be discarded and the third packet read by the host machine should be aligned. Figure 5.7 illustrates the cases.

5.3.3 Serial Interface



Misalignment Protection when short packet occurred



Misalignment Protection when long packet occurred

Figure 5.7: Operation of the Misalignment Protection Circuit

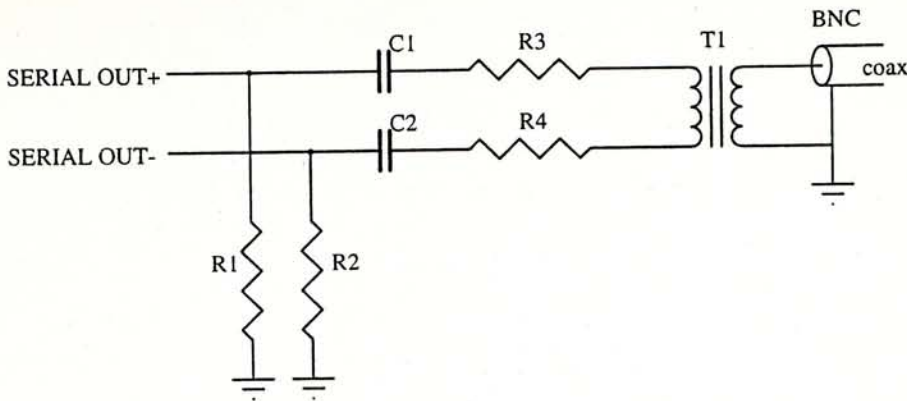


Figure 5.8: Serial Out Interface Circuit

This section will describe the interface circuit for the serial output of the TAXI transmitter and the serial input of the TAXI receiver. The circuit for serial output is shown in Figure 5.8. R1 and R2 provides the output loading for the differential ECL output (Tx+ and Tx-) of TAXI. The differential signal is transformer-coupled to the BNC connector. C1 and C2 are used to filter the DC signal, while R3 and R4 for impedance matching. With the transformer coupling, the differential signals can be transformed to single-ended signals which then pass to the coaxial cable.

In the receiver (Figure 5.9), the single-ended signal is transformed to differential signal by the transformer (T2). C3 and C4 will filter all the DC component of the signals, which generated by noise. Resistors network R5 to R8 provide two function, adding a DC level to the differential signal and matching the impedance. Their values should satisfied the following equations.

$$\frac{R5R7}{R5 + R7} = \frac{Z_o}{2}$$

$$\frac{R7}{R5 + R7} \times 5V = 3.7V$$

In the first equation, R5 and R7 provide an impedance of exactly half of the

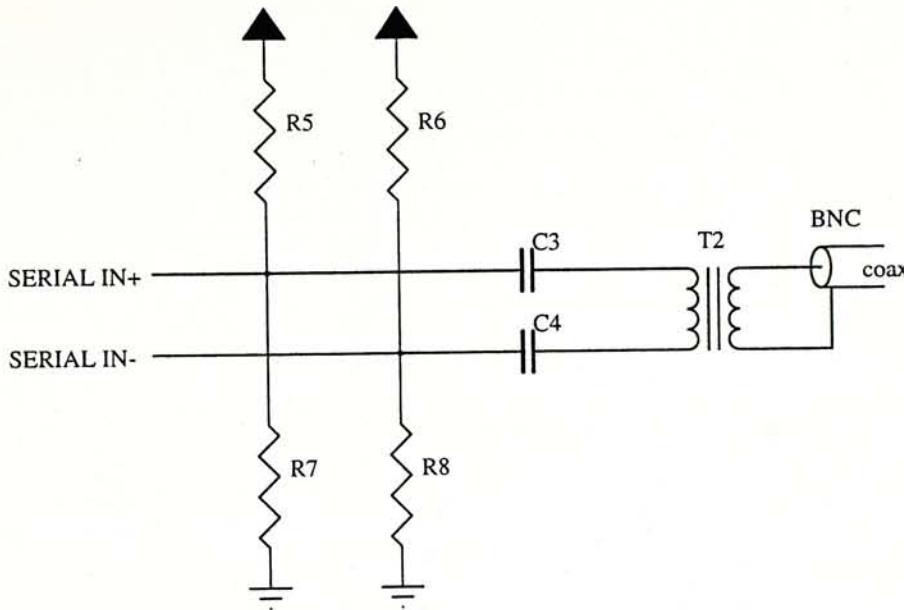


Figure 5.9: Serial In Interface Circuit

impedance of the cable (Z_o) for matching. The other half is provided by R6 and R8, which have the same values as R5 and R7 respectively. Second equation is come from the DC bias requirement for the serial input signal of the TAXI Receiver. Value of R1 and R2 should provide a suitable DC bias for SERIAL IN, which are a pair of differential PECL input. TAXI chip, and many other hybrid IC (TTL+ECL), shift the DC level of the standard ECL signal by +5V, which is the so-called Pseudo ECL (PECL). 3.7V is the midpoint of the PECL signal swing. It swings $\pm 800\text{mV}$ around 3.7V.

Values of the components are tabulated in Table 5.2. The transformer used in the NIC is a 16 pin DIP IC-liked component, which contains three transformers in one package.

Component	Value
R1, R2	330 Ω
R3, R4	27 Ω
C1, C2, C3, C4	0.1 μF
R5, R6	33 Ω
R7, R8	100 Ω

Table 5.2: Value of the components in Serial Interface Circuit

5.4 Design of the Hub/Router

In the demonstration, the hub is integrated with the CUMLAUDE NET router in a single PCB for better efficiency and integration. A brief introduction of the CUMLAUDE NET will first be covered. Then we will go into detail of the design of the hub/router. Since burst mode receivers are not commercially available, a concentrator is built to emulate the HFC environment. We will go through the design of the concentrator in the last section.

5.4.1 CUMLAUDE NET

CUMLAUDE NET[15] is a Gigabit hierarchical ring network developed in the Chinese University of Hong Kong. It is originated from the ACTA protocol[26, 27]. The network architecture of CUMLAUDE NET is shown in Figure 5.10. An operational dual ring, each running 100Mbps, has been developed (Level 1).

The dual ring is formed by several routers connecting together. Each 100 Mbps router has three ports, two for the dual-ring attachment (router modules) and one for local attachment (hub module). For a perfect integration, the BEBP algorithm is implemented directly on the hub module. The controller on the

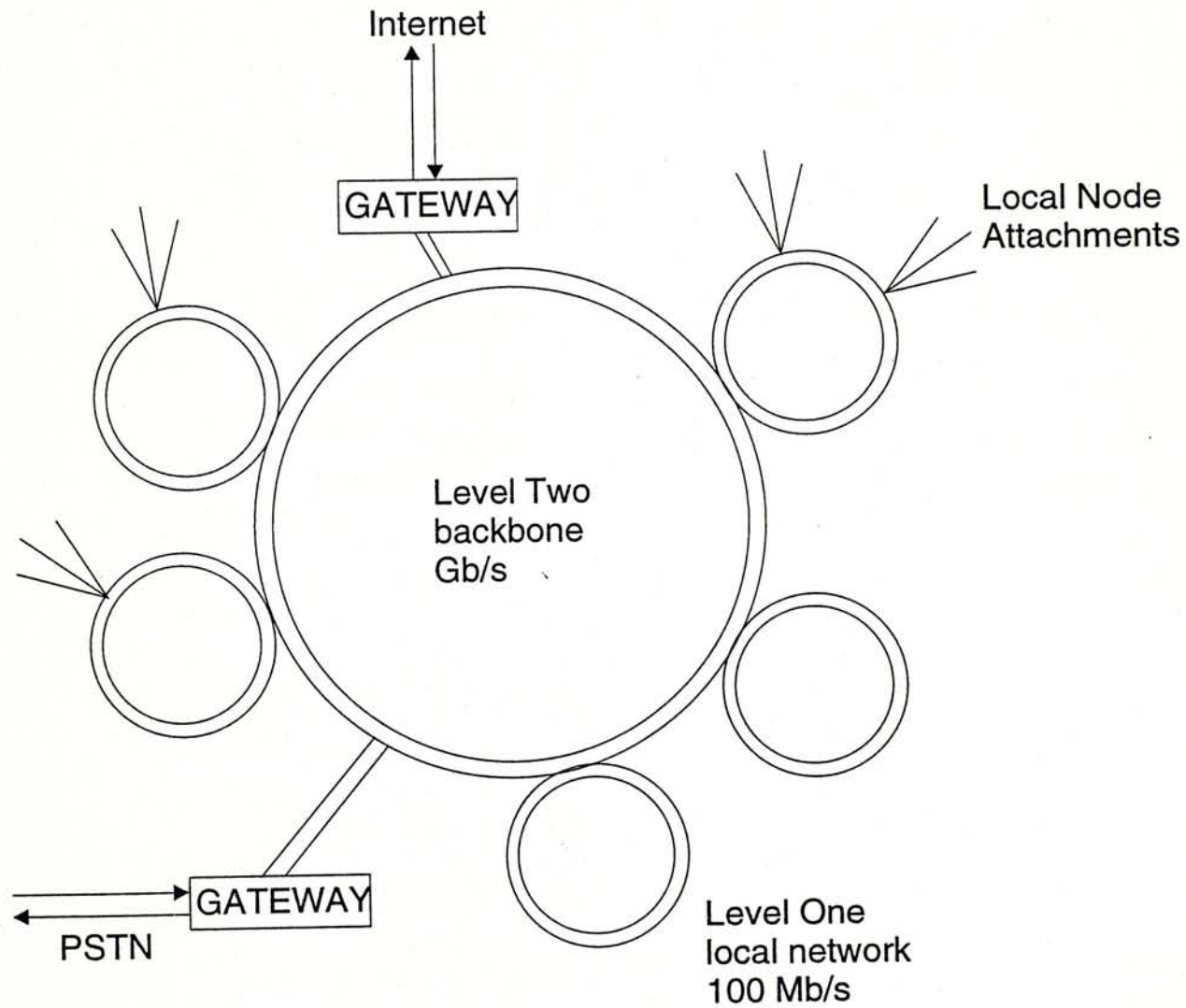


Figure 5.10: Network configuration of the CUMLAUDE NET

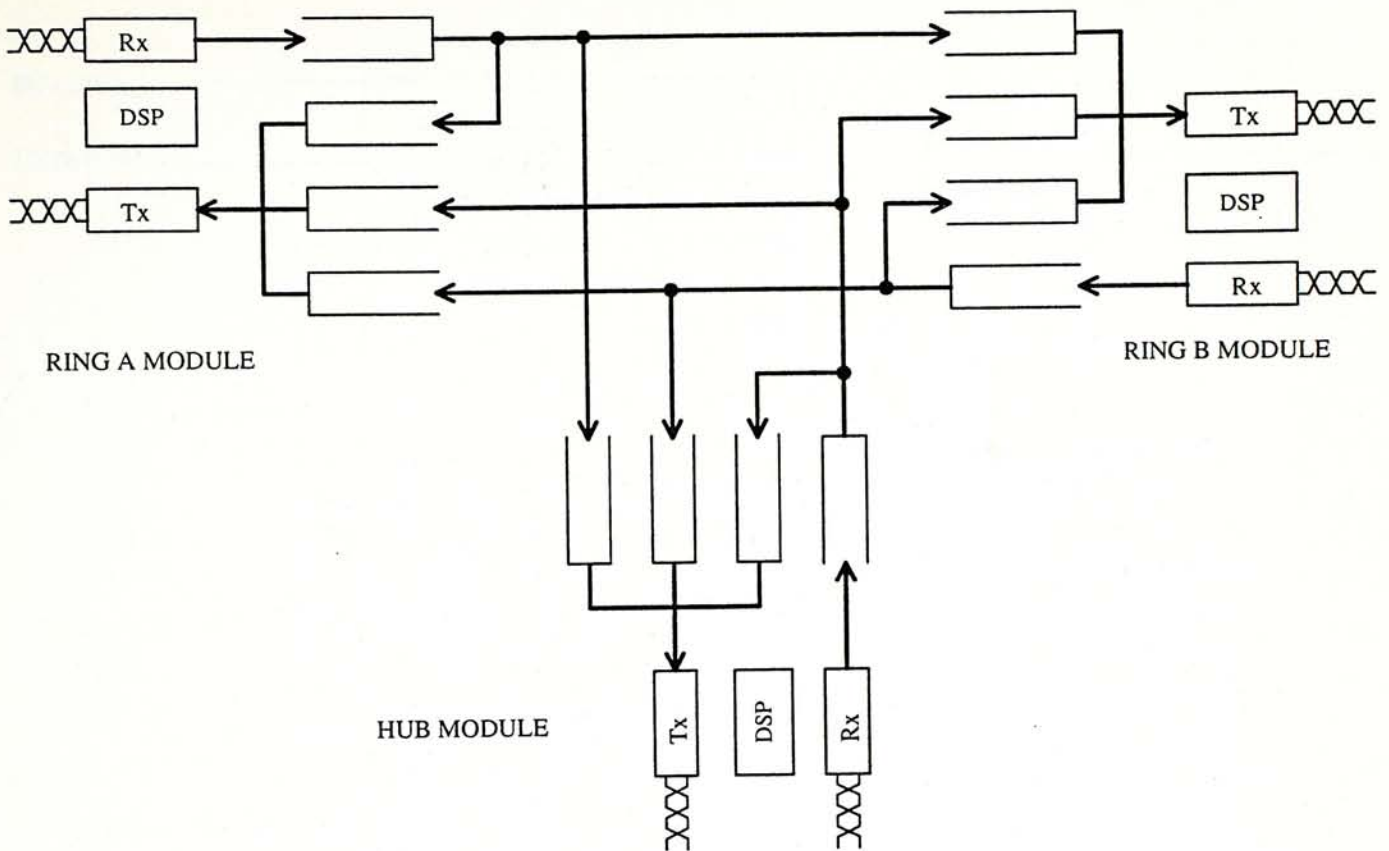


Figure 5.11: Block diagram of the router/hub

router board handles all the polling and routing algorithm.

5.4.2 Hub/Router

Figure 5.11 shows the block diagram of the router/hub. There are three independent controllers on the router board, Ring A and Ring B controller handle the routing in Ring A and Ring B according to the ACTA protocol. While the hub controller will generate poll commands according to the BEBP algorithm.

Packets received in any one modules are first examined by their own controller, according to the destination address, packets will be router to the appropriate output buffer for transmission. To avoid contention, all the possible paths are delicated path. Circuit diagrams for the hub/router are attached in

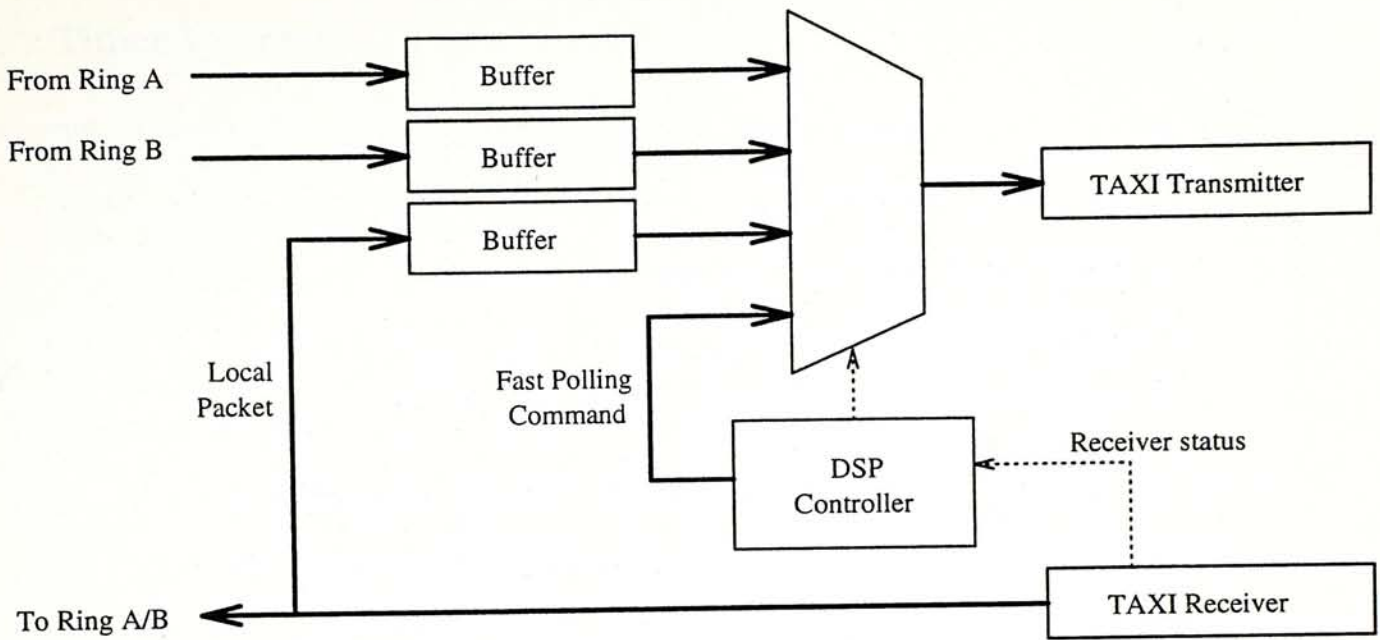


Figure 5.12: Block Diagram of the Hub.

Appendix D.2 to D.5.

Hub Module - Downlink

In the router module, packets in the output buffer will be transmitted following the ACTA protocol. While in the hub module, the packets will be transmitted in a round-robin basis. Other algorithm can also be used to improve the fairness and provide priority.

Figure 5.12 shows the block diagram of the hub module. The BEBP algorithm is handled by the DSP controller, which is the ADSP-2101[51] of Analog Device Inc. The packets in the three output buffers will be directed to the TAXI transmitter in a round-robin basis. Whenever the DSP wants to insert poll commands in the downlink, it will temporarily stop the transfer of packets from the output buffers. Which will be resumed after the transmission of the poll commands.

Timer Interrupt

The BEBP algorithm is implemented by timer-interrupt of DSP chip. There are two registers in ADSP-2101 to handle the timer, TCOUNT and TPERIOD. The count register, TCOUNT, will decrease by 1 for every instruction cycle. When TCOUNT reaches zero, an interrupt is generated, and TCOUNT is then reloaded the value from TPERIOD register.

In the beginning of the timer interrupt routine, TPERIOD will be equal to N_TIMER, which correspond to a period of t_{gu} . Then the packet transfer in TxFIFO is paused, a poll command is transmitted in the downlink, and then the packet transfer is resumed. If a packet is returned before another timer interrupt is received, this received packet will generate another interrupt, which will call the Packet Received Interrupt Routine. Such routine will change TPERIOD to P_TIMER, which correspond to $t_{gu} + t_{pkt}$. With this change, next timer interrupt will be delayed to allow enough time for the whole packet to receive completely. On the other hand, if no packet is received, the DSP will become idle until the next timer interrupt.

Hub Module - Uplink

When a packet is received from the TAXI receiver, it will be stored in the input buffer. Meanwhile an interrupt is generated, where the program will jump to the Packet Received Interrupt Routine. The DSP will read the first five bytes (the header) of the packet for address solving. If the destination address is within the same subnet, the packet will route to the local output buffer for downlink broadcast. If it is destined to other subnets, the packet will forward to the output buffer of the other router modules (Ring A or Ring B) accordingly.

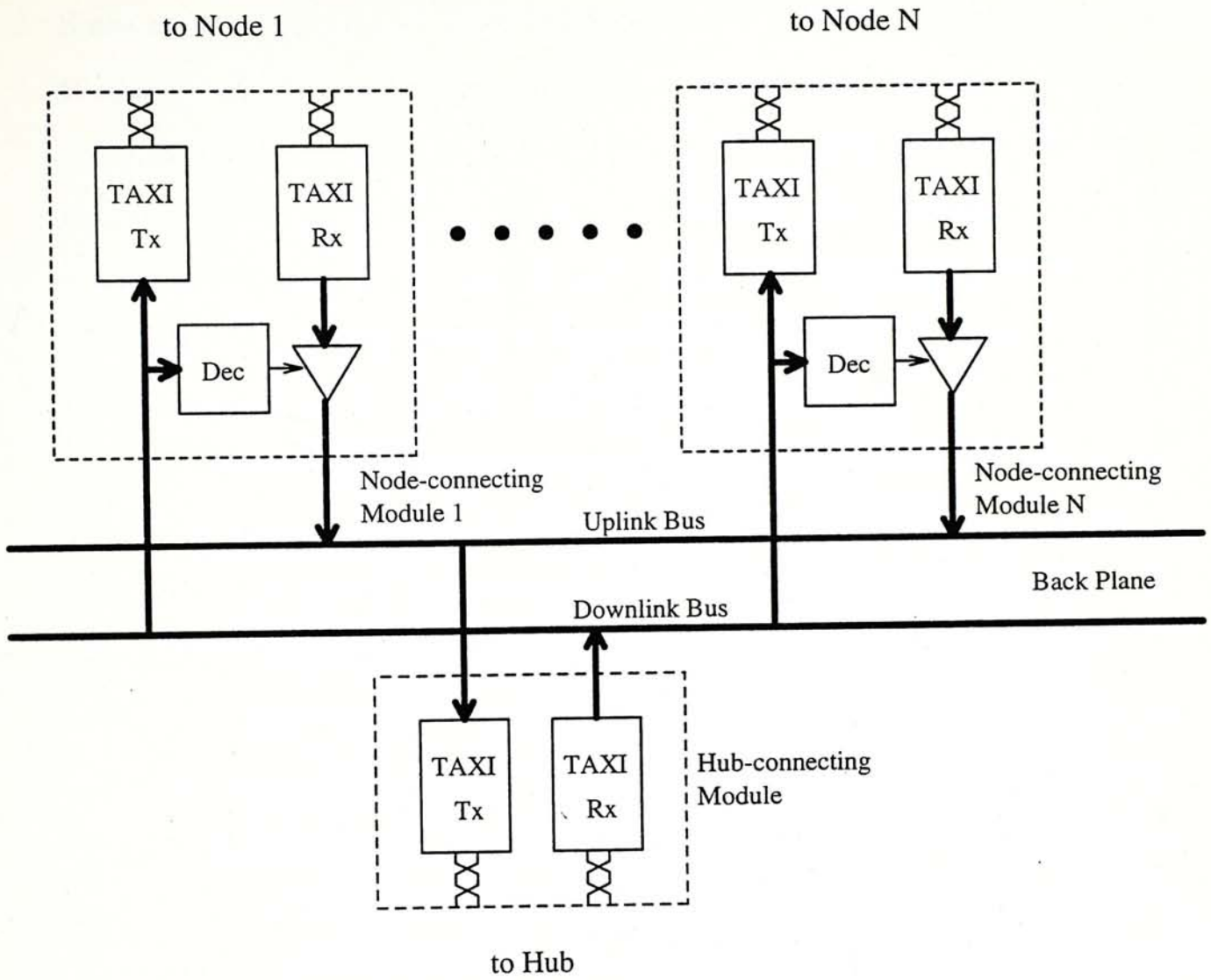


Figure 5.13: Block diagram of the Concentrator

All the above circuit are integrated in two ispLSI-1032 chips. The DSP program for the Hub is written in Assembly and is attached in Appendix F for reference.

5.4.3 Concentrator

Since burst mode receiver is not available in the market, a concentrator is built to emulate the HFC environment using continuous mode TAXI transceiver. Figure 5.13 shows the design of it. Every link is synchronized, the link selection is done on the circuit board rather than in the cable. On the passive backplane (Appendix D.6), there are two shared bus, the uplink bus and the downlink bus. All the hub-connecting module and node-connecting modules are connected on the backplane through the DIN41612 style connectors.

In the hub-connecting module (Appendix D.7), all the data received from the hub is broadcast to the downlink bus, while all the data on the uplink bus are transmitted to the hub. In the node-connecting module (Appendix D.8), the uplink is isolated from the backplane by a 9-bit bus buffer. The buffer will be opened when the decoder on the node-connecting module detected a poll command addressed to it. With such a device, the hub will switch between different nodes according to the poll commands issued, which can emulate the environment in the HFC environment.

5.5 Software - Device Driver

Device driver is a kernel software for the Operating System (OS) to control the hardware. Usually, the device driver will define some API for the OS. Such that application program can call the hardware through the API.

We choose to develop a UNIX device driver for the NIC because BEBP is a native IP network. A public domain UNIX called Linux is used. All the source codes of Linux is available in the public domain which is very convenience for development. In a UNIX system, device driver for network card is

called network driver. It has some special characteristics which differs from other character driver for other peripherals. A network driver should have the following functions:

- Interface to the IP layer
 1. return a value to the IP layer whether the packets to be sent is successful, failure or the network is busy
 2. pass the packets received from the network to the IP layer
- Control of the NIC
 1. monitor the status of network for proper flow control
 2. reset the network card under request from kernel (e.g. bootup)
 3. generate warning to kernel in case of emergency, e.g. too many corrupted packets, cable fault, etc.

Nearly the whole UNIX OS is written in C. For convenience, the network driver of NIC is also written in C. The source code for the driver and header file is attached in Appendix G. One of the special characteristics of network driver is that it does not have a `main()` routine. What a network driver has to do is to fill in a structure called `device`, by specifying the procedures for each function calls. There are 6 major functions : `nic_init()`, `nic_open()`, `nic_close()`, `nic_intr_handler()`, `nic_poll()`, `nic_start_xmit()`. By these functions, the kernel can control the NIC properly.

`nic_init()` will be called when the system is first bootup. Many key constants for the kernel is defined by this function, e.g. NIC packet size, MTU, IRQ

number of the NIC, etc. The OS will check the existence of the hardware and detect whether the hardware configuration of several devices have be collided. `nic_init()` provides all these critical information for the kernel.

`nic_open()` will be called by an application program. It can be part of the bootup script of the OS, or a command enter by the user. Major function of it is to reset the NIC. All the FIFO, Poll Mask, IRQ and other status will be reset. The IP address is also loaded to the NIC hardware by this function.

`nic_close()` will “turn-off” the NIC. All the IRQ, memory allocated for the NIC, and other system resources will be released. This function will be called by some system call of the OS like reboot, halt, etc.

`nic_intr_handler()` is the interrupt handler of the NIC. Whenever an interrupt which matched the IRQ number specified in the `nic_init()` is received, the kernel will call this function. It will first acknowledge the IRQ, check the IRQ register, then call the appropriate routine. If the IRQ is caused by a cable fault (VLTN), a message will prompt the user for the error. If the IRQ is caused by a received packet, an internal routine called `net_rx()` will be called. In every `net_rx()`, one packet will be read from the NIC Rx FIFO, and write to the kernel buffer. We use a while loop to read packet from the Rx FIFO, whenever the Rx FIFO is not empty, `net_rx()` will call once. With this approach, several packets can be read within one IRQ, which can solve the IRQ overlapping problem. Observations show that there can be as more as 8 packets received in one IRQ under busy condition.

`nic_poll()` is the polling routine of the NIC. The OS will call this routine periodically. This kind of polling routine is especially suitable for scheduled application. In the final version of the driver, `nic_poll()` routine is nearly empty.

At first, we use polling rather than interrupt to receive packets. That is, the kernel will poll the status of the RxFIFO periodically, If the RxFIFO is not empty, packets will be read. We are afraid that there will be too many context switch for the CPU to handle if interrupt is used to receive packet. But in the final design, where several packets are read within one IRQ routine, the context switch are not so frequent.

`nic_start_xmit()` is called whenever the kernel wants to send a packet to the network. Upper layer like IP will call this function for packet transmission. The TxFIFO status will first be checked for flow control. If the TxFIFO cannot occupy the incoming packet, this function will return a "busy" to the kernel. When the TxFIFO is available, an internal function `nic_write()` will be called, which will send the packet to the NIC.

For more details, please refer to the source code attached in Appendix G.

5.6 Testing of NIC

With the device driver for NIC installed in the system, many standard UNIX application can be used to test the NIC, which include PING, FTP, TELNET, etc. Other than these application level tests, two more low-level testing program is written to test the NIC. They are the Packet Error Rate Testing and UDP Transfer Rate Testing. The testing results are summarized in the following sections.

All the following tests are run on host machines with the following hardware and software configurations:

CPU : Intel 80486 66MHz DX2

RAM : 16 MBytes
IDE : IDE Add-on Board with 1 MByte Cache (VL-Bus)
Display : Super VGA Card, 1 Mbyte RAM on board (VL-Bus)
OS (DOS) : MS DOS Ver. 6.22
OS (Linux) : Linux ver. 1.1.8

5.6.1 Packet Error Rate Testing

This is a self-to-self testing of the NIC. One packet will be sent out to the NIC, which will be routed back by the hub later. After the packet is returned, the program will compare the content of the packet byte by byte. The content of the packet is randomly generated for better testing. The program is written in Turbo C under DOS environment. The source code is attached in Appendix H.1.

This is the typical result of the testing program:

```
CUMLAUDE NIC Loop Test finished!
```

```
No. of packets tested : 1142706  
No. of errors found : 0  
Packet Error Rate (PER): 0.000000  
No. of violation = 0
```

```
Error occurred at loop :
```

```
Violation occurred at loop :
```

No packet error is observed for over 1 million of packets. This corresponds to a Packet Error Rate (PER) of less than 10^{-6} . Or a Bit Error Rate of less than 10^{-9} .

5.6.2 UDP Transfer Rate Testing

TCP/IP is a very reliable protocol to provide high quality connection, which is especially suitable for computer network. Nearly all UNIX application are built on TCP/IP. But TCP/IP is not a very good protocol for testing of the network. The self recovery error routine, like retransmission, packet acknowledgement, will mask out a lot of network error. Therefore a UDP/IP testing program using datagram is written to test the network.

The source code of the testing program is listed in Appendix H.2.1 to Appendix H.2.5. It is a client-server testing program, where a client program (udplici) will run on one machine while a server program (udpserv) is run on another machine. The dgcli() and dgecho() provide an interface for the udpcli() and udpserv() to call the lower layer respectively. The function dgcli() will continuously send UDP packet into the network, once the connection is successfully set up. The dgecho() will continuously receive UDP packets and do error check. Data transfer rate is reported by the client - dgcli().

Different configurations are tested with the UDP program, like different size of network (4 to 64 nodes), both client and server on the same subnet (attached to the same hub), client and server attached to different hubs which are connected by CUMLAUDE NET Router, etc. No significant differences are reported. The transfer rate is always kept between 630 KByte/s to 680 KByte/s.

As discussed before, the major bottleneck of the existing NIC is the ISA Bus. 600 Kbytes/s has already approached the limit of the ISA Bus transfer rate.

5.6.3 Other Applications

PING

The ping application will send a ICMP packet to the network, and wait for the destination machine to echo back the packet. If the packet is successfully echo back, the delay will be recorded, which called the PING time. The PING time is around 3.2ms to 3.6ms for the BEBP.

TELNET

In a TELNET terminal, each key stroke will create four packets on the network. First, the client sends the packet to the server containing information about which key is pressed by the user. The server sends back a packet to acknowledge the reception. Then the server sends a packet to display the "key" on the client's terminal. The client sends back a packet to acknowledge the reception. Although the handshaking is rather complicated, all characters can be displayed immediately after the key strokes. No delay is observed for any key strokes.

FTP

FTP provides a very simple way to test the file transfer rate of the network. Basically, this can reflect the transfer rate of TCP/IP. Small file will produce unreliable data, so file of 2 MByte is used in the test. The FTP file transfer rate is recorded to be 200 KByte/s to 230 KByte/s. No significant differences are

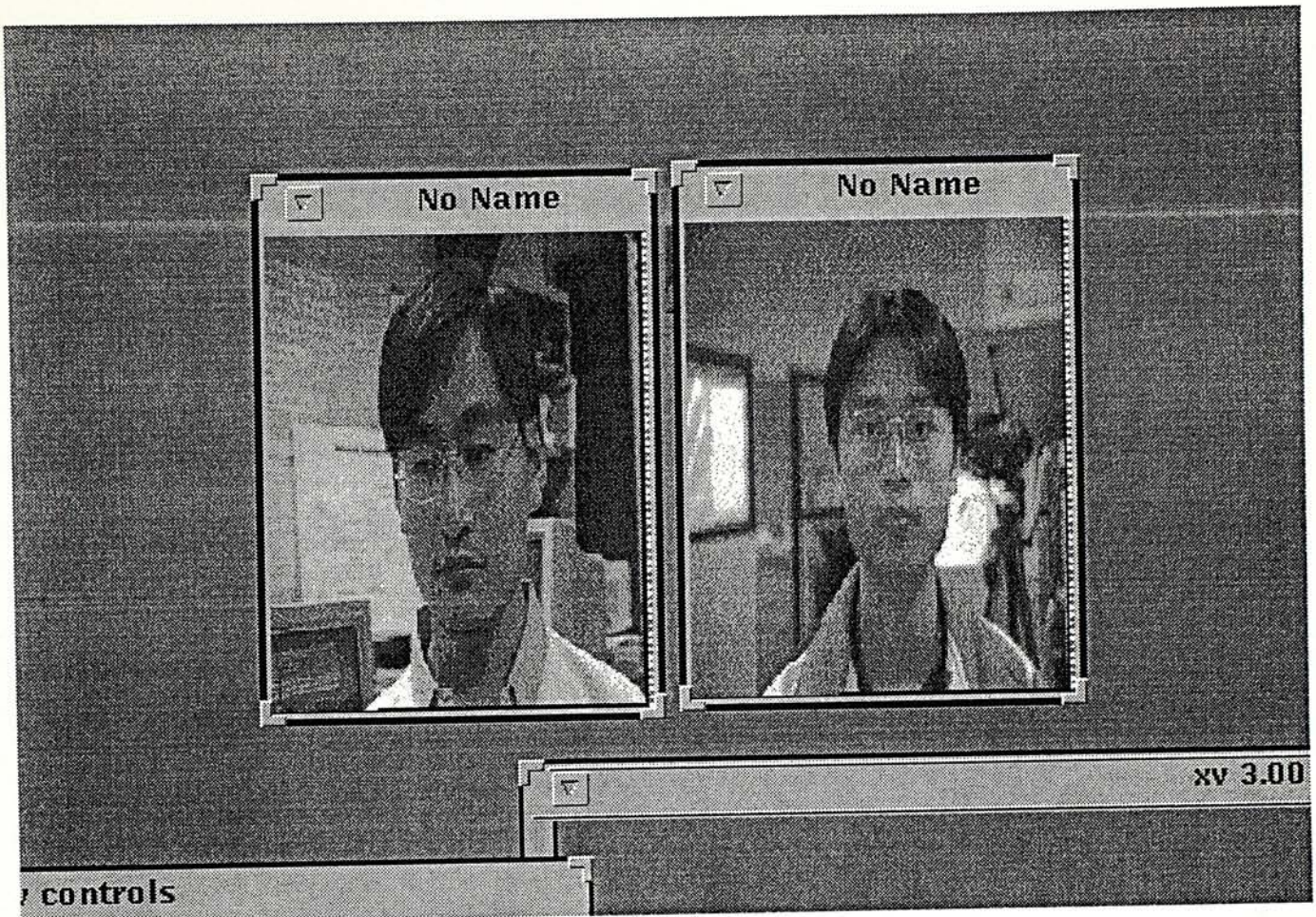


Figure 5.14: Video Conferencing using X-window Remote Display

observed for different configuration.

Remote Display

With the remote display capability of the X-window system, a simple video conferencing system is demonstrated. As shown in Figure 5.14, one window is a local display, while the other window is a remote display. Due to the limited bandwidth of the ISA bus and the inefficient transmission of TCP/IP, only seven frames per second of video can be achieved. Better performance can be obtained by developing a video conferencing system using UDP, and a faster video capture card.

Chapter 6

Conclusion

A Fast Polling Protocol has been proposed to provide collision-free media access in the Media Access Control (MAC) layer. The protocol is based on the Binary Exponential Backoff Polling algorithm to improve the throughput efficiency and to guarantee the performance of connection-oriented isochronous services. Both experimental demonstration (based on TAXI chip datalinks) and network simulations have been performed. The performance is found to be excellent. Bandwidth efficiency up to 95% can be achieved in the uplink, while over 85% efficiency can be maintained in the downlink even in the worst case. Network access delay for packets is guaranteed to be less than 1 ms under normal loading. In addition, both bandwidth utilization and the access delay is fair for every nodes.

We have also demonstrated a low-cost, 100-Mb/s multimedia network (LAN) that is compatible to most existing network architectures. Thus, broadband services can be easily provided without having to reinstall the existing cables / wires. For example, it can provide a simple method to upgrade the existing

10 Mb/s Ethernet-based LANs to 100-Mb/s multimedia networks. This is very important since 10Base2 and 10BaseT Ethernets are very popular in commercial offices and campuses, and a large volume of coaxial and UTP cables have already been installed in most commercial buildings. The proposed network can also be used as a low-cost ATM traffic concentrator at the hub.

Most importantly, the Fast Polling MAC protocol and the Binary Exponential Backoff Polling algorithm is compatible with the Hybrid Fiber-Coax (HFC) architecture, which is a very promising architecture for bringing future multimedia broadband services to the residential subscribers, and a large volume of coaxial cables has been installed by the CATV company, reaching a large percentage of homes. Thus, the Fast Polling Protocol provides a low-cost solution to the unification of LAN services and CATV services, and it works on all of the mentioned network architectures and physical layer media.

We believe that Fast Polling protocol with the Binary Exponential Backoff Polling algorithm will play an important role in the future integrated multimedia network. Further development work is still in progress to resolve the issues on spectrum utilization, power budgeting, and other datalink layer implementation issues.

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Appendix A

Abbreviation

ACTA	Adaptive Control Tunnable Channel Multiple Access
ANSI	American National Standards Institute
ARP	Address Resolution Protocol
ATM	Asynchronous Transfer Mode
BEBP	Binary Exponential Backoff Polling
BER	Bit Error Rate
CATV	Cable Television
CCITT	Consulting Committee International Telephone and Telegraph
CDDI	Copper Wire Distributed Data Interface
CDTP	Count Down To Poll Counter
CMOS	Complementary Metal Oxide Semiconductor
CPU	Central Processing Unit
CSMA	Carrier Sense Multiple Access
DEMUX	DeMultiplexer

DMA	Direct Memory Access
DSP	Digital Signal Processor
ECL	Emitter Coupled Logic
EISA	Extended Industrial Standard Architecture
FDDI	Fiber Wire Distributed Data Interface
FDM	Frequency Division Multiplexing
FEXT	Far End Cross Talk
FIFO	First In First Out
FTP	File Transfer Protocol
GAL	Gate Array Logic
HDLC	High-level Data Link Control
HFC	Hybrid Fiber Coax
ICMP	Internet Control Message Protocol
IDE	Intergrated Drive Electronics
IEEE	Institute of Electrical and Electronics Engineers
I/O	Input / Output
IP	Internet Protocol
IRQ	Interrupt
ISA	Industrial Standard Architecture
ispLSI	In-System Programmable Large Scale Integration
JPEG	Joint Photographic Experts Group
LAN	Local Area Network
LLC	Logic Link Control
MAC	Medium Access Control
MLT3	3-level Multi-Level Transition Coding

MMF	Multimode Fiber
MPEG	Motion Picture Experts Group
MTU	Maximum Transfer Unit
MUX	Multiplexer
NIC	Network Interface Card
NRZ	Non-Return to Zero
PCB	Printed Circuit Board
PCI	Peripheral Component Interconnect
PDU	Protocol Data Unit
PECL	Pseudo Emitter Coupled Logic
PLCC	Plastic Leaded Chip Carrier
PLD	Programmable Logic Device
PLL	Phase-Lock Loop
RFC	Request For Comments
RxFIFO	Receiver First In First Out Memory
RxSM	Receiver State Machine
SONET	Synchronous Optical Network
STP	Shielded Twisted Pair
TCP	Transmission Control Protocol
TxFIFO	Transmitter First In First Out Memory
TxSM	Transmitter State Machine
UDP	User Datagram Protocol
UTP	Unshielded Twisted Pair
VESA	Video Electronics Standards Association
VGA	Video Graphic Array

VLTN Violation

WWW World Wide Web

Appendix B

Simulation Source Code

beb.sim

```
DO
LET DATA.ARRIVAL.RATE = MAX.THROUGHPUT * OFFERED.LOAD / NUM.ACTIVE.NODE
LET TIME.INTERVAL = PACKET.SIZE/DATA.ARRIVAL.RATE * 1000
PRINT 3 LINE WITH N.NODE, NUM.ACTIVE.NODE, N.NODE-NUM.ACTIVE.NODE THUS
THE TOTAL NUMBER OF NODE IS *****
THE TOTAL NUMBER OF ACTIVE NODE IS *****
THE TOTAL NUMBER OF INACTIVE NODE IS *****
PRINT 1 LINE WITH PACKET.SIZE THUS
THE PACKET SIZE IS **** BYTES
PRINT 1 LINE WITH DATA.ARRIVAL.RATE THUS
THE PACKET ARRIVAL RATE OF EACH ACTIVE NODE IS ***** KBYTE/SEC
PRINT 1 LINE WITH PACKET.TRANSFER.TIME THUS
THE PACKET TRANSFER TIME IS **** US
PRINT 1 LINE WITH FIFO.SIZE THUS
THE FIFO SIZE IS **K BYTES
PRINT 1 LINE WITH FILENAME THUS
THE RESULT WILL BE WRITTEN TO *****
PRINT 1 LINE WITH END.TIME.SEC THUS
THE SIMULATION START..... FOR **..**** SECONDS

LET SAMPLING.TIME = 1000
LET POLL.SHORT.INTERVAL = 2
LET POLL.LONG.INTERVAL = PACKET.SIZE / MAX.THROUGHPUT * 1000
+ POLL.SHORT.INTERVAL
LET MAX.WAIT.LEVEL = 256
LET MAX.IP.BUFFER = 200
LET IP.POLL.TIME = 50
LET PACKET.RETURN = 0
LET END.TIME = END.TIME.SEC * 1000000
RESERVE NODEPTR(*) AS N.NODE
RESERVE GENPTR(*) AS N.NODE
RESERVE PKTTRAN(*) AS N.NODE

FOR M = 1 TO N.NODE
DO
CREATE A NODE CALLED NODEPTR(M)
ACTIVATE A PACKET.TRANSFER CALLED PKTTRAN(M) GIVING M NOW
ACTIVATE A PACKET.GENERATOR CALLED GENPTR(M) GIVING M NOW
ACTIVATE A NODE CALLED NODEPTR(M) GIVING M NOW
LOOP

FOR M = 1 TO N.NODE
STATUS(GENPTR(M)) = 0
FOR M = 1 TO NUM.ACTIVE.NODE
STATUS(GENPTR(M)) = 1
ACTIVATE A HUB NOW
ACTIVATE A INFO.COLLECT NOW
ACTIVATE A STOP.SIM IN END.TIME US
START SIMULATION
END

PROCESS NODE GIVEN INDEX
DEFINE INDEX AS AN INTEGER VARIABLE
LET ADDRESS(NODEPTR(INDEX)) = INDEX
UNTIL TIME.V > END.TIME
```

```
DO
IF (TIME.V = 0)
LET POLL.COUNT(NODEPTR(INDEX)) = 0
SUCCESS.NUM(NODEPTR(INDEX)) = 0
QUEUE.DELAY(NODEPTR(INDEX)) = 0
ACCESS.DELAY(NODEPTR(INDEX)) = 0
FIFO.OCCUPIED(NODEPTR(INDEX)) = 0
SUSPEND
ALWAYS
ADD 1 TO POLL.COUNT(NODEPTR(INDEX))
IF ( (PACKET.QUEUE(NODEPTR(INDEX)) IS EMPTY) OR
(STATUS(NODEPTR(INDEX)) = 1) )
PACKET.RETURN = 0
ALWAYS
IF ( (PACKET.QUEUE(NODEPTR(INDEX)) IS NOT EMPTY) AND
(STATUS(NODEPTR(INDEX)) = 0) )
PACKET.RETURN = 1
REMOVE THE FIRST PACKET FROM PACKET.QUEUE(NODEPTR(INDEX))
ADD 1 TO SUCCESS.NUM(NODEPTR(INDEX))
SUBTRACT 1 FROM FIFO.OCCUPIED(NODEPTR(INDEX))
ADD (TIME.V - TOTOP.TIME(PACKET)) TO ACCESS.DELAY(NODEPTR(INDEX))
ADD (TOTOP.TIME(PACKET) - ARRIVAL.TIME(PACKET)) TO
QUEUE.DELAY(NODEPTR(INDEX))
DESTROY THIS PACKET
IF FIFO.OCCUPIED(NODEPTR(INDEX)) NOT EQUAL TO 0
REMOVE THE FIRST PACKET FROM PACKET.QUEUE(NODEPTR(INDEX))
LET TOTOP.TIME(PACKET) = TIME.V
FILE THIS PACKET FIRST IN PACKET.QUEUE(NODEPTR(INDEX))
ALWAYS
ALWAYS
SUSPEND
LOOP
END

PROCESS HUB
DEFINE INDEX AS AN INTEGER VARIABLE
DEFINE WAIT.COUNT AS AN INTEGER 1-DIMENSIONAL VARIABLE
DEFINE WAIT.LEVEL AS AN INTEGER 1-DIMENSIONAL VARIABLE
RESERVE WAIT.COUNT(*) AS N.NODE
RESERVE WAIT.LEVEL(*) AS N.NODE
FOR INDEX = 1 TO N.NODE
WAIT.COUNT(INDEX) = 1
FOR INDEX = 1 TO N.NODE
WAIT.LEVEL(INDEX) = 1
UNTIL (TIME.V > END.TIME)
DO
FOR INDEX = 1 TO N.NODE
DO
```


beb.sim

```
WRITE TOTAL.PKT/END.TIME.SEC/NUM.ACTIVE.NODE
AS "AVERAGE NO OF PACKETS SENT BY EACH NODE : ", D(8, 2), " PACKET/SEC"
START NEW LINE
WRITE (TOTAL.PKT/NUM.ACTIVE.NODE/END.TIME.SEC) * PACKET.SIZE / 1000
AS "AVERAGE THROUGHPUT FOR EACH ACTIVE NODE : ", D(13,4), " KBYTE/SEC"
START NEW LINE
WRITE ALL.QUEUE.DELAY / TOTAL.PKT
AS "AVERAGE PACKET QUEUEING DELAY OVER ALL NODES : ", D(10,2), " US"
START NEW LINE
WRITE ALL.ACCESS.DELAY / TOTAL.PKT
AS "AVERAGE ACCESS DELAY OVER ALL NODES : ", D(10,2), " US"
START NEW LINE
WRITE ALL.TOTAL.QLEN * SAMPLING.TIME / END.TIME / NUM.ACTIVE.NODE
AS "AVERAGE NO OF PACKET IN NIC FIFO : ", D(13,6), " PACKETS"
CLOSE UNIT 10
STOP
END
START NEW LINE
WRITE N.NODE AS "NUMBER OF NODES : ", I 3
START NEW LINE
WRITE NUM.ACTIVE.NODE AS "NUMBER OF ACTIVE NODE : ", I 3
START NEW LINE
WRITE MAX.THROUGHPUT
AS "THE MAXIMUM THROUGHPUT OF THE NETWORK : ", D(8,2), " KBYTE/SEC"
START NEW LINE
WRITE FIFO.SIZE AS "SIZE OF FIFO IN NIC : ", I 3, " KBYTES"
START NEW LINE
WRITE TIME.V AS "SIMULATION TIME : ", D(13,2), " US"
START NEW LINE
WRITE PACKET.TRANSFER.TIME
AS "PACKET TRANSFER TIME OF THE NIC INTERFACE BUS : ", I 4, " US"
START NEW LINE
WRITE OFFERED.LOAD
AS "TOTAL OFFER LOAD RATIO FOR ALL NODES : ", D(5,3)
START NEW LINE
WRITE DATA.ARRIVAL.RATE
AS "DATA ARRIVAL RATE FOR EACH ACTIVE NODE : ", D(13,2), " KBYTE/SEC"
START NEW LINE
WRITE DATA.ARRIVAL.RATE * 1000 / PACKET.SIZE
AS "PACKET ARRIVAL RATE FOR EACH ACTIVE NODE : ", D(13,2), " PACKET/SEC"
START NEW LINE
WRITE CYCLE.NUM(HUB) / END.TIME.SEC
AS "NO OF POLL CYCLE EXECUTED BY THE HUB PER SEC : ", D(13,0)
START NEW LINE
WRITE ACTIVE.POLL.COUNT / NUM.ACTIVE.NODE / END.TIME.SEC
AS "AVERAGE POLL RECEIVED BY ACTIVE NODE PER SEC : ", D(15,2)
IF NUM.ACTIVE.NODE < N.NODE
START NEW LINE
WRITE IDLE.POLL.COUNT / (N.NODE - NUM.ACTIVE.NODE) / END.TIME.SEC
AS "AVERAGE POLL RECEIVED BY INACTIVE NODE PER SEC : ", D(15,2)
ALWAYS
START NEW LINE
WRITE TOTAL.PKT/END.TIME.SEC
AS "TOTAL NUMBER OF PACKET TRANSMITTED : ", I 10, " PACKET/SEC"
START NEW LINE
WRITE TOTAL.PKT/END.TIME.SEC * PACKET.SIZE / 1000
AS "TOTAL THROUGHPUT OF THE NETWORK : ", D(13,2), " KBYTE/SEC"
START NEW LINE
WRITE TOTAL.PKT/END.TIME.SEC * PACKET.SIZE / MAX.THROUGHPUT / 1000
AS "BANDWIDTH EFFICIENCY OF THE NETWORK : ", D(5,4)
START NEW LINE
```


Appendix C

Simulation Results

Ref.	Polling Algorithm	No. of Nodes	No. of Act. Nodes	Offered Load	FIFO Size	Host Bus Tran Time	Packet Size
int1	Round Robin	64	1	0.25-1.5	1 KBytes	0 μ s	516 Bytes
int2	Round Robin	64	2	0.25-1.5	1 KBytes	0 μ s	516 Bytes
int4	Round Robin	64	4	0.25-1.5	1 KBytes	0 μ s	516 Bytes
int8	Round Robin	64	8	0.25-1.5	1 KBytes	0 μ s	516 Bytes
int16	Round Robin	64	16	0.25-1.5	1 KBytes	0 μ s	516 Bytes
int32	Round Robin	64	32	0.25-1.5	1 KBytes	0 μ s	516 Bytes
int64	Round Robin	64	64	0.25-1.5	1 KBytes	0 μ s	516 Bytes
bin1	BEBP	64	1	0.25-1.5	1 KBytes	0 μ s	516 Bytes
bin2	BEBP	64	2	0.25-1.5	1 KBytes	0 μ s	516 Bytes
bin4	BEBP	64	4	0.25-1.5	1 KBytes	0 μ s	516 Bytes
bin8	BEBP	64	8	0.25-1.5	1 KBytes	0 μ s	516 Bytes
bin16	BEBP	64	16	0.25-1.5	1 KBytes	0 μ s	516 Bytes
bin32	BEBP	64	32	0.25-1.5	1 KBytes	0 μ s	516 Bytes
bin64	BEBP	64	64	0.25-1.5	1 KBytes	0 μ s	516 Bytes
n1	BEBP	1	1	0.25-1.5	1 KBytes	0 μ s	516 Bytes
n2	BEBP	2	2	0.25-1.5	1 KBytes	0 μ s	516 Bytes
n4	BEBP	4	4	0.25-1.5	1 KBytes	0 μ s	516 Bytes
n8	BEBP	8	8	0.25-1.5	1 KBytes	0 μ s	516 Bytes
n16	BEBP	16	16	0.25-1.5	1 KBytes	0 μ s	516 Bytes
n32	BEBP	32	32	0.25-1.5	1 KBytes	0 μ s	516 Bytes
n64	BEBP	64	64	0.25-1.5	1 KBytes	0 μ s	516 Bytes
n128	BEBP	128	128	0.25-1.5	1 KBytes	0 μ s	516 Bytes
f1	BEBP	64	4	0.25-1.5	1 KBytes	0 μ s	516 Bytes
f4	BEBP	64	4	0.25-1.5	1 KBytes	0 μ s	516 Bytes
f8	BEBP	64	4	0.25-1.5	1 KBytes	0 μ s	516 Bytes
tn4	BEBP	64	4	1	1 KBytes	0-600 μ s	516 Bytes
t0	BEBP	64	4	0.25-1.5	1 KBytes	0 μ s	516 Bytes
t200	BEBP	64	4	0.25-1.5	1 KBytes	200 μ s	516 Bytes
t400	BEBP	64	4	0.25-1.5	1 KBytes	400 μ s	516 Bytes
t600	BEBP	64	4	0.25-1.5	1 KBytes	600 μ s	516 Bytes
p32	BEBP	64	4	0.25-1.5	1 KBytes	0 μ s	32 Bytes
p64	BEBP	64	4	0.25-1.5	1 KBytes	0 μ s	64 Bytes
p128	BEBP	64	4	0.25-1.5	1 KBytes	0 μ s	128 Bytes
p256	BEBP	64	4	0.25-1.5	1 KBytes	0 μ s	256 Bytes
p512	BEBP	64	4	0.25-1.5	1 KBytes	0 μ s	512 Bytes
p1024	BEBP	64	4	0.25-1.5	1 KBytes	0 μ s	1024 Bytes
pp32	BEBP	64	64	0.25-1.5	1 KBytes	0 μ s	32 Bytes
pp64	BEBP	64	64	0.25-1.5	1 KBytes	0 μ s	64 Bytes
pp128	BEBP	64	64	0.25-1.5	1 KBytes	0 μ s	128 Bytes
pp256	BEBP	64	64	0.25-1.5	1 KBytes	0 μ s	256 Bytes
pp512	BEBP	64	64	0.25-1.5	1 KBytes	0 μ s	512 Bytes
pp1024	BEBP	64	64	0.25-1.5	1 KBytes	0 μ s	1024 Bytes

NUMBER OF NODES : 64
 NUMBER OF ACTIVE NODE : 4
 THE MAXIMUM THROUGHPUT OF THE NETWORK : 12500.00 KBYTE/SEC
 SIZE OF FIFO IN NIC : 8 KBYTES
 SIMULATION TIME : 1000000.00 us
 PACKET TRANSFER TIME OF THE NIC INTERFACE BUS : 0 US
 TOTAL OFFER LOAD RATIO FOR ALL NODES : .250
 DATA ARRIVAL RATE FOR EACH ACTIVE NODE : 781.25 KBYTE/SEC
 PACKET ARRIVAL RATE FOR EACH ACTIVE NODE : 1508.20 PACKET/SEC
 NO OF POLL CYCLE EXECUTED BY THE HUB PER SEC : 1369105.
 AVERAGE POLL RECEIVED BY ACTIVE NODE PER SEC : 14023.75
 AVERAGE POLL RECEIVED BY INACTIVE NODE PER SEC : 5355.00
 TOTAL NUMBER OF PACKET TRANSMITTED : 5987 PACKET/SEC
 TOTAL THROUGHPUT OF THE NETWORK : 3101.27 KBYTE/SEC
 BANDWIDTH EFFICIENCY OF THE NETWORK : .2481
 AVERAGE NO OF PACKETS SENT BY EACH NODE : 1496.75 PACKET/SEC
 AVERAGE THROUGHPUT FOR EACH ACTIVE NODE : 775.3165 KBYTE/SEC
 AVERAGE PACKET QUEUEING DELAY OVER ALL NODES : 7.61 US
 AVERAGE ACCESS DELAY OVER ALL NODES : 80.77 US
 AVERAGE NO OF PACKET IN NIC FIFO : .099500 PACKETS

NUMBER OF NODES : 64
 NUMBER OF ACTIVE NODE : 4
 THE MAXIMUM THROUGHPUT OF THE NETWORK : 12500.00 KBYTE/SEC
 SIZE OF FIFO IN NIC : 8 KBYTES
 SIMULATION TIME : 1000000.00 us
 PACKET TRANSFER TIME OF THE NIC INTERFACE BUS : 0 US
 TOTAL OFFER LOAD RATIO FOR ALL NODES : .500
 DATA ARRIVAL RATE FOR EACH ACTIVE NODE : 1562.50 KBYTE/SEC
 PACKET ARRIVAL RATE FOR EACH ACTIVE NODE : 3016.41 PACKET/SEC
 NO OF POLL CYCLE EXECUTED BY THE HUB PER SEC : 798206.
 AVERAGE POLL RECEIVED BY ACTIVE NODE PER SEC : 16460.50
 AVERAGE POLL RECEIVED BY INACTIVE NODE PER SEC : 3124.95
 TOTAL NUMBER OF PACKET TRANSMITTED : 12044 PACKET/SEC
 TOTAL THROUGHPUT OF THE NETWORK : 6238.79 KBYTE/SEC
 BANDWIDTH EFFICIENCY OF THE NETWORK : .4991
 AVERAGE NO OF PACKETS SENT BY EACH NODE : 3011.00 PACKET/SEC
 AVERAGE THROUGHPUT FOR EACH ACTIVE NODE : 1559.6980 KBYTE/SEC
 AVERAGE PACKET QUEUEING DELAY OVER ALL NODES : 25.54 US
 AVERAGE ACCESS DELAY OVER ALL NODES : 89.12 US
 AVERAGE NO OF PACKET IN NIC FIFO : .269000 PACKETS

NUMBER OF NODES : 64
 NUMBER OF ACTIVE NODE : 4
 THE MAXIMUM THROUGHPUT OF THE NETWORK : 12500.00 KBYTE/SEC
 SIZE OF FIFO IN NIC : 8 KBYTES
 SIMULATION TIME : 1000000.00 us
 PACKET TRANSFER TIME OF THE NIC INTERFACE BUS : 0 US
 TOTAL OFFER LOAD RATIO FOR ALL NODES : .750
 DATA ARRIVAL RATE FOR EACH ACTIVE NODE : 2343.75 KBYTE/SEC
 PACKET ARRIVAL RATE FOR EACH ACTIVE NODE : 4524.61 PACKET/SEC
 NO OF POLL CYCLE EXECUTED BY THE HUB PER SEC : 319072.
 AVERAGE POLL RECEIVED BY ACTIVE NODE PER SEC : 13963.25
 AVERAGE POLL RECEIVED BY INACTIVE NODE PER SEC : 1253.00
 TOTAL NUMBER OF PACKET TRANSMITTED : 18016 PACKET/SEC
 TOTAL THROUGHPUT OF THE NETWORK : 9332.29 KBYTE/SEC
 BANDWIDTH EFFICIENCY OF THE NETWORK : .7466
 AVERAGE NO OF PACKETS SENT BY EACH NODE : 4504.00 PACKET/SEC
 AVERAGE THROUGHPUT FOR EACH ACTIVE NODE : 2333.0720 KBYTE/SEC
 AVERAGE PACKET QUEUEING DELAY OVER ALL NODES : 82.44 US
 AVERAGE ACCESS DELAY OVER ALL NODES : 99.10 US
 AVERAGE NO OF PACKET IN NIC FIFO : .719000 PACKETS

NUMBER OF NODES : 64
 NUMBER OF ACTIVE NODE : 4
 THE MAXIMUM THROUGHPUT OF THE NETWORK : 12500.00 KBYTE/SEC
 SIZE OF FIFO IN NIC : 8 KBYTES
 SIMULATION TIME : 1000000.00 us
 PACKET TRANSFER TIME OF THE NIC INTERFACE BUS : 0 US
 TOTAL OFFER LOAD RATIO FOR ALL NODES : 1.000
 DATA ARRIVAL RATE FOR EACH ACTIVE NODE : 3125.00 KBYTE/SEC
 PACKET ARRIVAL RATE FOR EACH ACTIVE NODE : 6032.82 PACKET/SEC
 NO OF POLL CYCLE EXECUTED BY THE HUB PER SEC : 5832.
 AVERAGE POLL RECEIVED BY ACTIVE NODE PER SEC : 5812.00
 AVERAGE POLL RECEIVED BY INACTIVE NODE PER SEC : 29.00
 TOTAL NUMBER OF PACKET TRANSMITTED : 23194 PACKET/SEC
 TOTAL THROUGHPUT OF THE NETWORK : 12014.49 KBYTE/SEC
 BANDWIDTH EFFICIENCY OF THE NETWORK : .9612
 AVERAGE NO OF PACKETS SENT BY EACH NODE : 5798.50 PACKET/SEC
 AVERAGE THROUGHPUT FOR EACH ACTIVE NODE : 3003.6230 KBYTE/SEC
 AVERAGE PACKET QUEUEING DELAY OVER ALL NODES : 1141.71 US
 AVERAGE ACCESS DELAY OVER ALL NODES : 171.64 US
 AVERAGE NO OF PACKET IN NIC FIFO : 7.477500 PACKETS

NUMBER OF NODES : 64
 NUMBER OF ACTIVE NODE : 4
 THE MAXIMUM THROUGHPUT OF THE NETWORK : 12500.00 KBYTE/SEC
 SIZE OF FIFO IN NIC : 8 KBYTES
 SIMULATION TIME : 1000000.00 us
 PACKET TRANSFER TIME OF THE NIC INTERFACE BUS : 0 US
 TOTAL OFFER LOAD RATIO FOR ALL NODES : 1.250
 DATA ARRIVAL RATE FOR EACH ACTIVE NODE : 3906.25 KBYTE/SEC
 PACKET ARRIVAL RATE FOR EACH ACTIVE NODE : 7541.02 PACKET/SEC
 NO OF POLL CYCLE EXECUTED BY THE HUB PER SEC : 5803.
 AVERAGE POLL RECEIVED BY ACTIVE NODE PER SEC : 5800.75
 AVERAGE POLL RECEIVED BY INACTIVE NODE PER SEC : 29.00
 TOTAL NUMBER OF PACKET TRANSMITTED : 23197 PACKET/SEC
 TOTAL THROUGHPUT OF THE NETWORK : 12016.05 KBYTE/SEC
 BANDWIDTH EFFICIENCY OF THE NETWORK : .9613
 AVERAGE NO OF PACKETS SENT BY EACH NODE : 5799.25 PACKET/SEC
 AVERAGE THROUGHPUT FOR EACH ACTIVE NODE : 3004.0115 KBYTE/SEC
 AVERAGE PACKET QUEUEING DELAY OVER ALL NODES : 1179.64 US
 AVERAGE ACCESS DELAY OVER ALL NODES : 172.40 US
 AVERAGE NO OF PACKET IN NIC FIFO : 7.704750 PACKETS

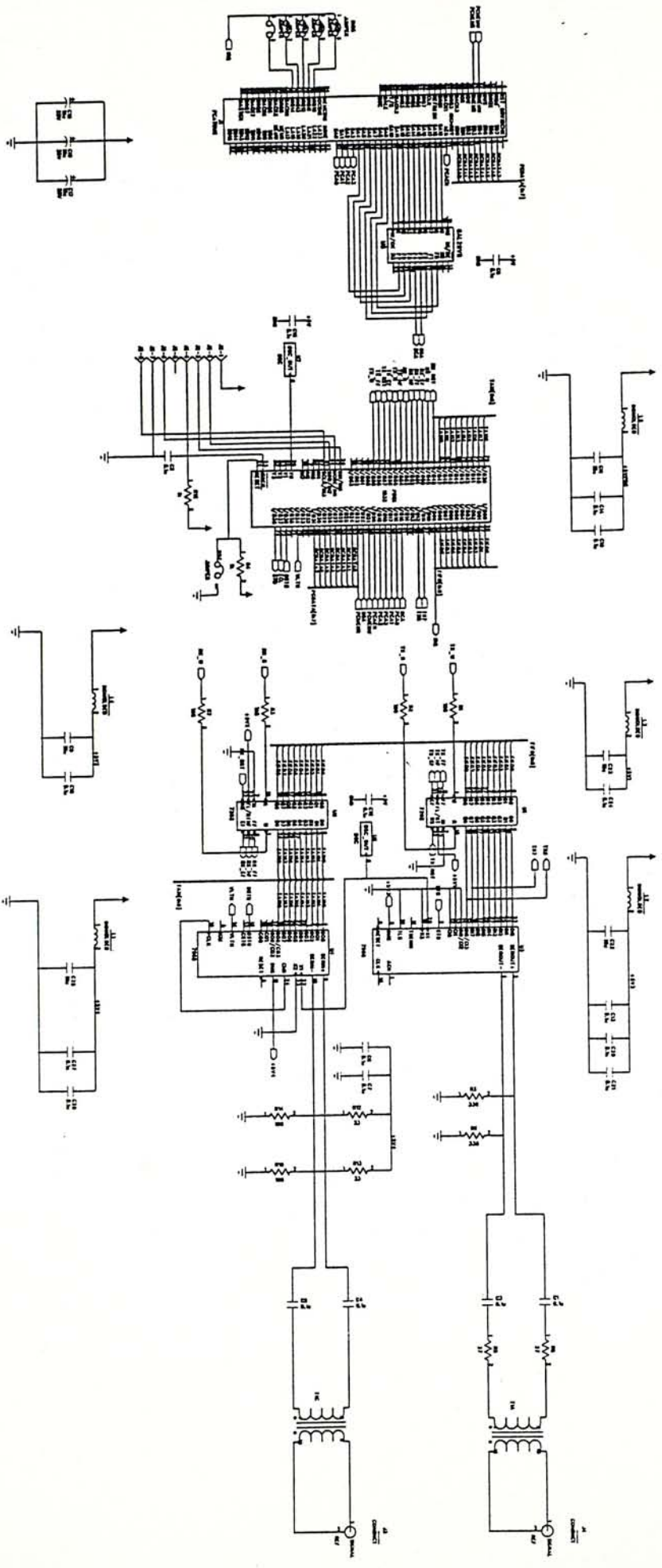
NUMBER OF NODES : 64
 NUMBER OF ACTIVE NODE : 4
 THE MAXIMUM THROUGHPUT OF THE NETWORK : 12500.00 KBYTE/SEC
 SIZE OF FIFO IN NIC : 8 KBYTES
 SIMULATION TIME : 1000000.00 us
 PACKET TRANSFER TIME OF THE NIC INTERFACE BUS : 0 US
 TOTAL OFFER LOAD RATIO FOR ALL NODES : 1.500
 DATA ARRIVAL RATE FOR EACH ACTIVE NODE : 4687.50 KBYTE/SEC
 PACKET ARRIVAL RATE FOR EACH ACTIVE NODE : 9049.23 PACKET/SEC
 NO OF POLL CYCLE EXECUTED BY THE HUB PER SEC : 5803.
 AVERAGE POLL RECEIVED BY ACTIVE NODE PER SEC : 5800.75
 AVERAGE POLL RECEIVED BY INACTIVE NODE PER SEC : 29.00
 TOTAL NUMBER OF PACKET TRANSMITTED : 23197 PACKET/SEC
 TOTAL THROUGHPUT OF THE NETWORK : 12016.05 KBYTE/SEC
 BANDWIDTH EFFICIENCY OF THE NETWORK : .9613
 AVERAGE NO OF PACKETS SENT BY EACH NODE : 5799.25 PACKET/SEC
 AVERAGE THROUGHPUT FOR EACH ACTIVE NODE : 3004.0115 KBYTE/SEC
 AVERAGE PACKET QUEUEING DELAY OVER ALL NODES : 1180.38 US
 AVERAGE ACCESS DELAY OVER ALL NODES : 172.40 US
 AVERAGE NO OF PACKET IN NIC FIFO : 7.709000 PACKETS

Appendix D

Circuit Diagram

- D.1 Network Interface Card
- D.2 Router/Hub - Ring A Module
- D.3 Router/Hub - Ring B Module
- D.4 Router/Hub - Hub Module
- D.5 Router/Hub - Power Module
- D.6 Concentrator - Back Plate
- D.7 Concentrator - Hub Connecting Module
- D.8 Concentrator - Node Connecting Module

118	100	100	100	100	100



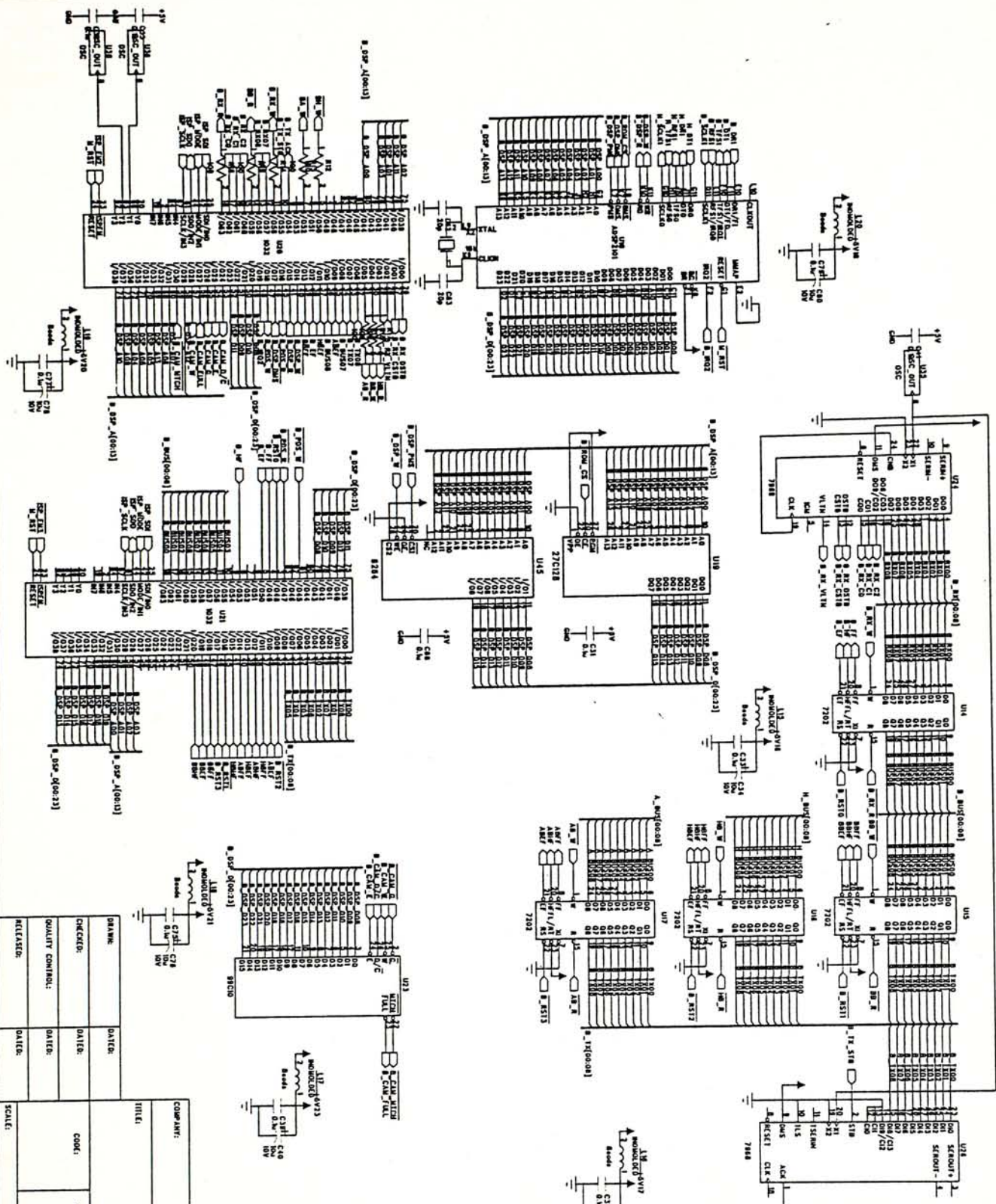
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NETWORK INTERFACE CARD

CUM AUDE NET PROJECT

DESCRIPTION	QUANTITY	UNIT	DATE
NETWORK INTERFACE CARD	1	PCB	
NETWORK INTERFACE CARD	1	PCB	
NETWORK INTERFACE CARD	1	PCB	
NETWORK INTERFACE CARD	1	PCB	
NETWORK INTERFACE CARD	1	PCB	

REVISION RECORD		
LTR	ECO NO.	APPROVED DATE:



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COMP. NO.:	COMP. NO.:	COMP. NO.:	COMP. NO.:

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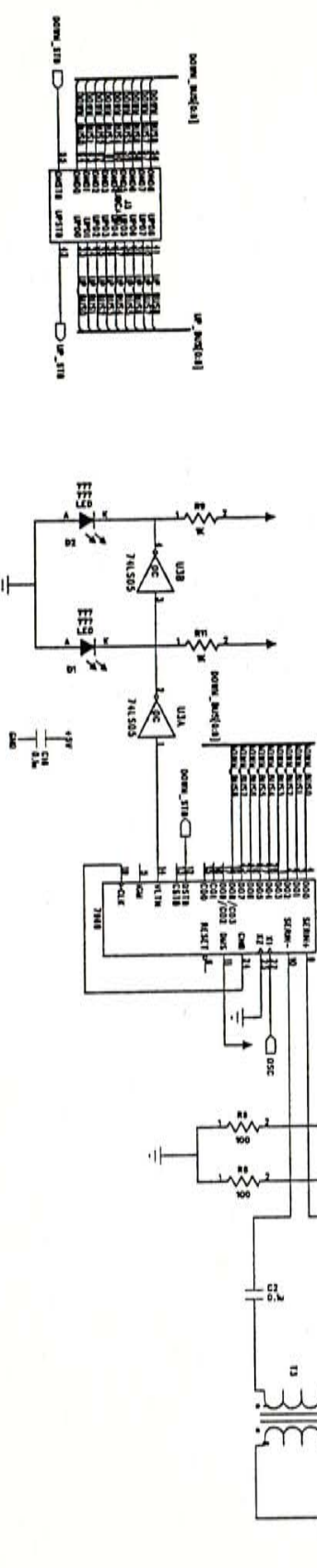
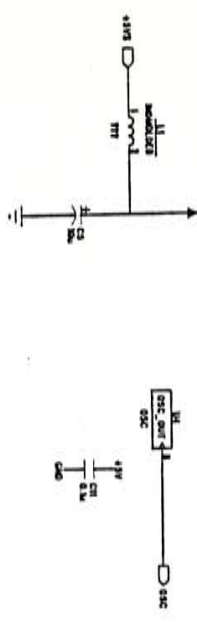
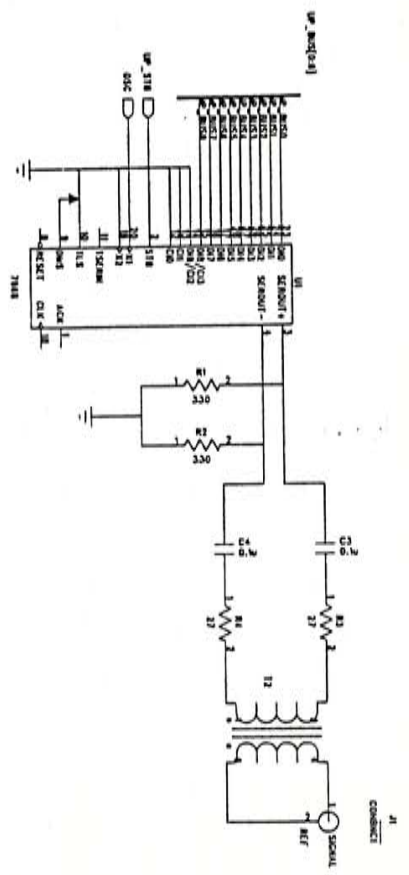
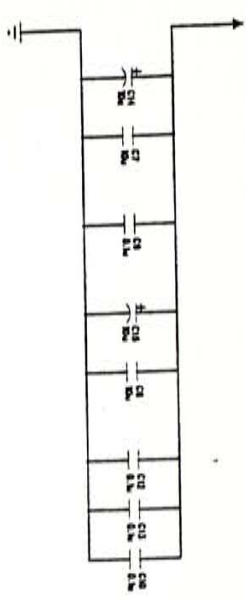
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REVISION RECORD			
LIB	EQ. NO.	APPROVED	DATE



A

B

C

D

COMPONENT: CUWLAUDE NET PROJECT			
TITLE: CONCENTRATOR : HUB-CONNECTING MODULE			
SCALE:	DATE:	SCALE:	DATE:
RELASER:	DATE:	SCALE:	DATE:
QUALITY CONTROL:	DATE:	SCALE:	DATE:
DESIGNER:	DATE:	SCALE:	DATE:
SAFELY:	DATE:	SCALE:	DATE:

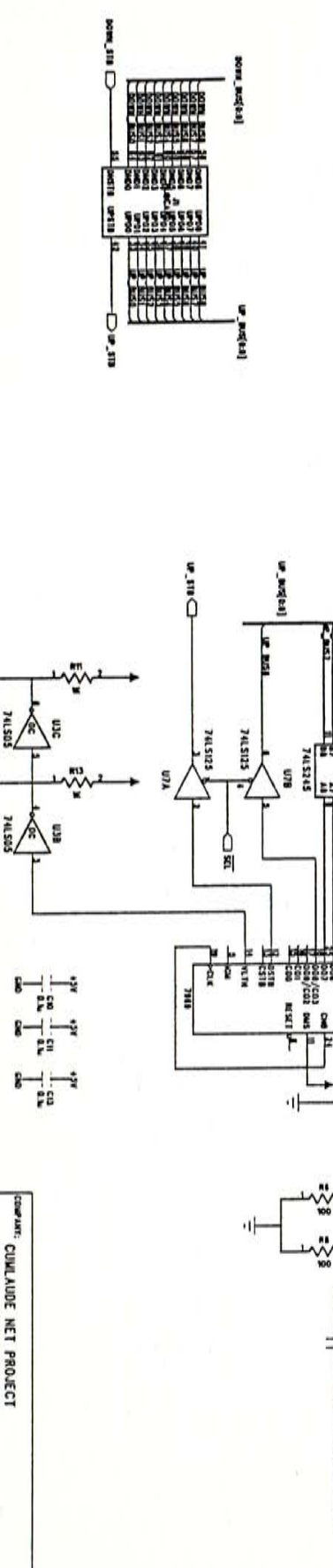
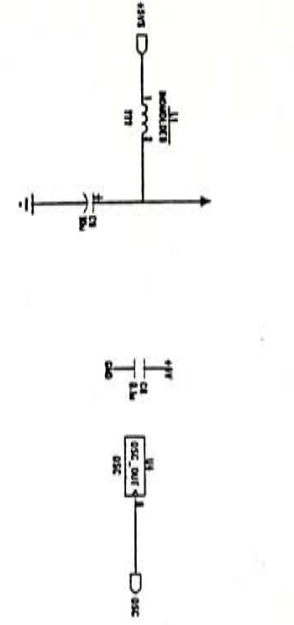
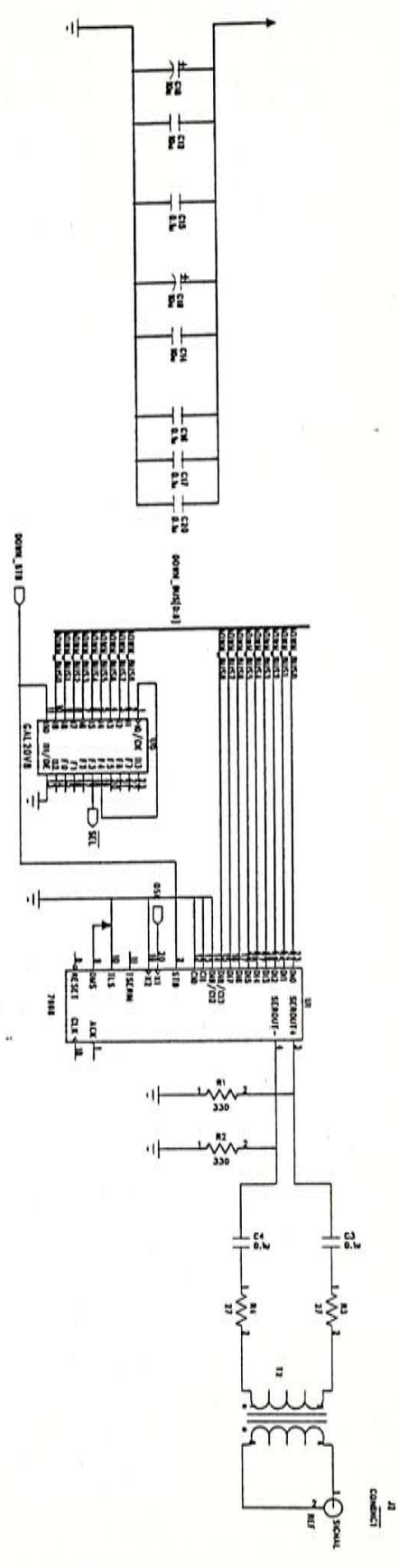
A

B

C

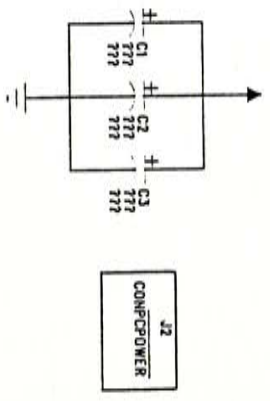
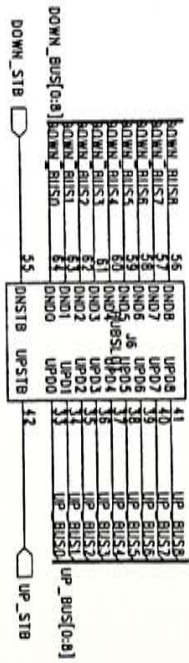
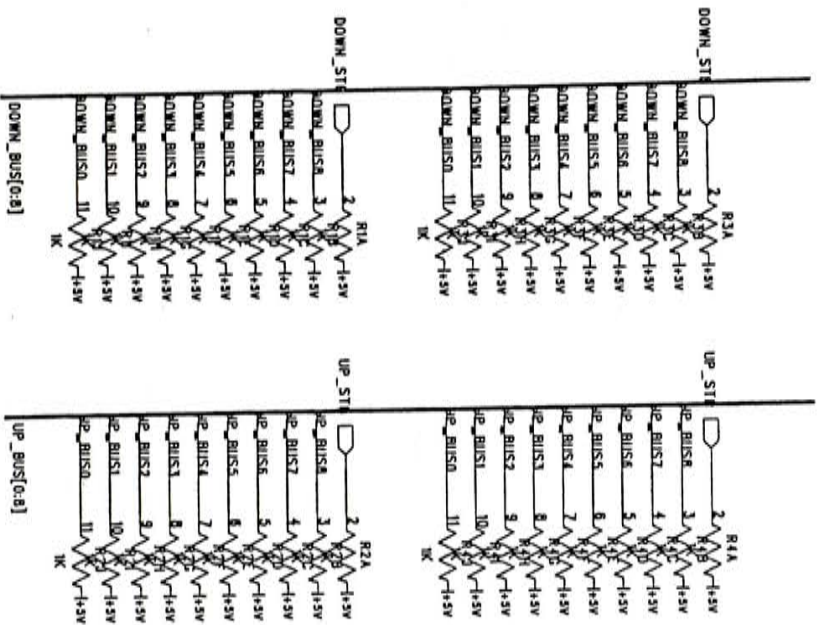
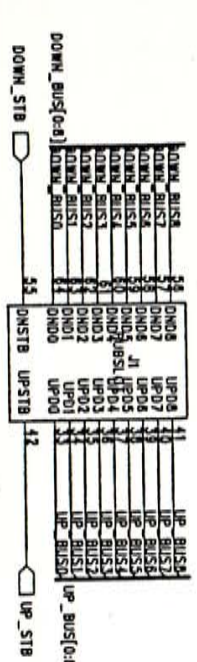
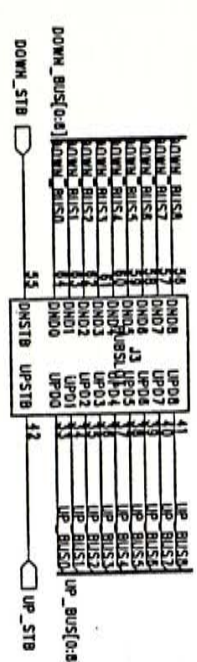
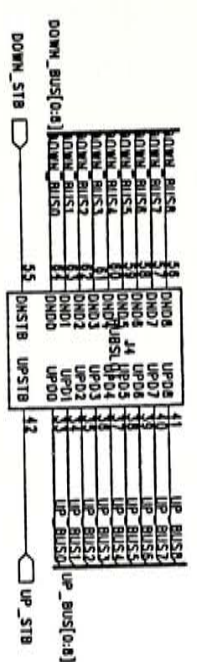
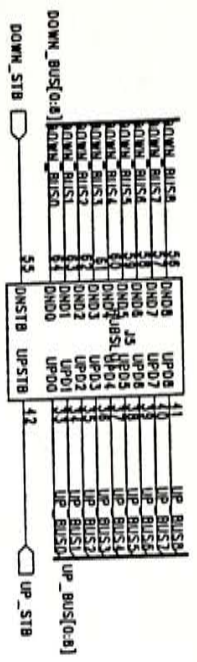
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REVISION RECORD			
REV	ECO NO.	APPROVER	DATE



COMPANY: CUMLAUDE NET PROJECT			
TITLE: CONCENTRATOR : NODE-CONNECTING MODULE			
DESIGNER:	DATE:	SCALE:	OF
CHECKER:	DATE:	COPIES:	
QUANTITY CONTRACT:	DATE:	DRAWING NO.:	REV.:
RELEASED:	DATE:	SCALE:	OF

REVISION RECORD			
LTR	ECO NO:	APPROVED:	DATE:



COMPANY: CUMLAUDE NET PROJECT

TITLE: **CONCENTRATOR :
BACK PLANE FOR 5 MODULES**

DRAWN:	DATED:	CODE:	SIZE:	DRAWING NO.:	REV:
CHECKED:	DATED:	QUALITY CONTROL:	DATED:	RELEASED:	DATED:
SCALE:	SHEET: OF				

Appendix E

PLD Source Code

E.1 GAL20V8 for NIC

E.2 Lattice ispLSI for NIC

E.3 GAL20V8 for Concentrator

pdspsc.pld

```
\begin{verbatim}
    PARTNO ;
    NAME PDSPC;
    DATE ;
    REV 01;
    DESIGNER Ringo Lam;
    COMPANY Lightwave Comm Lab, CUHK;
    ASSEMBLY PDSPC;
    LOCATION ;

/*****
/* ADDRESS DECODER FOR PCNIC */
/*****
/* TARGET DEVICES: 20V8 */
/*****
/* INPUTS */

PIN 1 = PCA10;
PIN 2 = PCA11;
PIN 3 = PCA12;
PIN 4 = PCA13;
PIN 5 = PCA14;
PIN 6 = PCA15;
PIN 7 = PCA16;
PIN 8 = PCA17;
PIN 9 = PCA18;
PIN 10 = PCA19;
PIN 15 = PCA09;
PIN 16 = PCA08;
PIN 17 = PCA07;
PIN 20 = PCA06;
PIN 21 = PCA05;
PIN 22 = PCA04;

/* OUTPUTS */

PIN 18 = BDA; /* d8XXX */
PIN 19 = BCA; /* D900X */

/* DEFINITIONS */

/* LOGIC EQUATIONS */

BDA = PCA19 & PCA18 & !PCA17 & PCA16 &
      PCA15 & !PCA14 & !PCA13 & !PCA12 ;

BCA = PCA19 & PCA18 & !PCA17 & PCA16 &
      PCA15 & !PCA14 & !PCA13 & PCA12 &
      !PCA11 & !PCA10 & !PCA09 & !PCA08 &
      !PCA07 & !PCA06 & !PCA05 & !PCA04 ;

\end{verbatim}
```


n64_0.1df

// Thu Jun 01 17:31:02 1995
 // N64_0.1df generated using Lattice pDS Version 2.20

LDF 1.00.00 DESIGNLDF;
 DESIGN NIC CARD CONTROLLER;

REVISION 1.0;

AUTHOR RINGO LAM;

PROJECTNAME CUM LAUDE NET;

DESCRIPTION

Decode the lowest byte of the IP address only.
 SW download the IP address into the hardware.;

PART pLSI1032-80LJ;

OPTION PULLUP ALL;

DECLARE

END; //DECLARE

SYM GLB D3 1 MUX;
 MUX2 (PCDOUT4, FDI4, REG4, MUXSEL);
 MUX2 (PCDOUT5, FDI5, REG5, MUXSEL);
 MUX2 (PCDOUT6, FDI6, REG6, MUXSEL);
 MUX2 (PCDOUT7, FDI7, REG7, MUXSEL);
 MUX2 (REG4, RX_EF, GND, REGSEL);
 MUX2 (REG5, RX_HF, GND, REGSEL);
 MUX2 (REG6, RX_FF, GND, REGSEL);
 MUX2 (REG7, GND, GND, REGSEL);
 END;

SYM GLB D4 1 MUX;
 MUX2 (PCDOUT0, FDI0, REG0, MUXSEL);
 MUX2 (PCDOUT1, FDI1, REG1, MUXSEL);
 MUX2 (PCDOUT2, FDI2, REG2, MUXSEL);
 MUX2 (PCDOUT3, FDI3, REG3, MUXSEL);
 MUX2 (REG0, TX_EF, IRQ0, REGSEL);
 MUX2 (REG1, TX_HF, IRQ1, REGSEL);
 MUX2 (REG2, TX_FF, GND, REGSEL);
 MUX2 (REG3, GND, GND, REGSEL);
 END;

SYM GLB D5 1 MUX;
 EQUATIONS
 MUXSEL = BCA;
 REGSEL = PCA0;
 FDOUT8 = !BCA;
 END;
 END;

SYM GLB A1 1 DEC;
 SIGTYPE RX_R OUT;

EQUATIONS

WR_DATA = BDA & !PCAEEN & !PCW;
 WR_HT = !PCA3 & PCA2 & !PCAL & !PCA0 & BCA & !PCAEEN & !PCW;
 RX_R = BDA & !PCAEEN & !PCR & !RX_EN;
 RX_EN.D = VCC;
 RX_EN.PTCLK = !(FDIN8 & !FDIN7 & RX_R);
 RX_EN.RE = GATE;

//LD14([IP40..IP43], [PCDINO..PCDIN3], IPSTB);
 //LD14([IP44..IP47], [PCDIN4..PCDIN7], IPSTB);
 END;
 END;

SYM GLB A0 1 DEC;
 LD11(PMASK,PCDINO,PMSTB);

EQUATIONS

PMSTB = !PCA3 & PCA2 & !PCAL & PCA0 & BCA & !PCAEEN & !PCW;
 IPSTB = !PCA3 & !PCA2 & PCAL & !PCA0 & BCA & !PCAEEN & !PCW;
 ERSTB = !PCA3 & PCA2 & PCAL & !PCA0 & BCA & !PCAEEN & !PCW;
 RD_REG = !PCA3 & !PCA2 & !PCAL & BCA & !PCAEEN & !PCR;
 END;
 END;

SYM GLB A2 1 IRQ;
 SIGTYPE IRQ0 OUT;

SIGTYPE IRQ1 OUT;

OR2(IRQ, IRQ0, IRQ1);

LSR1(IRQ0, !IRQ0_SET, !IRQ0_RST);

LSR1(IRQ1, !IRQ1_SET, !IRQ1_RST);

EQUATIONS

IRQ_ACK = !PCA3 & !PCA2 & !PCAL & PCA0 & BCA & !PCAEEN & !PCW;
 IRQ0_RST = PCDINO & IRQ_ACK;
 IRQ1_RST = PCDINI & IRQ_ACK;
 IRQ0_SET = RX_IRQ;
 IRQ1_SET = VLTN;
 END;
 END;

SYM GLB A3 1 RESET;
 SIGTYPE RST_STB OUT;

EQUATIONS

RST_STB = !PCA3 & !PCA2 & PCAL & PCA0 & BCA & !PCAEEN & !PCW;
 TXF_RST = PCDINO & RST_STB;
 TXSM_RST = PCDINI & RST_STB;
 END;
 END;

SYM GLB C2 1 TX;

EQUATIONS

STOP = !X8 & !X7 & TX_WR # TXSM_RST;
 TXEF.D = TX_EF & TAXI;
 TXEF.CLK = !SCLK;
 END;
 END;

SYM GLB C3 1 TX;

SIGTYPE TX_RD REG OUT;

EQUATIONS

TX_RD.D = TXEF & !TX_RD;
 TX_RD.CLK = SCLK;
 END;
 END;

SYM GLB C4 1 TX;

SIGTYPE TX_WR REG OUT;

EQUATIONS

TX_WR.D = TX_RD;
 TX_WR.CLK = !SCLK;

n64_0.1df

```
BC1.PTRE = RXSM_INIT;
IPE40 = IP40 !$ TAXID0;
IPE41 = IP41 !$ TAXID1;
END;
END;

SYM GLB C5 1 TX;
LSR1( TAXI, !START, !STOP);
EQUATIONS
START = PMASK & TX_EF & POLL;
END;
END;

SYM GLB C6 1 BUF;
EQUATIONS
//FDOUT4 = PCDIN4;
//FDOUT5 = PCDIN5;
FDOUT6 = PCDIN6;
FDOUT7 = PCDIN7;
END;
END;

SYM GLB C7 1 BUF;
EQUATIONS
//FDOUT0 = PCDIN0;
//FDOUT1 = PCDIN1;
FDOUT2 = PCDIN2;
FDOUT3 = PCDIN3;
END;
END;

SYM GLB D2 1 FOE;
SIGTYPE FOE OE;
EQUATIONS
FOE = WR_DATA # WR_HT;
TX_W = FOE;
END;
END;

SYM GLB D0 1 BUF;
EQUATIONS
FDOUT0 = PCDIN0;
FDOUT1 = PCDIN1;
//FDOUT2 = PCDIN2;
//FDOUT3 = PCDIN3;
END;
END;

SYM GLB D1 1 BUF;
EQUATIONS
FDOUT4 = PCDIN4;
FDOUT5 = PCDIN5;
//FDOUT6 = PCDIN6;
//FDOUT7 = PCDIN7;
END;
END;

SYM GLB B1 1 IP1;
SIGTYPE BCQ OUT;
AND8(BCQ, [TAXID7..TAXID0]);
EQUATIONS
BC1.D = BCQ;
BC1.PTCLK = SR1;

SYM GLB B2 1 IP2;
EQUATIONS
BC2.D = BCQ;
BC2.PTCLK = SR2;
BC2.PTRE = RXSM_INIT;
IPE42 = IP42 !$ TAXID2;
IPE43 = IP43 !$ TAXID3;
IPE44 = IP44 !$ TAXID4;
END;
END;

SYM GLB B3 1 IP3;
EQUATIONS
BC3.D = BCQ;
BC3.PTCLK = SR3;
BC3.PTRE = RXSM_INIT;
IPE45 = IP45 !$ TAXID5;
IPE46 = IP46 !$ TAXID6;
IPE47 = IP47 !$ TAXID7;
END;
END;

SYM GLB B4 1 IP4;
SIGTYPE IPE4 REG OUT;
AND8(P004, [IPE40..IPE47] );
EQUATIONS
IPE4.D = P004;
IPE4.PTCLK = SR4;
IPE4.PTRE = RXSM_INIT;
BC4.D = BCQ;
BC4.PTCLK = SR4;
BC4.PTRE = RXSM_INIT;
END;
END;

SYM GLB B7 1 MYPKT;
AND4(BC, [BC1..BC4]);
OR2(MYP, IPE4, BC);
EQUATIONS
MYPKT.D = MYP & RX_HF;
MYPKT.PTCLK = SR5;
MYPKT.PTRE = RXSM_INIT;
END;
END;

SYM GLB C1 1 RXSM;
EQUATIONS
RX_W = (TAXID8 # !TAXID6 ) & DSTB & MYPKT;
RX_TAIL = !TAXID8 & !TAXID7 & !TAXID6 & DSTB;
RX_HEAD = !TAXID8 & TAXID7 & !TAXID6 & DSTB;
RXSM_INIT = RX_HEAD # RX_TAIL # RXSM_RST;
RX_IRQ = !TAXID8 & !TAXID7 & !TAXID6 & DSTB & MYPKT;
END;
END;
```


n64_0.1df

```
DOE = RD_REG # RX_R;
END;
END;

SYM GLB A4 1 RESET;
EQUATIONS
RXP_RST = PCDIN2 & RST_STB;
RXSM_RST = PCDIN3 & RST_STB;
GATE = PCDIN4 & RST_STB;
END;
END;

SYM IOC IO11 1 PCD0;
XPIN IO PC_DATA_0 LOCK 37;
BI11(PCDINO, PC_DATA_0, PCDOU0, DOE);
END;

SYM IOC IO12 1 PCD1;
XPIN IO PC_DATA_1 LOCK 38;
BI11(PCDINI, PC_DATA_1, PCDOU1, DOE);
END;

SYM IOC IO13 1 PCD2;
XPIN IO PC_DATA_2 LOCK 39;
BI11(PCDIN2, PC_DATA_2, PCDOU2, DOE);
END;

SYM IOC IO14 1 PCD3;
XPIN IO PC_DATA_3 LOCK 40;
BI11(PCDIN3, PC_DATA_3, PCDOU3, DOE);
END;

SYM IOC IO15 1 PCD4;
XPIN IO PC_DATA_4 LOCK 41;
BI11(PCDIN4, PC_DATA_4, PCDOU4, DOE);
END;

SYM IOC IO16 1 PCD5;
XPIN IO PC_DATA_5 LOCK 45;
BI11(PCDIN5, PC_DATA_5, PCDOU5, DOE);
END;

SYM IOC IO17 1 PCD6;
XPIN IO PC_DATA_6 LOCK 46;
BI11(PCDIN6, PC_DATA_6, PCDOU6, DOE);
END;

SYM IOC IO18 1 PCD7;
XPIN IO PC_DATA_7 LOCK 47;
BI11(PCDIN7, PC_DATA_7, PCDOU7, DOE);
END;

SYM IOC IO41 1 FDO;
XPIN IO FIFO_DATA_0 LOCK 77;
BI11(FDINO, FIFO_DATA_0, FDOU0, FOE);
END;

SYM IOC IO43 1 FDI;
XPIN IO FIFO_DATA_1 LOCK 79;
BI11(FDINI, FIFO_DATA_1, FDOU1, FOE);
END;

SYM GLB B6 1 SR;
EQUATIONS
SR1.D = VCC;
SR2.D = SR1;
SR3.D = SR2;
SR4.D = SR3;
SR1.PTCLK = DSTB & TAXID8;
SR2.PTCLK = DSTB & TAXID8;
SR3.PTCLK = DSTB & TAXID8;
SR4.PTCLK = DSTB & TAXID8;
SR1.PTRE = RXSM_INIT;
SR2.PTRE = RXSM_INIT;
SR3.PTRE = RXSM_INIT;
SR4.PTRE = RXSM_INIT;
END;
END;

SYM GLB B5 1 POLL;
CONSTANT PADDR 'B00000000;
CMP8(PAE.GND.GND, [TAXID5..TAXID0], PADDR)
EQUATIONS
POLL = !TAXID8 & TAXID6 & DSTB & PAE;
SR5.D = SR4;
SR5.PTCLK = DSTB & TAXID8;
SR5.PTRE = RXSM_INIT;
END;
END;

SYM GLB A7 1 ;
LD14([IP44..IP47], [PCDIN4..PCDIN7], IPSTB);
//EQUATIONS
//IP44.D = PCDIN4;
//IP44.PTCLK = IPSTB;
//IP45.D = PCDIN5;
//IP45.PTCLK = IPSTB;
//IP46.D = PCDIN6;
//IP46.PTCLK = IPSTB;
//IP47.D = PCDIN7;
//IP47.PTCLK = IPSTB;
//END;
END;

SYM GLB A6 1 ;
LD14([IP40..IP43], [PCDINO..PCDIN3], IPSTB);
//EQUATIONS
//IP40.D = PCDINO;
//IP40.PTCLK = IPSTB;
//IP41.D = PCDIN1;
//IP41.PTCLK = IPSTB;
//IP42.D = PCDIN2;
//IP42.PTCLK = IPSTB;
//IP43.D = PCDIN3;
//IP43.PTCLK = IPSTB;
//END;
END;

SYM GLB A5 1 DOE;
SIGTYPE DOE OE;
EQUATIONS
```

n64_0.ldf

```
END;
SYM IOC IO49 1 FD3;
XPIN IO FIFO_DATA_3 LOCK 4;
IB11(FDIN3, FIFO_DATA_3, FDOOUT3, FOE);
END;
SYM IOC IO50 1 FD4;
XPIN IO FIFO_DATA_4 LOCK 5;
IB11(FDIN4, FIFO_DATA_4, FDOOUT4, FOE);
END;
SYM IOC IO48 1 FD5;
XPIN IO FIFO_DATA_5 LOCK 3;
IB11(FDIN5, FIFO_DATA_5, FDOOUT5, FOE);
END;
SYM IOC IO47 1 FD6;
XPIN IO FIFO_DATA_6 LOCK 83;
IB11(FDIN6, FIFO_DATA_6, FDOOUT6, FOE);
END;
SYM IOC IO46 1 FD7;
XPIN IO FIFO_DATA_7 LOCK 82;
IB11(FDIN7, FIFO_DATA_7, FDOOUT7, FOE);
END;
SYM IOC IO7 1 BDA;
XPIN IO BASE_DATA_ADDR LOCK 33;
IB11(BDA, BASE_DATA_ADDR);
END;
SYM IOC IO2 1 A0;
XPIN IO PC_ADDR0 LOCK 28;
IB11(PC_A0, PC_ADDR0);
END;
SYM IOC IO3 1 A1;
XPIN IO PC_ADDR1 LOCK 29;
IB11(PC_A1, PC_ADDR1);
END;
SYM IOC IO4 1 A2;
XPIN IO PC_ADDR2 LOCK 30;
IB11(PC_A2, PC_ADDR2);
END;
SYM IOC Y0 1 ;
XPIN CLK OSC LOCK 20 ;
IB11(SCLK, OSC);
END;
SYM IOC IO40 1 RXEF;
XPIN IO RX_FIFO_EF LOCK 76;
IB11(RX_EF, RX_FIFO_EF);
END;
SYM IOC IO42 1 RXHF;
XPIN IO RX_FIFO_HF LOCK 78;
IB11(RX_HF, RX_FIFO_HF);
```

```
END;
SYM IOC IO38 1 RXFF;
XPIN IO RX_FIFO_FF LOCK 74;
IB11(RX_FF, RX_FIFO_FF);
END;
SYM IOC IO31 1 RXW;
XPIN IO RX_FIFO_W LOCK 60;
OB21(RX_FIFO_W, RX_W);
END;
SYM IOC IO37 1 TXFF;
XPIN IO TX_FIFO_FF LOCK 73;
IB11(TX_FF, TX_FIFO_FF);
END;
SYM IOC IO35 1 TXHF;
XPIN IO TX_FIFO_HF LOCK 71;
IB11(TX_HF, TX_FIFO_HF);
END;
SYM IOC IO34 1 TXEF;
XPIN IO TX_FIFO_EF LOCK 70;
IB11(TX_EF, TX_FIFO_EF);
END;
SYM IOC IO36 1 RXRST;
XPIN IO RX_FIFO_RST LOCK 72;
OB21(RX_FIFO_RST, RXF_RST);
END;
SYM IOC IO39 1 TXRST;
XPIN IO TX_FIFO_RST LOCK 75;
OB21(TX_FIFO_RST, TXF_RST);
END;
SYM IOC IO51 1 RXR;
XPIN IO RX_FIFO_R LOCK 6;
OB21(RX_FIFO_R, RX_R);
END;
SYM IOC IO53 1 TXW;
XPIN IO TX_FIFO_W LOCK 8;
OB21(TX_FIFO_W, TX_W);
END;
SYM IOC IO1 1 IRQ;
XPIN IO PC_IRQ LOCK 27;
OB11(PC_IRQ, IRQ);
END;
SYM IOC IO52 1 STB;
XPIN IO TAXI_STB LOCK 7;
OB11(TAXI_STB, TX_WR);
END;
SYM IOC IO32 1 X8;
XPIN IO TAXI_OUT8 LOCK 68;
IB11(X8, TAXI_OUT8);
```


n64_0.1df

```
END;
SYM IOC IO20 1 T1;
XPIN IO TAXI_D1 LOCK 57;
IB11(TAXID1,TAXI_D1);
END;

SYM IOC IO28 1 DSTB;
XPIN IO TAXI_DSTB LOCK 55;
IB11(DSTB, TAXI_DSTB);
END;

SYM IOC IO26 1 T7;
XPIN IO TAXI_D7 LOCK 51;
IB11(TAXID7,TAXI_D7);
END;

SYM IOC IO22 1 T3;
XPIN IO TAXI_D3 LOCK 59;
IB11(TAXID3,TAXI_D3);
END;

SYM IOC IO21 1 T2;
XPIN IO TAXI_D2 LOCK 56;
IB11(TAXID2,TAXI_D2);
END;

SYM IOC IO27 1 T8;
XPIN IO TAXI_D8 LOCK 52;
IB11(TAXID8,TAXI_D8);
END;

SYM IOC IO25 1 T6;
XPIN IO TAXI_D6 LOCK 50;
IB11(TAXID6,TAXI_D6);
END;

SYM IOC IO30 1 TXR;
XPIN IO TX_FIFO_R LOCK 58;
OB21(TX_FIFO_R,TX_RD);
END;

SYM IOC IO29 1 VLTN;
XPIN IO VIOLATION LOCK 53;
IB11(VLTN,VIOLATION);
END;
END; //LDF DESIGNLDF

END;

SYM IOC IO33 1 X7;
XPIN IO TAXI_OUT7 LOCK 69;
IB11(X7, TAXI_OUT7);
END;

SYM IOC IO56 1 ;
XPIN IO AAA LOCK 11;
OB11(AAA , ERSTB);
END;

SYM IOC IO44 1 FD2;
XPIN IO FIFO_DATA_2 LOCK 81;
BI11(FDIN2, FIFO_DATA_2, FDOUT2, FOE);
END;

SYM IOC IO45 1 FD8;
XPIN IO FIFO_DATA_8 LOCK 80;
BI11(FDIN8, FIFO_DATA_8, FDOUT8, FOE);
END;

SYM IOC IO5 1 A3;
XPIN IO PC_ADDR3 LOCK 32;
IB11(PC_A3,PC_ADDR3);
END;

SYM IOC IO6 1 BCA;
XPIN IO BASE_CRTL_ADDR LOCK 31;
IB11(BCA, BASE_CRTL_ADDR);
END;

SYM IOC IO10 1 PCW;
XPIN IO PCMEMW LOCK 35;
IB11(PCW,PCMEMW);
END;

SYM IOC IO9 1 PCR;
XPIN IO PCMEMR LOCK 34;
IB11(PCR,PCMEMR);
END;

SYM IOC IO8 1 AEN;
XPIN IO PC_AEN LOCK 36;
IB11(PC_AEN,PC_AEN);
END;

SYM IOC IO19 1 T0;
XPIN IO TAXI_D0 LOCK 54;
IB11(TAXID0,TAXI_D0);
END;

SYM IOC IO23 1 T4;
XPIN IO TAXI_D4 LOCK 48;
IB11(TAXID4,TAXI_D4);
END;

SYM IOC IO24 1 T5;
XPIN IO TAXI_D5 LOCK 49;
IB11(TAXID5,TAXI_D5);
```

n0000.pld

```
PARTNO ;
NAME N0000;
DATE ;
REV 01;
DESIGNER Ringo Lam;
COMPANY Lightwave Comm Lab, CUHK;
ASSEMBLY N0000;
LOCATION ;
```

```
/*******/
/* ADDRESS DECODER FOR PCNIC */
/*******/
/* TARGET DEVICES: 20V8 */
/*******/
/* INPUTS */
```

```
PIN 1 = POLL;
PIN 2 = D8;
PIN 3 = D7;
PIN 4 = D6;
PIN 5 = D5;
PIN 6 = D4;
PIN 7 = D3;
PIN 8 = D2;
PIN 9 = D1;
PIN 10 = D0;
PIN 11 = DNSTB;
```

```
/* OUTPUTS */
```

```
PIN 18 = BUF;
PIN 19 = XPOLL; /* OUTPUT TO PIN 1 */
```

```
/* DEFINITIONS */
```

```
/* LOGIC EQUATIONS */
```

```
XPOLL = !D8 & D6 & DNSTB;
```

```
!BUF.D = !D5 & !D4 & !D3 & !D2 & !D1 & !D0;
```


Appendix F

DSP Program

hub.dsp

```

(CUM LAUDE NET ROUTER KERNEL FOR HUB)
MODULE/ram/boot=0/ABS=0 MAIN_ROUTINE; (PROGRAM LOADED)

.PORT STATUS;
.PORT FIFORST;
.PORT TAXITXWR;
.PORT DATARW;
.PORT TXSET;
.PORT TXRST;
.PORT TXPATH;
.PORT RXDMA;
.PORT RXPATH;
.PORT RXDMA;
.PORT IRQREG;
.PORT IRQMSK;
.PORT DMASTS;
.PORT POLL_SYNC;

.CONST MAXNODE=32;
.CONST A0=137,A1=189,A2=98,A3=46;

.CONST LA0=A0+0X100,LA1=A1+0X100,LA2=A2+0X100,LA3=A3+0X20*0X20+0x100;
.CONST CS=0XDF,SO=0X10,HADR=0X40+MAXNODE-1;
.CONST POLL_EN=0X7F,POLL_DIS=0XFF,IMSK=0X05;
.CONST N_TIMER=0X38F,P_TIMER=0X3F;

.VAR/DM/RAM/ABS=0X3900/SEG=INT_DM HEADER;
.VAR/DM/RAM/ABS=0X3901/SEG=INT_DM RXADR0;
.VAR/DM/RAM/ABS=0X3902/SEG=INT_DM RXADR1;
.VAR/DM/RAM/ABS=0X3903/SEG=INT_DM RXADR2;
.VAR/DM/RAM/ABS=0X3904/SEG=INT_DM RXADR3;
.VAR/DM/RAM/ABS=0X3906/SEG=INT_DM A_CNT;
.VAR/DM/RAM/ABS=0X3907/SEG=INT_DM B_CNT;
.VAR/DM/RAM/ABS=0X3908/SEG=INT_DM H_CNT;
[.VAR/DM/RAM/ABS=0X390A/SEG=INT_DM PADR;]
.VAR/DM/RAM/ABS=0X390B/SEG=INT_DM H_ERR;
.VAR/DM/RAM/ABS=0X390C/SEG=INT_DM TX_SEQ;
.VAR/DM/RAM/ABS=0X390D/SEG=INT_DM P_FLAG;
.VAR/DM/RAM/CIRC/ABS=0X3A00/SEG=INT_DM PADR [MAXNODE];

(CODE STARTS HERE)
(LOAD INTERRUPT VECTOR ADDRESS)

JUMP START; NOP; NOP; NOP; (RESET VECTOR)
JUMP RXPKT; NOP; NOP; NOP; (IRQ2 / INT)
RTI; NOP; NOP; NOP; (SPORT0 TRANSMIT INT)
RTI; NOP; NOP; NOP; (SPORT0 RECEIVE INT)
RTI; NOP; NOP; NOP; (IRQ0 / SPORT1 TRANSMIT INT)
RTI; NOP; NOP; NOP; (IRQ1 / SPORT1 RECEIVE INT)
JUMP TXPKT; NOP; NOP; NOP; (TIMER INTERRUPT)

(START)
START: AX0=1;
DM(0X3FFE)=AX0; (DM0 1 WAIT STATE)

AX0=DM(0X3FFF);
AY0=0XFFF8;
AR=AX0 AND AY0; (PM 0 WAIT STATE)
AX0=AR;

```

```

AY0=0X1C00; (ENABLE SPORT0)
AR=AX0 OR AY0;
DM(0X3FFF)=AR;

CALL SYNC_HLD;

AX0=N_TIMER; (TCOUNT REGISTER)
DM(0X3FFC)=AX0; (TPERIOD REGISTER)
DM(0X3FFD)=AX0;
AX0=0;
DM(0X3FFB)=AX0; (TSCALE REGISTER)

AX0=7; (RFSDIV0)
DM(0X3FF4)=AX0; (RFSDIV1)
DM(0X3FF0)=AX0;
AX0=0; (SCLKDIV0)
DM(0X3FF5)=AX0; (SCLKDIV1)
DM(0X3FF1)=AX0;
AX0=0X6A07; (SPORT0 CNTR)
DM(0X3FF6)=AX0;
AX0=0X2A07; (SPORT1 CNTR)
DM(0X3FF2)=AX0;

IFC=0X1E; (CLEAR INT)

AX0=0X0F;
DM(FIFORST) = AX0;
DM(TXSET)=AX0; (ENABLE TX)
AX0=0X0;
DM(FIFORST) = AX0; (RESET FIFO)
DM(A_CNT)=AX0;
DM(B_CNT)=AX0;
DM(H_CNT)=AX0;
DM(H_ERR)=AX0; (RESET COUNTER)

CNTR=MAXNODE;
AY0=0X40;
I1="PADR;
M1=1;
LI="PADR;
DO I_PADR UNTIL CE;
DM(I1,M1)=AY0;
AR=AY0+1;
I_PADR: AY0=AR;

AX0 = IMSK;
DM(IRQMSK)=AX0;

MSTAT=0X20;
IMASK=0X2B;
ICNTL=0;
M0=1;

WAIT: IDLE;
JUMP WAIT;

(=====)
RXPKT: AX0=DM(IRQREG);

```


hub.dsp

```

DM(IQREG)=AX0;
AY0=8;
AR=AX0 AND AY0;
IF EQ JUMP SYNC;

AY0=1;
AR=AX0 AND AY0;
IF NE JUMP RSTFIF01;

AY0=4;
AR=AX0 AND AY0;
IF EQ RTI;

RXRDY: AX0=N_TIMER;
DM(0X3FFC)=AX0;
AY1=1024;
AY0=2;
AR=AX0 AND AY0;
IF EQ JUMP RX;
AR=AY1-1;
AY1=AR;
IF NE JUMP RDDMAEND;
AX0=0X01;
AY0=0;
DM(FIFORST)=AX0;
DM(FIFORST)=AY0;
JUMP RXRDY;
AX0=N_TIMER;
DM(0X3FFC)=AX0;
AX0=DM(DATARW);
AY0=0X100;
AR=AX0 AND AY0;
IF NE JUMP HEAD_ERR;
AY0=0X80;
AR=AX0 AND AY0;
IF EQ JUMP HEAD_ERR;
AY0=0X40;
AR=AX0 AND AY0;
IF NE JUMP HEAD_ERR;
AY0=CS;
AR=AX0 AND AY0;
AX0=AR;
AY0=SO;
AR=AX0 OR AY0;
DM(HEADER)=AR;

GET_A0: AX0=DM(DATARW);
DM(RXADR0)=AX0;
CNTR=2;
AY0=LA0;
AR=AX0-AY0;
IF NE JUMP RXDMA_A;

RXDMA_A: AX0=1;
DM(RXPATH)=AX0;
IO=0X3900;
DO W_H_HDR UNTIL CE;
AX0=DM(IO,M0);
DM(DATARW)=AX0;
DM(RXDMA)=AX0;
RTI;

RXDMA_A: AX0=4;
DM(RXPATH)=AX0;
IO=0X3900;
DO W_A_HDR UNTIL CE;
AX0=DM(IO,M0);
DM(DATARW)=AX0;
DM(RXDMA)=AX0;
RTI;

HEAD_ERR: AX0=0XF0;
DM(RXPATH)=AX0;
DM(RXDMA)=AX0;
RTI;

SYNC: AX0=0X0F;
DM(FIFORST)=AX0;
CALL SYNC_HLD;
AX0=0;
DM(FIFORST)=AX0;
AX0=IMSK;
DM(IQMSK)=AX0;
AX0=N_TIMER;
DM(0X3FFC)=AX0;
RTI;

SYNC_HLD: DM(POLL_SYNC)=AX0;
CNTR=1024;
AX0=0X0F;
DO TIMING UNTIL CE;
TIMING: DM(FIFORST)=AX0;

[===== ALWAYS TO RING A FOR TESTING ONLY =====]

(JUMP RXDMA_A;)

RXDMA_H: AX0=1;
DM(RXPATH)=AX0;
IO=0X3900;
DO W_H_HDR UNTIL CE;
AX0=DM(IO,M0);
DM(DATARW)=AX0;
DM(RXDMA)=AX0;
RTI;

W_H_HDR: DM(DATARW)=AX0;
DM(RXDMA)=AX0;
RTI;

RXDMA_A: AX0=4;
DM(RXPATH)=AX0;
IO=0X3900;
DO W_A_HDR UNTIL CE;
AX0=DM(IO,M0);
DM(DATARW)=AX0;
DM(RXDMA)=AX0;
RTI;

HEAD_ERR: AX0=0XF0;
DM(RXPATH)=AX0;
DM(RXDMA)=AX0;
RTI;

SYNC: AX0=0X0F;
DM(FIFORST)=AX0;
CALL SYNC_HLD;
AX0=0;
DM(FIFORST)=AX0;
AX0=IMSK;
DM(IQMSK)=AX0;
AX0=N_TIMER;
DM(0X3FFC)=AX0;
RTI;

SYNC_HLD: DM(POLL_SYNC)=AX0;
CNTR=1024;
AX0=0X0F;
DO TIMING UNTIL CE;
TIMING: DM(FIFORST)=AX0;

```

hub.dsp

```

AX0=0X08;
AX0=DM(IRQREG);
AR=AX0 AND AY0;
IF EQ JUMP SYNC_HLD;
RTS;

RSTFIF01:AX0=1;
AY0=0;
DM(FIFORST)=AX0;
DM(FIFORST)=AY0;
RTI;

TXPKT: DM(TXRST)=AX0;
AX0=DM(I1,M1);
DM(TAXITXWR)=AX0; (TX POLL CMD)
AX0=P_TIMER;
DM(TXSET)=AX0;
DM(0X3FFC)=AX0;
M5=1;
W_TXCMP: AX0=DM(DMASTS);
I5=0X800;
PM(15,M5)=AX0;
AY0=0X08;
AR=AX0 AND AY0;
IF NE RTI;

AX0=DM(STATUS); (H_EF)
AY0=0X08;
AR = AX0 AND AY0;
IF NE JUMP TX_H; (A_EF)
AY0=0X40;
AR = AX0 AND AY0;
IF NE JUMP TX_A;
AY0=0X200; (B_EF)
AR = AX0 AND AY0;
IF NE JUMP TX_B;
RTI;

TX_A: AX0=2;
DM(TXPATH)=AX0;
DM(TXDMA)=AX0;
RTI;

TX_B: AX0=4;
DM(TXPATH)=AX0;
DM(TXDMA)=AX0;
RTI;

TX_H: AX0=1;
DM(TXPATH)=AX0;
DM(TXDMA)=AX0;
RTI;

(RXPKT_A: AX0=RX0;
AY0=POLL_EN;
AR=AX0-AY0;
IF EQ JUMP WR_POLL;
IF LT JUMP INC_ACNT;
AY0=POLL_DIS;
WR_POLL: DM(P_FLAG)=AY0;

```

```

RTI;
INC_ACNT:AY0=DM(A_CNT);
AR=AY0+1;
DM(A_CNT)=AR;
RTI;

RXPKT_B: AX0=RX1;
AY0=DM(B_CNT);
AR=AY0+1;
DM(B_CNT)=AR;
RTI;)

ENDMOD;

```


Appendix G

Device Driver

G.1 The Network Driver : `nic.c`

G.2 The Header File : `nic.h`

nic.c

```
/* inic.c: kernel driver for NIC (interrupt version). */

#include <linux/config.h>
#include <linux/kernel.h>
#include <linux/sched.h>
#include <linux/types.h>
#include <linux/fcntl.h>
#include <linux/interrupt.h>
#include <linux/ptrace.h>
#include <linux/ioport.h>
#include <linux/in.h>
#include <linux/malloc.h>
#include <linux/string.h>
#include <asm/system.h>
#include <asm/bitops.h>
#include <asm/io.h>
#include <asm/dma.h>
#include <errno.h>

#include <linux/netdevice.h>
#include <linux/etherdevice.h>
#include <linux/skbuff.h>
#include <linux/timer.h>
#include <../net/inet/arp.h>

#include "nic.h"

#define USE_POLL
#undef USE_POLL

struct nic_private {
    struct enet_statistics stats;
};

#ifdef HAVE_AUTOIRQ
/* From auto_irq.c, in ioport.h for later versions. */
extern void autoirq_setup(int waittime);
extern int autoirq_report(int waittime);
/* The map from IRQ number (as passed to the interrupt handler) to 'struct
 * device'.
 */
extern struct device *irq2dev_map[16];
#endif /* HAVE_AUTOIRQ */

#ifdef RT_DEBUG
#define RX_DEBUG
#undef RX_DEBUG
#endif

#ifdef TX_DEBUG
#define TX_DEBUG
#undef TX_DEBUG
#endif

/* Use volatile to avoid over optimizations */
#define nic_reset ((volatile unsigned char *)NIC_RESET)
#define nic_status ((volatile unsigned char *)NIC_STATUS)
```

```
#define nic_data_addr ((volatile unsigned char *)NIC_DATA_ADDR)
#define nic_header_addr ((volatile unsigned char *)NIC_HEADER_ADDR)
#define nic_trail_addr ((volatile unsigned char *)NIC_TRAIL_ADDR)
#define nic_pmask ((volatile unsigned char *)NIC_PMASK)
#define nic_ip_addr ((volatile unsigned char *)NIC_IP_ADDR)
#define nic_irq ((volatile unsigned char *)NIC_IRQ)
#define nic_err ((volatile unsigned char *)NIC_ERR_PORT)

struct device *nic_dev;
unsigned int error_count=0;

/* Index to functions, as function prototypes. */
/* Function prototypes */
int nic_init(struct device *dev);
static int nic_close(struct device *dev);
static struct enet_statistics *nic_get_stats(struct device *dev);
static int nic_hard_header(unsigned char *buff, struct device *dev, unsigned short
+ type, void *daddr, void *saddr, unsigned len, struct sk_buff *skb);
static void nic_intr_handler(int intr_ptr);
static void nic_poll(void);
static int nic_open(struct device *dev);
static int nic_rebuild_header(void *buff, struct device *dev, unsigned long dst, st
+ ruct sk_buff *skb);
static int nic_start_xmit(struct sk_buff *skb, struct device *dev);
static unsigned short nic_type_trans(struct sk_buff *skb, struct device *dev);

/* Internal functions */
static int nic_write(unsigned char *buff, int count);
static int net_rx(struct device *dev);
static int print_pkt(unsigned char *buff);
static void print_header(struct nic_header *nh);

/***** Init/Open/Close *****/
int
nic_init(struct device *dev)
{
    int i;

    dev->hard_start_xmit = nic_start_xmit;
    dev->open = nic_open;
    dev->hard_header = nic_hard_header;
    dev->type_trans = nic_type_trans;
    dev->stop = nic_close;
    dev->get_stats = nic_get_stats;
    dev->rebuild_header = nic_rebuild_header;
    /* dev->queue_xmit = dev_queue_xmit; */

    dev->mtu = NIC_PACKET_SIZE;
    dev->addr_len = NIC_ADDR_LEN;
    dev->type = NIC_TYPE;
    dev->hard_header_len = sizeof(struct nic_header);
    dev->flags = IFF_BROADCAST;
    dev->family = AF_INET;
    dev->priv = kmalloc(sizeof(struct nic_private), GFP_KERNEL);
    memset(dev->priv, 0, sizeof(struct nic_private));
    for (i = 0; i < NIC_ADDR_LEN; i++)
        dev->broadcast[i] = 0xff;

    dev->pa_addr = 0;
    dev->pa_brdaddr = 0;
}
```


nic.c

```

dev->pa_mask = 0;
dev->pa_alen = sizeof(unsigned long);

for (i = 0; i < DEV_NUMBUFFS; i++)
    skb_queue_head_init(&dev->buffs[i]);

dev->tbusy = 0;
dev->interrupt = 0;
nic_dev = dev;

dev->irq = NIC_IRQ_NO;

/* ether_setup(dev) ??? */
printk("Cum Laude NIC driver installed at irq 10 (hard-wired), resetting ... ");

printk("done.\n");
return 0;
}

int
nic_open(struct device *dev)
{
    int    loop;

    if (request_irq(dev->irq, &nic_intr_handler)) {
        printk("NIC: open can't request irq %d\n", dev->irq);
        return -EAGAIN;
    }
    irq2dev_map[dev->irq] = dev;

    printk("%s: request to open device.\n", dev->name);

    for (loop = 0; loop < NIC_ADDR_LEN; loop++)
        dev->dev_addr[loop] = NIC_HD_ADDR;

    memcpy(dev->dev_addr, &(dev->pa_addr), 4); /* HW add is 4 now */
    *nic_ip_addr = (unsigned char) *((unsigned char *)&dev->pa_addr+3);

    dev->tbusy = 0;
    dev->interrupt = 0;
    dev->start = 1;

    *nic_reset = 0xff;
    *nic_irq = 0xff;
    *nic_pmask = NIC_PMASK_OFF;
    error_count=0;

#ifdef USE_POLL
    timer_table[NIC_TIMER].fn = nic_poll;
    timer_table[NIC_TIMER].expires = jiffies + NIC_POLL;
    timer_active |= 1 << NIC_TIMER;
#endif
    return 0;
}

int
nic_close(struct device *dev)
{
#ifdef USE_POLL
    timer_active &= ~(1 << NIC_TIMER);
#endif
}

#endif
dev->tbusy = 1;
dev->start = 0;
free_irq(dev->irq);
irq2dev_map[dev->irq] = 0;
/* How about dev->priv? No one seems to free it! */

return 0;
}

/***** Poll/Interrupt *****/
/*
 * The typical workload of the driver: Handle the network interface
 * interrupts.
 */
static void
nic_intr_handler(int reg_ptr)
{
    int    irq = -(((struct pt_regs *) reg_ptr)->orig_eax + 2);
    struct device *dev = (struct device *) (irq2dev_map[irq]);
    unsigned char  irq_register;

    if (dev == NULL) {
        printk("net_interrupt(): irq %d for unknown device.\n", irq);
        return;
    }
    if (dev->interrupt)
        printk("%s Re-entering the interrupt handler.\n", dev->name);
    dev->interrupt = 1;

    if ((irq_register = *nic_irq) & NIC_IRQ_VLTFN)
    {
        *nic_irq = irq_register;
        printk("nic_intr_handler: IRQ VIOLATION!!!\n");
        printk("Please type reset.nic to reset the network card!\n");
    }
    else
    {
        error_count = 0;
        *nic_irq = irq_register;
        while (*nic_status & NIC_DOWN_EMPTY_MASK && (error_count < 5))
            /* Got a packet(s). */
            net_rx(dev);

        dev->interrupt = 0;
        return;
    }
    static void
    nic_poll(void)
{
#ifdef USE_POLL
    struct device *dev = nic_dev;

    if (dev->tbusy && (~(*nic_status) & NIC_UP_MASK_USING)) {
        dev->tbusy = 0;
        if (ELP_KERNEL_TYPE < 3)
#endif
}

```


nic.c

```

nic_get_stats(struct device *dev)
{
    return &(((struct nic_private *) dev->priv)->stats);
}

/***** Debugging Functions *****/
static void
print_pkt(unsigned char *buff)
{
    int i;

    for (i = 0; i < NIC_PACKET_SIZE; i++)
        printk("%4X ", *buff++);
}

static void
print_header(struct nic_header *nh)
{
    int loop;

    printk("nh->type : %X, nh.length : %X\n", nh->type, nh->length);
    printk("nh->daddr :");
    for (loop = 0; loop < NIC_ADDR_LEN; loop++)
        printk(" %X", nh->daddr[loop]);
    printk("\n");

    printk("nh->saddr :");
    for (loop = 0; loop < NIC_ADDR_LEN; loop++)
        printk(" %X", nh->saddr[loop]);
    printk("\n");
}

/*
 * Local variables: compile-command: "gcc -D_KERNEL_
 * -I/usr/src/linux/net/inet -Wall -Wstrict-prototypes -O6 -m486 -c nic.c"
 * version-control: t kept-new-versions: 5 tab-width: 4 End:
 */
)

int
nic_rebuild_header(void *buff, struct device *dev, unsigned long dst,
                  struct sk_buff *skb)
{
    struct nic_header *nh = (struct nic_header *) buff;

    if (nh->type != htons(ETH_P_IP)) {
        printk("eth_rebuild_header: Don't know how to resolve type %d address\n", (int)
+ nh->type);
        memcpy(nh->saddr, dev->dev_addr, dev->addr_len);
        return 0;
    }
    memcpy(nh->daddr, dst, dev, dev->pa_addr, skb) ? 1 : 0; */
}

unsigned short
nic_type_trans(struct sk_buff *skb, struct device *dev)
{
    struct nic_header *nh = (struct nic_header *) skb->data;

    if (ntohs(nh->type) < 1536)
        return htons(ETH_P_802_3);

    return nh->type;
}

static struct enet_statistics *

```


nic.h

```
unsigned short length; /*exclude the header and trailer */
};
/*
int nic_open(struct device *dev);
int nic_hard_header(unsigned char *buff, struct device *dev, unsigned short type,
void *daddr, void *saddr, unsigned len, struct sk_buff *skb);
int nic_rebuild_header(void *buff, struct device *dev, unsigned long dst,
struct sk_buff *skb);
unsigned short nic_type_trans(struct sk_buff *skb, struct device *dev);

int nic_start_xmit(struct sk_buff *skb, struct device *dev);
int nic_write(unsigned short *buff, int count);
int nic_read(unsigned short *buff, int count);
int nic_init(struct device *dev);
*/
#endif

512 /*including HEADER and data */
/* bytes */
4
0x04
0x02
0x01
0x40
0x20
0x10
0x000d9004
0x000d9004
0x000d8000
0x000d9003
0x000d9000
0x000d9001
0x000d9002
0x000d9005
0x000d9006
0x80
0x0f /* org:0x00 */
0x01
0x04
0x02
0x08
0x10
0x01
0x02
0x00
0x01
NIC_UP_EMPTY_MASK
NIC_DOWN_EMPTY_MASK
1 /* ETHERNET */ /* original 3 */
1
#define NIC_TIMERON 1
#define NIC_TIMEROFF 2
#define NIC_TIMER 10
#define NIC_IRQ_NO 10
#define NIC_WAIT_STATE 3000
#define NIC_CS 1
#define NIC_CE 2
#define NIC_SO 4
#define NIC_SR1 8
#define NIC_SR2 16
#define NIC_NT 32
#define NIC_BC 64
struct nic_header {
unsigned char daddr[NIC_ADDR_LEN];
unsigned char saddr[NIC_ADDR_LEN];
unsigned short type;
```

Appendix H

Testing Program

H.1 Packet Error Rate Testing Program

H.2 UDP Rate Testing Program

H.2.1 Datagram Client : dgcli.c

H.2.2 Datagram Server : dgecho.c

H.2.3 UDP Client : udpcli.c

H.2.4 UDP Server : udpserv.c

H.2.5 The Header File : inet.h

single.c

```

)
if (error_flag==1)
{
    printf("Wrong Header/Trailer\n");
    fprintf(error, "Wrong Header/Trailer at Loop %ld\n", loop)
}
if (error_flag==2)
{
    printf("Wrong Data\n");
    fprintf(error, "Wrong data error at byte %d , loop %ld\n",
loop , count, loop);
}
fprintf(error, "packet error at loop %ld\n", loop);
for(x=0;x<(LENGTH/16);x++)
{
    for(y=0;y<16;y++)
    {
        if ((x*16+y)==count) fprintf(error, "%2.2x^ ", te
        else fprintf(error, "%2.2x ", temp[x*16+y]);
    }
    fprintf(error, "\n");
    for(y=0;y<16;y++)
    {
        if ((x*16+y)==count) fprintf(error, "%2.2x^ ", re
        else fprintf(error, "%2.2x ", receive[x*16+y]);
    }
    fprintf(error, "\n");
}
error_count++;
error_loop[j++]=loop;
if(error_count==error_stop) goto getout;
}
loop++;
if(loop%lp==0)
{
    printf("%ld packet tested, ", loop);
    printf("%ld packet error, ", error_count);
    printf("PER=%f\n", (float)((float)error_count/(float)loop));
}
}while(!kbhit());

getout:
a = importb(IMR);
exportb(IMR, a|0x04);

/*clrscr();*/
printf("CUMLAUDE NIC Loop Test finished!\n\n");
printf("No. of packets tested : %ld\n", loop);
printf("No. of errors found : %ld\n", error_count);
printf("Packet Error Rate (PER): %f\n", (float)((float)error_count/(float)loop));
printf("No. of violation = %d\n", vltm);
printf("\nError occurred at loop : %d\n",
for(i=0;i<error_count;i++) printf("%ld\t", error_loop[i]);
printf("\nViolation occurred at loop : %d\n",
for(i=0;i<vltm;i++) printf("%ld\t", vltm_loop[i]);

```


dgecho.c

```

/*
 * Read a datagram from a connectionless socket
 * Prompt for every 1000 datagram received
 */
#include <sys/file.h>
#include <sys/types.h>
#include <sys/socket.h>
#define SIZE 256
dg_echo(sockfd, pcli_addr, maxclilen)
int sockfd; /* ptr to appropriate sockaddr_XX structure */
struct sockaddr *pcli_addr; /* sizeof(*pcli_addr) */
int maxclilen;
{
    int n, clilen;
    int snd_fd;
    unsigned char recvbuffer[1024];
    unsigned long count=0;
    for ( ; ) {
        clilen = maxclilen;
        n = recvfrom(sockfd, recvbuffer, SIZE, 0, pcli_addr, &clilen);
        if (n < 0)
            printf("UDP dg_echo: recvfrom error!\n");
        else
            {
                count++;
                if ((count%1000) == 0)
                    printf("UDP server: Received packets: %ld\n", count);
            }
    }
}

```

dgcli.c

```

/*
 * Continuously send fixed size datagram to datagram socket
 * Prompt the user for every 5000 datagram with transfer rate
 */
#include <stdio.h>
#include <linux/time.h>
#include <sys/file.h>
#include <sys/types.h>
#include <sys/socket.h>
#include <unistd.h>
#define SIZE 256
dg_cli(sockfd, pserver_addr, servlen)
int sockfd; /* ptr to appropriate sockaddr_XX structure */
struct sockaddr *pserver_addr; /* actual sizeof(*pserver_addr) */
int servlen;
{
    int n, i;
    unsigned long j = 0;
    int snd_fd, count;
    unsigned char buffer[1024], recvbuffer[1024];
    double rate;
    float time_diff;
    struct timeval time_start, time_end;
    for (i=0; i<SIZE; i++)
        buffer[i] = i;
    gettimeofday(&time_start, (struct timezone *)0);
    while (1) {
        /* for (i=0; i<5000; i++); */
        if (sendto(sockfd, buffer, SIZE, 0, pserver_addr, servlen) != SIZE)
            printf("UDP dg_cli: sendto error on socket!\n");
        else
            {
                j++;
                if ((j%5000) == 0)
                    {
                        printf("UDP client: Sent packets: %ld\n", j);
                        gettimeofday(&time_end, (struct timezone *)0);
                        time_diff = (time_end.tv_sec*1000000+time_end.tv_usec)-
                            (time_start.tv_sec*1000000+time_start.tv_usec);
                        rate = (double)((float)(5000*512)/(time_diff/1000));
                        printf("time_diff: %f us\n", time_diff);
                        printf("UDP client: Transfer rate=%f bytes/ms\n", rate);
                        gettimeofday(&time_start, (struct timezone *)0);
                    }
            }
    }
}

```

udpserver.c

```
/*
 * Example of server using UDP protocol.
 */
#include "inet.h"
#include "usr/src/linux/include/linux/in.h"

main(argc, argv)
int argc;
char *argv[];
{
    int sockfd;
    struct sockaddr_in serv_addr, cli_addr;
    pname = argv[0];

    if ((sockfd = socket(AF_INET, SOCK_DGRAM, IPPROTO_UDP)) < 0)
        printf("UDP server: can't open datagram socket!\n");

    memset((char *)&serv_addr, 0, sizeof(serv_addr));
    serv_addr.sin_family = AF_INET;
    serv_addr.sin_addr.s_addr = htonl(INADDR_ANY);
    serv_addr.sin_port = htons(SERV_UDP_PORT);

    if (bind(sockfd, (struct sockaddr *)&serv_addr, sizeof(serv_addr)) < 0)
        printf("UDP server: can't bind local address!\n");

    printf("UDP test program: Server is running!\n");
    dg_echo(sockfd, (struct sockaddr *)&cli_addr, sizeof(cli_addr));
}
)
```

inet.h

```
/*
 * Definitions for WTP client/server program
 */
#include <stdio.h>
#include <sys/types.h>
#include <sys/socket.h>
#include <netinet/in.h>
#include <arpa/inet.h>

#define SERV_UDP_PORT 6544
#define SERV_HOST_ADDR "137.189.97.45" /* host addr for server */

char *pname;
```

udpcli.c

```
/*
 * Example of client using UDP protocol.
 */
#include "inet.h"

main(argc, argv)
int argc;
char *argv[];
{
    int sockfd;
    struct sockaddr_in cli_addr, serv_addr;
    pname = argv[0];

    /*
     * Fill in the structure "serv_addr" with the address of the
     * server that we want to send to.
     */
    bzero((char *)&serv_addr, sizeof(serv_addr));
    serv_addr.sin_family = AF_INET;
    serv_addr.sin_addr.s_addr = inet_addr(SERV_HOST_ADDR);
    serv_addr.sin_port = htons(SERV_UDP_PORT);

    /*
     * Open a UDP socket (an Internet datagram socket).
     */
    if ((sockfd = socket(AF_INET, SOCK_DGRAM, IPPROTO_UDP)) < 0)
        printf("UDP client: can't open datagram socket!\n");

    /*
     * Bind any local address for us.
     */
    memset((char *)&cli_addr, 0, sizeof(cli_addr)); /* zero out */
    cli_addr.sin_family = AF_INET;
    cli_addr.sin_addr.s_addr = htonl(INADDR_ANY);
    cli_addr.sin_port = htons(0);
    if (bind(sockfd, (struct sockaddr *)&cli_addr, sizeof(cli_addr)) < 0)
        printf("UDP client: can't bind local address!\n");

    dg_cli(sockfd, (struct sockaddr *)&serv_addr, sizeof(serv_addr));

    close(sockfd);
    exit(0);
}
)
```


CUHK Libraries



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