Storage Of Decimal Numbers By Square Loop Magnetic Core And Its Application In Pulse Counting

十位數字貯存在矩形性磁環中的方法及其在脈沖計算上的應用

by

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Abstract

The method of using a square-loop magnetic core as storage element of high information density is investigated with emphasis on the memory of decimal numbers. A non-destructive readout for sensing the storage is presented. Also, how to apply the decimal magnetic storage device in pulse counting and simple arithmatic operations are discussed.

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List of symbols

A	number (stored in the counter)
	register
ADD	addition control signal
a	constant
α	proportional constant
B	magnetic induction
	register
B_r	remanence induction
B_s	saturation induction
b	constant
β	normalized factor for $f(\Phi)$
C	capacitance
	magnetic counter input terminal
	register
C_r	clear
c	proportional constant
D	diode
d_i	inner diameter of magnetic core
d_o	outer diameter of magnetic core
Δt	pulse duration
$\Delta\Phi_{eff}$	effictive flux switching for each input
$\Delta\Phi_{fly}$	magnetic flyback flux for each input
$\Delta\Phi_{tot}$	total flux switching for each input
δ	flux difference between a stored number and its complement in the magnetic counter
E	amount of equipment

$\mathcal{E}$	battery e.m.f.
e	natural number
F	forward counting signal
ff	flip-flop
$f(\Phi)$	function of flux
G_j	controllable AND gate
G_i	controllable AND gate input terminal
G_o	controllable AND gate output terminal
GC	Permalloy G core counter
H	magnetic field strength
H_c	coercive force
H_i	applied force
H_o	threshold force
h	height of magnetic core
I_B	transistor base current
I_C	transistor collector current
I_j	LED indicator inputs
i_j	switching current
j	numerical index
k	switching coefficient
k'	slope of straight line
ℓ	mean length of magnetic core
M.P.	marker pulse
M.R.P.	multiplicative read pulses
M.R.P.G.	multiplicative read pulse generator
m	number (digits of decimal number)
N	number
	turns of winding

n	number
	half storage capacity of the magnetic counter
o/p	magnetic counter output terminal
Ξ	vector sum
Q_j	transistor
Q , $\overline{Q}$	positive and complementary output of the flip-flop
R	resistance
	reset input of flip-flop
	reverse counting signal
	Reading
$\overline{R}$	Count inhibit (complement of Reading)
R.P.	read pulses
R.P.G.	read pulse generator
R_B	transistor base resistor
R_C	transistor collector resistor
R_1	effective resistance of primary loop
R_2	effective loading of the core
reg.	register
r	radix number
$r_{CE(sat)}$	saturation resistance of transistor CE junction
r_D	diode forward resistance
r_s	switching winding resistance
S	clear switch of magnetic counter
	set input of flip-flop
	total domain wall area per volume
SR	squareness ratio of magnetic core
SUB	subtraction control signal

Σ	scalar sum
T	pulse width
	change 'circuit state' input of magnetic counter
	delay time
T_c	Curie temperature
T_s	switching time
T_j	transistor
t	time
τ	domain volume
V	voltage
$V_{BE(sat)}$	saturation voltage of transistor BE junction
V_C	transistor collector voltage
V_{CC}	supply voltage
$V_{CE(sat)}$	saturation voltage of transistor CE junction
V_D	diode forward voltage
V_{DT}	voltage drop across diode and ON transistor CE
	junction during pulsing
V_E	transistor emitter voltage
V_{in}	input voltage
V_{ind}	induced voltage
V_o	output voltage
V_s	switching voltage
v	speed of domain boundary motion
Φ	magnetic flux
Φ_r	flux remanence
Φ_s	saturation flux
φ	angle
ψ	function of flux

I. Introduction

Square-loop core has long been used as binary element in the control, communication and computing systems for years. Only in the last decade, its application has been extended to multilevel storage, which is effected by changing the flux level in the hysteresis loop of the core. This chapter gives a brief review of the development of multilevel core counters and explains the aims of the project.

1.1 Magnetic core characteristics

Magnetic core material which exhibits a rectangular hysteresis loop (Fig.1-1) has two unique values of flux at zero applied field, $+\Phi_r$ and $-\Phi_r$, called remanence or residual flux. These are the binary states of the core. The positive remanence $+\Phi_r$ may be designated as the binary 1, or set state and $-\Phi_r$ as the binary 0 or reset state. To change the remanence, a field, called coercive force H_c, must be applied in reverse. A core can then be switched from one state to the other by applying a current pulse through a winding wound on the core. The dynamic path during the switching are indicated by the dotted lines 'rabs' and 'scdr' in Fig.1-1. The nearly horizontal paths 'ra' and 'sc' are traversed during the rise time of the applied pulse and the paths 'bs' and 'dr' during the fall time. Hence, it can be seen that the nearly vertical paths, which give rise to most of the flux reversal, take up the most of the switching time.

The rectangular-hysteresis-loop core is very useful as storage element. Because of its two distinct remanent states of magnetization

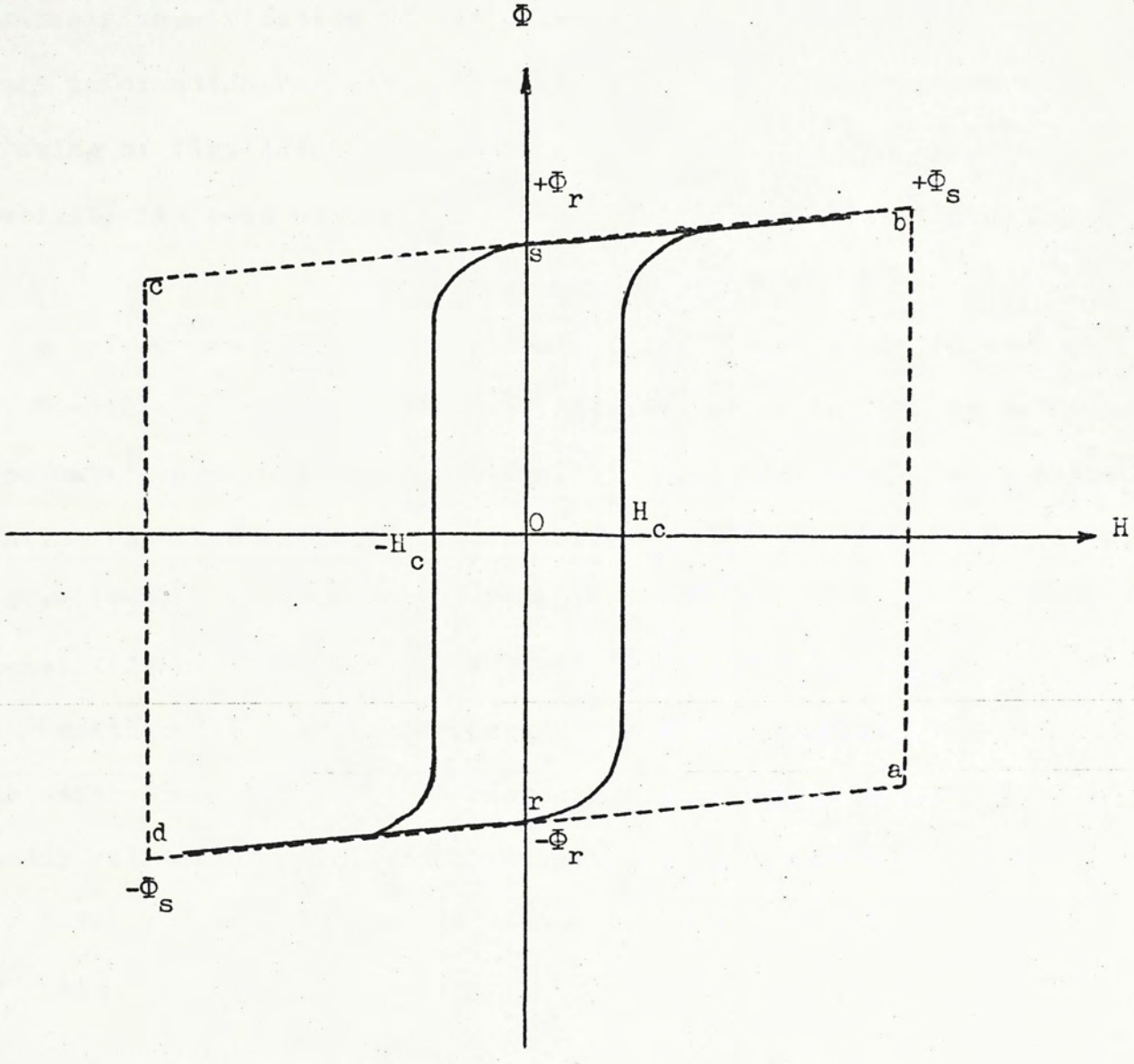


Fig.1-1 A rectangular hysteresis loop

which provide bistable operation, it has been used in digital computation and control. However, the characteristic of rectangular hysteresis magnetization is not only its capability of handling binary information but also its volt-time integral determined by the swing of flux level in the hysteresis loop. This integrating capability has been utilized in development of multilevel counters.

1.2 Brief review of the development of multilevel magnetic core counter

The idea of multilevel switching was started in 1952 by Duffing-Tschermark[1], and further by Pittman(1955)[2]. Its application in pulse counting was then exploited by Schaeffer(1958)[3], Sakurai-Tanaka(1959)[4], Hardies(1959)[5], Nisbet(1960)[6], Freeman(1962)[7], Carter-Knoke(1962)[8], Rozenblat(1966)[9], Ho(1968)[10], Ho(1971)[11] and Rozenblat-Fedin(1973)[12].

Consider the hysteresis characteristic shown in Fig.1-1. The flux swing from $+\Phi_s$ to $-\Phi_s$ in response to an applied voltage V is exactly related to a volt-time integral. If the core has a winding of N turns and the winding resistance is small, the core flux is then given by :

$$\Phi_s = \frac{1}{2N}\int V\,dt \qquad (1\text{-}1)$$

which shows that the core integrates the input voltage with respect to time until a definite value of the integral is attained, at which time it saturates.

Suppose the input consists of a series of unidirectional pulses of equal volt-time area, then a fixed number of such pulses, say n pulses, will be required to drive the core from negative to positive saturation, i.e.

$$2 N \Phi_s = \sum_{1}^{n} \int_{\Delta t} V \, dt \qquad (1\text{-}2)$$

where Δt is the duration of the voltage pulse.

With this fundamental concepts, Pittman[2] built a circuit as shown in Fig.1-2, in which transistor T_1 is activated by the input pulses V_{in} at a fixed frequency and thus switching the core from negative saturation to positive saturation. Transistor T_2 is used for resetting the flux instantly to negative saturation from positive saturation. During the resetting, a voltage pulse is obtained at the output terminals (Fig.1-3).

In 1958, Schaeffer slightly modified the circuit of Fig.1-2 and applied it in event counting for earth satellite[3]. Later, Hardies made a further investigation of its capability of time delays[5]. In 1960, Nisbet proposed a magnetic decade counter yet operating in the same principle (Fig.1-4), except that the core is energized in one direction by discharging a "counting" capacitor and then the other direction by discharging a "reset" capacitor. His circuit however has a limitation in counting speed due to the time required for recharging the capacitors.

In 1962, Freeman improved the reliability and operating range of previous magnetic counters by adding a pulse forming circuit (Fig.1-5)[7], which provides the required constant volt-second pulse to the counter regardless of the characteristics of the input pulses. The pulse former uses a core identical to the counter core.

The drawback of the foregoing circuits is that there are too many operating windings on the rectangular hysteresis loop core besides the output winding, which makes it unattractive in production.

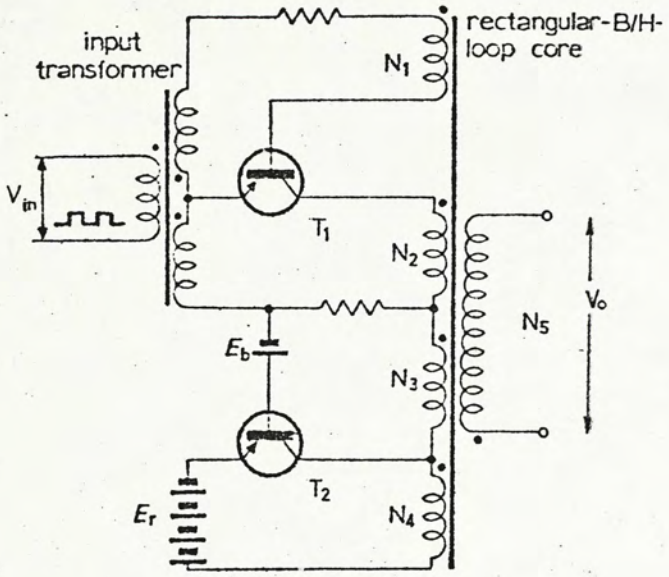


Fig.1-2 Pittman's time delay circuit

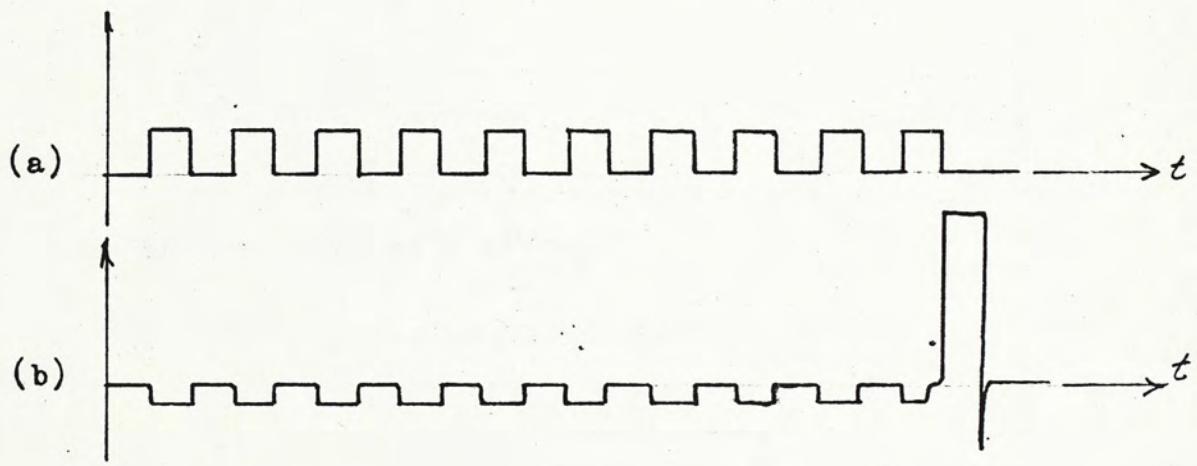


Fig.1-3 Input and output for the circuit of Fig.1-2
(a) input V_{in} (b) output V_o

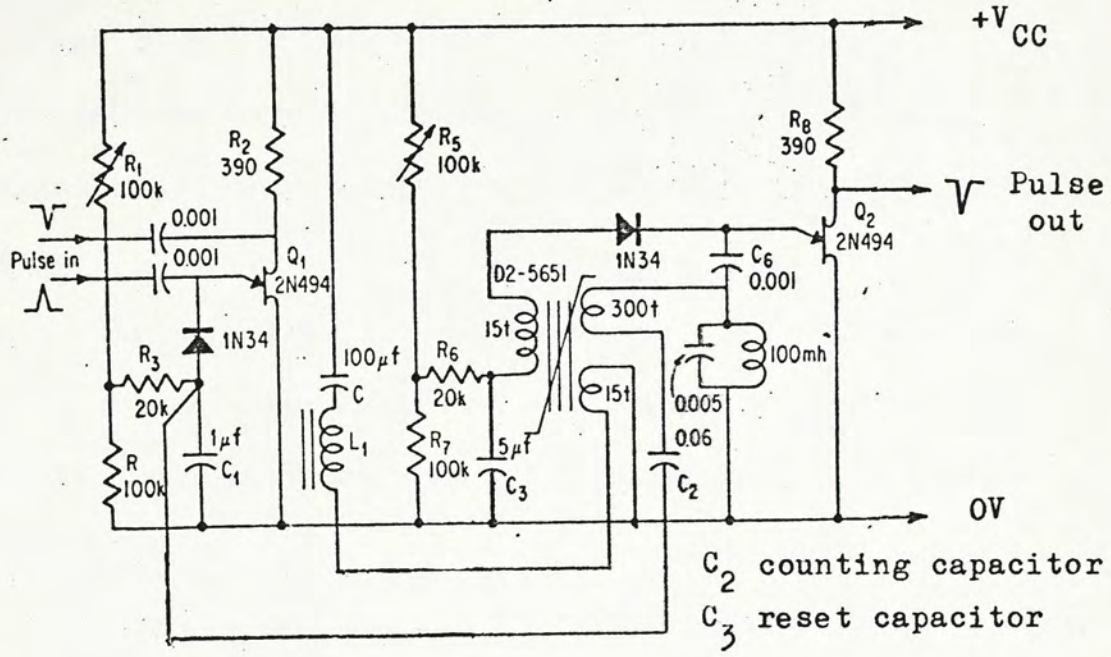


Fig.1-4 Nisbet's decade counter

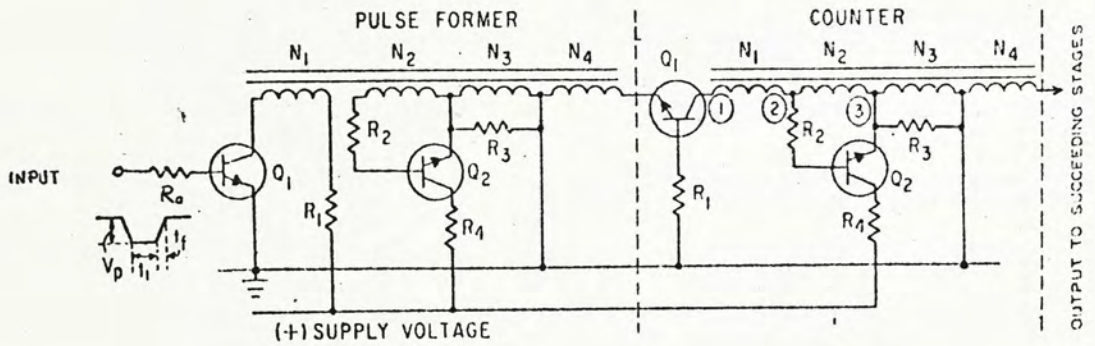


Fig.1-5 Freeman's circuit

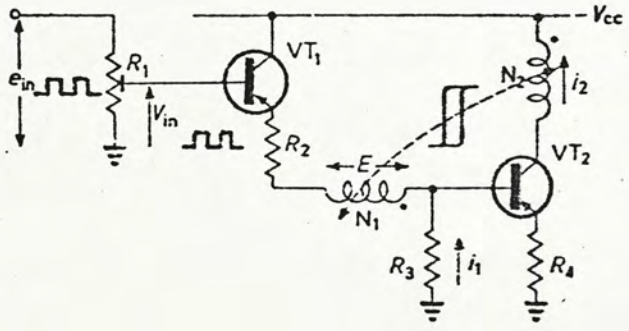


Fig.1-6 Simplified counter circuit by Ho

Then, Ho developed a simpler circuit (shown in Fig.1-6) by removing some windings on the core but still maintaining the same performance.

Also various methods have been proposed for improving the linearity in magnetic switching. For example, Hardies in 1959[5] used bipolar write pulses and Rozenblat in 1966[9] introduced positive feedback to compensate the nonlinear effect in magnetic switching. However, the proposed schemes are found not sufficiently effective and are too complicated for use in systems which contain a large number of core counters.

However, all counters have one common feature that is the counter core is driven in a number of discrete steps from negative to positive saturation by a series of unidirectional pulses of equal volt-time area. After the magnetic state has reached the positive saturation, the core is immediately reset to the negative saturation. During the resetting operation, the input pulse cannot be applied, i.e., the resetting interval must be shorter than the idle period between two input pulses. This results in limiting the counting speed. Also, the rapid change of flux from positive to negative saturation will induce a large e.m.f. in the input winding, thus the transistor used must be able to withstand the high peak voltage. These drawbacks had been remedied by Ho[11] in 1971. He made use of a flip-flop incorporated with a centre tapped winding to energize the core such that a stepwise magnetic flux is built up in one direction and then reversed in the other direction after reaching saturation. By doing so, the counting capability of the core and the speed are increased. Present investigation is an extention of Ho's work.

1.3 Object of the research

The aim of the project is to find a decimal counter which can perform the following :

(1) Reversible counting

So far no multilevel magnetic counter are able to perform reversible counting because of the difficulty in reversing the path of the hysteresis loop. For binary mode of operation, this problem does not exist as the core only changes its states between two remanences. Hence, the primary aim of the project is to find a method for reversible counts.

(2) Nondestructive readout

The readout method is a difficult problem for multilevel magnetic counter since the information on the state of count is contained in the magnetic flux of the cores. When the transfluxor is used as counting core, the readout circuit can be connected to the small aperture [12, 13] and an induced voltage proportional to the change of the flux level is obtained. However the transfluxor is an expensive core compared with the toroid. For the sake of economy, we want to study whether a nondestructive readout can be arranged for an ordinary toroidal core.

(3) Arithmatic operation

A proper interconnection of decimal magnetic counters can perform arithmatic operation such as addition, subtraction, multiplication and division.

II. Direct Storage Of Decimal Number

Although binary number system is well developed, it is by no means the best number system for machine computation. This chapter explains why the decimal system is the most suitable one for machine calculation and also introduces a circuit for storage of decimal number.

2.1 Reasons for the choice of decimal number system

Although nowadays computers and electronic calculators are operated with systems in binary nature, it is by no means that binary is the only possible system for development of these machines. One should remember that the steps that lead to the present state of binary system development are :

1) the purely philosophical logic concepts of "true" and "false",
2) the mathematical foundations by Boole[14],
3) the establishment of a switching theory by Nakasima[15] and Shannon[16] based on Boole's mathematical foundations.

In addition, because of the availability of binary switching device which is assumed inexpensive and reliable, it gives an impression that there is no prospect of developing comparable decimal or other radix devices. The binary representation has thus been universally employed, no matter what the radix choice (ternary, quinary, octal, decimal, etc.) is for a particular machine.

However, before one is satisfied with the well established binary system, one may better ask himself if it is the most efficient number system. This question may be separated into two parts :

1) Which number system will require a minimum number of storage equipment in order to represent a given number ?

and 2) Which number system will perform the simplest arithmatic operation ?

To answer the first part, it has been presented by several authors [17,18] that the amount of equipment , E, required to store a number $N = r^m$ in an r-radix system is proportional to r, i.e.

$$E = c\, r\, m \qquad (2\text{-}1a)$$

where c is a proportional constant.

Substituting in (2-1a) for $m = \frac{\ln N}{\ln r}$

$$E = c\, r \left[\frac{\ln N}{\ln r}\right] \qquad (2\text{-}1b)$$

Differentiating (2-1b) with respect to r, we obtain a minimum at $r = e \cong 2.718$. Integral radices only are of practical interest. The number 3 is nearer to e than 2. Table 2.1 shows the amount of equipment required to store an arbitrary number $N = e^{30}$ (which is chosen for convenience of calculation) and apparently, ternary system is favourable. However, since the decimal system is used in the majority of computer input-output devices, it is easily shown that the ternary system is one of the least efficient number systems for such applications, because the ternary-coded decimal utilizes only 37 percent of the available states (10 out of 3^3) as compared to the BCD where 10 out of 16 states are used. Further, equ.(2-1a) was formulated on the assumption that there would be no multi-state

storage elements available except the binary ones. If multi-level switching devices are developed, such an argument will no longer hold. In fact, the development of a particular computing machine is based on the technique of conversion of decimal to a certain radix and that radix to decimal (e.g. decimal to binary and binary to decimal). Because of such conversion, it requires many storage elements which are necessary unless direct computation with decimal system could be established.

Table 2.1 Total number of storage equipment required to store a certain number for various radix (calculation is based on an assumed number $N = e^{30}$)

r	ln r	$\left[\frac{\ln N}{\ln r}\right]$	$r\left[\frac{\ln N}{\ln r}\right] \propto E$	
2	0.693	44	88	
3	1.099	28	84	← Minimum
4	1.386	22	88	
5	1.609	19	95	
6	1.792	17	102	
7	1.946	16	112	
8	2.079	15	120	
9	2.197	14	126	
10	2.303	14	140	
11	2.398	13	143	
12	2.485	13	156	
13	2.565	12	156	
14	2.639	12	168	
15	2.708	12	180	
16	2.773	11	176	
17	2.833	11	187	
18	2.890	11	198	
19	2.944	11	209	
20	2.996	11	220	

As to the arithmatic operation, any number system can perform it well, since they all follow a few simple rules of their own. Taking addition as example, in the decimal system, where there are ten symbols, if the addition of two symbols is greater than 9 then a digit is carried to a higher order of ten. The game applies to ternary and binary numbers, where there are only three and two symbols respectively. The tables for decimal, ternary and binary additions are shown in Table 2.2 .

However, one may immediately notice from the tables that only the decimal system can give the direct answer of sums while the others need encoding and decoding process in the computation when same answer as that obtained by decimal system is desired. Thus the choice of decimal system seems to be the best.

2.2 A magnetic decimal counter

As already mentioned in the Introduction that the square hysteresis loop core has been used by many people[1-11] as a device for storing and counting because of its unique volt-time integrating property. The early types of counter have only the ability to count-up or down, i.e., the core is driven from the negative saturation to positive saturation by a series of unidirectional pulses of equal volt-time area (Fig.2-1). After reaching the positive saturation, the core is reset to the negative saturation. The long resetting time from one saturation state to the other during which no data can be applied and the large induced e.m.f. due to the rapid change of magnetic flux are the main disadvantages of these counters. It was in 1971 that Ho designed a counter which has the ability of

Table 2.2 Addition tables for decimal, ternary and binary number system

+	0	1	2	3	4	5	6	7	8	9
0	0	1	2	3	4	5	6	7	8	9
1	1	2	3	4	5	6	7	8	9	10
2	2	3	4	5	6	7	8	9	10	11
3	3	4	5	6	7	8	9	10	11	12
4	4	5	6	7	8	9	10	11	12	13
5	5	6	7	8	9	10	11	12	13	14
6	6	7	8	9	10	11	12	13	14	15
7	7	8	9	10	11	12	13	14	15	16
8	8	9	10	11	12	13	14	15	16	17
9	9	10	11	12	13	14	15	16	17	18

(a) Addition table for decimal number system

+	000	001	002	010	011	012	020	021	022	100
000	000	001	002	010	011	012	020	021	022	100
001	001	002	010	011	012	020	021	022	100	101
002	002	010	011	012	020	021	022	100	101	102
010	010	011	012	020	021	022	100	101	102	110
011	011	012	020	021	022	100	101	102	110	111
012	012	020	021	022	100	101	102	110	111	112
020	020	021	022	100	101	102	110	111	112	120
021	021	022	100	101	102	110	111	112	120	121
022	022	100	101	102	110	111	112	120	121	122
100	100	101	102	110	111	112	120	121	122	200

(b) Addition table for ternary number system

+	0000	0001	0010	0011	0100	0101	0110	0111	1000	1001
0000	0000	0001	0010	0011	0100	0101	0110	0111	1000	1001
0001	0001	0010	0011	0100	0101	0110	0111	1000	1001	1010
0010	0010	0011	0100	0101	0110	0111	1000	1001	1010	1011
0011	0011	0100	0101	0110	0111	1000	1001	1010	1011	1100
0100	0100	0101	0110	0111	1000	1001	1010	1011	1100	1101
0101	0101	0110	0111	1000	1001	1010	1011	1100	1101	1110
0110	0110	0111	1000	1001	1010	1011	1100	1101	1110	1111
0111	0111	1000	1001	1010	1011	1100	1101	1110	1111	10000
1000	1000	1001	1010	1011	1100	1101	1110	1111	10000	10001
1001	1001	1010	1011	1100	1101	1110	1111	10000	10001	10010

(c) Addition table for binary number system

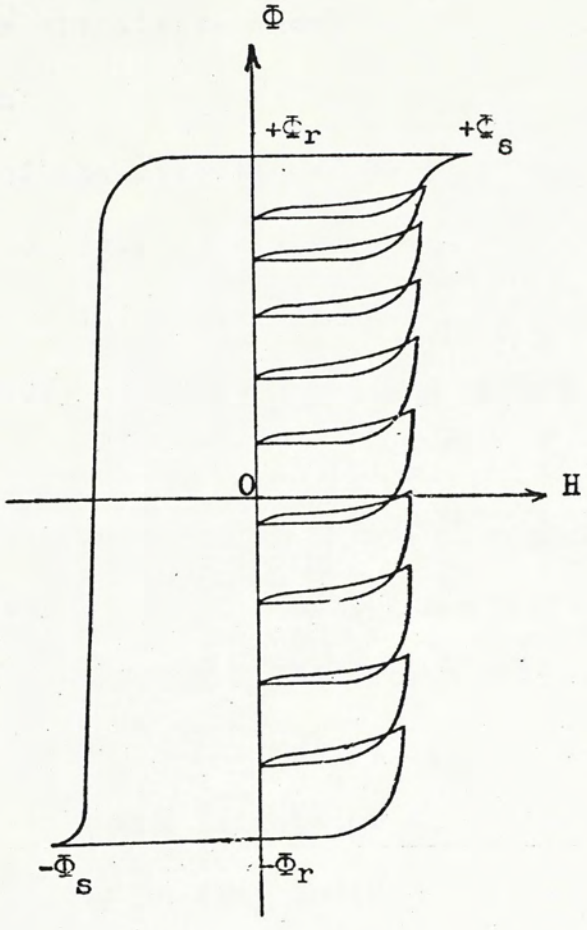


Fig.2-1 Incrementation of magnetic flux inside the magnetic core for conventional magnetic counters

both count-up and count-down, thus eliminating the disadvantages mentioned above. The circuit is shown in Fig.2-2.

2.2.1 The operation

The operation of the circuit can be briefly illustrated as follows (referring to Fig.2-2) : assume that in the quiescent condition, the core is initially placed at the negative saturation, transistor Q_1 is saturated ($V_{C1} \cong 0$) , Q_2 is cutoff ($V_{C2}=V_{C(off)}$) and Q_3 is cutoff.

Now if a positive rectangular pulse of amplitude V_{in} is applied to the base of transistor Q_3 at $t=t_1$, the diode D_1 connected to the collector of the ON transistor Q_1 will be the first to conduct while D_2 remains non-conducting. A current, i_1 , thus starts to flow through the left winding N_1 , D_1 and transistor Q_1 . This current causes a voltage drop V_s to appear in the winding N_1 which consists of the induced e.m.f. V_{ind} ($=N_1 \frac{d\Phi}{dt}$) and the IR drop on the winding resistance. If the winding resistance is small and the core is not saturated, it can be noted that $V_s \cong V_{ind} \cong V_{CC}$. By the action of centre tapping ($N_1=N_2$), the induced e.m.f. V_{ind} appears also in the winding N_2 . The polarities of the induced e.m.f. is indicated in the circuit of Fig.2-2.

Let the potential at the emitter of transistor Q_3 be V_{E3} ($= V_{ind}+V_{D1}$). The potential at point A_2 is then equal to V_E+V_{ind} . Diode D_2 now conducts and it brings the collector voltage of Q_2 to a higher potential of a value given by $V_{E3}+V_{ind}-V_D$ (where V_D is the voltage drop across the diode D_2, $=V_{D2}$). This voltage will terminate at the time t_2 (Fig.2-3) when the input V_{in} ceases, and the collector voltage of Q_2 will then return to $V_{C(off)}$. During the pulsing

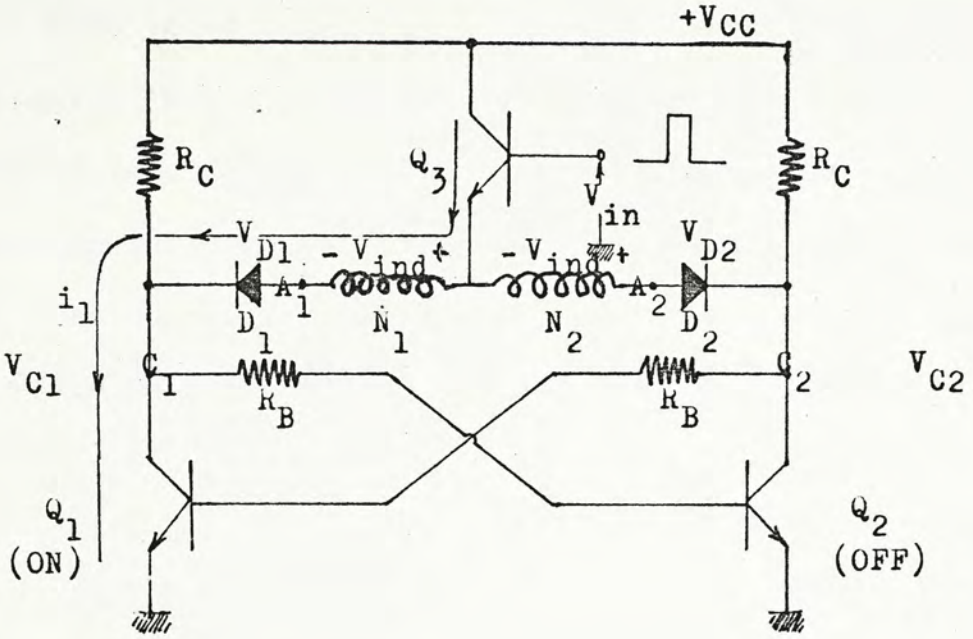


Fig.2-2 The improved decimal counter

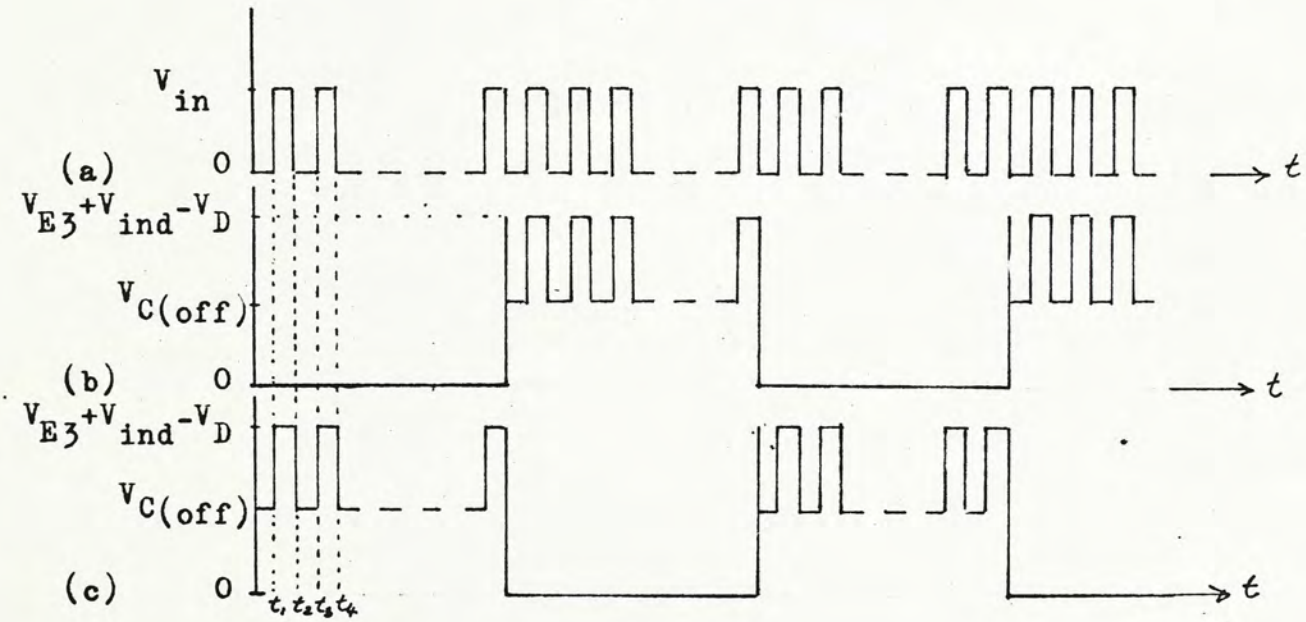


Fig.2-3 Change of collector voltage in response to input pulses for the circuit shown in Fig.2-2
(a) input pulse V_{in} (b) Q_1 collector voltage V_{C1}
(c) Q_2 collector voltage V_{C2}

period, from t_1 to t_2 , Q_1 remains in saturation.

For each input pulse V_{in} , there will be a corresponding change of flux level in the core. For instance, the first pulse V_{in} brings the flux to level '1' and after its termination at $t=t_2$, the flux remanence in the core is obtained corresponding to '1' as shown in Fig.2-4. The change of flux in response to the applied voltage pulse V_{in} is given by (Appendix II equ.AII-8) :

$$\frac{d\Phi}{dt} = \frac{\frac{N_1 V_s}{r_s} + \frac{N_2 V_D}{R_2} - H_o \ell}{\frac{N_1^2}{r_s} + \frac{N_2^2}{R_2}} \qquad (2\text{-}2)$$

where V_s is the voltage drop on the winding N_1 ,

r_s is the winding resistance,

R_2 is the effective loading of the core ($=R_B /\!/ R_C + r_s$),

H_o is the threshold force closely related to H_c ,

and ℓ is the mean length of the core.

Further application of the input pulse V_{in} with the same duration will switch the flux level to '2' and brings the magnetization of the core one step nearer to the positive saturation. The number of pulses n that will change the core flux from negative saturation $-\Phi_s$ to positive saturation $+\Phi_s$ is given by (Appendix II equ.AII-10)

$$n = \frac{2\,\Phi_s}{\frac{\frac{N_1 V_s}{r_s} + \frac{N_2 V_D}{R_2} - H_o \ell}{\frac{N_1^2}{r_s} + \frac{N_2^2}{R_2}} T - \Phi_s \frac{1-SR}{2}} \qquad (2\text{-}3)$$

where $T=t_2-t_1=t_4-t_3=\ldots$ is the duration of the input pulse, and SR is the squareness ratio of the core. The second term in the denominator is the magnetic flyback flux associated with the termination of each input.

At the n^{th} pulse, the flux reaches to the positive saturation and the inducted e.m.f. V_{ind} across the winding N_1 collapses. The collector of the transistor Q_1 will be approximately equal to (Appendix II equ.AII-11) :

$$V_{C1} = \frac{r_{CE(sat)}}{r_s+r_D+r_{CE(sat)}} \left[V_{in}-V_{BE(sat)}-V_D\right] \qquad (2\text{-}4)$$

where $r_{CE(sat)}$ is the saturation resistance of the CE junction of transistor Q_1 ,

and $V_{BE(sat)}$ is the saturation voltage of the BE junction of the switching transistor Q_3 .

This voltage will cause Q_2 to conduct and forces the flip-flop to flip over. The magnetic core is now excited with the winding N_2 (Fig.2-2). For the $n+1^{th}$ to $2n^{th}$ input pulses, the magnetic core is driven from $+\Phi_s$ to $-\Phi_s$, and the corresponding changes of flux are also in steps as shown in Fig.2-4. The flip-flop will flip over again at the end of the $2n^{th}$ pulse. Hence, the total number of pulses that can be stored in the counter is equal to :

$$2n = \frac{4\,\Phi_s}{\dfrac{\dfrac{N_1V_s}{r_s}+\dfrac{N_2V_D}{R_2}-H_o\ell}{\dfrac{N_1^2}{r_s}+\dfrac{N_2^2}{R_2}}\,T-\Phi_s\dfrac{1-SR}{2}} \qquad (2\text{-}5)$$

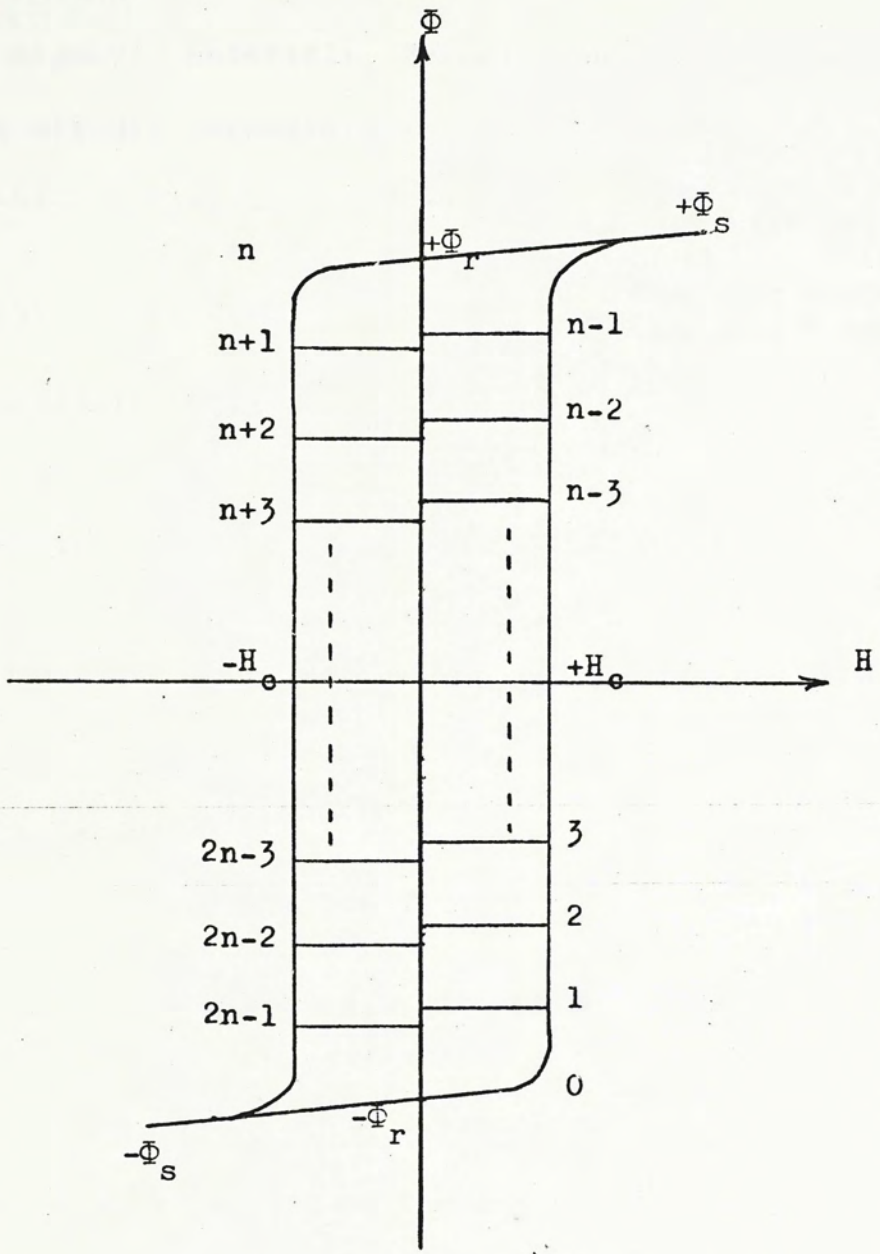


Fig.2-4 Change of flux level in the magnetic core for the circuit shown in Fig.2-2

2.2.2 The performance

Measurements of the circuit of Fig.2-2 were obtained on two kinds of magnetic materials, Permalloy G and F, together with the following circuit parameters :

V_{CC}=5V R_C=1.1K $N_1=N_2=$ {350 turns (s.w.g.38) for G core; 400 turns (s.w.g.38) for F core}

V_{in}=5V R_B=8.2K r_s = {9.4 ohm for G core; 10.7 ohm for F core}

Transistors (Q_1,Q_2,Q_3) : 2N4127

Diodes (D_1 , D_2) : OA47

Core dimensions : Inner diameter d_i = 12.7 mm

Outer diameter d_o = 19.0 mm

Height h = 6.3 mm

Mean length ℓ = 4.99 cm

Core characteristics :

Saturation flux Φ_s = {2.39×10^{-5} weber for G core; 2.70×10^{-5} weber for F core}

Squareness ratio SR = {0.950 for G core; 0.9286 for F core}

Threshold force H_o = 40 A/m for both G and F core

Fig.2-5 shows a plot of the input pulse width (T) against the reciprocal of the corresponding stored number (1/2n) in the counter for both Permalloy G and F cores. It was found that the Permalloy F core having a larger saturation flux Φ_s, less squareness ratio SR (hence larger magnetic flyback flux) and more winding wound on it, requires a larger pulse width than the G core to store the same number in the counter.

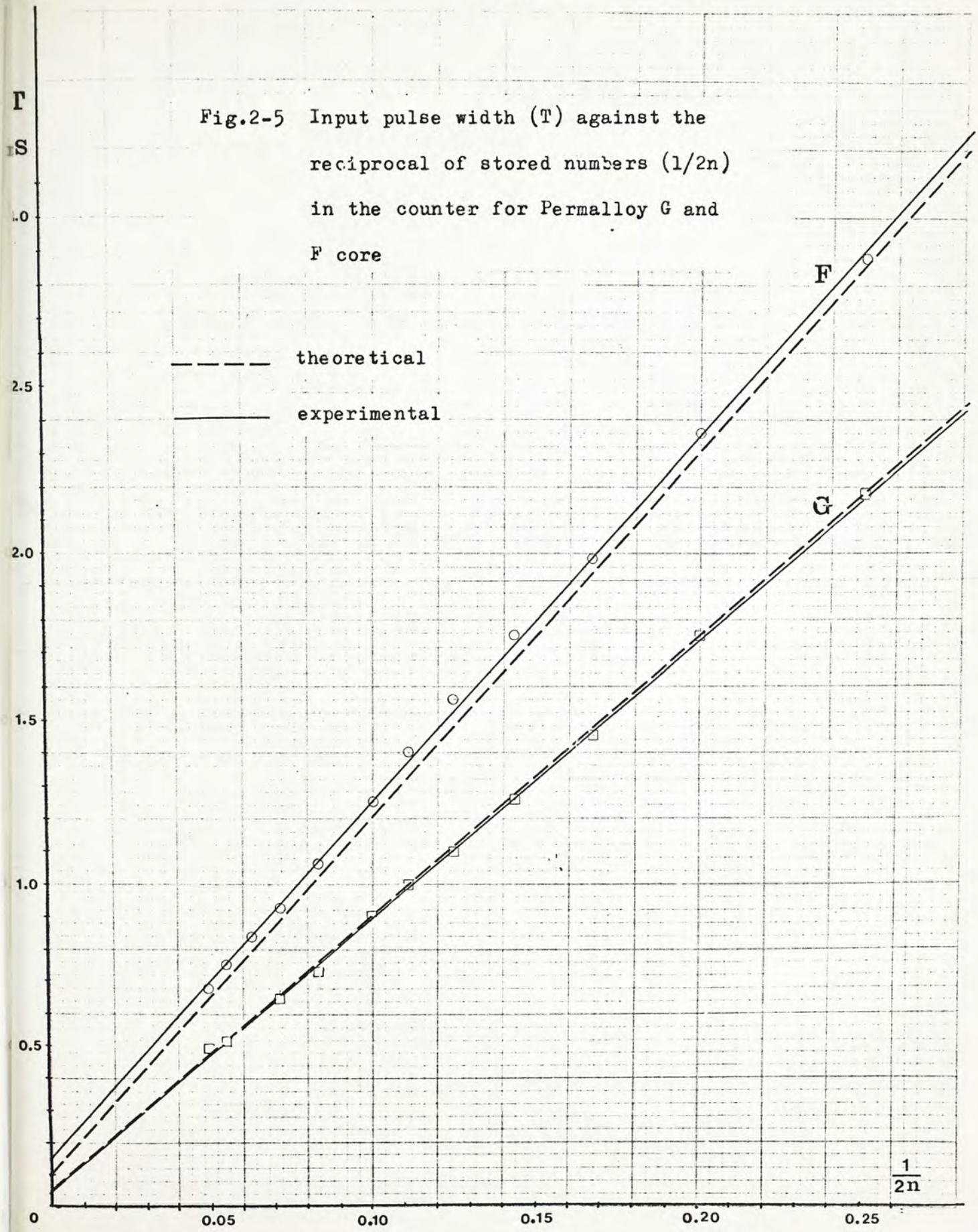


Fig.2-5 Input pulse width (T) against the reciprocal of stored numbers (1/2n) in the counter for Permalloy G and F core

For the sake of comparison of the experimental and the theoretical results , equ.(2-5) can be rewritten as :

$$T = \frac{k'}{2n} + T_o \qquad (2\text{-}6)$$

where $k' = \frac{4\Phi_s}{c}$ is the slope of the straight line,

$$T_o = \frac{\Phi_s \frac{1-SR}{2}}{c}$$ is the y-intercept,

and $$c = \frac{\frac{N_1 V_s}{r_s} + \frac{N_2 V_D}{R_2} - H_o \ell}{\frac{N_1^2}{r_s} + \frac{N_2^2}{R_2}}$$ is a circuit parameter.

Substituting the data given in the previous page into (2-6) yields :

$$T\ (mS) = \begin{cases} \frac{8.547}{2n} + 0.053 & \text{for the G core counter} \quad (2\text{-}7a) \\ \frac{11.047}{2n} + 0.099 & \text{for the F core counter} \quad (2\text{-}7b) \end{cases}$$

The corresponding experimental results are :

$$T\ (mS) = \begin{cases} \frac{8.503}{2n} + 0.0445 & \text{for the G core counter} \quad (2\text{-}8a) \\ \frac{11.029}{2n} + 0.149 & \text{for the F core counter} \quad (2\text{-}8b) \end{cases}$$

The discrepancy between equ.(2-7) and equ.(2-8) is given below.

$$\Delta k' = \begin{cases} -0.51\% & \text{for G core counter} \\ -0.16\% & \text{for F core counter} \end{cases}$$

$$\Delta T_o = \begin{cases} -16.0\% & \text{for G core counter} \\ +50.5\% & \text{for F core counter} \end{cases}$$

It can be seen that the SR of Permalloy F core is too low to be used as a 'multi-level' storage device.

By choosing a suitable pulse width for decimal storage, the input voltage V_{in} , switching current i_1 , collector voltages of Q_1 and Q_2 , rate of change of flux $\frac{d\Phi}{dt}$ and the flux level Φ for both Permalloy G and F core were measured and then shown in Fig.2-6 and Fig.2-7 respectively.

From these figures, it can be observed that the switching current increases abruptly at the end of the 5^{th} and the 10^{th} pulses which corresponds to the collapse of the induced e.m.f. V_{ind} .

The rate of flux change is consistent during pulsing period (Fig.2-6(e) and Fig.2-7(e)). A comparison of the theoretical predictation and the experimental result is given as following :

core material	theoretical	experimental	difference
Permalloy G	0.01127 weber/sec	0.0115 weber/sec	+2.0%
Permalloy F	0.00979 weber/sec	0.00925 weber/sec	-5.5%

The main reason that F core has a lower switching rate is that the number of turns is larger. This linear rate of flux change is a consequence of the voltage switching under the condition of low circuit resistance (discussion on this aspect is given in Appendix I).

The magnetic flux flybacks are also noted in the figures for both materials. Permalloy F has a less square hysteresis loop thus its flyback effect is more pronounced.

The 10 discrete flux states with 5 on the count up direction and 5 on the count down direction are noted in the flux display (Fig.2-6(f) and Fig.2-7(f)).

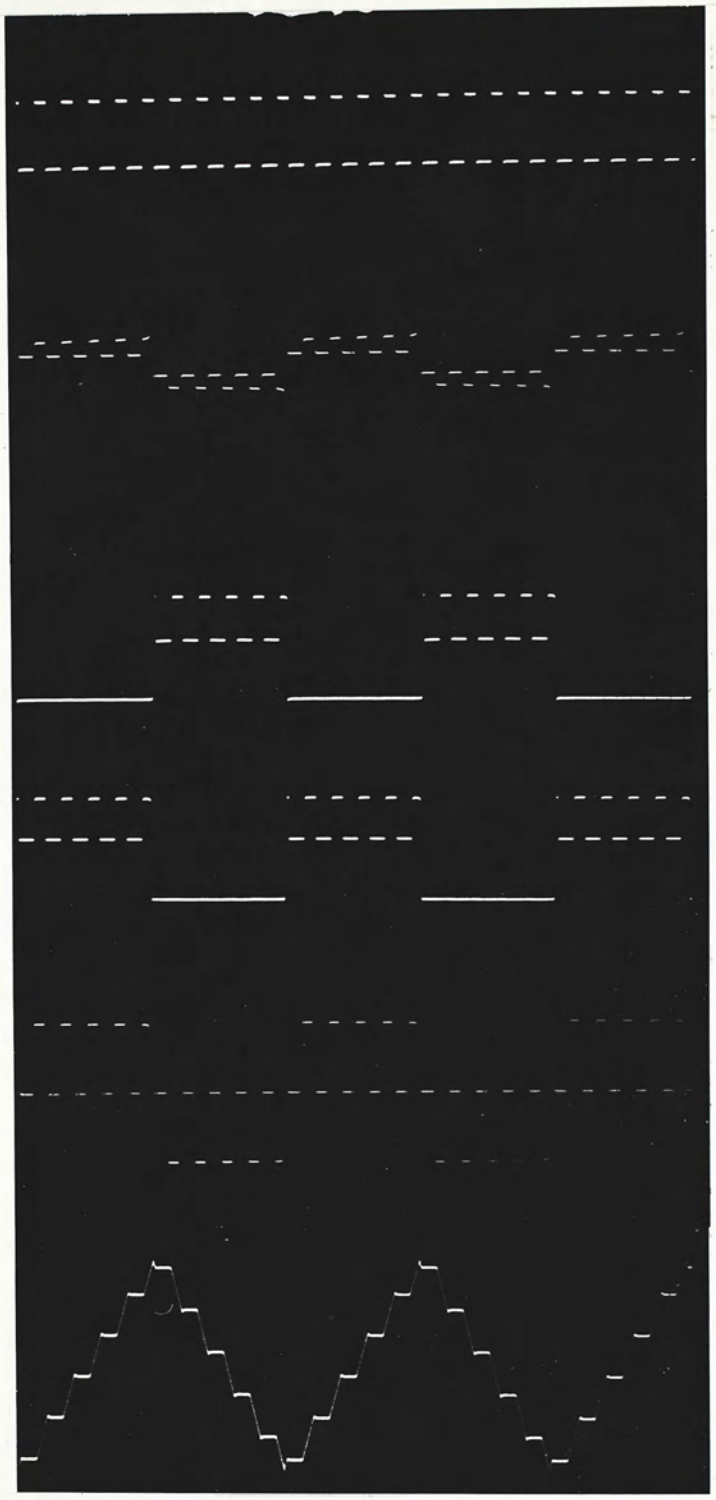


Fig.2-6 Measured waveform of the Permalloy G core magnetic decade counter

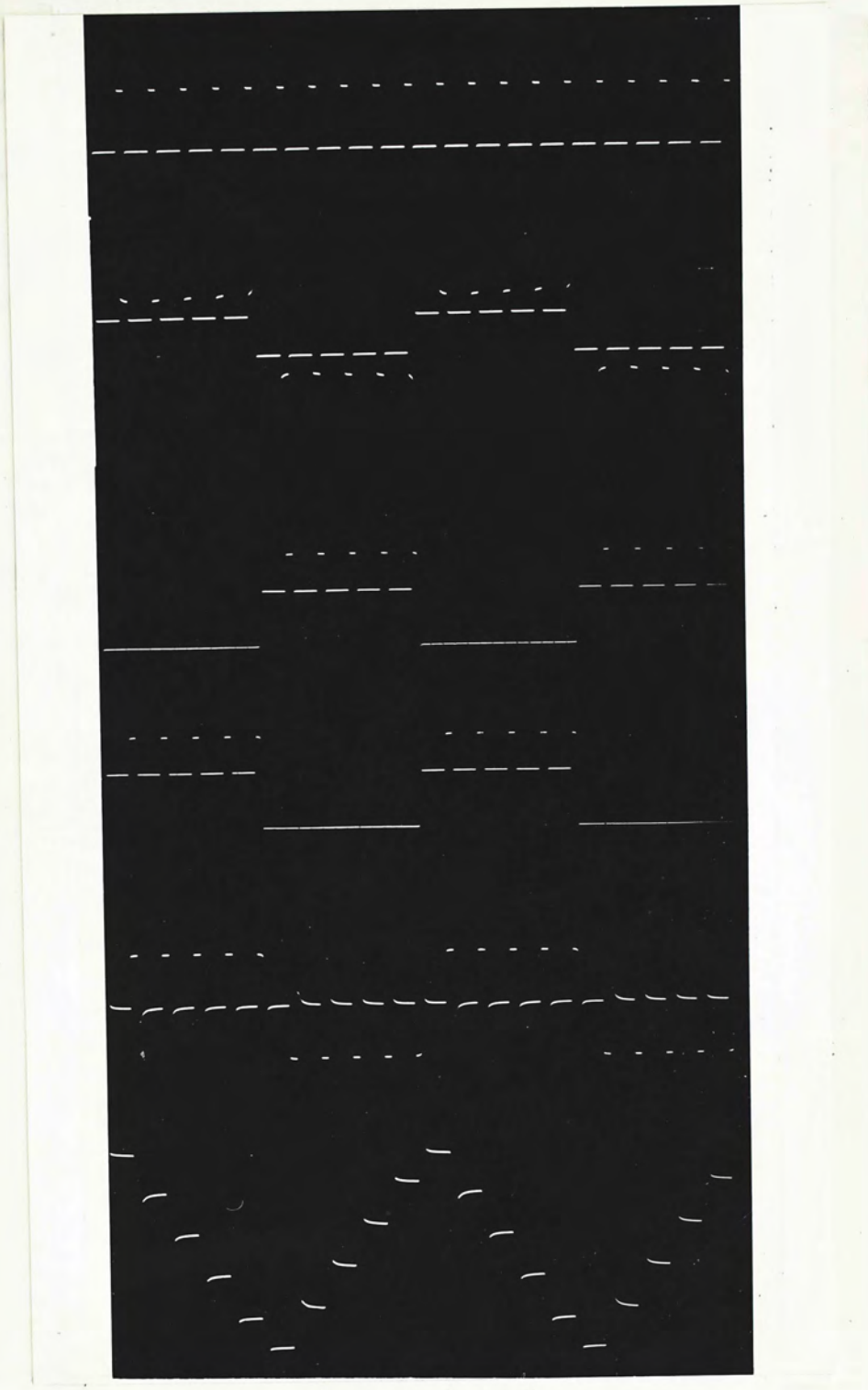
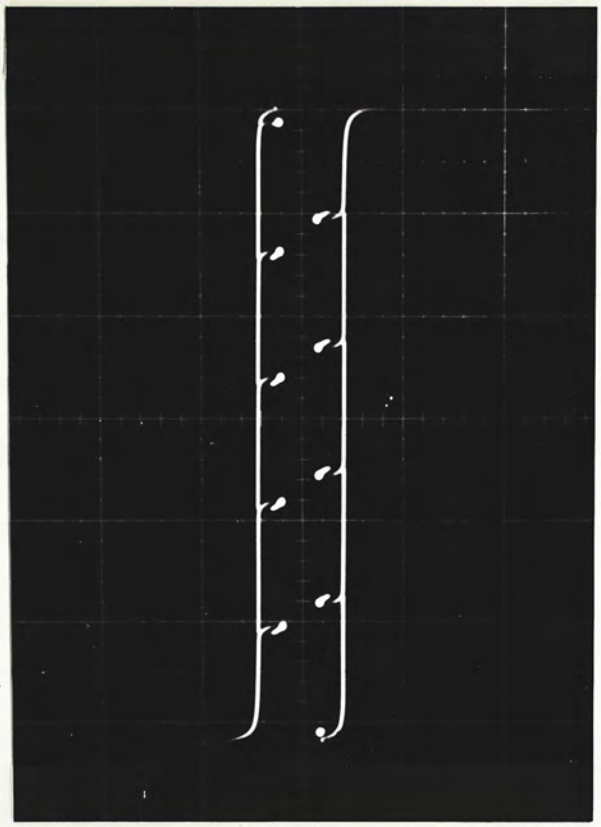


Fig.2-7 Measured waveform of the Permalloy F core magnetic decade counter

The hysteresis loops for both materials G and F during pulsing are shown in Fig.2-8 and 2-9 respectively. It should be noted that the current flowing in the windings was obtained by putting a small monitoring resistor in each emitter of the transistor, consequently a d.c. component was imposed in it. However the hysteresis loops so obtained are still very impressive.

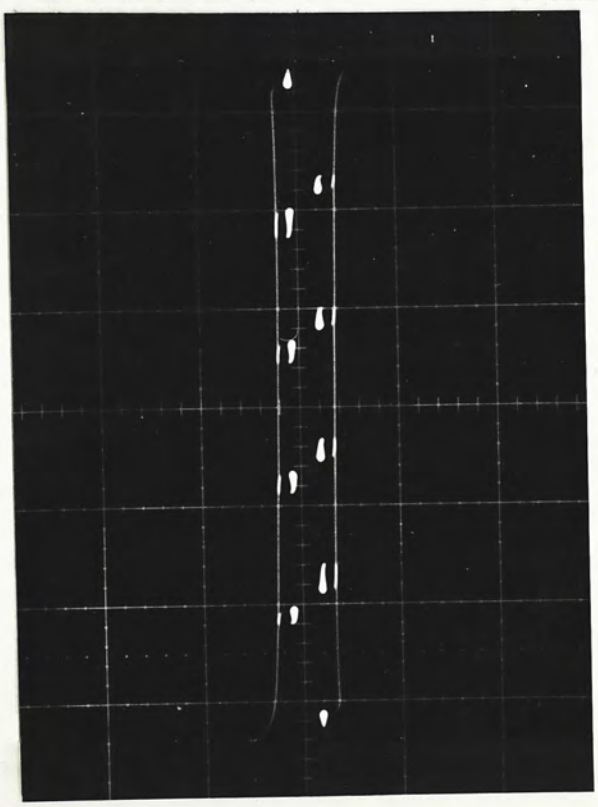
The stability of the magnetic counter was found fairly high. The decimal storage capacity was found to be unchanged after many hours of continuous operation.



Horizontal : H
187 A/m/DIV

Vertical : Φ
0.75×10^{-5}
weber/DIV

Fig.2-8 Hysteresis loop of Permalloy G core in decimal storage



Horizontal : H
267 A/m/DIV

Vertical : Φ
0.75×10^{-5}
weber/DIV

Fig.2-9 Hysteresis loop of Permalloy F core in decimal storage

III. Reversible Count Of Magnetic Counter

The magnetic counter considered in the last chapter is a forward decimal counter. The counter 'runs' for one complete cycle for every ten input pulses with defined volt-time integral. This chapter explains how to operate the circuit in reversible counts. Also, a single stage reversible magnetic counter is constructed.

3.1 Principle of reversible operation

In order to understand the principle of reversible operation of the circuit shown in Fig.2-2, let us consider its simplified circuit represented by Fig.3-1 in which transistors Q_1, Q_2 and Q_3 are represented by the switches S_1, S_2 and S respectively. Battery with emf $\mathcal{E}$ is equivalent to the input voltage V_{in}. An input pulse of width T applied to the circuit is considered now as closing switch S for a time of duration T. It is first assumed that switch S_1 is closed, switch S_2 is open and the core is at a magnetic flux $-\Phi_r$ (Fig.3-1b) which is substantially the same as the negative saturation $-\Phi_s$. Switch S is now closed providing a pulse current i_1 to magnetize the core in the positive direction. When '1' is attained (Fig.3-1b) after a duration of time T, S is opened to terminate the current pulse. As the current i_1 ceases, a remanence is obtained corresponding to the flux of point '1' and having substantially the same value. Assume that S has been closed four times and the flux level '4' is attained. Now, it is desired to subtract 'one' (or, reversely count 'one') from the content of storage of '4'. The way of achieving it is by the following procedure :

1) Open switch S_1 and close switch S_2 so as to provide a path for the flow of current i_2 which is in opposition to i_1.
2) Close switch S <u>once</u> (with the preset time interval T) to provide a current i_2 to winding N_2 (Fig.3-1a). The flux in the core is thus reversed as indicated by the path 'abcd' in Fig.3-1b.
3) Close switch S_1 and open switch S_2 again so that the core will be continuously magnetized by i_1 in the positive direction.

If the magnetic switching is linear, i.e., the flux level can be expressed in the general form :

$$\Phi(n) = \begin{cases} \Phi(0) + n\,\Delta\Phi_{eff} & n \leq 5 \\ \Phi(0) + (10-n)\,\Delta\Phi_{eff} & n \geq 5 \end{cases} \qquad (3\text{-}1)$$

where n is the stored number,

$\Phi(0)$ is the initial flux level ($= -\Phi_r$) ,

$\Delta\Phi_{eff}$ is the effective flux switching for each input.

The flux level corresponding to the storage of '4' will come down to that corresponding to the storage of '3'.

It is worth to note that in changing the 'circuit state' once (i.e., the interchange of the switching conditions of S_1 and S_2) , the states in the core are changed into the complement of the original states automatically. Take the storage of '4' as example (Fig.3-1b), when S_1 is closed, the flux remanence of '4' is at point 'a'. After S_1 is opened and S_2 is closed, the remanence 'a' becomes that of storage '6', because on applying the 7^{th} pulse, the flux in the core moves down to point '7' yielding a corresponding value of remanence 'd'.

Based on this idea, a way of subtraction (or, reversible count) is obtained, and its process can be illustrationed as follows (for decimal operation) .

step	circuit condition	content (change of flux level)
1.	Reset	0
2.	Input A pulses	A
3.	Change 'circuit state'	10-A
4.	Input B pulses	(10-A) + B
5.	Change 'circuit state'	$10-\left[(10-A)+B\right] = A - B$

The above illustration applies to one single counter only. It is also assumed that both A and B are less than 10. If several of this counter are cascaded to form register of many digits, negative sign can be generated to indicate negative numbers are obtained in the subtraction (or, reverse count).

The ideal changes of flux level in the core for the decimal digit and its corresponding complement are indicated in Fig.3-2a. The actual changes of flux states are shown in Fig.3-2b. The difference in the flux level of a digit and its complement, says, δ , is due to the non-ideal characteristic of the magnetic core. However, the complement theory of reversible count is still valid as long as δ is a constant (which is a consequence of the build-up of magnetic flux in equal steps,i.e. the linear magnetic switching).

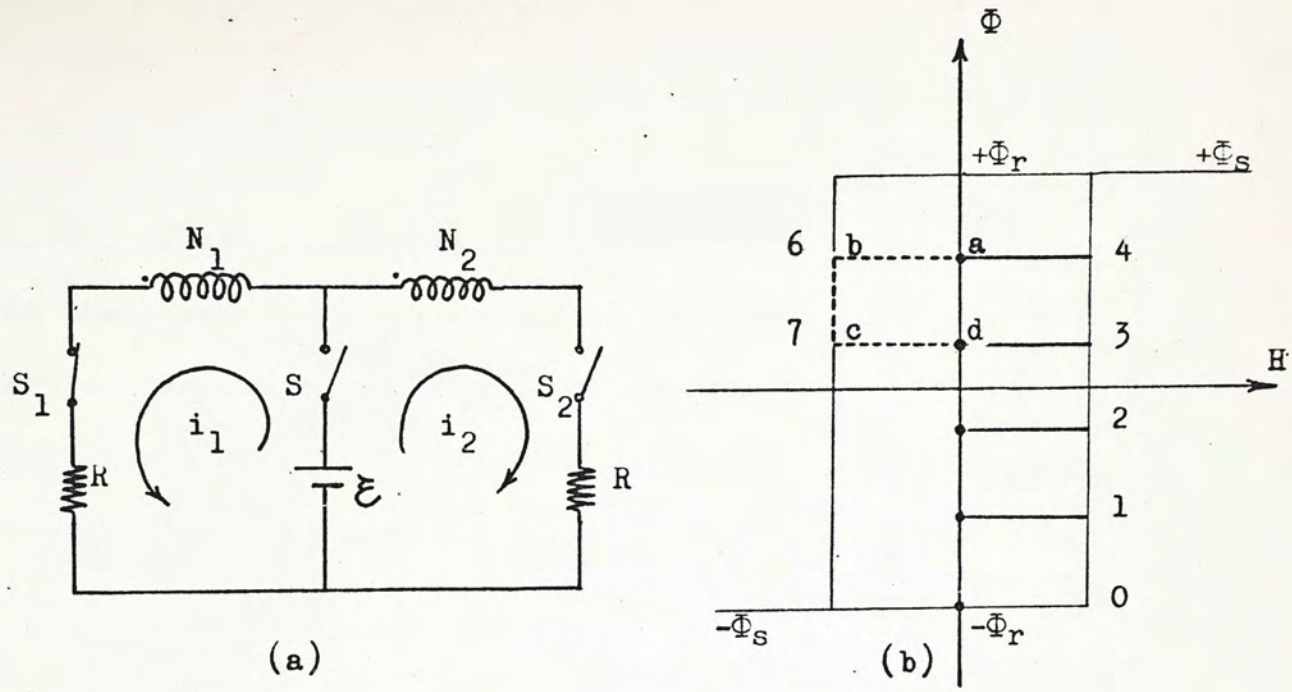


Fig.3-1 (a) Simplified circuit for the magnetic counter of Fig.2-2

(b) Change of flux level in the hysteresis loop

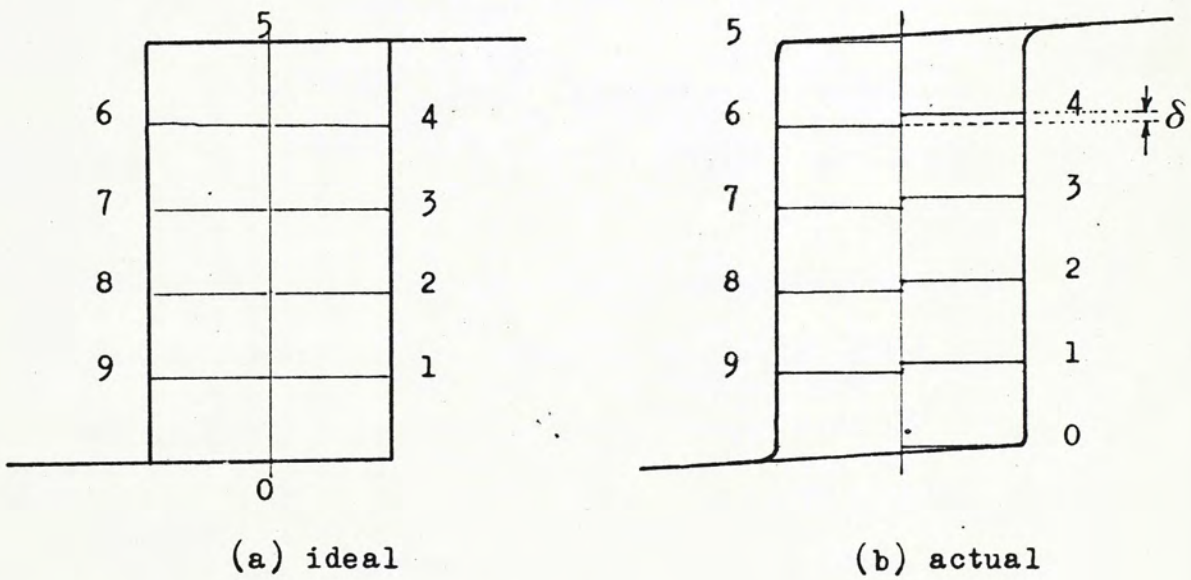


Fig.3-2 Change of flux level in response to number of pulses

3.2 Problem of non-linear magnetic switching

The phenomenon of linear magnetic switching described in the last section depends on the degree of squareness of the magnetic core which has a great affect to the reversible counts. A rectangular core is said ideal if the ratio B_r/B_s is unity. However, the present values readily attainable are in the range 0.90 to 0.96.

Consider the flux pattern of a Permally F core (B_r/B_s=13KGs/14KGs =92.9%) shown in Fig.3-3. It is found that :

$$\Delta\Phi_{tot}(1)=\Delta\Phi_{tot}(2)=1.18\times10^{-5} \text{ weber}$$

but $\Delta\Phi_{fly}(1)=0.20\times10^{-5}$ weber

while $\Delta\Phi_{fly}(2)=0.15\times10^{-5}$ weber

so $\Delta\Phi_{eff}(1)=\Delta\Phi_{tot}(1)-\Delta\Phi_{fly}(1)=0.98\times10^{-5}$ weber

but $\Delta\Phi_{eff}(2)=\Delta\Phi_{tot}(2)-\Delta\Phi_{fly}(2)=1.03\times10^{-5}$ weber

Because $\Delta\Phi_{eff}(1) \neq \Delta\Phi_{eff}(2)$, the reversible count becomes difficult. As already noted by Rozenblat and Fedin[12], the main shortcoming of the usual magnetic counter is the nonlinear dependence of flux on n, especially if ferrite transfluxors are used as counter core. Although many methods for compensating this nonlinearity have been proposed[5,9,12], they are too complicate to put into practice. Here, we prefer to choose a core of higher degree of squareness, Permalloy G core which has B_r/B_s = 95% for simplicity.

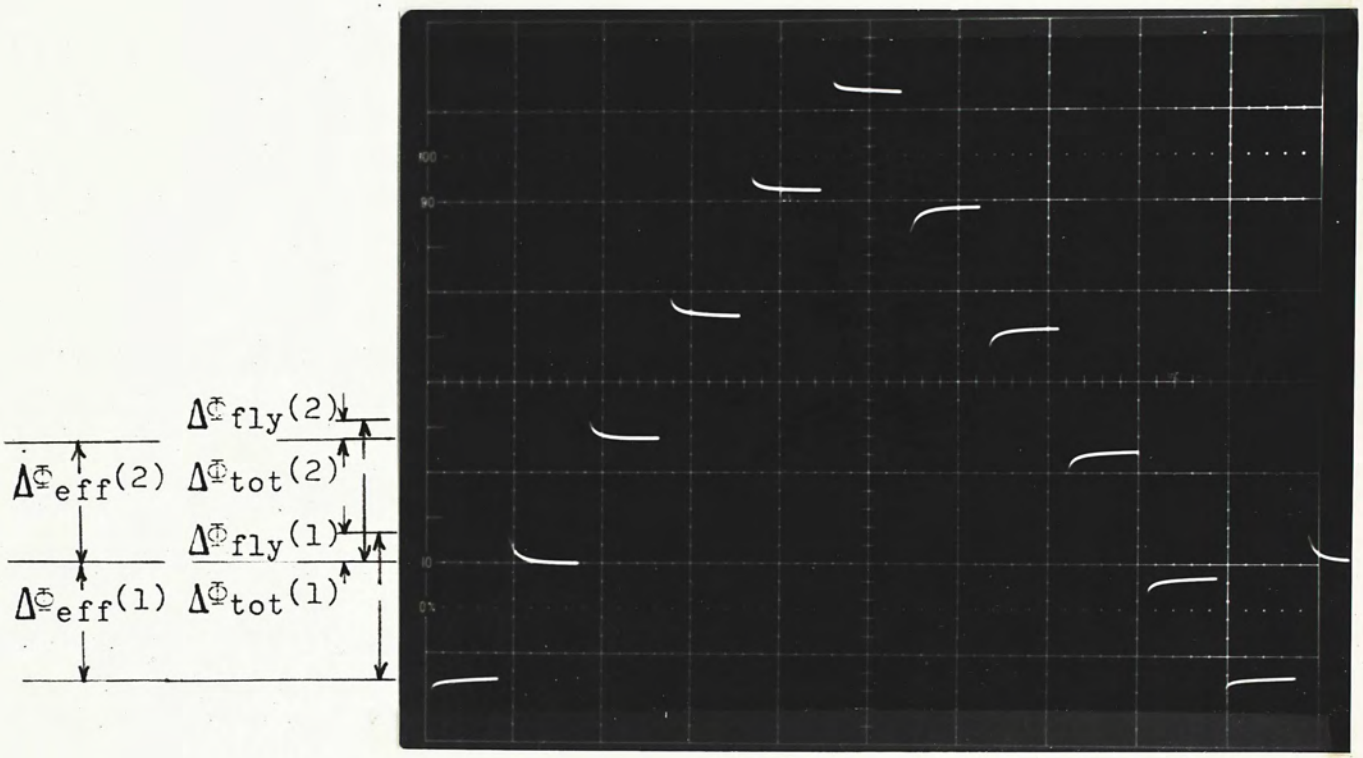


Fig.3-3 Flux pattern of Permalloy F core

Vertical : 0.75×10^{-5} weber/DIV

Horizontal : 10mS/DIV

3.3 Circuit realization - a single stage reversible magnetic counter

A single stage reversible magnetic counter is given in Fig.3-4. The circuit has the following features :

(1) Reset S capable to clear the content of the storage in the core and reset the transistor flip-flop (Q_1 and Q_2),

(2) T input a pulse with sharp falling edge applied to the 'T' terminal will change the 'circuit state',

(3) Output a pulse (width$\cong C(R_1 /\!/ R_2)$) will be delivered at the output terminal when the counter count from 9 to 0.

In order to count pulses with arbitrary waveform, a pulse-forming circuit (PF) must be associated with the counter itself. It is placed in front of the input of transistor Q. The PF which generates approprite rectangular pulses with preset volt-time integral consists mainly a monostable multivibrator. In order to obtain larger operating temperature range, the magnetic blocking oscillator is preferable, but in the research, semiconductor circuit is chosen because of its high speed and more rectangular output waveform.

The counter together with the PF will be symbolized by Fig.3-5 henceforth.

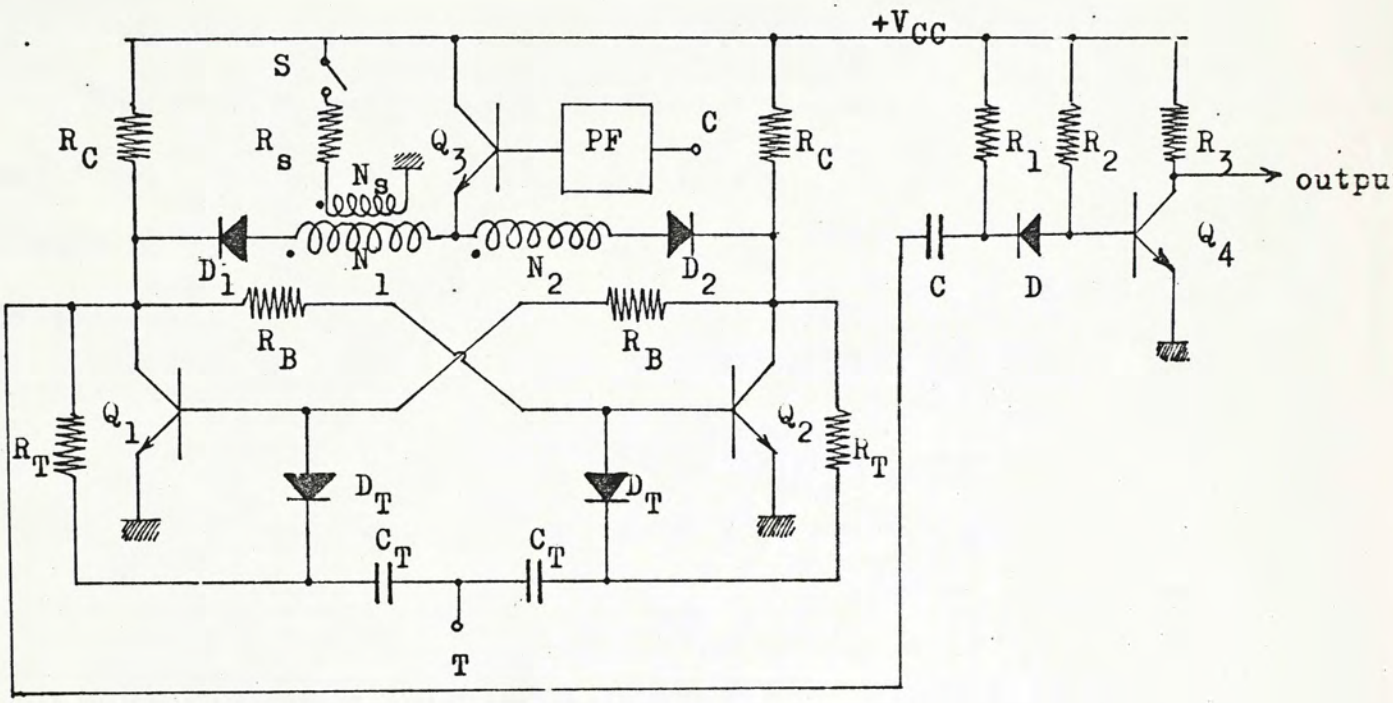


Fig.3-4 A single stage reversible magnetic counter

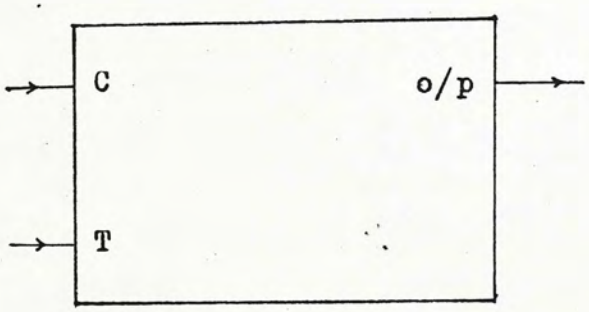


Fig.3-5 Symbolic diagram for the reversible counter shown in Fig.3-4 (including the PF)

IV. Read Out Method

The readout method is a remarkable engineering problem for multilevel storage in the magnetic core. In this chapter, a short review of the binary readout method is given and the difficulties of extending the idea to multilevel storage is discussed. A new digital readout method is then formulated and how to implement it is described.

4.1 Readout concept of binary system

The usual readout for the binary system is accomplished by applying a rectangular current pulse to the input winding of the core in the '0' direction. If the core is in the '1' state, the current will reverse the flux direction, and the resulting flux change will induce a voltage in the output winding. If the core is already in the '0' state, the current will only cause a small flux change, from Φ_r to Φ_s, and then back to Φ_r as the current falls back to zero. By discriminating the sense-out voltage, the storage of '1' and '0' is distinguished. Fig.4-1 shows a sketch of voltage waveform on the output winding. This output voltage is proportional to the rate of flux change. Actually, the distinction between the '1' voltage and the '0' voltage need not be made on the basis of amplitude alone, but to use a 'strobing' sensing amplifier which can be gated ON for only a short interval at the time when the '1' voltage reaches its peak and when the '0' voltage is falling. By means of the strobing technique, it is possible to

achieve a 10:1 amplitude discrimination between 1's and 0's that differ in peak amplitudes by only 3:1 or 4:1[19]. However, the information stored in the core will be destroyed by the reading excitation. In order to restore the information, it is in common practice to reverse the read current (i.e. drive in the '1' direction) after a readout of '1'. When the cores are arranged in two dimensional form, where the cores located at the same x or y coordinate are linked by a x or y selection winding respectively, the restore cycle is usually accomplished by reversing the x and y current[20,21]. Unfortunately, the core stores '0' originally will go to the '1' state after that restore cycle. To prevent this undesired switching, the Z (inhibit) winding which links all the cores in the core plane is introduced. During the restore cycle, the Z winding is driven by a half switching current in such a direction to oppose the switching if there is a '0' obtained in the previous read cycle.

In order to increase the operating speed of normal memories, the mentioned readout method which requires an additional restore cycle is not satisfactory and various non-destructive readout methods have been proposed[22-30], namely; make use of the small aperture of transfluxor[22,23], disturbing readout[24], readout by radio frequency[25], readout by quadrature fields[26], the use of BIAX [27,28], readout with pulses of short duration[29,30] and the fixed storages in which the contents cannot be altered electrically but to perform the mechanical alterations[22]. However, the simplest methods that have been developed are not nearly so simple as one might wish, and N.R.Scott pointed out that the problem of non-destructive readout has proved to be very thorny[31].

4.2 Multilevel storage readout

4.2.1 Analogy readout

The straight forward readout method following that for the binary system is to discriminated the amplitudes of the sense voltage during the reset of the core to initial saturation from various flux levels. Using Fig.4-1 as a guideline, the voltages appearing on the sense winding for various storage, when the core is being read, may be sketched as shown in Fig.4-2. In principle, a sense amplifier with certain strobing technique may give a linear output voltage proportional to the numbers stored, by means of which the stored information is detected.

However, there are several shortcomings in this method :

(a) There is difficulty in distinction of the voltage amplitudes between the one and its neighbourhood, especially when they are affected by some other factors such as noise, uneven winding distribution, temperature variation etc. .

(b) The readout is destructive, unless a restore cycle can immediately follow the read cycle so as to restore the number in the core. This method, however, has been found much more difficult than that used in the binary system.

(c) The readout method may be applicable only for the flux increment in a way as shown in Fig.2-1. But for the change of flux stepwise in up and down direction as shown in Fig.2-4, the method is not suitable, because the flux levels between a number A and its complement 2n-A is so close (differ by δ) that they are hard to be distinguished and so are the amplitude of the induced e.m.f. due to the change of these two flux levels.

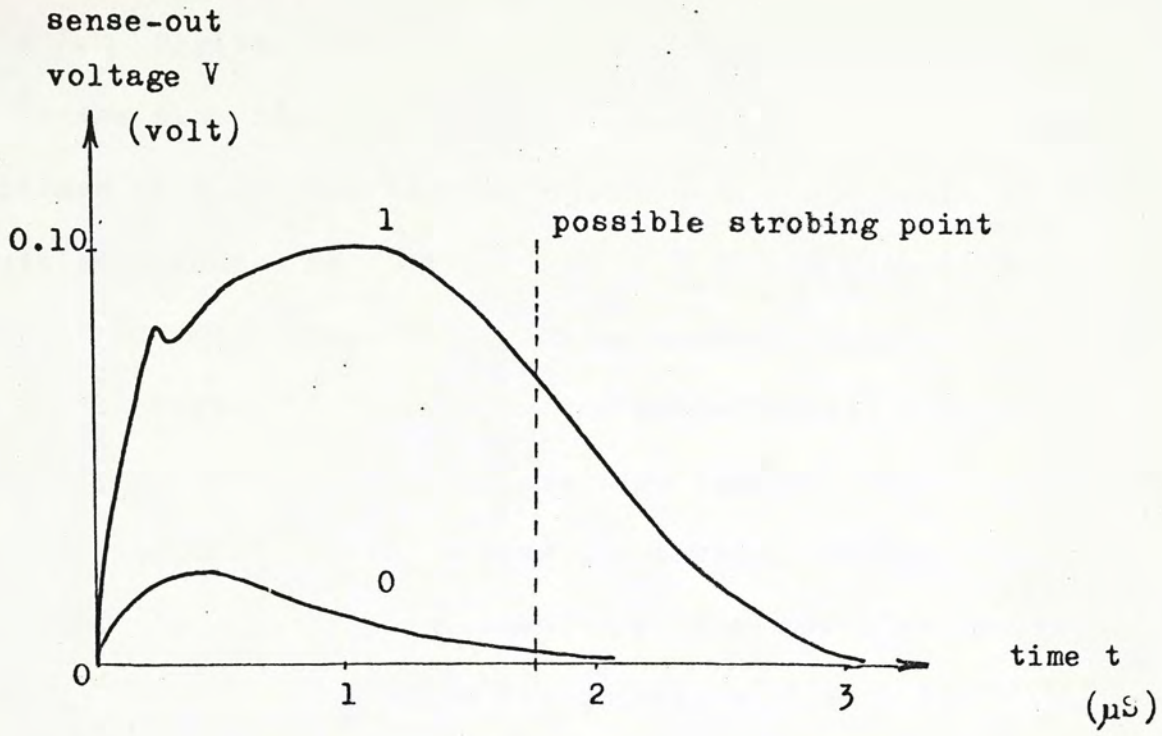


Fig.4-1 Sketch of the 0- and 1- voltage waveforms for binary storage

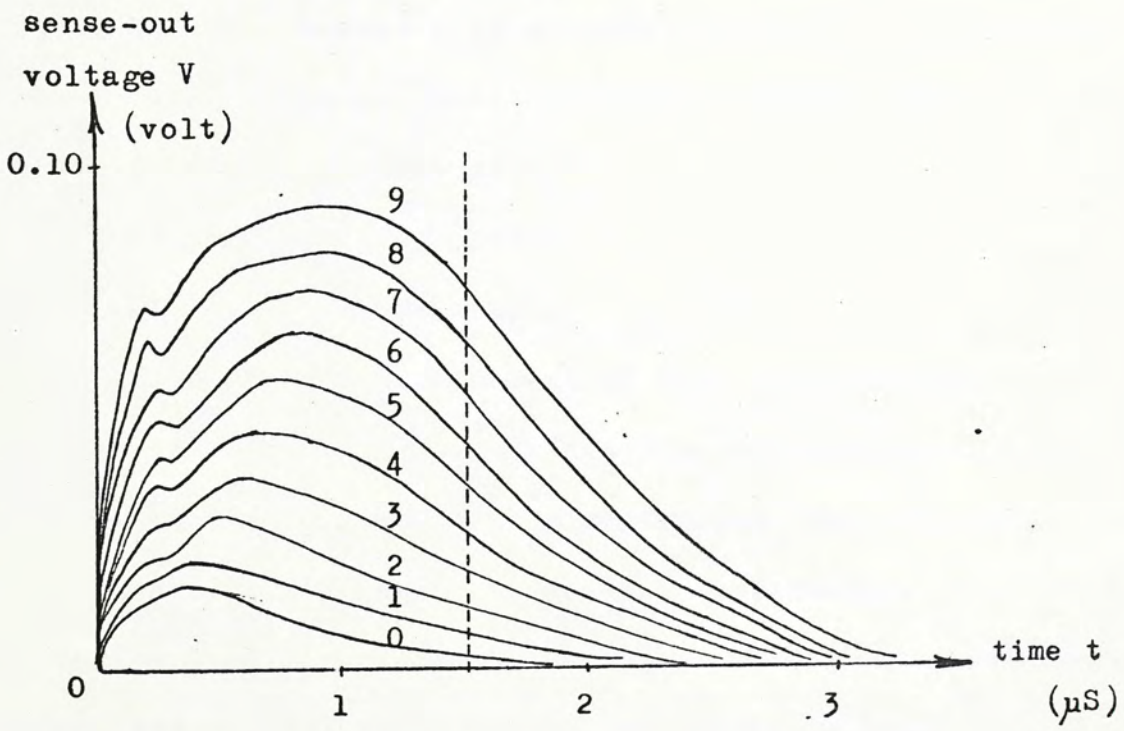


Fig.4-2 The readout voltage waveform for multilevel storage (Ten flux steps are assumed)

4.2.2 Digital readout

In the case that the core flux changes in steps in both directions (Fig.2-4), a digital readout may be obtained with a circuit arrangement as shown in Fig.4-3. A read signal starts a series of clocked pulses to drive the magnetic counter via an OR gate in the forward direction as the write pulses. This signal together with the clock pulses are also fed to a controllable AND gate, the output of which is used for digital display. When the storage of the counter is cleared, i.e. the core flux returns to '0' (Fig.2-4), an output from the counter will stop the clock pulse and the controllable AND gate. With such an arrangement, it can be noted the readout is a complement of the stored number. For instance, suppose the counter core has a storage capacity of 2n pulses (cf. Fig.2-4) and a number A is already written in. The required numbers of read pulses to reset the core is obviously equal to 2n-A which is the complement of A.

4.2.3 Nondestructive readout

4.2.3.1 The principle

The readout arrangement of Fig.4-3 is useful when subtraction is to be performed by addition of complement. Nevertheless, the storage in the counter core is destructed. The following modified idea of 4.2.2 may provide a read-and-restore cycle to the core. Consider the Fig.4-4 which shows the counter core is in decimal operation. Assume that a number '4' has initially been written in. If an additional 10 pulses of same volt-time integral as the write pulse are applied to the core, the flux will change around the hysteresis loop as indicated by the arrow as shown in Fig.4-4.

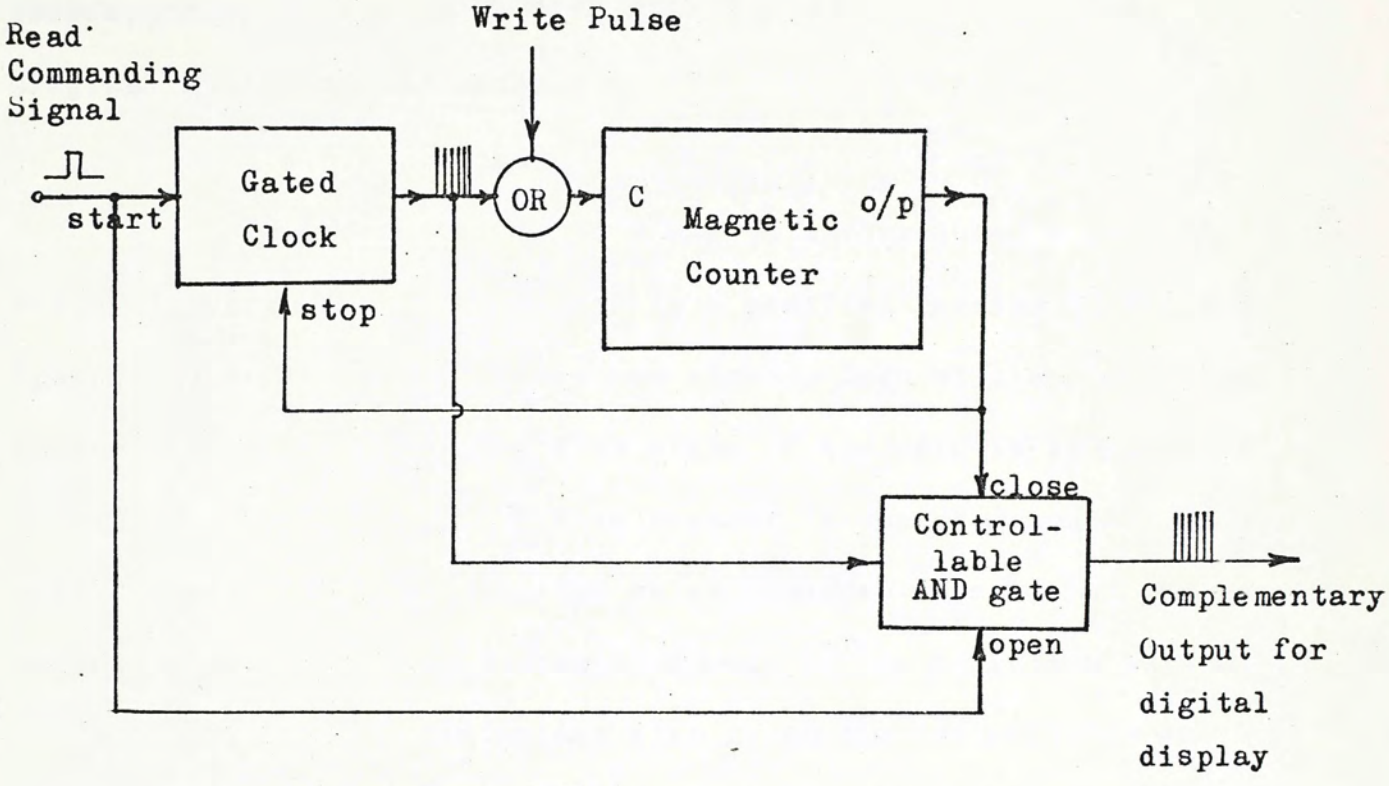


Fig.4-3 Digital complementary readout arrangement

At the end of the 10^{th} pulse, a flux remanence will be obtained corresponding to the point '4'. Thus it can be seen that the original state '4' is restored.

4.2.3.2 Schematic layout

In order to implement the foregoing idea, a schematic set up is shown in Fig.4-5 which is a modified version of Fig.4-3. Again, assume that the counter has already been written in by four pulses. In other words, the flux state of the core is at point '4' (Fig.4-4). In order to read this content, a read commanding signal starts the read pulse generator which provides a series of 10 read pulses to drive the counter continuously in the direction as the write pulses. These read pulses also go to the controllable AND gate G1. When the core flux returns to '0' after receiving six read pulses (Fig.4-4), an output from the counter will open the controllable AND gate G1 to let the rest of read pulses pass through. The trailing edge of the 10^{th} pulse will close the AND gate G1. Therefore the number of pulses that will come out from gate G1 is 10-6=4 , which is the number stored in the counter core. If the complementary readout is desired, an output may be obtained from the controllable gate G2. (The operation of this gate has already been discussed in 4.2.2.)

4.2.3.3 A complete readout system

Based on the foregoing discussions, a complete readout system for a four stages magnetic counter is constructed as shown in Fig.4-6. All stages in the counter are read simultaneously and are isolated from each other by gates during the readout operation. The readout system consists of the following parts :

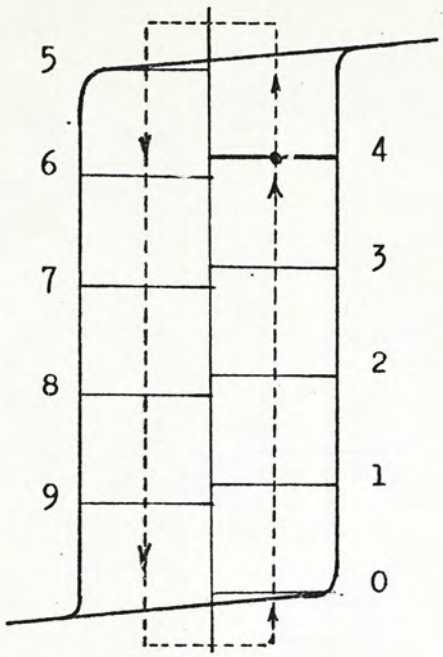


Fig.4-4 Illustration of the read and restore process

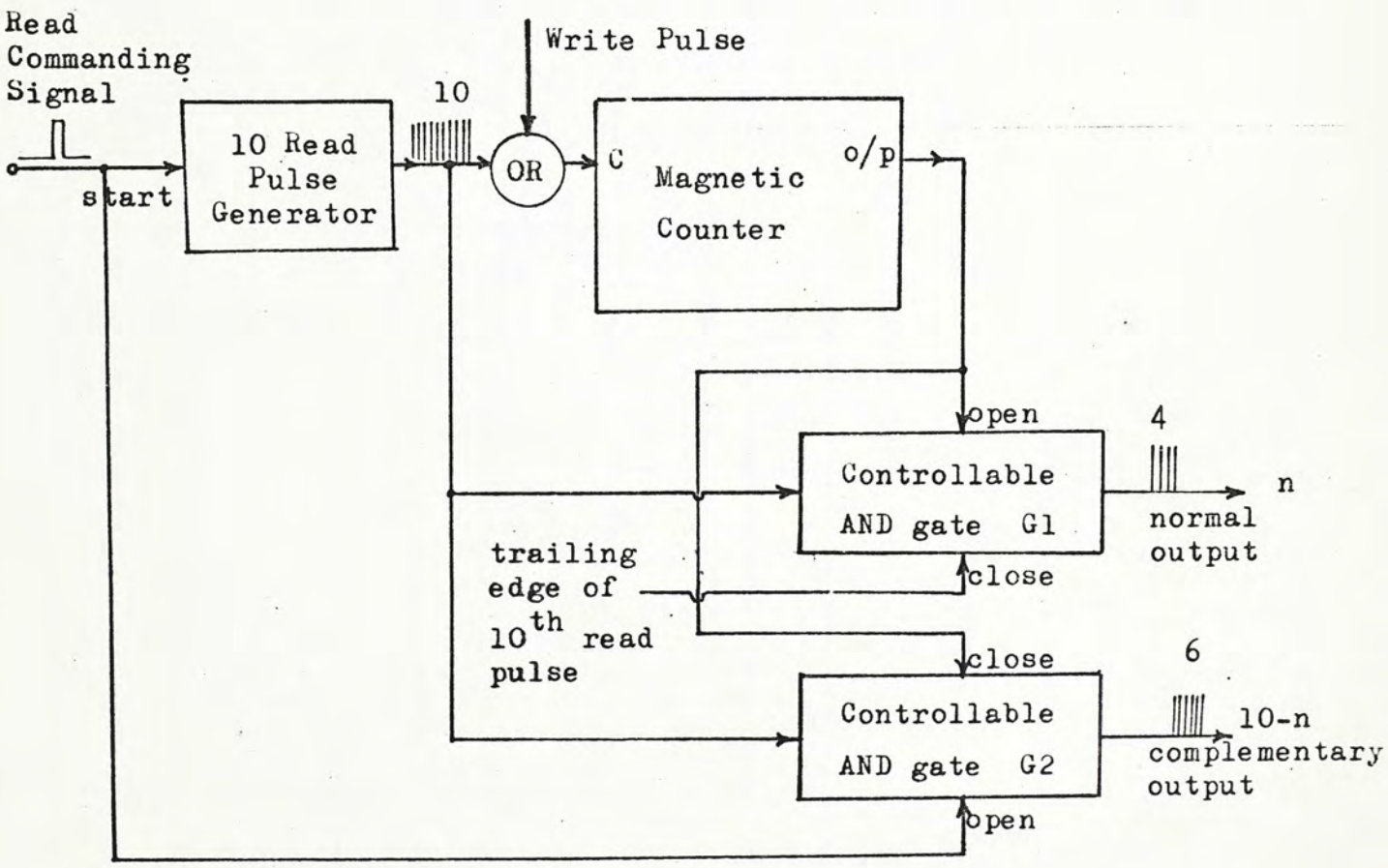


Fig.4-5 Schematic layout for the nondestructive readout

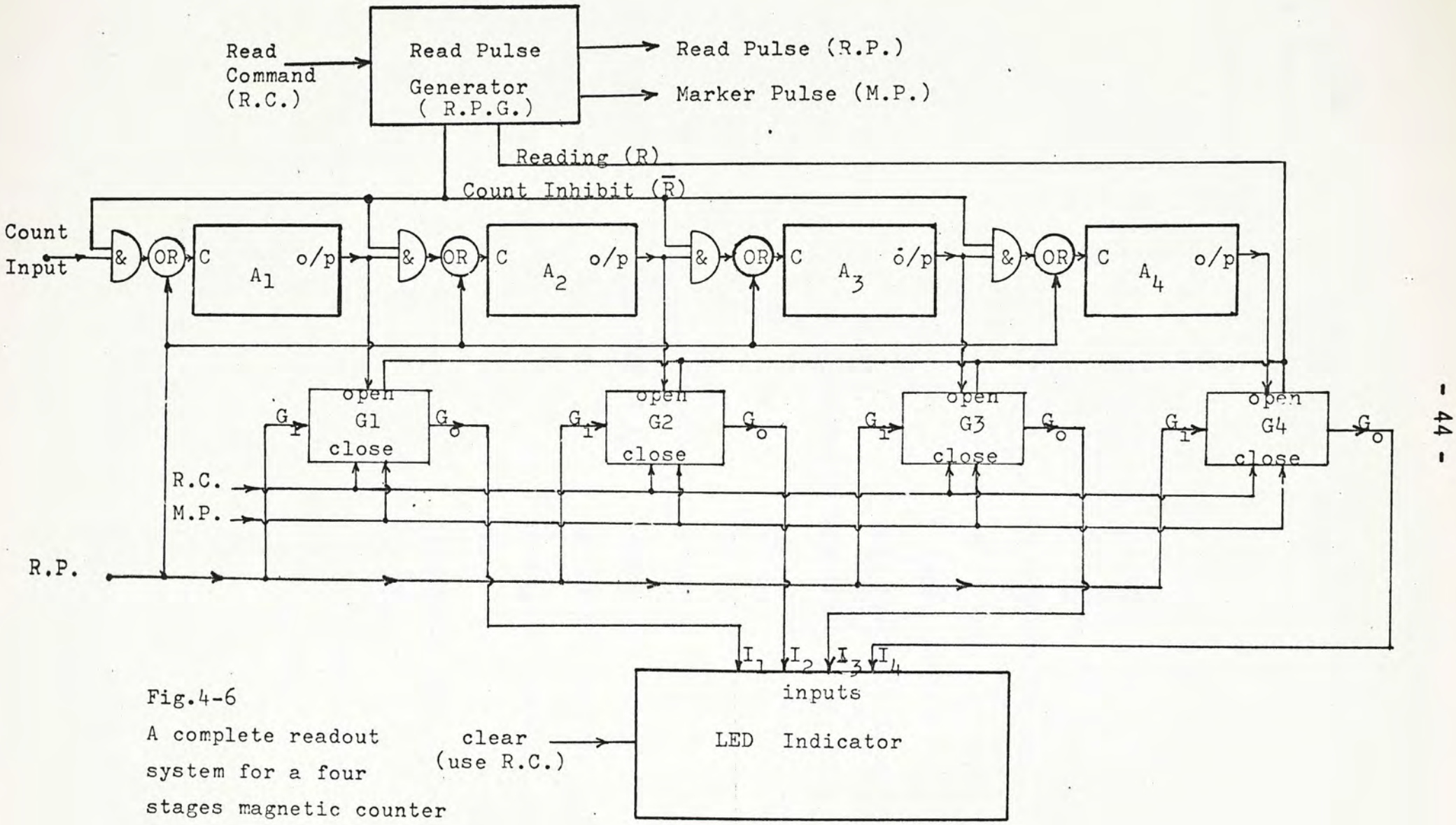


Fig.4-6
A complete readout system for a four stages magnetic counter

NAME	TERMINALS	FUNCTION
1. Read Pulse Generator (R.P.G.)	a. Read Command (R.C.)	initiate the R.P.G. by a read commanding signal.
	b. Read Pulse (R.P.)	generate a burst of 10 pulses once the R.P.G. is initiated.
	c. Marker Pulse (M.P.)	following the 10^{th} read pulse to indicate the end of read operation.
	d. Reading (R)	a logic level to indicate the read operation is going on.
	e. Count Inhibit ($\bar{R}$)	complement of R, to isolate the counting stages during the read operation.
2. Controllable AND gate (G1,G2,etc.)	a. Input (G_i) & Output (G_o)	pulses arriving at G_i can be transmitted to G_o only when the gate is opened.
	b. Open	gated input (AND) to open the gate.
	c. Close	dual inputs OR input to close the gate.
3. LED Indicator	a. Inputs (I_1,I_2,etc.)	to count the number of pulses from each controllable AND gate output (G_o) and display them numerically.
	b. Clear	to clear the counters in the Indicator for the preparation of next input.

The readout system operates in the steps given below :

1. READ COMMAND — start the readout operation,
   close all controllable AND gates,
   separate all counting stages,
   clear the content in the LED Indicator.
2. 10 READ PULSES — run all counting stages,
   open the controllable AND gate with the counter output,
   the gate output (G_o) drives the LED Indicator.
3. END OF READ — (R) connect all counting stages,
   (M.P.) close all controllable AND gates.

The Read Pulse Generator, controllable AND gate and the LED Indicator are shown in Fig.4-7, 4-8 and 4-9 respectively.

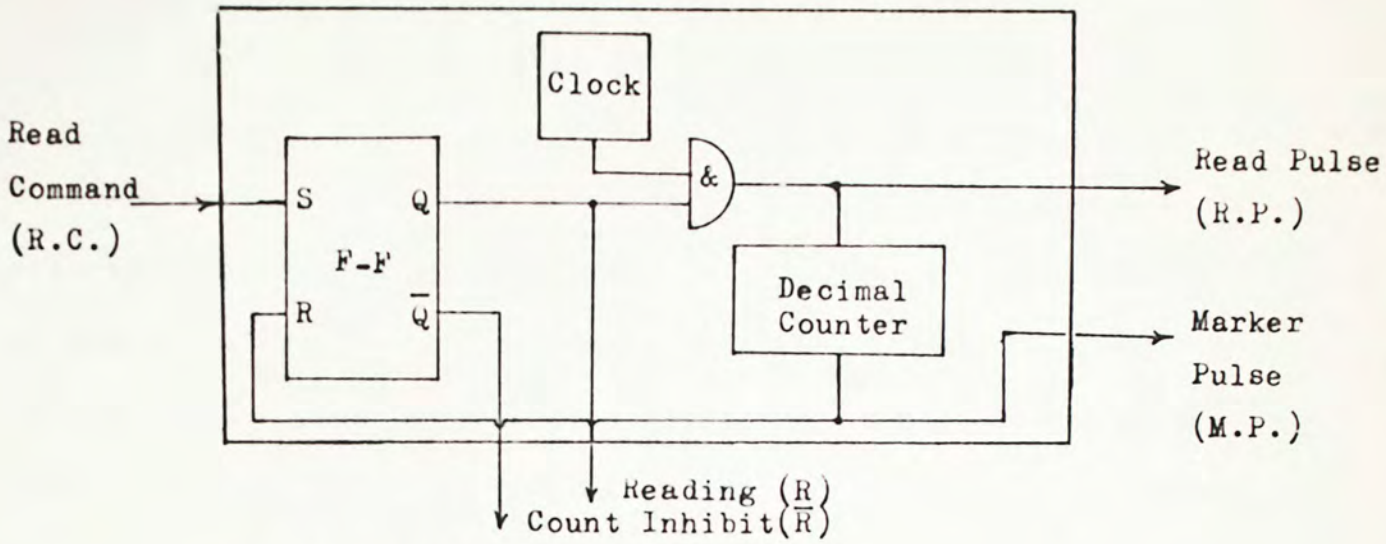


Fig.4-7 Read Pulse Generator

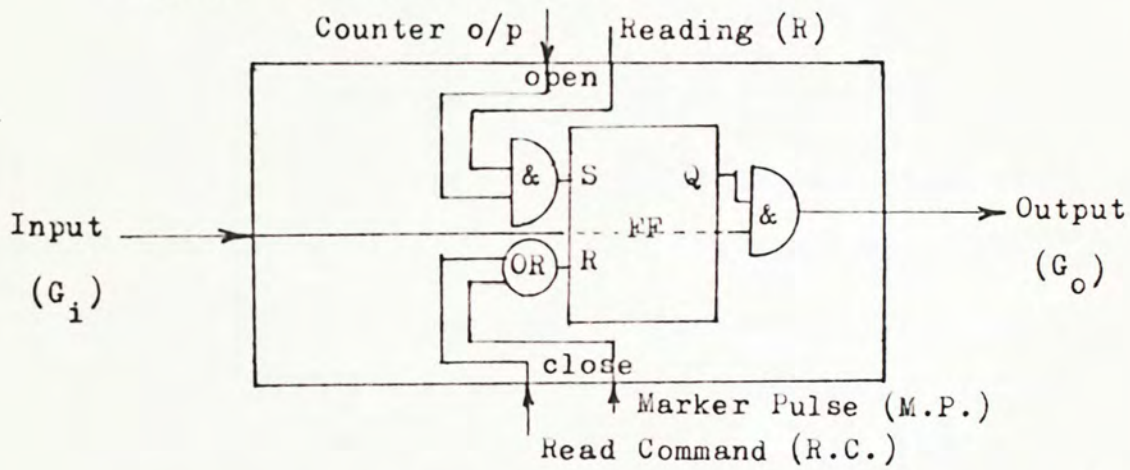
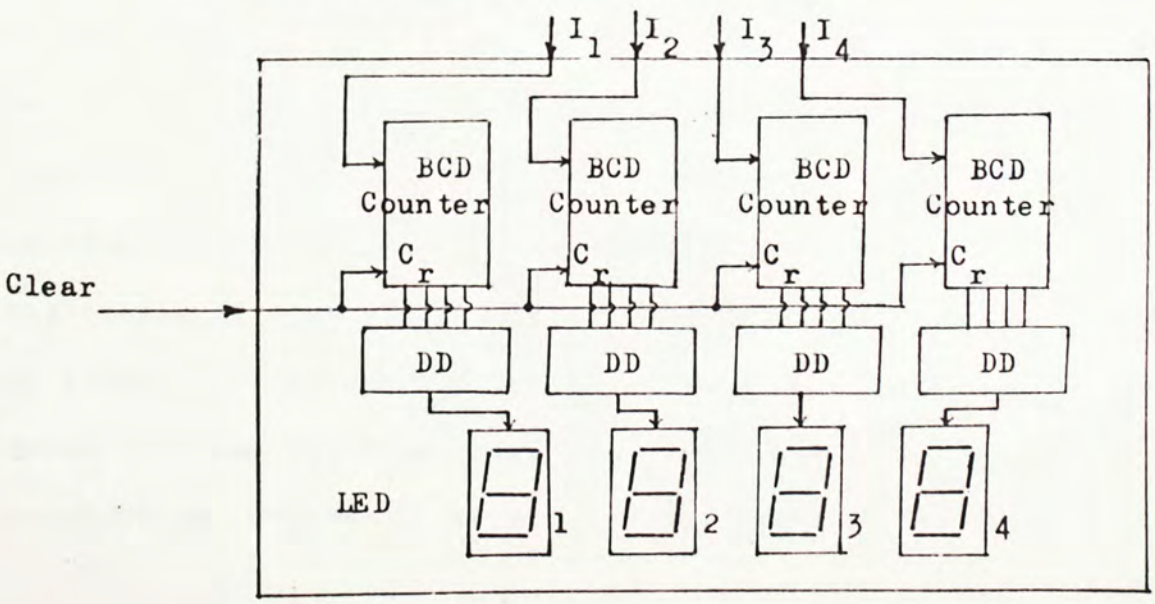


Fig.4-8 Controllable AND gate



DD : BCD to 7 segment Decoder/ Driver

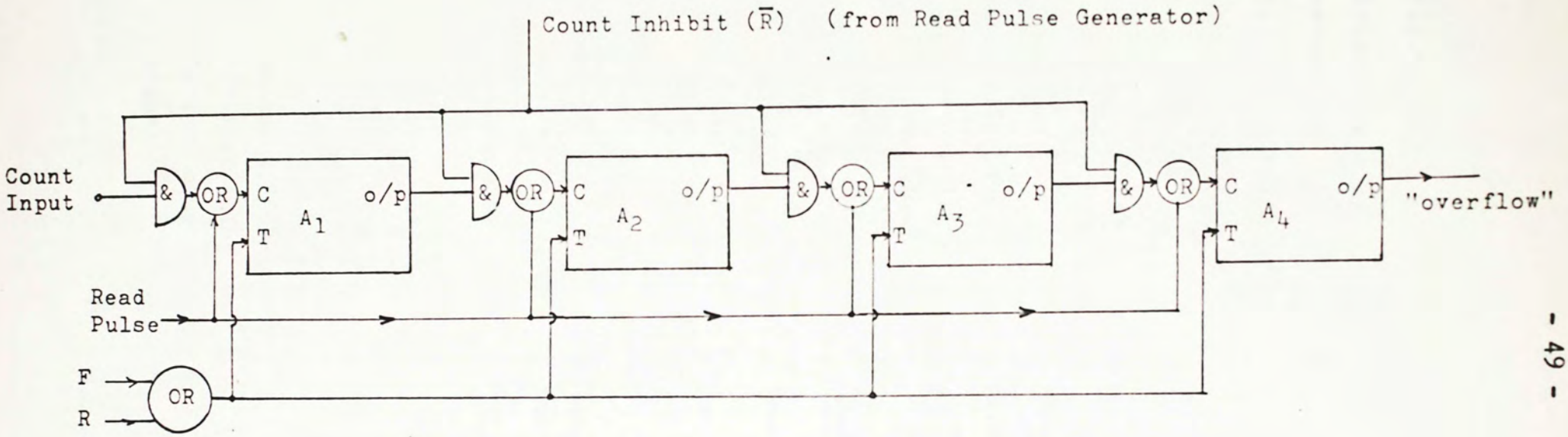
Fig.4-9 LED Indicator

V. Application

The circuit developed in the previous chapter is a basic component for building up systems. This chapter shows an example of how to interconnect four stages of such a circuit to form a reversible 4-digits decimal counter. In addition, the use of the circuit as registers for simple arithmatic operations is explained.

5.1 A four-stage reversible decimal counter

Using the symbol defined in Fig.3-5, a four-stage reversible counter is connected up as shown in Fig.5-1. Each stage has a cycle of operation for every 10 input pulses. In other words, each gives an output in response to 10 pulses at its input. The output of a stage is connected to the input terminal C of the next stage via an AND gate in series with an OR gate (the operation of each stage is already given in Chapter III). Let us define the output from a stage after a cycle of operation to be a "carry" since it is carried forward to the next stage in succession. The reverse operation of the counter can now be explained as follows : Taking an example for illustration, assume that the counter has initially registered 12 counts, i.e. '2' is indicated by stage A_1 and '1' by stage A_2 (Fig.5-1) and the corresponding flux states of the cores in these two stages are shown in Fig.5-2(a). It is now required to reverse the counts by 5 so that the final count is



F : forward counting signal

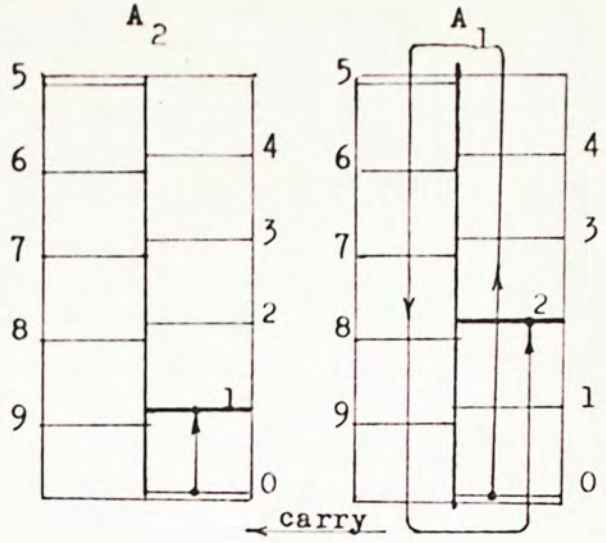
R : reverse counting signal

Fig.5-1 A four stages reversible counter

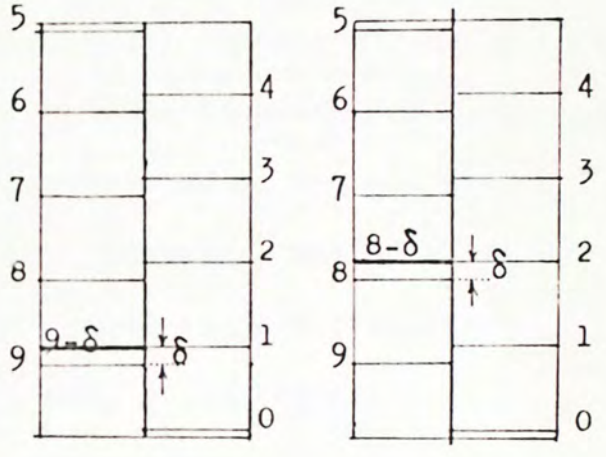
Fig.5-2

Flux state diagram for reversible count

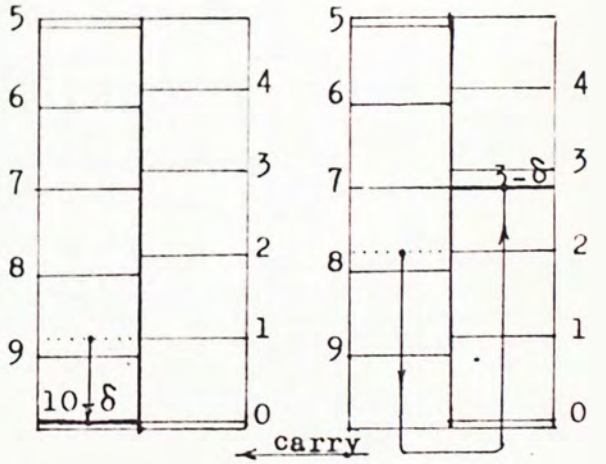
(a) storage of '12' (forward count)



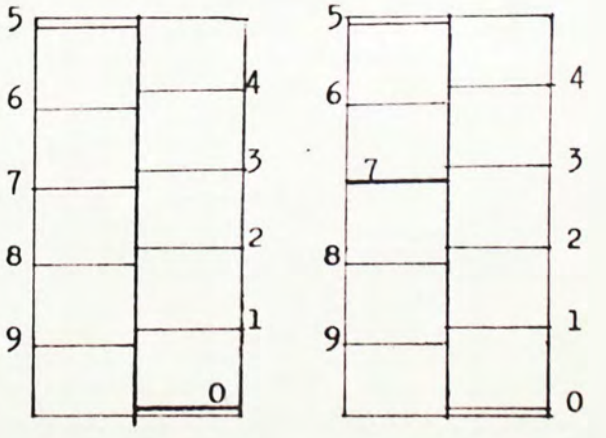
(b) change of flux state after applying the reverse counting signal



(c) change of flux state after the application of 5 write pulses



(d) change of flux state after applying the forward counting signal



12-5-7. The first step is to apply a reverse counting signal to the stages to alter their circuit states thus changing accordingly their core flux states to their complements, i.e. the flux level of A_1 changes from '2' to '8-δ', and A_2 changes from '1' to '9-δ' where δ is a small difference in flux remanence between a flux level and its complementary one (Fig.5-2b). Then 5 write pulses are applied to drive the counter continuously. This changes the core flux state in A_1 to '3-δ' and A_2 to '10-δ' (Fig.5-2c). Finally a forward counting signal is applied to the counter to make it ready for forward operation again. During this step, the flux state of A_1 becomes at level '7' and A_2 at '0' (Fig.5-2d). The whole procedure may be summarized by the following table if the small difference in flux remanence between a flux level and its complementary one, δ, is neglected.

Table 5-1

Procedure of reversible operation

control signal	counting stages	
	A_2	A_1
1. initial count is '12'	flux state at '1'	flux state at '2'
2. application of a reverse counting signal	flux state is changed to its complement (10-1)	flux state is changed to its complement (10-2)
3. application of 5 write pulses	no change	flux state is changed to (10-2)+5=8+5=13
4. no signal is applied	(10-1) + '1'	$\because$ 13>10, a "carry" '1' is delivered to A_2 $\therefore$ 13-10 = 3
5. application of a forward counting signal	flux state is changed to its complement 10-[(10-1)+1] = 0	flux state is changed to its complement 10-3 = 7
THE REVERSE-COUNT OPERATION IS COMPLETED		

5.2 Arithmatic operation

A bank of the decimal counters can be treated as a register, and with suitable control procedure, arithmatic operations such as: addition, subtraction, multiplication and division can be performed. The idea and procedure of each kind of the operation will be discussed below.

5.2.1 Addition and subtraction

5.2.1.1 Basic idea

In performing addition (or subtraction) of two numbers, the least significant digits are first added (or subtracted), then if there is any carry (or borrow), it is added to (or subtracted from) the sum (or difference) of the next more significant digits. The procedure is carried up to the most significant digits. For example : 2571+1234=3805 and 2571-1234=1337 is carried out in four steps.

5.2.1.2 Realization

This kind of operation may be performed by connecting up several reversible counters of Fig.5-1 in parallel as the example shown in Fig.5-3. Each stage in register B requires a series of 10 read pulses to complete the read-and-restore cycle. Assume two numbers (e.g. three digits) are stored in registers A and B respectively, and the content in register B is to be added to that in register A. This may be done by reading out the content of each stage in register B and feeding it one by one to the corresponding parallel stage in register A; the addition is thus accomplished. In this case, register A is used as an accumulator.

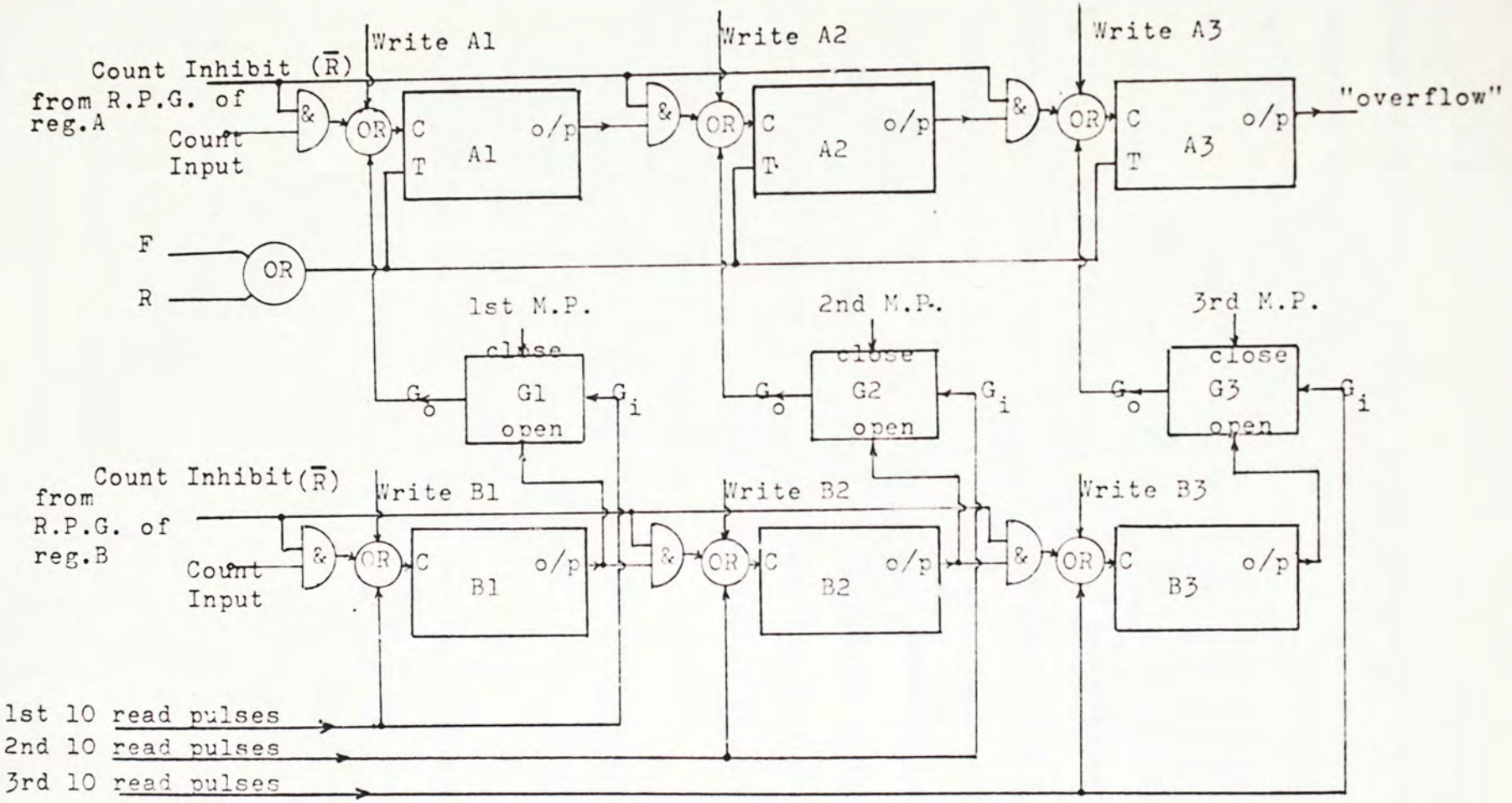


Fig.5-3 An example circuit for addition and subtraction of two decimal numbers

When the subtraction (A-B) is desired, the content in each stage of register A must first be changed to its complement and then carrying out a parallel addition as above. Finally a manipulation is performed in a way as the reversible counter illustrated in Sec.5.1 in order to obtain the answer.

The above method, however, is inefficient, for it requires a long time to transfer the data from one register to the other. If there are m stages in the register, it requires m series of 10 read pulses to finish the operation since the information is transferred digit by digit. This is undesirable in machinary calculation, particularly when two large numbers are involved in the operation.

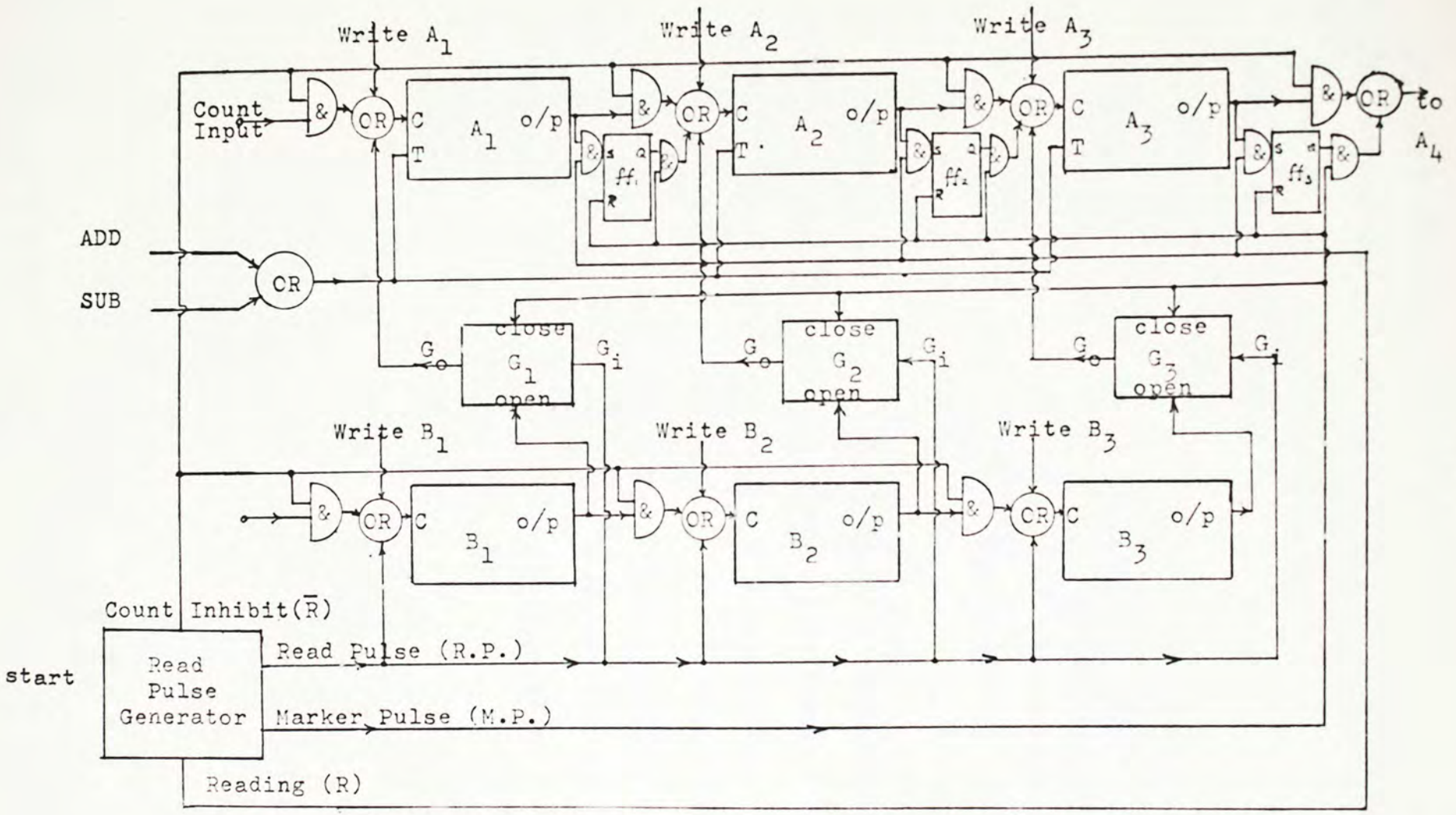
An alternative circuit that may save a lot of computation time is shown in Fig.5-4. The operation of this circuit is illustrated as follows :

(1) The content of each stage in register B is readout simultaneously by a burst of 10 read pulses and is fed to the corresponding stages in register A.

(2) During the reading process, sucessive stages in register A are separated from each other by the AND gates (cf. Fig.4-6) and the output from the stages (carry) is used to set a memory element (e.g. flip-flop, ff).

(3) The marker pulse following the 10^{th} read pulse will reset the memory element and at the same time generate a "carry" to the next stage.

Using this method, a computation time of the order of 11 read pulses is required, regardless of the number of stages in the register. Also, only one read pulse generator is required.



* ADD is similar to F(the forward counting signal) and SUB to R (the reverse counting signal)

Fig.5-4 Parallel addition and subtraction of two decimal numbers by two steps method

The features of the circuit may be summarized below.

(1) The corresponding digits of addend and augend are added simultaneously and the carry (if any) is stored in a binary storage element instead of propagated into the next stage, and

(2) a carry pulse is generated and propagated after the parallel transfer of information by a "marker pulse".

Subtraction can be processed in a similar way as that for addition.

5.2.2 Multiplication

5.2.2.1 Basic idea

Multiplication is carried out by successive addition. For example : 3x5 can be treated as 3+3+3+3+3 (5 times) which is equal to 15. For a decimal number multiplied by a single digit, such as : 1234 x5, the method is exactly the same, i.e. 1234+1234+1234+1234+1234 = 6170. But for multiplication of two decimal numbers (more than 1 digit), the computation must be carried out in terms of single digit multiplication . For example : 1234 x 246 is carried out as :

(1) 1234 x 6 =

```
  1234
  1234
  1234
  1234
  1234
+ 1234
  7404
```

1st partial product, to register--------7404

(2) 1234 x 40 =

```
  12340
  12340
  12340
+ 12340
  49360
```

2nd partial product, to register-------49360

(3) 1234 x 200 =

```
  123400
+ 123400
  246800
```

3rd partial product, to register------246800

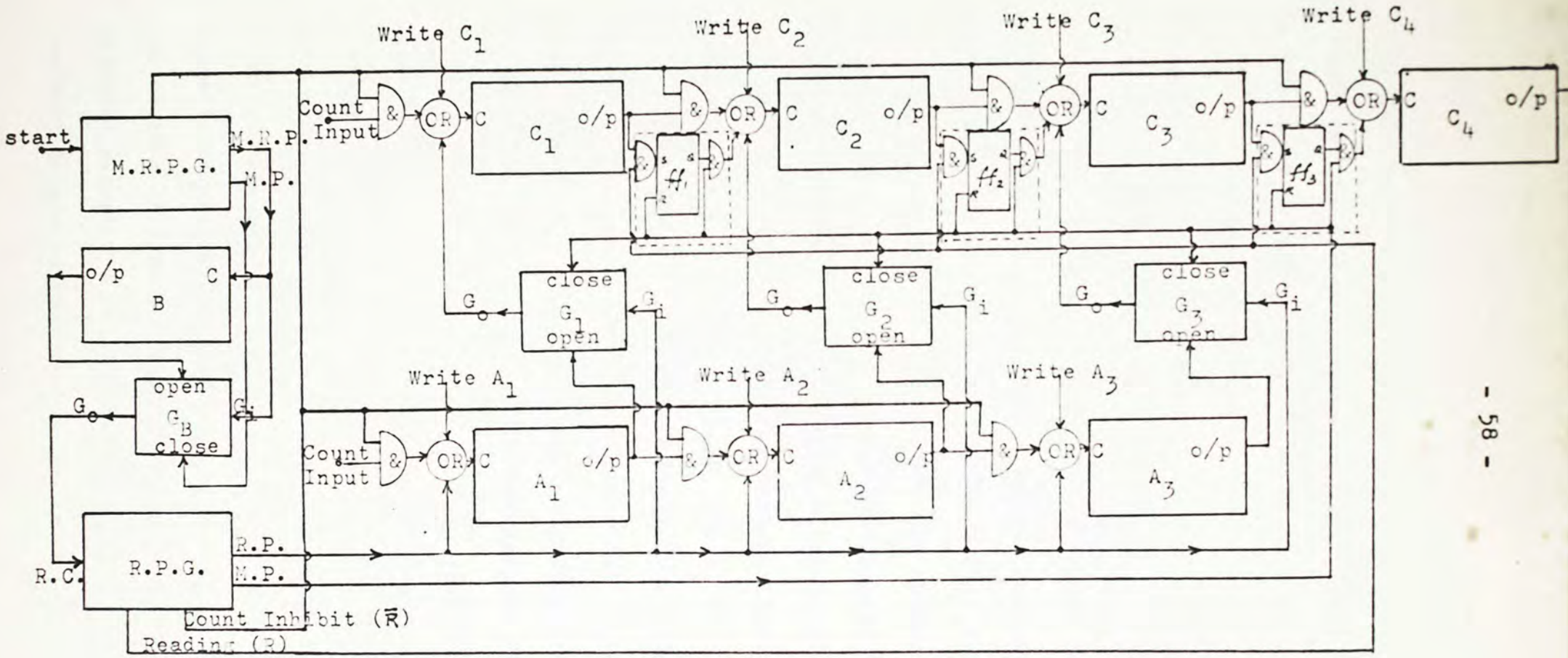
(4) the total product will then be the sum of these partial products.

```
   7404
  49360
+ 246800
Product ------ 303564
```

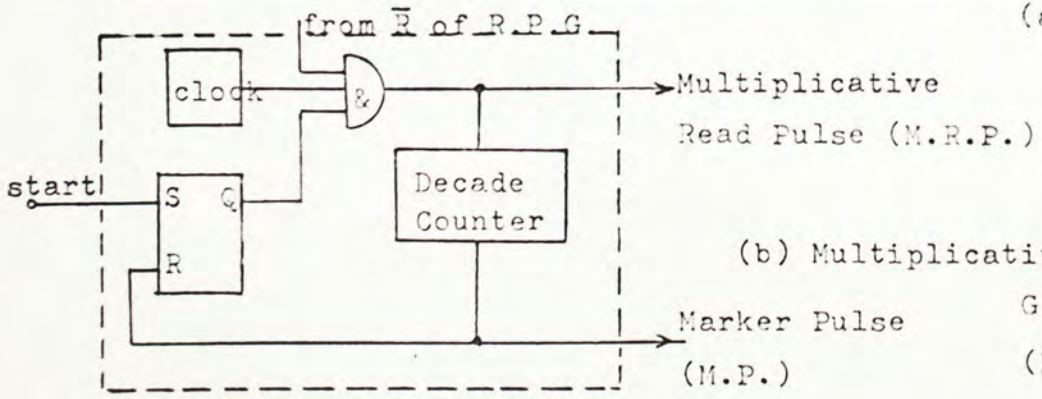
5.2.2.2 Realization

For simplicity, consider first the multiplication of a decimal number with a single digit. Utilizing the addition circuit shown in Fig.5-4, a multiplication circuit is connected up as shown in Fig.5-5(a). Register B is used to store the multiplier. Register A is used to memorize the multiplicand. Register C is used to register the product. When performing the calculation, a burst of 10 read pulses is first applied to register B by the "multiplicative read pulse generator"(M.R.P.G.). These pulses will read out the content in register B and transform it into a number of pulses. Each of these pulses will activate the "read pulse generator"(R.P.G.) (see Fig.4-7) which makes the content of register A transfer to register C. After each transfer, the "marker pulse"(M.P.) of R.P.G. will assist the overflow in any stage in register C to be carried forward to the next stage (detailed operation is already given in 5.2.1.2).

Now let us define the process of transferring once the content in register A to register C as the "transfer cycle". Since the content in register B determines the frequency of transfer of the content in register A to register C, the digital readout of register B must be regulated such that each digit will follow the "transfer cycle". This is accomplished by feeding the "count inhibit" ($\overline{R}$) signal back to the M.R.P.G. from the R.P.G. (Fig.4-7). This signal will disable or enable the AND gate inside the M.R.P.G. (Fig.5-5b) depending on the conditions of R.P.G. whether it is in operation or not.



(a) Multiplication of a decimal number with a single digit



(b) Multiplicative Read Pulse Generator (M.R.P.G.)

Fig.5-5 Multiplication by repeated addition (m digits x 1 digit, m=3 is arbitrary chosen)

Using this method, the multiplication time for a decimal number and a digit may vary from 10 clock pulses (if the multiplier is zero) up to 100 clock pulses (if the multiplier is nine).

For multiplication of two decimal numbers, each has m and n digits respectively (m for multiplicand, n for multiplier), the system layout for an arbitrary values m=4, n=2 is shown in Fig.5-6, in which register A stores the multiplicand, register B stores the multiplier and register C memorizes the product. To start the operation, the M.R.P.G. is initiated and register B is read digit by digit with the help of the shift register. For the assumed n=2, the shift register is preset to '1 0'. (For n digits multiplier, the shift register is preset to '1 $\overbrace{0\ 0\ \ldots\ 0}^{n-1}$'.) Suppose B_1 is to be read first, the number of times of parallel transfer of content from register A to C ($A_1 \rightarrow C_1$, $A_2 \rightarrow C_2$, etc.) via AND gates $\&_1$, $\&_3$, $\&_5$ and $\&_7$ is determined by the content in B_1. When the multiplication between the number in register A and that in B_1 is completed, the marker pulse (M.P.) from the M.R.P.G. will change the state of the shift register from '1 0' to '0 1'. This change produces two effects upon the system, (1) multiplication is to be performed between register A and B_2, (2) content transfer, via AND gates $\&_2$, $\&_4$, $\&_6$ and $\&_8$, is one digit shifted to the right of the corresponding stages, i.e. $A_1 \rightarrow C_2$, $A_2 \rightarrow C_3$, etc. (Fig.5-6). So the next 10 read pulses from the M.R.P.G. will input to B_2 and the number of times of parallel transfer of content from register A to C (one digit shift forward) is determined by the content of B_2. The partial product of the content in register A and that in B_2 is added to the previous one (between register A and B_1) with one digit shifted forward. The operation will terminate when each digit in register B (the multiplier) has

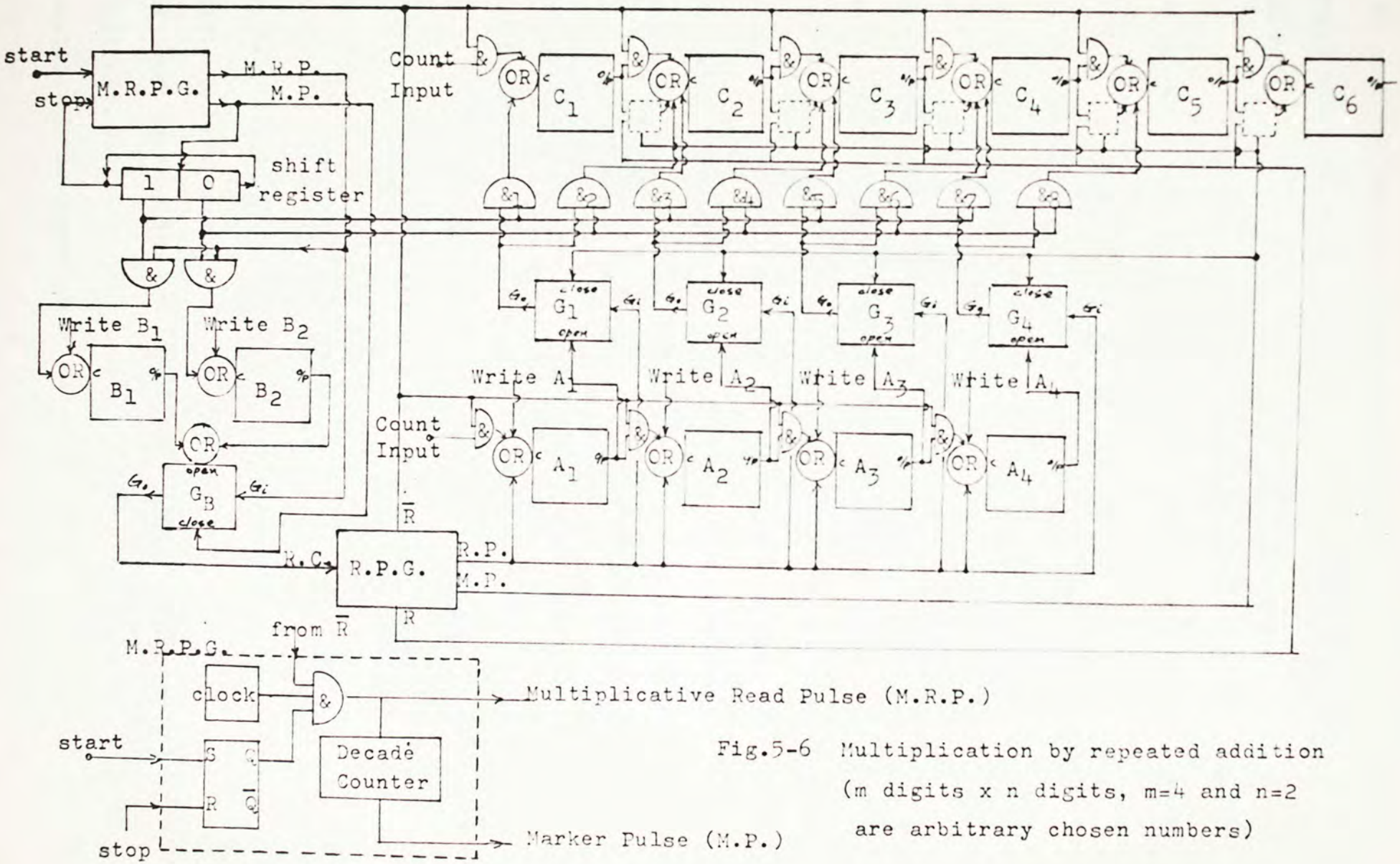


Fig.5-6 Multiplication by repeated addition
(m digits x n digits, m=4 and n=2
are arbitrary chosen numbers)

been read and the '1' in the shift register has resumed its original preset position which accordingly generates a "stop" signal for the M.K.P.G. .

The multiplication time for this layout will vary between 10n pulses (if the multiplier is zero) to 100n pulses (if the multiplier is 10^n-1).

5.2.3 Division

5.2.3.1 Basic idea

Similar to multiplication, which can be reduced to a series of additions, division can be reduced to a numbers of subtractions. As discussed by Gschwind[22], three kinds of division can be used, namely, division with test feature, restoring division and non-restoring division. The idea of "division with test feature" is straight forward, the divisor is subtracted from the dividend repeatedly until the difference is less than the divisor (which is the remainder). Then, the performed number of subtractions is the desired quotient. This method, however, requires an expensive comparator. In the method of "restoring division", with no comparator, the divisor is subtracted from the dividend repeatedly until a negative number results. The proper dividend is then restored by the addition of the divisor. The third method (non-restoring division), however, can save the restoring step by adding the divisor repeatedly to the negative, one digit shifted forward, dividend. The number of additions required to obtain a positive dividend is then the complement of the desired digit in the quotient. Following is a numerical example of 178÷111 for illustration of the procedure of these two methods.

restoring division

```
                178
1.        - 111 ----- 1
                67
2.        - 111 -----(2)
              - 44
3.        + 111 ----- 1
                67
4. shift
                670      1.0
5.        - 111 --- 1.1
                559
6.        - 111 --- 1.2
                448
7.        - 111 --- 1.3
                337
8.        - 111 --- 1.4
                226
9.        - 111 --- 1.5
                115
10.       - 111 --- 1.6
                  4
```

non-restoring division

```
                178
1.        - 111 ----- 1
                67
2.        - 111 ----- 2
              - 44
3. shift
               -440      2.0
4.        + 111 --- 1.9
               -329
5.        + 111 --- 1.8
               -218
6.        + 111 --- 1.7
               -107
7.        + 111 --- 1.6
                  4
```

It is noted[22] that the non-restoring division saves an average of 20% of operations than the restoring division. Thus, our realization will base on the former one. The flow chart for "non-restoring division" is shown in Fig.5-7.

5.2.3.2 Realization

For simplicity, assume that the dividend is not greater than ten times of the divisor (just as the illustrated example). Following the idea shown in Fig.5-7, the schematic layout for non-restoring division is shown in Fig.5-8. The steps of operation of the circuit is given as follows :

1. Division start signal --

(i) activiate the Division Read Pulse Generator (D.R.P.G.),

(ii) set the dividend register (reg.A) ready for subtraction and the quotient register (reg.C) ready for addition.

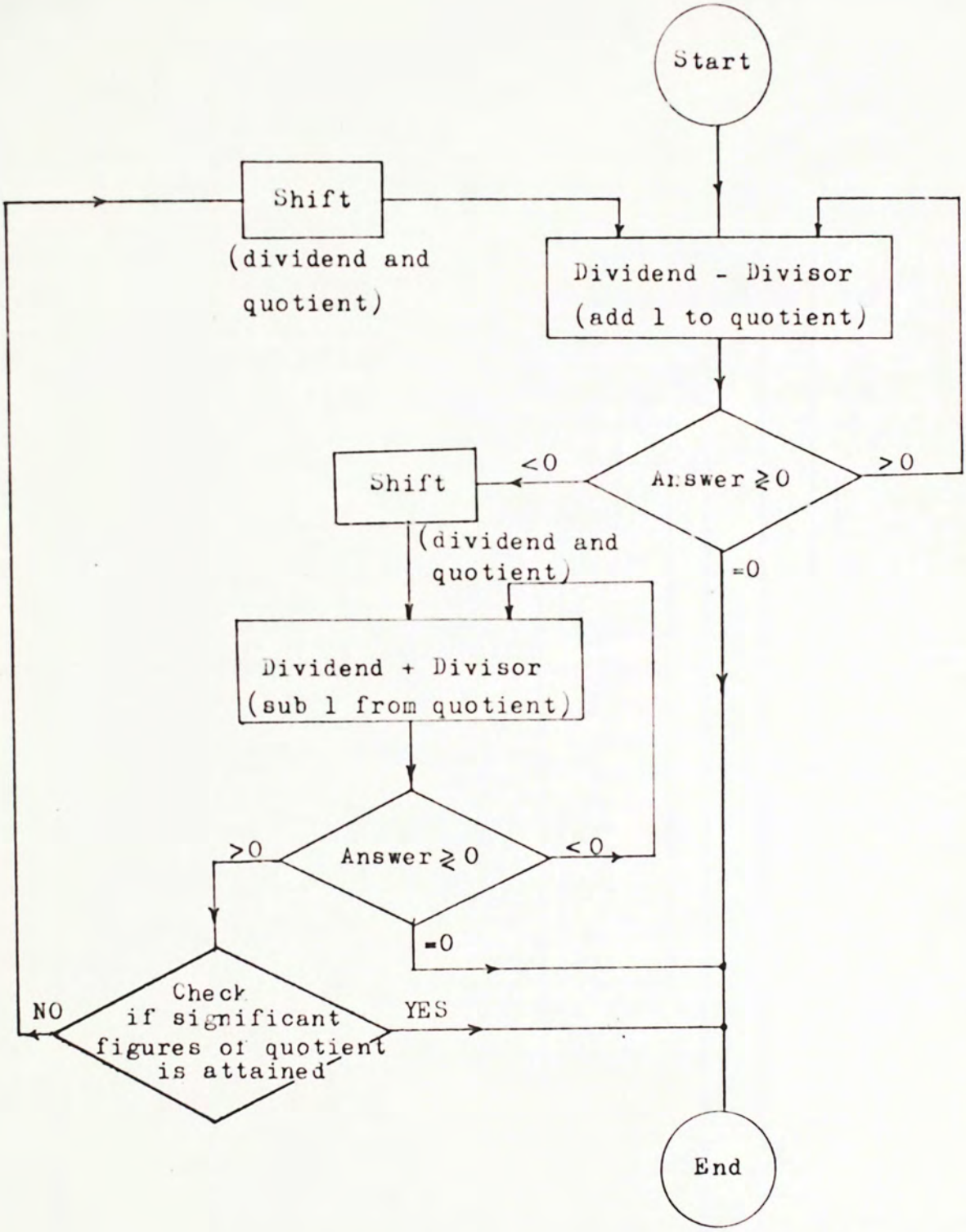


Fig.5-7 Flow chart for "non-restoring division"

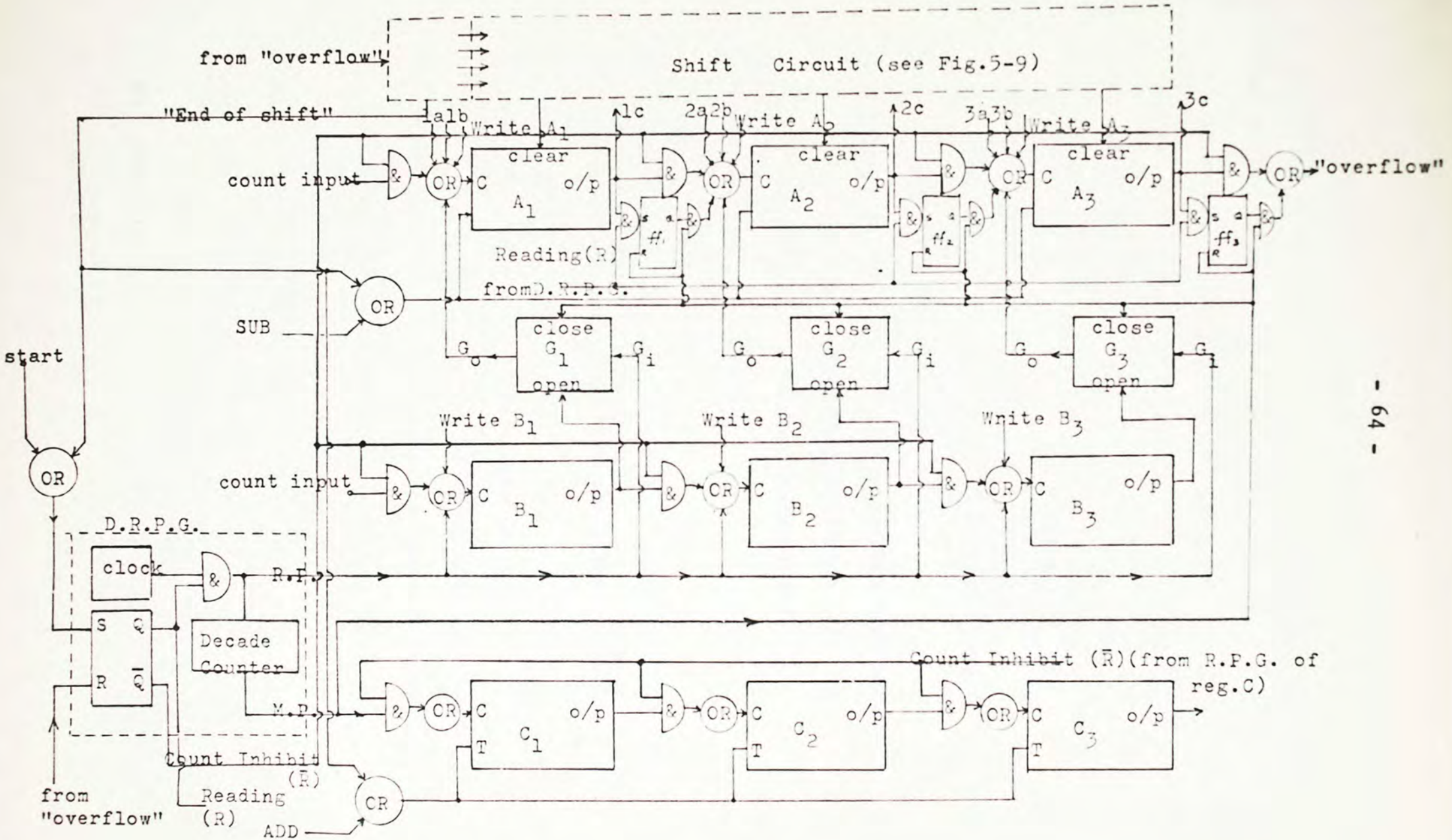


Fig.5-8 Schematic layout for non-restoring division

2. The D.R.P.G. generates :

(a) series of 10 read pulses --

to read content of reg.B (divisor register) repeatedly and transfer parallelly to reg.A,

(b) count inhibit ($\overline{R}$) --

to isolate all counting stages,

(c) marker pulse (M.P.) --

(i) to add '1' to the quotient register (reg.C) for each parallel transfer,

(ii) to generate the "carry" pulse for continuous propagation from stage to stage in register A (the "carry" from the last stage A_3 is termed "overflow").

3. "Overflow" from register A --

(i) stop D.R.P.G.,

(ii) "shift" the content in reg.A and C one digit forward (circuit and discussion about the "shift" mechanism will be given later).

4. "End of shift" from the Shift circuit --

(i) change circuit state of reg.A and reg.C (operation of these registers are changed from ADD to SUB and SUB to ADD),

(ii) re-activiate the D.R.P.G. .

5. The D.R.P.G. generates :

(a) series of 10 read pulses --

(same as step 2(a))

(b) count inhibit ($\overline{R}$) --

(same as step 2(b))

(c) marker pulse (M.P.) --

(i) to subtract '1' from the quotient register (reg.C) for each parallel transfer,

(ii) to assist the "carry" (same as step 2(c)(ii)).

6. "Overflow" from register A --

stop the D.R.P.G..

7. Check if the significant figure of the quotient is attained,

(i) if YES, division completed.

(ii) if NO, "shift" the content in reg.A and C one digit forward (the checking method will not be discussed in the text).

8. "End of shift" from the Shift circuit --

(same as step 4)

Using the illustrated numerical example again, i.e. 178÷111, the change of "flux state" in the dividend register (reg.A) and the divisor register (reg.C) during the non-restoring division operation is given below.

	Dividend register A_3	A_2	A_1	Quotient register C_2	C_1
1. enter dividend and divisor	1	7	8 .	0	0 .
2. change circuit state of reg.A (giving complements of $A_3..A_1$)	9-δ	3-δ	2-δ.	0	0 .
3. parallel transfer of divisor	10-δ	4-δ	3-δ.	0	1 .
4.	1-δ	5-δ	4-δ.	0	2 .
overflow					
5. shift	5-δ	4-δ	10-δ.	2 .	0
6. change circuit state of register A and register C	5	6	0 .	8-δ.	10-δ

	A_3	A_2	A_1	C_4	C_3	C_2	C_1
7. parallel transfer of divisor	6	7	1 .			9-δ.	1-δ
8.	7	8	2 .			9-δ.	2-δ
9.	8	9	3 .			9-δ.	3-δ
10.	0	0	4 .			9-δ.	4-δ
overflow							
11. shift	0	4	0 .		9-δ.	4-δ	10-δ
12. change circuit state of							
register A and register C	10-δ	6-δ	10-δ.		1 .	6	0
13. parallel transfer of divisor	1-δ	8-δ	1-δ.		1 .	6	1
overflow							
14. shift	8-δ	1-δ	10-δ.		1 .	6	1	0
15. change circuit state of							
register A and register C	2	9	0 .	9-δ.	4-δ	9-δ	10-δ
16. parallel transfer of divisor	4	0	1 .	9-δ.	4-δ	10-δ	1-δ
17.	5	1	2 .	9-δ.	4-δ	10-δ	2-δ
18.	6	2	3 .	9-δ.	4-δ	10-δ	3-δ
19.	7	3	4 .	9-δ.	4-δ	10-δ	4-δ
20.	8	4	5 .	9-δ.	4-δ	10-δ	5-δ
21.	9	5	6 .	9-δ.	4-δ	10-δ	6-δ
22.	0	6	7 .	9-δ.	4-δ	10-δ	7-δ
overflow							
23. End of division				(1 .	6	0	3)

(assume quotient of 4 significant figures is required)

The "shift" operation in the above example (steps 5,11,14) for the dividend and quotient registers can be described with the aid of Fig.5-9. The idea of shifting the content of reg.A one digit in advance is explained as follows :

(1) read out the content of reg.A and transfer it parallelly into an auxiliary register, say, reg.A', which is assumed initially empty. That is, $A_1 \rightarrow A'_1$, $A_2 \rightarrow A'_2$ etc. .

(2) clear the content of register A.

(3) read out the content of reg.A' and transfer it back to reg.A but with one digit shifted to the right (Fig.5-9), i.e. $A'_1 \rightarrow A_2$, $A'_2 \rightarrow A_3$ etc. .

(4) clear the content of register A'.

The schematic layout shown in Fig.5-9 can accomplish the mentioned idea. In response to the "overflow" signal of register A (Fig.5-8), the control signal generator in the Shift circuit will generate the following control signals :

(1) a series of 10 read pulses (R.P.) followed by a marker pulse (M.P.),

(2) logic levels A→A' and A'→A to control the content transfer,

(3) clear pulse with sufficient time interval to close switch S (Fig. 3-4) of each decimal counter in the register (A or A') and hence return their flux state to '0'.

These control signals will arrive in the following sequence :

(1) Clear pulse to register A'.

(2) A→A' = 1 , A'→A = 0 .

(3) 10 read pulses followed by a marker pulse. These read pulses (via terminals 1b, 2b, etc.) will read out the content of reg.A and transfer it to the corresponding stages in reg.A' (i.e. $A_1 \rightarrow A'_1$,

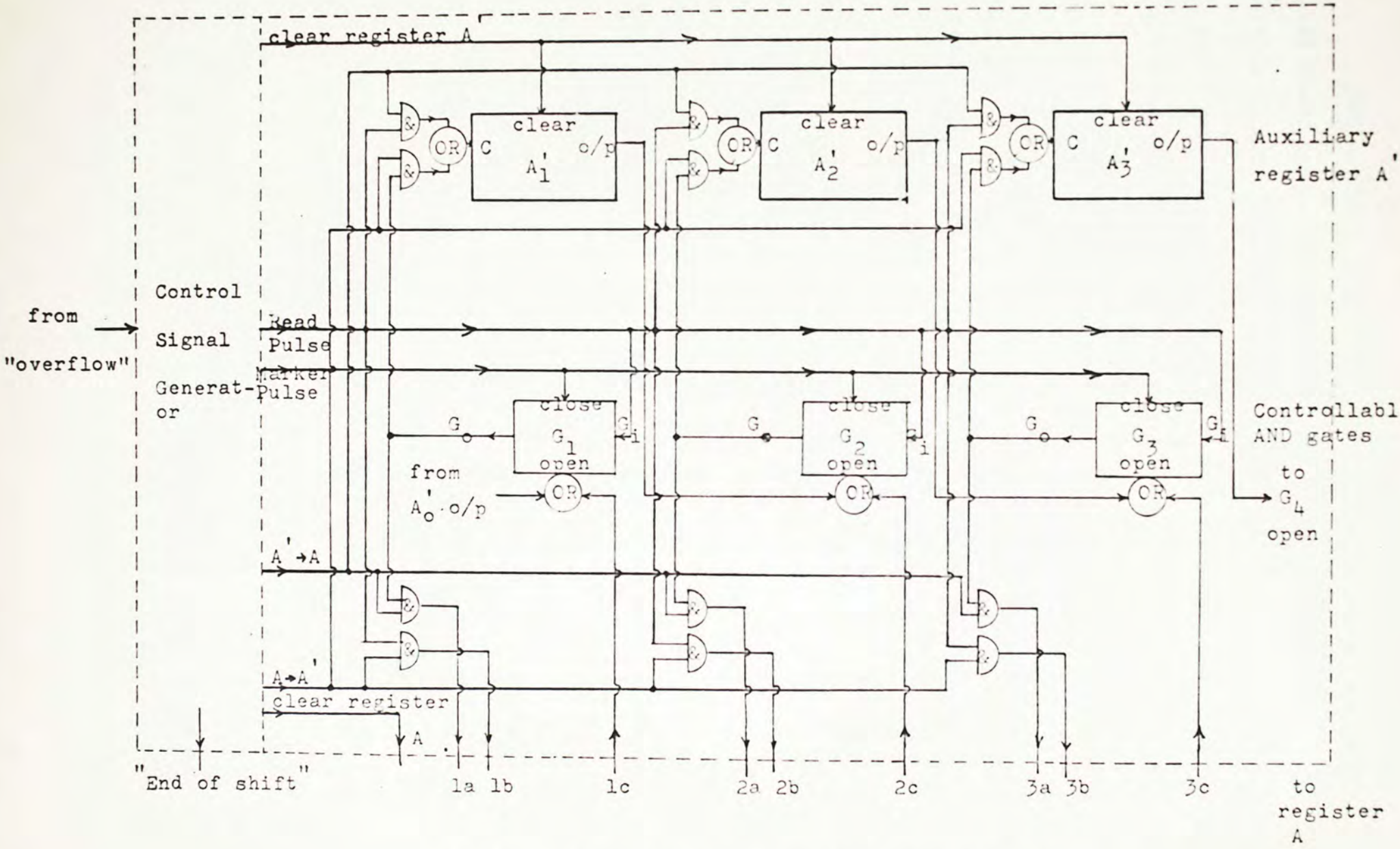


Fig.5-9 Schematic layout of the Shift Circuit

$A_2 \rightarrow A'_2$, etc.).

(4) Clear pulse to register A.

(5) $A' \rightarrow A = 1$, $A \rightarrow A' = 0$.

(6) 10 read pulses followed by a marker pulse. These read pulses will read out the content of reg.A' and transfer it back to reg.A (via terminals 1a, 2a, etc.) but with one digit shifted to the right (Fig.5-9).

Finally, the last marker pulse may be used as the "End of shift" signal (Fig.5-8) to re-activiate the D.R.P.G. .

VI Conclusion

Although square-loop magnetic cores have been widely used in binary systems yet it does not mean that there is no room for them to be used in multi-valued systems. Experiments show that a square-loop core has high storage density by utilization of its volt-time integrating property. Chapter I reviews the available multi-level counting circuits in the light of requirements for the development of storing decimal numbers by the core. Realization of decimal counting circuit with only one core in it is dealt with in Chapter II. In fact, the circuit is not limited to decimal operation, it can be extended to count any number of pulses. A simple magnetic theory for prediction of the number of counts is given. The theoretical calculations and experimental results agree quite well. The reversible operation of the circuit is studied in Chapter III and an extension to four stages reversible counter is described in Chapter V. When using the circuit as memory, the content in the core must be sensed out without being destroyed. A non-destructive readout method is hence given in Chapter IV. Application in simple arithmatic operation is also investigated in Chapter V. However, the development of the whole system is not yet completed, and some problems have to be further studied; namely, (1) the operating speed of the system, and (2) the selection of core.

About the problem of operating speed, one may have a first impression that the operating speed is slower than that of binary system. Of course, a newly developed system can hardly be compared with a well established one, but the problem is not so serious when one looks into it. The first reason that one has such an impression

is the magnetic core used in the research is quite large which accordingly requires a large switching time (pulse width). However, this problem can be solved by using smaller magnetic core. Since smaller core has a larger ratio of core surface area to core volume, the hysteresis loss which takes the form of heat can be more readily removed. This 'by-product' implies a smaller core can be driven more often than a larger one for the same rise in temperature. Consider the read-write operation. 10 read pulses are required for the non-destructive read operation in decimal system whilst only 2 pulses of opposite direction are required for read and restore in the binary. This paradoxical argument can be solved immediately by considering the switching time. For binary system, each of the read and restore pulse must have a minimum width of the order of the switching time T_s of that core, but that for decimal system is only 1/5 T_s because of partial switching. Hence the read time for both system is the same. Following the same idea, the average write time for decimal system is the same to that of binary system although pulses are input serially in the former case. However, the greatest advantage of decimal system over other radix system is that no coding and decoding is required since our daily used data is on base of ten, and it will save a lot of conversion time too.

About the problem of core selection, it can be divided into : (a) nature of core, e.g., Permalloy and ferrite, and (b) characteristic of the core, e.g., the squareness of the cores.

The choice between Permalloy and ferrite core is an engineering problem concerning the difference in properties between them. Some of their differences are listed below : (ref. 32, 33)

	Permalloy	ferrite
1. squareness ratio of hysteresis loop SR	higher	lower
2. saturation flux density B_s	0.8-1.6 weber/m^2	0.2 weber/m^2
3. coercive force H_c	10 Amp/m	80 Amp/m
4. Curie temperature T_c	460 C	300 C
5. thermal conductivity	higher	lower
6. thermal sensitivity	lower	higher
7. cost	higher	lower
8. switching coefficient k	5×10^{-5} sec.amp/m	8×10^{-5} sec.amp/m
9. hysteresis loss per volume per cycle	117 joules/m^3	80 joules/m^3

Notes : 1. squareness ratio SR is defined in Appendix I (AI-17);

2. switching coefficient k is defined by :

$k = T_s (H_i - H_o)$.

Ferrite cores are preferable in binary system for their advantages of low cost and higher switching rate in coincident current mode of operation. However, an expensive thermal stablizing system is required due to their characteristic of higher thermal sensitivity. If decimal memory system is constructed by utilizing the decimal magnetic counter, the coincident current method will be rejected. So Permalloy core, which has a lower switching coefficient, can be switched faster than ferrite for the same voltage excitation. Moreover, the higher saturation flux density enables smaller Permalloy cores to be used for the same flux swing, and the loss per core is consequently reduced which enables a higher repetitive switching rate. The higher squareness ratio of Permalloy cores implies their constant flux flyback in magnetic switching. Thus Permalloy cores are more preferable in multi-level

storage than ferrite cores. In addition, the hysteresis loop of the ferrite cores has a round shape at position near to flux saturation, this will cause miscounting frequently in magnetic counter[35].

Finally, it can be noted that the decimal storage technique developed in this research is another open area in the multi-valued logic systems. It may have a challenging opportunity in the future.

Appendix I

Simple Magnetic Switching Theory

This appendix is introduced to provide a simple, yet sufficient analysis concerning the response of a switched magnetic core, in particular, under the excitation of a constant voltage. For detailed analysis, references are given at the end of the appendix. Following topics will be discussed.

1. Mechanism of magnetic switching and magnetic core under constant force excitation,
2. Magnetic core driven by constant voltage,
3. Magnetic flyback and nonsquareness effect.

1. Mechanism of magnetic switching and magnetic core under constant force excitation

The analysis of magnetic switching is based on the domain theory of the ferromagnetism. Consider a ferromagnetic specimen of volume τ which contains N domains. Its net induction with reference to a specified direction is :

$$\vec{B} = \frac{1}{\tau} \overset{N}{\underset{j=1}{\Xi}} \tau_j \vec{B}_j \qquad \text{(AI-1)}$$

where τ_j and $\vec{B}_j$ are the volume and induction of the j^{th} domain, Ξ is a vector sum.

The magnitude of B is :

$$B = \frac{1}{\tau} \sum_j \tau_j B_j \cos\varphi_j \qquad \text{(AI-1a)}$$

where φ_j is the angle between $\vec{B}_j$ and $\vec{B}$ (the specified direction).

To obtain the rate of change of the induction, we differentiate (AI-1a) with respect to time,

$$\frac{dB}{dt} = \frac{1}{\tau}\sum_j \left(\tau_j \cos\varphi_j \frac{dB_j}{dt} + B_j \cos\varphi_j \frac{d\tau_j}{dt} - \tau_j B_j \sin\varphi_j \frac{d\varphi_j}{dt} \right) \quad \text{(AI-2)}$$

Equ(AI-2) can be interpretated as follows : the induction change inside a ferromagnetic specimen may be due to :

(i) the change in magnitude of $\vec{B}_j$ of a domain (says, due to temperature variation),

(ii) the change in domain volume (i.e., by domain wall motion),

(iii) the rotation of magnetization of a domain.

Assume that the environmental conditions (temperature and etc.) are fixed, $\frac{dB}{dt}$ may be resulted by either domain wall motion or rotation of magnetization, or both. Since wall motion involves rotation of spins at the boundary and requires less energy than the rotation of magnetization, it turns out to be a dominating process in the magnetic switching.

So the following analysis of the magnetic switching will based on the following assumptions :

(1) the flux in a magnetic core reverse through domain wall movement,

(2) the domain grows uniformly throughout the cross section of the material and the boundary conditions occurs at the surface of the core are ignored,

(3) the domain boundary move in a speed v proportional to the net applied field H_i, i.e.,

$$v = \alpha (H_i - H_o) \quad \text{(AI-3)}$$

where α is a proportional constant,

and H_o is a constant of the material in close relation to the coercive force.

(4) the domain wall area depends on the net flux Φ only. If S is the total wall area per unit volume, we have :

$$S = \psi(\Phi) \qquad \text{(AI-4)}$$

where $\psi(\Phi)$ is a function of flux (core state).

This function may be interpretated as follows : for small Φ , as H_i applies, the domain wall will move outward to increase the domain volume, which implies S is an increasing function for small Φ. But this increase continuous until the walls start colliding with each other, hence S decrease after reaching a maximum value.

Thus, the rate of increase of magnetic flux in the core is given by :

$$\frac{d\Phi}{dt} = c\, v\, S = c\, v\, \psi(\Phi) \qquad \text{(AI-5)}$$

where c is a constant of the dimension of flux, which is clearly equal to $2\Phi_s$ since, in the unit of time, the flux changes from $-\Phi_s$ to $+\Phi_s$ in the volume vS.

Equ(AI-5) together with equ(AI-3) give :

$$\frac{d\Phi}{dt} = \alpha\, c\, \psi(\Phi)(H_i - H_o) = f(\Phi)(H_i - H_o) \qquad \text{(AI-6)}$$

where $f(\Phi) = \alpha\, c\, \psi(\Phi)$

Equ(AI-6) is the fundamental equation for magnetic flux switching. Although the function $f(\Phi)$ is quite difficult to determine theoretically and it depends very much on the shape of the specimen, yet it can be found by experiment which may be performed as follows : First, excite the magnetic core with a constant current, which generate a constant

field H_i ($>H_o$), the rate of flux change $\frac{d\Phi}{dt}$ is detected by a sensing winding wound on the core. The function $f(\Phi)$ is then displayed on the C.R.O. by applying the integrated sensed output (which is the flux) to the X input and the sensed output itself to the Y input.

A plot of $f(B)$ for a 1/8 mil 4-79 Mo-Permalloy lamination was given by Chen and Papoulis in the appendix of their paper (reference A3). The scale is normalized and the function is reproduced here in Fig.AI-1. The curve is valid for different value of applied field and different kind of thin core (~1/8 mil), ferrite and Permalloy.

For practical design calculation, $f(\Phi)$ shown can be approximated to be a semi-circle with equation : (reference A5)

$$f(\dot{\Phi}) = \beta_N \sqrt{1 - (\Phi/\Phi_s)^2} \qquad \text{(AI-7)}$$

where β is the normalized factor of dimension "resistance-length".

Then equ(AI-6) becomes :

$$\frac{d\Phi}{dt} = \beta_N \sqrt{1 - (\Phi/\Phi_s)^2} \quad (H_i - H_o) \qquad \text{(AI-8)}$$

Equation (AI-8) will be used in the following analysis to describe the response of a switched magnetic core.

2. Magnetic core driven by a constant voltage

Consider a magnetic core with input winding of N_1 turns and resistance R_1 and loaded by a resistor R_2 connected across another winding of N_2 turns is driven by a voltage V at the input, as shown in Fig.AI-2.

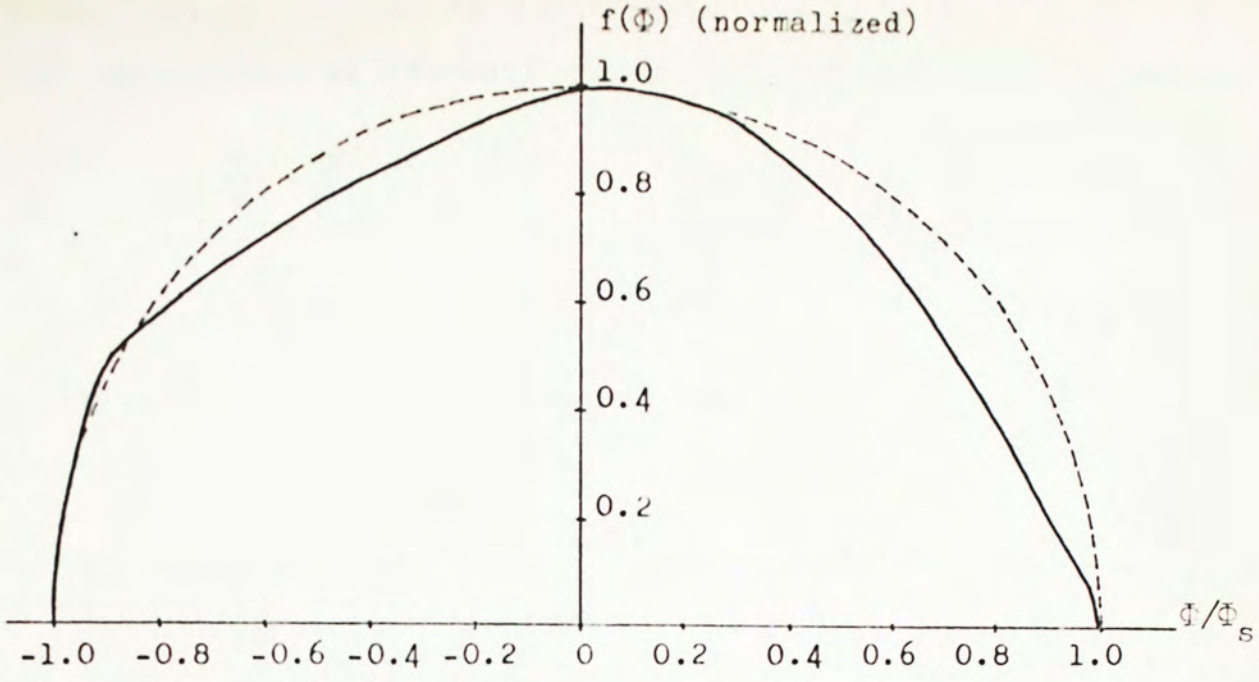


Fig.AI-1 The plot of $f(\Phi)$ for a 1/8 mil 4-79 Mo-Permalloy lamination (B_s=0.86 weber/m^2) can be well approximated to be a semi-circle

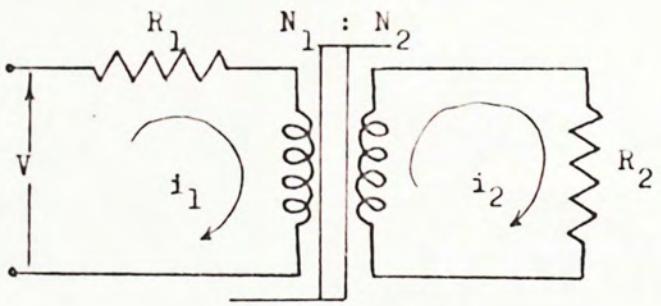


Fig.AI-2 A loaded magnetic core driven by a voltage source

By application of Kirchoff's equation to both loops, one obtain :

$$i_1 = \frac{V}{R_1} - \frac{N_1}{R_1}\frac{d\Phi}{dt} \qquad \text{(AI-9)}$$

$$i_2 = \frac{N_2}{R_2}\frac{d\Phi}{dt} \qquad \text{(AI-10)}$$

The driving field is then, by Ampere's law :

$$H_i = \frac{1}{\ell}(N_1 i_1 - N_2 i_2) \qquad \text{(AI-11)}$$

where ℓ is the mean length of the core.

Substituting (AI-9),(AI-10) and (AI-11) into equ(AI-8), after arranging terms, one obtain :

$$\frac{1 + a\sqrt{1-x^2}}{\sqrt{1-x^2}}\,dx = b\,dt \qquad \text{(AI-12)}$$

where $a = \frac{\beta}{\ell}\left(\frac{N_1^2}{R_1} + \frac{N_2^2}{R_2}\right)$

$$b = \frac{\beta}{\ell}\left(\frac{N_1 V}{R_1} - H_o \ell\right) / \Phi_s$$

$x = \Phi / \Phi_s$ ranging from -1 to +1.

Equ(AI-12) describes the time rate of flux change after the switching voltage V has been applied.

The solution to the differential equation (AI-12) can be obtained by integrating the left from -1 to x and the right from 0 to t, which is :

$$\arcsin x + \frac{\pi}{2} + a(x+1) = b\,t \qquad \text{(AI-13)}$$

The switching time (the time required for complete flux reversal) can be evaluated by putting x = +1 (positive saturation) into (AI-13),

which gives :

$$T_s = \frac{2a + \pi}{b} \qquad \text{(AI-14)}$$

Here, we are only interested in how the flux changes with time. A simple interpretation of the flux solution given in equ(AI-13) is given as follows :

(1) Usually $a = \frac{\beta}{\ell}\left(\frac{N_1^2}{R_1} + \frac{N_2^2}{R_2}\right)$ is very large such that $a(x+1)$ is much greater than $\arcsin x + \frac{\pi}{2}$ even for the smallest x $(=-\Phi_r/\Phi_s)$; in this case, the term $\arcsin x + \frac{\pi}{2}$ is dropped with respect to the term ax.

(2) Equ(AI-13) then becomes :

$$\left(\frac{N_1^2}{R_1} + \frac{N_2^2}{R_2}\right) x = \left(\frac{N_1 V}{R_1} - H_o \ell\right) t \,/\, \Phi_s$$

$$\text{or} \quad \left(\frac{N_1^2}{R_1} + \frac{N_2^2}{R_2}\right)\Phi_s \, x = \left(\frac{N_1 V}{R_1} - H_o \ell\right) t \qquad \text{(AI-15)}$$

(3) If $\frac{N_1 V}{R_1} \gg H_o$ (i.e., hard drive) and $N_1 \cong N_2$, $R_1 \gg R_2$, equ(AI-15) reduced to the simplest form :

$$N_1 \Phi_s \, x = V \, t \qquad \text{(AI-16)}$$

this is in fact a direct consequence of Faraday law $\left(V_{ind} = N \frac{d\Phi}{dt}\right)$ applied to an unloaded core with input winding of low resistance.

Conclusion :

When the magnetic core is driven by a constant voltage, the rate of flux change is described by equ(AI-13) in general, and usually, the approximated solution given in equ(AI-15) is valid, which implies the flux increment is practically a linear function of time.

3. Magnetic flyback and nonsquareness effect

It is well known that the behaviour of a ferromagnetic material excited by external field (at low frequency) can be described by the hysteresis loop. When the core is driven by a series of rectangular pulses, the hysteresis loop consists of a major loop and a numbers of minor loops as that given in Fig.2-1. The minor loops formed by magnetic flux flyback occurs at the termination of each applied field is emphatically given in Fig.AI-3.

The magnetic flux flyback is a collective result of the elastic motion of the domain walls and elastic rotation of magnetic spin. Since there are certain preferred positions for domain walls and directions for magnetization vector which corresponds to a lower energy state, they return to the nearest stable state once the excitation is removed and result in the magnetic flux flyback.

In order to analysis the effect of magnetic flyback, a quantitative parameter -- the Squareness Ratio (SR) of the core is defined as : (Fig.AI-4)

$$SR = 1 - \frac{\Delta\Phi_{2Hc}}{\Phi_s} \qquad \text{(AI-17)}$$

From the definition, a core with a squarer hysteresis loop has a higher SR, and the magnetic flyback is less significant. For an ideal square loop core, the SR is 1 and no magnetic flux flyback can be observed.

Using the modified hysteresis loop instead of the ideal one, a flyback flux is associated with each incremental flux switching. If $\Delta\Phi_{tot}$ represents the total flux switched by a single pulse, the flyback flux ($\Delta\Phi_{fly}$) must be subtracted from this value in order to get the effective flux ($\Delta\Phi_{eff}$) in response to the applied pulse. This flyback

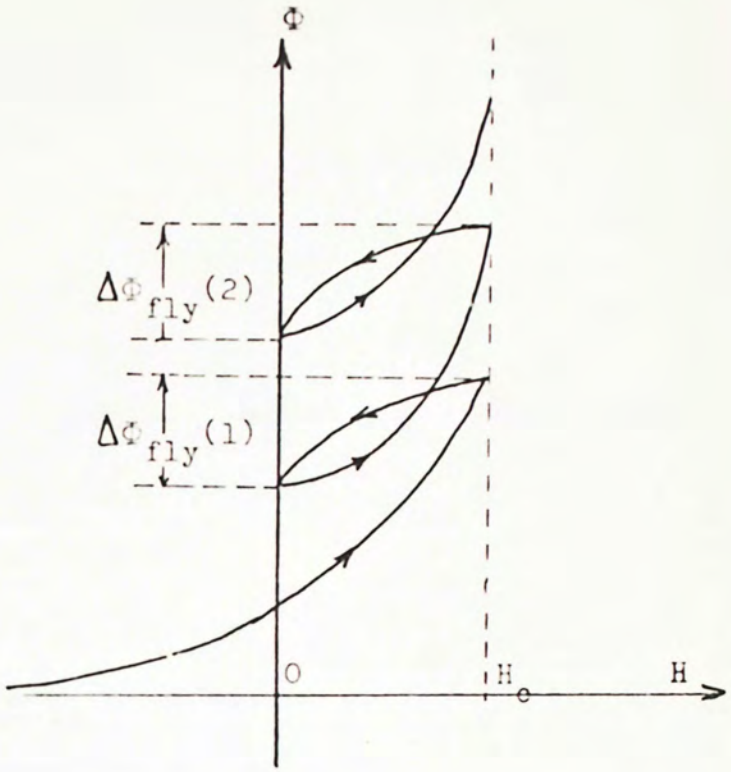


Fig.AI-3
Magnetic flux
flyback

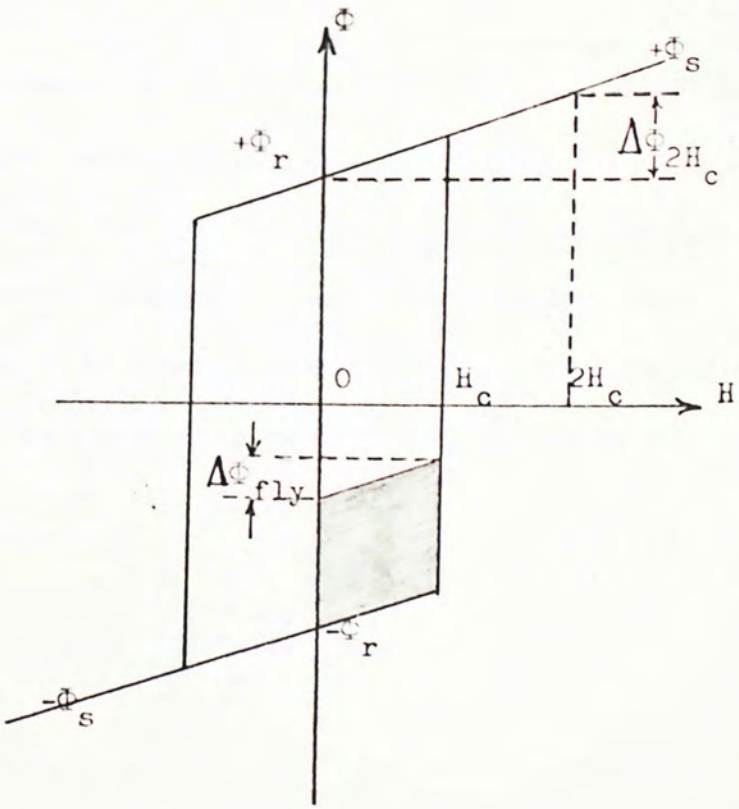


Fig.AI-4
Improved model for
the hysteresis loop
to account for the
magnetic flyback
effect

flux is related to the SR of the core by :

$$\Delta\Phi_{fly} = \Phi_s (1 - SR)/ 2 \qquad (AI-18)$$

Then the effective flux switching for each input pulse is :

$$\Delta\Phi_{eff} = \Delta\Phi_{tot} - \Delta\Phi_{fly} \qquad (AI-19)$$

If equation (AI-16) is valid, the minimum pulse width for magnetic switching is found to be (by putting $\Delta\Phi_{tot} = \Delta\Phi_{fly}$) :

$$T_{min} = \left[(1-SR)/2\right]\left[N\Phi_s/V\right] \qquad (AI-20)$$

This equation can explain the case why no effective switching is observed even when sufficient excitation is applied to the core.

However the analysis given above is valid only for the cores of high degree of squareness, such as Permalloy G core where the flyback flux is found to be a constant (see Fig.2-6(f)). But for the Permalloy F core and most ferrite core, the hysteresis loop is less square that give a variable flyback flux (Fig.3-3). Yet it can still be approximated to be a linear function of the flux, and is given by : (reference A6)

$$\Delta\Phi_{fly}(x) = \Delta\Phi_{fly}(0) + bx \qquad (AI-21)$$

where $\Delta\Phi_{fly}(0)$ is the initial flyback flux,

b is a constant,

and $x = \Phi/\Phi_s$ ranges from -1 to +1.

In this case, the magnetic switching is nonlinear as long as $\Delta\Phi_{tot}$ is a constant.

References for Appendix 1

A1. Bennion,D.R.,Crane,H.D. and Nitzan,D.: Digital Magnetic Logic, McGraw Hill, 1969, chapters 11, 12.

A2. Carter,W.L., and Knoke,P.J.: Unconventional approach to Pulse-Width Measurement, Electronics, vol.35, no.43, Oct., 1962, pp.51-53.

A3. Chen,T.C. and Papoulis,A.: Terminal properties of magnetic cores, Proc.IRE, vol.46, no.5, May, 1958, pp.839-849.

A4. Goodenough,J.B.: A theory of domain creation, coercive force in polycrystalline ferromagnetics, Phys.Rev., vol.95, Aug., 1954, pp.917-932.

A5. Neeteson,P.A.: Square-loop Ferrite Core Switching, Philips Technical Library, Netherlands, 1964, chapters 2, 4-6,17.

A6. Rozenblat,M.A. and Fedin,G.V.: A multilevel core counter and its use, IEEE Trans.Mag., MAG-9, no.1, March, 1973, pp.27-31.

A7. Williams,H.J.,Shockley,H.,and Kittel,C.: Studies of the propagation velocity of a ferromagnetic domain boundary, Phys.Rev., vol.80, Dec., 1950, pp.1090-1094.

Appendix II

Circuit Analysis For The Magnetic Counter

1. Quiescent Condition

Assume that the leakage current I_{CBO} is negligible, the transistors Q_1 and Q_2 are identical, the collector voltage and current and base current for both saturated and cutoff conditions are given by : (from equivalent circuit shown in Fig.AII-1)

$$V_{C(off)} = V_{CC} - V_{BE(sat)} \frac{R_B}{R_B + R_C} + V_{BE(sat)} \qquad \text{(AII-1a)}$$

$$V_{C(on)} = V_{CE(sat)} \qquad \text{(AII-1b)}$$

$$I_{C(off)} = 0 \qquad \text{(AII-2a)}$$

$$I_{C(on)} = \frac{V_{CC} - V_{CE(sat)}}{R_C} \qquad \text{(AII-2b)}$$

$$I_{B(off)} = 0 \qquad \text{(AII-3a)}$$

$$I_{B(on)} = \frac{V_{C(off)} - V_{BE(sat)}}{R_B} = \frac{V_{CC} - V_{BE(sat)}}{R_B + R_C} \qquad \text{(AII-3b)}$$

It is assumed that the gain of the transistors are sufficiently large to ensure one transistor is saturated while the other is cutoff.

2. Switching Condition

(a) before the core is saturated

When the input voltage V_{in} is applied to the input terminal, the effective switching voltage across the winding is V_s, which is given by : (see equivalent circuit shown in Fig.AII-2)

$$V_s = V_{in} - V_{BE(sat)} - V_{DT} \qquad \text{(AII-4)}$$

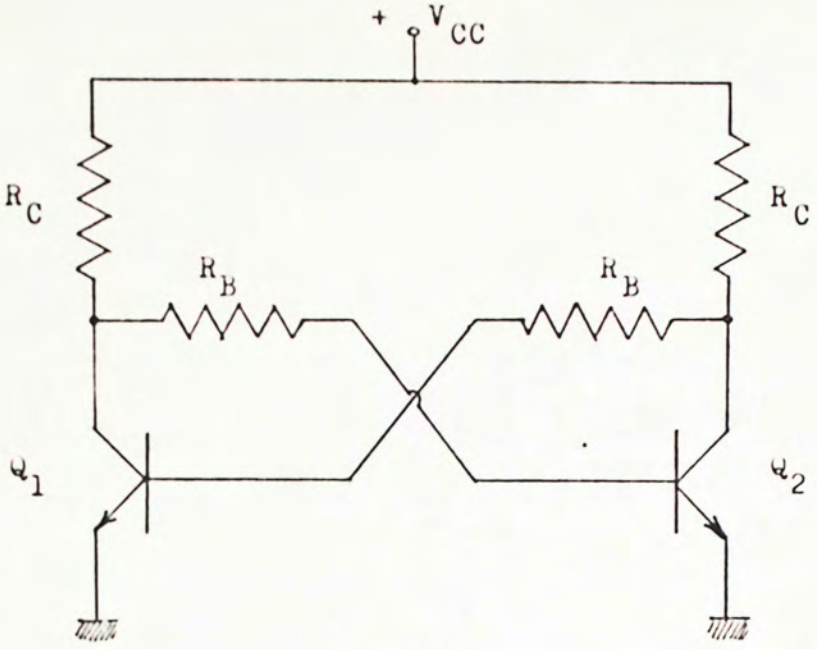


Fig.AII-1 Circuit for quiescent condition

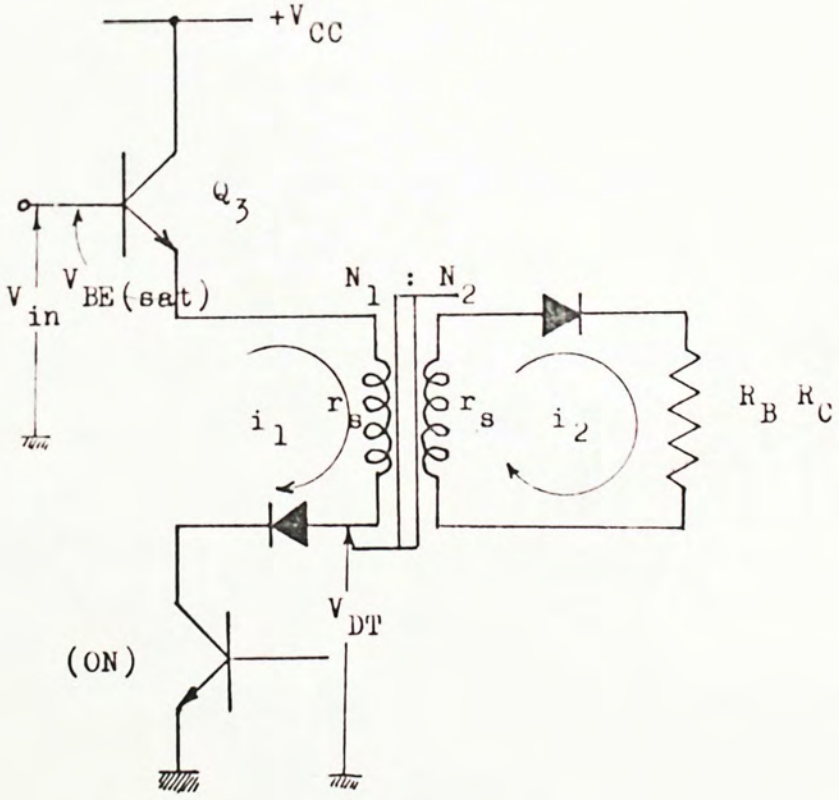


Fig.AII-2 Equivalent circuit of counter circuit : before the core is saturated .

where $V_{BE(sat)}$ is the saturation voltage across the BE junction of transistor Q_3,

and V_{DT} is the DC voltage drop across the diode and the CE junction of the saturated transistor during pulsing.

Assuming the switching transistor Q_3 has a low output impedance and that the switching winding has a resistance of r_s, the input loop equation is :

$$i_1 = \frac{V_s}{r_s} - \frac{N_1}{r_s}\frac{d\Phi}{dt} \qquad \text{(AII-5)}$$

Since the core is now loaded by a diode in series with the parallel of R_B and R_C, together with the winding resistance r_s, the secondary loop equation is modified to be :

$$i_2 = \frac{N_2\frac{d\Phi}{dt} - V_D}{R_2} \qquad \text{(AII-6)}$$

where V_D is the voltage drop on the diode,

and $R_2 = (R_C /\!/ R_B) + r_s$

Using the analysis in Appendix I, the differential equation is given by :

$$\frac{1 + a\sqrt{1-x^2}}{\sqrt{1-x^2}}\,dx = b\,dt \qquad \text{(AII-7)}$$

where $a = \frac{\beta}{\ell}\left(\frac{N_1^2}{r_s} + \frac{N_2^2}{R_2}\right)$

$$b = \frac{\beta}{\ell}\left(\frac{N_1 V_s}{r_s} + \frac{N_2 V_D}{R_2} - H_o\ell\right) / \Phi_s$$

and $x = \Phi / \Phi_s$ ranging from -1 to +1.

The corresponding solution to the above equation is then equal to equ(AII-13) in Appendix I with only the constant a and b change to the expression as given above.

Taking the circuit parameter of the G core counter as an example :

$$a = \frac{1}{4.99\times10^{-2}}\left(\frac{350^2}{10}+\frac{350^2}{980}\right) = 2.5\times10^5$$

in which, the fact that β is of the order of unity, $\ell = 4.99\times10^{-2}$ m and $r_s = 10$ ohm are used.

Even for the smallest $x = -\Phi_r/\Phi_s = -0.95$ (G core)

$$a(x+1) = (2.5\times10^5)(0.05) = 1.25\times10^4$$

is still much greater than $\left[\arcsin x + \frac{\pi}{2}\right]_{max} = \pi$, so that the approximated solution in equ(AI-15) of Appendix I can be used, which implies :

$$\frac{d\Phi}{dt} = \frac{\frac{N_1V_s}{r_s}+\frac{N_2V_D}{R_2}-H_o\ell}{\frac{N_1^2}{r_s}+\frac{N_2^2}{R_2}} \qquad \text{(AII-8)}$$

To include the flyback flux, the expression of (AI-18) in Appendix I gives :

$$\Delta\Phi_{fly} = \Phi_s\frac{1-SR}{2}$$

then the effective flux change for an input pulse of width T is :

$$\Delta\Phi_{eff} = \Delta\Phi_{tot} - \Delta\Phi_{fly}$$

$$= \frac{\frac{N_1V_s}{r_s}+\frac{N_2V_D}{R_2}-H_o\ell}{\frac{N_1^2}{r_s}+\frac{N_2^2}{R_2}}T - \Phi_s\frac{1-SR}{2} \qquad \text{(AII-9)}$$

The number of pulses required to switch the core from $-\Phi_s$ to $+\Phi_s$ is then equals to :

$$n = \frac{2\Phi_s}{\Delta\Phi_{eff}} = \frac{2\Phi_s}{\dfrac{\dfrac{N_1 V_s}{r_s} + \dfrac{N_2 V_D}{R_2} - H_o \ell}{\dfrac{N_1^2}{r_s} + \dfrac{N_2^2}{R_2}} T - \Phi_s \dfrac{1 - SR}{2}} \qquad \text{(AII-10)}$$

(b) when the core is saturated

After applying the n^{th} pulse, the core reaches its positive saturation which cause the induced e.m.f. on the windings to collapse. Diode D_2 will cease to conduct, thus decoupling winding N_2 from the collector of the OFF transistor Q_2. The equivalent circuit for this condition is shown in Fig.AII-3. The voltage at the collector of the ON transistor Q_1 is given approximately by :

$$V_{C_1} = \frac{r_{CE(sat)}}{r_s + r_D + r_{CE(sat)}} \left[V_{in} - V_{BE(sat)} - V_D \right] \qquad \text{(AII-11)}$$

This voltage will transmit to the base of transistor Q_2, and, if large enough, switch it from OFF condition to ON condition. Transistor Q_1 will be turned off accordingly by the flip-flop effect.

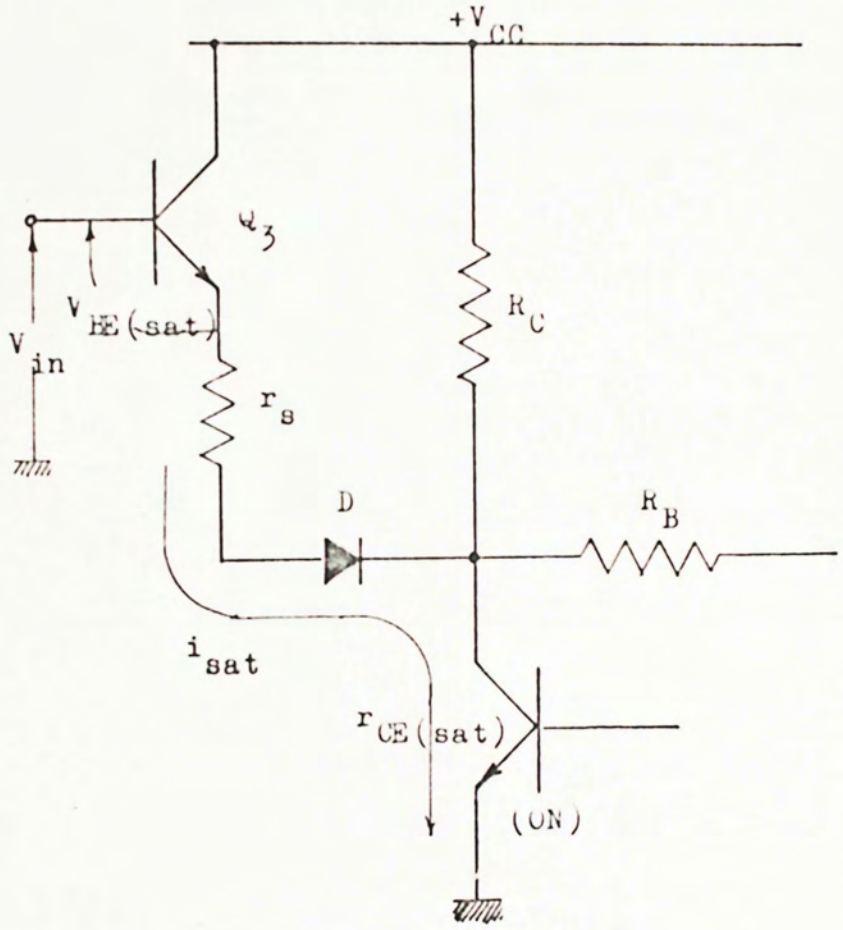


Fig.AII-3 Equivalent circuit of counter circuit : when the core is saturated.

Appendix III

The Magnetic Counter Stability

The experiments show that about 2% tolerance in the volt-time integral of the input pulse has no effect on the counts in the core. Taking the four constructed G core counters as an example, the required pulse width for decimal storage in each is :

pulse amplitude V_{in} = 5 V

	Pulse Width (μ S)		
	T_{min}	T_{max}	Tolerance*
GC1	880	900	1.12%
GC2	887	923	1.99%
GC3	940	1010	3.59%
GC4	995	1033	1.87%
		Average Tolerance =	2.14%

* Tolerance= $T_{max}-T_{min}/T_{max}+T_{min}$

The significance of above measurements show that the magnetic counter has good stability because each stores the same numbers of count regardless of the tolerances in pulse width.

Since, from equ.2-5, the change in the pulse width is related to that of the switching voltage by : (assume $N_1=N_2$)

$$\frac{\Delta T}{T} + \frac{\Delta V_s}{V_s + \frac{r_s V_D}{R_2} - \frac{r_s}{N} H_o \ell} = 0 \qquad \text{(AIII-1)}$$

Together with the experimental result, i.e., a tolerance in T even when the switching voltage V_s is kept constant, equ(AIII-1) is modified to be :

$$\frac{\Delta T}{T} + \frac{\Delta V_s}{V_s + \frac{r_s V_D}{R_2} - \frac{r_s}{N} H_o \ell} = 2.14\% \qquad \text{(AIII-2)}$$

For the given circuit parameter, $V_s \gg \frac{r_s V_D}{R_2} - \frac{r_s}{N} H_o \ell$, by equ(AII-4) in Appendix II, the condition of stability of the magnetic counter can then be described by the following expression :

$$\frac{\Delta T}{T} + \frac{\Delta V_{in}}{V_{in} - V_{BE(sat)} - V_{DT}} = 2.14\%$$

Appendix IV

The Constructed Circuits

The constructed circuits include (1) read pulse generator , (2) controllable AND gate, (3) LED indicator and (4) pulse former (PF) for each counting stage (see Fig.3-4), besides the magnetic counter.

1. Read Pulse Generator

The constructed read pulse generator can generate 4 bursts of 10 read pulses separated by the marker pulses. The schematic layout and the output time chart is shown in Fig.AIV-1(a) and (b) respectively. The actual circuit is shown in Fig.AIV-2.

2. Controllable AND Gate

The actual circuit of the controllable AND gate (for 4 counting stages) is shown in Fig.AIV-3.

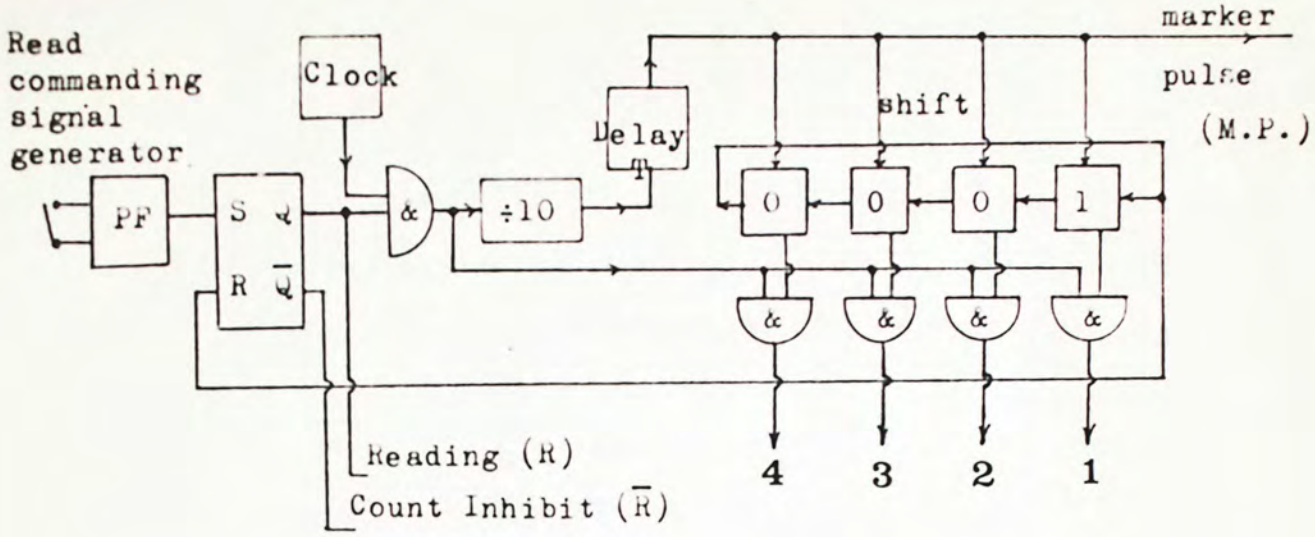
3. LED Indicator

The constructed LED indicator has only a single input terminal that the 4 bursts of readout pulses should have to enter serially. The schematic layout is shown in Fig.AIV-4 and the actual circuit is shown in Fig.AIV-5.

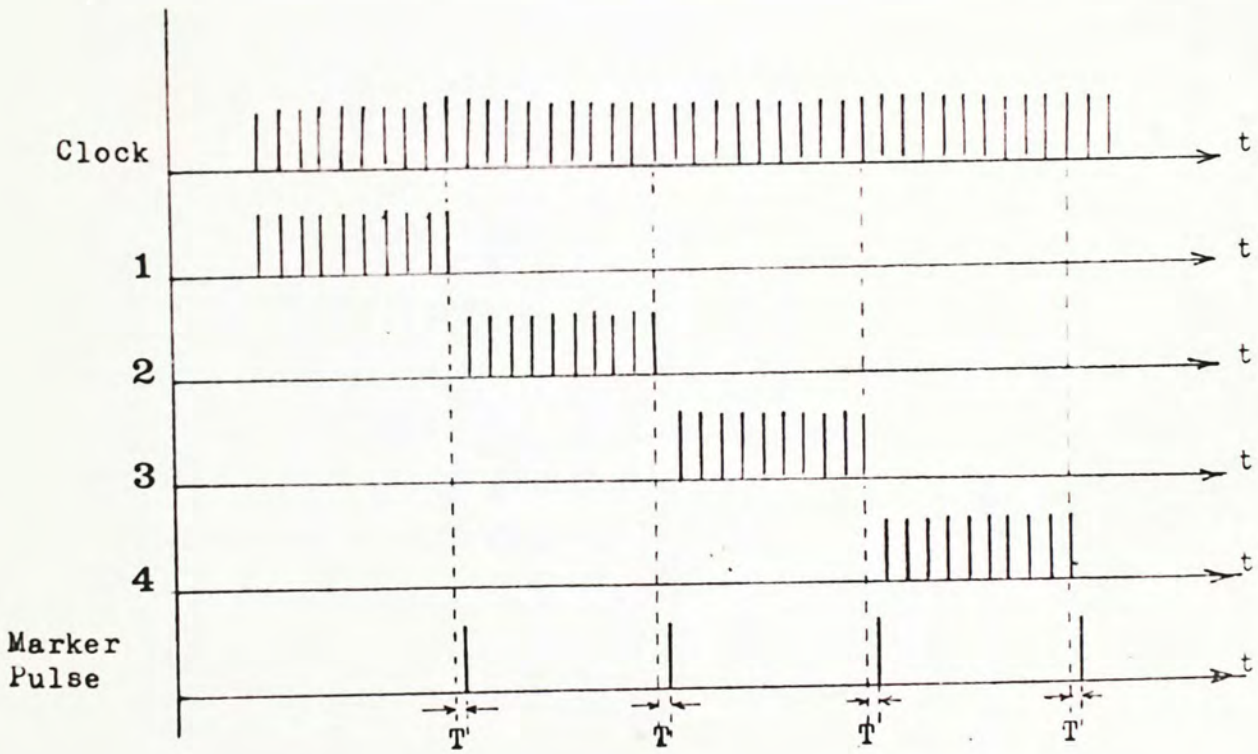
4. Pulse Former for counting stage

The actual circuit is shown in Fig.AIV-6.

The photographs for the experimental set up, constructed circuits (listed above) and the magnetic counter are given in Fig.AIV-7, AIV-8 and AIV-9 respectively.

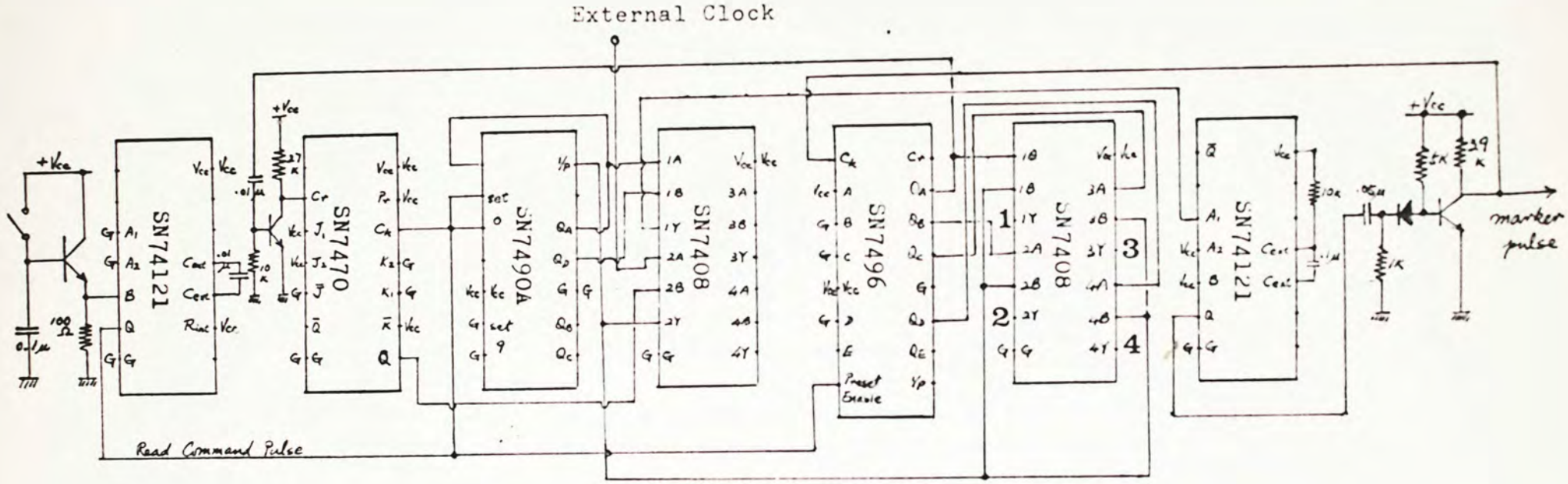


(a) Schematic layout of the read pulse generator



(b) Time chart of the read pulse generator

Fig.AIV-1 Read Pulse Generator



Read Commanding Signal Generator | flip-flop | Decade Counter | AND gates | shift register | AND gates | Delay and trailing edge pulse former

Fig.AIV-2 Actual circuit of the Read Pulse Generator

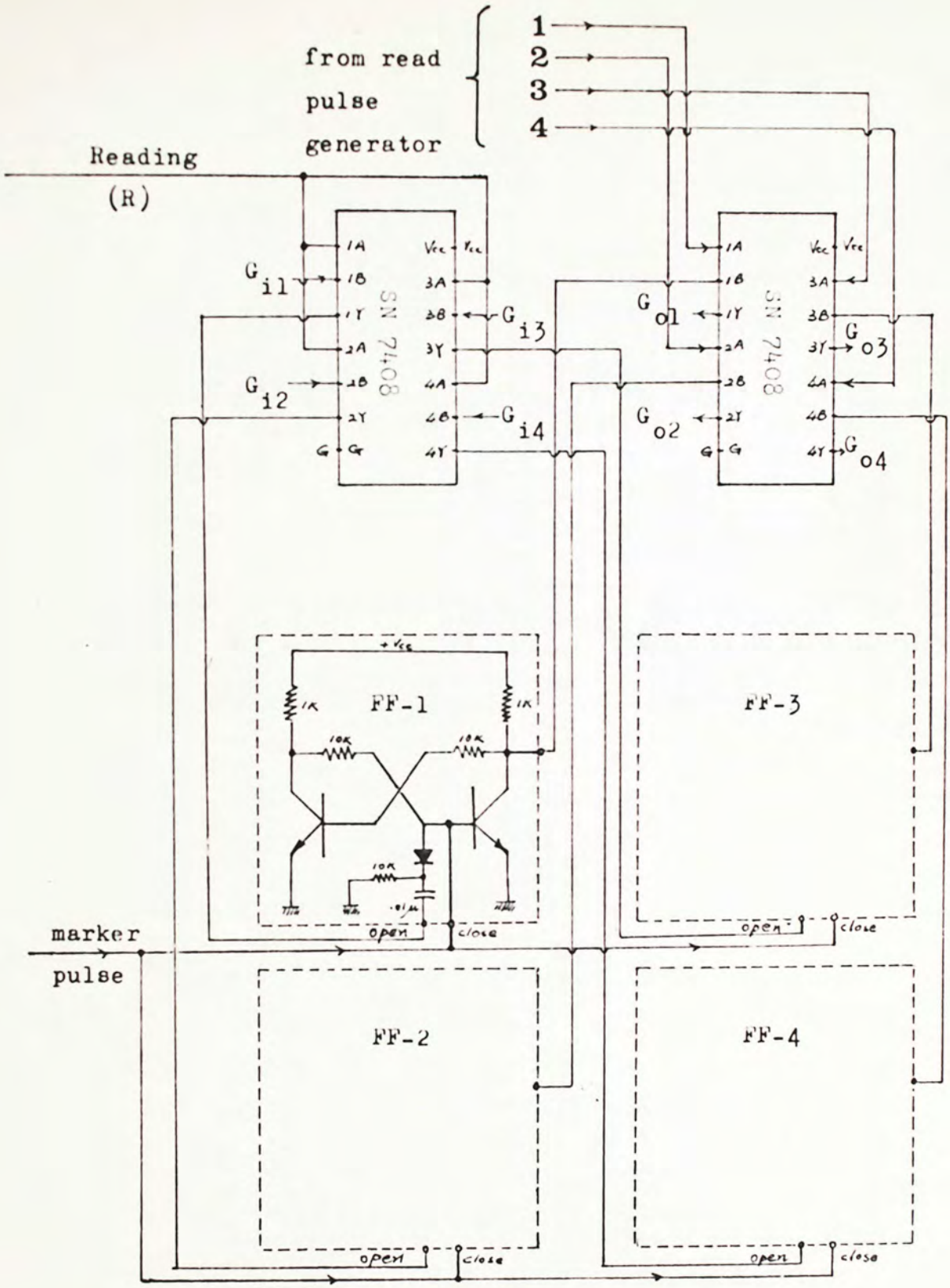


Fig.AIV-3 Controllable AND gate
(for 4 counting stages)

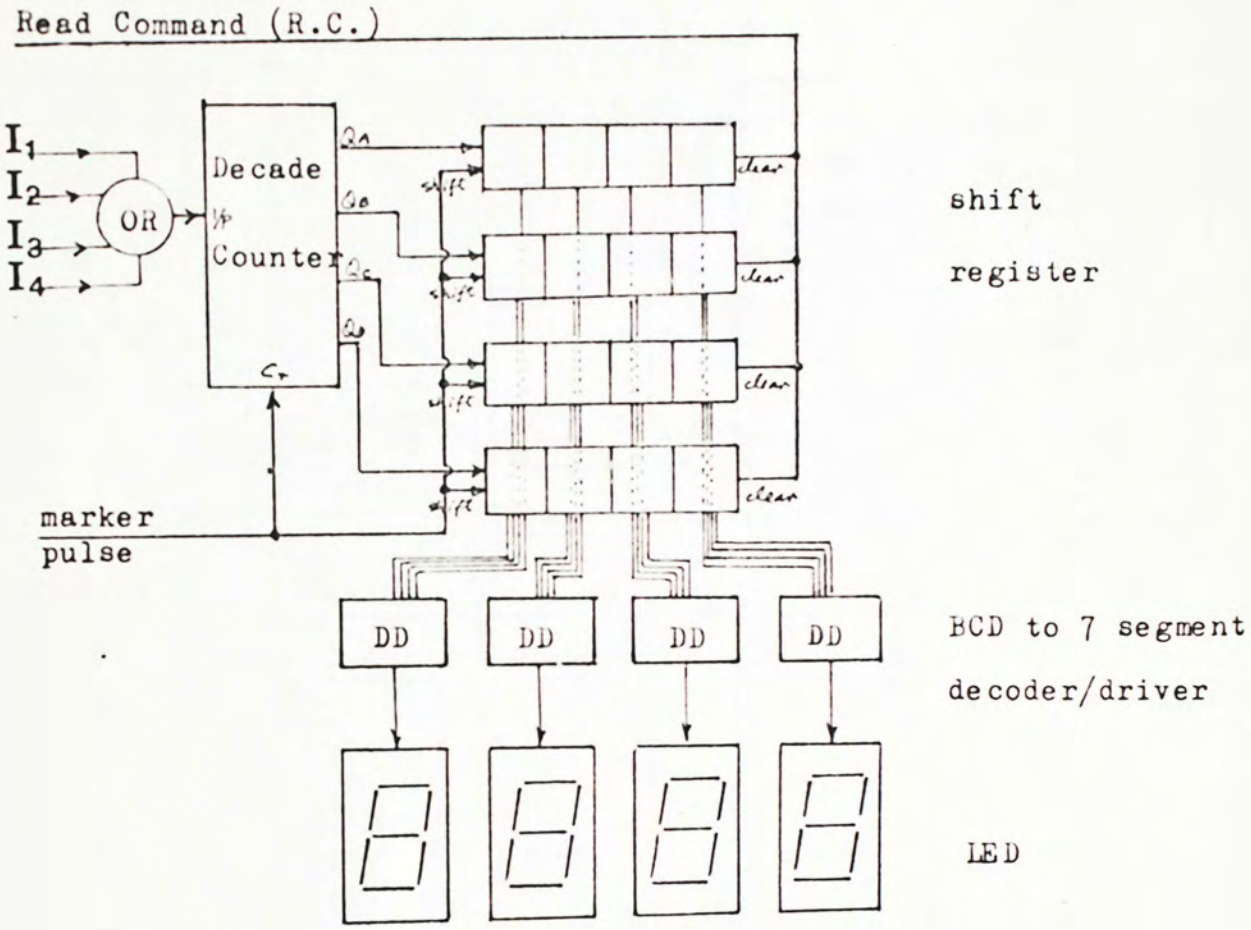


Fig.AIV-4 Schematic layout of the LED indicator

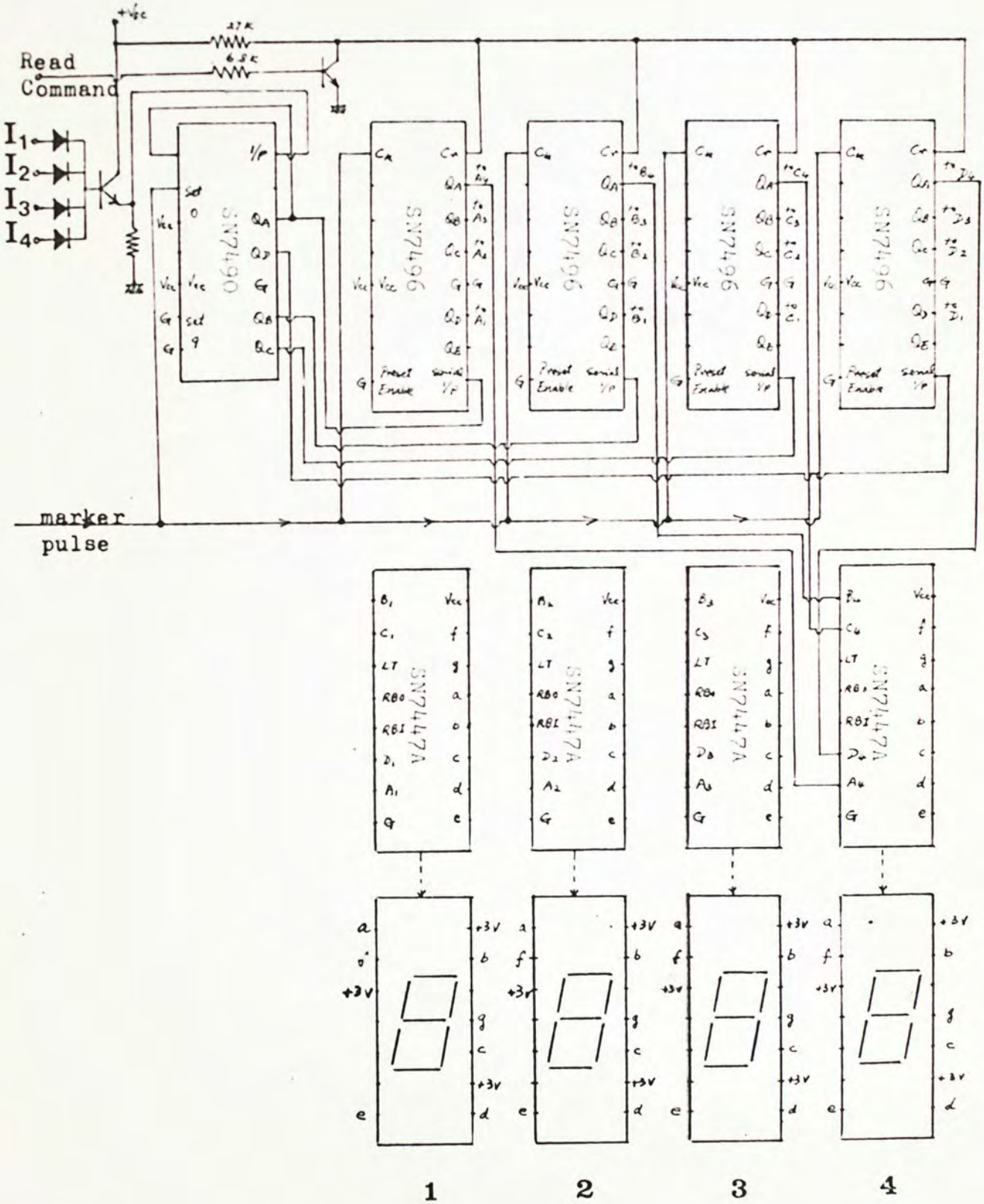


Fig.AIV-5 Actual circuit of

the LED indicator

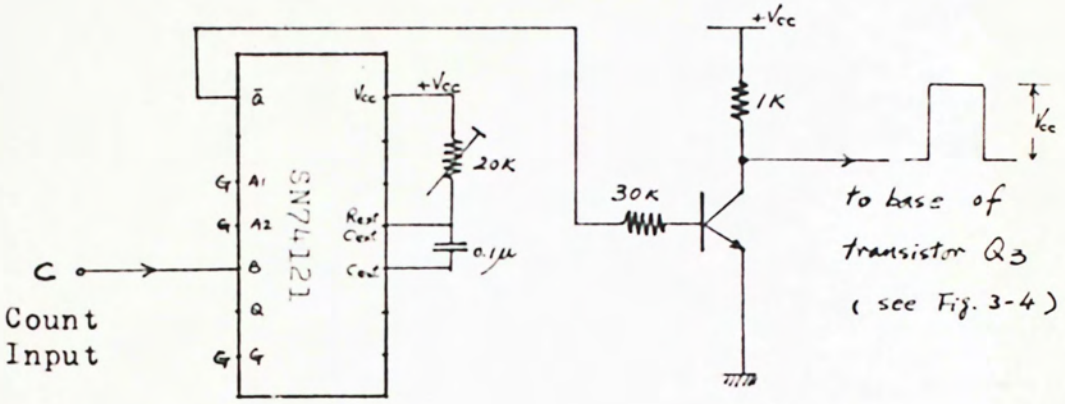


Fig.AIV-6 Actual circuit of

Pulse Former

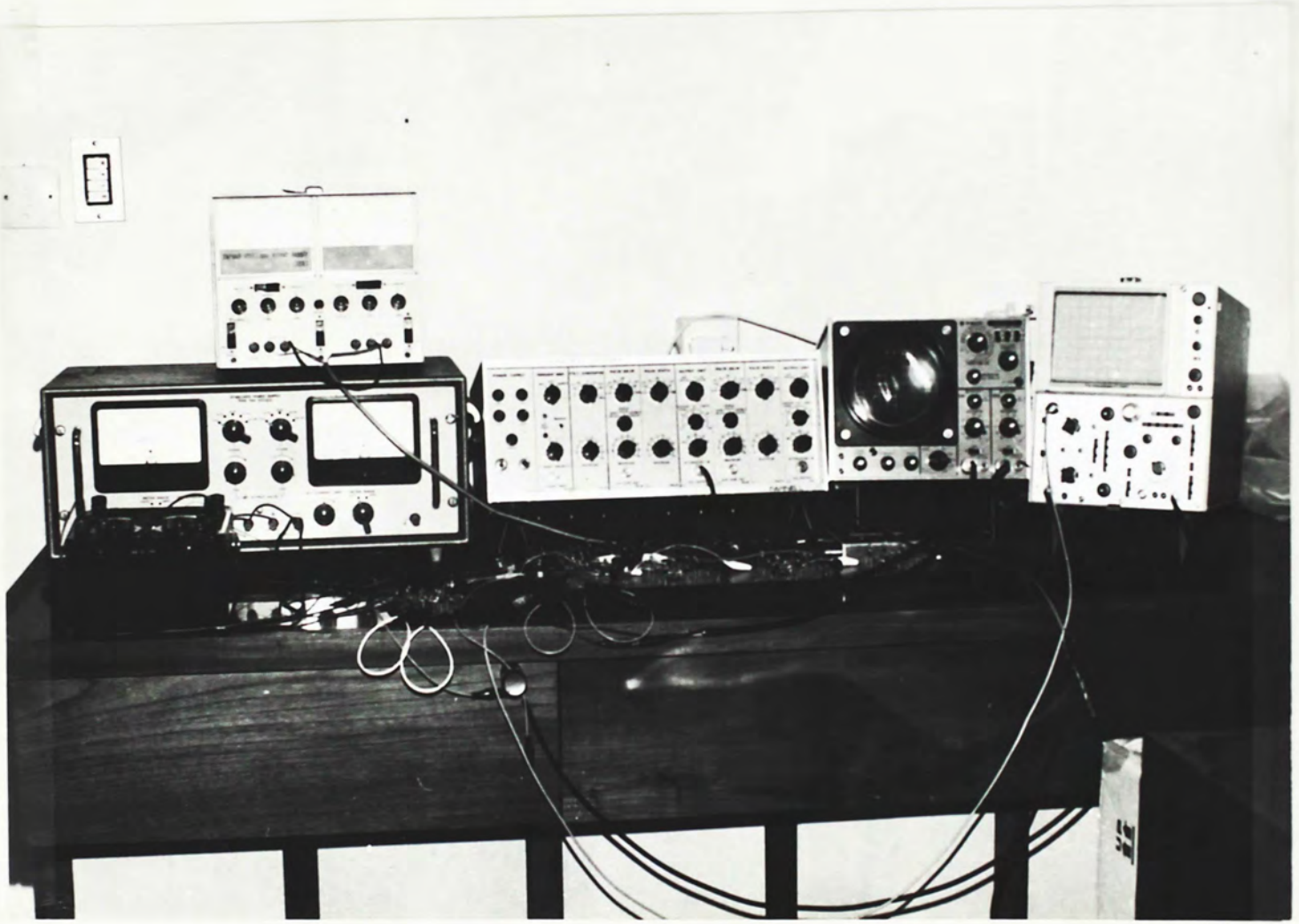


Fig.AIV-7 The experimental set up

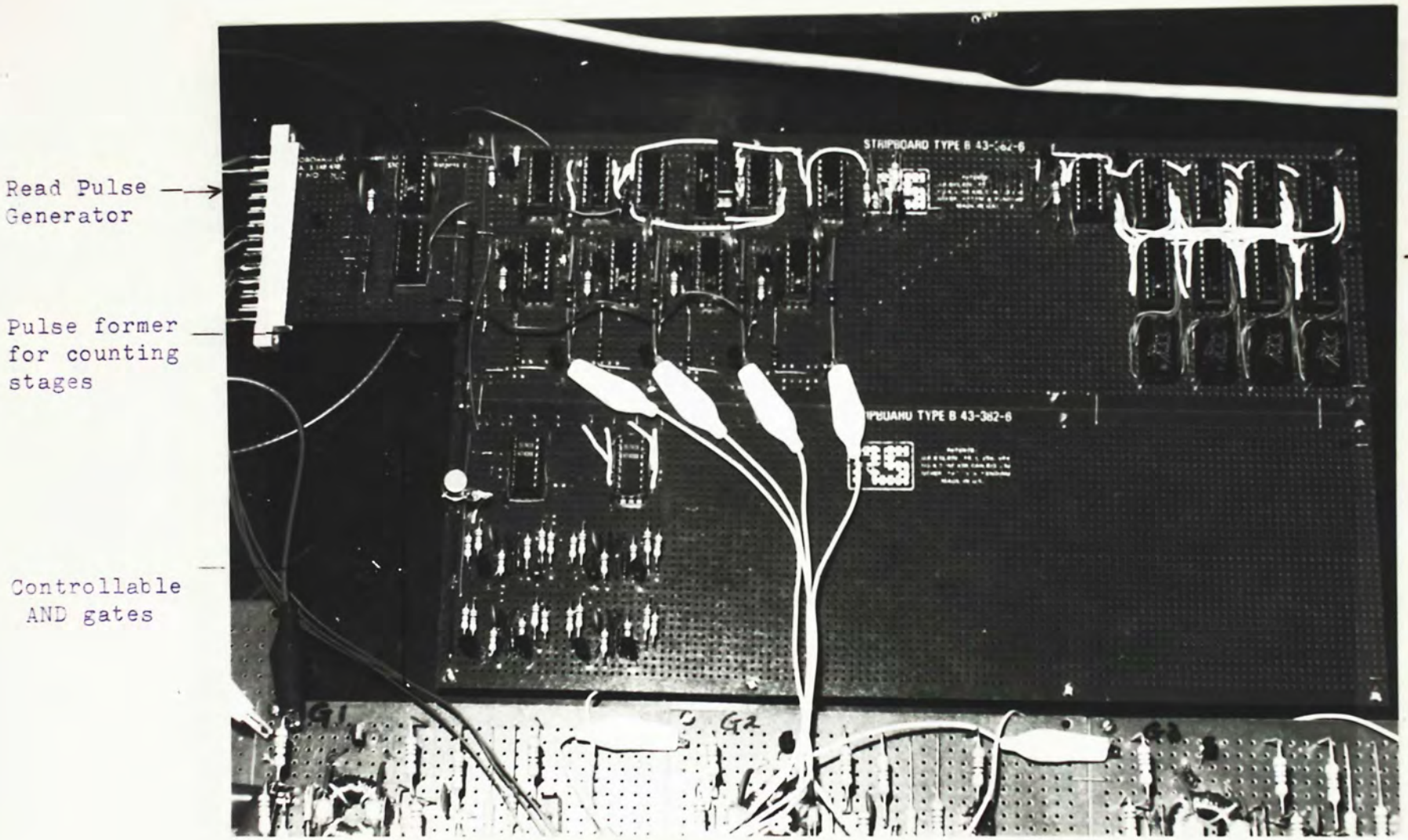


Fig.AIV-8 The constructed circuits

(Read pulse generator, controllable AND gates, LED indicator and pulse formers for counting stages)

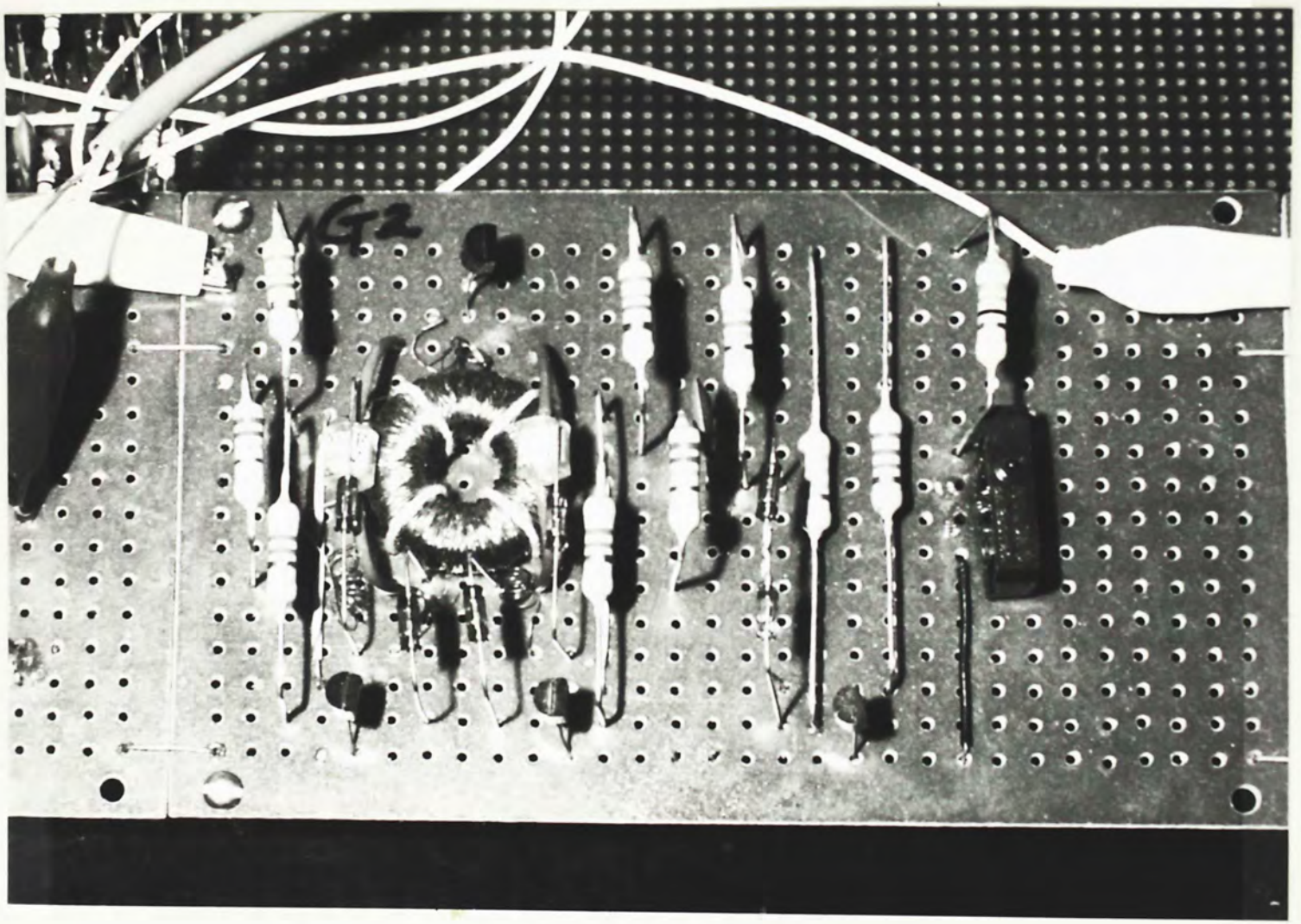


Fig.AIV-9 The magnetic counter

References

1. Duffing,P. and Tschermark,M.: Die Zahldrossel ein magnetisches Schaltungselement, Siemens-Zeitschrift, vol.26, Apr., 1952, p.140.
2. Pittman,G.F.Jr.: A high-accuracy static time delay device utilizing transistors, AIEE Trans., Pt-1, vol.74, Mar., 1955, pp.54-58.
3. Schaeffer,D.H.: Magnetic core event counter for earth satellite memory, Elect.Eng., vol.77, 1958, p.52.
4. Sakurai,Y. and Tanaka,T.: A magnetic counter, J.Soc.Instr.Tech. Japan, vol.9, 1959, pp.283-289.
5. Hardies,C.E.: Long time delays from a single magnetic storage core, AIEE Trans. (Communication and Electronics), vol.78, Nov., 1959, pp.457-461.
6. Nisbet,T.R.: Counting pulses within the magnetic hysteresis loop, Control Eng., Nov.,1960, pp.149-151.
7. Freeman,J.D.: New idea in counting:Incrementally magnetized cores, Electronics, June, 1962, pp.40-43.
8. Carter,W.L. and Knoke,P.J.: Unconventional approach to pulse-width measurements, Electronics, vol.35, no.43, Oct., 1962, pp.51-53.
9. Rozenblat,M.A.: Magnetic devices in automatic control and computers, Moscow, 1966 (in Russian).
10. Ho,H.H.: Simple multipulse magnetic counter, Elect.Eng., vol.40, July, 1968, pp.407-409.

11. Ho,H.H.: A multipulse magnetic counter with improved method of storage and counting of pulses, Int.J.Electronics, vol.31, no.3, 1971, pp.265-277.

12. Rozenblat,M.A. and Fedin,G.V.: A multilevel core counter and its use, IEEE Trans.Mag., MAG-9, no.1, Mar., 1973, pp.27-31.

13. Sakurai,Y.: Non-destructive read-out magnetic counter, Annual Meeting of Institute of Electrical Engineers of Japan, 430, 1962.

14. Boole,G.: The Mathematical Analysis Of Logic, Blackwell, 1948.

15. Nakasima,A.: Theory of equivalent transformation of simple partial paths in the relay circuit, J.Inst.Elect.Engrs., no.165 (1936) and no.167 (1937).

16. Shannon,C.E.: A symbolic analysis of relay and switching circuits, AIEE Trans., vol.57, 1938, p.713.

17. Scott,N.R.: Analog and Digital Computer Technology, McGraw-Hill, 1960.

18. Morris,D.J. and Alexander,W.: An introduction to the ternary code number system, Elect.Eng., vol.32, 1960, pp.554-557.

19. Scott,N.R.: Electronic Computer Technology, McGraw-Hill, 1970, p.457,

20. Forrester,J.W.: Digital information storage in three dimensions using magnetic cores, J.Appl.Phys., vol.22, Jan., 1951, pp.44-48.

21. Papian,W.N.: A coincident-current magnetic memory cell for the storage of digital information, Proc.IRE, vol.40, no.4, April, 1952, pp.475-478.

22. Gschwind,H.W.: Design Of Digital Computers, An Introduction, Springer-Verlag, 1967.

23. Rajchman,J.A. and Lo,A.W.: The transfluxor, Proc.IRE, vol.44, no.3, Mar., 1956, pp.321-332.

24. Lambert : Nondestructive readout of matallic tape computer cores, Trans.IRE, vol.EC-8, no.4, Dec., 1959, pp.470-474.

25. Widrow : A radio-frequency nondestructive readout for magnetic core memories, Trans.IRE., Electronic Computer, EC-3, no.4, Dec., 1954, pp.12-15.

26. Buck,D.A. and Frank,W.I.: Nondestructive sensing of magnetic cores, Trans.AIEE, vol.72, Pt-1, Jan., 1954, pp.822-830.

27. Wanlass, and Wanlass : BIAX high speed magnetic computer element, IRE Wescon Conference Record, no.5, Sept/Oct., 1959, pp.46-48.

28. Boutwell, and Conn : The BIAX magnetic element, Datamation, vol.5, no.5, Sept/Oct., 1959, pp.46-48.

29. Newhouse,V.L.: The utilization of domain-wall viscosity in data-handling devices, Proc.IRE, vol.45, no.11, Nov., 1957, pp.1484-1491.

30. Kilburn, and Grimsdale : A digital computer store with very short read time, Proc.IEEE, vol.47, no.11, Nov., 1960, pp.567 -572.

31. Scott,N.R. : Electronic Computer Technology, McGraw-Hill, 1970.

32. Brown,D.R.,Buck,D.A. and Menyuk,N.: A comparison of metals and ferrites for high-speed operation, Trans.AIEE,vol.73, Pt-1, Jan., 1955, pp.631-635.

33. Robert,J.: High Frequency Applications Of Ferrites, section 4.6 : Comparison of ferrite and metallic core, English Language Book Society and English University Press, 1965.