Adiabatic Clock Recovery Circuit

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Abstracts

Power dissipation is a major concern in VLSI design. An adiabatic switching has great potential to achieve low power; numerous designs of this logic have been presented in [1,2,3,4,5]. The main concept of adiabatic switching is to recycle charge stored in nodes or use AC power supply that is varied with logical operations, then the power consumption will be less than CV_{on}^2 per signal transition [6].

All these adiabatic designs present the realization of low power dissipation. However, one problem is usually not taken into concern. Are these adiabatic designs applicable to our daily life? Many adiabatic designs need a complex clocking scheme which is very different from conventional CMOS and need special interface circuits to connect to conventional CMOS.

Among various adiabatic designs, adiabatic quasi-static CMOS (AqsCMOS) logic [7,8] is one that is totally compatible to conventional CMOS. Therefore, it has potential advantages over other adiabatic logic. However, the AqsCMOS has several disadvantages; it requires a rather complex power clock supply and its speed is limited by the frequency of the power clock supply.

AqsCMOS is very suitable for contactless smart card applications. Since, it is feasible to extract the carrier frequency from the smart card¡¦ transmitting signal as power clock supply for AqsCMOS logic using a center tapped RF transformer. Besides, according to smart card system standard ISO 14443, the signal rate of type B interface is 106 kbp/s, therefore the speed limitations of AqsCMOS logic is not a problem here.

Contactless smart card is an important issue nowadays and become a strategic topic for research. Besides, the power consumption limits the complexity of the integrated circuit in smart card. This motivates the application of this logic to smart card.

This project focuses on the development of the AqsCMOS design to evaluate clock recovery circuit used in contactless smart card.

摘要

在超大規模集成電路(VLSI)設計中, 電量消耗是其中一個主要考慮因素。其中絕熱式交遞(adiabatic switching)有很大潛力達到低功率, 所以有很多絕熱式設計提出來[1,2,3,4,5]。他們的主要概念是回收存放在電容裡的電子或者電源是隨著邏輯操作而變化, 使每次的信號改變的電量消耗少於 CV_{on}^2 [6]。

眾多絕熱式設計都顯示能夠達到低功率, 但是一個主要因素不常考慮, 就是這些絕熱式設計是否可適用於我們的日常生活中。許多絕熱式設計是與傳統互補式金氧半電晶體(CMOS)非常不同, 所以需要介面(interface)和傳統互補式金氧半電晶體的邏輯部份交流, 此外亦需要一個複雜時鐘系統。

在各種各樣的絕熱式設計之中, 絕熱近似穩態互補式金氧半電晶體(adiabatic quasi-static CMOS -- AqsCMOS)邏輯 [7,8] 是一個完全與傳統互補式金氧半電晶體邏輯兼容的, 所以與其他絕熱邏輯比相它較優越。雖然與傳統互補式金氧半電晶體邏輯, 它需要較複雜時鐘供應能量及它的速度受時鐘頻率限制。

但 AqsCMOS 是非常適合在非接觸型集成電路卡/(聰明卡)使用,因爲只要使用中央抽頭(center tapped)的 RF 變壓器, 就可從聰明卡的傳送的信號中提取載波頻率, 作爲 AqsCMOS 邏輯的能量供應。 此外, 根據聰明卡系統標準 ISO 14443, B 型介面的信號率是 106 kbp/s, 因此 AqsCMOS 邏輯的速度局限在這裡不是問題了。

非接觸型聰明卡是現今一個熱門研究項目。而能量供應限制了聰明卡裡集成電路的複雜性。 這刺激了利用這邏輯在聰明卡上, 使電量消耗減低從而增加電路的複雜性。

本論文集中評估 AqsCMOS 設計在應用非接觸型聰明卡的時鐘再生潛力。

Acknowledgements

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1. Introduction

1.1. Low Power Design

In recent years, there has been a phenomenal growth in portable communication and computing electronic devices, thus power dissipation is becoming a major concern in VLSI design.

Conventional CMOS is an attractive technology because of its negligible static power dissipation. However, its dynamic power dissipation is equal to $\frac{1}{2}CV^2f$ and this dissipation is unavoidable when it has transition. Conventional approaches to low power design are using smaller transistor size, lower supply voltage and minimize switching activities [9,10].

However, the recent sub-micron technologies have improved speed i.e. higher frequency and complexity of integrated circuit (which is proportional to capacitance). Therefore, the power dissipation dramatically increases due to high frequency and large parasitic capacitance. It becomes harder and harder to reduce power by conventional approaches.

In order to meet the demand of low power operation, we need to focus on reducing dynamic power dissipation. Adiabatic CMOS logic is one approach that can meet this criterion. The main idea of adiabatic switching is to reduce power consumption by recycling charges between the charge and discharge cycle.

1.2. Power Consumption in Conventional CMOS Logic

There are three major source of power dissipation in conventional digital CMOS logic [10]:

1. Static power – it includes power lost by the reverse leakage currents and power consumed in the sub-threshold current region.
2. Dynamic power – it is due to the charging and discharging load and parasitic capacitors.
3. Short circuit power –it is due to short-circuit current (I_{sc}) during switching transient between on and off status.

The total power consumption can be summarized in the following equation:

$$P_{total} = I_{leak} \times V_{dd} + I_{sub} \times V_{dd} + p_t \times C_p \times V \times V_{dd} \times f_{clk} + I_{sc} \times V_{dd} \quad \text{---------- (1.1)}$$

The followings will discuss each component in detail.

The first two terms of equation (1.1) represents the static power dissipation. The total static power mainly consists of two components: the power dissipation P_{leak} contributed from leakage current I_{leak} and the power dissipation P_{sub} arises from sub-threshold current I_{sub}.

I_{leak} : reverse leakage current
I_{sub} : sub-threshold current

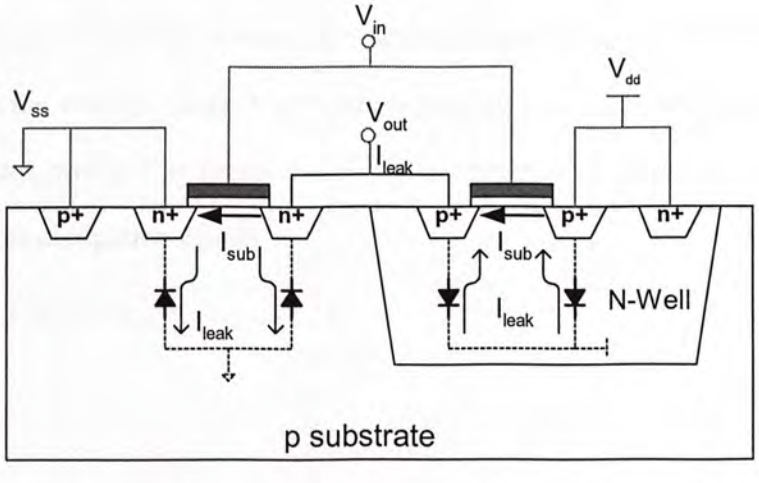


Figure 1.1. : Reverse leakage current and sub-threshold current in inverter

The leakage currents occur when the p-n junctions between the drain and the bulk of the transistor are reverse-biased. The reverse-biased junctions conduct a reverse saturation currents which are drawn form the supply voltage as shown in Figure 1.1.

The total power due to these leakage currents is equal to

$P_{leak} = I_{leak} \times V_{dd}$ ---------- (1.2)

The sub-threshold current is a function of the input voltage. When the gate to source voltage is very close the threshold voltage of the logic gate, the sub-threshold current becomes significant due to the carrier diffusion between the source and drain regions of the transistor.

The total power dissipation is equal to

$P_{sub} = I_{sub\ (mean)} \times V_{dd}$ ---------- (1.3)

The mean value of sub-threshold current is for both pmos and nmos transistors. This current increase drastically with the increase of temperature and this parameter is especially important to charge-storage devices.

The third term represents dynamic power dissipation i.e. the energy dissipates during a switching transition. It is equal to $p_t \times C_p \times V \times V_{dd} \times f_{clk}$, where p_t is the probability that a power consuming transition occurs (the activity factor), C_p is the load and parasitic capacitance, V is the voltage swing, V_{dd} is supply voltage and f_{clk} is the clock frequency. In general, the voltage swing V is same as the supply voltage V_{dd}; therefore, sometime we say the dynamic power dissipation equals

$P_{dynamic} = p_t \times C_p \times V_{dd}^2 \times f_{clk}$ ---------- (1.4)

When a node of a CMOS circuit changes from state "zero" to "one", the load capacitor is charged to V_{dd} via the pmos block. Then it is discharged to ground (gnd) via nmos transistors when the state changes from "one" to "zero".

Take an inverter as an example, the charging and discharging path are as followings:

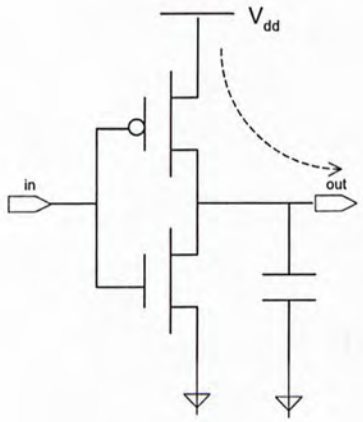


Figure 1.2. : Inverter charging phase

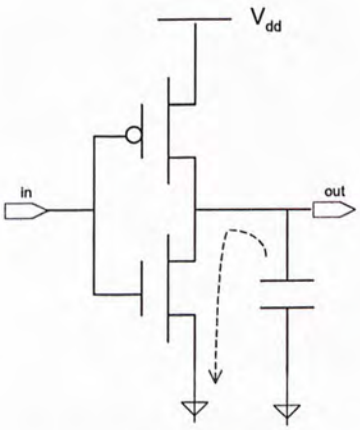


Figure 1.3. : Inverter discharging phase

The energy is consumed to supply this charge at the voltage V_{dd}, so the supplied energy in each transition is $QV_{dd} = C_pV_{dd}^2$. Only half of the energy is stored in capacitor C_p and another half is dissipated in pmos (when charging) or nmos (when discharging).

During charging phase, the output node (out) has a transition from zero to ¡§one¡¤i.e. th output node charges up to V_{dd}. At this status, the pmos is . ono and can be model as a simple resister.

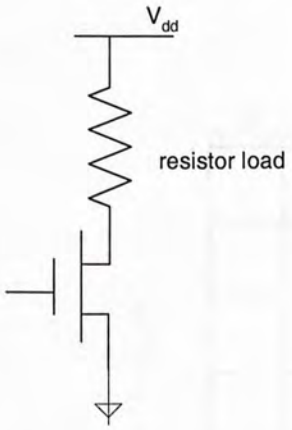


Figure 1.4. : Pmos model as a resistor

Therefore, we can model the charging of the load capacitors with a first order RC circuit as shown in Figure 1.5.

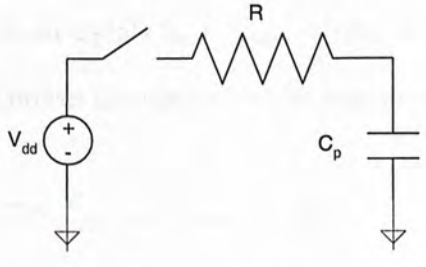


Figure 1.5. : First order RC charging circuit

When the switch is closed, current flows through R and charges C_p towards V_{dd}. The energy taken from the power supply is $C_pV_{dd}^2$. However, half of the energy ($\frac{1}{2}C_pV_{dd}^2$) is stored in C_p and the other half is dissipated in R i.e. pmos.

Similarly, during the discharging phase, the output node makes a transition from ¡§one¡¨ t zero. The energy stored in C_p discharges via nmos and $\frac{1}{2}C_pV_{dd}^2$ energy is dissipated.

The last term of equation (1.1) represents the short circuit power dissipation. There is a short circuit current I_{sc}, which arises when both the nmos and pmos transistors are simultaneously active, conducting current directly form supply (V_{dd}) to ground as illustrated in Figure 1.6. and Figure 1.7.

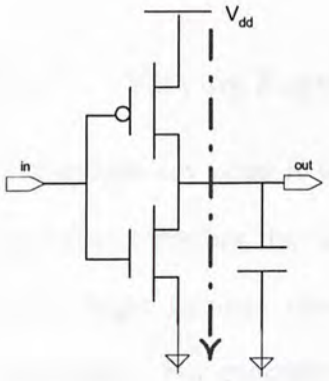


Figure 1.6. : Short circuit current of an inverter

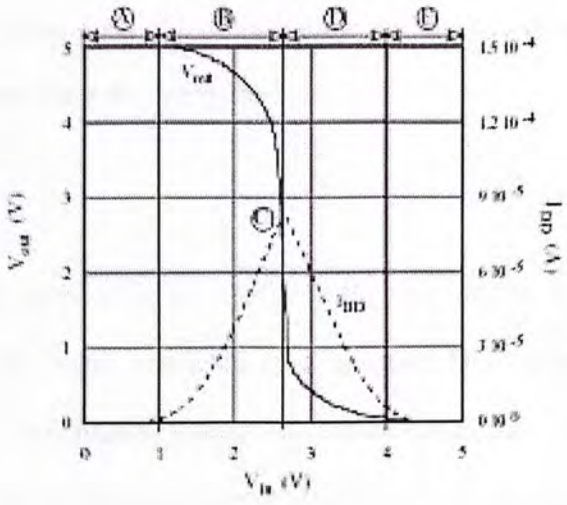


Figure 1.7. : DC transfer curve of an inverter

The short circuit power dissipation equals $I_{sc} \times V_{dd}$. Using an approximated average short circuit current, the short circuit power dissipation can be explained:

$$P_{sc} = \frac{\beta}{2}(V_{dd}{}^2 - 2V_{th})^3 \times \tau \times f_{clk} \quad \text{---------- (1.5)}$$

where β is gain factor of nmos or pmos and assume the same, V_{th} is the threshold voltage (assume equal threshold voltage for pmos and nmos) and τ is rise or fall time of input voltage (assume equal rise and fall time).

1.3. Adiabatic Switching

A new approach of reducing power consumption of CMOS circuit is using adiabatic technique. "Adiabatic" is a term used to describe thermodynamics processes that exchange no heat with the environment in Physics. Main concepts of this methodology are using supply voltage that varies with the logical operations [6] or recycling the electric charge among the nodes of the circuit rather than dissipating the energy as heat.

1.3.1. Varying Supply Voltage

A dominant key point is to lower the voltage drop while the charge is flowing into the load capacitor, therefore the supply voltage is no longer restricted to a constant DC voltage. Many logic families introduced in which the supply voltage is varied with the logic operations. For example, both Efficient Charge Recovery Logic (ECRL) [2,11] shown in Figure 1.8. and 2N-2N2P Logic (2N-2N2P) [12] shown in Figure 1.9. are powered by a varying voltage.

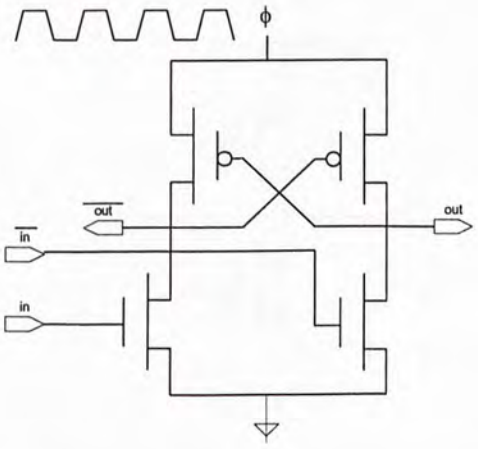


Figure 1.8. : Basic ECRL Gate (inverter)

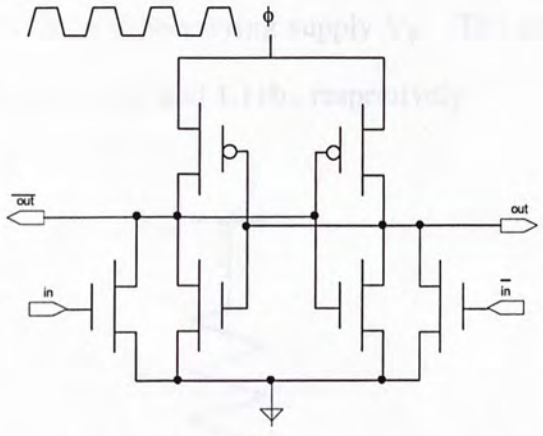


Figure 1.9. : Basic 2N-2N2P Gate (inverter)

In an ideal case, power dissipation can be reduced just by using a linear voltage ramp for power supply, however the rise and fall times of this power supply must be made much longer than the natural RC time constant of the node. T.J. Gabara [13] first illustrated the basis operation of using a linear ramp voltage. He proposed a CMOS circuit using stepwise supply voltage as an alternative choice.

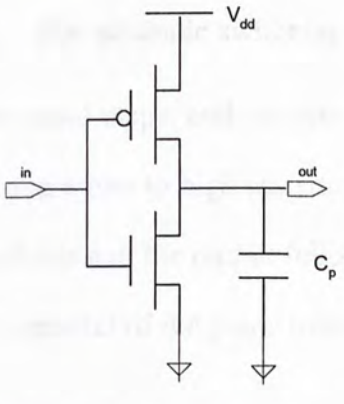


Figure 1.10a. : Conventional inverter

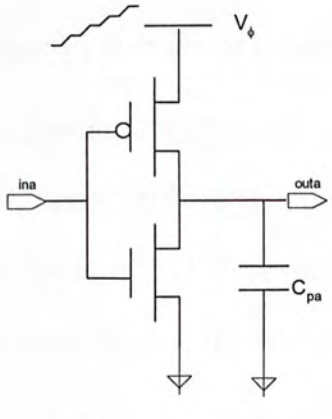


Figure 1.10b. : Adiabatic inverter

Take an inverter as an example, consider an adiabatic CMOS inverter in Figure 1.10b. which is similar to the conventional CMOS inverter s topology; the only difference is the circuit is driven by a time-varying supply V_ϕ. The simplified equivalent charging circuits are shown is Figure 1.11a. and 1.11b., respectively:

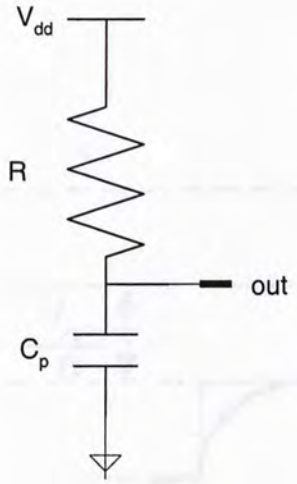


Figure 1.11a. : Conventional inverter equivalent circuit

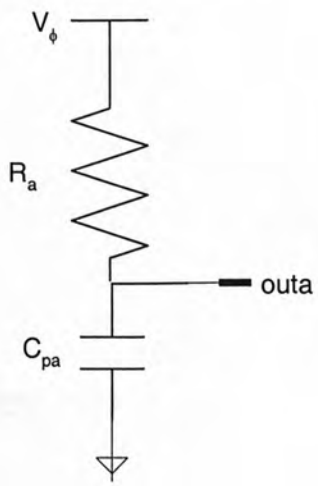


Figure 1.11b. : Adiabatic inverter equivalent circuit

Recall from previous section 1.2., energy dissipated during a charging or discharging cycle is $\frac{1}{2}C_p V_{dd}^{\ 2}$. For adiabatic switching, supply voltage V_ϕ is stepwise increasing from ¡ §zer o to V_{dd} with n equal steps, and assumes the input is making a high to low transition and the output is making a low to high transition. When V_ϕ ramps up from zero potential, the pmos transistor conducts and the output follows the supply voltage. This approach can reduce the drain-source potential of the pmos transistor and the drain current, because the supply voltage is lower.

Consider the equivalent circuit of the inverter, when the supply voltage V_ϕ ramps from zero to V_{dd} as shown in Figure 1.12., the drain current then can be represented as

$$I_a = C_{pa}\frac{\partial V_{outa}}{\partial t} = \frac{V_{i+1} - V_{outa}}{R_a} \quad \text{---------- (1.6)}$$

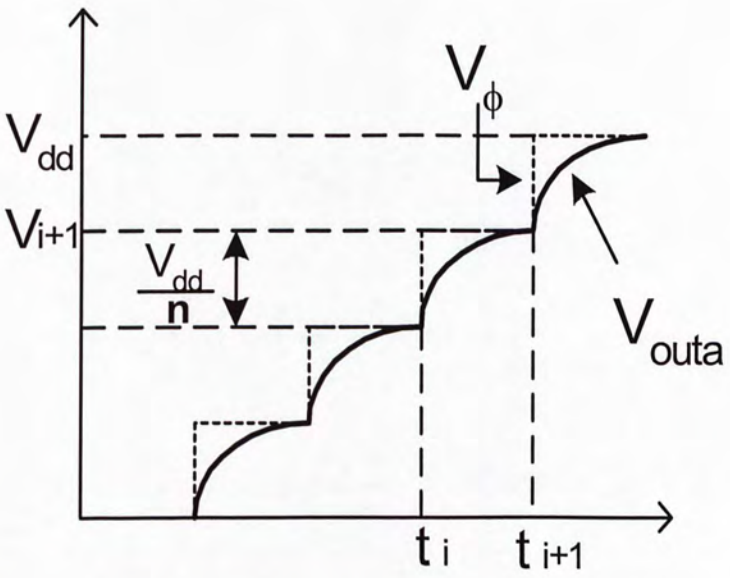


Figure 1.12. : Graph of analysis of ramp voltage supply

Solving the differential equation from $t = t_i$ to time $t < t_{i+1}$, the output voltage becomes

$$V_{outa} = V_{i+1} - \frac{V_{dd}}{n}e^{-\frac{t}{R_a C_{pa}}} \quad \text{---------- (1.7)}$$

where n is the number of steps of the supply voltage V_ϕ .

Then, I_a becomes

$$I_a = \frac{V_{i+1} - V_{outa}}{R_a} = \frac{V_{dd}}{nR_a}e^{-\frac{t}{R_a C_{pa}}}$$

In each voltage step n_i, the dissipated energy is

$$E_{step} = \int_0^{\infty} I_a^{\,2} \times R_a \;\; \partial t$$

$$= \int_0^{\infty} \left(\frac{V_{dd}}{nR_a} \right)^2 e^{-\frac{2t}{R_a C_{pa}}} R_a \;\; \partial t$$

$$= \frac{V_{dd}^{\,2}}{n^2 R_a} \int_0^{\infty} e^{-\frac{2t}{R_a C_{pa}}} \;\; \partial t$$

$$= \frac{V_{dd}^{\,2}}{n^2 R_a} \times \frac{-R_a C_{pa}}{2} e^{-\frac{2t}{R_a C_{pa}}} \Bigg|_0^{\infty}$$

$$= \frac{1}{n^2} \times \frac{1}{2} \times C_{pa} \times V_{dd}^{\,2} \qquad \text{---------- (1.8)}$$

For supply ramping from zero to V_{dd} in n steps, the total energy consumed in charging the capacitance C_{pa} to potential V_{dd} is

$$E_{total} = n \times E_{step}$$

$$= \frac{1}{n} \times \frac{1}{2} \times C_{pa} \times V_{dd}^{\,2} \qquad \text{---------- (1.9)}$$

Compare equation 1.9 with the term $\frac{1}{2} C_p V_{dd}^{\,2}$ the energy dissipation in conventional CMOS. The power dissipation of an adiabatic logic is inversely proportional to the number of steps of the supply voltage. Theoretically the energy dissipation approaches zero if a very slow ramp supply voltage is used, i.e. n tends to infinity.

The adiabatic logic circuits consume low power by trading the operation speed with power consumption. Therefore, adiabatic logic circuits most likely can only apply to applications where speed is not a critical problem.

1.3.2. Charge Recovery

Adiabatic logic also reduces power dissipation by recovering charges stored in the circuit and returning them to the voltage supply. In adiabatic logic circuit, the power supply is implemented with a resonant circuit that can reclaim the electrical energy stored in the capacitor and reuses it in the next cycle. Consider Pass Transistor Adiabatic (PAL) [3] shown in Figure 1.13. as an example, both end of pmos and nmos block are connected to a power clock, it is obviously that charges will return to the power clock during discharging phase.

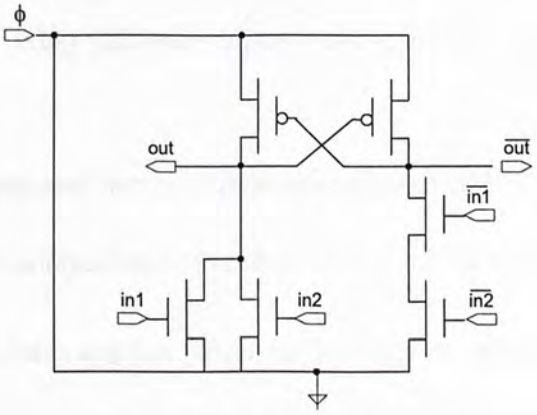


Figure 1.13. : Basic PAL gate

Another example is 2N-2N2D logic [14], the charges is stored in two dummy load capacitors alternately. When node "out" makes a transition to logic "one", it recovers the charges from load capacitor of node "$\overline{out}$".

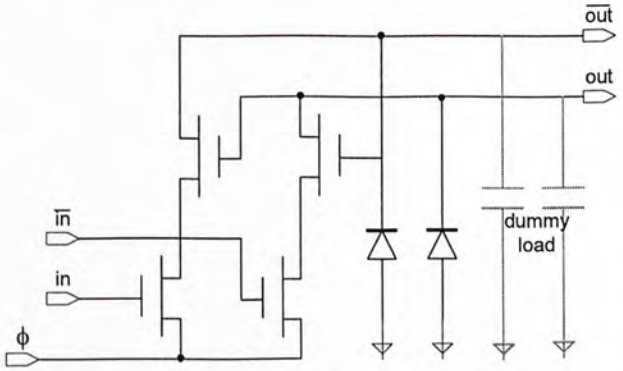


Figure 1.14. : Basic 2N-2N2D gate

2. Adiabatic Quasi-static CMOS Logic

Many adiabatic logic families have been proposed recently [2-5,14]. Most of them require special type of clocking schemes, which are not compatible to conventional CMOS. Interface circuits are required to provide interface to conventional CMOS [15].

Adiabatic Quasi-static CMOS logic (AqsCMOS) is modified from conventional CMOS logic [7,8]. It has many advantages over other adiabatic logic families:

1. The clocking scheme is less complex, it only require a pair of differential sinusoidal clocks, while some other adiabatic logics need complex clocking scheme, such as 4 phases clocks.
2. The topology is simple and very similar to conventional CMOS logic.
3. It is static and totally compatible with conventional CMOS logic, no interface is required.

Moreover, it is fully adiabatic and has power saving property that is independent of the output loading.

2.1. AqsCMOS Logic Building Block

The basic topology of AqsCMOS logic consists of the charging and discharging of parasitic capacitor with a sinusoidal power supply, and special logic devices are used to select the charging or discharging paths.

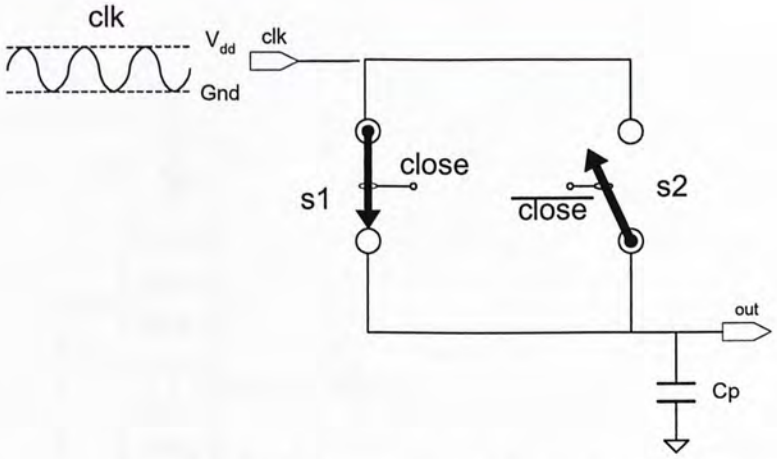


Figure 2.1. : Basic topology of AqsCMOS

As illustrated in above figure, switches s1 and s2 are special devices which only permit current flowing in a single direction as indicated by the arrowhead of the switches. The parasitic capacitor is charged when both of the following criteria are satisfied.

(1). The sine wave input is positive.

(2). The switch s1 is turn on.

When the parasitic capacitor is fully charge, the output is clamped at V_{dd} even the power supply is switching between V_{dd} and ground.

When s2 turn on by the control signal, the output cannot be discharged while the power clock is having a potential higher than the potential of the output. The output will start to discharge when the power clock starts to fall from V_{dd} to ground.

Throughout the whole charging and discharging cycle, no direct path is permitted between supply clock and ground. As a result, energy stored at the parasitic capacitor is completely recovered back to the supply clock. Ideally, no power is dissipated during the signal transition process.

Topology of AqsCMOS logic is illustrated in Figure 2.2. :

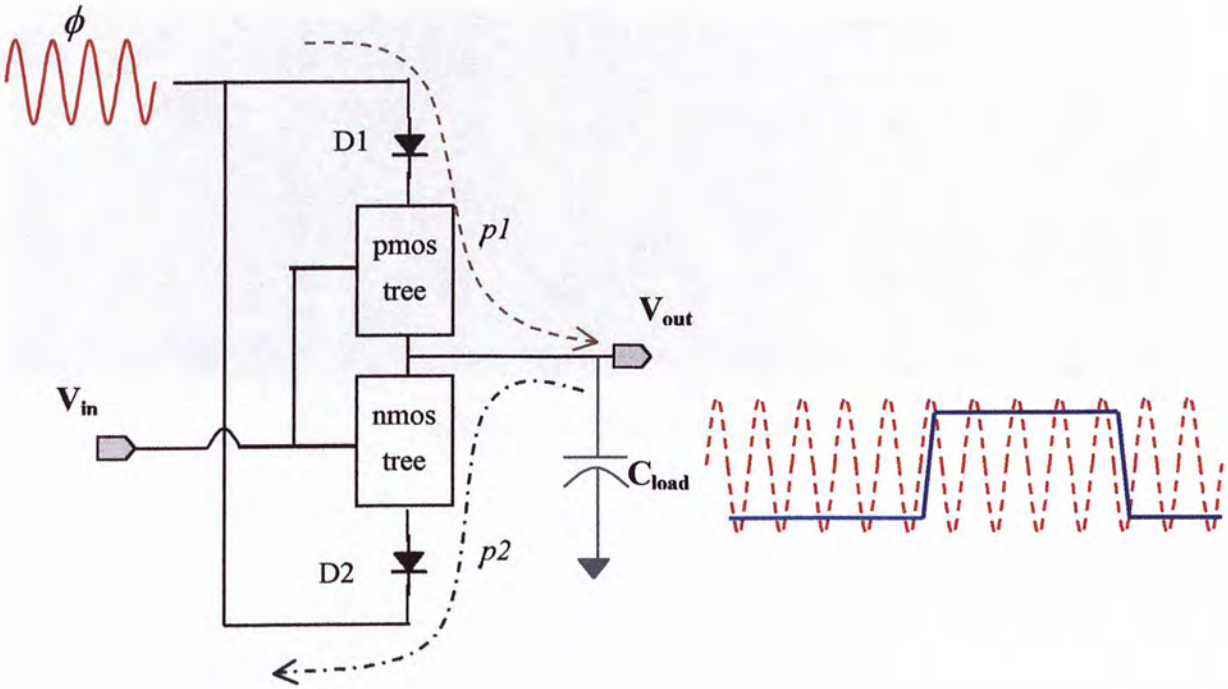


Figure 2.2. : AqsCMOS model

The path between the power clock and the parasitic capacitor is separated into charging and discharging paths. The charging path consists of a "pmos tree" function that is built from basic pmos transistor and a diode. Function "pmos tree" is a monodirectional function. Current can only flow from the clock to the output node following the direction p1 as shown on Figure 2.2.

In contrast, "nmos tree" only permits current to flow from the output node to the power clock. The discharge current can only flow from the output node and back to the power clock in one direction as illustrated by path p2 on Figure 2.2.

One unique characteristic of AqsCMOS logic is the transitions of output is synchronized to the power clock as shown in Figure 2.3. We will utilize this special property to perform clock recovery for this project.

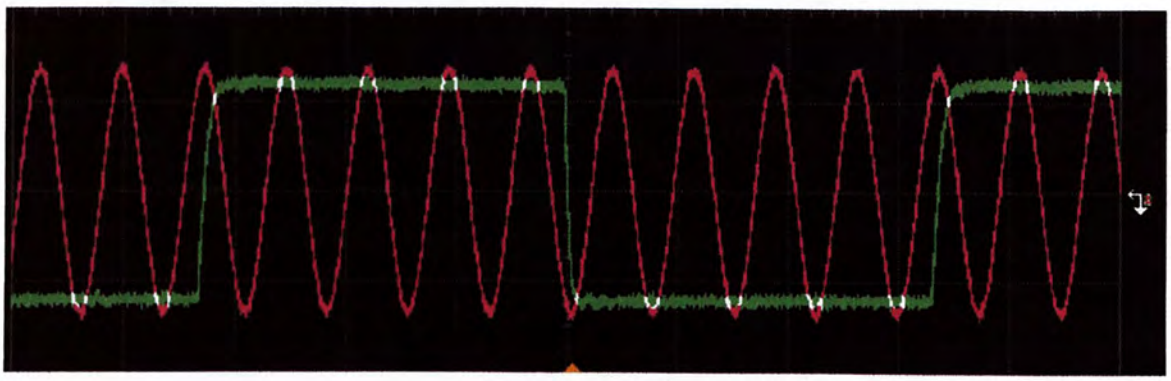


Figure 2.3. : Output transition

2.2. AqsCMOS inverter

The basic building block of AqsCMOS logic is an AqsCMOS inverter as illustrated in Figure 2.4. Diodes D1 and D2 are built by connecting a MOSFET transistor's gate and drain together (CMOS diode).

Both end of pmos and nmos blocks are connected to the power clock ϕ that providing clocking signal and delivering desirable power. The output node "out" consists of a capacitor load which includes all the parasitic and load capacitances.

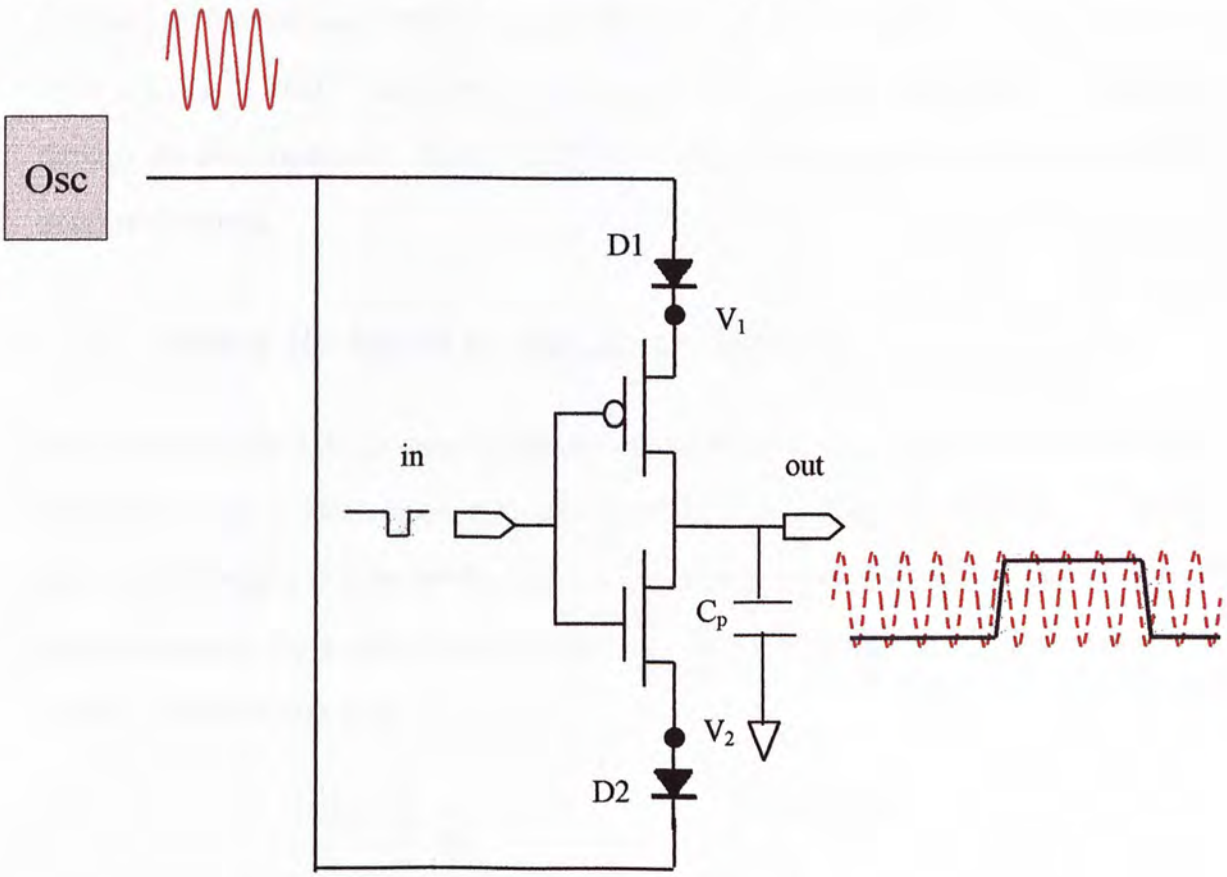


Figure 2.4. : AqsCMOS inverter

Consider the inverter in Figure 2.4., diode D1 and the pmos transistor assemble the charging functional block p1. Diode D1 acts as a current direction barrier. It permits current to flow in one direction from supply source (oscillator) toward node V_1.

When output signal requires a high to low transition, nmos transistor will turn on. Charge stored at the output is transferred to the parasitic node V_2. Potential of V_2 will be built-up. Diode D2 only establishes a forward bias while the potential difference between clock signal and V_2 is smaller than the threshold voltage of D2.

A discharging path is connected between the output node and supply clock. Discharging current transfer all the energy stored at the output node back to the supply clock. In this situation, power only consume by the small resistance of the charging path.

Compare to conventional CMOS inverter, energy dissipation in each charging/discharging cycle is $C_pV_{dd}^2$. Half of the energy is dissipated in pmos and the rest of them is dissipated through the nmos transistor. In AqsCMOS inverter, majority of the charge is recycled back to the power clock.

2.3. Power Reduced in Sinusoidal Supply

Recall from section 1.3.1., power dissipation can be reduced, when the rise and fall times of the power supply is much longer than the natural RC time constant of the node. Consider our case, the supply is a sinusoidal signal. In charging phase, the pmos is closed, current flows through the diode and pmos and charges C_p. It is equivalent to the simplified charging circuit shown in Figure 2.5b.

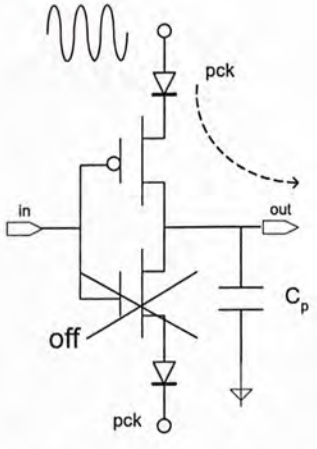


Figure 2.5a. : Charging phase

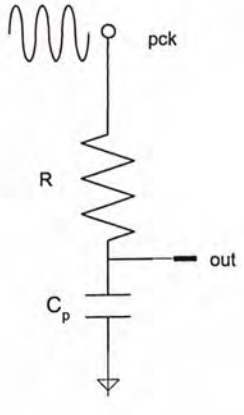


Figure 2.5b. : Equivalent circuit

We assume the charging of the output capacitor C_p is following the rising edge of the sinusoid power clock supply with frequency f_{pck}. The power supply clock is equal to $\frac{V_{dd}}{2}\sin\left(2\pi f_{pck}t-\frac{\pi}{2}\right)+\frac{V_{dd}}{2}$. Assume the charging time is equal to $\frac{T_{pck}}{4}$ period of the power clock supply.

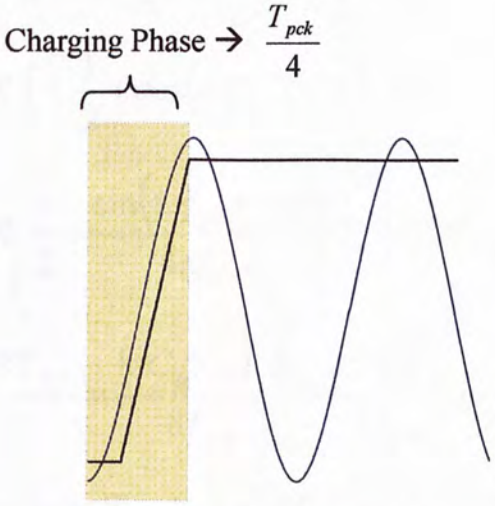


Figure 2.6. : Charging curve

$$I = C_p \frac{\partial V_{out}}{\partial t} = C_p \frac{\partial\left(\frac{V_{dd}}{2}\sin\left(2\pi f_{pck}t-\frac{\pi}{2}\right)+\frac{V_{dd}}{2}\right)}{\partial t}$$
$$= C_p \frac{V_{dd}}{2}\cos\left(2\pi f_{pck}t-\frac{\pi}{2}\right)2\pi f_{pck}$$
$$= \pi f_{pck} C_p V_{dd}\cos\left(2\pi f_{pck}t-\frac{\pi}{2}\right)$$

Energy dissipated during a charging cycle:

$$E = \int_0^{\frac{T_{pck}}{4}} I^2 \times R \ \partial t$$

$$= \int_0^{\frac{T_{pck}}{4}} \left(\pi f_{pck} C_p V_{dd}\right)^2 \cos^2\left(2\pi f_{pck} t - \frac{\pi}{2}\right) \times R \ \partial t$$

$$= \left(\pi f_{pck} C_p V_{dd}\right)^2 R \int_0^{\frac{T_{pck}}{4}} \cos^2\left(2\pi f_{pck} t - \frac{\pi}{2}\right) \ \partial t$$

$$= \left(\pi f_{pck} C_p V_{dd}\right)^2 R \int_0^{\frac{T_{pck}}{4}} \frac{1}{2} + \cos\left(4\pi f_{pck} t - \pi\right) \ \partial t$$

$$= \left(\pi f_{pck} C_p V_{dd}\right)^2 R \left(\frac{t}{2} + \frac{\sin\left(4\pi f_{pck} t - \pi\right)}{4\pi f_{pck}} \Bigg|_0^{\frac{T_{pck}}{4}} \right) = \left(\pi f_{pck} C_p V_{dd}\right)^2 R \left(\frac{T_{pck}}{8} + 0 - 0 - 0 \right)$$

$$= \frac{\left(\pi f_{pck} C_p V_{dd}\right)^2 R T_{pck}}{8} = \frac{\left(\pi C_p V_{dd}\right)^2 R}{8 T_{pck}} = \frac{\pi^2 R C_p}{4 T_{pck}} \times \frac{1}{2} C_p {V_{dd}}^2$$

$$\leq \frac{1}{2} C_p {V_{dd}}^2 \qquad when \ \ T_{pck} \geq \frac{1}{4}\pi^2 R C_p \approx 2.47 \pi^2 R C_p$$

The above equation proved that power dissipation can be reduced, when the rise and fall times of the power supply is much longer than the natural RC time constant of the node. For example, if the inverter is a large buffer and its output capacitor is very large (1 pF). The combine resistance of the pmos and the diode is 0.1 Ω. The sinusoidal power clock is at 100 MHz. Then the energy dissipated during a charging cycle will be

$$E = \frac{\pi^2 R C_p}{4 T_{pck}} \times \frac{1}{2} C_p {V_{dd}}^2 = \frac{\pi^2 \bullet 0.1 \bullet 1 \times 10^{-12}}{4 \bullet 10 \times 10^{-9}} \times \frac{1}{2} C_p {V_{dd}}^2$$

$$= 2.47 \times 10^{-5} \times \frac{1}{2} C_p {V_{dd}}^2$$

Therefore, the energy dissipated by an adiabatic circuit is 40486 times lower then the power dissipated in conventional CMOS, which is $\frac{1}{2} C_p {V_{dd}}^2$.

2.4. Clocking Scheme

In AqsCMOS logic, a differential sinusoidal clocking scheme is used. The power clock is 180° out of phase as shown in Figure 2.7b.

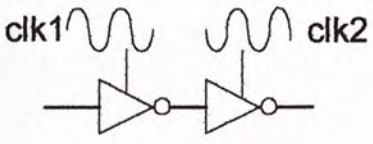


Figure 2.7a. : Pipelined inverters

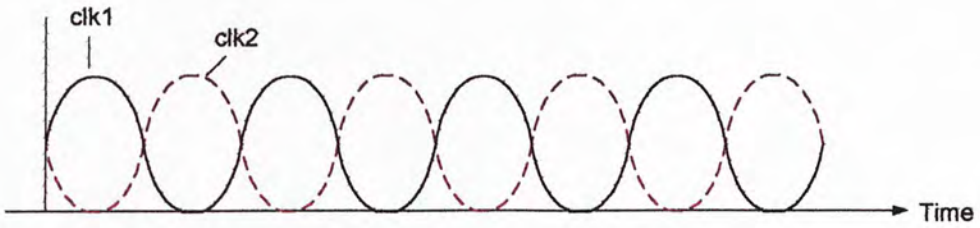


Figure 2.7b. : Clock scheme

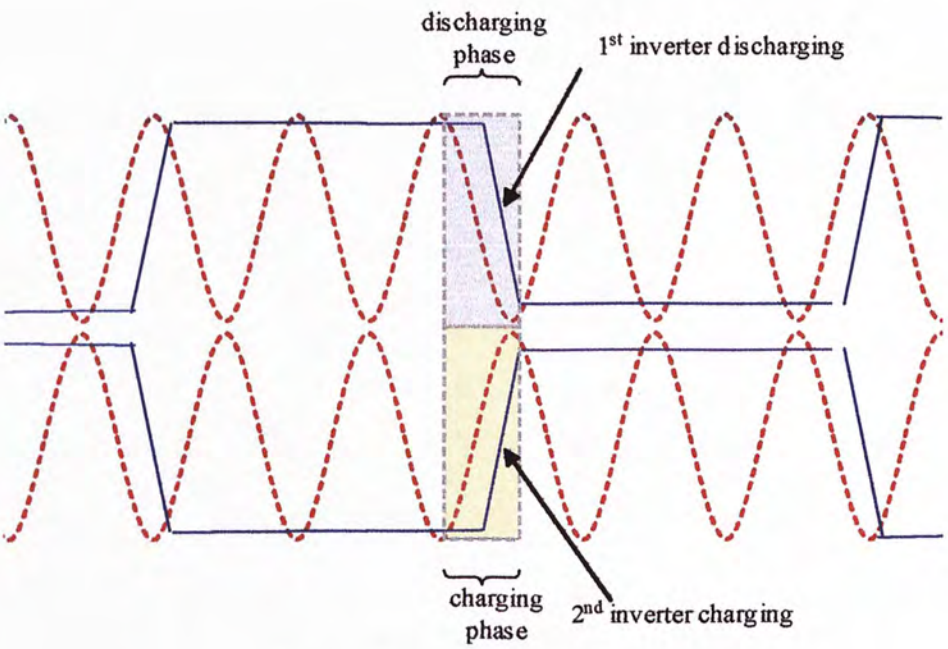


Figure 2.7c. : Output transitions

Consider the case above, when the first inverter is discharging, the second inverter is charging. However, the charging is restricted to the falling edge of the power clock supply. Therefore, the second inverter needs a sinusoid which is 180° out of phase of previous one.

3. Contactless Smart Card

Smart cards represent a new technology that has tremendous potential for enhancing the security of distributed systems, as it offers functions for secure information storage and information processing that relies on VLSI chip technology.

In contactless smart cards, energy and data are transferred without any electrical contact between the card and the terminal [16]. The absence of the contact has a great advantage of easy to use and more convince. Therefore, it has achieved the status of commercial products and is used in various domains in the last few years, for example, banking, telephony, tickets, transport, electronic signatures and identification.

3.1. Architecture

In the operating principles of contactless cards, the techniques used are not new. They have been common knowledge for many years in Radio-Frequency Identification RFID system, which have been used for a variety of applications e.g. animal implants.

In order to be able to communication with the terminal, the contactless card must be satisfied:

1. energy transfer for supplying power to the integrated circuit
2. transmission of the clock signal
3. data transfer to the smart card
4. data transfer from the smart card

Inductive coupling is the most widely used technique for providing both power and communications to the smart card. A simplified diagram of a smart card with an embedded antenna is shown in Figure 3.1.

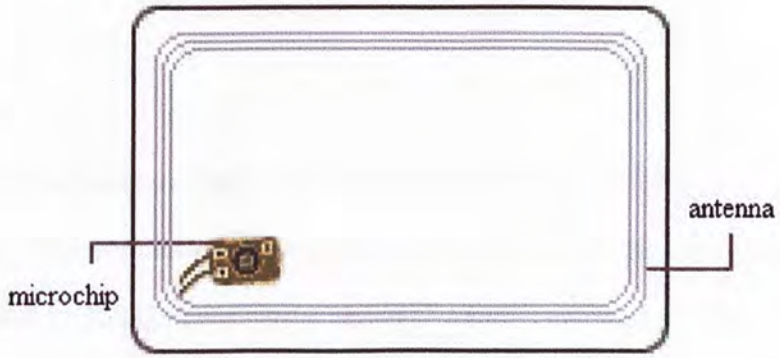


Figure 3.1. : Contactless smart card layout

Typical architecture of a contactless smart card is illustrated in Figure 3.2. :

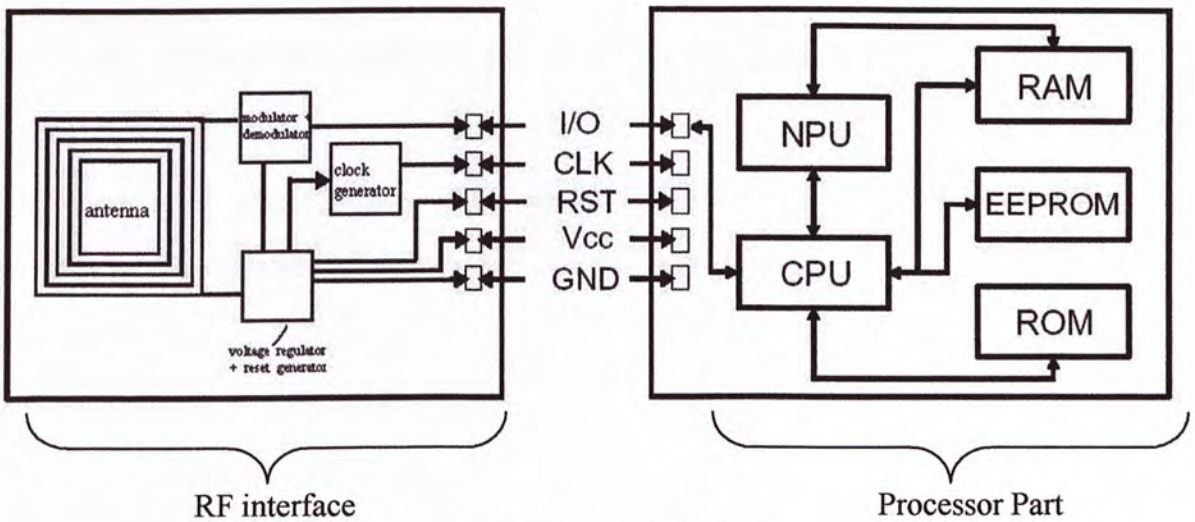


Figure 3.2. : Typical architecture of a contactless smart card

The heart of the chip in smart card is a processor, CPU, which controls the access to the memory and evaluates the security logic. For a more complex security control, processor works together with memory chips with security logic, e.g., carry out encryption.

The processor is surrounded by four additional functional blocks:

1. mask ROM
2. EEPROM
3. RAM
4. an I/O port.

The mask ROM contains the chip's operating system, which is "burned in" when the chip is manufactured. The content of the ROM is thus identical for all the chips of a production run, and it cannot be changed during the chip's lifetime.

The EEPROM is the chip's non-volatile memory. Data and program code can be written to and read from the EEPROM under the control of the operating system.

The Ram is the processor's working memory. This memory is volatile, and all the data stored in it are lost when the chip's power is switched off.

The serial I/O interface usually consists only of a single register, through which data are transferred bit by bit.

As there is no actual contact with terminal, RF interface is required to extract power, communicate with terminal and recover the clock signal.

3.2. Standardization

The perquisite for the worldwide extension of smart cards into every life has been the creation of national and international standards. A smart card is normally one component of a complex system, so the interfaces between the card and the rest of the system must be exactly specified and matched to teach other. ISO standard will be considered.

As early as 1988, an ISO working group was given the task of preparing a standard for contactless smart cards. Their assignment was to define a standard for contactless cards that is largely compatible with the other standards for identification cards. This means that a contactless card can also contain other functional elements, such as a magnetic strip, embossing and chip contacts. This is to allow contactless cards to also be used in existing systems that use other technologies.

Standardization started with "close-coupled" cards (ISO/IEC 10536), since the microprocessors available at that time had relatively high power consumption, and this made energy transfer over relatively large distance impossible. The essential parts of this standard have been completed and approved.

In the meantime, there are two other standards under development, namely ISO/IEC 14443 for "proximity integrated circuit cards" (systems with a working range of around a centimeter) and ISO/IEC 15693 for "vicinity cards" (systems with a working range of up to one meter).

These standards are in turn based on previous ISO standards in the series 7810, 7811, 7812 and 7813, which define the characteristics of identification cards in the ID-1 format.

All the standards are described summarily in the following.

1. ISO 7810 identification cards physical characteristics of credit card size document

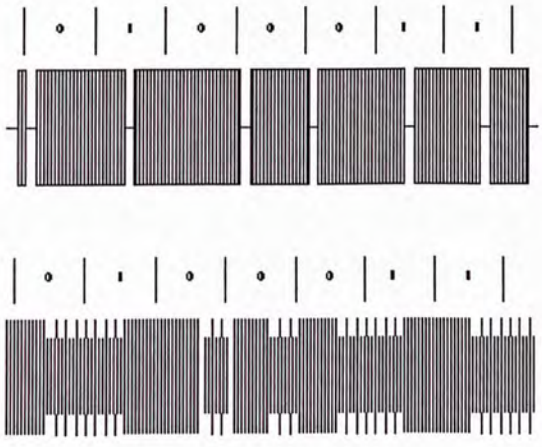
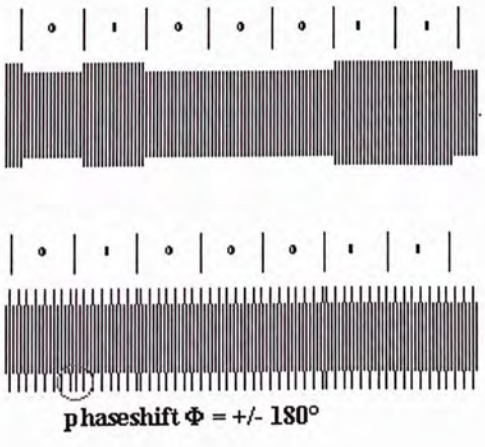
2. ISO 7811 identification cards recording technique
   i. Part 1 : embossing
   ii. Part 2 : magnetic stripe
   iii. Part 3 : location of embossed characters on ID-1 cards
   iv. Part 4 : location of read-only magnetic tracks - track 1 and 2
   v. Part 5 : location of read-write magnetic track - track 3
   vi. Part 6 : magnetic stripe high coercivity

3. ISO 7812 identification cards identification of issuers
   i. Part 1 : numbering system
   ii. Part 2 : application and registration procedures

4. ISO 7813 identification cards financial transaction cards

5. ISO 10536 identification cards contactless integrated circuits cards close-coupled cards
   i. Part 1 : physical characteristics
   ii. Part 2 : dimensions and location of coupling areas
   iii. Part 3 : electronic signals and reset procedures
   iv. Part 4 : answer to reset and transmission protocols

6. ISO 14443 identification cards contactless integrated circuits cards proximity cards
   i. Part 1 : physical characteristics
   ii. Part 2 : radio frequency power and signal interface
   iii. Part 3 : initialization and anticollision
   iv. Part 4 : transmission protocols

common parameters	power supply: 13.56 MHz, inductive coupling field strength: 1.5 7.5 a/m
Type A 	Downlink: ASK 100 %, Modified Miller Code, 106kb/s Uplink: load modulation with 846 kHz sub-carrier, ASK-modulated, Manchester Code, 106 kb/s Anticollision: Binary Search Tree
Type B 	Downlink: ASK 10 %, NRZ Code, 106kb/s Uplink: load modulation with 846 kHz sub-carrier, BPSK modulated, NRZ Code, 106 kb/s Anticollision: Slotted Aloha

7. ISO 15693 vicinity cards

   i. Part 1 : physical characteristics

   ii. Part 2 : radio frequency power and signal interface

   iii. Part 3 : anticollision and transmission protocol

   iv. Part 4 : extended command set and security features

power supply	13.56 MHz, inductive coupling 1.5 1 7.5 a/m field strength
downlink (data transmission reader > card)	modulation: 10% or 100% ASK bit coding: 1 out of 256 or 1 out of 4 baud rate: 1.65 kb/s or 26.48 kb/s
uplink (data transmission card > reader)	modulation: load modulation with sub-carrier bit coding: Manchester, the sub-carrier is ASK (423 kHz) or FSK (423 / 485 kHz) modulated baud rate: 1.65 kb/s or 26.48 kb/s

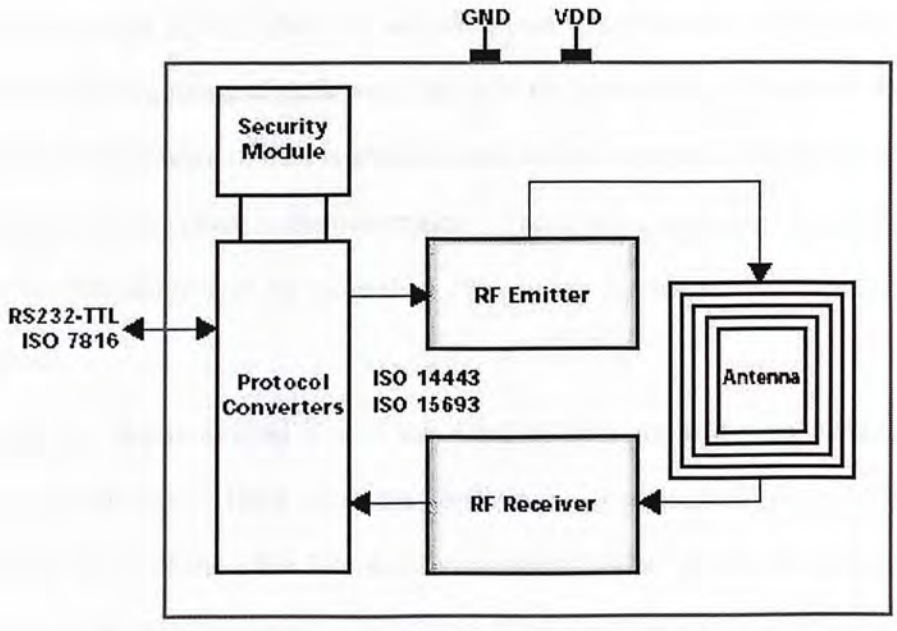


Figure 3.3. : Summary of ISO standards in contactless smart card

3.3. Universal Asynchronous Receiver and Transmitter (UART)

Contactless smart cards communicate with the terminal – smart card interface device via a serial channel. The protocol used for serial communications is a half-duplex one. The communication channel is a single, shared line that enables either party to transmit or receive data. However, both parties may not transmit data simultaneously.

In contactless smart cards, as absence of the contact, it cannot share a clock signal between the sender and receiver and synchronous communications not support. Instead, the sender and receiver must agree on timing parameters in advance and special bits are added to each word, which are used to synchronize the sending and receiving units, the words "Asynchronous Serial Transmission" are used to describe this kind of communication. Then the receiver can sample the signal on the serial line at the same rate as the transmitter sends it in order for the correct data to be received. This rate is known as the bit rate or baud rate.

When a word is given to the UART for asynchronous transmissions, a bit called the "Start Bit" is added to the beginning of each word that is to be transmitted. The Start Bit is used to alert the receiver that a word of data is about to sent, and to force the clock in the receiver into synchronization with the clock in the transmitter. These two clocks must be accurate enough to not have the frequency drift by more than 10% during the transmission of the remaining bits in the word.

After the start bit, the individual bits of the word of data are sent with sending the least significant bit (LSB) first. Each bit in the transmission is transmitted for exactly the same amount of time as all of the other bits and the receiver "looks" at the I/O at approximately halfway through the period assigned to each bit to determine if the bit is a "1" or a "0".

For example, if it takes two seconds to send each bit, the receiver will examine the signal to determine if it is a "1" or a "0" after one second has passed, then it will wait two seconds and then examine the value of the next bit, and so on.

How to implement this in hardware? A clock, which is much faster than the bit rate, is used to examine the signal. For example, a clock that is four times faster than the bit rate and it is counting from 1 to 4 and repeat. The receiver only looks at the signal when count 3, then it sure looking at the I/O at approximately halfway through the period assigned to each bit.

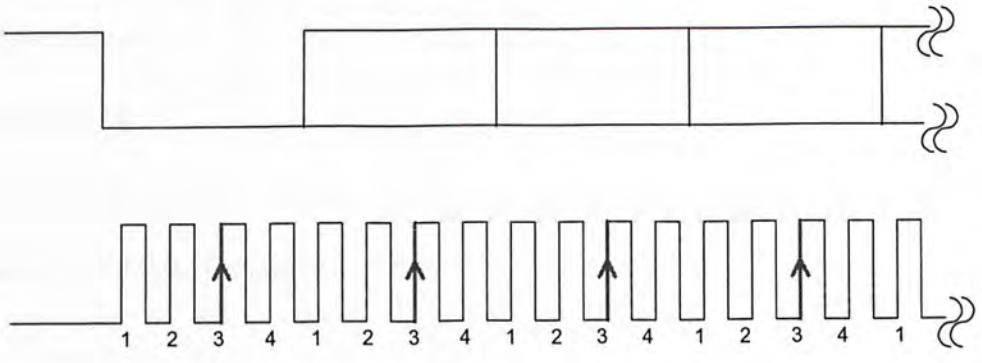


Figure 3.4. : Signal and clock

When the entire data word has been sent, the transmitter may add a parity bit that the transmitter generates. The parity bit may be used by the receiver to perform simple error checking. Then, at least one stop bit is sent by the transmitter.

When the receiver has received all of the bits in the data word, it may check for the parity bits, and then the receiver looks for a stop bit. If the stop bit does not appear when it is supposed to, the UART considers the entire word to be garbled and will report a framing error to the host processor when the data word is read.

The following waveform illustrates a typical serial byte transmission:

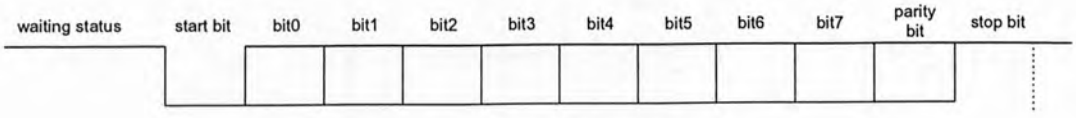


Figure 3.5. : Serial byte

Typically, the UART is connected between a central processor and a serial device. It has a transmitter section and a receiver section. The transmitter converts the bytes into a serial stream of data bits as they are prepared for transmission.

The receiver takes the incoming stream of bits and groups them into 8-bit chunks so they can be reconstructed as bytes. A buffer is also used to temporarily hold incoming data.

A typical UART architecture consists of the following blocks:

1. Transmit Block
2. Receive Block
3. Control Logic
4. Clock & Baud Rate Generator

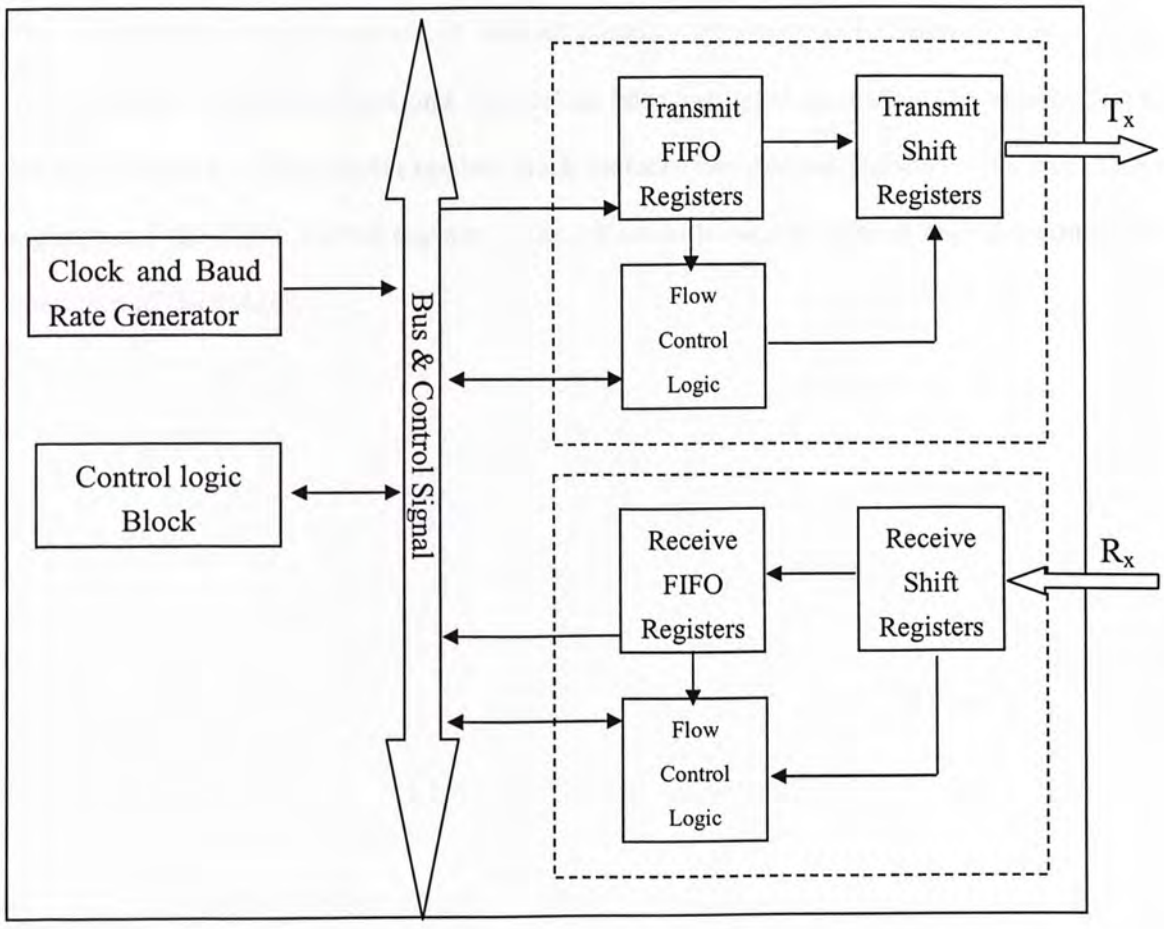


Figure 3.6. : Typical architecture of UART

The transmit block includes the Transmit Holding Register (THR), Transmit Shift Register (TSR), Transmit FIFO Register (TFR) and Transmit Flow Control Logic. Whenever the CPU writes parallel data into the THR. Data is shifted out serially from the TSR.

The receive block includes the Receive Buffer Register (RBR), Receive Shift Register (RSR), Receive FIFO Register (RFR) and Receive Flow Control Logic. Whenever the Receiver Shift Register has received a complete character, it is immediately transferred to the RBR or to the RFR. The CPU reads parallel data either from the RBR or from the RFR depending upon the mode of operation.

The control logic block consists of two sub-blocks – "Select" and "Control" logic blocks. They decode the address lines and chip select lines and generate enables to various UART internal registers. The register control block includes two control registers – the line control register and the FIFO control register. The bit set in these two control registers control the operation of the UART.

4. Clock Recovery

Adiabatic logic has significant advantage in reducing power and achieves the key criterion of the contactless smart card. Among the adiabatic logic families, AqsCMOS is most suitable for smart card application, as it is simple, compatible to the conventional CMOS and requires less complex clock scheme.

For general digital circuit applications, AqsCMOS requires an additional analog oscillator to generate differential sinusoid for the power clock. However, for smart card applications, the sinusoid power clock can be obtained from the RF carrier using a center tapped RF transformer. Moreover, according to smart card system standard ISO 14443, the signal rate of type B interface is 106 kbp/s, therefore the speed limitations of AqsCMOS logic is not a problem here.

4.1. Adiabatic Ring Oscillator

In a serial data transfer between the contactless smart card and the terminal, an oscillator is required to generate high frequency clock for both TFR and RFR (mention in UART in previous section) – shift register to convert data into serial data format or to receive serial data spring. In simplest case, ring oscillator can be used to satisfy this purpose. The ring oscillator is triggered with the negative edge of the start bit and stop after a fixed number of internal clock pulses. The ring oscillator is designed to synchronize to the start bit.

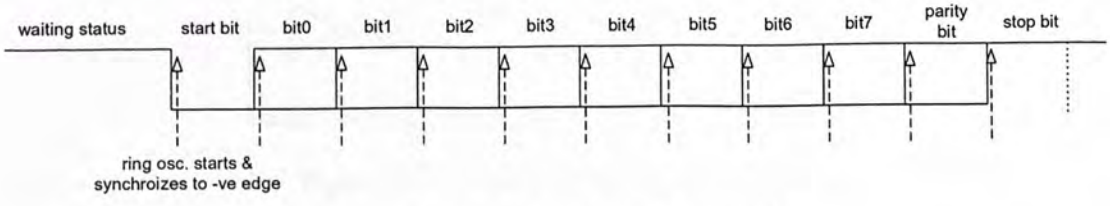


Figure 4.1. : Synchronize to the start bit

In AqsCMOS logic, all the output transitions are limited to the rising and falling edges of the power clock supply. A 'seven' stages AqsCMOS shown in Figure 4.2 is used to evaluate the performance of the oscillator.

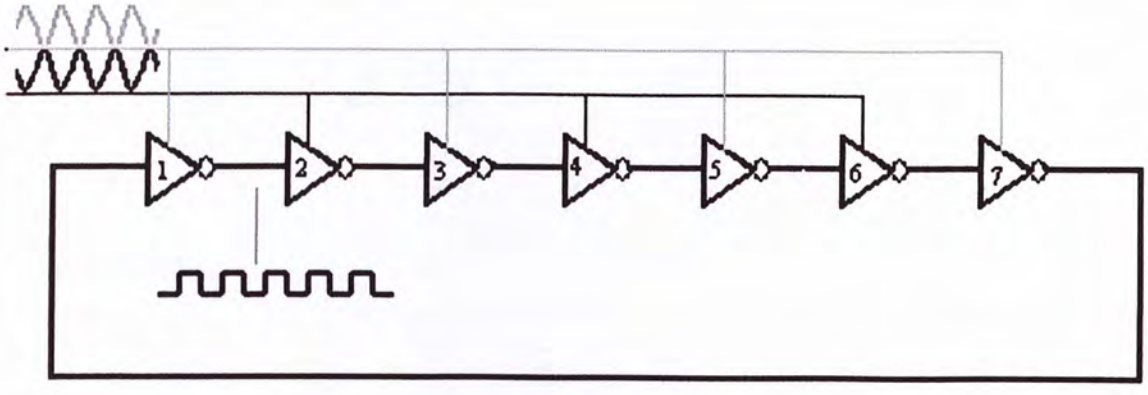


Figure 4.2. : AqsCMOS ring oscillator

In AqsCMOS ring oscillator, alternated inverter is power by one of the differential power clock as illustrated in Figure 4.2.

In our example, 1st, 3rd, 5th and 7th inverters share the same sinusoid power clock, while 2nd, 4th and 6th inverters use the other 180° out of phase sinusoid power clock. Obviously, the first and last inverted are pipelined but share the same clock.

These pipelined inverters using same clock will affect the throughout of the system. Consider this node as the start point, the critical time is when signal pass through the delay path of the ring and back to the start point as illustrated in Figure 4.3.

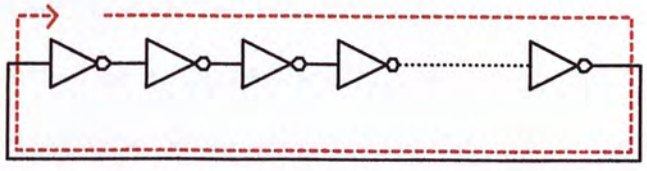


Figure 4.3. : Ring oscillator delay path

The AqsCMOS ring oscillator will not function properly if the total delay of the ring oscillators is less than one and a half of the period of the power clock as illustrated in Figure 4.4.

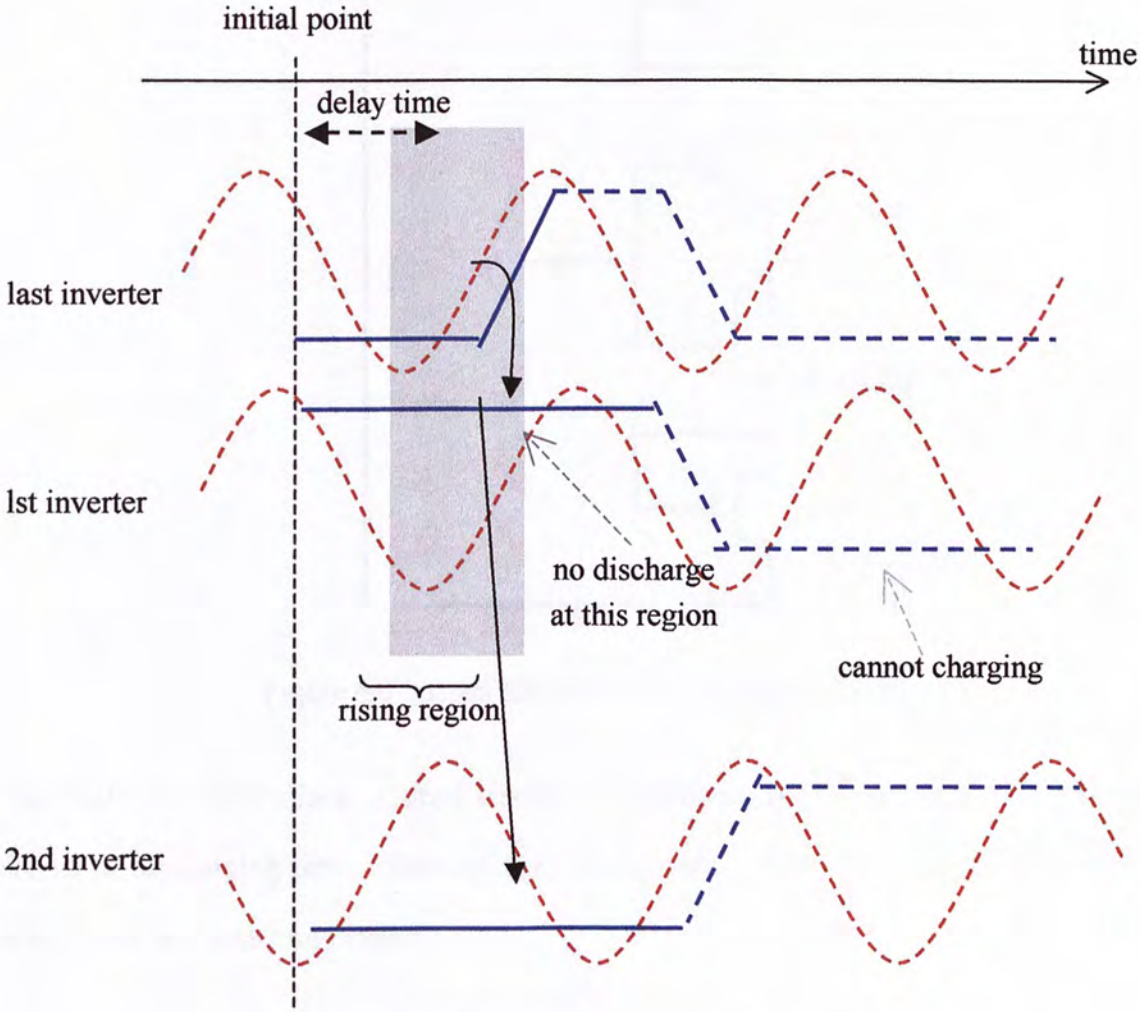


Figure 4.4. : Timing curve by short delay

The top trace illustrated the last inverter is switching from low to high. However, the power clock is still at high, thus the first inverter cannot discharge right away. The first inverter has to wait until the power clock return to low before it can discharge. This condition will cause a timing error.

A schematic diagram of an AqsCMOS inverter used in the ring oscillator is illustrated in below, we use smaller pmos and nmos to increase the propagation delay :

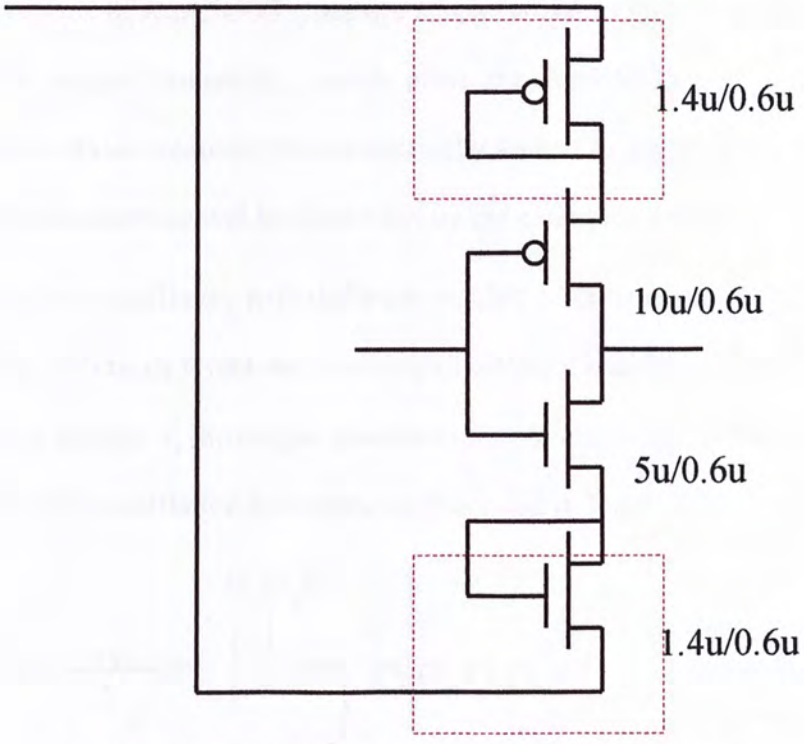


Figure 4.5. : AqsCMOS inverter in ring oscillator

A smallest size MOS diode is used instead of traditional p-n junctions diode to increase charging or discharging time. Besides, the leakage current of MOS diode is smaller and the output signal becomes more stable.

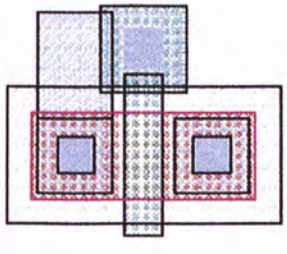


Figure 4.6. : Layout of a nmos diode

4.2. Special Frequencies of AqsCMOS Ring Oscillator

The output transitions of AqsCMOS gates are synchronized to the rising and falling edges of the power clock supply (sinusoids), which gives the AqsCMOS ring oscillator a unique property. The oscillator frequency is automatically locked to the power clock supply. The principle of this characteristic will be illustrated by the examples below.

In a conventional ring oscillator, with different number of inverters in the oscillator, the total propagation delay will be different and resulting in different oscillating frequency. However, in AqsCMOS ring oscillator, the output transitions are synchronized to the power clock and it is not a function of the oscillation frequency as illustrated in Figure 4.7.

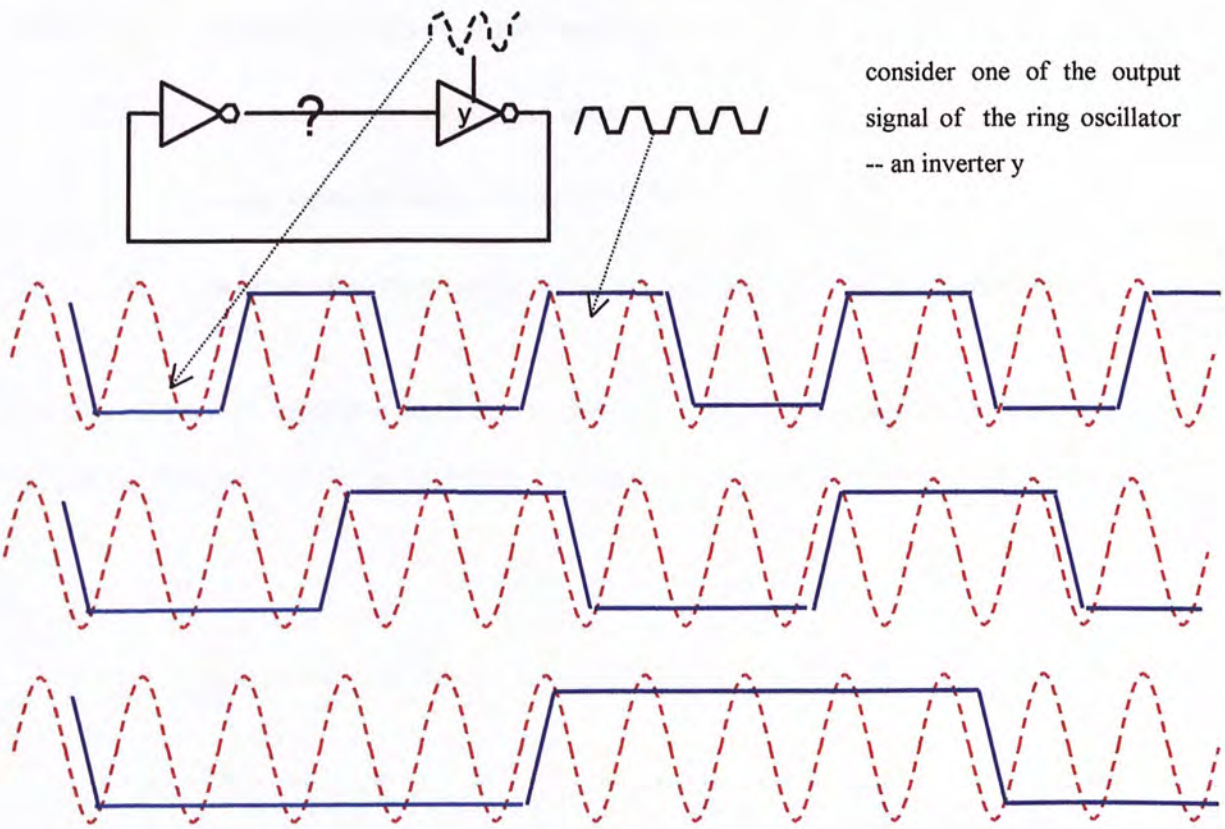


Figure 4.7. : Power clock and different oscillator frequencies

Consider the three examples above, all the transitions follow the power clock. As a result, the frequency of the oscillation will be the frequency of the power clock sinusoid divided by 3, 5 or 7. In contactless smart card example, 13.56 MHz sinusoid will be used for power clock supply, and then the resulting frequency will be 4.52 MHz, 2.712 MHz, 1.937 MHz and so on.

The Mathematical expression of the output frequency of the oscillator in terms of delays and power clock supply frequency is as follow.

$$f_{osc} = \frac{f_{pck}}{2 \times [t_{pd} \times f_{pck}]_u}$$

where f_{osc} is output frequency of the oscillator

f_{pck} is power clock supply frequency

t_{pd} is propagation delay of ring oscillator

$[\cdot]_u$ is function to take number in [] ceiling to m = n + 0.5 (n is an integer)

Consider the UART problem discussed in previous section, a faster clock is required, in order to sample the signal on the serial line and obtain the correct data as illustrated in Figure 4.8.

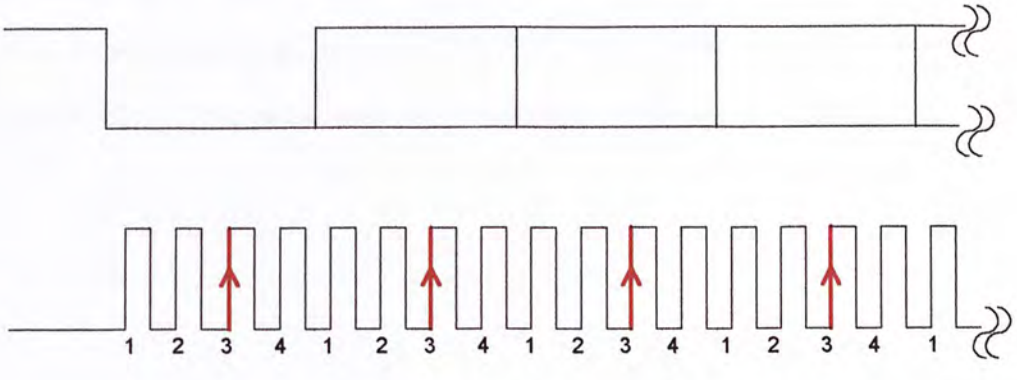


Figure 4.8. : Sampling waveform of an UART

Using contactless smart card with 13.56 MHz carrier frequency and 106 kb/s data rate as an example, we power the AqsCMOS ring oscillator with the 13.56 MHz RF carriers. The oscillation frequency is set at 1/9 of the power clock that is equals to 1.51 MHz. The oscillation frequency is about 14 times faster than the 106 kb/s data. A 14 stages counter is used that samples the serial line at each of the 7^{th} count. The simulation result of this principle is demonstrated at appendix IV.

4.2. Power Extraction

In contactless smart card, power must be obtain from the transmitting signal through antenna as shown in Figure 4.9.

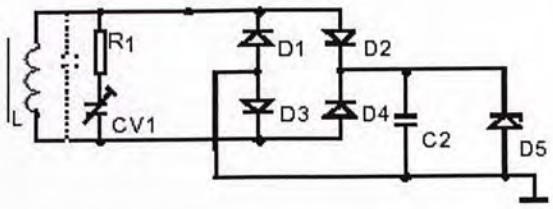


Figure 4.9. : Common power extraction circuit for smart card

Since the coupling between the coil at the terminal and the card is very weak, the efficiency of getting rectified voltage through antenna is low; therefore the power of the card is limited. In AqsCMOS logic, we do not need a rectified DC voltage to power the AqsCMOS circuits. However, we still need to generate a rectified DC voltage for substrate bias which consumes negligible power. Thus using AqsCMOS will improve the power budget of smart card.

As discussed in previous section, AqsCMOS require differential power clock. A simple method to generate a differential power clock signal from the RF carries is illustrated in Figure 4.10.

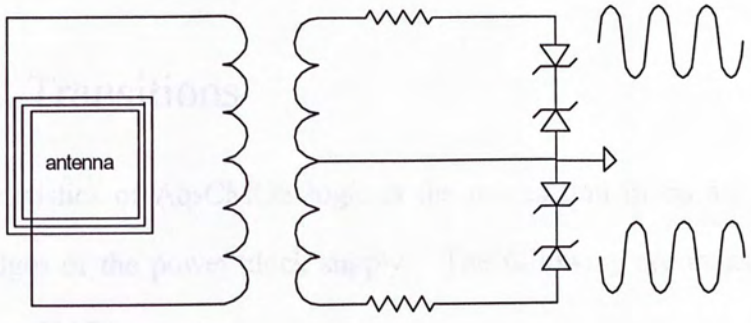


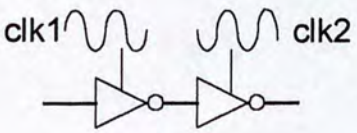
Figure 4.10. : Circuit for extracting differential sinusoid signals form RF carriers

5. Evaluations and Measurement Results

We have designed and fabricated an AqsCMOS ring oscillator, the measurement results are presented in this chapter.

5.1. Output Transitions

One of the characteristics of AqsCMOS logic is the output transitions are synchronized to rising or falling edges of the power clock supply. The following are measurements of two series connected AqsCMOS inverters.



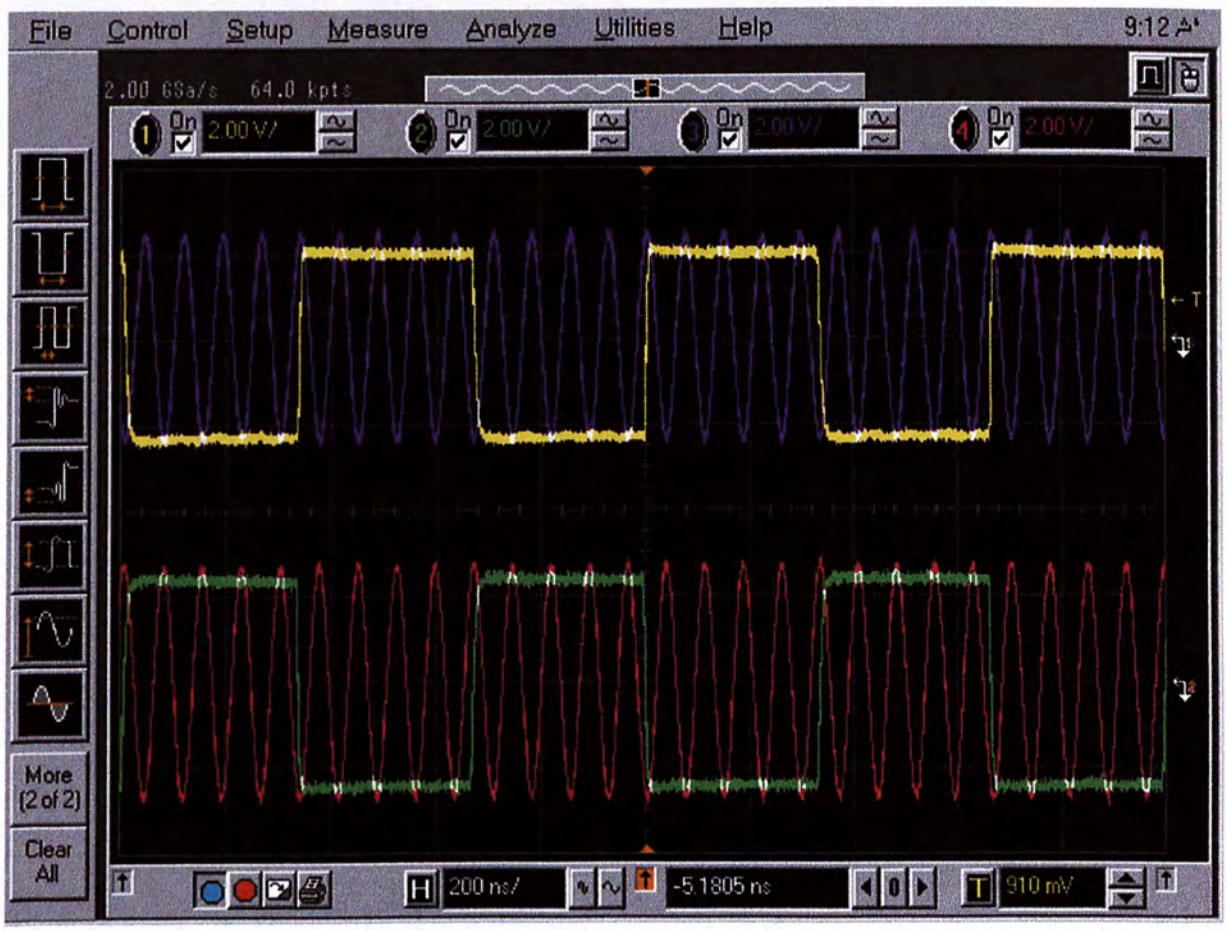


Figure 5.1. : Measured waveforms of two series connected inverters

5.2. Ring Oscillator

A 13.56 MHz of RF carriers of contactless smart card is chosen as the power for the AqsCMOS oscillator. Since the output transitions are synchronized to the rising and falling edges of the power clock, the oscillating frequency will be locked to the frequency relate to the RF carriers. Figure 5.2. is the measurement result of a 39 stages AqsCMOS ring oscillator, oscillating at 1.51 MHz with a power clock signal of 13.56 MHz.

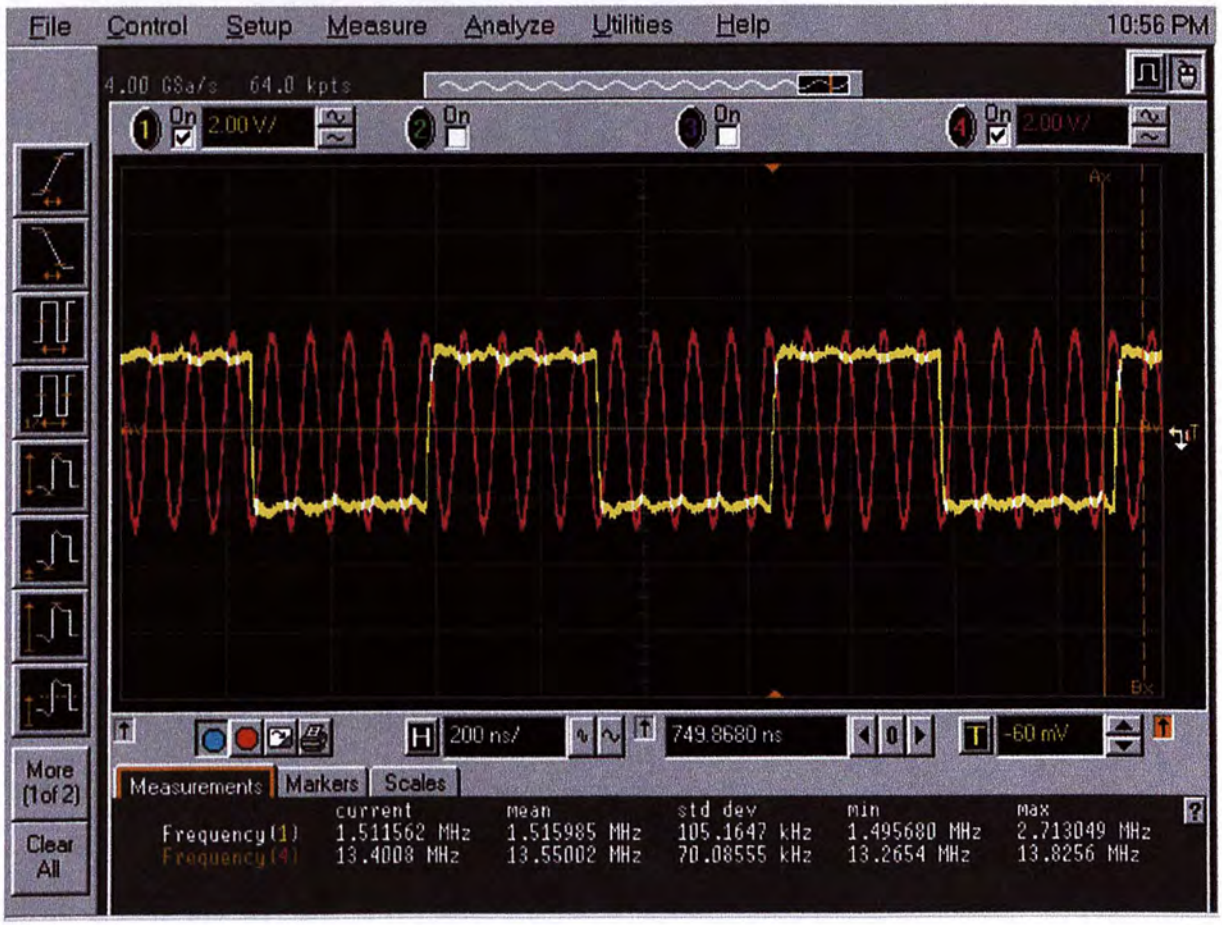


Figure 5.2. : Measurement results

We also investigate the performance of the ring oscillator with temperature change using simulation. Figure 5.3. illustrates the layout of a 21 stages ring oscillator.

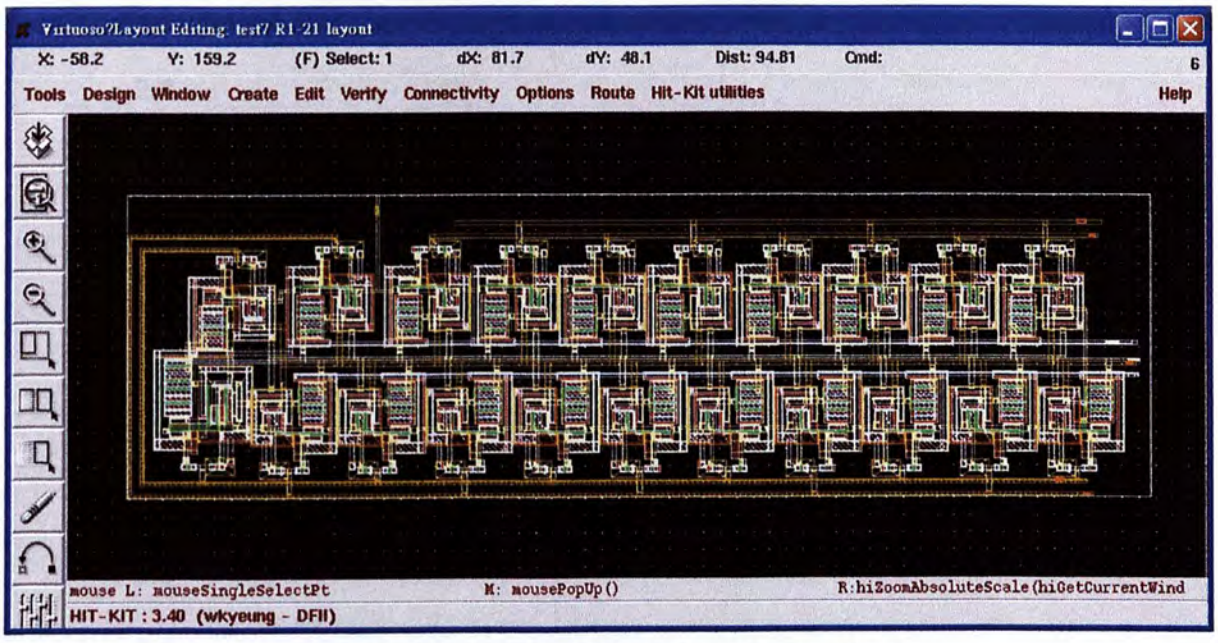


Figure 5.3. : Layout of 21 stages ring oscillator

We have simulated the oscillator form 20 °C to 246 °C. Figure 5.4. shows the outputs of the oscillator at different temperatures. The test results demonstrate that the oscillator is extremely stable.

Unlike conventional CMOS ring oscillator which is very sensitive to temperature variation. The reason for the small temperature sensitivity is because of the output transitions are synchronized to the power clock.

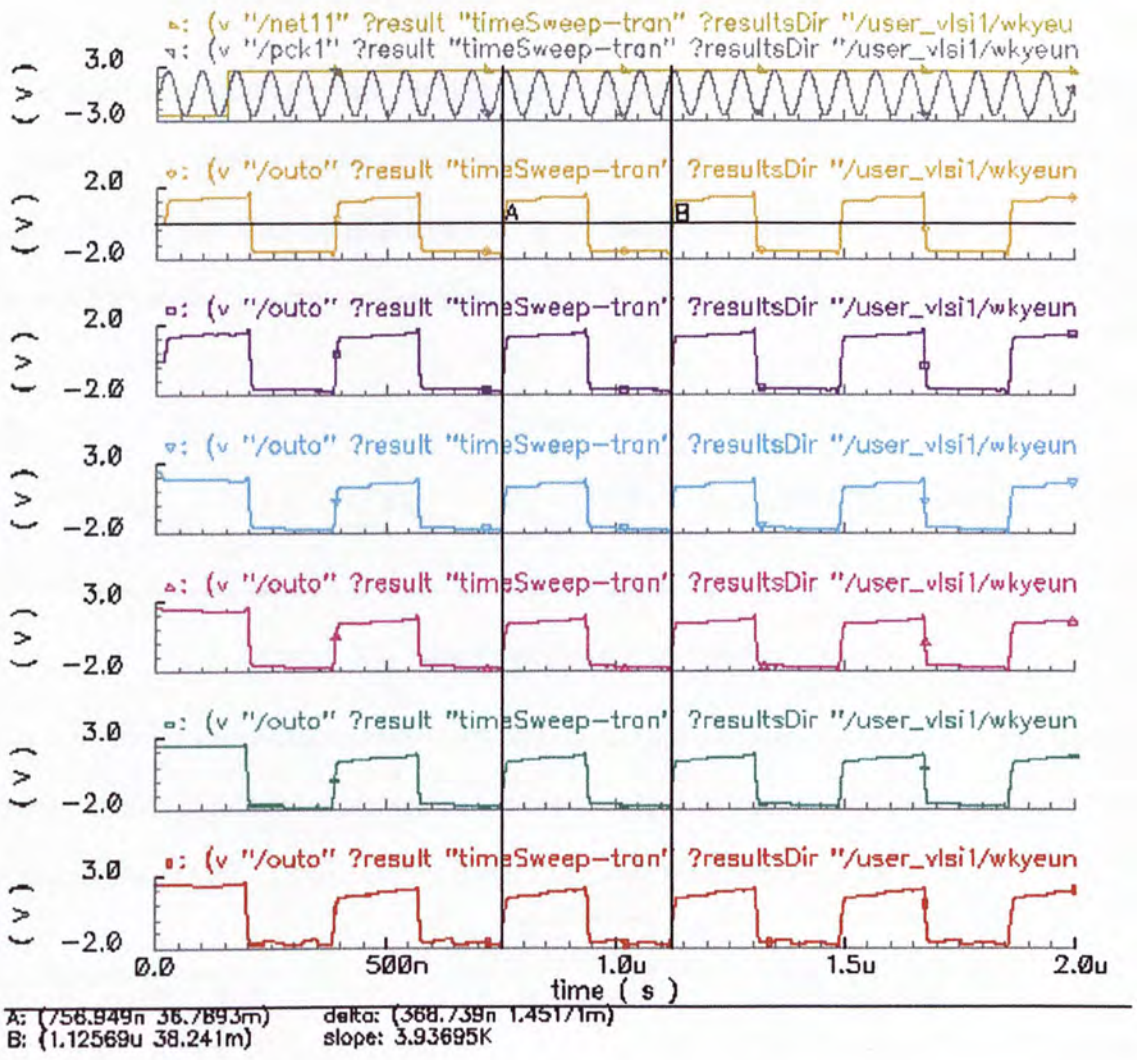


Figure 5.4. : Results with different temperatures

1st trace : power clock supply

2nd trace : oscillator output at 20 °C

3rd trace : oscillator output at 50 °C

4th trace : oscillator output at 100 °C

5th trace : oscillator output at 150 °C

6th trace : oscillator output at 200 °C

7th trace : oscillator output at 246 °C

5.3. Synchronization

The designed ring oscillator with "enable" signal is shown in Figure 5.5. A negative edge of the "start bit" is used together with some control logic to enable / disable the oscillator. Synchronization can then be implemented by connecting the two chips together. Referring to Figure 5.6., chip 1 is a transmitter and chip 2 is the corresponding receiver.

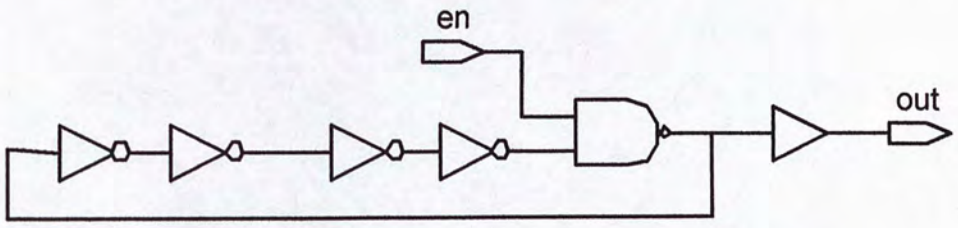


Figure 5.5. : Ring oscillator with "enable" input

Figure 5.6. shows the measurement setup to evaluate the clock recover circuit. We assume a 5V pulse enable signal is connected to the enable input of Figure 5.5. after the "start bit" is detected by the UART. This verifies if the clock will synchronize to the "start bit".

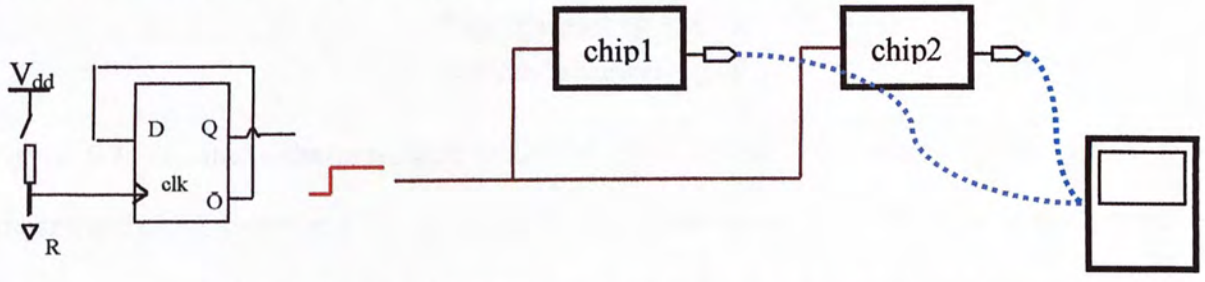


Figure 5.6. : Measurement setup to evaluate the enable signal

Figure 5.7. : Measured recovered clock signal
Top : transmitter signals
Bottom : receiver signal

Figure 5.7. illustrates the measured recovered clock signal. The traces on the top are the transmitted clock signal and RF carrier at the transmitter terminal. The trace at the bottom is the recovered clock signal at the smart card. The measured results demonstrate that the clock recover circuit is operating properly.

5.4. Power Consumption

The actual power consumption is too small to measure, so we can only present simulation results. We have found the current draw from two power clock supply by simulation.

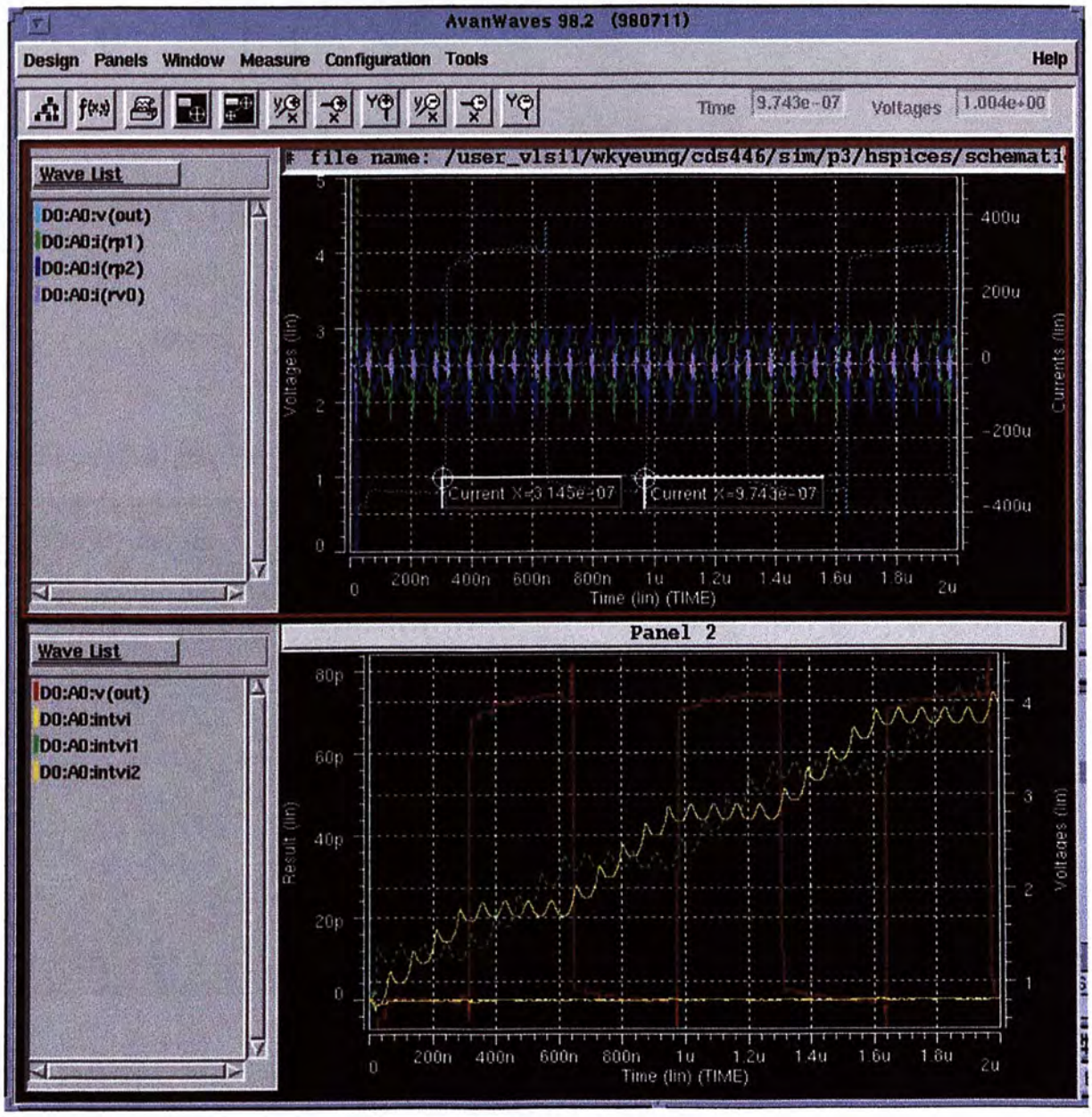


Figure 5.8. : Power simulation 1

The output frequency is $\frac{1}{T} = \frac{1}{(9.743 - 3.145) \times 10^{-7}} = \frac{1}{6.598 \times 10^{-7}} \approx 1.52 \ \ MHz$

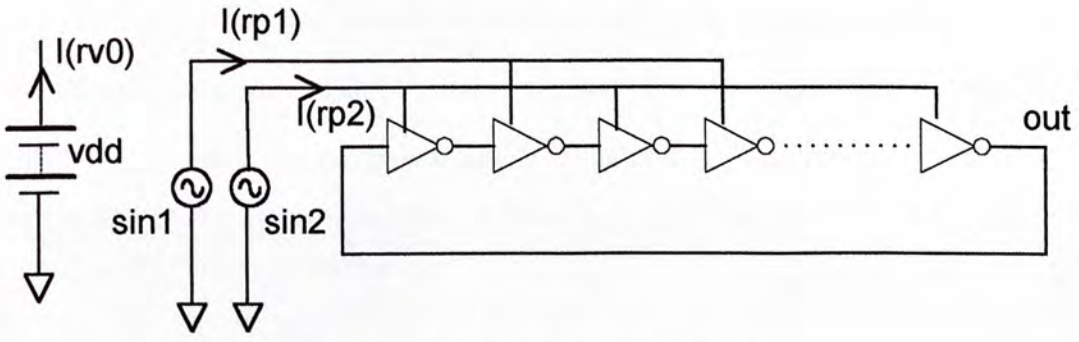


Figure 5.9 : Simulation schematic

The curve intvi1 is $f(t) = \int_0^t V_{\sin 1}(t) \times I_{rp1}(t) dt$

intvi2 is $f(t) = \int_0^t V_{\sin 2}(t) \times I_{rp2}(t) dt$

intvi is $f(t) = \int_0^t V_{vdd}(t) \times I_{rv0}(t) dt = \int_0^t 5 \times I_{rv0}(t) dt$

In Figure 5.8. panel 2:

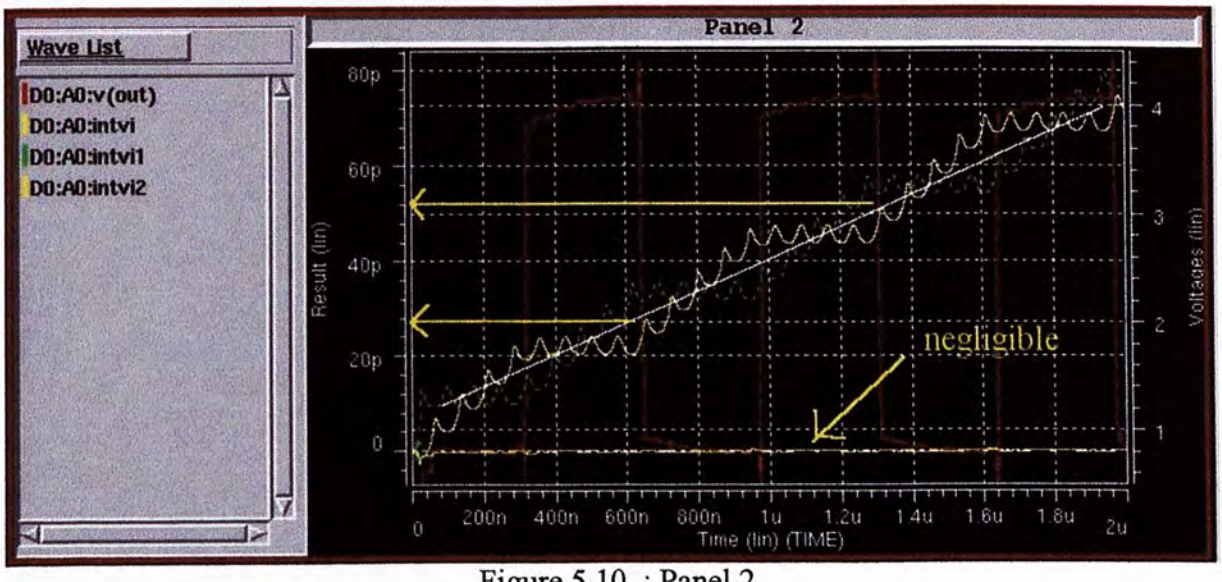


Figure 5.10. : Panel 2

The power of the circuit can be illustrated below:

$$P = \frac{1}{T}\int_{t1}^{t2} V(t) \times I(t) dt \qquad t2 - t1 = T$$

$$= f \times \left(\int_0^{t2} V(t) \times I(t) dt - \int_0^{t1} V(t) \times I(t) dt \right)$$

$$= 1.52 \times 10^6 \left(52 \times 10^{-12} - 28 \times 10^{-12} \right)$$

$$= 36.48uW$$

As there are two power clock supplies, the total power consumption is about 72.96 μW.

In order to do comparison, we have done the same simulation on a conventional CMOS ring oscillator that has the same output frequency, the total number of gates is equal to 4289. We have found the current draw from power supply V_{dd} -- I(r0) in Figure 5.11.

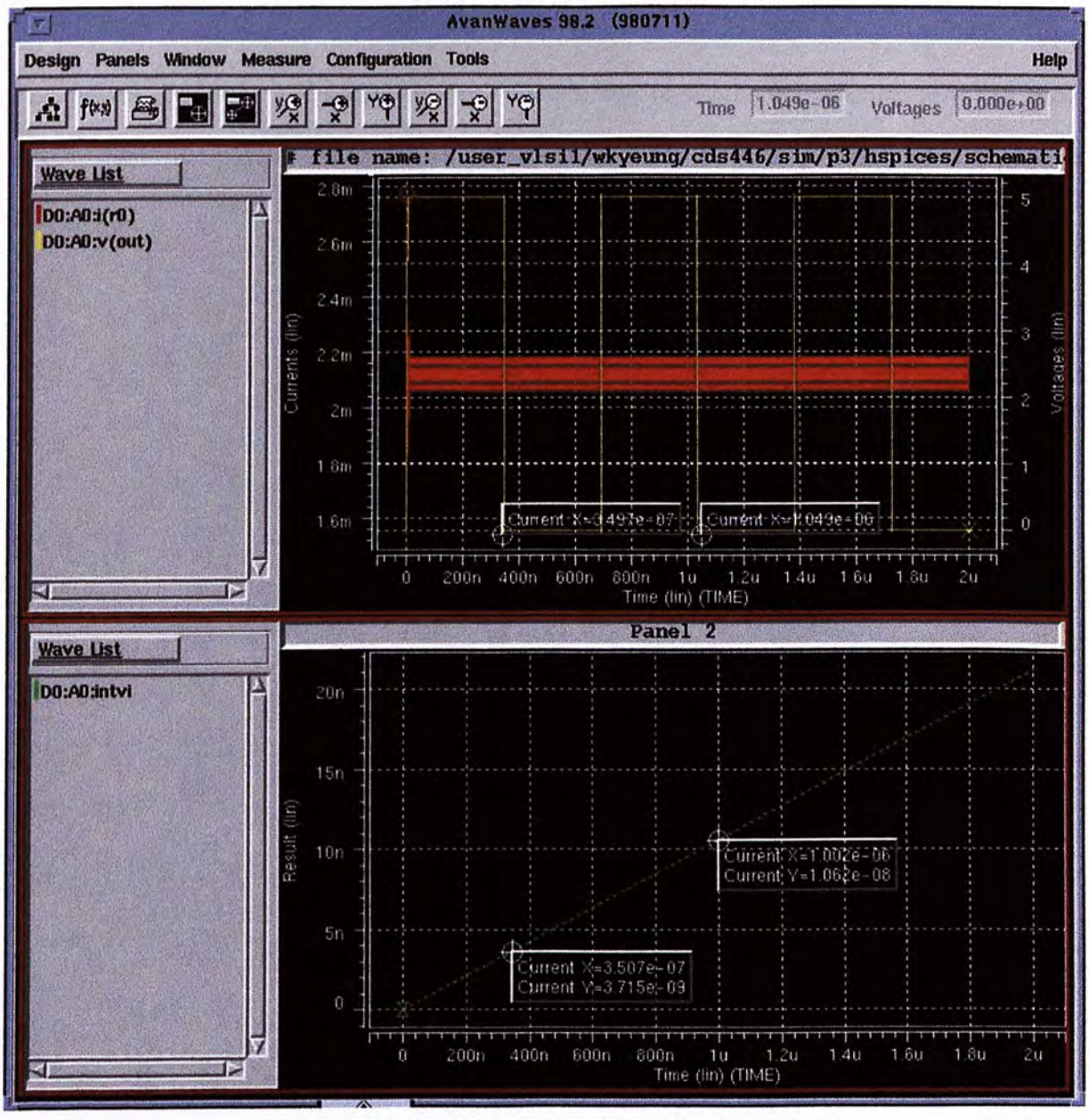


Figure 5.11: Power simulation 2

The output frequency is $\frac{1}{T} = \frac{1}{(10.49 - 3.497)\times 10^{-7}} = \frac{1}{6.993\times 10^{-7}} \approx 1.43 \ \ MHz$

The curve intvi is $f(t) = \int_0^t V_{vdd}(t) \times I_{vdd}(t) dt = \int_0^t 5 \times I_{vdd}(t) dt$

$$P = \frac{1}{T}\int_{t1}^{t2} 5 \times I(t)dt \qquad t2 - t1 = T$$
$$= f \times \left(\int_0^{t2} 5 \times I(t)dt - \int_0^{t1} 5 \times I(t)dt \right)$$
$$= 1.43 \times 10^6 \left(10.62 \times 10^{-9} - 3.715 \times 10^{-9}\right)$$
$$= 9.8mW$$

The power dissipation in a conventional CMOS ring oscillator is approximately 134 times larger than the power dissipated in an adiabatic ring oscillator operating at the same frequency.

6. Conclusion

We have demonstrated the topology of Adiabatic Quasi-static CMOS logic (AqsCMOS). It is totally compatible with conventional CMOS logic and the topology is simple. We have used the special property of AqsCMOS to design a clock recover circuit for contactless smart card application. RF carrier extracted from the transmitter is used to power up the clock recover circuit.

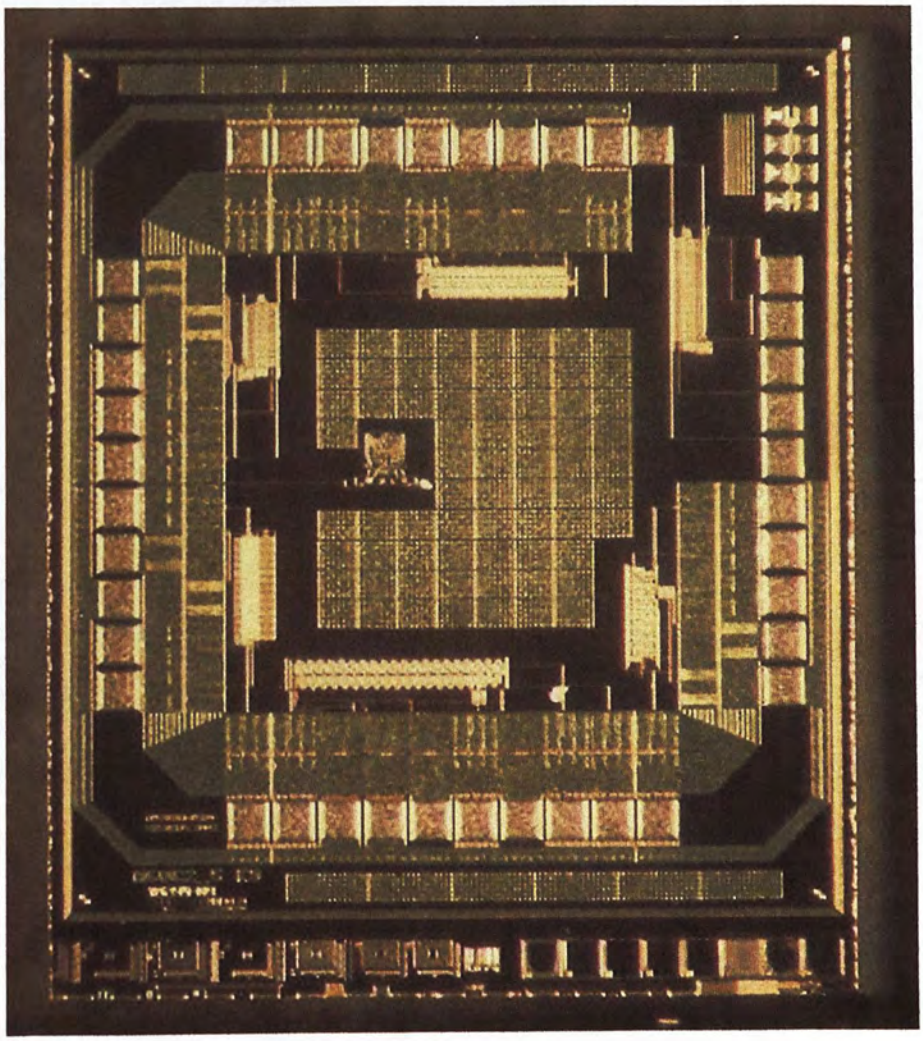
Experimental results have verified that the clock recover circuit using AqsCMOS is working properly. Moreover, we have also observed that the new clock recover circuit is extremely stable over a wide range of temperatures. There are three major advantages of this new design compare to conventional design :

1. Very simple circuitry, no complicated PLL circuit is required.
2. Power directly by RF carrier.
3. As a result of the special synchronization property of AqsCMOS. The new clock recover circuit is extremely stable over a wide range of temperatures. No timing jitter is detected between the transmitter and receiver.

A paper titled "Clock Recovery Circuit with Adiabatic Technology (Quasi-Static CMOS Logic)" base on this work was presented at ISCAS2003.

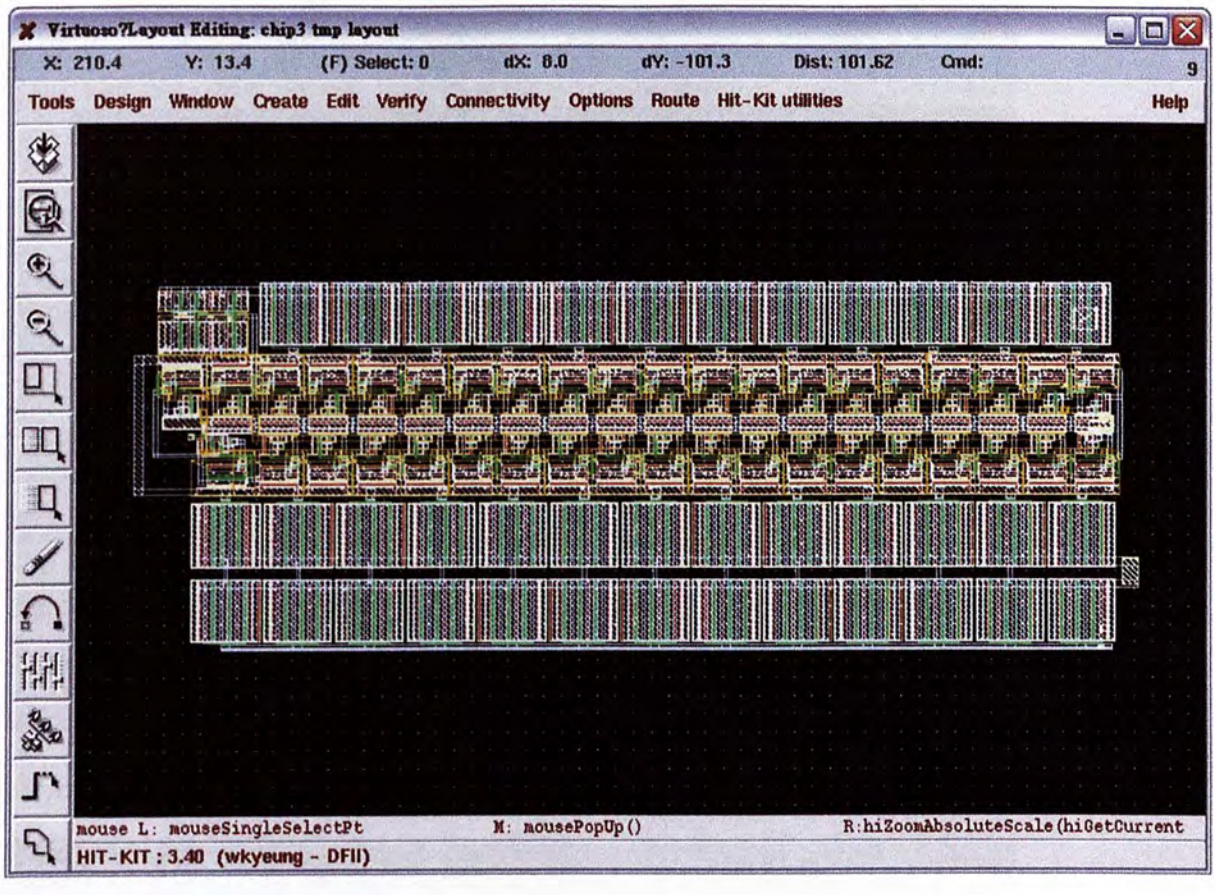
Appendix I

Chip Layout



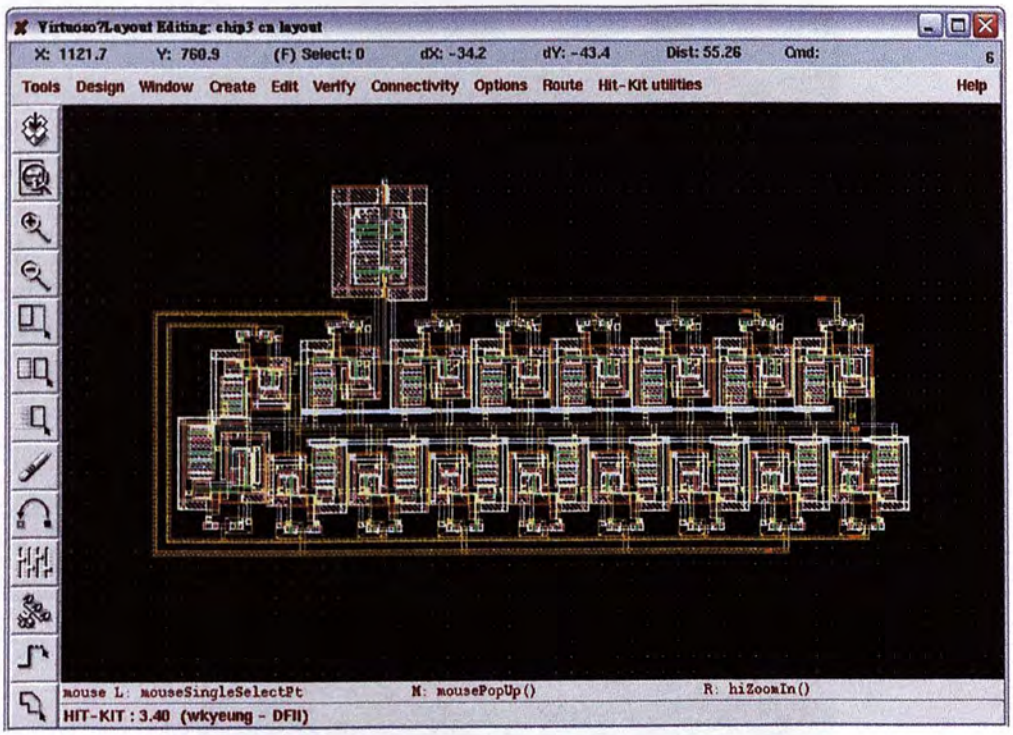
Appendix IIa

Layout of Oscillator (type 1) – 39 stages

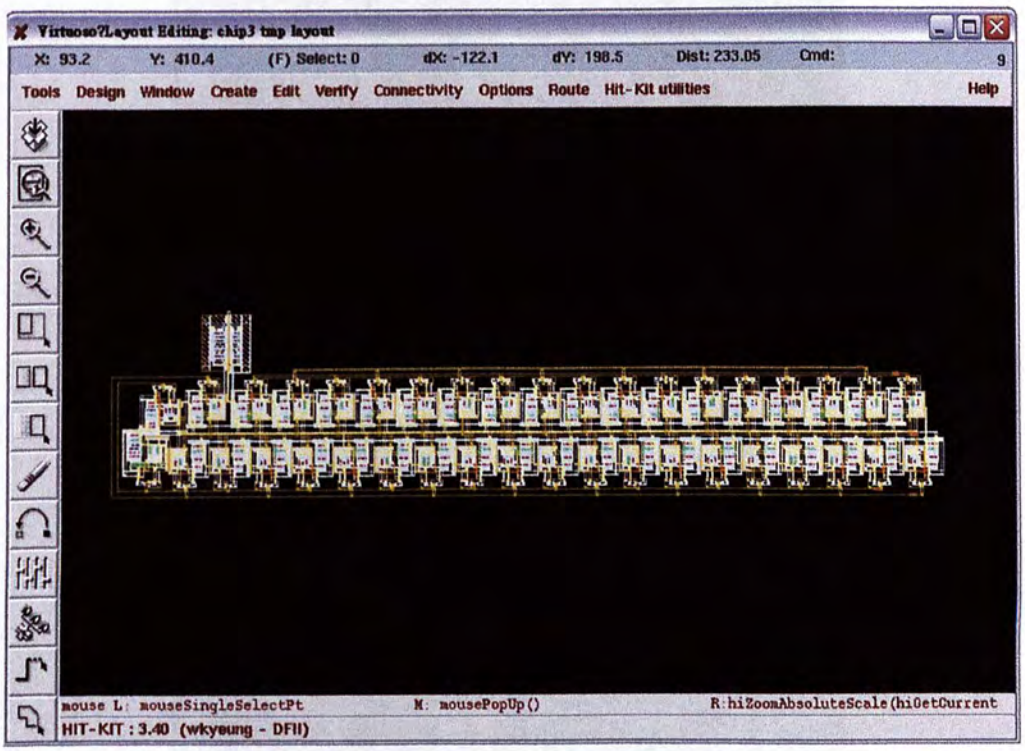


Appendix IIb

Layout of Oscillator (type 2) – 17 stages

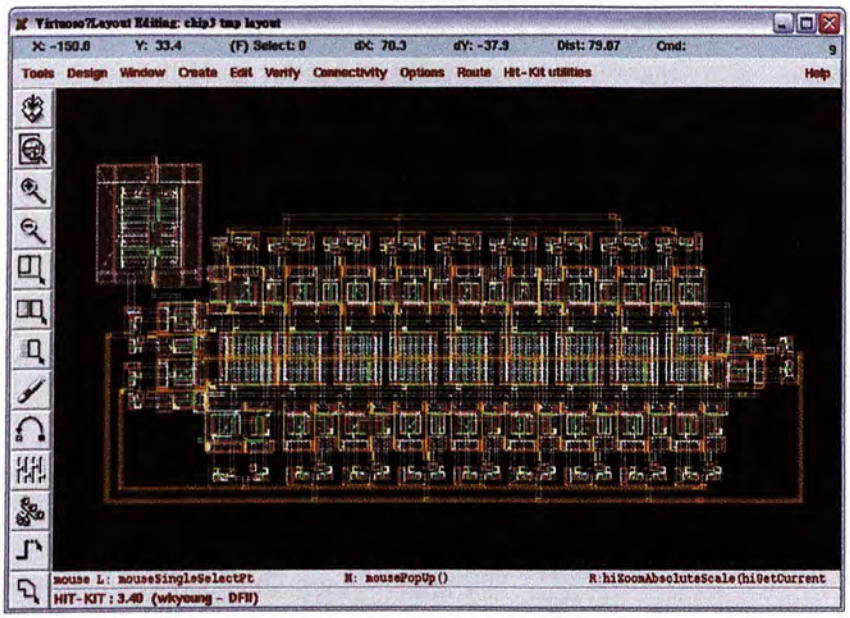


Layout of Oscillator (type 2) – 39 stages

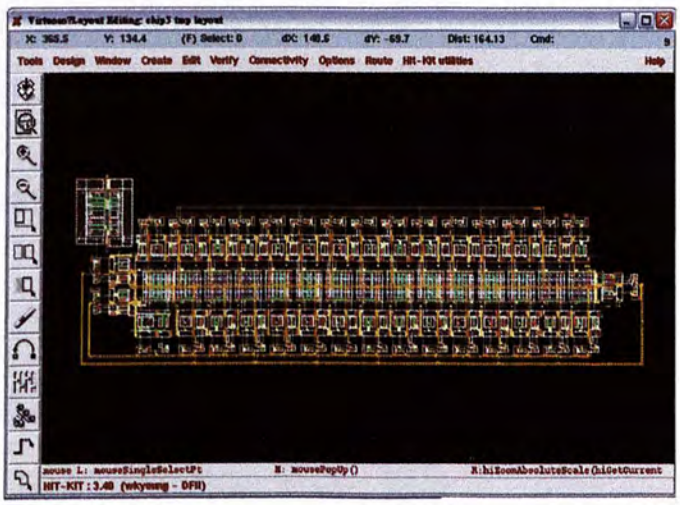


Appendix IIc

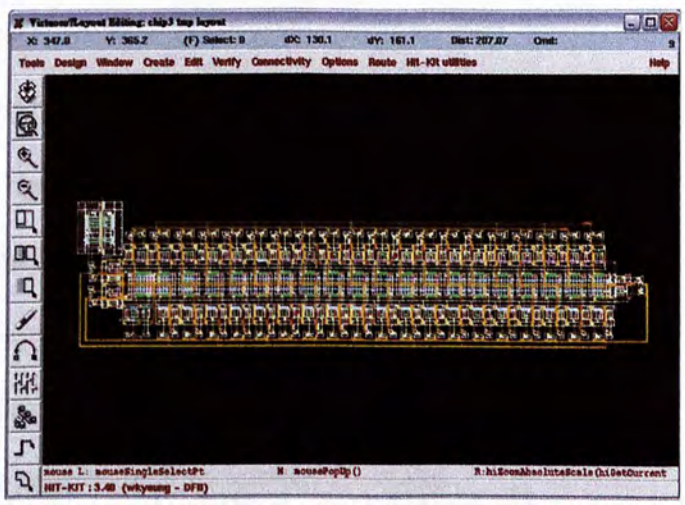
Layout of Oscillator (type 3) – 21 stages



33 stages



43 stages



Appendix III

Bibliography of ISO/IEC card standards

ISO/IEC 7811-1: 1995, Identification cards - Recording technique - Part 1: Embossing.

ISO/IEC 7811-2: 1995, Identification cards - Recording technique - Part 2: Magnetic stripe.

ISO/IEC 7811-3: 1995, Identification cards - Recording technique - Part 3: Location of embossed characters on ID-1 cards.

ISO/IEC 7811-4: 1995, Identification cards - Recording technique - Part 4: Location of read-only magnetic tracks - Tracks 1 and 2.

ISO/IEC 7811-5: 1995, Identification cards - Recording technique - Part 5: Location of read-write magnetic track - Track 3.

ISO/IEC 7811-6: 1996, Identification cards - Recording technique - Part 6: Magnetic stripe - High coercivity

ISO/IEC 7812-1: 1993, Identification cards - Identification of issuers - Part 1: Numbering system.

ISO/IEC 7812-2: 1993, Identification cards - Identification of issuers - Part 2: Application and registration procedures.

ISO/IEC 7813: 1995, Identification cards - Financial transaction cards.

ISO/IEC 7816-1: 1998, Identification cards - Integrated circuit(s) cards with contacts - Part 1: Physical characteristics.

ISO/IEC 7816-2: 1998, Identification cards - Integrated circuit(s) cards with contacts - Part 2: Dimensions and location of the contacts.

ISO/IEC 7816-3: 1997, Identification cards - Integrated circuit(s) cards with contacts - Part 3: Electronic signals and transmission protocols.

ISO/IEC 10536-1: 1992, Identification cards - Contactless integrated circuit(s) cards - Part 1: Physical characteristics.

ISO/IEC 10536-2: 1995 Identification cards - Contactless integrated circuit(s) cards - Part 2: Dimensions and location of coupling areas.

International Standard ISO/IEC 14443-1 was prepared by Joint Technical Committee ISO/IEC/JTC1, Information technology.

ISO/IEC 14443-1: Identification cards - Contactless integrated circuit(s) cards - Proximity cards - Part 1: Physical characteristics.

ISO/IEC 14443-2: Identification cards - Contactless integrated circuit(s) cards - Proximity cards - Part 2: Radio frequency power and signal interface.

ISO/IEC 14443-3: Identification cards - Contactless integrated circuit(s) cards - Proximity cards - Part 3: Initialization & anticollision.

ISO/IEC 14443-4: Identification cards - Contactless integrated circuit(s) cards - Proximity cards - Part 4: Transmission protocols.

ISO/IEC 15693 -1: Identification cards - Contactless integrated circuit(s) cards - vicinity cards - Part 1: physical characteristics.

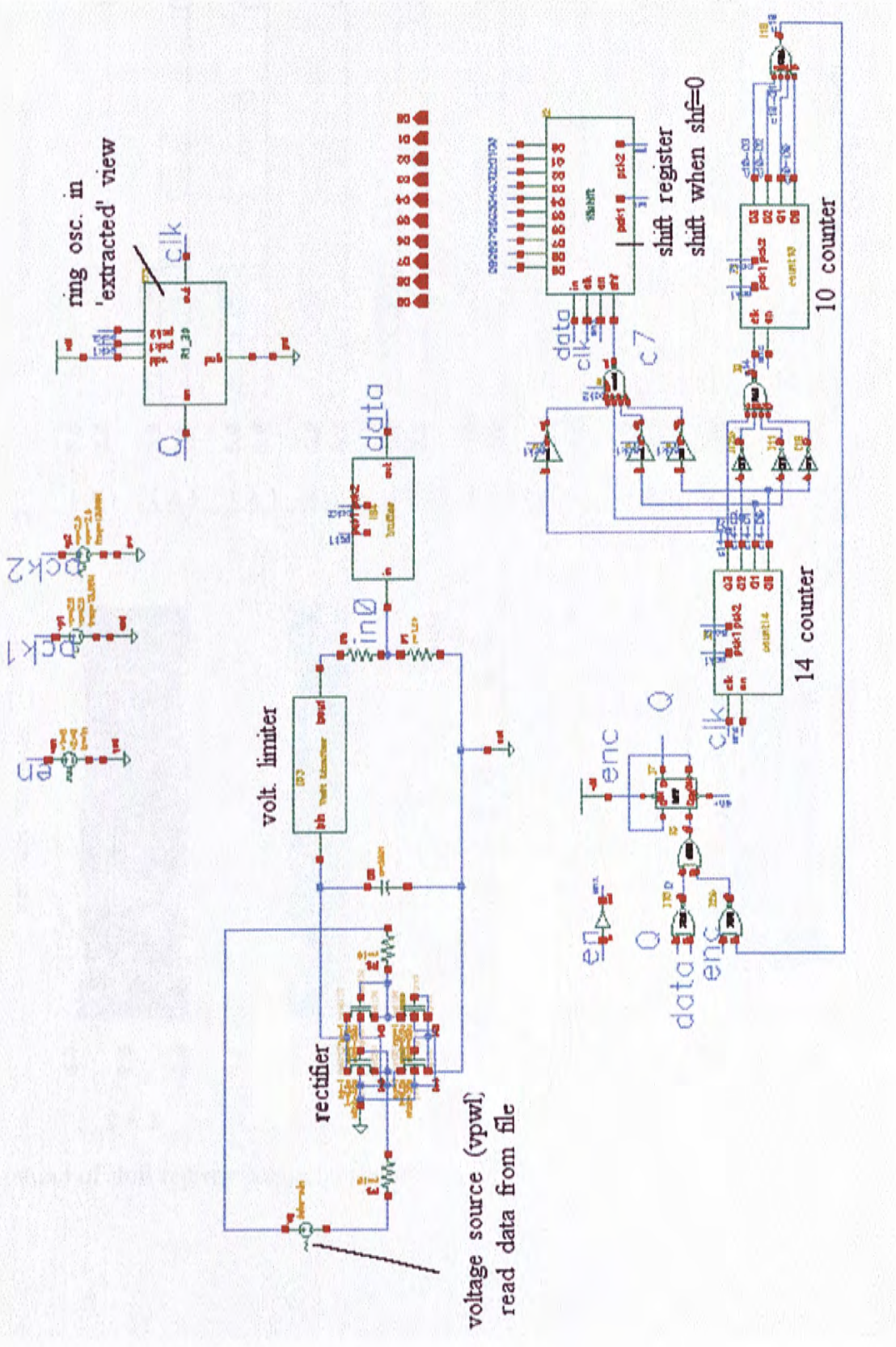
ISO/IEC 15693-2: Identification cards - Contactless integrated circuit(s) cards - vicinity cards - Part 2: radio frequency power and signal interface.

ISO/IEC 15693-3: Identification cards - Contactless integrated circuit(s) cards - vicinity cards - Part 3: anticollision and transmission protocol.

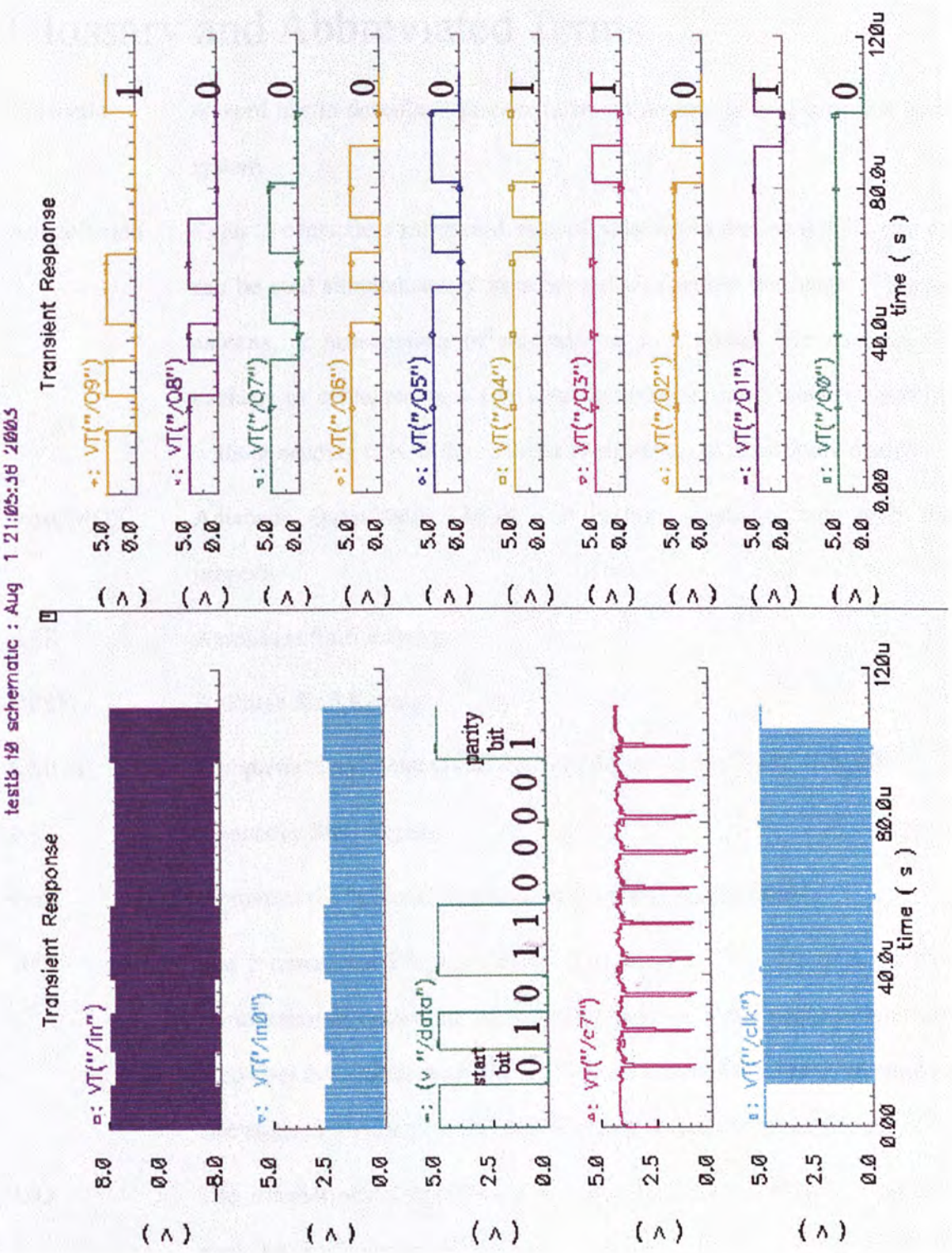
ISO/IEC 15693-4: Identification cards - Contactless integrated circuit(s) cards - vicinity cards - Part 4: extended command set and security features

Appendix IV

Schematic



Simulation results



The output of shift register can get the right data.

Glossary and Abbreviated Terms

Adiabatic	A word use to describe a process in which no heat is gained or lost by the system
Anticollision	Refer to contactless smart card, anticollision means the capabilities that data can be read simultaneously from several tags within the range of a single antenna, or arrangement of antennas, as in a portal. The contents of a package or container on a conveyor belt can be simultaneously identified without needing to read the contents of all packaged items individually.
AqsCMOS	Adiabatic Quasi-static CMOS – it is fully adiabatic logic with static property.
ASK	Amplitude Shift Keying
BPSK	Bi-Phase Shift Keying
CMOS	Complementary Metal Oxide Semiconductor 互補式金氧半電晶體
FSK	Frequency Shift Keying
Gnd	It presents the "ground" (i.e. common) of integrated circuit
IEC	The International Electrotechnical Commission – the IEC is a worldwide commission develops the specialized system for worldwide standardization. It co-operates closely with ISO. The IEC covers the fields of electrical and electronics technology, while ISO is responsible for all other fields.
ISO	The International Organization for Standardization – ISO is a worldwide association of around 100 national standards agencies, with one per country. It was founded in 1948 and is non-national organization to promote the development of standards throughout the world. It co-operates closely with IEC when deal with the field of electrical and electronics.

NRZ	non-return to zero
Smart Card	集成電路卡/(聰明卡) – Its professional name is integrated circuit card. It more popularly known smart card, as it is portable, tamper-resistant computer with a programmable data store.
UART	Abbreviation of Universal Asynchronous Receiver and Transmitter –used for communication with serial input/output devices
V_{dd}	It represents the supply voltage in integrated circuit
VLSI	Very Large Integrated Circuit 超大規模集成電路

Reference

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