Matching Properties and Applications of Compatible Lateral Bipolar Transistors (CLBTs)

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Hiu Yung WONG

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Abstract

As System-On-a-Chip (SOC) and mixed-signal technologies become increasingly popular, realization of Bipolar Junction Transistors (BJTs) and Metal-Oxide-Semiconductor Field Effect Transistors (MOSFETs) on the same chip has also increased in importance. This is because BJTs and MOSFETs are well-known for their superior properties in implementing high speed analog and low power digital circuits respectively. Since no additional processing steps are required, Compatible Lateral Bipolar Transistors (CLBTs), which are parasitic lateral BJTs formed in Complementary Metal-Oxide-Semiconductor (CMOS) processes, provide an inexpensive means and alternative to BiCMOS processes.

At the same time, deep submicron and low-power ICs put more stringent requirements on the matching properties of the devices, especially in analog circuits. Matching properties refer to the degree of similarity between electrical parameters of two identically designed and used devices. MOSFETs are notorious for their poor matching properties in subthreshold conduction and CLBTs are generally expected to have better matching properties. In this thesis, the matching properties of CLBTs and MOSFETs fabricated using a typical digital IC process have been studied and compared systematically and quantitatively, in the hope of providing useful data for circuit designers. Test

chips containing arrays of *pnp* CLBTs and nMOSFETs were fabricated using the AMI-ABN $1.5\mu m$ n-well process. In an n-well process, only *pnp* CLBTs can be fabricated and their matching properties were compared with those of nMOSFETs, which are optimized in such a process. The arrays were designed for a good balance between the number of devices, number of available pins and accuracy. Shift registers and transmission gates were used to select individual devices for testing. To emulate a practical condition, the *pnp* CLBTs were cascoded with *p*MOSFETs and surrounded with *p*-type guard rings and designed to have similar layout area as that of the nMOSFETs for fair comparisons. Each chip contained 144 *pnp* CLBTs and 225 nMOSFETs, giving a total of 576 *pnp* CLBTs and 900 nMOSFETs in 4 chips.

Individual *pnp* CLBTs under the same biasing conditions were tested at nominal collector current levels from $100nA$ down to $1nA$. The drain currents at levels ranging from $10\mu A$ down to $1nA$ of individual *p*MOSFETs (CLBTs operating in MOS mode) and nMOSFETs were also measured. The matching properties of the devices at different current levels were then calculated. It was found that the matching properties of the nMOSFETs were 3-4 times better than those of the *pnp* CLBTs and the latter were, in turn, about 3 times better than those of the *p*MOSFETs. By applying the Law of Area, it was estimated that *p*MOSFETs with similar layout area as that of the *pnp* CLBTs would show similar matching properties as the *pnp* CLBTs. The devices were also paired up as current mirrors and they showed similar matching results.

可相容側向雙極性電晶體(**CLBT**)之匹配特性及其應用

作者：黃驍勇

摘要

隨著單晶片系統（SOC）和混合訊號（mixed-signal）技術的日益普及，將雙極性接面電晶體（BJT）和金氧半場效電晶體（MOSFET）實現於同一晶片上也變得更爲重要；蓋因 BJT 和 MOSFET 分別專長於構造高速度類比和低功率數位電路。由於可相容側向雙極性電晶體（Compatible Lateral Bipolar Transistor, CLBT）在互補式金氧半（CMOS）製程中自然而成，並不需要其他附加工序，它們也就成爲了便宜的 BiCMOS 替代品。

與此同時，深次微米（deep submicron）和低功率集成電路對元件的匹配特性（matching properties）的要求也越來越高，在類比電路中尤其如此。所謂匹配特性是指兩等同設計和應用元件所表現的電路參數之相似度。由於 MOSFET 在次臨界區（subthreshold region）之匹配特性特別差，加上 CLBT 一般被認爲有較好的匹配特性，本論文希望通過對在標準 CMOS 製程中生成之 MOSFET 與 CLBT 進行系統和定量的比較和研究，從而爲電路設計者提供有用的數據。本研究採用 AMI-ABN1.5μm *n*-well 製程製作含有 *pnp* CLBT 和 *n*MOSFET 矩陣的晶片。由於 *n*-well 製程只能生成 *pnp* CLBT 並且是爲 *n*MOSFET 而進行優化的，我們因此比較了這兩者的匹配特性。矩陣的設計應用移位暫存器和傳輸閘選取其中的元件測試，以便在有限的針腳下最準確地測試最多元件。爲了模仿真實情況，*pnp* CLBT 都串疊（cascoded）了 *p*MOSFET，由 *p*-型防護圈（guard ring）圍繞，並採用了和 *n*MOSFET 相當的佈置面積以便有較公平的比較。每一片晶片

含有 144 個 *pnp* CLBT 和 225 個 *n*MOSFET，在四片晶片中，總共就有 576 個 *pnp* CLBT 和 900 個 *n*MOSFET。

本研究測讀各個 *pnp* CLBT 在相同偏壓情況下的集電極電流，範圍由 100nA 到 1nA，同時也測讀 *p*MOSFET（把 CLBT 操作在 MOS 模式下）和 *n*MOSFET 的漏極電流，而範圍則由 10μA 到 1nA，並由此計算它們的匹配特性。結果顯示，*n*MOSFET 的匹配特性比 *pnp* CLBT 的要好上 3-4 倍，而後者則比 *p*MOSFET 的要好 3 倍左右。用面積定律（Law of Area）可以計算出和 *pnp* CLBT 相當大小的 pMOSFET 會跟 *pnp* CLBT 有相近的匹配特性。最後，當把各元件配對成電流鏡的時候，它們的匹配特性也顯示出相似的結果。

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Chapter 1

Introduction

1.1 Motivation and Objectives

The two main types of transistors used in today's Integrated Circuits (ICs) are the Bipolar Junction Transistor (BJT) and the Metal-Oxide-Semiconductor Field Effect Transistor (MOSFET), or simply MOS transistor. Complementary MOS (CMOS) is the process and circuit technique of using two types of complementary MOSFETs, namely pMOSFETs and nMOSFETs, which has the advantage of high speed and low power dissipation. With the advent of IC technology, digital circuits have become widespread and the CMOS process has been optimized for digital applications [IF94]. In spite of this, BJTs still retain many advantages over those of CMOS for some critical analog applications such as bandgap voltage references [DLVO85], photodetectors [ZCFK98], silicon cochlea [vSFV96], temperature sensors [BH96], and Digital-to-Analog Converters (DACs) [BBW90]. However, since CMOS and bipolar processes are incompatible, additional masking steps are required to combine both types of transistors on the same chip, which is the more expensive BiCMOS process. As System-on-a-Chip (SOC) becomes increasingly popular, the need for integrating the analog peripherals and digital processing cores on the same chip is increasing [Chi98]. Under such a situation, the Compatible Lateral Bipolar Transistors (CLBTs) have received renewed interest.

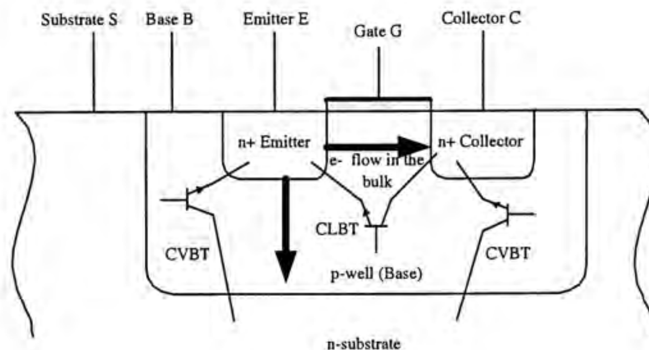

Figure 1.1: Cross-sectional view of CLBT.

CLBTs are the parasitic BJTs formed in CMOS process by operating the MOSFETs in bipolar mode (explained in detail in Section 4.2). The structure is shown in Figure 1.1. Therefore, BJTs and MOSFETs can be realized on the same wafer without additional costs using a standard CMOS process. MOSFETs can be used for implementing high density digital logic while the CLBTs can be used in the analog parts.

Technology downward scaling continues to be a major trend in the IC industry. According to the projections of the Semiconductor Industry Association (SIA), the feature size of the IC process would reach $0.05\mu m$ by the year 2011 [Josed]. Deep submicron technology requires further lowering of the supply voltage; on one hand to prevent the increase in electric field when device dimensions are decreasing with constant supply voltage, and, on the other hand, to reduce power consumption since the number of transistor per unit area is increasing in quadratic manner. In fact, the supply voltage and power per chip are predicted to be $0.5V$ and $174W$ by 2011 respectively by SIA. Analog circuits operating under ultra-low power supply voltages require well-matched devices for proper operation. Matching properties refer to the similarities between the electrical properties of two identically designed and used components after fabrication. However, MOSFETs fail to meet such requirements especially in low current level operations. Since CLBTs have been shown to

have better matching properties than CMOS [Vit83, PA89, vSFV96, RHL97], a study of low voltage and low power circuits incorporating CLBTs becomes more meaningful.

CLBTs have been gaining interest since 1969 [LHIK69]. CLBTs were analyzed and incorporated in current mirrors and amplifiers, and were shown to have lower noise than those incorporating only MOSFETs by Vittoz in 1983 [Vit83]. In 1985, accurate CMOS voltage references incorporating CLBTs were realized [DLVO85]. Arreguit then proposed a more complete model for CLBTs in 1989 in his PhD thesis [Arr89] and the CLBT was shown to have better matching properties than MOSFETs since they push the flow of carriers away from the surface of the device. The matching of CLBT current mirrors also has been shown to be better than that of MOSFET current mirrors, especially under low current levels [PA89]. Applications have used CLBTs for their improved matching properties over MOSFETs, some examples being a Variable Gain Control (VGC) circuit [PA89], a silicon cochlea [vSFV96], and a logarithmic photoreceptor [RHL97].

Even though many applications of CLBTs appear in the literature, to the best of our knowledge, the matching properties of CLBTs have not been investigated systematically and quantitatively hitherto. Matching properties, however, are very critical in the design of low power analog circuits. The main aim of this thesis is to study the matching properties of CLBTs and compare them with *n*MOSFETs and *p*MOSFETs fabricated with a standard CMOS process in a systematic and quantitative fashion. Applications of CLBTs for improved circuits were also studied.

1.2 Contributions

Test chips containing arrays of cascoded *pnp* CLBTs with *p*-type guard rings and *n*MOSFETs were fabricated using the standard AMI-ABN $1.5\mu m$ *n*-well

process. An efficient parameter extraction array for bipolar devices was designed. This design provides a good balance between the number of devices to be tested, number of pins and accuracy.

The *pnp* CLBTs and *n*MOSFETs were designed to have similar layout areas. There were in total 900 *n*MOSFETs and 576 *pnp* CLBTs. A testing setup was developed to perform automatic extraction of transistor parameters. Using this setup, the matching properties of the *pnp* CLBTs and *n*MOSFETs, as well as the *pnp* CLBTs operating as *p*MOSFETs, were measured.

A preliminary study of the application of Floating-Gate CLBTs (FG-CLBTs) was also carried out. An Operational Transconductance Amplifier (OTA) incorporating FG-CLBTs as the input differential pair was designed and fabricated. The advantage of using CLBTs in OTAs is that they are expected to have lower noise. By utilizing the residual gate effects of the CLBTs, we showed that it was possible to trim the offset of the OTA by using hot electron injection and electron tunnelling in this standard $1.5\mu m$ process.

1.3 Organization of the Thesis

An introduction on the structures and representative fabrication technologies of CMOS, BJT, and BiCMOS circuits is presented in Chapter 2. In Chapter 3, matching properties are introduced. In Chapter 4, the structures, modeling, and main characteristics of CLBTs are discussed. Experimental results of the DC characteristics of the CLBTs and MOSFETs fabricated using this process are also included in this chapter. Experimental results of the matching properties of CLBTs, *n*MOSFETs and *p*MOSFETs and the comparisons and analysis are given in Chapter 5. Conclusions are given in Chapter 6. Finally, a review of floating gate technologies is presented in Appendix A and the design, characteristics and experimental results of the trimmable FGOTA are given in Appendix B. Process parameters are given in Appendixes C and D.

Chapter 2

Devices and Fabrication Processes

2.1 Introduction

Since the invention of planar technology in the 1960's, the integration of large numbers of devices on a single silicon die became possible and effective. Bipolar, CMOS and BiCMOS Integrated Circuit (IC) processes were then developed in the 60's, 70's, and 80's respectively. This chapter presents the structures and models of the Bipolar Junction Transistors (BJTs) and Metal-Oxide-Semiconductor Field Effect Transistors (MOSFETs), which are the representative active elements in bipolar and CMOS processes respectively. Representative IC processes and the pros and cons of these technologies and devices are also discussed. All these serve as the basis for the understanding of the following chapters.

2.2 BJTs

2.2.1 Structure and Modeling of BJTs

There are three terminals in a bipolar transistor, namely the collector C, base B, and emitter E (Figure 2.1). Bipolar technology is usually optimized for vertical *npn* BJTs [Arr89, GM93] and Figure 2.1 shows the cross-sectional view of a vertical *npn* transistor. For an *npn* transistor in the forward active mode, the base-emitter junction would be forward biased with $V_{BE} > 0$ and the base-collector junction would be reverse biased ($V_{BC} < 0$). The electrons are injected into the base as minority carriers and collected in the collector. The collector current I_C, base current I_B, and forward current gain β_F can be expressed as [GM93]:

$$I_C = qAD_n \frac{n_{po}}{W_B} \exp \frac{V_{BE}}{U_T} \tag{2.1}$$

$$I_B = \left(\frac{1}{2}\frac{n_{po} W_B qA}{\tau_b} + \frac{qAD_p}{L_p}\frac{n_i^2}{N_D}\right) \exp \frac{V_{BE}}{U_T} \tag{2.2}$$

$$\beta_F = \frac{I_C}{I_B} = \frac{1}{\frac{W_B^2}{2\tau_b D_n} + \frac{D_p}{D_n}\frac{W_B}{L_p}\frac{N_A}{N_D}} \tag{2.3}$$

where q is the electronic charge ($1.6 \times 10^{-19} C$), A is the effective emitter area, D_n is the electron diffusion constant, W_B is the effective base width, n_{p0} is the equilibrium electron concentration in the base, U_T is the thermal voltage, τ_b is the minority-carrier lifetime in the base, D_p is the diffusion constant for hole, L_p is the diffusion length for hole in emitter, n_i is the intrinsic carrier concentration in silicon, N_A is the acceptor concentration, and N_D is the donor concentration.

From the equations, the collector current depends on both process parameters and layout design. IC designers can only control I_C through the layout of different emitter areas and the emitter area is defined as the horizontal area of the base and emitter interface (Equation 2.1).

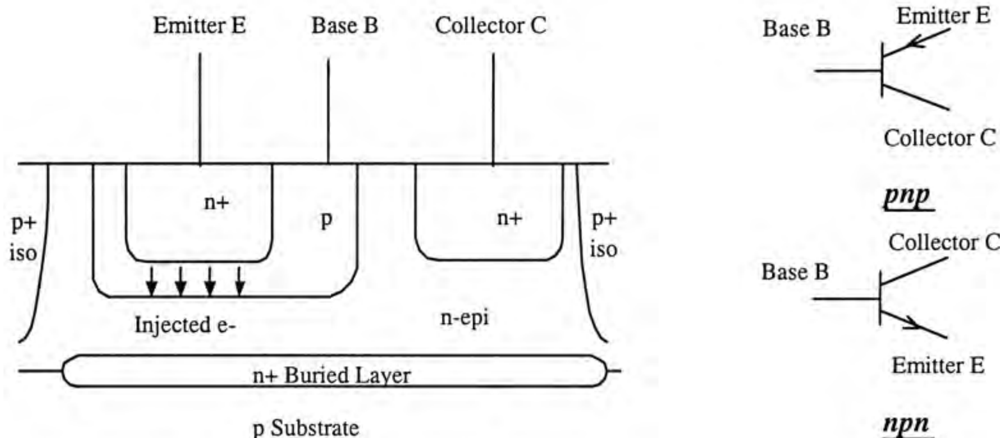

Figure 2.1: Cross-sectional view of vertical *npn* bipolar transistor (left) and *npn* and *pnp* bipolar transistor symbols (right).

2.2.2 Standard BJT Process and BJT Characteristics

Standard bipolar integrated circuits using the bipolar process optimized for vertical *npn* BJT are usually fabricated on a lightly doped (111)-oriented *p*-type substrate (Figure 2.1) [Has01]. (111) silicon crystal helps to prevent the formation of the parasitic *p*MOSFETs between the base and the isolations. Then an n^+-buried layer is formed, followed by the growth of an *n*-type epitaxial layer. Isolation diffusion, base implant and emitter diffusion then follow to form the isolations, base, and emitter and collector regions respectively. Other active and passive devices are formed based on these masks. The optimization of the vertical *npn* BJTs poses limitation of the performance on *pnp* BJTs and in fact, only lateral and substrate *pnp* BJTs can be formed in such a process.

The characteristics of bipolar processes optimized for vertical *npn* transistors are summarized as follows [Arr89]:

- A n^+ buried layer is implemented to prevent undesirable injection of carriers into the *p*-substrate and to decrease the collector series resistance (Figure 2.1).

- The base width, the vertical distance between the n^+ emitter region and the n epitaxial collector region, is minimized to increase β_F (Equation 2.3).
- The emitter region is heavily doped to increase the ratio of emitter to base doping densities N_D/N_A to increase β_F (Equation 2.3).
- Early effect and avalanche multiplication effects are minimized by keeping the collector doping as low as possible. The Early effect refers to the fact that the depletion width of base-collector junction will increase as V_{CB} increases, thus lowering the effective base width. According to Equation 2.1, I_C will increase even under constant V_{BE}, thereby lowering the output resistance.

Since most bipolar processes are optimized for vertical *npn* transistors, they have higher gain (100 to 200) than that of substrate (60 to 100) and lateral (30 to 50) *pnp* transistors [Arr89]. Compared with MOSFETs, bipolar junction transistors (BJTs) have more driving power to overcome the speed bottleneck of driving large capacitive loads. However, they consume more power than MOSFETs, so they are suitable for high speed but low transistor density design.

2.3 MOSFETs and Complementary MOS (CMOS)

2.3.1 Structure and Modeling of MOSFETs

The polysilicon-gate CMOS process is optimized to form complementary *p*MOSFET and *n*MOSFET transistors on a common substrate. *n*MOSFETs and *p*MOSFETs use electrons and holes as majority carriers respectively. Unlike bipolar devices, they only use either holes or electrons as carriers, so, they are also known as unipolar devices. Figure 2.2 shows the cross-sectional view

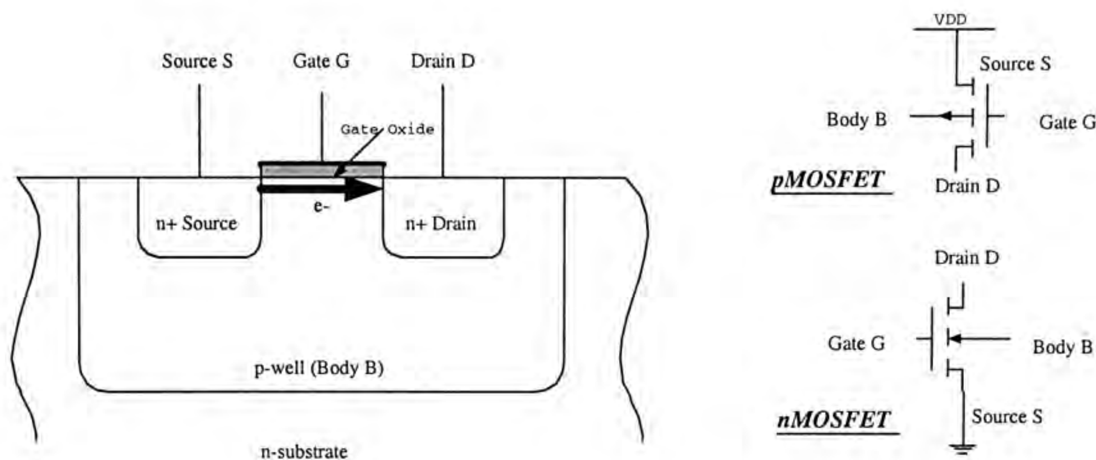

Figure 2.2: Cross-sectional view of an nMOSFET (left) and the symbols for nMOSFET and pMOSFET transistors (right).

of an nMOSFET and its symbol respectively. There are four terminals in an nMOSFET, namely the source S, gate G, drain D, and body B. The gate is isolated from the well by a layer of thin gate oxide. The body refers to the well and is usually grounded to the lowest potential of the circuit in operation. During normal operations, the drain is connected to a higher potential with respect to the source and body such that $V_{DS} > 0V$ and $V_{SB} = 0V$. As a result, the n-type drain, p-type well, and n-type source form a pair of back-to-back diodes and would only conduct a small leakage current which is known as subthreshold conduction or weak inversion and obeys an exponential law. If the gate-source voltage V_{GS} is larger than a certain voltage, namely the threshold voltage V_T, electrons would accumulate on the surface near to gate oxide to an extent such that the electron concentration is higher than the hole concentration. An n-type region is then effectively formed on the surface and this phenomenon is called strong inversion and the channel is called the inversion layer. The nMOSFET would then be able to conduct drain current I_D, which depends on both V_{GS} and V_{DS}. The nMOSFET is said to be in linear mode. When $V_{DS} > V_{GS} - V_T$, I_D will no longer depend on V_{DS} and the nMOSFET is in saturation mode. The $I - V$ transfer characteristic of nMOSFET can be

expressed as [EKV95]:

Weak inversion ($V_S > V_P$ and $V_D > V_P$):

$$I_D = 2n\beta U_T^2 \exp\frac{V_P}{U_T}(\exp\frac{-V_S}{U_T} - \exp\frac{-V_D}{U_T}) \quad (2.4)$$

Linear mode under strong inversion ($V_S \leq V_P$ and $V_D \leq V_P$):

$$I_D = n\beta(V_P - \frac{V_S + V_D}{2})(V_D - V_S) \quad (2.5)$$

Saturation mode under strong inversion ($V_S \leq V_P$ and $V_D > V_P$):

$$I_D = \frac{n\beta}{2}(V_P - V_S)^2 \quad (2.6)$$

where

$$V_P \cong \frac{V_G - V_{T0}}{n} \quad (2.7)$$

$$\beta = \frac{W}{L}\mu_n C_{ox} \quad (2.8)$$

$$V_{T0} = V_{FB} + \Psi_0 + \gamma\sqrt{\Psi_0} \quad (2.9)$$

and V_P is the pinch-off voltage, V_{T0} is the threshold voltage when the channel is in equilibrium and depends on the surface charge density, n is the slope factor, β is the current factor, U_T is the thermal voltage, W and L are the width and length of the gate respectively, μ_n is the mobility of electron, C_{ox} is the gate oxide capacitance per unit area, V_{FB} is flat band voltage, $\Psi_0 = 2\Phi_F + \textit{several}\ U_T$ where Φ_F is the Fermi potential, and γ is the body factor. Note that both V_{T0} and γ also depend on C_{ox} and the doping of the bulk.

pMOSFETs have a similar structure to nMOSFETs. The majority carriers of pMOSFETs are holes. The source and drain regions of a pMOSFET are p-type while the body is of n-type. It is possible to put nMOSFETs and pMOSFET on the same chip without adding many process steps, and this is called CMOS technology.

2.3.2 Standard n-well CMOS Process and MOSFETs Characteristics

There are three kinds of CMOS processes, n-well, p-well and twin-well. In Figure 2.3, the substrate is of p-type, so an nMOSFET can be formed directly on it. In order to form a pMOSFET, an n-type well has to be formed first as the body of the pMOSFET. Then, the source and drain of the pMOSFET are formed by creating p-type regions in the n-well. This is known as an n-well CMOS process. It is also possible to have a p-well process with nMOSFETs being built in the p-wells and pMOSFETs built directly on an n-substrate (shown in Figure 2.2). In some processes, which are called the twin-well processes, both the p-well and n-well are formed simultaneously. Twin-well processes are usually found in deep submicron processes because in these processes, the bodies of the MOSFETs have to be highly doped to reduce the chance of punch-through. Counter doping becomes very unfavorable and highly doped n-wells and p-wells have to form separately. However, it should be noted that in a twin-well process, either one type of wells are still connected together to the substrate as the substrate must be either p or n-type. In this thesis, an n-well process was used and so, only the n-well processes will be discussed.

For an n-well process, CMOS integrated circuits are usually fabricated on (100)-oriented p-type substrate, which is heavily doped with boron to minimize the resistivity. The (100) silicon creates lower surface state density and improves the threshold voltage control [Has01]. An epitaxial layer of about 5 to $10\mu m$ is then grown followed by n-well diffusion. A moat mask is then used to define the active areas where the MOSFETs will form. After the formation of gate oxide, threshold adjust implantation is used to adjust the threshold voltage of the MOSFETs to the range of $0.7V$ to $0.9V$. Polysilicon deposition and patterning and source/drain implantation then follow. The following can be observed for an n-well CMOS process:

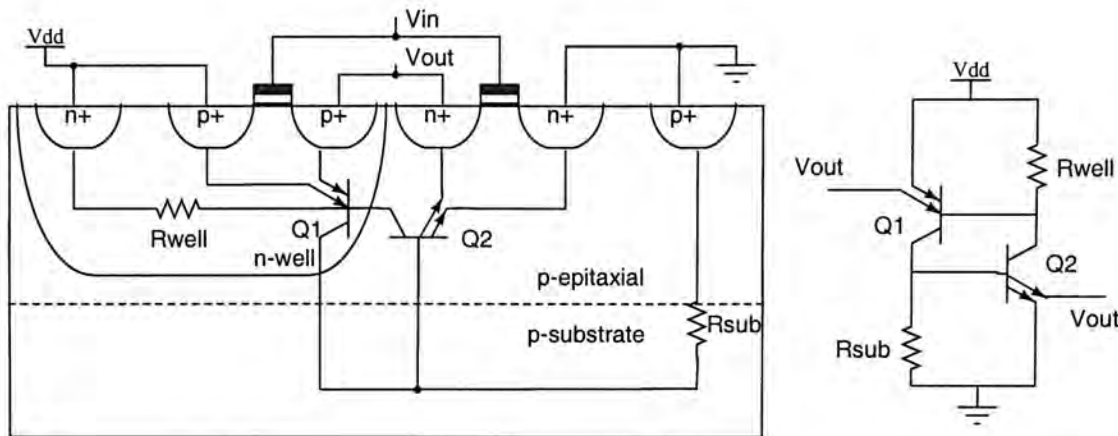

Figure 2.3: Cross-sectional view of an n-well CMOS process with latch-up circuit identified (left) and the extracted model of the latch-up circuit (right) (adapted from [KL99]).

Firstly, the n-well has higher dopant concentration due to counter doping, so pMOSFETs have poorer parameters than nMOSFETs because the carrier mobility in pMOSFETs degrades due to the counter doping [Has01, LHC86].

Secondly, as shown in Figure 2.3, it is possible for the nMOSFETs and pMOSFETs to form an unfavorable latch up circuit. Latch-up is defined as the generation of a low-impedance path in CMOS chips between the power supply rail and the ground rail due to interaction of parasitic *pnp* and *npn* transistors. Under normal conditions, there is only a high impedance path between the power rails as $Q1$ and $Q2$ are off. As shown in the model of latch up circuits, if there is an increase in the collector current of either parasitic bipolar transistors due to an external disturbance, the transistors will drive each other in positive feedback path. In the worst case, it would destroy the device by forming a too large current [KL99]. To prevent latch up, either the R_{well} or R_{sub} has to be reduced, which could be achieved by increasing the doping level of the well or adding a guard ring to trap the injected minorities, or the gain of the bipolar transistors has to be reduced by increasing the separation distance between opposite type MOSFETs. Usually, the minimal distance between opposite types of MOSFET specified by the design rule of

a process is enough to prevent latch-up in a properly-biased digital circuit. However, when the wells are biased differently as in Compatible Lateral Bipolar Transistors (CLBTs), guard rings have to be added (detailed in Section 4.8).

Thirdly, unlike the bipolar processes, CMOS processes do not require a buried layer as MOSFETs are surface devices, in which the carriers flow near to the $Si - SiO_2$ interface. However, when the MOSFETs are operated as lateral bipolar devices, considerable minorities injected from the source or drain into the body will travel vertically and be collected by the substrate in the absence of buried layers. The lateral gain will then be significantly decreased.

2.4 BiCMOS Technology

CMOS is currently the major technology used in integrated circuit designs. CMOS devices feature high input impedance, low offset switches, high packing density, low switching power consumption, and high scalability. Despite these advantages, CMOS still cannot completely replace bipolar devices not just in analog circuits but also the digital ones since bipolar devices retain some advantages over CMOS, among which are larger capability to drive capacitive loads, larger transconductance, lower 1/f noise, and better matching properties. BiCMOS technologies combine CMOS and bipolar technologies on the same chip so the advantages of both types of transistors can be used together. Then, the low-noise high speed parts could be achieved by bipolar circuits and the low-speed logic parts could be implemented with CMOS. Usually, a typical mixed-signal circuit contains $90 - 95\%$ digital circuits and $5 - 10\%$ analog circuits [Has01].

However, the BiCMOS process cannot just be a simple modification of BJT or CMOS process. Analog BiCMOS processes require at least fifteen masks (in contrast to the baseline of eight masks in BJT and nine masks in CMOS), which is much more complicated. Additional processing steps such as buried

layers, deep $n+$ sinkers, and base diffusions must be included in addition to the CMOS processes. Such complicated process means also higher wafer costs, longer manufacturing time, lower process yields, more difficult controls on the diffusions, and most importantly, more expensive products. Therefore, the inexpensive CLBTs in CMOS provide an attractive alternative to using BiCMOS.

2.5 Summary

In this chapter, modern IC technologies, namely the bipolar, CMOS and BiCMOS processes have been presented. The most commonly used devices, BJTs and MOSFETs were discussed in details, and their structures and modeling were presented.

Chapter 3

Matching Properties

3.1 Introduction

In this chapter, the background of matching properties of MOSFETs and BJTs is presented. The importance and equations of mismatch measurements are discussed. Previous work on the matching properties of MOSFETs and BJTs is summarized. This chapter provides a basis for the discussion of the matching properties of CLBTs.

3.2 Importance of Matched Devices in IC Design

3.2.1 What is Matching?

Matching deals with statistical device differences between pairs of identically designed and identically used active or passive elements such as transistors, resistors, and capacitors [PTV98]. Devices specifically constructed to obtain a known constant ratio are called *matched devices* [Has01]. Mismatch is the process that causes time-independent random variations in physical quantities of such devices. Analog circuits place particularly stringent requirements on

matching resistors, capacitors, and transistors because the vital circuit components, such as operational amplifiers, Digital-to-Analog Converters (DACs), multiplexed analog systems, and reference sources demand highly matched current mirrors and differential pairs for high enough accuracy [Gre92]. Additionally, the trends described in the following subsections make the study of better matching devices become even more important.

3.2.2 Low-power Systems

Matched components are becoming increasingly important since low-voltage circuits have become a major trend and will surely dominate the electronic industry in the future. In digital circuits, the supply voltage is expected to reach $0.5V$ (minimum logic Vdd) by the year of 2011 [Josed]. Firstly, there are more needs for portable systems such as low-power hearing aids, cardiac pacemakers, cellular phones, pagers, portable computers and telecommunications products. Moreover, as transistor density and operating frequency increase, heat dissipation becomes a more urgent problem to be solved, which requires the further lowering of supply voltage. As System-On-a-Chip (SOC) becomes an effective means for realizing cost-effective products and more efficient electronic systems, analog circuits will be restricted to operating under such low power supplies. When the voltage supply decreases, it becomes more difficult to keep the signal-to-offset, or signal-to-noise ratio large enough for accurate operation [IF94]. Analog circuits which work well under conventional voltage supplies may malfunction under low voltage supplies due to the increase in the significance of the mismatch.

3.2.3 Device Size Downward Scaling

The impact of matching also increases as the dimensions of the devices are being reduced. As predicted by the Semiconductor Industry Association (SIA),

the feature size of semiconductor devices would reach $50nm$ in 2011 [Josed]. As a result, the mismatching caused by the limited resolution precision of lithographical process during IC fabrication would become more explicit as the relative error increases.

3.2.4 Analog Circuits and Analog Computing

Even though it has been predicted for years that analog circuits would fade out very soon, there are still strong needs for analog circuits in today's IC industry. For example, Analog-to-Digital Converters (ADCs) and Digital-to-Analog Converters (DACs) are necessary for electronic equipment to interact with the analog physical world. High performance anti-aliasing filters and reconstruction filters are required to implement high speed front ends in communication systems [JM97]. In these circuits, the associated current mirrors and differential pairs should have very good matching properties.

At the same time, there has been an increase in interest in analog computing and neuromorphic engineering in recent years. Neuromorphic Engineering is a field based on the design and fabrication of artificial neural systems, such as vision systems, head-eye systems, and roving robots, whose architecture and design principles are based on those of biological nervous systems [Mea89]. In these two areas, both active and passive elements operate in analog circuits for precise computation. For example, translinear circuits use MOSFETs operating in the subthreshold region for multiplication and logarithmic operations [Min99]. Well matched devices are thus required to realize such systems and the design of precise analog circuits requires a thorough understanding of the matching behavior of components available in any given technology.

3.3 Measurement of Mismatch

Due to the importance of matching properties, extensive studies have been carried out on the matching properties of capacitors [STK84, McC81], MOSFETs [LHC86, PTV98, PDW89, WPM97, HHG98, BSR+95, LWMM98] and bipolar transistors [CE96a, TI96]. Significant results have been achieved, especially for MOSFETs. The followings summarize some of the related theories of matching properties and the important results of the matching properties of MOSFETs and bipolar transistors.

3.3.1 Definitions and Statistics of Mismatch

Two commonly used equation sets

There are different definitions of mismatch in literature [Has01, Gre92, PGJ+95]. In [Has01], the mismatch δ between two devices is usually expressed as a deviation of the measured device ratio from the intended device ratio and is expressed by the following equation:

$$\delta = \frac{\frac{x_2}{x_1} - \frac{X_2}{X_1}}{\frac{X_2}{X_1}} \tag{3.1}$$

where the intended values are X_1 and X_2 and the measured values are x_1 and x_2 [Has01]. For N samples, the mean of the mismatch m_δ is defined as:

$$m_\delta = \frac{1}{N}\sum_{i=1}^{N}\delta_i \tag{3.2}$$

and the standard deviation of the mismatches σ_δ is defined as:

$$\sigma_\delta = \sqrt{\frac{1}{N-1}\sum_{i=1}^{N}(\delta_i - m_\delta)^2} \tag{3.3}$$

Another statistical approach for evaluating the stochastic mismatch between two identically designed elements on the same chip was proposed by Pergoot in 1995 [PGJ+95]. The mismatch between two identical parameters

P1 and P2, measured on two different identically designed elements, is defined as the standard deviation of the normal distribution of N ($N > 30$) absolute differences $\delta_a = \Delta P = (P1 - P2)$ (e.g. for threshold voltage) or relative differences $\delta_r = \Delta P/P = (P1 - P2)/(P1 + P2) * 200[\%]$ (e.g. for transconductance or resistance). The mismatch is thus defined in either of the following forms,

$$\sigma(\Delta P) = \sqrt{\frac{1}{N-1}\sum_{i=1}^{N}(\delta_a - m_{\delta a})^2} \tag{3.4}$$

$$\sigma(\Delta P/P) = \sqrt{\frac{1}{N-1}\sum_{i=1}^{N}(\delta_r - m_{\delta r})^2} \tag{3.5}$$

where $m_{\delta a}$ and $m_{\delta r}$ are the means of δ_a and δ_r respectively.

Formulae used in this thesis

There are two main differences between the above two methods. Firstly, in [Has01], the ratio between the two parameters is emphasized and the intended ratio has to be known while the one in [PGJ+95] requires only the measured values. The first one is especially useful for measuring the mismatch of devices having ratio other than 1 : 1, while the second one is simpler and no absolute intended parameter value is required and only the mean of the measured parameters is used for computation ($(P1 + P2)/2$). Secondly, the first method defined the mismatch as the relative ratios and the second one defined it as the standard deviation of the relative ratios. However, this is not of great importance.

In this thesis, the mismatches of currents in CLBTs and MOSFETs in the arrays will be measured first. Then the adjacent transistors would be paired up as current mirror and their mismatch will be measured. When measuring the mismatch of currents in the MOSFET and CLBT array, the relative differences of the second method are used. Since arrays of independent transistors are used instead of transistor pairs, the mean of the measured current $\bar{I}$ will be used as

the reference. The equation for the mismatch of the measured currents σ_{δ_I} of N transistors is shown as follows:

$$\sigma_{\delta_I} = \sqrt{\frac{1}{N-1}\sum_{i=1}^{N}(\delta_{Ii} - m_{\delta_I})^2} \tag{3.6}$$

where,

$$\delta_{I_i} = \frac{I_i - \bar{I}}{\bar{I}} \tag{3.7}$$

$$m_{\delta_I} = \frac{1}{N}\sum_{i=1}^{N}\delta_{Ii} \tag{3.8}$$

and I_i is the measured current of the ith transistor.

In this work, Equations 3.1 to 3.3 will be used to calculate the mismatch of the transistor pairs.

3.3.2 Types of Mismatches

In general, there are two sources of parameter variations in integrated circuit fabrication processes.

a. Systematic mismatches [STK84, Elz96] These types of mismatches would affect adjacent elements with identical geometries similarly. The main causes include [Has01]:

1. Process Biases - This refers to geometry shrinking or expanding during photolithography, etching, diffusion, and implantation. The process bias is the difference between the drawn width and the actual width of components.
2. Variations in Etch Rate - This refers to the variations in etch rate of oxide by the etchant in different sizes of openings. Since large openings grant more access to the etchant, the etch rate is faster.
3. Stress Gradients - Silicon is piezoresistive, which means that its resistivity will change under different stresses. Due to the tension

produced by the packaging, there is always a gradient of stress, and thus a change of resistivity across the die.

4. Temperature Gradients - According to Equation 2.1, the collector current depends exponentially on the temperature of the device. This is also true for MOSFETs in subthreshold region (Equation 2.4). This temperature effect becomes extremely important when power transistors are built on the same chip as matched devices. The best way to reduce the temperature effect is to put the matched devices in isotherms and far away from the power transistors.

Systematic mismatch will become more serious when the transistors are unequally designed or asymmetrically placed. On the other hand, it can be reduced by proper layout techniques. For example, variations in sheet resistance and junction depth of the implanted and diffused regions across the wafer resulting from non-uniform conditions during the predeposition and diffusion of the impurities could be corrected by using a common-centroid geometry (Figure 3.1).

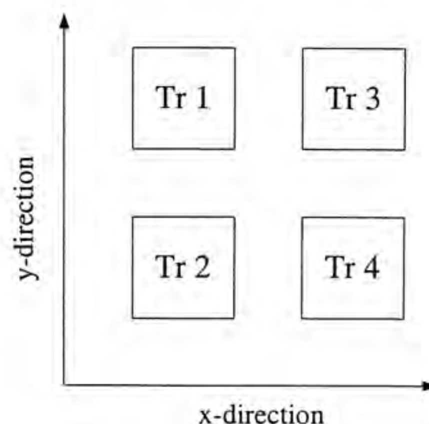

Figure 3.1: Common-centroid layout constructed with 4 unit devices connected as QUAD. Transistor T1=Tr1+Tr4, transistor T2=Tr2+Tr3.

b. Random (Stochastic) mismatches [STK84, Elz96] Such mismatches are caused by random statistical fluctuations and irregularities of the components [Has01]. For example, the edges of the polysilicon exhibit microscopic irregularities, which resulted from the granularity of the polysilicon and imperfections in the photoresist. As a result, the resistors and capacitors, as well as transistors, formed by the polysilicons will vary through the chip. This type of mismatch differs from element to element, and cannot be corrected by layout techniques. They are normally distributed with a mean of zero. Therefore, the only way to reduce the mismatch is to improve the fabrication process and increase the components areas. Random mismatches pose the ultimate limitation on the achievable accuracy for circuit designers.

There are two kinds of fluctuations in this kind of mismatch, peripheral fluctuations (fluctuations that occur only along the edges of the device) and area fluctuations (fluctuations occur throughout the device). When the area to edge length ratio is large enough, the area fluctuations will dominate and the peripheral effects can be neglected. For example, the mismatch of a capacitor with capacitance C can be represented as [Has01]:

$$\sigma_{\delta_C} = \frac{1}{\sqrt{C}}\sqrt{k_a + \frac{k_p}{\sqrt{C}}} \tag{3.9}$$

where k_a and k_p are constants representing the contribution of area fluctuations and peripheral fluctuations respectively. When the area is large enough (with large C), the term containing k_p can be neglected and the mismatch of the capacitors depends only on the area fluctuation.

3.3.3 Matching Properties of MOSFETs

There have been three main types of studies on the matching properties of MOSFETs. Only the first two are of interest in this thesis:

a. Main mismatch sources and matching modeling

Referring to the MOSFET current equations (Equation 2.4 to 2.9), the mismatch of drain current can depend on the threshold voltage V_T, body factor γ and current factor β [PDW89]. However, due to the difficulty in controlling the diffusion process, surface charge formation and oxide thickness, the main source of error is the threshold voltage and the current factor. The mismatch of drain current can thus be represented in terms of the mismatches of V_T and β. Generally, MOSFETs operate in the saturation region in analog circuits. In the saturation region, the mismatches of the drain interconnect paths would make no significant contribution to the current mismatch [LHC86, BGS96]. In this thesis, we only consider the mismatch model for MOSFETs in the saturation region.

In saturation, the variances of the threshold voltage $\sigma^2_{V_T}$ and the current factor σ^2_β [BSR+95, LWMM98, PDW89, LHC86] are represented as:

$$\sigma^2(\Delta V_T) = \frac{A^2_{1VT}}{W_{eff}L_{eff}} + \frac{A^2_{2VT}}{W_{eff}L^2_{eff}} - \frac{A^2_{3VT}}{W^2_{eff}L_{eff}} \tag{3.10}$$

$$\frac{\sigma^2(\Delta \beta)}{\beta^2} = \frac{A^2_{\beta^2}}{W_{eff}L_{eff}} + \frac{A^2_{L^2}}{W_{eff}L^2_{eff}} + \frac{A^2_{W^2}}{W^2_{eff}L_{eff}} \tag{3.11}$$

where V_T and β are the threshold voltage and current factor of the MOS transistor under test, W_{eff} and L_{eff} are the effective gate width and channel length of the MOSFET, and A_{1VT}, A_{2VT}, A_{3VT}, A_{W^2}, A_{L^2} and A_{β^2} are process related constants.

The variance in the drain current can then be derived as:

$$\frac{\sigma^2(\Delta I)}{I^2} = \frac{\sigma^2(\Delta \beta)}{\beta^2} + 4\frac{\sigma^2(\Delta V_T)}{(V_P - V_S)^2} \tag{3.12}$$

where V_S is the Source voltage and V_P is the pinch off voltage.

For large enough transistors ($L_{eff} > 1.2\mu m$) [BSR+95], the second and third term of Equations 3.10 and 3.11 can be neglected. The mismatches of the threshold voltage and current factor are then inversely proportional to the square root of the effective gate area ($W_{eff}L_{eff}$), which is the well-known Law of Area.

$$\sigma(\Delta V_T) = \frac{A_{VT0}}{\sqrt{W_{eff}L_{eff}}} \tag{3.13}$$

$$\frac{\sigma(\Delta\beta)}{\beta} = \frac{A_\beta}{\sqrt{W_{eff}L_{eff}}} \tag{3.14}$$

where A_{1VT} and $A_{\beta 2}$ are restated as A_{VT0} and A_β respectively. Substituting these equations into (3.12), the mismatch of the drain current will also obey the Law of Area:

$$\frac{\sigma(\Delta I)}{I} = \frac{1}{\sqrt{W_{eff}L_{eff}}}\sqrt{A_\beta^2 + 4\frac{A_{VT0}^2}{(V_P - V_S)^2}} \tag{3.15}$$

From the matching model given, the following conclusions can be drawn:

- When the gate length is larger than $1.2\mu m$, the mismatches of the threshold voltage, current factor and drain current of MOSFETs are inversely proportional to the effective gate area (3.13 to 3.15). This suggests that matching will become more and more critical as the technology is scaled down.
- The second and third terms of (3.10) and (3.11) account for the short and narrow channel effects respectively due to edge roughness [BSR+95]. The negative term in (3.10) indicates that the narrow channel effect makes a negative contribution to the mismatch of the threshold voltage. This is because, in contrast to the short channel effect which makes the depletion region controlled by the gate smaller (e.g. Drain-Induced-Barrier Lowering DIBL), the narrow channel effect increases it.

- The mismatch of the drain current depends on the overdrive voltage $V_P - V_S$. If the overdrive voltage is small ($V_{GS} < V_T + 1.5V$ when the slope factor $n \approx 1$), the mismatch in threshold voltage (second term in (3.15)) dominates and the mismatch of the drain current is roughly proportional to $1/\sqrt{I_D}$ as A_β can be neglected and $I_D \propto (V_P - V_S)^2$. This value reaches a maximum and levels off in subthreshold region [LWMM98, FW94].

The matching properties of MOSFETs in the sub-threshold region have not been studied as extensively as that in the saturation region. However, as sub-threshold circuits have become more important in order to reduce power consumption, their matching properties have increased in importance. On the other hand, the matching properties of MOSFETs are simpler in the first order approximation because the mismatch is independent of the current level. The current equation of MOSFET in sub-threshold region in simple form (Equation 2.4) is restated here for convenience:

$$I_D = 2n\beta U_T^2 \exp\frac{V_P}{U_T}(\exp\frac{-V_S}{U_T} - \exp\frac{-V_D}{U_T})$$

When V_D is large enough ($V_D \gg$ a few kT), such as when the drain is connected to the power rail, and V_S is connected to the ground, the equation can be simplified as:

$$I_D = 2n\beta U_T^2 \exp\frac{V_P}{U_T} = I_0 \exp\frac{V_G}{nU_T} \tag{3.16}$$

where $I_0 = 2n\beta U_T^2 \exp\frac{-V_T}{nU_T}$. By differentiating the above equation with respect to I_0, we have,

$$\delta I_D = \exp(\frac{V_G}{nU_T})\delta I_0$$

Rearranging the terms,

$$\frac{\delta I_D}{I_D} = \frac{\delta I_0}{I_0} \tag{3.17}$$

Therefore the mismatch of the drain current is independent of V_{GS}, which means that it is also independent of the current level. This explains why the mismatch of MOSFETs levels off in the subthreshold region [FW94].

Previous research has also shown that nMOSFETs have inherently better matching properties than pMOSFETs [LHC86]. This is because most of the CMOS fabrication processes are optimized for nMOSFETs. As a result, an extra ion implantation step is required to adjust the threshold voltage of pMOSFETs to a suitable value. Due to this additional threshold adjust implant, there is larger variation in the surface concentration in pMOSFETs. As as result, the matching of the threshold voltage in pMOSFETs is poorer than that in nMOSFETs. Furthermore, there is larger mobility variation due to the counterdoping in pMOSFETs.

b. Reducing systemic mismatch

The topography and transistor matching relationship have been studied and it was shown that the common centroid and interdigitated waffle transistor layout structures (Figure 3.2) show almost no systematic mismatch. However, under die stress, the finger style transistor pair shows significant systematic mismatch [BGS96]. Moreover, dummy devices (or

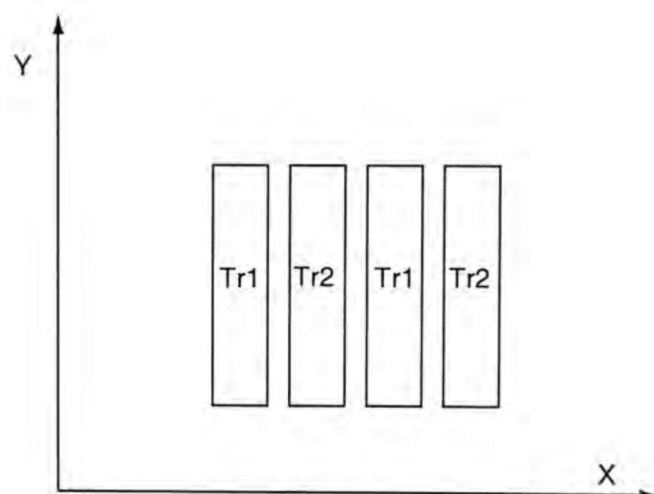

Figure 3.2: Interdigitated finger layout of transistors Tr1 and Tr2.

etch guards) can be added to surround the array of devices to reduce the effect of variations in polysilicon etch rate. The dummy devices have the same spacing between the adjacent devices as that between the devices in the array. So, the boundary devices will not be over etched due to the larger spacing [Has01].

c. Modified MOS structures for reducing random mismatches

Suggestions for changing the structure or fabrication process of standard MOSFETs have also appeared in the literature, such as vertical MOSFETs [RKHS95] or the deposition and etch-back technique [HHG98]. These techniques were not studied or applied in this thesis because only a standard fabrication process was available.

3.3.4 Matching Properties of BJTs and CLBTs

There have been few studies published on the matching properties of bipolar devices [TI96, TP98, Has01, CE96b], especially of CLBTs [Vit83, CHH96, PA89]. Most of the studies dealt with the vertical BJTs and they are summarized below.

Firstly, random fluctuations in base doping, emitter junction area, the densities of recombination center in the emitter base depletion region and Area-to-Periphery ratio are significant sources accounting for the mismatches in BJTs [Has01]. Referring to Equation 2.1, they all play important roles in determining the collector current. The base doping and densities of recombination center are process dependent, which will affect the gains and cannot be controlled by circuit designers. Similar to MOSFETs, the larger the emitter area, the better will be the matching properties because effects of the random errors due to photolithography can be reduced. In vertical BJTs, minorities in base can also pass through the periphery of the base diffusion into the collector in addition to the vertical action (Figure 2.1), which will change the effective

resistance of the collector. Therefore, the Area-to-Periphery ratio should be maximized to reduce the side wall effects. The mismatch of the vertical BJTs due to the variations of emitter area can then be represented as [Has01]:

$$\sigma_{\delta_{I_C}} = \frac{1}{\sqrt{A_E}}\sqrt{k_a + \frac{k_r k_p}{\sqrt{A_E}}} \tag{3.18}$$

where A_E is the vertical emitter area, k_r is a constant, and k_a and k_p are constants representing the contributions of area and peripheral fluctuations respectively. The equation can then be simplified to be the Law of Area when the Area-to-Periphery ratio is large enough [TI96, TP98]:

$$\sigma_{\delta_{I_C}} = \sqrt{\frac{k_a}{A_E}} \tag{3.19}$$

Temperature gradient is another important source of mismatches in BJTs as mentioned in Section 3.3.2. Since the temperature coefficient of the base-emitter voltage is about $-2mV/^{o}C$, that of the collector current then will be equivalent to $80,000ppm/^{o}C$ [Has01]. Therefore, the location of the BJTs differential pairs should be carefully planned and placed far away from any power transistors. Temperature gradient will be a big problem for matching if the power consumption of the chip is high.

For the CLBTs, the above results are still applicable. In addition, there are some important published results that motivated the systematic and quantitative study of matching properties of CLBT in this thesis.

1. It has been shown that gated lateral bipolar action in weakly inverted MOS transistors can improve the matching properties. This shines a light that the matching properties of CLBT would be better than that of MOS [CHH96]. This is because, under the same bias conditions, CLBTs matching mainly depends on geometrical and processing factors (lateral and vertical emitter areas and doping concentration of the base) that are different from and better controlled than those of MOSFETs (length and width of the channel, surface doping and oxide properties) [Arr89] .

2. The CLBTs have been used to implement highly accurate circuits such as a Gilbert gain cell (a two-quadrant analog multiplier) [PA89] and current sources in a silicon cochlea [vSFV96]. Both circuits have demonstrated that CLBTs have better matching properties than MOSFETs.

3. The Law of Area can be applied in bipolar devices where WL is the effective lateral emitter area [TP98].

There have been several studies comparing the matching properties of CLBTs and MOSFETs. In these studies, CLBTs are generally thought and shown to have better matching properties than MOSFETs in these processes and were even used for replacing MOSFETs in some critical matching circuits. However, most of the studies did not make fair enough comparisons between the CLBTs and MOSFETs. They are summarized in Table 3.1.

Paper	Comparisons	Process	CLBT	MOS-FET	Area ratio
[Vit83]	Current Mirror	p-well	npn	n-type	CasM
[PA89]	Current Mirror	$3\mu m$ p-well	npn	n-type	CasM
[CHC96]	Current Mirror	$0.8\mu m$ twin-well	NMOS with BJT action	n-type	1:1
[vSFV96]	Current Mirror	—	npn($1.5\mu m$ p-well)	n-type($2\mu m$ n-well)	—
[RHL97]	Photoreceptor	$2\mu m$ n-well	pnp	p-type	2:1

Table 3.1: Previous results comparing the matching properties of MOSFETs and CLBTs.

The first four publications compared the mismatch of current mirrors and the last one compared the signal-to-offset of a photoreceptor. $CasM$ means that the CLBTs were operated directly as MOSFETs for comparison, which means the gate area is at least 10 times smaller than a normal MOSFET with similar layout area as the CLBT. Therefore, the CLBTs were compared with MOSFETs which had effectively smaller layout areas. It should also

be noted that in [vSFV96], different fabrication processes were used. The CLBT design was fabricated using ECPD15 (a single-poly double-metal 1.5μm CMOS process) at ES2 (Grenoble, France) [vSFV96] while the MOSFET design used a standard double-poly double-metal 2μm CMOS technology at MOSIS [WKLM92]. Moreover, the publications also compared poorer matching MOSFET type in the corresponding process (e.g. nMOSFETs in a p-well process and pMOSFETs in an n-well process) with CLBTs. However, as mentioned in Section 2.3, due to counter doping, the matching properties of the MOSFETs formed in the well is poorer (pMOSFETs are poorer than nMOSFETs in an n-well process and nMOSFETs are poorer than pMOSFETs in a p-well process) [LHC86]. This motivates the comparison between the matching properties of CLBTs with the better matching MOSFET (nMOSFET in n-well process).

3.4 Summary

This chapter has summarized previous research results on the matching properties of CMOS and bipolar devices. Special emphasis was placed on CMOS and the importance of, equations for and factors affecting the mismatches in these devices. It was also pointed out that fairer comparison between MOSFETs and CLBTs are needed because previous research mainly compared the mismatch of MOSFETs of much smaller area than that occupied by the CLBTs.

Chapter 4

CMOS Compatible Lateral Bipolar Transistors (CLBTs)

4.1 Introduction

Compatible Lateral Bipolar Transistors (CLBTs) and Compatible Vertical Bipolar Transistors (CVBTs) are both parasitic bipolar devices found in a CMOS process (Figure 4.1). Since CVBTs can only be used in common-collector configurations, they are of limited use to circuit designers and will not be discussed in detail in this thesis.

In this chapter, the structure and operation of CLBTs are first introduced. Then the DC model proposed by Arreguit [Arr89] is presented. CLBTs are modeled as BJTs with some special characteristics including low current gain and low Early voltage. Moreover, the collector current actually depends on the gate voltage, which is called the residual gate effect. These characteristics are all discussed in detail. Following this, applications of CLBTs in the literature and the design and layout of CLBTs for practical use are presented. Finally, the gains of CLBTs, current-voltage ($I - V$) characteristics of *pnp* CLBTs, *n*MOSFETs, and CLBTs operating as *p*MOSFETs fabricated using the AMI-ABN 1.5μm *n*-well process, and their measurement setup are given.

4.2 Structure and Operation

The structure of a CLBT is the same as that of a MOSFET because it is a parasitic bipolar device in a CMOS process (Figure 4.1). A CLBT has five terminals, namely the emitter E, collector C, base B, substrate S, and gate G, which correspond to the drain D, source S, body (well) B, substrate Sub, and gate G terminals of a MOSFET respectively [Vit83, Arr89]. In order to have the base of a CLBT biased at potentials other than the rails, CLBTs have to be formed in a well. Therefore, only *pnp* CLBTs and *npn* CLBTs could be formed in n-well and p-well processes respectively. It is impossible to realize *pnp* and *npn* CLBTs on the same chip using traditional CMOS processes even in twin-well processes because one type of the well must be connected together to the substrate at Gnd or Vdd (Section 2.3.2). Therefore, BiCMOS process must be used if both types of bipolar devices have to be realized at the same time. Nonetheless, usually only small numbers and only one type of bipolar device are required to implement mix-signal circuits.

Under normal operation conditions, an n-MOSFET formed in a p-well has the substrate and p-well connected to the highest and lowest potentials re-

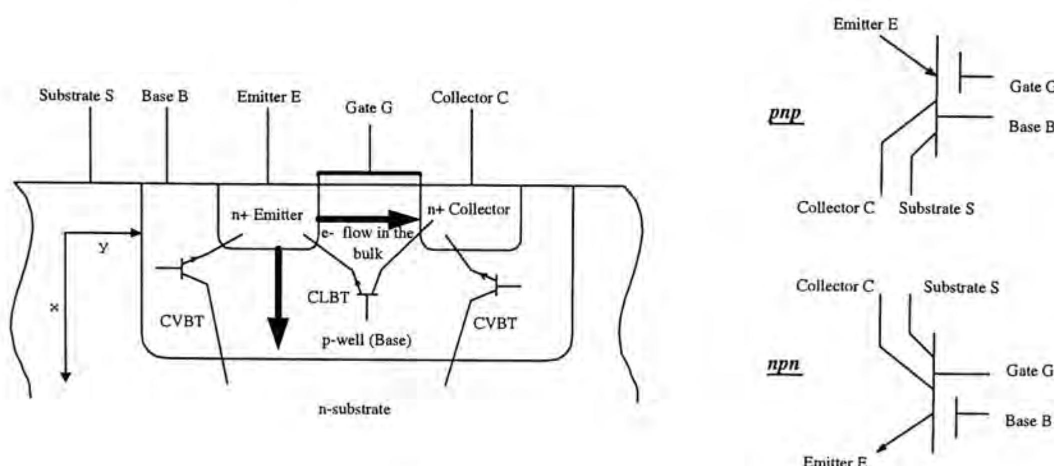

Figure 4.1: The cross-section of an *npn* CLBT with parasitic bipolar transistors identified (left) and symbols for *npn* and *pnp* CLBTs (right).

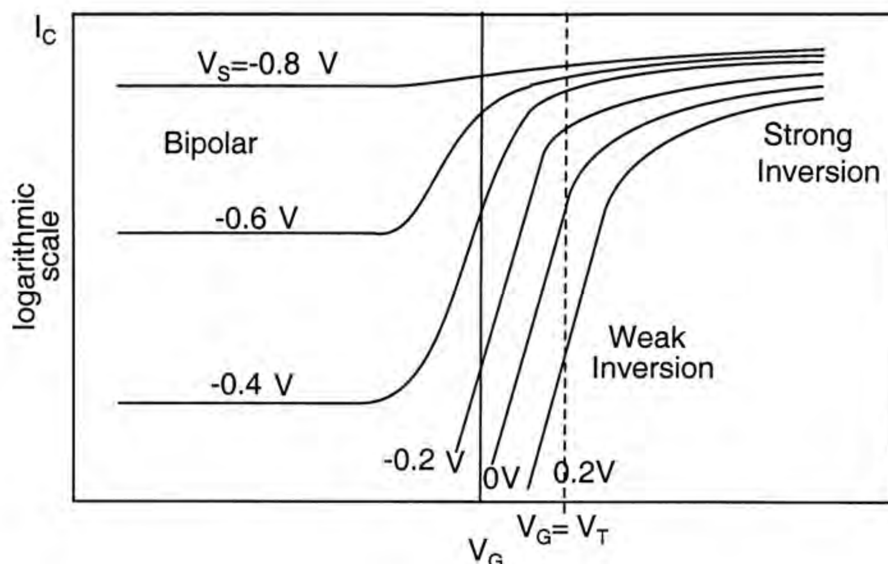

Figure 4.2: Transfer characteristics from source to drain of an *n*MOSFET when V_B and V_D kept at Gnd and Vdd respectively (adapted from [Arr89]).

spectively. The source is connected to a lower potential than the drain. If the gate-source voltage (V_{GS}) is larger than the threshold voltage (V_T), strong inversion occurs and the $I_{DS}(V_{GS})$ transfer characteristics obey a square law as described in Section 2.3 (Equation 2.6). When V_{GS} is lower than the threshold voltage, it is in weak inversion. According to Equation 2.4, it will appear as a straight line when the collector current is plotted against the gate voltage on a log scale (Figure 4.2).

When the gate to well voltage (V_{GB}) becomes negative, there will be accumulation of holes at the interface between the SiO_2 insulating gate and the well. If now, the well is forward biased with respect to the source, electrons will be injected into the *p*-well and then diffuse toward the drain laterally. With a large enough negative gate voltage, the current will be independent of the gate voltage V_G (Figure 4.2). The device is now operating in pure bipolar mode and the source, drain, and well becomes the emitter, collector, and base respectively [Vit83, Arr89]. By applying similar arguments, *p*MOSFETs can operate as *pnp* CLBTs if the gate to well voltage is large enough and they will have a transfer characteristic similar to that shown in Figure 4.2.

However, due to the lack of an n^+ buried layer in the CMOS process, the electrons injected from the emitter into the base (well) will also diffuse into the substrate. The substrate can be regarded as a second collector of a vertical *npn* transistor and, therefore, a CLBT is a 5-terminal device.

4.3 DC Model of CLBTs

DC and AC models of CLBTs were studied systematically in Arreguit's PhD thesis [Arr89]. However, since it is unnecessary to include the AC Model for the understanding of the matching properties of CLBTs, it is not presented.

The DC model of a CLBT in various operation regions can be described with a set of 6 parameters, 3 voltage dependent current sources, which link the 3 junctions of the CLBT two by two, and 3 current gains in a generalized Ebers-Moll model. The 3 junctions are the base-collector (BC), base-emitter (BE), and base-substrate (BS) junctions. This model is suitable for hand calculations. The first order DC model of an *npn* CLBT is shown in Figure 4.3 with the following equations:

$$I_{CE} = f_G I_{ol}(\exp\frac{V_{BE}}{U_T} - \exp\frac{V_{BC}}{U_T}) \quad (4.1)$$

$$I_{SE} = I_{ov}(\exp\frac{V_{BE}}{U_T} - \exp\frac{V_{BS}}{U_T}) \quad (4.2)$$

$$I_{SC} = I_{ow}(\exp\frac{V_{BC}}{U_T} - \exp\frac{V_{BS}}{U_T}) \quad (4.3)$$

$$I_{BE} = \frac{f_G I_{ol} + I_{ov}}{\beta_E}(\exp\frac{V_{BE}}{U_T} - 1) \quad (4.4)$$

$$I_{BC} = \frac{f_G I_{ol} + I_{ow}}{\beta_C}(\exp\frac{V_{BC}}{U_T} - 1) \quad (4.5)$$

$$I_{BS} = \frac{I_{ov} + I_{ow}}{\beta_S}(\exp\frac{V_{BS}}{U_T} - 1) \quad (4.6)$$

$$(4.7)$$

where U_T is the thermal voltage, I_{ol}, I_{ov}, and I_{ow} are constants related to the α−gains of CE, SE and SC respectively and β_E, β_C, and β_S are the

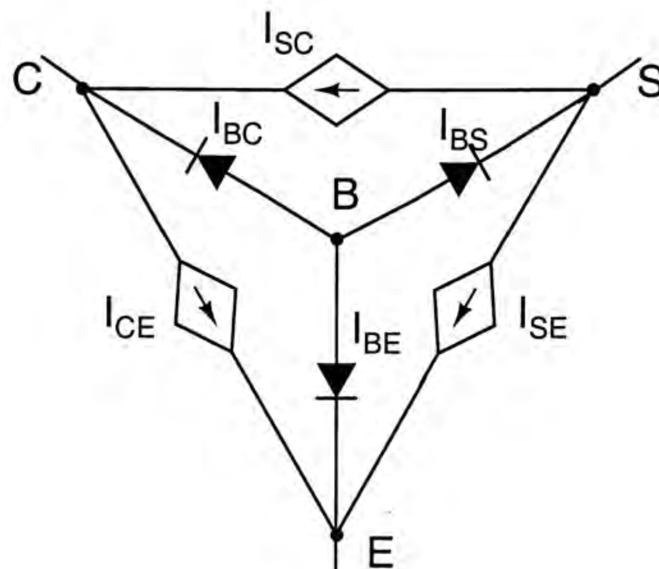

Figure 4.3: First order Ebers-Moll model for *npn* CLBT.

emitter, collector, and substrate forward current gains respectively. f_G is the gate function and is multiplied to account for a non-flat band condition.

Terminal capacitances and resistances could be included for AC and second order effects. A more complicated Gummel-Poon model written in the circuit simulator ESACAP was also implemented by Arreguit. In 1998, *pnp* CLBTs were modeled as a subcircuit of three parasitic bipolar transistors as shown in Figure 4.1 using the SPICE Gummel-Poon model which accounted for the substrate interaction. The model gave accurate fits between the measured ($0.6\mu m$ CMOS *n*-substrate process) and simulated data in both the forward and reverse region of operation over a large bias range ($I_B = -0.1nA$ to $-0.1mA$) [MMMM98].

4.4 Residual Gate Effect in Accumulation

The collector current of a CLBT is supposed to be independent of the gate voltage V_G when V_{GB} is sufficiently low in *npn* CLBTs or sufficiently high in *pnp* CLBTs. However, by analyzing the MOS structure in accumulation mode,

it is found that the gate to well voltage actually has an effect on the lateral collector current. This is known as the residual gate effect [Arr89]. Actually, it was shown that the lateral collector current depended on the gate to base voltage of about 10% over $5V$ for a typical low-voltage Si-gate SACMOS $3\mu m$ process [Ash88].

In accumulation mode, the majority carriers in the substrate will accumulate under the $Si-SiO_2$ interface and the profile of the carriers decreases exponentially away from the interface into the bulk. For example, in nMOSFETs, the density of holes in p-substrate along the x-axis under the gate (Figure 4.1) can be represented as:

$$p(x) = N_A \exp -\frac{\psi}{U_T} \tag{4.8}$$

or

$$-\frac{\psi}{U_T} = \ln\frac{p(x)}{N_A} \tag{4.9}$$

where N_A is the equilibrium hole concentration, ψ is the potential relative to neutral body and U_T is the thermal voltage. By plotting Equation 4.9 with normalized potential for different surface potentials as a function of normalized distance, one can obtain Figure 4.4 [Arr89]. From this graph, we can see that the profile of the accumulated charge is limited to within 2 to 3 Debye lengths (L_D). Since the junction depth of a CLBT is usually more than 10 Debye lengths, the gate only has small effect on the charge concentration and, thus, small effect on the lateral collector current. From the graph, one can also conclude that the larger the surface potential ψ_s, the smaller is the residual gate effect, which is consistent with the previous argument that if the gate to body is biased sufficiently low for an npn CLBT, the gate voltage will not have an effect on the lateral collector current.

The residual gate effect may degrade the matching properties of CLBTs because the lateral collector current now depends on the gate voltage. On the

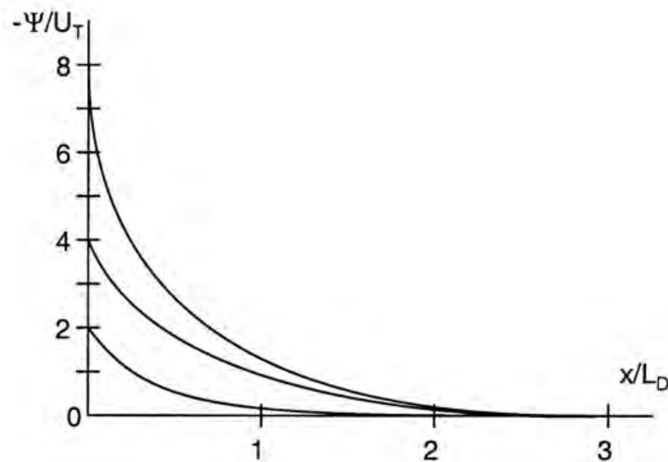

Figure 4.4: Electrostatic potential ψ as a function of normalized x to Debye length L_D. The surface potential ψ_S is $-2, -4, -8$ U_T respectively (adapted from [Arr89]).

other hand, one can utilize such properties to circumvent the different errors inherent in a four-quadrant multiplier [Arr89] or trim an amplifier incorporating CLBTs. In this thesis, such a possibility was investigated and will be presented in Chapter B.

4.5 Main Characteristics of CLBTs

4.5.1 Low Early Voltage

In standard BJT processes, the base region is highly doped with respect to the collector and contacts directly to the lightly doped epitaxial layer of the collector region (Section 2.2). Therefore, they have very high Early voltage. However, as CLBTs are fabricated in standard CMOS processes, the emitter and collector of a CLBT are both highly doped, and the base is lightly doped, this results in a low Early voltage and, thus, low output resistance. This is because when the reverse collector-base voltage increases, the depletion region will increase and occur mainly in the lowly doped base side, thus the effective base width decreases and the rate electrons get injected into collector

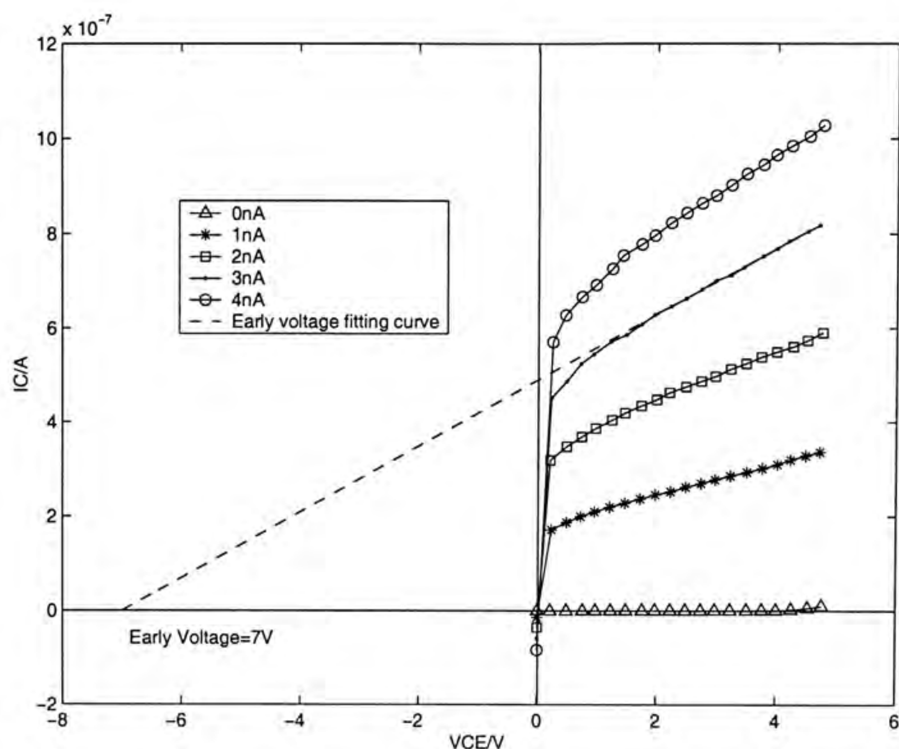

Figure 4.5: The current-voltage characteristics of a *pnp* CLBT fabricated using AMI-ABN $1.5\mu m$ n-well CMOS process without cascode. The Early voltage is about $7V$.

increases (Section 2.2). Moreover, lower Early voltage also means that the drain current would depend more on the gate-collector voltage. As a result, the matching properties would be affected by the applied gate voltage. One way to improve the output impedance is to use a cascode circuit (detailed in Section 4.6) [Arr89, vSFV96]. Figure 4.5 shows the current-voltage characteristics of a *pnp* CLBT fabricated with a standard $1.5\mu m$ process. It can be seen that the Early voltage is approximately $7V$.

4.5.2 Low Lateral Current Gain at High Current Levels

The base width of the lateral transistor is approximately the distance between the source and drain, and is usually larger than that ($0.1\mu m$ for superbeta bipolar transistor) in a bipolar process [GM93]. Moreover, in the absence of the buried layer in CMOS processes, there will be vertical bipolar action in

addition to the lateral bipolar action. A considerable portion of the injected minorities in the base region will diffuse vertically and be collected by the substrate. Therefore, the lateral current gain I_C/I_B is generally smaller than the gains of the vertical bipolar transistors [LHIK69]. At low current levels, the lateral component dominates, while at high current levels, the voltage drop across the lateral emitter resistance leads to a debiasing of the sidewall junction and reduces the lateral component. The vertical component then dominates and current-crowding is observed under the emitter contact [MMMM98]. That means the gain is low for CLBT at high current levels.

However, due to downward technology scaling, the channel length of MOSFETs will decrease and is expected to reach $0.05\mu m$ in 2011 [Josed]. This becomes comparable with the base width of superbeta bipolar transistors. Moreover, as low-power devices also dominate (detailed in Section 3.2.2), CLBTs would be operated under low current levels. These two points may make CLBTs more versatile in low power applications. In fact, as shown in Figure 4.5, the gain at a 1nA base current level can reach about 300 in a $1.5\mu m$ CMOS process.

4.5.3 Other Issues

In a $0.6\mu m$ n-well process, it has been shown that the lateral $\alpha_L = -\frac{I_C}{I_E}$ is in the range from 0.6 to 0.8 and vertical $\alpha_V = -\frac{I_S}{I_E}$ in the range from 0.2 to 0.4 [MMMM98]. It is difficult to increase α_L because of the lack of a buried layer.

Since the emitter area is the lateral one, layout area increases quadratically as the lateral emitter area increases. As a result, the vertical bipolar action will increase faster than the lateral one. Therefore, without buried layers, a CLBT with minimum emitter layout area will give the maximum lateral current gain.

To address the issue of the relationship between the lateral (A_l) and vertical

(A_v) emitter areas, by assuming a square emitter with side length l, an Area-to-Periphery (A/P) ratio is introduced and defined as,

$$A/P\ ratio = \frac{A_v}{l} = \frac{l^2}{l} = l \tag{4.10}$$

Since the effective diffusion depth (d) of the emitter and collector of the CLBT can be regarded as a constant in the same fabrication process, the A/P ratio is thus proportional to the ratio of the vertical to lateral emitter area (A_v/A_l) because

$$\frac{A_v}{A_l} = \frac{l^2}{4 \times l \times d} = \frac{l}{4 \times d} \propto l$$

4.6 Enhanced CLBTs with Cascode Circuit

To solve the problem of low Early voltage, cascode circuits [Arr89, vSFV96] can be used as shown in Figure 4.6. The *pnp* CLBT is cascoded with a *p*MOSFET sharing the same *n*-well. Therefore, the bulk of the cascode transistor and the base of the CLBT will have the same voltage. V_{cas} is the applied gate voltage of the cascode transistor and should be chosen to ensure that the CLBT is never saturated and that the *p*MOSFET transistor is in the saturation mode.

Figure 4.6: Structure (left) and layout (right) of cascoded *pnp* CLBT.

By using an nMOSFET in the same p-well, one can construct a cascoded *npn* CLBT. The resulting current-voltage characteristics of cascoded CLBTs will be presented in Section 4.9.

4.7 Applications

Various analog applications have incorporated CLBTs due to their good matching properties and compatibility with the CMOS process. Applications include:

Four-quadrant multiplier and precision compressor gain controller Arreguit has built four-quadrant multiplier and compressor gain controller with CLBTs using $3\mu m$ CMOS process. The residual gate effect has been used to circumvent the different errors inherent in the multiplier [Arr89].

Exponential filters for silicon cochlea [vSFV96] CLBTs were used as current mirrors in exponentially scaled filters for modeling silicon cochlea. The frequency responses of the silicon cochlea were shown to have higher regularities in the cut-off frequencies and gain by using CLBTs. It was because the current sources implemented with CLBTs had better matching properties than those implemented with MOSFETs in the subthreshold region.

Low-voltage CMOS bandgap reference [Vit83, DLVO85] Bandgap voltage references are accurate voltage references which are almost independent of temperature. They are better implemented with bipolar devices than MOSFETs. Although simple voltage references can be implemented with substrate bipolar devices (vertical BJTs), CLBTs provide higher flexibilities. For example, they have been used for building low output impedance bandgap reference [DLVO85]. Therefore, in CMOS processes, CLBT is a very good candidate for building bandgap voltage references.

Logarithmic photoreceptor [RHL97] CLBTs have been incorporated in a logarithmic photoreceptor for improving matching and dynamic range. Traditionally, *p*MOSFETs are used as the load devices which would only exhibit a logarithmic response when operating in the subthreshold region. CLBTs exhibit a logarithmic current-to-voltage relationship over a larger range of currents. As a result, the dynamic range was increased to 7 to 8 order of magnitudes instead of 4 to 5 in the case of a *p*MOSFET load. Moreover, the matching properties of CLBTs are better than *p*MOSFET and the Signal-to-Offset (S/O) ratio of the receptor was shown to be 31% to 137% better than that for *p*MOSFET loads.

High gain SOI photodetector [ZCFK98] The CLBTs were also incorporated on SOI substrate as a photodetector which could provide higher current amplification over conventional phototransistors due to the vertical bending induced by an n^+ gate.

4.8 Design and Layout of CLBTs

The CLBTs used in this thesis follow the same design shown in Figure 4.6, except that a p^+ guard ring was added to surround each CLBT and the Magic layout of a *pnp* CLBT is shown in Figure 4.7.

In the normal operations of a CLBT, the base-emitter junction is forward biased and, thus, there always will be minorities injecting from the emitter into the base, which is the well of a MOSFET. Therefore, the chance of latch-up will increase if there is a MOSFET of an opposite type adjacent to the CLBT and the minimum spacing rules for designing the CMOS circuits then become insufficient for preventing latch-up (Section 2.3.2). So, CLBTs for densely packed chips must be surrounded with guard rings to minimize the latch-up probability [Ker, Arr89]. One method of constructing the guard rings is to surround the well with a majority collector. For instance, a p^+ diffusion

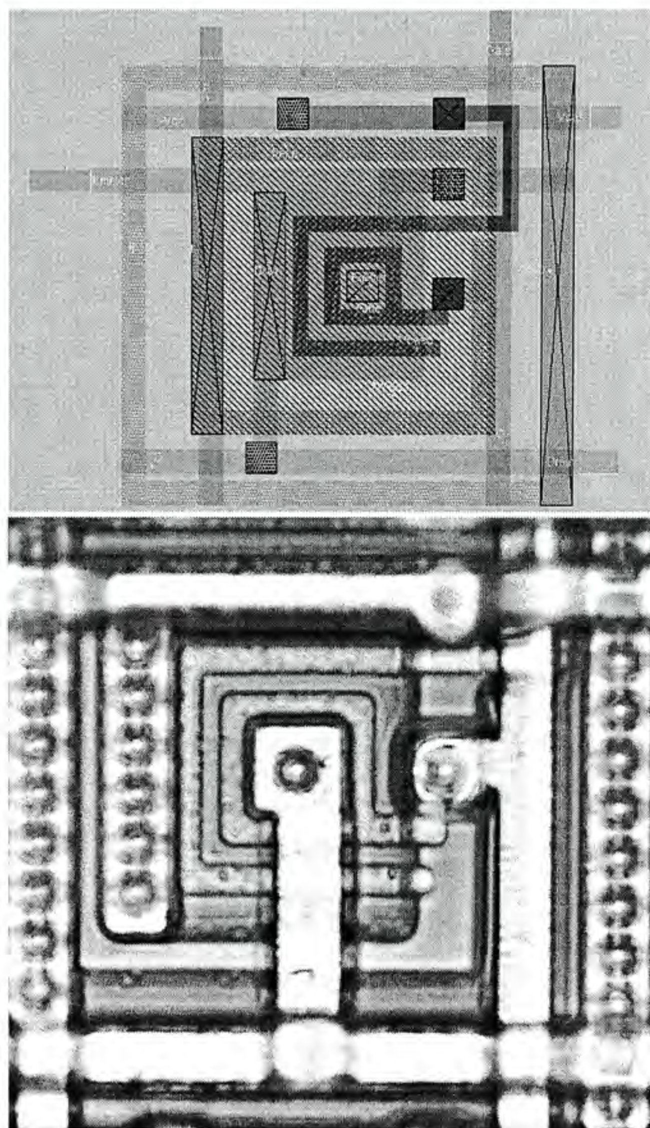

Figure 4.7: Magic layout (top) and the photomicrograph (bottom) of a *pnp* CLBT cell with cascoded circuit. The outermost ring is the guard ring connected to *Gnd*.

ring biased at *Gnd* surrounding a *pnp* CLBT will be effectively collecting the majority carriers, holes, drifted into the *p*-substrate from the *n*-well, and thus reducing the substrate resistance R_{sub} and the feedback effect of the latch-up circuit (Figure 2.3). In order to have a fair comparison, guard rings were added to the CLBTs in the CLBT matching properties test chips.

The characteristics of the CLBT shown in Figure 4.7 are summarized as:

- The collector surrounds the emitter to increase the lateral emitter area

	without Guard Ring	with Guard Ring
bare	$35 \times 40 = 1400\lambda^2$	$48 \times 54 = 2592\lambda^2$
cascoded	$43 \times 44 = 1892\lambda^2$	$56 \times 58 = 3248\lambda^2$

Table 4.1: The areas of different structures of CLBTs (λ^2). In this thesis, $\lambda = 0.8\mu m$ was used. Bare CLBT refers to CLBT not cascoded.

and so, increase the lateral collector current with respect to the vertical one. This is a common approach used in circuit applications of CLBTs [Arr89, vSFV96].

- A p^+-ring surrounds the well and is connected to ground. This will absorb holes injected from the n-well into the substrate to reduce the chance of latching up.
- The structure is made as compact as possible to improve large and small signal characteristics.
- A cascode pMOSFET is incorporated in the cell to reduce the Early effect.

In some applications, CLBTs need not be cascoded. The CLBTs may also share the same guard rings. Table 4.1 summarized the areas of the variations of CLBTs.

4.9 Experimental Results of Single *pnp* CLBT, *n*MOSFET and *p*MOSFET

Besides arrays of *pnp* CLBTs and *n*MOSFETs (detailed in Chapter 5), there are also isolated devices in the test chips fabricated for extracting the $I-V$ transfer characteristics. The AMI-ABN $1.5\mu m$ n-well process (detailed in Section 5.3) was used and two batches of test chips were fabricated and the

process parameters are listed in Appendixes C and D respectively. In the first batch, there are isolated cascoded *pnp* CLBTs with guard rings with vertical emitter area of $6 \times 6\ \lambda^2$. The terminals of this CLBTs were connected directly to the I/O pins. In the second batch, there are isolated bare *pnp* CLBTs (CLBTs without cascode *p*MOSFETs) with vertical emitter area of 6×6, 10×10, and $34 \times 34\lambda^2$ respectively, which means their Area-to-Periphery (A/P) ratios are 6, 10 and 34λ respectively. These CLBTs share the same terminals and are selected by the transmission gates. Therefore, 4-wire sense technique was required when measuring these CLBTs. There is no isolated *n*MOSFETs in both batches, one *n*MOSFET in the MOSFET array was selected for extracting the $I - V$ characteristics in batch 2.

The following data was measured and analyzed using the measurement system detailed in Section 5.7:

1. The current gains at different base current level (from $0.1nA$ to $1mA$) of bare *pnp* CLBTs of different sizes were measured. (Figure 4.8).

2. The $I - V$ characteristics of the CLBTs from source to drain as a function of $Vs - Vb$ and $Vb - Vg$ were measured and plotted (Figure 4.9 and 4.10). These graphs were used to determine the gate voltage required for operating a MOSFET in pure bipolar mode.

3. The $I - V$ characteristics of the cascoded and bare *pnp* CLBTs with nA-order base current level were measured and plotted (Figure 4.11 and 4.12).

4. The $I - V$ characteristics of *n*MOSFETs were measured and plotted (Figure 4.13).

5. The transfer characteristics of cascoded and bare *pnp* CLBTs operating as *p*MOSFETs were measured and plotted (Figure 4.15).

4.9.1 CLBT Gains

The gains ($\beta = \frac{I_C}{I_B}$) of the bare *pnp* CLBTs with different sizes were measured and plotted in Figure 4.8. The gain was measured by applying different base currents (I_B) to the selected device, by fixing the emitter and collector voltages at $5V$ and Gnd respectively. It can be seen that the gain of the CLBTs increases as current level decreases. This is mainly due to the high level injection which was explained in Section 4.5.2. Although the current gain should be independent of the emitter area as predicted by Equation 2.3, the graph shows that the gain of CLBT with larger A/P ratio is lower. This can be explained by the fact that the lateral to vertical emitter area ratio decreases when A/P ratio is increasing. Therefore, the lateral current gain decreases. The results

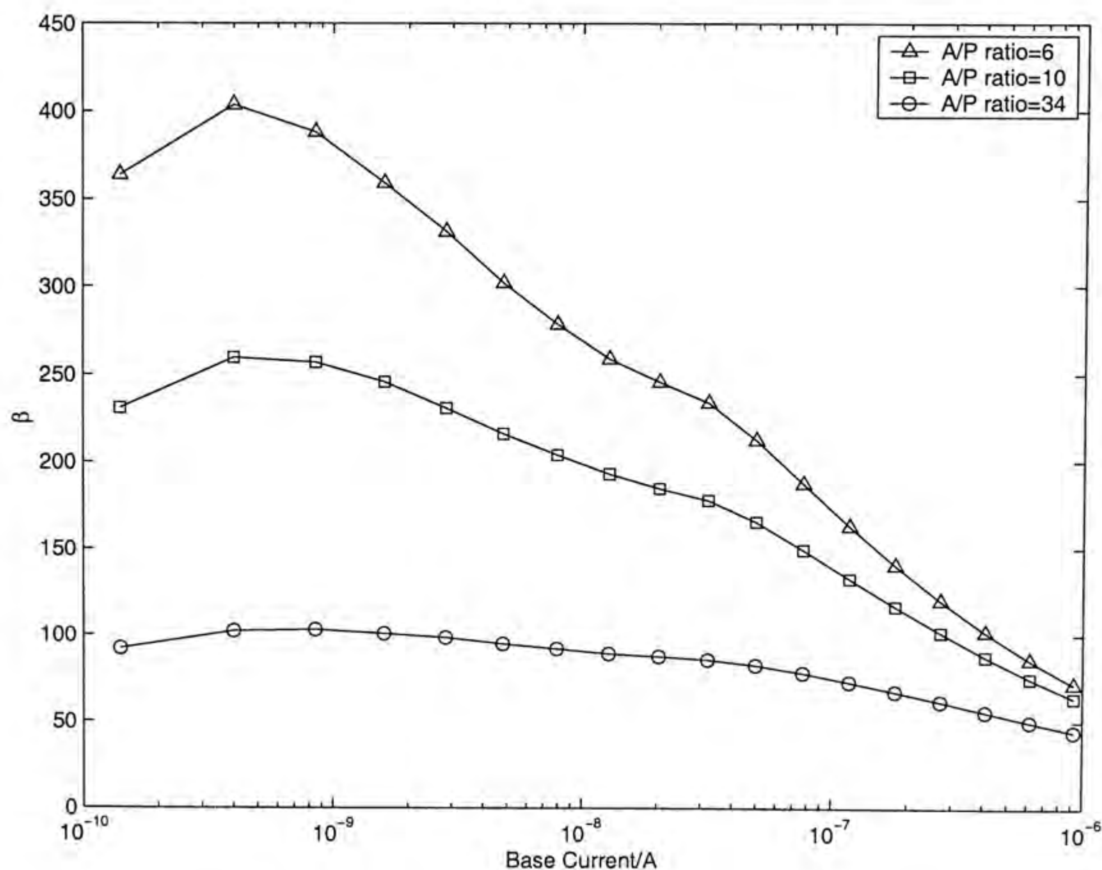

Figure 4.8: Current gains of bare *pnp* CLBTs with different Area-to-Periphery (A/P) ratio.

confirm that the gain of the CLBTs without buried layer depends also on the A/P ratio. To obtain maximum lateral gain, the smallest A/P ratio should be used, which means the emitter should be a square if triangular layout is not possible.

4.9.2 Gate Voltage Required for Pure Bipolar Action

Figure 4.9 shows the transfer characteristics from source to drain of the bare *pnp* CLBT with minimum emitter area (A/P ratio of 6) under different gate voltages. The well (base) and the drain were biased at $5V$ and $0V$ respectively and all the measurements were taken with respect to the base voltage. V_{SB} was swept from $-0.4V$ to $1V$ and the drain current was measured for different gate voltage V_G. For low V_G ($V_G < 5V$), the curve is a typical MOSFET one,

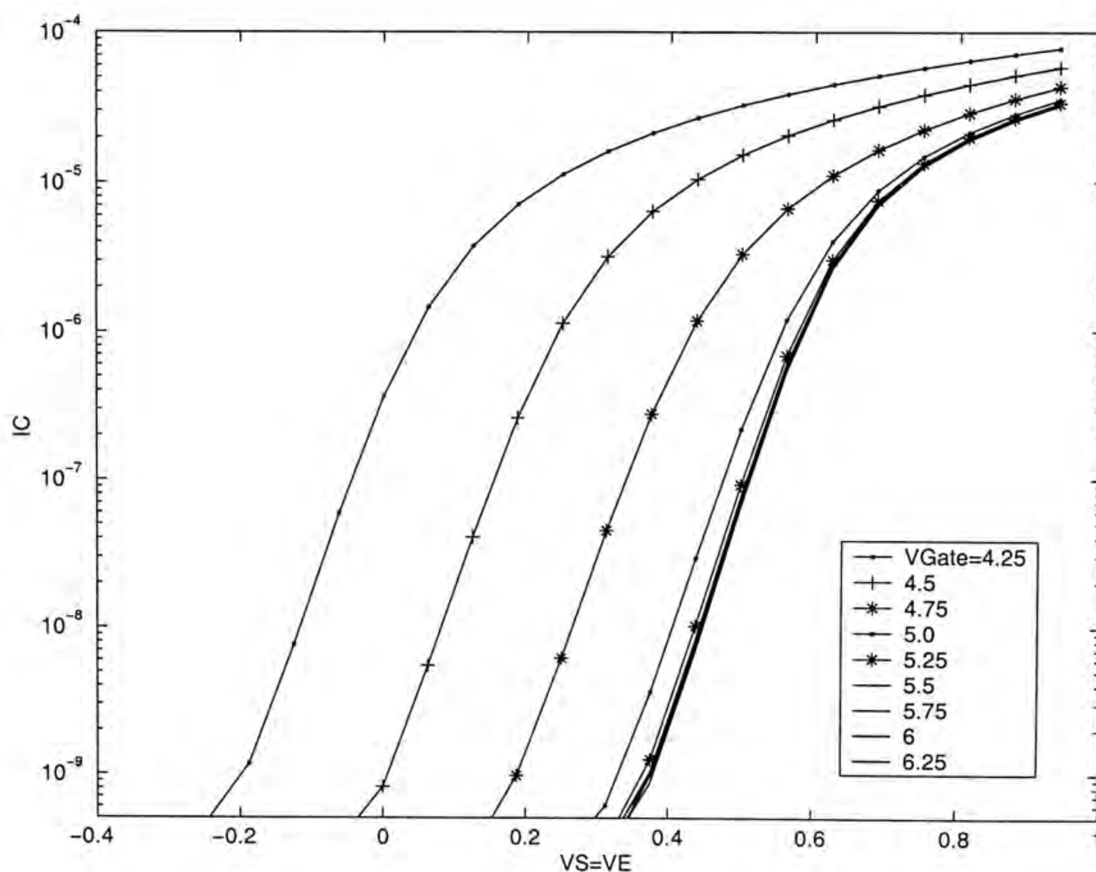

Figure 4.9: Transfer Characteristics from source to drain as a function of Vs-Vb.

beginning in the subthreshold region and enters the quadratic region as V_{SB} increases. However, as the V_G increases, the curves become indistinguishable, which means that the drain current no longer depend on the gate voltage. This mode is the pure bipolar mode. In pure bipolar mode, the curves were expected to be straight lines in the logarithmic plot. However, due to the high level injection, they level off when I_C reaches several μA. From the graph, the voltage required to enter bipolar mode is approximately $5.5V$. However, in order to minimize the residual gate effect, the gate voltages were set at $6V$ to $7V$ in the following experiments.

Figure 4.10 shows the transfer characteristics from source to drain of the bare *pnp* CLBT as a function of $V_B - V_G$ with $V_B = 5V$. This graph shows how the device changed from strong inversion to weak inversion and then to

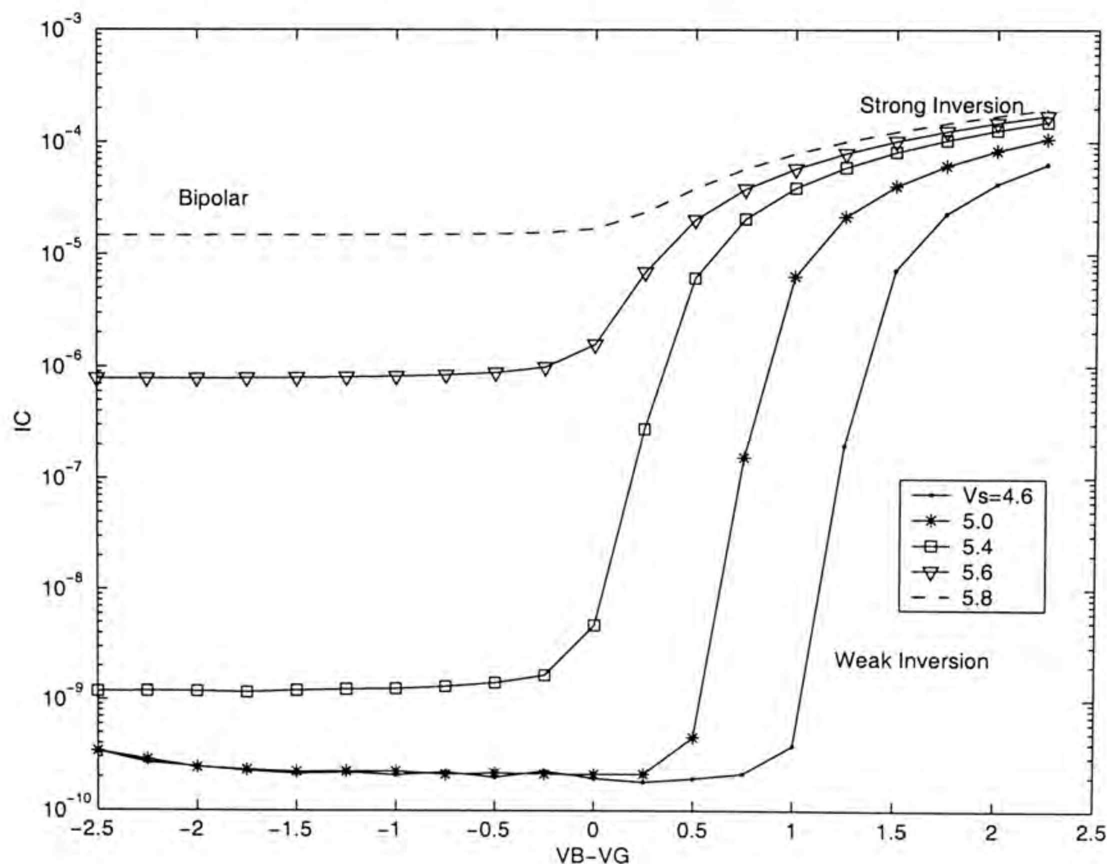

Figure 4.10: Transfer Characteristics from source to drain as a function of Vb-Vg.

bipolar under different biases. This graph is consistent with Figure 4.2 and explained in detail in Section 4.2.

4.9.3 $I-V$ and Other Characteristics of Bare *pnp* CLBTs

The bare *pnp* CLBTs with vertical emitter areas of $6 \times 6\lambda^2$, $10 \times 10\lambda^2$, and $34 \times 34\lambda^2$ were tested. The $I - V$ characteristics of the *pnp* CLBTs with minimum emitter area are shown in Figure 4.11. The emitter and gate were biased at $5V$ and $6.51V$ respectively. Different base currents were then applied with the collector voltage sweeping from $0V$ to $5V$. The corresponding collector voltages and currents were then measured. It was found that the Early voltage was very low, approximately $7.7V$. This suggests that a cascode circuit is required for practical use. Table 4.2 shows the gains and Early voltages at $1nA$ current levels of the isolated CLBTs for comparison.

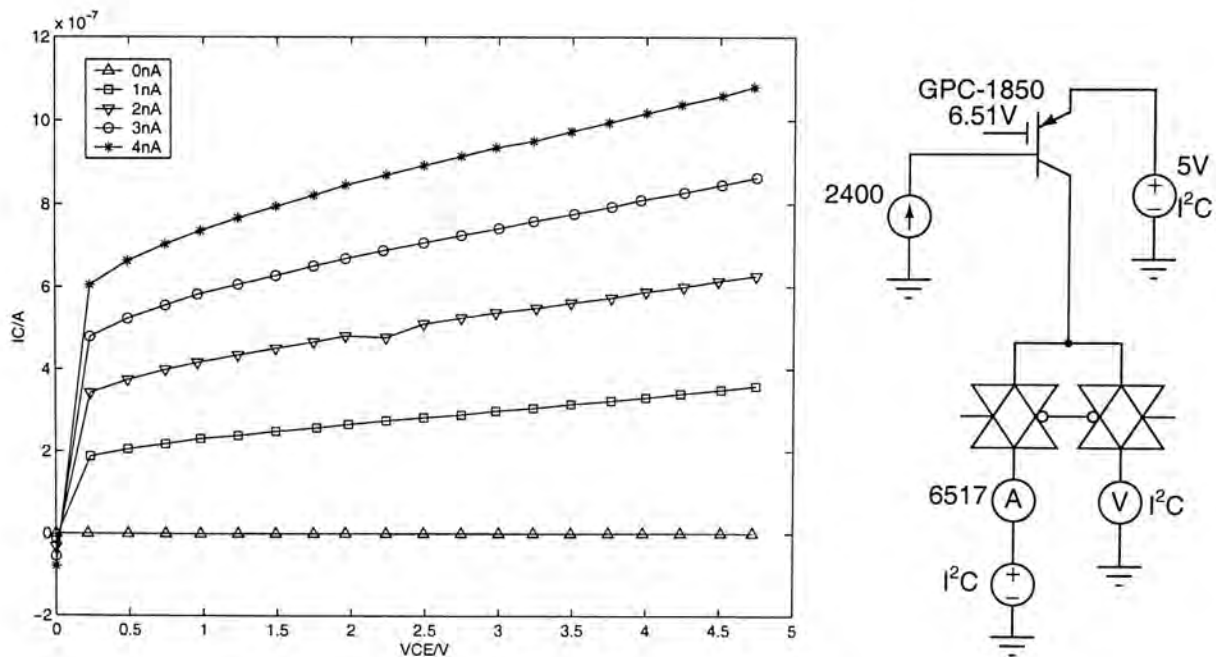

Figure 4.11: Transfer characteristics of bare CLBTs (left) and the measurement setup (right).

	CLBT 1	CLBT 2	CLBT 3
Vertical Emitter Area λ^2	6×6	10×10	34×34
Area to Periphery Ratio λ	6	10	34
Lateral Emitter Area Ratio	6	10	34
Current Gain	270	194	88
Early Voltage	7.7V	6.5V	4.1V

Table 4.2: Characteristics of CLBTs of different sizes.

4.9.4 Transfer Characteristics of a Cascoded *pnp* CLBT

The transfer characteristics of a cascoded *pnp* CLBT with vertical emitter area of $6 \times 6\lambda^2$ and the measurement setup are shown in Figure 4.12. It can be seen that under the bipolar operating condition, the MOSFET operates well as a bipolar device. The V_{cas} was set to $3V$ and V_{gate} to $6.51V$. The emitter voltage was fixed at $5V$ with the collector voltage sweeping from $0V$ to $5V$ at different value of I_B. The gain at base current level of nA order is about 250 which agrees with our previous measurement of the gain. Moreover, with the

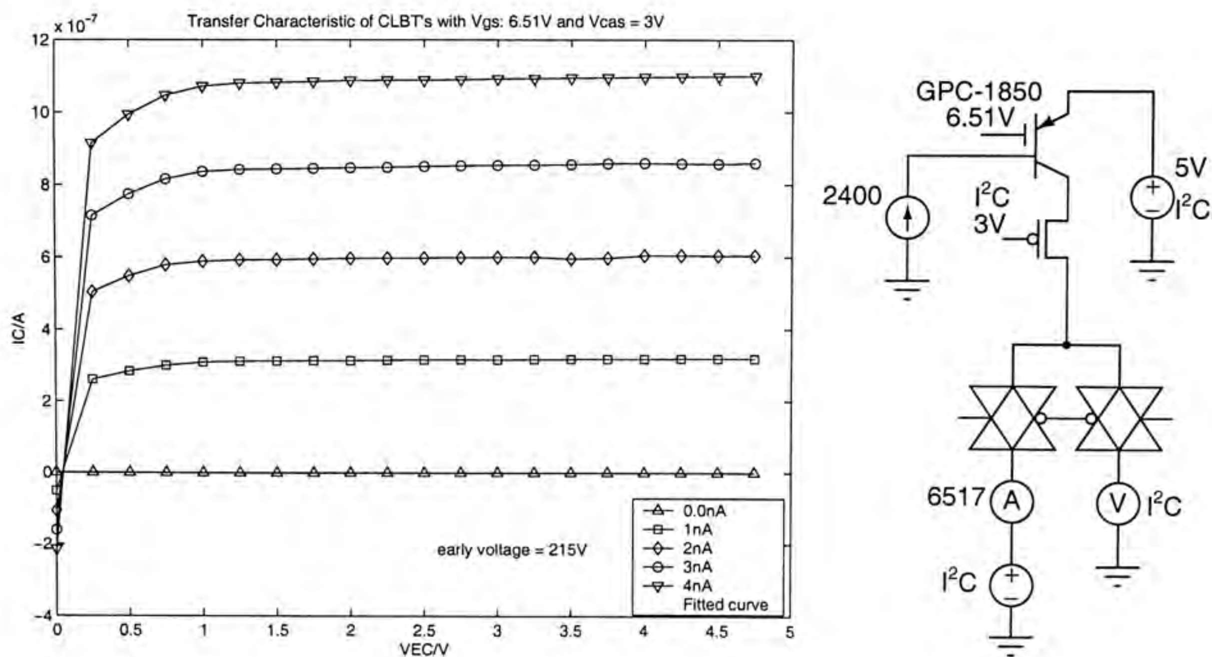

Figure 4.12: Transfer characteristics of cascoded CLBTs (left) and the measurement setup (right).

cascode *p*MOSFET, we can achieve Early Voltage as large as $215V$, making it suitable for many applications.

4.9.5 Transfer Characteristics of an *n*MOSFET

The transfer characteristics of the *n*MOSFET were found by fixing the gate voltage at different levels and sweeping V_{DS} to measure the drain current (Figure 4.13). Since there were a large potential drop across the transmission gate of the selected device at high drain current levels, the V_{DS} was sensed

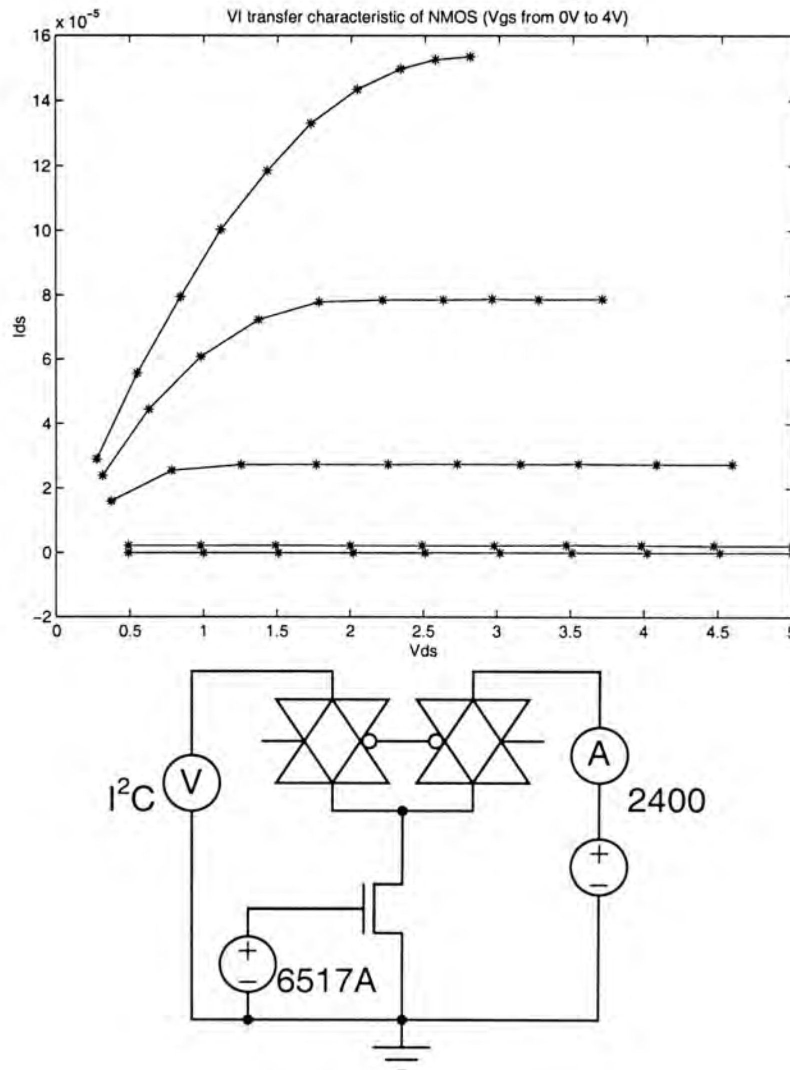

Figure 4.13: Transfer Characteristics of *n*MOSFET (top) and the measurement setup (bottom).

at the sense port for the plots. As a result, the V_{DS} could not reach $3V$ at high current levels even though the I^2C board (described in Section 5.7) was programmed to apply $V_{DS} = 5V$.

4.9.6 Transfer Characteristics of Cascoded and Bare CLBTs Operating as *p*MOSFETs

The transfer characteristics of the bare and cascoded *pnp* CLBTs with vertical emitter area of $6 \times 6\lambda^2$ operating as *p*MOSFETs were also measured and the measured setup are shown in Figure 4.14 and 4.15. Like the case in measuring the $I - V$ characteristics of *n*MOSFET, a 4-wire sense technique was used for bare *pnp* CLBTs. However, since the cascoded *pnp* was isolated with the terminals connected directly to the pins of the chips, 4-wire sense technique was not required. Therefore the V_{DS} were the same as the applied voltages.

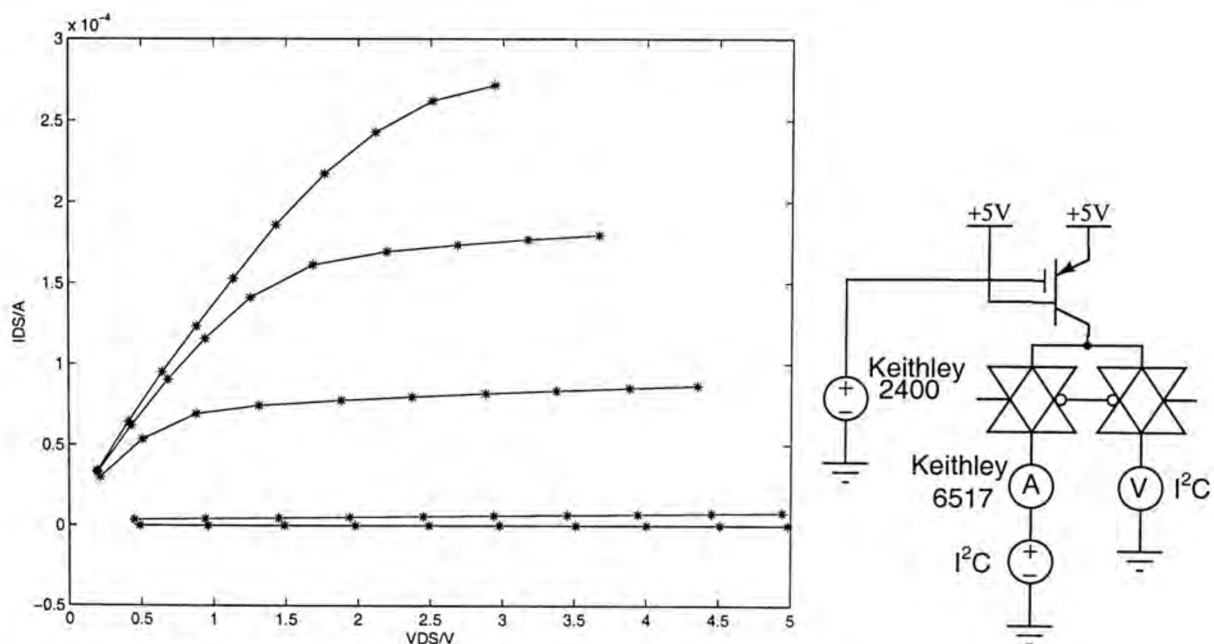

Figure 4.14: Transfer characteristics of bare CLBT operating as *p*MOSFET at V_{GS} from $0V$ to $4V$ (left) and the measurement setup (right).

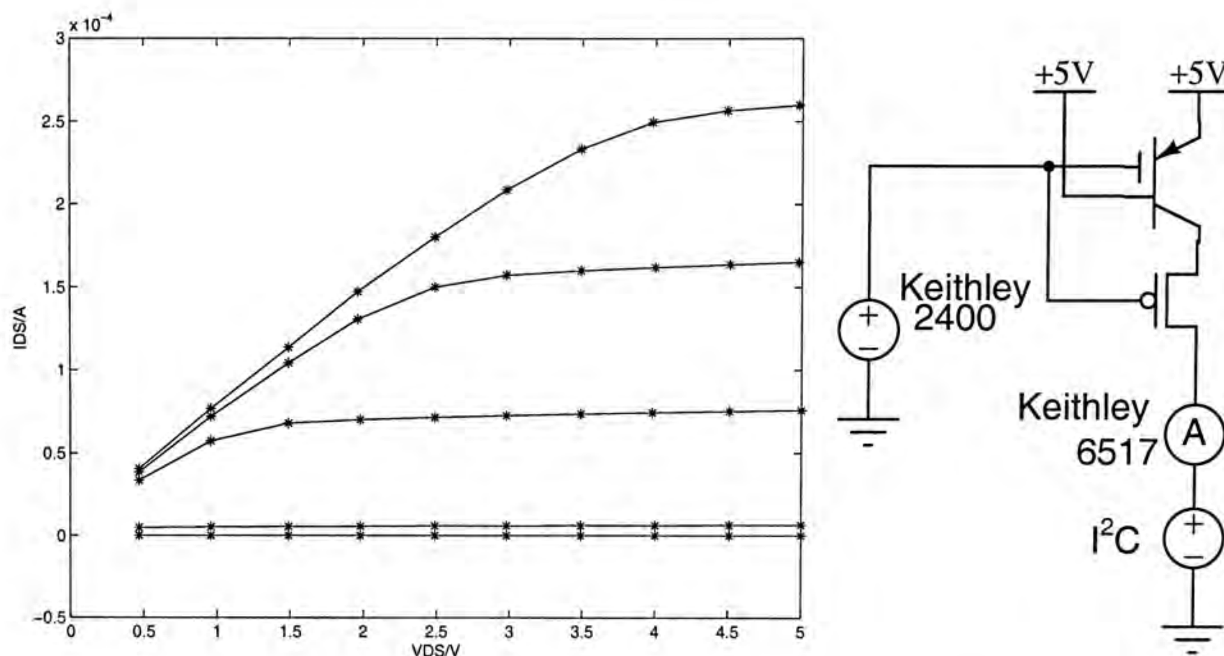

Figure 4.15: Transfer characteristics of cascoded CLBT operating as pMOSFET at V_{GS} from $0V$ to $4V$ (left) and the measurement setup (right).

4.10 Summary

This chapter presented the structure and principles of the operation of CLBTs. The DC model has been reviewed and the residual gate effect and main characteristics were discussed. It was found that the Early voltage of a CLBT can be as low as $7V$. However, CLBTs have better performance in low current level operations and in fact, its gain can be as high as 300 at $1nA$ base current. Cascoded CLBTs and guard rings were introduced to facilitate the operation of CLBTs in practical circuits. The measured $I-V$ transfer characteristics of pnp CLBTs, nMOSFETs and CLBTs operating as pMOSFETs were presented and it was should that CLBTs exhibited higher gain ($\beta_F = 300$ at $I_B = 1nA$) at low current levels. The cascoded CLBT has a measured Early voltage larger than $200V$ which is a large improvement over the bare CLBT with an Early voltage of $7V$.

Chapter 5

Experiments on Matching Properties

5.1 Introduction

In this chapter, the design of the matching properties test chip is first presented. In order to test large number of MOSFETs and CLBTs on a chip with limited pins, the devices are organized in arrays and shift registers and transmission gates are used for selecting individual devices for testing. The structures of the test chip will be explained in detail. Then the setups and procedures for testing the mismatches of *pnp* CLBTs, *n*MOSFETs, and CLBTs operating as *p*MOSFETs, are given. The mismatches of each type of the devices in every chip at different current levels will be presented. A three dimensional plot of the distribution of the current in each device array at $100nA$ level in a particular chip will be shown for qualitative analysis of the causes of mismatches in that device. Finally, devices are paired up as current mirrors and their mismatches are calculated and compared.

5.2 Objectives

The current matching properties of CLBTs and MOSFETs fabricated with a standard CMOS process were compared. The process chosen was the AMI-ABN $1.5\mu m$ n-well process, in which only *pnp* CLBTs could be fabricated. Since nMOSFETs are more common in circuit design and show better matching properties than pMOSFETs, nMOSFETs are tested and compared with *pnp* CLBTs [LHC86]. Of course, the nMOSFETs need to be of similar size as the CLBTs for a fair comparison since matching properties depend heavily on the layout area. The *pnp* CLBTs were also operated as pMOSFETs and their matching properties were tested. The Law of Area was then applied to the pMOSFETs so that the current matching properties between the nMOSFETs, pMOSFETs and *pnp* CLBTs could be compared.

As matching properties are stochastic processes, a large number of identical device need to be fabricated to get statistically significant data. Figure 5.1 shows the block diagram of the test chip. There are two 15×15 test arrays,

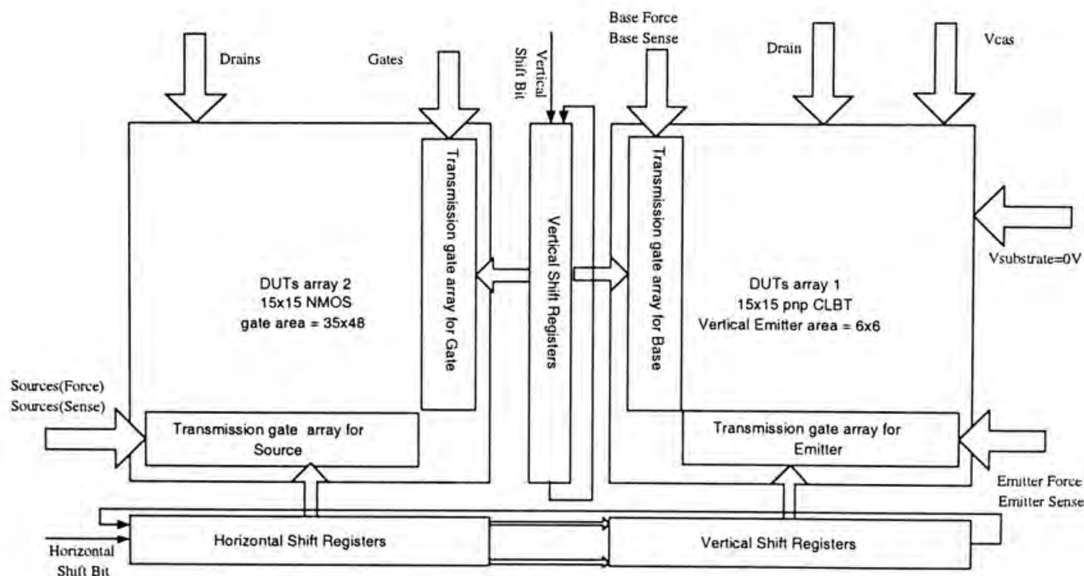

Figure 5.1: Top structure of the first batch matching properties test chips (array 1 was modified in the second batch).

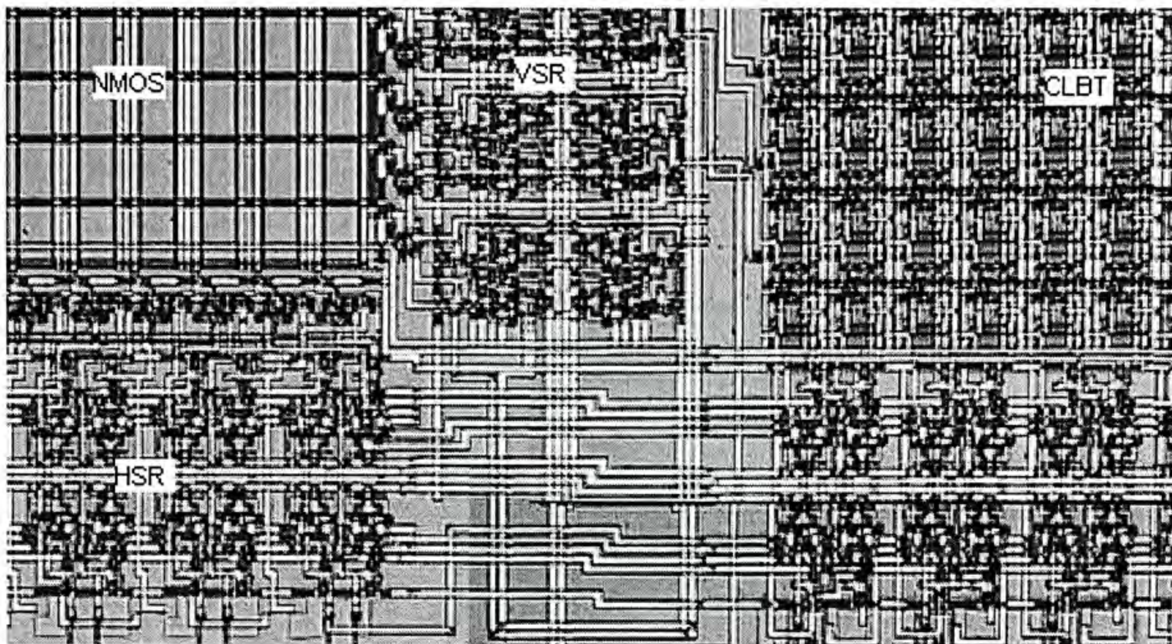

Figure 5.2: The photomicrograph of the test arrays of the second batch. HSR and VSR are the horizontal and vertical shift registers respectively.

giving a total of 225 Devices Under Test (DUTs) in each array. Array 1 is the array of cascoded *pnp* CLBTs with guard rings with minimum vertical emitter area of 36 (6×6) λ^2 ($\lambda = 0.8\mu m$). That means the Area-to-Periphery (A/P) ratio (Section 4.5.3) is 6. Array 2 contains nMOSFETs with gate area of 1680 (35×48) λ^2, which results in similar overall cell layout area as that of the CLBTs.

The arrays have their terminals connected to the pins of the chip independently and, thus, other arrays would not be affected when an array is under testing. There are transmission gate arrays on the boundaries of the test arrays as shown. The input signals such as gate, source, drain, emitter, base voltages, etc. of an array are applied to all inputs of the transmission gate of that array. There are shift registers running horizontally and vertically. The shifting bits are used to control the transmission gate array, through which the input voltage and current could pass to the DUTs. At any time, only one horizontal transmission gate and one vertical transmission gate would be enabled, so, only one DUT would be tested at any time with others being isolated.

5.3 Technology

The technology chosen for the fabrication was the AMI-ABN $1.5\mu m$ feature size process. This was an n-well CMOS process with 2 metal layers, 2 poly layers and an NPN option. The design rules followed were SCMOS rules with $\lambda = 0.8\mu m$. The chip designs were submitted to IC broker, MOSIS, two times for two batches of fabrication. In the second batch, the design of the CLBT array was modified (detailed in Section 5.4.2). The process parameters of the first and second batches are given in Appendix C and D respectively. In each batch, 5 Tiny-Chips with size of $2.2mm \times 2.2mm$ were fabricated. The substrate was started with P-Bulk/P-Epi type with a total of 14 mask levels. Lightly doped drains (LDD) was also included for improved reliability against hot carrier degradation [AMI]. As suggested by MOSIS, the minimum channel width should not be 3λ, as in other SCMOS rule sets, but rather 5λ. This design rule has been followed throughout the design [The]. This technology was chosen because of its availability and reasonable cost. MAGIC 6.0 was used to layout out all the circuits.

5.4 Design of Testing Arrays

5.4.1 nMOSFET Array

The testing structure of the nMOSFET array followed the same structure proposed by L. Portmann [PLK98]. Testing array design is a balance between pin consumption and accuracy. The structure shown in Figure 5.3 is a testing matrix of nMOSFETs. The drains of all the nMOSFETs are connected to a common drain terminal (*Drains*) of the matrix. The gates of the nMOSFETs of the same column are connected together to the output of the transmission gate of that column. Then all the inputs of the column transmission gates are connected together to the common gate input (*Gates*). $\overline{S_{GN}}$ and S_{GN} are the

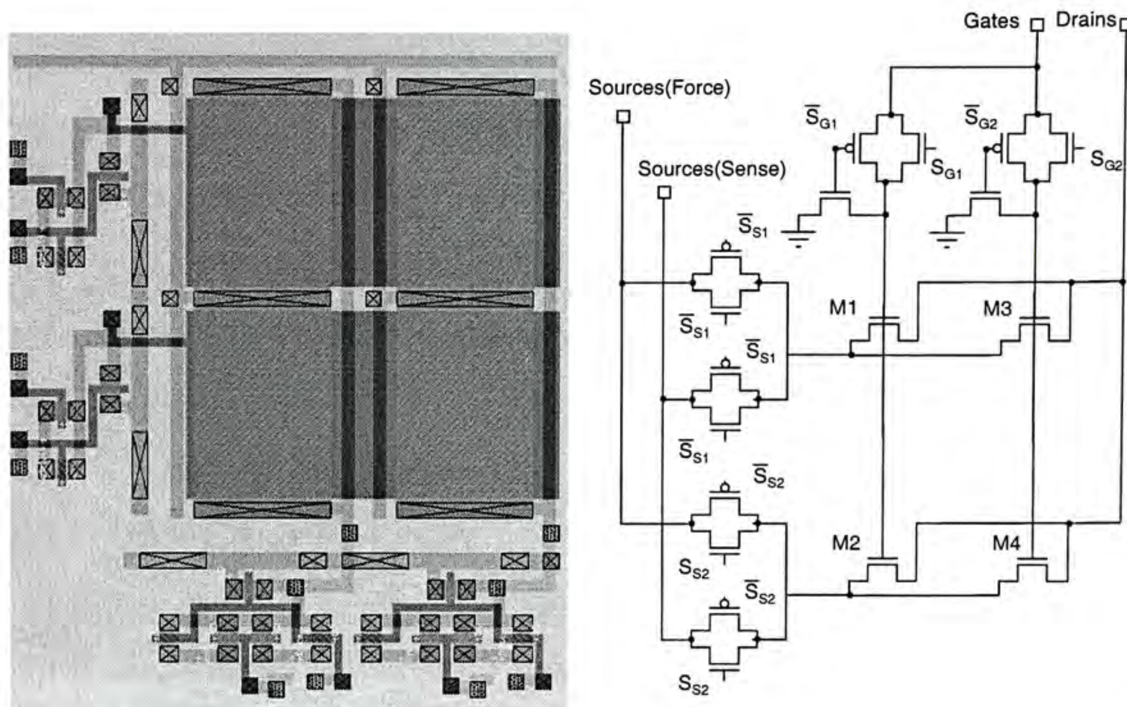

Figure 5.3: Simplified nMOSFET test structure layout with 4×4 DUTs (left) and nMOSFET test structure proposed by L. Portmann [PLK98].

outputs of the shift register controlling the transmission gate of column N. When S_{GN} is high, the corresponding transmission gate would be turned on and become low impedance. Then the input gate bias could be applied on all the gates of the nMOSFETs in that column. The gates of other columns would be pulled to ground, and thus, are cut off. Since there is essentially no current flowing through the transmission gate, the voltages at the input and output of the turned-on transmission gate would be the same. A similar selection scheme is used for the source terminals with S_{SN} and $\overline{S_{SN}}$ as the output of the shift registers. There is essentially no current flowing through the unselected rows because the transmission gates on the unselected row would be cut off. However, as there would be current flowing through the selected device as well as the corresponding row transmission gate, the potential at the source of the nMOSFETs would be different from the applied voltage due to a potential drop across the transmission gate. To address this problem, a 4-wire sense technique

was used. One pair of transmission gates are used to extract the transfer characteristics of the devices. The Force terminal ($Sources(Force)$) is connected to current or voltage sources and an ammeter for measuring the drain current (I_{DS}) and the Sense terminal ($Sources(Sense)$ is connected to a voltmeter for measuring the voltage applied on the source of the nMOSFETs. By using the above scheme, the transfer characteristics of individual nMOSFETs can be extracted.

5.4.2 *pnp* CLBT Array

Design 1

A similar design to the nMOSFET test array was also applied to the CLBT array as shown in Figure 5.4. As discussed in the previous section, cascode circuits were included in the test array. For simplicity, the substrate connections of the pMOSFETs are not shown. As the body of the pMOSFET is an n-well, it is connected as the base of the *pnp* CLBT. The substrates, i.e. the p-type epitaxial layer, of all the CLBTs were grounded.

The DUTs in the array are selected in the same way as the nMOSFET array with two main differences. First, unlike the gate terminal of MOSFET which essentially conducts no current, Force and Sense terminals ($Base\ Force$ and $Base\ Sense$) are required for the base input because the DUT would draw current when the transistor is selected and cause a potential drop across the transmission gate. Additional $Sense$ terminals are used for the measurement of the base voltage. The other difference is that, to unselect other transistors, the base voltage has to be set to Vdd instead of Gnd. During testing, all the drains are connected to ground. For unselected rows, the emitters would be connected to ground. Hence, all the devices on those rows would be in cut-off mode as the base voltage is in the range of ground to Vdd and both base-emitter and base-collector junctions are reverse biased. For unselected columns, all the

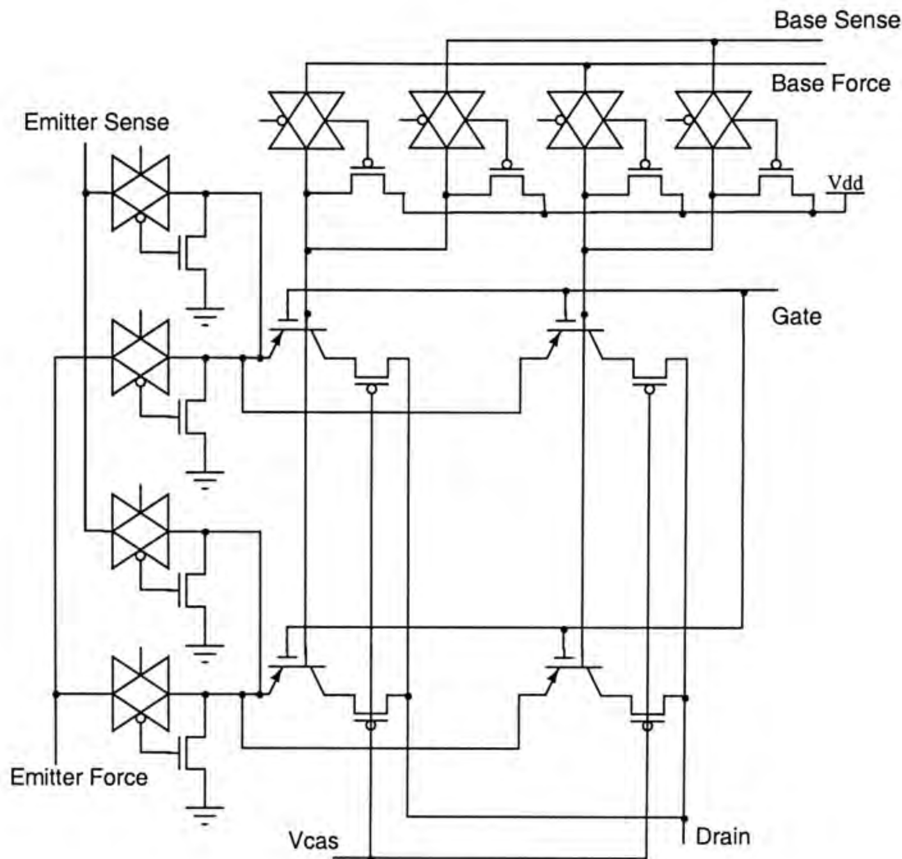

Figure 5.4: The original CLBT test array circuit with 4 × 4 DUTs.

base-collector and base-emitter junctions are reverse biased as the base voltage is at Vdd. Ideally, only the selected elements would contribute to the current flowing through the common drain.

Design 2

The matching properties of the CLBTs in the first batch test chips were found to be worse than those of the MOSFETs, which was opposite to expectation. It was suspected that it was due to the mismatch between the transmission gates. Theoretically, since the 4-wire sense measuring method was used, the base and emitter voltage could be adjusted while monitoring the voltage of the sensing terminals at the same time so that every CLBT could be applied with the same V_{BE} and V_{CE}. However, it was difficult to adjust the three ports at the same time during automatic parameter extraction. As a result, the collector and

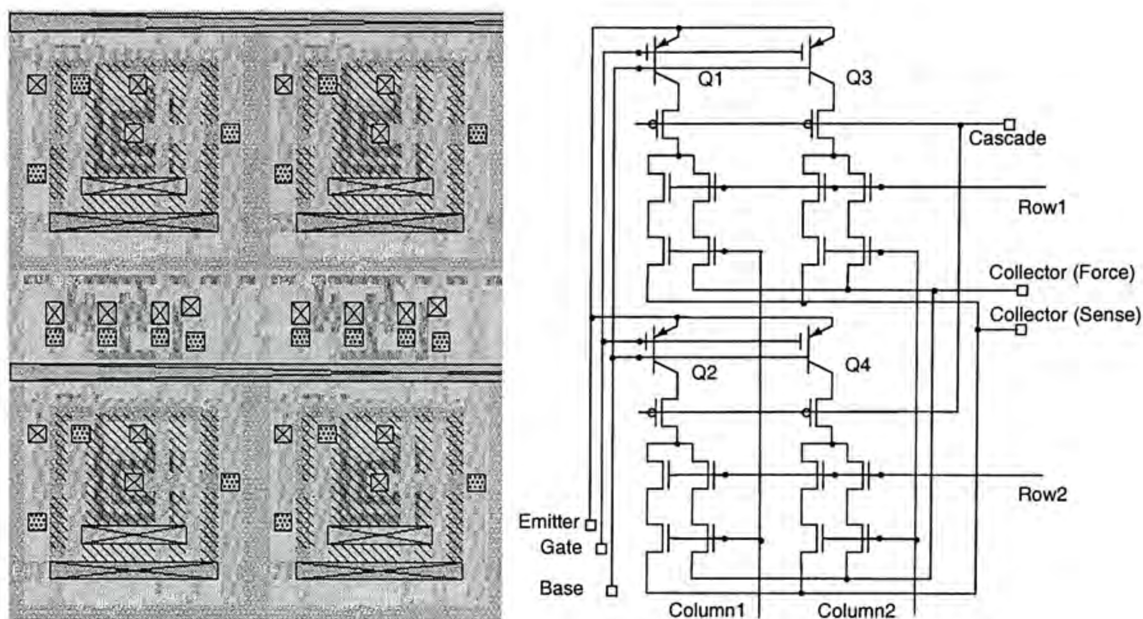

Figure 5.5: The modified CLBT test structure layout with 4 × 4 DUTs (left) and schematic diagram of the new test structure (right).

base inputs to the transmission gates were fixed to a certain voltage during testing and identical testing conditions for each CLBT could not be guaranteed. Moreover, this test structure could not be used for testing nano-order collector current levels because the sum of the leakage currents of the unselected devices could exceed $1nA$. As suggested by Dr. van Schaik [vS], the CLBT array was modified so that it is easier to achieve the desired conditions.

Figure 5.5 shows the modified testing structure. In the array, transmission gates to the base and the emitter were eliminated. During testing, the same base and emitter voltages are applied to all CLBTs. On the other hand, 2 transmission nMOSFETs were added in cascode with the drain of the cascode pMOSFET. The gates of the transmission gates are controlled by the output of a shift register. Obviously, a device will only contribute to the overall drain current when both the transmission gates are turned on. In this design, an nMOSFET transmission gate was used instead of the complementary transmission gate because we wanted to reduce the area occupied by the transmission

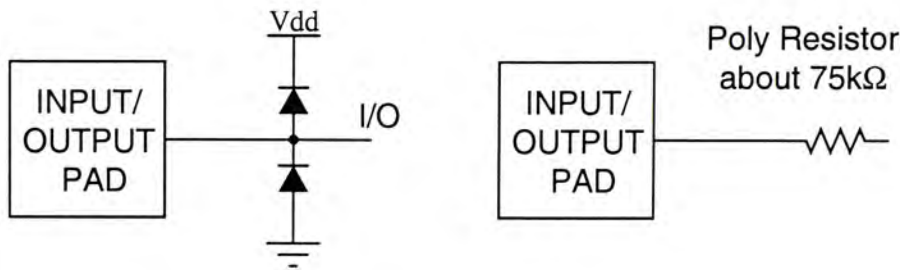

Figure 5.6: A typical analog I/O pad (left) and I/O pad for CLBT gate (right).

gate. Even so, due to the increased layout area, the number of DUT was reduced to 12 × 12 in this array. Again, a 4-wire sense measurement was used to eliminate the mismatch of the nMOSFET transmission gates.

5.5 Design of Input and Output Pads (I/O Pads)

The I/O pads used are typical analog I/O pads. In order to prevent electrostatic hazards, the input of each pad is clamped with 2 diodes to Vdd and Gnd. So the voltage would not excess the Vdd or Gnd more then the forward voltage of the diodes (typically $0.7V$)(Figure 5.6). However, for the gate voltage input of the CLBTs, as the gate voltage must be higher than the Vdd, it was not protected with a clamping diode. To protect it, a long polysilicon resistor was added in series to reduce the chance of being damaged by electrostatic discharge (ESD) (Figure 5.6).

5.6 Shift Register

To control the transmission gates, shift registers were used. The shift register is a critical part in the control circuit of the chip. A shift register proposed by C. Mead [Mea89] was selected as it was compact and had been used successfully in

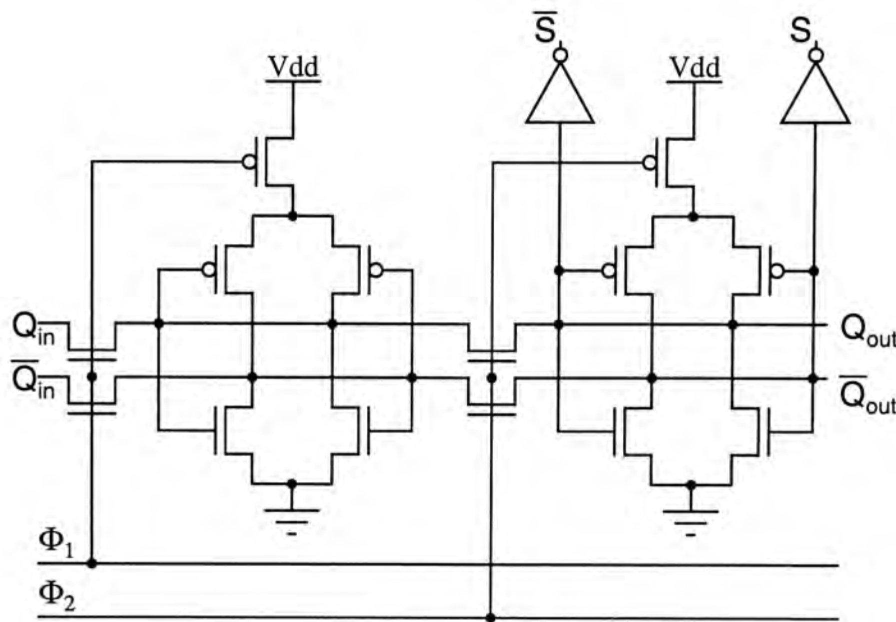

Figure 5.7: Schematic diagram of a shift register bit.

previous IC designs (Figure 5.7). Buffers (inverters) are added to the outputs of the shift register bits to drive a large capacitive load. The shift register bit has two stages and uses a two phase non-overlapping clock scheme, meaning that clock signals Φ_1 and Φ_2 would never be high at the same time. Each stage consists of a pair of cross-coupled inverters. It has two stable states as each inverter output feeds the input of the other. One is to store signal "1" on the top rail and a "0" on the bottom rail. The other is to store signal "0" on the top rail while "1" on the bottom rail. On the rising edge of Φ_2, the power to the second cross-coupled stage is cut off and the nMOSFET transmission gate is turned on, so data could be passed from the previous stage to the next stage. When Φ_2 falls, the power is restored and the input cut off, so the value is kept. Similar transfer occurs to the first stage during Φ_1.

5.7 Experimental Equipment

There were 5 main pieces of test equipment used for the automatic extraction of the device parameters:

Keithley 2400 SourceMeter^{TM} This is a source meter able to source voltage from $5\mu V$ to $210V$ and current from $50pA$ to $1.05A$ with reading back feature. The available current range is from $1\mu A$ to $1A$ with $5\frac{1}{2}$-digit resolution [Gro96]. The smallest range is $1\mu A$ with resolution of $50pA$ and the largest range is $1A$ with resolution of $50\mu A$. It has RS-232 Interface for communication with Personal Computers (PCs).

Keithley 6517A Electrometer This is an electrometer which can measure DC current in different ranges with $5\frac{1}{2}$-digit resolution [Gro96]. The smallest range is $20pA$ with resolution of $100aA$ and the largest is $20mA$ with resolution of $100nA$. It also has RS-232 Interface for communication with Personal Computers (PCs).

I^2C testing board This is a board developed by Dr. Philip Leong for testing analog VLSI chips. It was built with I^2C chips and has 16×8-bit analog outputs, 16×8-bit analog inputs and 16 digital I/O channels and could be interfaced with PCs through the parallel port. The resolution of the board is about $0.02V$ under $5V$ power supply. The digital ports were used for generating clock signals for the shift registers and the analog outputs were used for biasing the DUT.

GW GPC-1850 multi-source meter Another voltage source is required to provide $5V$ power supply for the operation of the I^2C board and the test chip. Another source, which can deliver higher voltage than the power supply is needed for biasing the gate (V_{gate}) for bipolar action. These were all provided by a GW CPC-1850 power supply.

PC and Software The PC was used for controlling the Keithley equipment through the serial ports and the I^2C board through the parallel port. Visual C^{++} was used as programming tool for automatic data extractions and MATLAB was used for data analysis and graph manipulations.

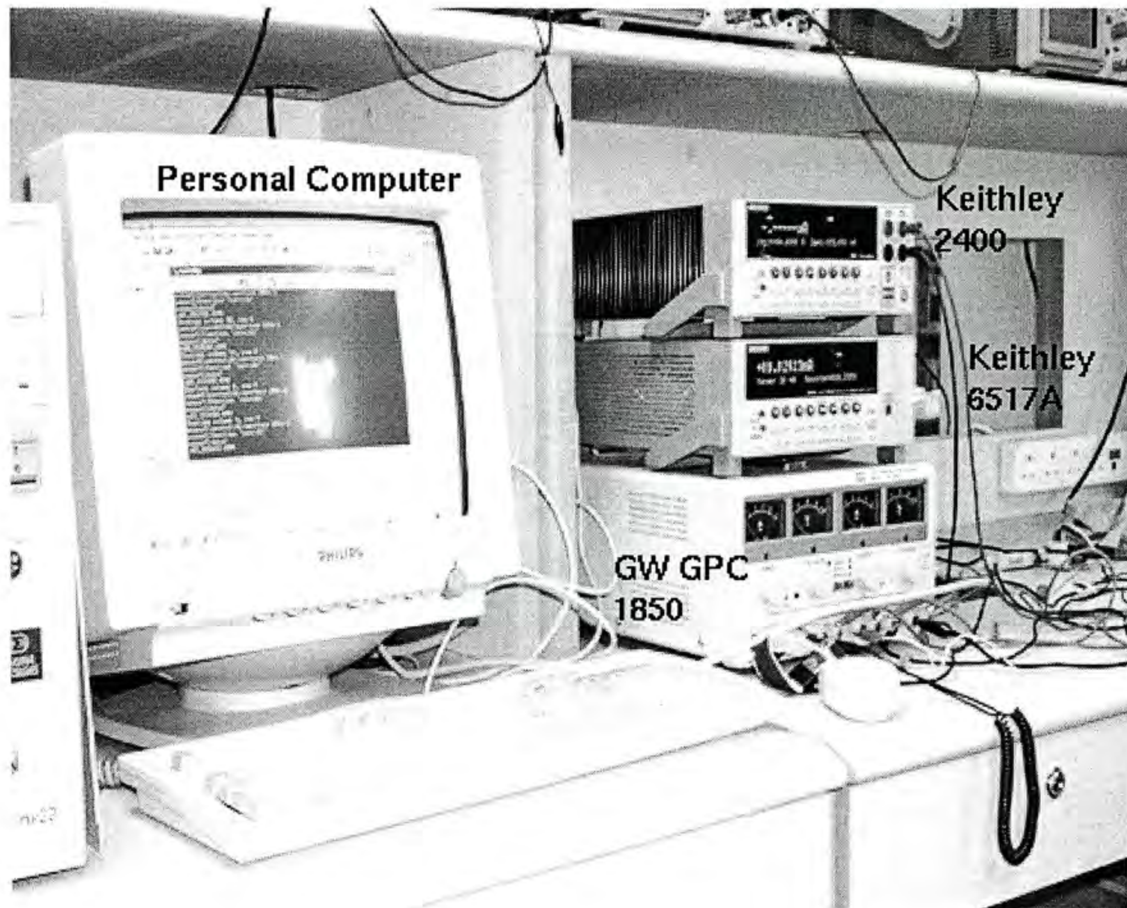

Figure 5.8: Photograph of the experimental setup.

5.8 Experimental Setup for Matching Properties Measurements

5.8.1 Setup for Measuring the Mismatches of the Devices

The setup for automatically extracting the current matching properties of the transistors are shown in Figure 5.9. The matching properties of the nMOSFETs and CLBTs operating as pMOSFETs with nominal drain currents of $1nA$, $10nA$, $100nA$, $1\mu A$, and $10\mu A$ were measured. For cascoded CLBTs, when the collector current is larger than $1\mu A$, the gain becomes too low. This also suggest that there is a strong debiasing effect in the sidewall

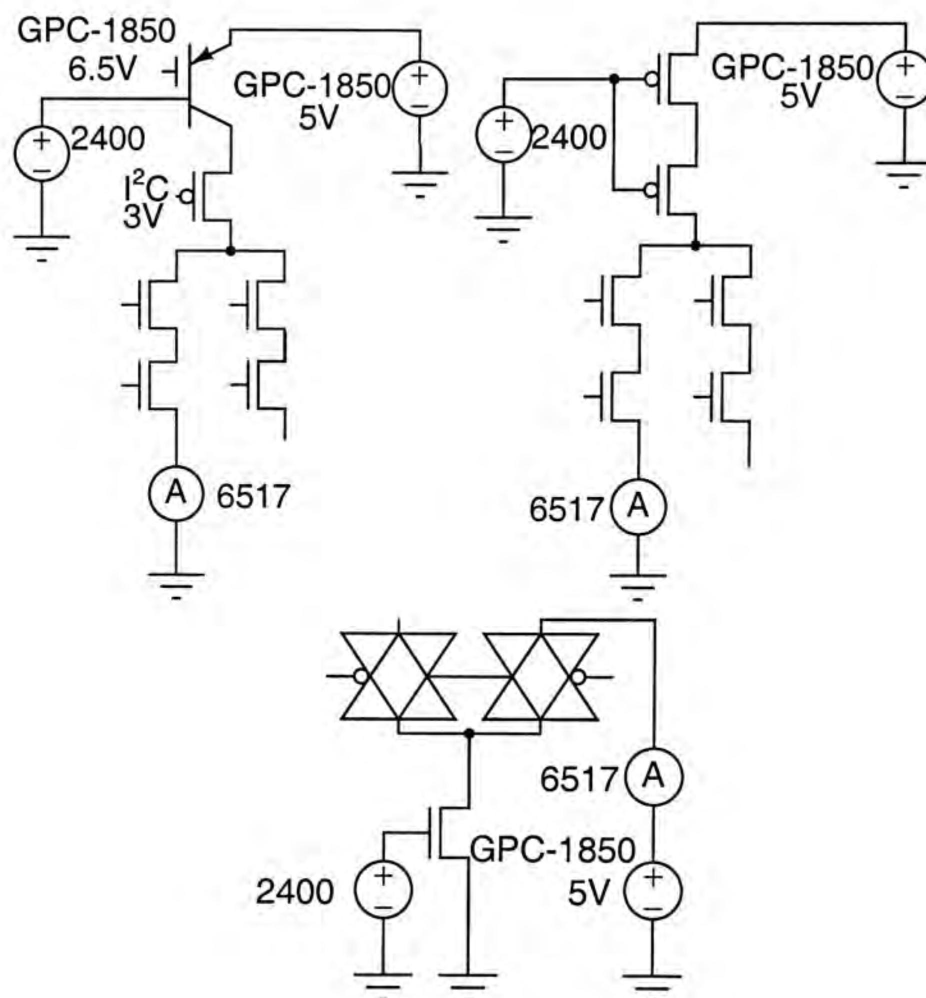

Figure 5.9: Setup for automatically extracting the matching properties of cascoded CLBTs (top left), CLBTs operating as *p*MOSFETs (top right) and *n*MOSFETs (bottom).

junction (Section 4.5.2). Such mode of operation is not favorable in most circuits. So the matching properties of the CLBT at current levels larger than $100nA$ were not tested.

All the devices were assumed to work with a $5V$ Vdd power system. The emitter, source and drain of the CLBTs, *p*MOSFETs and *n*MOSFETs, respectively, were connected to the $5V$ power supply. Since a Keithley 2400 can supply a very stable and accurate voltage source, it was used to bias the base and the gate of the CLBTs and MOSFETs respectively because the corresponding collector current and drain current varies exponentially with it. Table 5.1 shows the voltage required for biasing the transistors at the current

Current Level	$1nA$	$10nA$	$100nA$	$1\mu A$	$10\mu A$
CLBTs	$4.6V$	$4.53V$	4.4	NA	NA
NMOSs	$0.445V$	$0.538V$	$0.65V$	$0.866V$	$1.49V$
CLBTs as pMOSFETs	$4.347V$	$4.267V$	$4.18V$	$4.07V$	$3.81V$

Table 5.1: Voltages applied to the base and gate of CLBTs and MOSFETs for different current levels.

levels used for testing.

The Keithley 6517 was used to read the collector or drain currents. Additionally, several others points should be noted for the experiments and data:

- For the measurement of the nMOSFETs, the transistors were all in the saturation region. Moreover, for the given current levels, both by experiments and simulations, it was found that the voltage dropped across the bypassing transistors were less than $30mV$. Therefore, the mismatch between the bypassing transistors can be neglected. To simplify the data extraction setup with the available equipment, the $Sense$ terminals were not used during testing.

- For the measurement of the CLBTs, the cascode voltage V_{cas} was always biased to $3V$ which gave a reasonable operating range and Early voltage. All the CLBTs were measured in the linear region. Similar to the nMOSFETs, the $Sense$ terminals were not used.

- For the measurement of the pMOSFETs, the gates of the cascode pMOSFETs and the gates of the CLBTs were connected as the gates of the new pMOSFETs and the bases of the CLBTs were connected to Vdd. Similar to the nMOSFETs, the $Sense$ terminals were not used during testing.

5.8.2 Testing Procedures

As mentioned in Section 5.4.2, it was found that the original CLBT test arrays were not feasible for measuring the matching properties with the available equipment, therefore only the test chips containing the second design of CLBT arrays were tested for the matching properties (Appendix D). There are totally 5 chips fabricated in a lot. However, due to some unknown reasons (maybe due to oxide breakdown of the gate), one of them behaved abnormally (unreasonably low CLBT current level when compared with the other chips applied with the same voltages) and was not included in the testing. The four chips were labeled as $Chip1$, $Chip2$, $Chip3$ and $Chip4$. Firstly, the CLBTs were operated as pMOSFETs. The drain current of each pMOSFET in the arrays were recorded for later processing. In order to reduce the thermal effects, the lowest current level ($1nA$) was tested first by applying the corresponding voltage in Table 5.1. After the drain currents of all the devices in each of the four chips had been recorded, the next higher current level was then tested. The selection of the device for testing and setting of the current level were controlled by a PC which communicated with Keithley 2100 and also read data from Keithley 6517. Then the nMOSFET and the CLBT array were tested in a similar way.

5.8.3 Data Analysis

After all the data had been recorded, they were analyzed statistically and presented in the following sub-sections. Firstly, the mismatch of each devices in each chip were calculated by using Equations 3.6 to 3.8.

Then, the devices would be paired up as current mirrors and, by using Equations 3.1 to 3.3, the standard deviations of the mismatches of the mirrors were then found.

5.9 Matching Properties

5.9.1 Matching Properties of nMOSFETs

Figure 5.10 shows the drain currents of the nMOSFETs in the array of *chip*1 at $100nA$. The data was obtained by measuring the drain current in each DUT from column 1 to column 15 for each row, starting from row 1 to row 15. Column 15 and row 15 is nearest to the center of the chip. The top figure shows these data in one dimensional view. It is obvious that there is a pattern repeated every 15 samples. The current level generally decreases from column

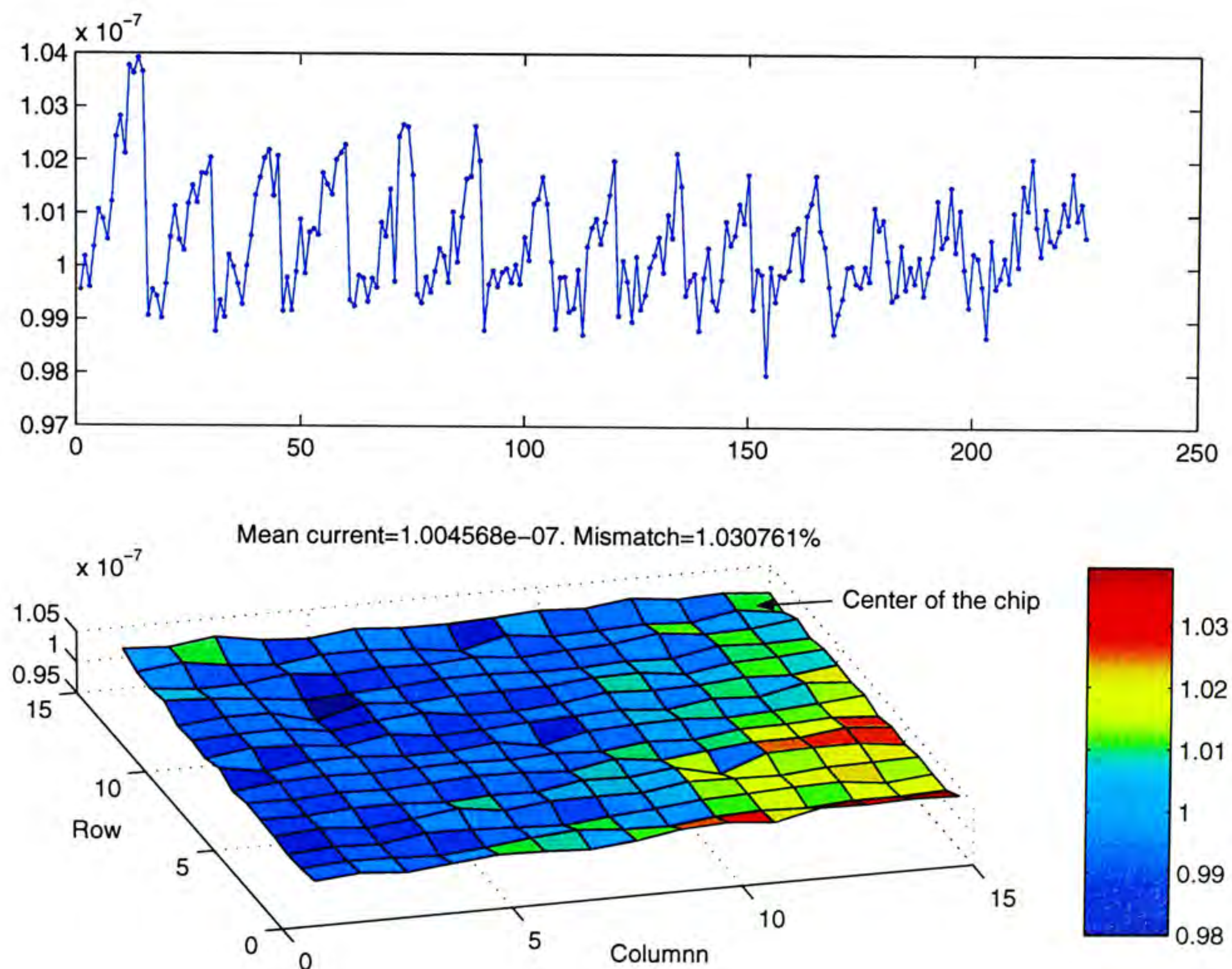

Figure 5.10: Matching properties of nMOSFET under $100nA$ current level in $Chip1$. The top figure shows the current values (in A) in one dimensional view and the bottom one shows the values in two dimensional view.

15 to column 1 and also from row 1 to row 15. This can be explained by oxide thickness and diffusion concentration gradients along the chip. This result is consistent with the notion that oxide variations are dominating factors for the mismatch of MOSFETs.

The mismatches of nMOSFETs at different current levels show similar properties. Table 5.2 and Figure 5.11 summarize mismatches calculated using Equations 3.6 to 3.8:

Current Level	$1nA$	$10nA$	$100nA$	$1\mu A$	$10\mu A$
chip1	2.71e+00	1.70e+00	1.03e+00	4.50e-01	1.76e-01
chip2	9.03e-01	8.74e-01	6.12e-01	3.01e-01	1.38e-01
chip3	9.34e-01	1.01e+00	6.18e-01	2.90e-01	1.34e-01
chip4	1.04e+00	1.09e+00	7.64e-01	3.85e-01	1.81e-01

Table 5.2: Average mismatch of nMOSFETs (%).

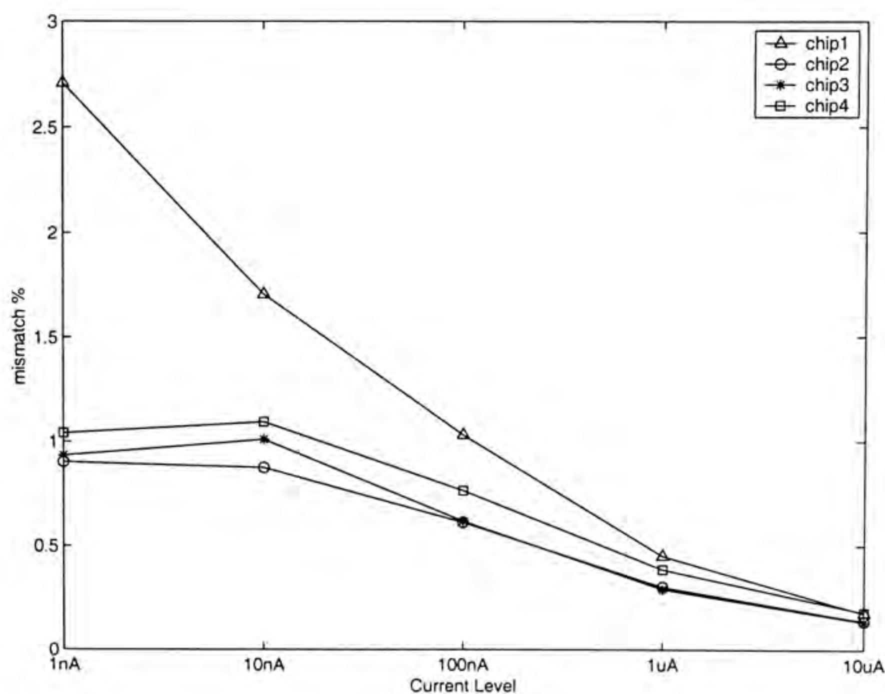

Figure 5.11: Mismatch of the nMOSFETs at different current levels.

5.9.2 Matching Properties of CLBTs

Figure 5.12 shows the measured currents of the CLBTs in the array of *chip*1 at the current level of $100nA$. Similar to nMOSFETs, the CLBTs were tested from column 1 to column 12 for each row, starting from row 1 to row 12. The top figure shows the measured currents in one dimensional view and the bottom one shows the data in a two dimensional array. Row 1 and column 12 is the transistor nearest to the center of the chip. From the graphs, it can be found that mismatch does not have a clear spatial tendency as for the nMOSFET case. This is because the mismatch is no longer dominated by the

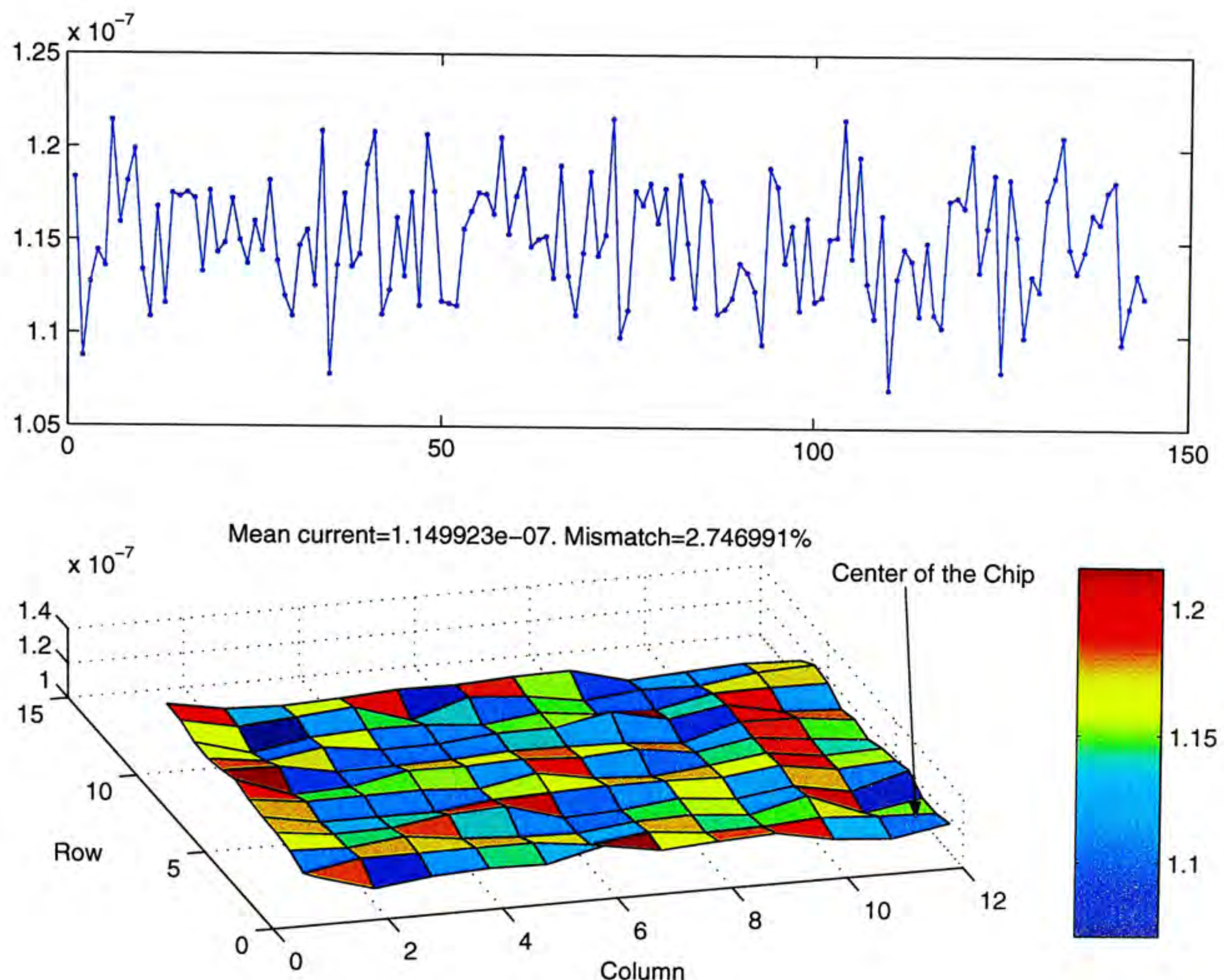

Figure 5.12: Matching properties of *pnp* CLBTs under $100nA$ current level in *Chip*1. The top figure shows the current values (in A) in one dimensional view and the bottom one shows the values in two dimensional view.

thickness of the oxide and other systematic mismatches.

Current Level	$1nA$	$10nA$	$100nA$
chip1	3.52e+00	3.12e+00	2.75e+00
chip2	4.19e+00	3.57e+00	3.08e+00
chip3	4.57e+00	3.28e+00	2.79e+00
chip4	3.61e+00	3.54e+00	3.04e+00

Table 5.3: Average mismatch of CLBTs (%).

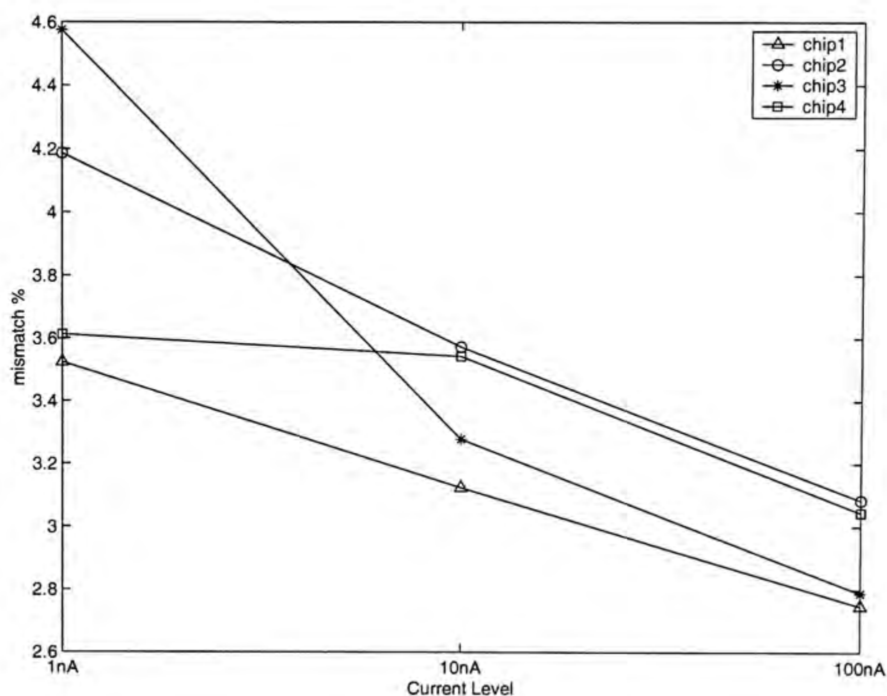

Figure 5.13: Mismatch of the CLBTs at different current levels.

5.9.3 Matching Properties of pMOSFETs

Figure 5.14 shows the distribution of the the drain currents of the pMOSFETs at the $100nA$ current level in the array of *chip*1. Since pMOSFETs are just CLBTs operating in MOSFET mode, they have the same locations as the CLBTs. Again, the data was obtained by sweeping from column 1 to 12 for each row, starting from row 1 to row 12. pMOSFET at column 12 and row 1 is nearest to the center of the chip.

Table 5.4 and Figure 5.15 show the mismatches of pMOSFET at different

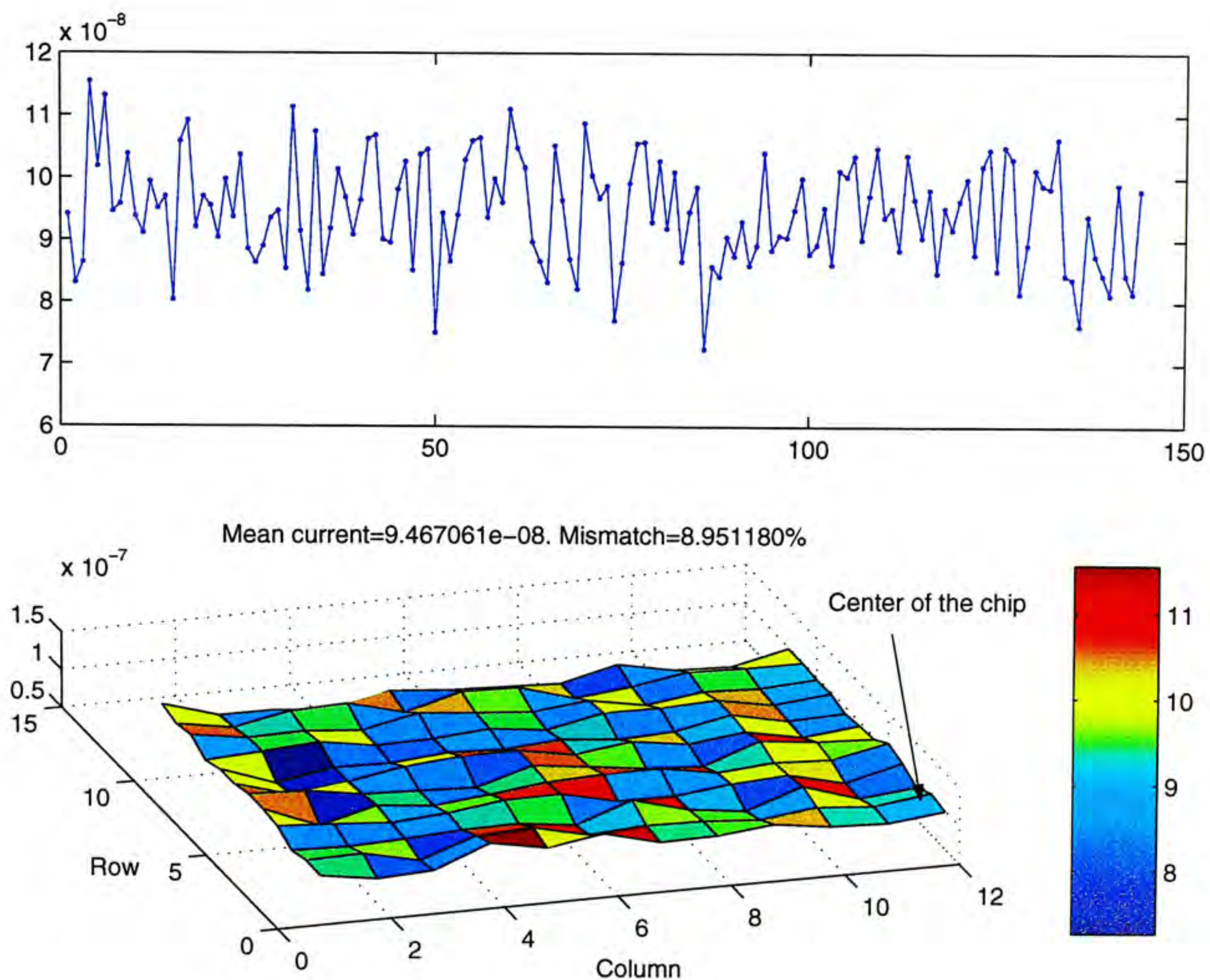

Figure 5.14: Matching properties of CLBTs operating as pMOSFETs under $100nA$ current level in $Chip1$. The top figure shows the current values (in A) in one dimensional view and the bottom one shows the values in two dimensional view.

Current Level	$1nA$	$10nA$	$100nA$	$1\mu A$	$10\mu A$
chip1	1.11e+01	1.06e+01	8.95e+00	5.01e+00	1.37e+00
chip2	1.09e+01	1.08e+01	9.02e+00	4.95e+00	1.35e+00
chip3	1.08e+01	1.01e+01	8.67e+00	4.64e+00	1.40e+00
chip4	1.18e+01	1.15e+01	9.30e+00	4.82e+00	1.34e+00

Table 5.4: Average mismatch of pMOSFET (%).

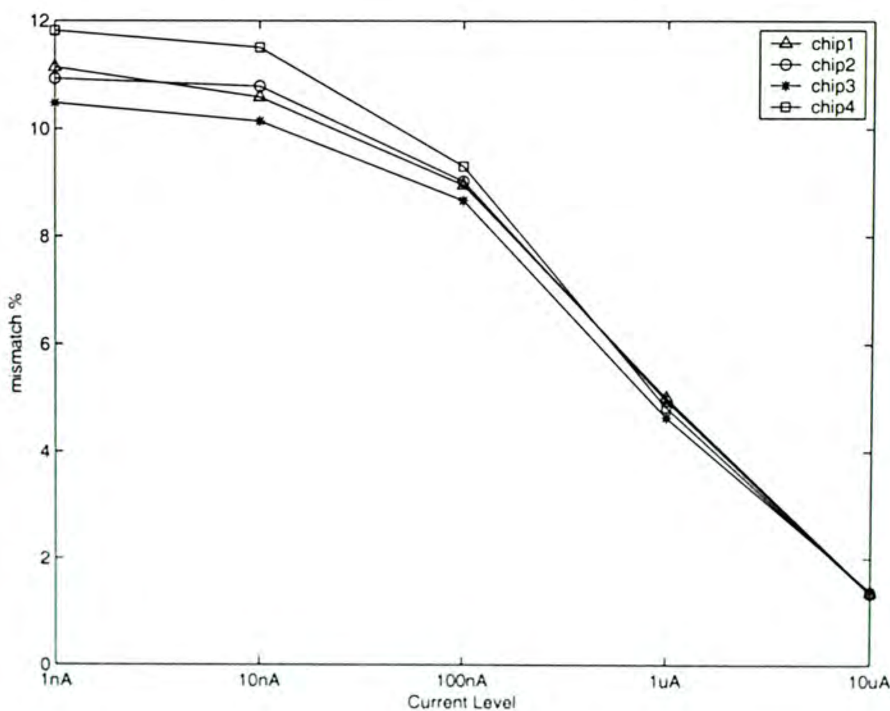

Figure 5.15: Mismatch of the pMOSFETs at different current levels.

current levels in all the chips.

The CLBTs operating as pMOSFETs have the worst matching properties. However, this is not a fair comparison because the layout gate area of the pMOSFETs is just $166\lambda^2$, which is much less than that of nMOSFETs ($1440\lambda^2$). For fair comparison, by applying the Law of Area, the mismatches of the pMOSFETs with gate area of $1440\lambda^2$ are estimated to be about:

$$\sigma(\delta_{I_{large}}) = \frac{\sigma(\delta_{I_{small}})}{\sqrt{Area\ Ratio}} = \frac{\sigma(\delta_{I_{small}})}{2.9453}$$

where $\sigma(\delta_{Ismall})$ and $\sigma(\delta_{Ilarge})$ are the mismatches of the pMOSFETs with gate area of $166\lambda^2$ and that with area of $1440\lambda^2$ respectively. The data in Table 5.4 was used for estimating the mismatch of pMOSFET with comparable layout area with CLBT and nMOSFET and are shown in Table 5.5 and Figure 5.16.

Current Level	$1nA$	$10nA$	$100nA$	$1\mu A$	$10\mu A$
chip1	3.78e+00	3.59e+00	3.04e+00	1.70e+00	4.64e-01
chip2	3.71e+00	3.66e+00	3.06e+00	1.68e+00	4.57e-01
chip3	3.56e+00	3.44e+00	2.94e+00	1.57e+00	4.75e-01
chip4	4.01e+00	3.91e+00	3.16e+00	1.64e+00	4.55e-01

Table 5.5: Mismatch of the scaled pMOSFET estimated using the Law of Area (%).

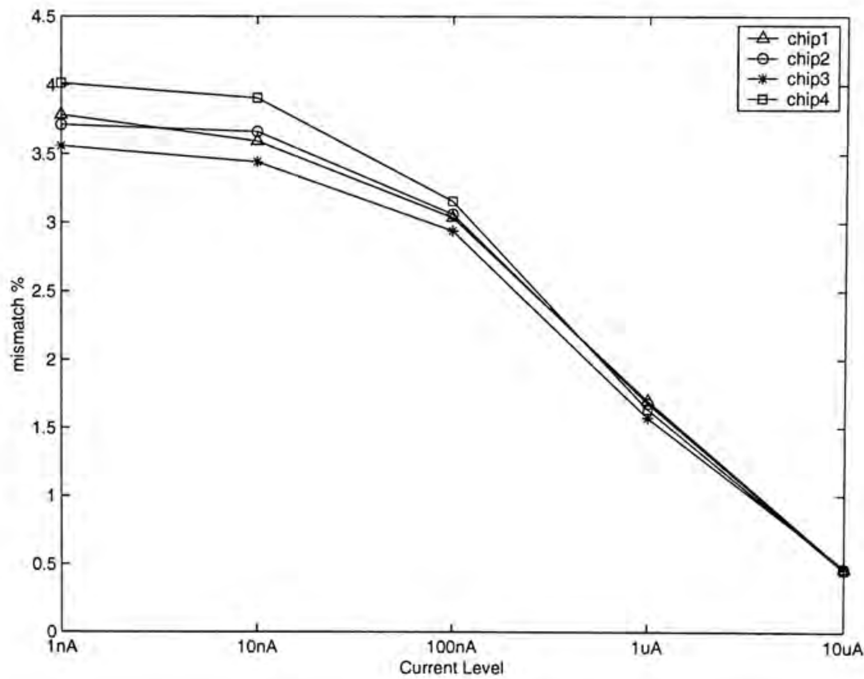

Figure 5.16: The estimated mismatch of the scaled pMOSFETs at different current levels.

5.9.4 Comments on the Matching Properties of CLBT, nMOSFET, and pMOSFET

The mismatch of the nMOSFETs is the smallest among the 3 types of devices. It is less than 0.2% at $10\mu A$ current level and levels off to about 1% in subthreshold. For the *pnp* CLBTs, their mismatch is about 3 to 4 times poorer than that of the nMOSFETs and is about 3% and 4% at $100nA$ and $1nA$ current levels respectively. The mismatch of *pnp* CLBTs operating as pMOSFETs is the worst and is about 1.4% at $10\mu A$ and 11% at $1nA$.

However, according to the Law of Area, the pMOSFETs would have the similar mismatch as the *pnp* CLBTs (both are about 4% at $1nA$ current level) if they were designed to have the similar layout area as the CLBTs. This also suggests that, in some circuits where cascoded circuits are not required for CLBTs and the CLBTs are grouped together so that they can share the guard rings, *pnp* CLBTs would be preferred to pMOSFETs because they will have the same matching properties while the area is greatly reduced (about $20-50\%$ reduction if cascode circuits were not included as shown in Table 4.1).

From Figure 5.11 and 5.16, the mismatches of both the nMOSFETs and pMOSFETs level off when the current levels are less than $10nA$. This is because they are operating in the subthreshold region, whereas for the CLBTs, the mismatch is still increasing at current levels $< 10nA$.

From the one dimensional views of the current distribution in the arrays, it is found that only the nMOSFETs show very explicit periodic trends. The reason is that the matching properties of the MOSFETs depend strongly on the oxide thickness and the doping concentration of the bodies. Therefore, nMOSFET array gives an explicit gradients of the current levels. For pMOSFETs, although their matching properties should also depend on the thickness of the oxide and body doping concentration, due to counter doping

and also the irregular shape of the gate, these two factors become less significant. It is probably that the mismatch is now dominated by other random factors such as the fixed oxide charges and surface state charges.

5.9.5 Mismatch in CLBT, nMOSFET, and pMOSFET Current Mirrors

The matching of the transistors is extremely important in current mirror or differential pairs, in which the matched ratio is specified and the matching between the two transistors within the pairs (local mismatch) is of major concern. The mismatches of the transistors calculated in the previous subsections reflect only the general mismatches of the transistors and the global mismatch is more important. In order to provide information about the matching properties of current mirrors implemented with the three types of transistors, the adjacent transistors were paired up as current mirrors and their mismatches were calculated using Equations 3.1 to 3.3. The equations are repeated here for convenience:

$$\delta = \frac{\frac{x_2}{x_1} - \frac{X_2}{X_1}}{\frac{X_2}{X_1}}$$

$$m_\delta = \frac{1}{N}\sum_{i=1}^{N}\delta_i$$

$$\sigma_\delta = \sqrt{\frac{1}{N-1}\sum_{i=1}^{N}(\delta_i - m_\delta)^2}$$

Since the transistors are identically designed, they are expected to have the same current, i.e. $\frac{X_2}{X_1} = 1$. The mismatches of all the transistor pairs were computed and shown in Table 5.6 and Figure 5.17. For nMOSFETs, there were $4 \times 7 \times 15 = 420$ pairs in total. For CLBTs and pMOSFETs, there were $4 \times 6 \times 12 = 288$ pairs.

The following observations can be made:

Current Level	$1nA$	$10nA$	$100nA$	$1\mu A$	$10\mu A$
nMOSFET	1.12e+00	1.08e+00	7.77e-01	3.70e-01	1.52e-01
CLBT	5.18e+00	4.84e+00	4.17e+00	NA	NA
CLBT as pMOSFET	1.49e+01	1.46e+01	1.20e+01	6.35e+00	1.70e+00
Scaled pMOSFET	5.07e+00	4.95e+00	4.07e+00	2.16e+00	5.76e-01

Table 5.6: The mismatches of the transistor pairs at different current levels (%).

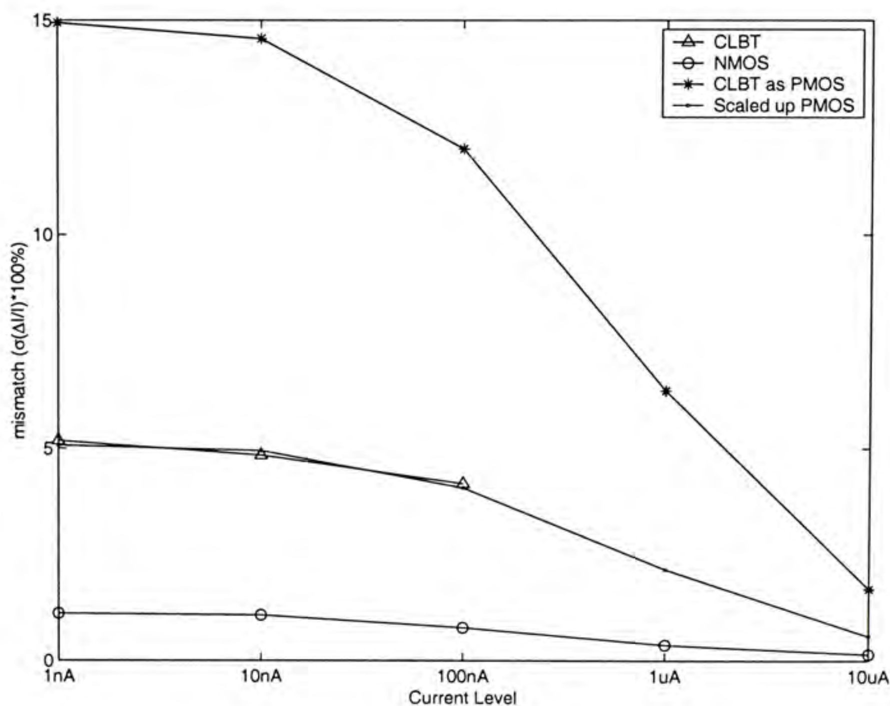

Figure 5.17: The mismatches of the transistor pairs at different current levels.

- nMOSFETs current pairs have the best matching properties. They are about 4 to 6 times better than the CLBTs.
- Although CLBTs current pairs show better matching properties than CLBTs operating as pMOSFETs (about 3 times), they should actually have similar mismatch if they were the same size.
- The mismatch of the MOSFETs levels off when they enter the subthreshold region, which agrees with the theory in Section 3.3.3.

5.10 Summary

In this chapter, the structure and layouts of the matching properties test chip were presented. The measurement procedures for the matching properties of CLBTs and MOSFETs were detailed and the measured matching properties of the devices were presented and analyzed. It was concluded that in the process used, the matching properties of the *n*MOSFETs were approximately 4 times better than that of the *pnp* CLBTs and that of the *p*MOSFETs were expected to be similar to that of the *pnp* CLBTs. Therefore, at least for this process, CLBTs might not be a good alternative to MOSFETs for critical matching circuits unless cascoded circuits were not used and guard rings were shared.

Chapter 6

Conclusion

This research was first motivated by the fact that there were several previous publications on the better matching properties of CMOS Compatible Lateral Bipolar Transistors (CLBTs) than the MOSFETs. Most of them did not perform the comparisons in a fair enough fashion and quantitative figures were not given. Moreover, due to the compatibility of CLBTs with the CMOS process, CLBTs provide an inexpensive alternative to the BiCMOS process under the trends of today's System-On-a-Chip (SOC) and mixed signal processing. Therefore, the matching properties of the CLBTs and MOSFETs were intended to be studied systematically and quantitatively, in the hope of providing useful data for circuit designers. In the literature, CLBTs have also been used for implementing critical circuits such as DACs, silicon cochlea, and bandgap voltage references. In this thesis, their applications were further investigated, especially the possibility of utilizing the gate terminal of the CLBTs.

Test chips containing arrays of *pnp* CLBTs and *n*MOSFETs were fabricated with AMI-ABN $1.5\mu m$ *n*-well process. The arrays were designed for a good balance between the number of devices, number of available pins and accuracy. The scheme is to use transmission gates and shift registers to select individual devices in the arrays. There are 225 *n*MOSFETs in the MOSFET array and 144 *pnp* CLBTs in the CLBT array, giving a total of 900 *n*MOSFETs and 576 *pnp* CLBTs in the 4 working test chips.

The drain and collector currents of the MOSFETs and CLBTs were measured respectively ranging from $10\mu A$ to $1nA$ for nMOSFETs and $100nA$ down to $1nA$ for *pnp* CLBTs. The mismatches of the current were then analyzed. The devices were also paired up as current pairs and their matching properties were calculated. It was found that the matching properties of the nMOSFET were in fact 3-4 times better than those of the *pnp* CLBTs. When the *pnp* CLBTs were operated as pMOSFETs and their mismatches were computed, it was found that the mismatch of the pMOSFETs was about 3 times poorer than that of the *pnp* CLBTs. By applying the Law of Area, mismatches of pMOSFETs with layout area similar to that of the *pnp* CLBTs were almost as good as those of the *pnp* CLBTs.

The mismatch results were consistent with those in the literature. However, previous studies compared CLBTs with larger overall layout area than the MOSFETs. This study shows that CLBTs may not be a good alternative to MOSFETs in some critical matching circuits, at least for the AMI-ABN $1.5\mu m$ process that was used.

Appendix A

Floating Gate Technology

In this Appendix, floating gate technology will be presented. The structure of floating gate MOSFETs and techniques for adjusting the floating charge, namely the electron tunnelling and hot electron injection, in standard CMOS technologies are presented. These would serve as the basis for the understanding to the FG-CLBTs and their applications to be presented in Appendix B.

A.1 Floating Gate

When the polysilicon gate of an ordinary MOSFET (poly 1) is completely surrounded by oxide (SiO_2) without any external connection, the gate is said to be floating and known as the floating gate (FG). The charge on the polysilicon will then suffer less than 0.1% loss in 10 years under room temperature [Car89, TB91]. FG is thus a good analog memory for circuits operating below 300K. Any device incorporated with floating gate is called the floating gate device.

If now another polysilicon layer (poly2) lays on top of the floating gate, the top polysilicon can still function as a gate to the MOSFET but the performance will be affected by the amount and type of charge stored in the floating gate. This is the floating gate transistors and the structure and symbols are shown in Figure A.1.

Floating gate transistors have been widely studied since the 1970s [FB71,

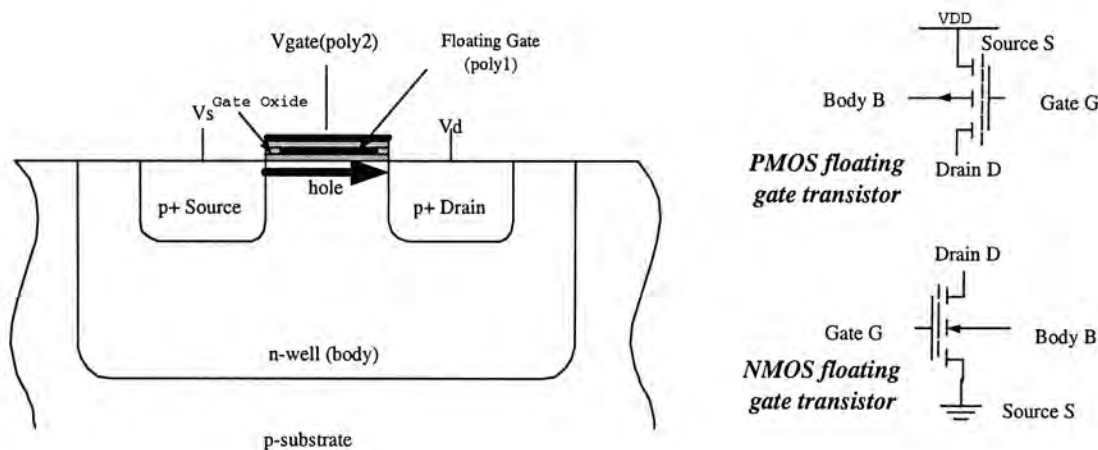

Figure A.1: Cross-sectional view of PMOS floating gate transistor (left) and the symbols of NMOS and PMOS floating gate transistors (right).

SS77b, SS77a, SK80, Gie80]. In digital circuits, they are used as non-volatile programmable devices such as Electrical Programmable Read Only Memories (EPROMs), Electrical Erasable Programmable Read Only Memories (EEPROMs) and flash memories [Vee98]. The floating gates can store charges for a long time to represent bit information of 1's or 0's. They are important in modern electronic equipment as they are non-volatile and electrically programmable.

Floating gate devices are also used in accurate analog computings and circuit trimming because the floating gate charge can be controlled almost as accurate as one electronic charge. Minch has used it for implementing translinear circuits [Min99]. Jin et. al. have used it for building non-volatile computation cell [JRL99]. Other applications include single-transistor silicon synapses [DHMM96] and D/A converters [WKR99].

A.2 Tunnelling

Although silicon oxide is an excellent insulator, significant numbers of electrons can still leave the floating gate if the oxide is thin enough. According to

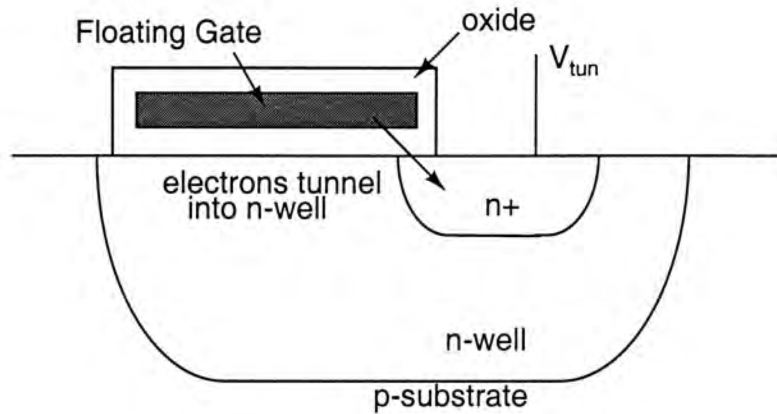

Figure A.2: Cross-sectional view showing how an n-well is used to remove electron from floating gate through tunnelling.

quantum theory, the electron is actually a span of wave-function in space. When an electron encounters an energy barrier which is larger than its total energy, there is still a finite probability for the electron to cross the barrier and the probability is inversely exponentially proportional to the thickness of the barrier [Kas00]. This is know as tunnelling. Standard CMOS process usually has the gate oxide above $30nm$, which is too thick for observable tunnelling. However, when the electric field across the oxide is high enough, it will reduce the effective energy barrier width and, thus, increase the probability of the electron to penetrate the insulator. This process is called field emission (or Fowler-Nordheim Tunneling [LS69]). For a SiO_2 barrier with barrier height Φ under an external electric field of E, the current density of the tunnelling current can be represented as:

$$J = \frac{q^3 E^2}{8\pi h \Phi} \exp \frac{-4(2m)^{\frac{1}{2}} \Phi^{\frac{3}{2}}}{3\hbar q E} \tag{A.1}$$

where, $\hbar = h/2\pi$ with h being the Planck's constant, q is the electronic charge, and m is the free-electron mass.

According to the tunnelling equation, to achieve a reasonable tunnelling current, the applied electric field must be high enough. This casts another problem, that to achieve high enough field, the gate oxide may have to be

biased near its breakdown voltage ($\approx 760mV/nm$ [Cha]). Fortunately, oxide breakdown can be avoided with special layout. Figure A.2 shows the structure of the tunnelling well that can be used in an n-well process, in which the edge of the polysilicon lays directly above the n-well. Due to the irregularity of the boundaries of the oxide grown at the edges of the polysilicon, the electric field will be enhanced and highly concentrated there [TB91, Car89]. Therefore, tunnelling electric field can be achieved with lower voltage, and oxide breakdown can be avoided. Such method has been successfully used in $2\mu m$ processes [TB91, Car89, HMD99].

To achieve tunnelling in an n-well CMOS process, one could just simply apply high voltage to an n-well. This method can then be used to remove electrons from the floating gate and thus reduce the potential of the floating gate.

A.3 Hot Electron Effect

When a pMOSFET is biased with high source to drain voltage, the energetic channel carriers, holes, will cause impact ionization when colliding with the lattice and electrons will be created at the drain edge of the drain-to-channel depletion region due to the high electric field there [HMD99]. The electrons will then travel back to the channel, gaining more energy. Some electrons will become energetic enough to overcome the silicon barrier and enter the gate. This phenomenon is known as the hot electron effect (Figure A.3). The injection current is exponentially proportional to the injection voltage, V_{inj}. It can be used to increase the number of electrons, i.e. decrease the potential, in a floating gate.

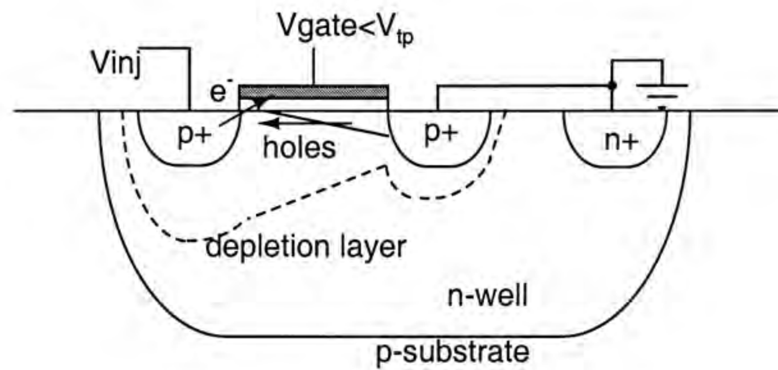

Figure A.3: Cross-sectional view showing how hot electron injection is achieved in a *p*MOSFET.

A.4 Summary

This Appendix introduced the basic theories of standard CMOS floating gate technologies. Electron tunnelling and hot electron injection were presented to be effective techniques for adjusting the number of electrons in the floating gate fabricated with standard $2\mu m$ CMOS processes.

Appendix B

A Trimmable Transconductance Amplifier

B.1 Introduction

Operational Transconductance Amplifiers (OTAs) incorporating CLBTs as input pairs exhibit lower noise than those incorporating MOSFETs [Vit83]. In this Appendix, an OTA incorporating with *pnp* CLBTs as input pair will be presented. It shows the possibility of trimming the OTA by using the residual gate effect of the CLBTs. A floating gate CLBT (FG-CLBT) was also designed and incorporated in an OTA. The floating gate is used to stored the charges required to trim the OTA. The experimental results are presented.

B.2 Trimmable Transconductance Amplifier using Floating Gate Compatible Lateral Bipolar Transistors (FG-CLBTs)

Due to the residual gate effect of the CLBTs (detailed in Section 4.4), the collector current is dependent on the gate voltage. This can be used to trim the offset of a differential amplifier if floating gate CLBTs (FG-CLBTs) are

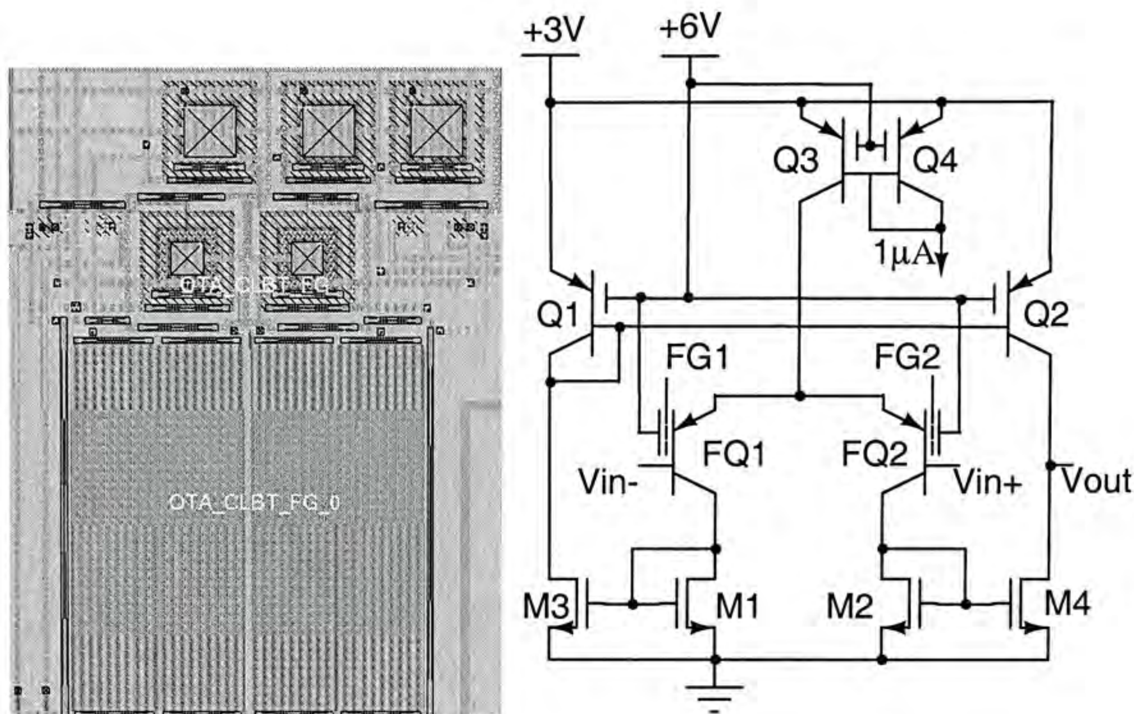

Figure B.1: Layout of FGOTA (left, current source $Q4$ not shown) and its schematic diagram (right).

used as the differential input pairs.

A 2-stage Operational Transconductance Amplifier (OTA) containing a differential input stage with FG-CLBTs as input pair was designed and fabricated. Figure B.1 shows the layout and schematic diagram of the Floating-Gate OTA (FGOTA) and Figure B.2 shows its photomicrograph. The design is modified from Vittoz' design in [Vit83]. In Vittoz' design, all the bipolar transistors are normal *npn* CLBTs. In our design, we used only normal *pnp* CLBTs for $Q1$, $Q2$, $Q3$, and $Q4$ while *pnp* FG-CLBTs were used as the differential inputs, $FQ1$ and $FG2$. The FGOTA was simulated in PSPICE with all the CLBTs replaced by vertical *pnp* bipolar transistors with $3V$ power supply and $1\mu A$ current source. The gain β and Early voltage V_A of the bipolar transistors were set to be 100 and $10V$ respectively, which are the typical values of CLBTs under such collector current level (Chapter 4). The resulted DC gain is about $51.6dB$ with bandwidth $\approx 1000Hz$ which shows the similar performance

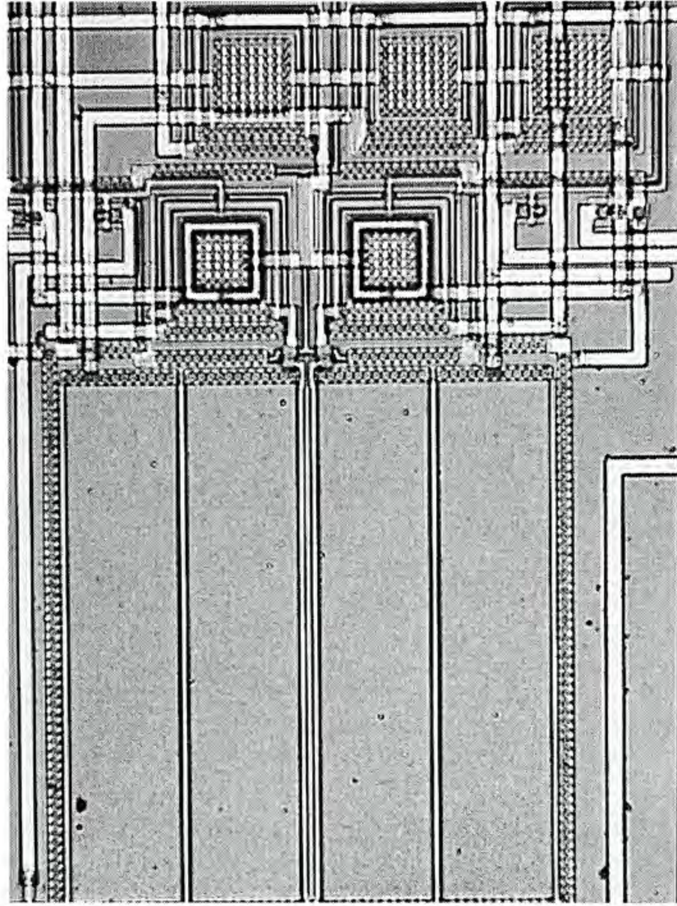

Figure B.2: Photomicrograph of the FGOTA

as that one reported by Vittoz.

Another OTA with exactly the same design as the FGOTA except $FQ1$ and $FQ2$ are replaced by normal *pnp* CLBTs was also fabricated. They are used to verify the results of the FGOTAs.

B.2.1 Residual Gate Effect and Collector Current Modulation

As mentioned in Section 4.4, there are residual gate effects in *npn* CLBTs. The same thing is also true for *pnp* CLBTs. When the Gate-Source voltage V_{GS} of a *pnp* CLBT is sufficiently high ($> 1.2V$[Vit83, Arr89], Section 4.9.2), the collector current becomes independent of V_{GS} and the transistor is in pure bipolar mode. CLBTs are used as pure bipolar devices in most of the literature

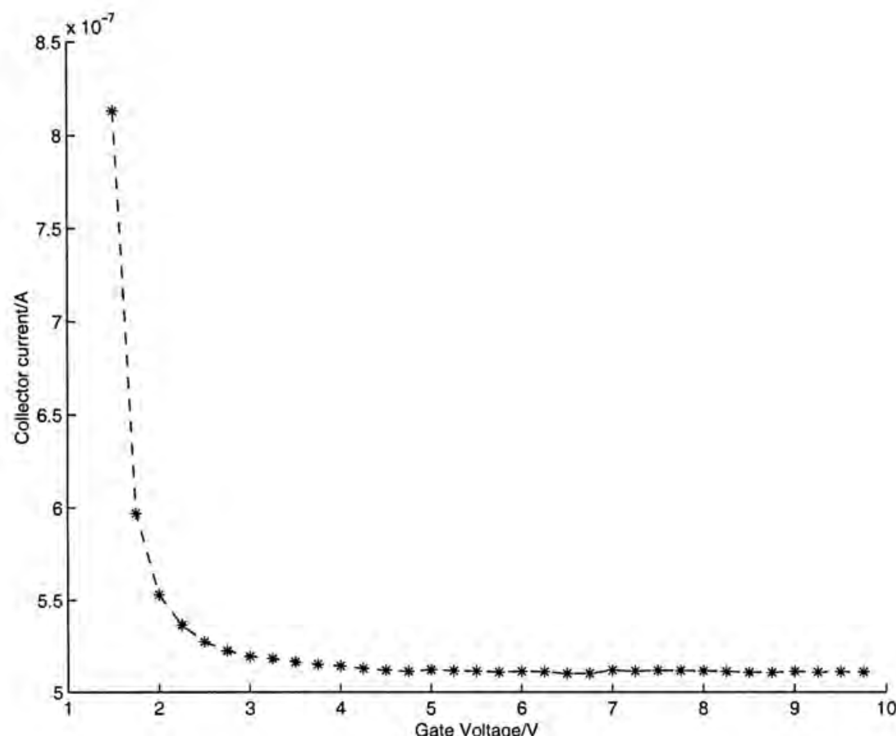

Figure B.3: Residual gate effects of a *pnp* CLBT.

by fixing the gate terminal at a suitable voltage [Vit83, RHL97]. However, it should be recognized that, from strong inversion ($V_{GS} < V_{TP}$), to weak inversion ($0V > V_{GS} \geq V_{TP}$), and then to pure bipolar mode ($V_{GS} \gg V_{TP}$), there exist continuities. By lowering V_{GS}, one can modulate the collector current by operating the transistor in the region between deep bipolar mode and weak inversion, which is the residual gate effect. The lateral collector current (I_C) will increase as the gate voltage decreases because the hole concentration near the Si/SiO_2 interface will increase.

The dependence of collector current on V_{GS} is process dependent. The residual gate effect of a single cascoded *pnp* CLBT with vertical emitter area of $6 \times 6\lambda^2$ has been measured under an environment that emulates the CLBT in the OTA (Appendix C). The emitter, base, and V_{cas} were biased at $2V$, $1.5V$, and $0V$ (all obtained by simulation), respectively. The emitter voltage was then adjusted such that the drain current was about $0.5\mu A$ with gate voltage V_G at $6V$. Then V_G was swept from $10V$ to $1V$ and the drain currents

were recorded. Figure B.3 shows the relation between the drain current and V_G. It is found that the residual gate effect results in about 10% drain current variation for $8V$ of V_{GS} variation at a $0.5\mu A$ current level in our process. Larger modulation can then be achieved by biasing the transistor in the weak inversion mode, which gives a hybrid of a weak inversion MOSFET and a BJT.

From Figure B.3, there should be enough current modulation for most applications if the transistors is biased in the weak inversion region ($V_G > 1.5V$). However, when I_C is limited by a current source (which is not the case in our emulation testing), such as in a differential pair, the modulation of collector current in weak inversion region will be much smaller than that shown in Figure B.3. It becomes necessary to operate the CLBT in moderate inversion or even strong inversion regions in order to sufficiently modulate I_C. The CLBT can then be qualitatively regarded as a BJT and a MOSFET in parallel. Due to the weaker current driving power of MOSFET than that of BJT, with PSPICE simulation, it was found that the MOSFET must be biased in strong inversion region in order to have $10\% - 20\%$ current modulation. Such current modulation can be used for compensating mismatches between CLBTs and has been demonstrated by trimming BiCMOS preamplifier offset by biasing the gate voltage of the input pair CLBTs at different voltages [Arr89]. The offset V_{os} of a CLBT differential pair with load resistance R can be represented as [Arr89]

$$V_{os} = U_T \log (1 - \epsilon_B)(1 - \epsilon_R)\frac{f_{G+}}{f_{G-}} \tag{B.1}$$

where U_T is the thermal voltage, ϵ_B, ϵ_R are the CLBT and loading resistance mismatches respectively, and f_{G+}, f_{G-} are the floating gate functions of the input pair.

Although the surface current will increase after modulation, $10\% - 20\%$ I_C changes usually will be enough for trimming an amplifier. Amplifiers that use CLBTs after trimming are still expected to have lower noise than MOSFET

ones.

B.2.2 Floating Gate CLBTs

To obviate the need of voltage multiplication [Arr89] and to obtain an accurate and non-volatile gate voltage [SG88, Car89, TB91], a floating gate can be used as the gate terminal of a CLBT. In this process, the AMI-ABN 1.5μm double-polysilicon n-well process, poly1 is used as the floating gate (FG) and poly2 is used as the control gate (CG) of the CLBT ($FQ1$ and $FQ2$ in Figure B.1). The layout of FG-CLBT is shown in Figure B.4. Since poly1 is completely surrounded by SiO_2, the charge inside will suffer less than 0.1% loss in 10 years under room temperature [Car89, TB91]. FG is thus a good analog memory for circuits operating below 300K. The structure of a FG-CLBT is the same as that of an ordinary CLBT besides that a floating gate (detailed in Appendix A) is added. The figure also shows the n-well used for electron tun-

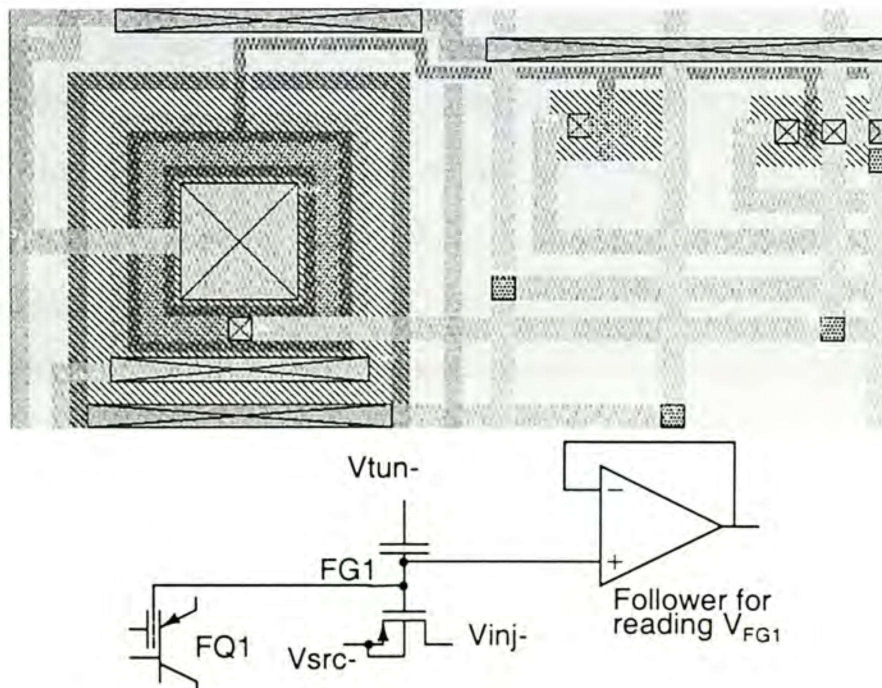

Figure B.4: Layout of FG-CLBT (top left), the tunnelling n-well (top middle), and injection pMOSFET (right top) and the schematic diagram (bottom).

nelling and pMOSFET used for hot electron injection. Since the floating gate of the FG-CLBT is connected to the gate above the n-well and the pMOSFET, the amount of charges in floating gate can be controlled through tunnelling and hot electron injection.

As the floating gate must be isolated to prevent the leakage of charge, the floating gate is connected to a follower, whose output is connected to an output pin. The potential of the floating gate will be modified by injection or tunnelling to trim the OTA so that the offset voltage is virtually zero. The potential of the floating gate can be read through the output of the follower.

B.2.3 Electron Tunnelling

The tunnelling structure is formed by laying the floating gate polysilicon over an n-well. A capacitor is formed with the gate oxide acting as an energy barrier preventing the electrons leaving the FG (Figure B.4). However, there is a finite probability for an electron to pass through a thin energy barrier even though the total energy of the electron is less than that of the barrier, which is known as tunnelling (Section A.2). According to Equation A.1, the tunnelling probability depends heavily on the oxide thickness t_{ox}, temperature T, and the voltage across the oxide $V_{tun} - V_{fg}$, where V_{tun} and V_{fg} are the tunnelling voltage applied to the n-well and FG voltage respectively when the following equation is substituted into Equation A.1:

$$E = \frac{V_{tun} - V_{fg}}{t_{ox}} \tag{B.2}$$

where E is the electric field strength across the oxide. Therefore, the tunnelling current I_{tun} at constant temperature can be represented as [HMD99]:

$$I_{tun} \propto exp(-\frac{t_{ox}}{V_{tun} - V_{fg}}) \tag{B.3}$$

By applying a high enough voltage to the well, the electrons confined in the floating gate can tunnel through the gate oxide into the n-well and, V_{fg} will

increase. Since the edges of the polysilicon are located at the middle of the n-well, the electric field is concentrated there and the tunnelling voltage required is then reduced [Car89]. For the $31.6nm$ thick gate oxide in our process, to have a reasonable rate of tunnelling ($3mV/s$), $V_{tun} - V_{fg}$ has to be at about $23V$. This is below the breakdown voltage of the oxide which is about $760mV/nm \times 31.6nm = 24V$.

B.2.4 Hot Electron Injection

To reduce V_{fg}, a minimum size pMOSFET with the source and body connected together and a FG as the gate terminal is used for hot-electron injection as shown in Figure B.4 (detailed in Section A.3). The source voltage (V_{src}) has to be raised above V_{fg}, or alternatively, V_{fg} can be pulled to be lower than V_{src} by reducing the CG voltage, so that the transistor can conduct current. When the channel-drain voltage V_{cd} is high enough (achieved by lowering the injection voltage V_{inj}), holes entering the drain-to-channel depletion region will cause impact ionization generating electron-hole pairs under the high electric field [HMD99]. Some electrons will become energetic (hot) enough to inject into the FG and reduce V_{fg}. It was found that $V_{inj} < -6.5V$ will give significant injection.

B.2.5 Experimental Results of the OTA

The OTA without FG-CLBTs was tested first. In this circuit, the gates of the CLBT were connected to pads which were controlled by an external voltage source. The gates of the CLBTs were biased at $6V$ and the Vdd and I_{src} were set to $3V$ and $1\mu A$ respectively. First, the offset of the OTA was measured to be about $5.79mV$ when $V_{G+} = V_{G-} = 6V$, where V_{G+} and V_{G-} are the gate voltages of the positive and negative differential inputs. The V_{G+} was then lowered to $1.728V$ at which the offset was found to be less than $20\mu V$. The

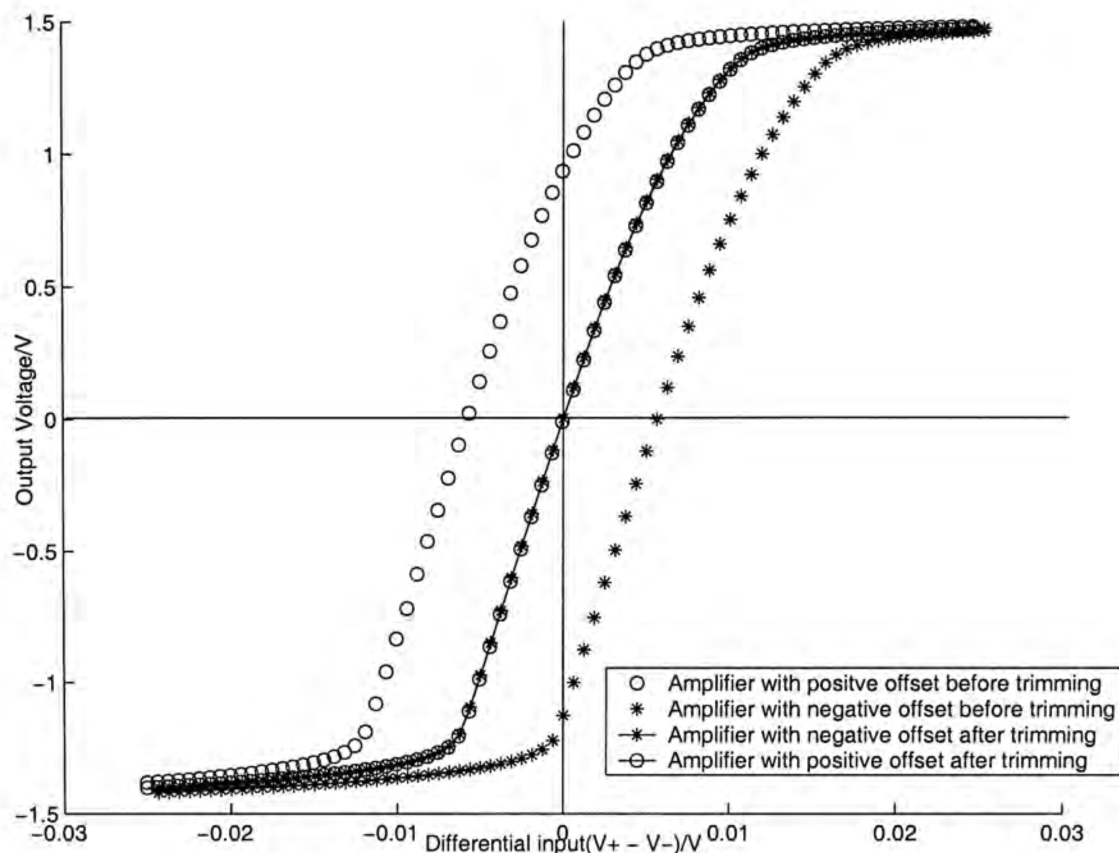

Figure B.5: VTCs of trimmed and untrimmed OTA (all the measurements were taking $1.5V$ as reference).

Voltage Transfer Characteristic (VTC) is plotted in Figure B.5. Although the transfer curves of the OTA are not symmetric, which might be due to the high common mode influence, it was found that the transfer characteristic was not changed after trimming. Since the fabricated OTAs all had an initial positive offset, in order to confirm the possibility of trimming negative offsets using residual gate effect, $11.5mV$ was applied to the negative input to emulate an operational amplifier with negative offset of about $-5.6mV$. Then the V_{G+} was connected back to $6V$ but with V_{FG-} decreased to $1.746V$ and it was found that it gave the similar result as the positive offset case. All the data are shown in Figure B.5.

B.2.6 Experimental Results of the FGOTA

Due to capacitive coupling effects, the CGs of $FQ1$ and $FQ2$ in Figure B.1 must be tied to a fixed voltage so that the floating gate voltages (V_{FG1}, V_{FG2}) can be kept constant. Initially, V_{FG1} and V_{FG2} were found to be greater than $3V$ with CGs tied to ground. The CGs were then connected together with the gates of $Q1$ to $Q4$ at $6V$, under which all the CLBTs and FG-CLBTs were sure to be in deep bipolar mode. The offset was measured to be $5.67mV$. Hot-electron injection was used to bring down V_{FG2} until the offset became negative. This is equivalent to increasing the current in the positive input side, or adding a negative voltage source in series with V_{in+}. Tunneling was then used to trim the offset by bringing up V_{FG2} again. By monitoring V_{FG2} and V_{out}, V_{tun+} was set such that $V_{tun+} - V_{FG2} \approx 23V$ for coarse trimming and $22V$ for fine trimming when V_{out} became near to AC ground. Due to oxide

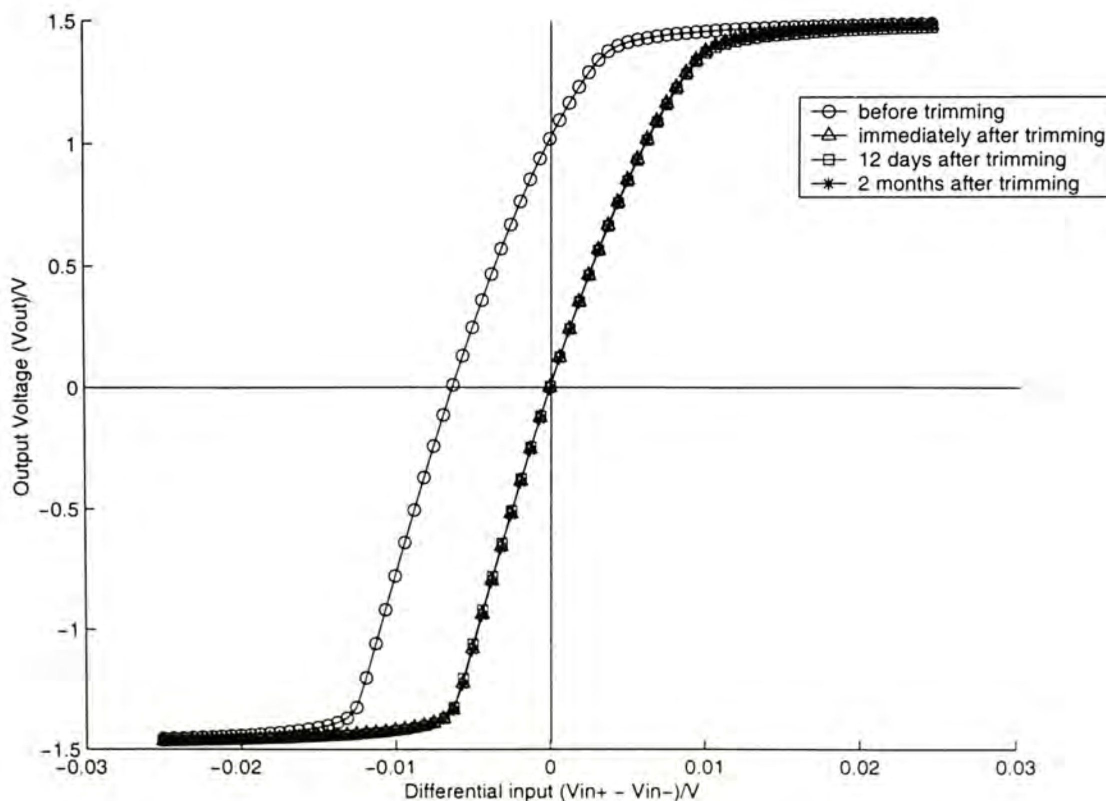

Figure B.6: VTCs of trimmed and untrimmed FGOTA (all the measurements were taking $1.5V$ as reference).

relaxation [SG88, Car89] and the small coupling effect between the FG and the tunneling n-well, the offset has to be over-trimmed so that it will give minimum offset under normal operations. The VTCs of the amplifier before and after trimming are shown in Figure B.6. Again, although their VTCs are not symmetric, the VTC is unchanged after trimming. The trimmed offset was less than $10\mu V$ and $V_{FG2} = 0.901V$. The results were consistent with those of normal OTAs described in the previous section.

B.3 Summary

In this Appendix, a transconductance amplifier which used CLBTs for low noise and the residual gate effect for trimming the offset was described. Floating gates were shown to be a good way for storing charges required for OTA trimming. An FGOTA with initial offset of $5.67mV$ fabricated using a $1.5\mu m$ n-well CMOS process was successfully trimmed to be less than $10\mu V$.

Appendix C

AMI-ABN $1.5\mu m$ n-well Process Parameters (First Batch)

```
Provided by MOSIS:
http://www.mosis.org/cgi-bin/cgiwrap/umosis/swp/params/ami-abn/t03k-
params.txt

T03K SPICE BSIM3 VERSION 3.1 PARAMETERS
SPICE 3f5 Level 8, Star-HSPICE Level 49, UTMOST Level 8
* DATE: May 24/00
* LOT: t03k                    WAF: 05
* Temperature_parameters=Default
.MODEL CMOSN NMOS (                                  LEVEL   = 49
+VERSION = 3.1            TNOM    = 27               TOX     = 3.12E-8
+XJ      = 3E-7           NCH     = 7.5E16           VTH0    = 0.5903183
+K1      = 0.9587197      K2      = -0.0703124       K3      = 7.3462516
+K3B     = -1.8217143     W0      = 3.580548E-7      NLX     = 1E-8
+DVT0W   = 0              DVT1W   = 0                DVT2W   = 0
+DVT0    = 0.7328029      DVT1    = 0.2424502        DVT2    = -0.2050429
+U0      = 689.3279051    UA      = 2.357804E-9      UB      = 2.06224E-19
+UC      = 4.812442E-11   VSAT    = 1.482765E5       A0      = 0.7369712
```

```
+AGS     = 0.1133263      B0      = 1.36088E-6     B1      = 5E-6
+KETA    = -3.845663E-3   A1      = 5.405407E-4    A2      = 0.4886241
+RDSW    = 2.926798E3     PRWG    = -0.0596312     PRWB    = -0.0518228
+WR      = 1              WINT    = 6.944201E-7    LINT    = 2.348738E-7
+XL      = 0              XW      = 0              DWG     = -2.170665E-8
+DWB     = 3.051225E-8    VOFF    = -8.003683E-3   NFACTOR = 0
+CIT     = 0              CDSC    = 2.4E-4         CDSCD   = 0
+CDSCB   = 0              ETA0    = -0.016616      ETAB    = -0.2751783
+DSUB    = 0.898894       PCLM    = 1.6190873      PDIBLC1 = 7.468765E-3
+PDIBLC2 = 2.199057E-3    PDIBLCB = -0.0794461     DROUT   = 0.062272
+PSCBE1  = 1.488034E9     PSCBE2  = 5E-10          PVAG    = 0.1061084
+DELTA   = 0.01           MOBMOD  = 1              PRT     = 0
+UTE     = -1.5           KT1     = -0.11          KT1L    = 0
+KT2     = 0.022          UA1     = 4.31E-9        UB1     = -7.61E-18
+UC1     = -5.6E-11       AT      = 3.3E4          WL      = 0
+WLN     = 1              WW      = 0              WWN     = 1
+WWL     = 0              LL      = 0              LLN     = 1
+LW      = 0              LWN     = 1              LWL     = 0
+CAPMOD  = 2              XPART   = 0.4            CGDO    = 1.67E-10
+CGSO    = 1.67E-10       CGBO    = 1E-11          CJ      = 2.871391E-4
+PB      = 0.9650878      MJ      = 0.5191048      CJSW    = 1.287484E-10
+PBSW    = 0.99           MJSW    = 0.1            CF      = 0           )
*
.MODEL CMOSP PMOS (                                LEVEL   = 49
+VERSION = 3.1            TNOM    = 27             TOX     = 3.12E-8
+XJ      = 3E-7           NCH     = 2.4E16         VTH0    = -0.721901
+K1      = 0.4504895      K2      = 7.44969E-7     K3      = 12.4287693
+K3B     = -2.0238234     W0      = 2.667845E-7    NLX     = 7.030273E-7
+DVT0W   = 0              DVT1W   = 0              DVT2W   = 0
```

```
+DVT0    = 1.0333326     DVT1    = 0.2741578     DVT2    = -0.0643206
+U0      = 264.2496194   UA      = 4.896349E-9   UB      = 1.083086E-21
+UC      = -1.04926E-10  VSAT    = 1.81286E5     A0      = 0.178225
+AGS     = 0.148856      B0      = 4.310015E-6   B1      = 5E-6
+KETA    = -3.524955E-3  A1      = 0             A2      = 0.2159697
+RDSW    = 1.084351E3    PRWG    = 3.028969E-3   PRWB    = -0.2799616
+WR      = 1             WINT    = 7.844628E-7   LINT    = 8.142472E-8
+XL      = 0             XW      = 0             DWG     = -2.956928E-8
+DWB     = 3.181366E-8   VOFF    = -0.0542035    NFACTOR = 0.2360326
+CIT     = 0             CDSC    = 2.4E-4        CDSCD   = 0
+CDSCB   = 0             ETA0    = 0.02765       ETAB    = -1.009098E-4
+DSUB    = 0.1573752     PCLM    = 3.519463      PDIBLC1 = 1.697242E-3
+PDIBLC2 = 2.148623E-3   PDIBLCB = 1.18207E-3    DROUT   = 0.0386639
+PSCBE1  = 1.492954E9    PSCBE2  = 1.922198E-9   PVAG    = 0.1553586
+DELTA   = 0.01          MOBMOD  = 1             PRT     = 0
+UTE     = -1.5          KT1     = -0.11         KT1L    = 0
+KT2     = 0.022         UA1     = 4.31E-9       UB1     = -7.61E-18
+UC1     = -5.6E-11      AT      = 3.3E4         WL      = 0
+WLN     = 1             WW      = 0             WWN     = 1
+WWL     = 0             LL      = 0             LLN     = 1
+LW      = 0             LWN     = 1             LWL     = 0
+CAPMOD  = 2             XPART   = 0.4           CGDO    = 2.21E-10
+CGSO    = 2.21E-10      CGBO    = 1E-11         CJ      = 2.773731E-4
+PB      = 0.7430725     MJ      = 0.4316544     CJSW    = 1.803877E-10
+PBSW    = 0.99          MJSW    = 0.1022318     CF      = 0              )
```

Appendix D

AMI-ABN $1.5\mu m$ n-well Process Parameters (Second Batch)

```
Provided by MOSIS:
http://www.mosis.org/cgi-bin/cgiwrap/umosis/swp/params/ami-abn/t09z
-params.txt

T09Z SPICE BSIM3 VERSION 3.1 PARAMETERS
SPICE 3f5 Level 8, Star-HSPICE Level 49, UTMOST Level 8
* DATE: Nov 15/00
* LOT: T09Z                  WAF: 03
* Temperature_parameters=Default
.MODEL CMOSN NMOS (                              LEVEL   = 49
+VERSION = 3.1          TNOM    = 27             TOX     = 3.16E-8
+XJ      = 3E-7         NCH     = 7.5E16         VTH0    = 0.5513465
+K1      = 0.9662553    K2      = -0.0739446     K3      = 13.1449046
+K3B     = -6.1796255   W0      = 1E-5           NLX     = 1E-8
+DVT0W   = 0            DVT1W   = 0              DVT2W   = 0
+DVT0    = 0.8445798    DVT1    = 0.4222699      DVT2    = -0.3675825
+U0      = 639.5850946  UA      = 1.112728E-9    UB      = 1.618549E-18
+UC      = 6.766521E-12 VSAT    = 1.116886E5     A0      = 0.6406476
```

```
+AGS     = 0.0835774      B0      = 1.709473E-6    B1      = 5E-6
+KETA    = -3.466964E-3   A1      = 0              A2      = 1
+RDSW    = 3E3            PRWG    = -0.0317338     PRWB    = -0.0366101
+WR      = 1              WINT    = 6.256764E-7    LINT    = 2.623417E-7
+XL      = 0              XW      = 0              DWG     = -6.480276E-9
+DWB     = 3.712087E-8    VOFF    = -0.0213964     NFACTOR = 0.6290693
+CIT     = 0              CDSC    = 0              CDSCD   = 0
+CDSCB   = 5.240693E-5    ETA0    = -1             ETAB    = -0.08048
+DSUB    = 1              PCLM    = 1.2188601      PDIBLC1 = 7.898452E-3
+PDIBLC2 = 1.931811E-3    PDIBLCB = -0.1           DROUT   = 0.0568803
+PSCBE1  = 5.876864E9     PSCBE2  = 2.082232E-9    PVAG    = 0.1729939
+DELTA   = 0.01           RSH     = 53             MOBMOD  = 1
+PRT     = 0              UTE     = -1.5           KT1     = -0.11
+KT1L    = 0              KT2     = 0.022          UA1     = 4.31E-9
+UB1     = -7.61E-18      UC1     = -5.6E-11       AT      = 3.3E4
+WL      = 0              WLN     = 1              WW      = 0
+WWN     = 1              WWL     = 0              LL      = 0
+LLN     = 1              LW      = 0              LWN     = 1
+LWL     = 0              CAPMOD  = 2              XPART   = 0.4
+CGDO    = 1.79E-10       CGSO    = 1.79E-10       CGBO    = 1E-9
+CJ      = 2.869797E-4    PB      = 0.99           MJ      = 0.5314948
+CJSW    = 1.553965E-10   PBSW    = 0.99           MJSW    = 0.1
+CF      = 0            )
*
.MODEL CMOSP PMOS (                                LEVEL   = 49
+VERSION = 3.1            TNOM    = 27             TOX     = 3.16E-8
+XJ      = 3E-7           NCH     = 2.4E16         VTH0    = -0.8002516
+K1      = 0.4612185      K2      = -8.435342E-6   K3      = 14.0089935
+K3B     = -2.5658256     W0      = 2.446962E-6    NLX     = 7.841214E-7
```

```
+DVT0W   = 0             DVT1W   = 0             DVT2W   = 0
+DVT0    = 1.2531383     DVT1    = 0.3657227     DVT2    = -0.0648652
+U0      = 246.45306     UA      = 3.869902E-9   UB      = 1E-21
+UC      = -1.11744E-10  VSAT    = 2E5           A0      = 0.4772375
+AGS     = 0.1500772     B0      = 3.862432E-6   B1      = 5E-6
+KETA    = -2.106339E-3  A1      = 0             A2      = 0.364
+RDSW    = 3E3           PRWG    = 0.0770871     PRWB    = -0.1344699
+WR      = 1             WINT    = 7.336969E-7   LINT    = 1.413122E-7
+XL      = 0             XW      = 0             DWG     = -2.439851E-8
+DWB     = 4.050848E-8   VOFF    = -0.0518651    NFACTOR = 0.5350168
+CIT     = 0             CDSC    = 0             CDSCD   = 0
+CDSCB   = 1.054811E-4   ETA0    = 0.06903       ETAB    = 3.787991E-4
+DSUB    = 0.2873        PCLM    = 5.2078859     PDIBLC1 = 9.107209E-5
+PDIBLC2 = 1E-3          PDIBLCB = -1E-3         DROUT   = 0.0556701
+PSCBE1  = 3.308675E9    PSCBE2  = 6.843803E-8   PVAG    = 9.5257414
+DELTA   = 0.01          RSH     = 74.5          MOBMOD  = 1
+PRT     = 0             UTE     = -1.5          KT1     = -0.11
+KT1L    = 0             KT2     = 0.022         UA1     = 4.31E-9
+UB1     = -7.61E-18     UC1     = -5.6E-11      AT      = 3.3E4
+WL      = 0             WLN     = 1             WW      = 0
+WWN     = 1             WWL     = 0             LL      = 0
+LLN     = 1             LW      = 0             LWN     = 1
+LWL     = 0             CAPMOD  = 2             XPART   = 0.4
+CGDO    = 2.33E-10      CGSO    = 2.33E-10      CGBO    = 1E-9
+CJ      = 2.951059E-4   PB      = 0.7404097     MJ      = 0.426184
+CJSW    = 1.929182E-10  PBSW    = 0.99          MJSW    = 0.1569554
+CF      = 0           )
```

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