A Low Voltage 900 MHz CMOS Mixer

BY

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Abstract

Abstract of thesis entitled:

A Low Voltage 900 MHz CMOS Mixer

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This thesis presents two low voltage mixer architectures. They are **(1) Current Folded Mirror Mixer**, and **(2) Current Mode Mixer**. The two different architectures used could reduce the number of series connected transistors.

The current folded mirror mixer, which use a current mirror to connect a Gilbert quad (LO part) to the emitter coupled pair (RF part) in parallel instead of the series connection. So, it could operate at a single 1.5 V voltage supply. The current mode mixer could even operate at a lower voltage at 1.2 V. Moreover, the linearity is much better. It is due to the using of input RF and LO current instead of voltage. Two testing circuits have been designed, tested and fabricated with an **AMS® 0.6 μm CMOS** technology.

The measurement results of the two circuits show good agreement with the

simulation results. Experimentally, the Current Folded Mirror Mixer achieves an input 900 MHz at which IIP3 of 1 dBm is measured. Its conversion loss and 1-dB compression are measured to be 2.5 dB and –3 dBm respectively. It occupies an active die area 250 μm × 300 μm, and consumes 7.5 mW from a single 1.5 V supply.

The second circuit is a Current Mode Mixer, which has a better linearity at a lower supply voltage than the current folded mirror mixer. From the measurement result, it achieves an input 900 MHz and down converted to 10 MHz with –9.1 dB conversion gain. The 1-dB compression point and IIP3 are measured to be 3 dBm and 10 dBm respectively. It dissipates 3 mW from a single 1.2 V voltage supply and the active area is 400 μm × 400 μm.

The two new low voltage current folded mirror mixer and current mode mixer have similar performance compare to conventional Gilbert Cell mixer, which cannot operate at less than 1.5 V.

摘要

本論文將介紹兩個使用不同結構的低電壓混頻器，它們分別是（1）電流源摺疊鏡像混頻器，和（2）電流模混頻器。由於兩種不同結構方法的運用，因此能減少晶體管串聯接合的數目。

電流源摺疊鏡像混頻器，是利用電流鏡並聯的方式代替了串聯的方式把吉伯四元組 Gilbert quad（震盪器部份）和射極耦合對（射頻部份）連接一起，因此，它能夠在 1.5 V 的低電壓下操作。電流模混頻器更能在更低的電壓下 1.2 V 操作，而且，它能給予更好的線性度，這是由於震盪器部份和射頻部份的輸入改用了電流的方式而不是電壓的方式。這兩個測試電路已經被設計、製造和測試，而其製程利用了 AMS© 0.6 微米互補金屬氧化半導體技術。

這兩個電路的實驗結果顯示與電腦的模擬結果有相當程度的吻合。在實驗中，電流源摺疊鏡像混頻器在 900 兆赫輸入下，它的輸入三階截距點能達到 1 dBm，而它的全頻帶轉換增益和 1-dB 增益壓縮點分別為-2.5 dB 和 -3 dBm，電路小片的有效面積為 250 微米乘 300 微米，在單一的 1.5 V 電壓供應下，它的總功率消耗為 7.5 mW。

第二個電路是電流模混頻器，它能在更低的電壓供應下給予更佳的線性度。在實驗的結果中，電流模混頻器在 900 兆赫輸入及向下移頻到 10 兆赫下，它的全頻帶轉換增益是-9.1 dB，輸入三階截距點和 1-dB 增益壓縮點分別為 3 dBm 和 10 dBm，在單一的 1.2 V 電壓供應下，它的總功率消耗為

3 mW，而電路小片的有效面積為 400 微米乘 400 微米。

這兩個新的低電壓混頻器能夠給予相當接近的效能相比吉伯盒式(Gilbert Cell)混頻器，而且吉伯盒式混頻器不能於 1.5 V 或更低的電壓下運作。

Acknowledgments

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Chapter 1

Introduction

1.1 Motivation

The ability to communicate with people on the move has evolved remarkably. The new wireless communications methods and services have been enthusiastically adopted by people throughout the world. Particularly during the past ten years, interest and demand for portable wireless communication services like digital cellular phones have increased the emphasis on the development of low-cost, high-performance communications ICs. The operating frequency bands used in the modern mobile systems range from 900 MHz to 1.9 GHz, for example, Global System for Mobile (GSM) is operated at 900 MHz and 1.8 GHz, and the Personal Communication Services (PCS) operated at 1.9 GHz. At such high frequencies, the mobile system usually consists of several ICs and many discrete components, which increase the size and power consumption. These factors limit the size, weight and battery life of mobile systems.

The latest sub-micron CMOS technologies offer a feasible and attractive solution to this problem. The new CMOS technologies are suitable for single chip transceiver implementation, we can design and build a complete communications

system on a single chip.

The major CMOS RF building blocks for a single chip system included low-noise amplifiers (LNA), bandpass filters (BPF), mixers, voltage control oscillators (VCO) and power amplifiers (PA). Several designs have been reported in different literatures [[1], [2], [3], [4], [5], [6]] recently. However, most of the published designs have some drawbacks such as poor noise performance, poor linearity and high operating voltage (3 V or higher). This thesis is focused on the mixer building block, our goal is to design and build a CMOS RF mixer, which can operate by a single 1.5 V or even lower voltage supply.

1.2 Technical Challenges of CMOS RF Design

The evolution of CMOS technologies to sub-micron and deep sub-micron has bought the operating frequency, f_t, beyond the GHz range. However, it is still a big challenge to design RF frequency integrated circuit because of the inherent nature of the CMOS technology, such as large device parasitic capacitances, inaccurate high-frequency transistor models, and lack of high-quality and precise on-chip passive components. To overcome these design barriers, special new circuit design techniques are needed. We will address some of this new technique in Chapter 6.

1.3 General Background

Mixer is one of the fundamental building blocks in communication systems such as lock-in amplifiers [[7], [8]] and wireless receivers [[9], [10]], as shown in Figure 1.1 and Figure 1.2 respectively.

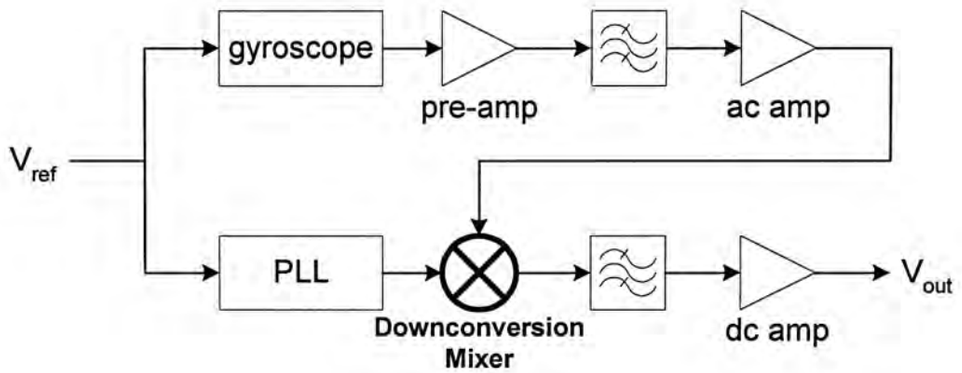


Figure 1.1: The block diagram of a lock-in amplifier

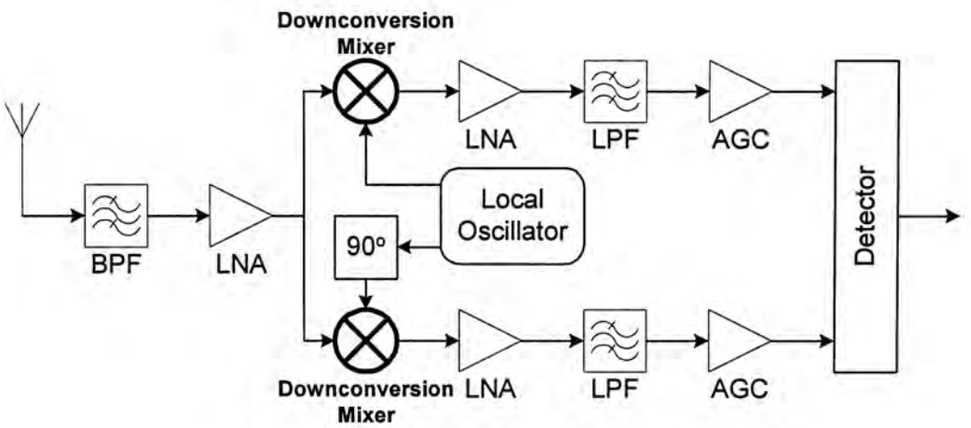


Figure 1.2: A simplified front-end RF receiver

Shown in Figure 1.2 is a simplified block diagram of a front-end RF receiver. At this high frequency, conventional designs use GaAs or bipolar transistors and discrete surface acoustic wave (SAW) filters. Since each component is using different technologies, thus, it is not possible to fabricate a single chip system. In addition, high-power output buffers are required to drive the signals from one chip to another. Therefore, conventional RF front end requires several discrete components to build.

1.3.1 Bipolar and CMOS Mixers

The Gilbert multiplier cell is one of the most commonly used mixer. However, the linearity of the bipolar mixer is not good due to the exponential I-V characteristics of the bipolar transistor. Resistive degeneration is a well-known technique to reduce the non-linearity at the expense of power dissipation and noise performance. Recently, capacitive degeneration is another approach to linearize the circuit with less power consumption [3].

The CMOS mixer based on the traditional bipolar cross-coupled differential modulator stage introduced by Gilbert [11]. However, the operation of the bipolar mixer proposed by Gilbert is due to the translinear of the bipolar transistor. This phenomenon does not translate directly into an equivalent CMOS current behavior. The CMOS counterpart of the traditional bipolar mixer is therefore operated in a switching mode instead. Usually, a fully differential structure is used in order to be effectively suppressed the quadratic nonlinearity. So, CMOS mixers not only have the advantage of being integrable, but also have a better linearity.

1.4 Research Goal

The successful implementations of many RF front-end circuits in CMOS technology have shown the feasibility of a low-cost high-performance single chip transceiver, but CMOS RF circuits are still at an early stage of the research topic. Therefore, more research efforts are needed to improve the performance of RF CMOS components.

This thesis attempts to design, fabricate and measure an RF downconversion mixer using standard CMOS technology. The major focus is not only on CMOS

implementation but also on low-voltage, high linearity and large dynamic range.

1.5 Thesis Outline

The operating principles of mixers are reviewed in Chapter 2, followed by the definition of some basic terminologies and analysis parameters, such as conversion, linearity and noise performance, for characterizing RF circuits.

Chapter 3 will give out the brief introduction and comparison on different CMOS mixer topologies used in the past. Afterwards, the two proposed mixers will be analyzed in detail in terms of large and small signal analysis, conversion gain and noise performance in Chapter 4.

In Chapter 5, the two proposed mixers would be simulated using SpectreRF® simulator in order to verify the working principle. At the same time, it would be given out the simulation result of the conversion gain and linearity etc..

Chapter 6 covers some special techniques for drawing analog components layout, including transistors, resistors, capacitors, substrate tap and pad.

Then the testing prototypes and measurement setups are outlined in Chapter 7. Detailed measurements of two proposed downconversion mixers are presented.

Chapter 8 concludes the whole thesis with a summary of the achievements and the experimental result in this research

Chapter 2

RF Fundamentals

2.1 Introduction

This chapter provides some general background to facilitate the discussion of the mixer. The operating principles as well as the figure of merits used for characterizing mixer performance are reviewed. In addition, analyses of these figures help to optimize the circuits for different applications. For example, the distortion sets the largest input signal level before the nonlinearity dominated. Moreover, it is very important for engineers to understand the meaning of these figures, because they are the common languages to specific the entire system.

2.2 Frequency Translation

Most RF communication transceivers manufactured today utilize a conventional superheterodyne approach. In this architecture, the mixer translates an incoming Radio Frequency (RF) signal to a lower frequency, known as the intermediate frequency (IF). Armstrong invented this architecture in 1918 [12], sought this frequency lowering simply to make it easier to obtain the requisite gain, other significant advantages accrue as well. The two modified architectures, direct

conversion [13] and wide-band IF with double conversion [14], have invented later, their operation principle is similar to the superheterodyne. Therefore, "frequency translation" or "mixing" becomes an essential part of wireless communication. This process can be accomplished by multiplication of an RF signal with a periodic one. "***Mixer***" is a circuit element responsible for this operation in the receiver.

The basic operation of a mixer is to multiply two signals in time domain. The following equations illustrate the basic multiplication of two signals:

Received Signal: $$X_{RF}(t) = A_{RF}\cos\omega_{RF}t + A_{IM}\cos\omega_{IM}t \quad (2.1)$$

Local Oscillator: $$X_{LO}(t) = A_{LO}\cos\omega_{LO}t \quad (2.2)$$

where $A_{RF}\cos\omega_{RF}t$ represents the RF wanted signal

$A_{IM}\cos\omega_{IM}t$ represents the image signal

$A_{LO}\cos\omega_{LO}t$ represents the LO signal

After multiplication:

$$\begin{aligned} X_{IF}(t) &= (A_{RF}\cos\omega_{RF}t + A_{IM}\cos_{IM}t)(A_{LO}\cos\omega_{LO}t) \\ &= A_{RF}A_{LO}\cos\omega_{LO}t\cos\omega_{RF}t + A_{IM}A_{LO}\cos\omega_{LO}t\cos\omega_{IM}t \\ &= \frac{A_{RF}A_{LO}}{2}\left[\cos(\omega_{LO}-\omega_{RF})t + \cos(\omega_{LO}+\omega_{RF})t\right] \\ &\quad + \frac{A_{IM}A_{LO}}{2}\left[\cos(\omega_{IM}-\omega_{RF})t + \cos(\omega_{IM}+\omega_{RF})t\right] \end{aligned} \quad (2.3)$$

Multiplication generates results in output signals at the sum and difference frequencies of the input signals, as shown in Figure 2.1.

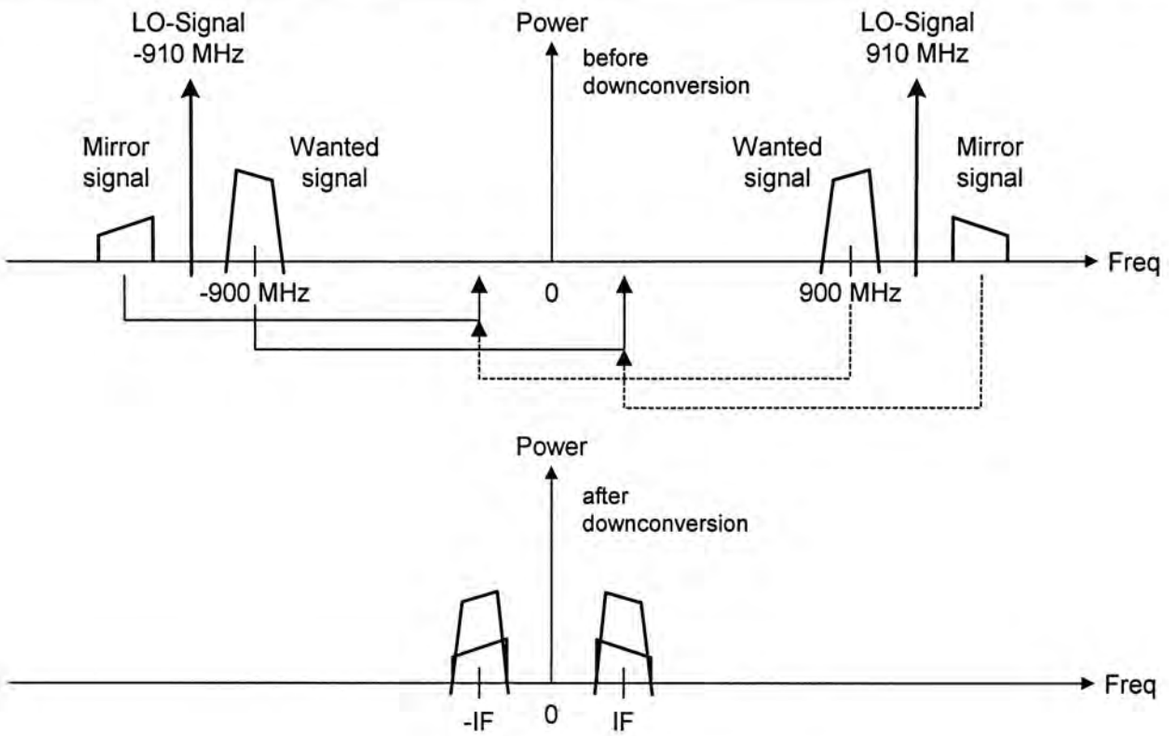


Figure 2.1: The downconversion scheme of an IF receiver

2.3 Conversion Gain

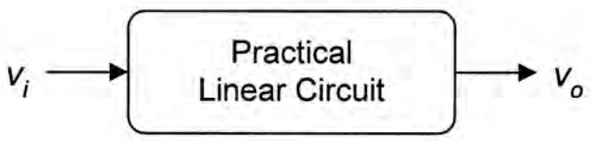
One important mixer characteristic is conversion gain (or loss), which is defined as the ratio of the desired IF output to the value of the RF input expressed as a power ratio. Conversion gain can be greater than unity in active mixers; whereas the passive one is always smaller than unity. Conversion gain in excess of unity is usually preferred because of the larger output signal; however, a high conversion gain does not guarantee a better sensitivity. Hence we also need to consider the noise figure of the system.

2.4 Linearity

In RF circuits, linearity is an useful parameter to measure the dynamic range. When a receiver is detecting a weak radio signal at the present of a strong

interference signal. The strong interference signal can drive the receiver into nonlinear region and generate new frequencies, which may swamp out the desired weak signal. Thus, the linearity of a receiver determines the maximum allowable signal level at its input.

All real-life linear systems exhibit some degree of nonlinearity. Suppose the output-to-input characteristic of a system can be modeled by a Power Series shown in Figure 2.2:



$$v_o = a_0 + a_1 v_i + a_2 v_i^2 + a_3 v_i^3 + \ldots \tag{2.4}$$

Figure 2.2: Linear system modeled by a Power Series

For analytical simplicity, terms higher than the third power are neglected in hand calculations.

Now, consider two sinusoidal input signals in different amplitude and slightly different frequencies:

$$v_i = A_1 \cos\omega_1 t + A_2 \cos\omega_2 t \tag{2.5}$$

Substituting equation (2.5) into the power series, after expanding and collecting the same terms, we could find:

The fundamental frequency terms:

$$\text{At } \omega_1: \quad \left(a_1 + \frac{3}{4}a_3 A_1^2 + \frac{3}{2}a_3 A_2^2\right) A_1 \cos\omega_1 t \tag{2.6}$$

$$\text{At } \omega_2: \quad \left(a_1 + \frac{3}{4}a_3 A_2^2 + \frac{3}{2}a_3 A_1^2\right) A_2 \cos\omega_2 t \tag{2.7}$$

Second-order terms:

$$\text{At } 2\omega_1: \quad \left(\frac{1}{2}a_2A_1^2\right)\cos 2\omega_1 t \tag{2.8}$$

$$\text{At } 2\omega_2: \quad \left(\frac{1}{2}a_2A_2^2\right)\cos 2\omega_2 t \tag{2.9}$$

$$\text{At } \omega_1 \pm \omega_2: \quad (a_2A_1A_2)[\cos(\omega_1+\omega_2)t + \cos(\omega_1-\omega_2)t] \tag{2.10}$$

Third-order terms:

$$\text{At } 3\omega_1: \quad \left(\frac{1}{4}a_3A_1^3\right)\cos 3\omega_1 t \tag{2.11}$$

$$\text{At } 3\omega_2: \quad \left(\frac{1}{4}a_3A_2^3\right)\cos 3\omega_2 t \tag{2.12}$$

$$\text{At } 2\omega_1 \pm \omega_2: \quad \left(\frac{3}{4}a_3A_1^2A_2\right)[\cos(2\omega_1+\omega_2)t + \cos(2\omega_1-\omega_2)t] \tag{2.13}$$

$$\text{At } \omega_1 \pm 2\omega_2: \quad \left(\frac{3}{4}a_3A_1A_2^2\right)[\cos(\omega_1+2\omega_2)t + \cos(\omega_1-2\omega_2)t] \tag{2.14}$$

In most circuits of interest, the output is a "compressive" or "saturating" function of the input; that is, the gain approaches zero for sufficiently high input levels as shown in Figure 2.3:

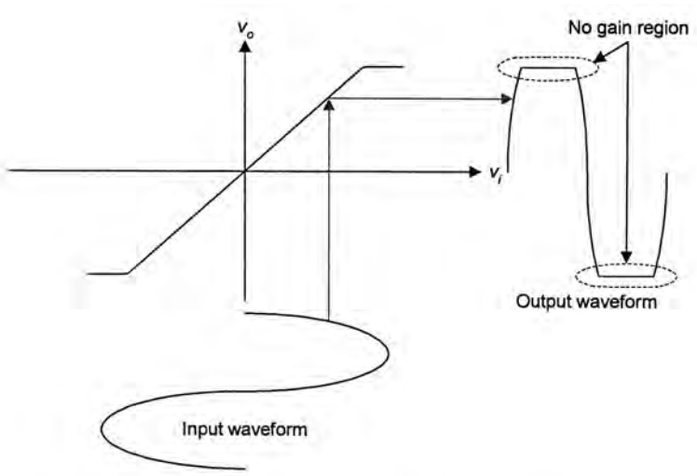


Figure 2.3: A Linear system with saturating characteristics

This compressive transfer curve implies that the first order term and third order terms of the power series equation (2.4) have opposite signs, that is $a_1 = -a_3$. From equation (2.6), we see that the third-order distortion reduces the gain of a mixer as a function of the input amplitude.

2.4.1 1-dB Compression Point

As previous stated that as the input power increases, the gain of the fundamental component would be reduced. So, it has defined that the input level at which the small-signal gain is reduced by 1 dB is called the 1-dB compression point.

For the 1-dB compression simulation, one tone input signal is needed only. Therefore, A_2 in the Equation (2.5) would set to 0. By considering the fundamental component shows in Equation (2.6):

$$20\log a_1 - 1\text{dB} = 20\log\left(a_1 + \frac{3}{4}a_3 A_{-1dB}^2\right)$$

$$A_{-1dB} = \sqrt{0.145\left|\frac{a_1}{a_3}\right|} \qquad (2.15)$$

The 1-dB compression is typically measured in dBm. The graphical representation could be seen in Figure 2.5.

2.4.2 Third Intercept Point (IP3)

As two close interference signals are passed through a non-linear system, a third-order intermodulation product will be created (Figure 2.4). As the amplitude of the two sinusoidal test tones at ω_1 and ω_2 in equation (2.5) are increased with equal amplitude ($A_1 = A_2$), the third-order intermodulation distortion products will be

increased at the rate of a *cubed* as shown in equation (2.13) and (2.14). IP3 is the point at which the amplitude of the third orders harmonic signal is equal to the fundamental signal. The input (*IIP3*) and output (*OIP3*) third-order intercept point are shown in Figure 2.5. IIP3 can be found by equating the coefficient of equation of the fundamental component to the third-order intermodulation component:

$$a_1 A_{IIP3} = \frac{3}{4} a_3 A_{IIP3}^3$$

$$A_{IIP3} = \sqrt{\frac{4}{3}\left|\frac{a_1}{a_3}\right|} \tag{2.16}$$

Comparing equation (2.15) with (2.16), we see that

$$A_{-1dB}(dB) \cong A_{IIP3}(dB) - 10\,dB \tag{2.17}$$

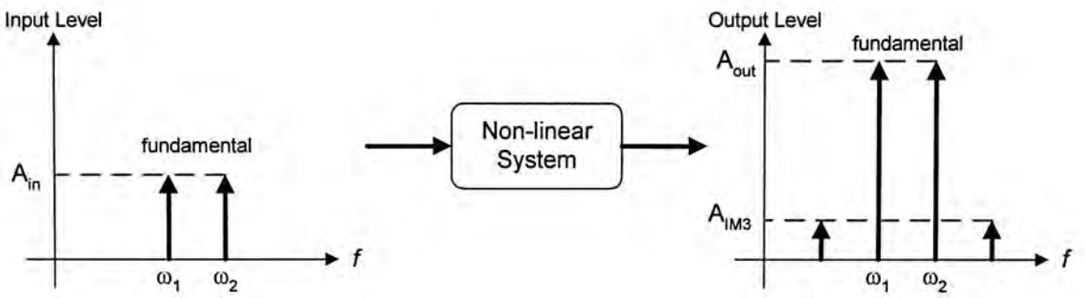


Figure 2.4: Setup of two-tone test

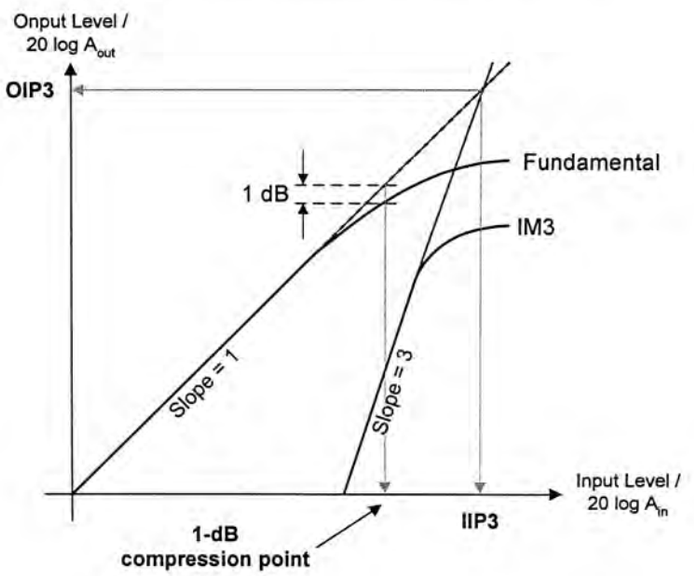


Figure 2.5: Definition of the 1-dB compression point and IIP3

2.5 Dynamic Range (DR)

In wireless environment, radio signal strength can vary greatly depending on the distance between the transmitter and receiver, and the medium in between. We use dynamic range to determine the ability of a receiver to accommodate both large and small signals. Receivers with high dynamic range are more tolerant to the variations of the input signal strength. We can define the DR into two categories: Spurious-Free Dynamic Range (SFDR) and Blocking Dynamic Range (BDR). Usually, the receiver noise floor sets the lower bounds of both dynamic range definitions.

2.5.1 Spurious-Free Dynamic Range (SFDR)

The SFDR is defined as the noise floor corresponding to the signal level at which third-order intermodulation distortion products rise to the noise floor level in the two-tone test (Figure 2.6).

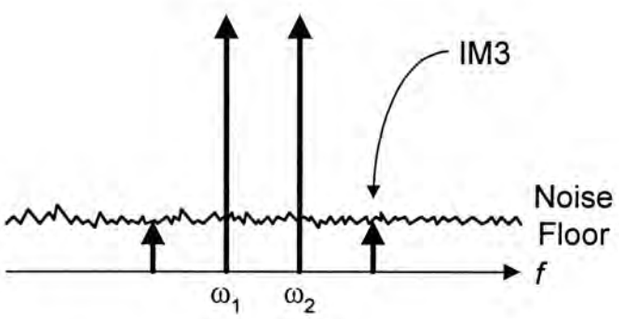


Figure 2.6: Upper bound of SFDR

Figure 2.7 shows the definition of the SFDR graphically. By using trigonometry function, SFDR can be expressed in terms of P_{IIP3} and the P_{NsFlr}.

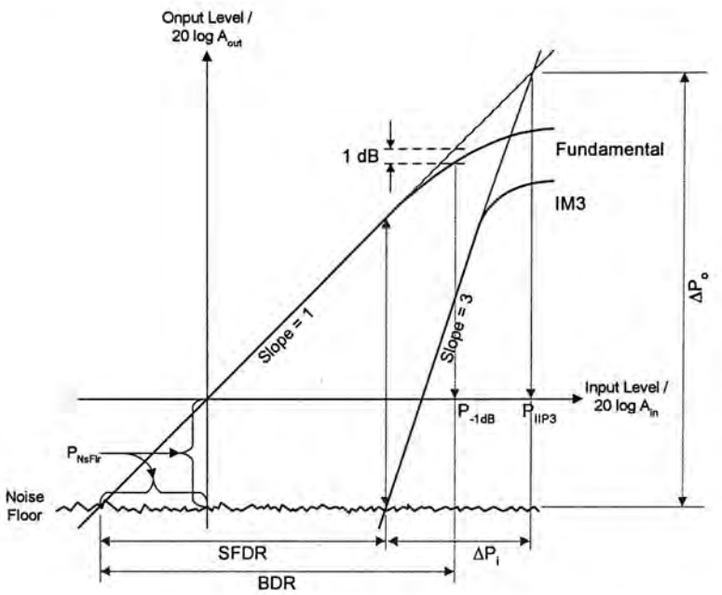


Figure 2.7: Graphical representation of SFDR and BDR

As the fundamental component has a slope of 1 on a dB scale, ΔP_o is equal to (P_{IIP3}-P_{NsFlr}). Since the third-order intermodulation products has a slope of 3 on a dB scale, ΔPi is equal to

$$\Delta P_i = \frac{P_{IIP3} - P_{NsFlr}}{3} \tag{2.18}$$

Therefore, the SFDR is equal to

$$\begin{aligned} \text{SFDR} &= (P_{IIP3} - \Delta P_i) - P_{NiFlr} \\ &= P_{IIP3} - \frac{P_{IIP3} - P_{NiFlr}}{3} - P_{NiFlr} \\ &= \frac{2}{3}(P_{IIP3} - P_{NiFlr}) \end{aligned} \tag{2.19}$$

2.5.2 Blocking Dynamic Range (BDR)

The BDR is defined as the noise floor corresponding to the signal at the 1-dB compression point (Figure 2.7). It is a measure of resilience to a large out-of-band

blocking signal that, by driving the receiver into compression, de-sensitizes it to a small desired signal. BDR can be measured in terms of 1-dB compression point and the noise floor that is equal to

$$BDR = P_{-1dB} - P_{\text{NsFlr}} \tag{2.20}$$

2.6 Blocking and Desensitization

Desensitization would occur when the receiver is detecting a weak signal in the presence of a strong interfering signal, the small signal gain of the receiver is reduced by the interferer. As the interferer's signal amplitude is large enough to reduce the overall gain of the desired signal to zero, the phenomena is known as blocking. To see this effect, set $A_1 << A_2$ in equation (2.5):

$$\left(a_1 + \frac{3}{2}a_3 A_2^2\right) A_1 \cos\omega_1 t \tag{2.21}$$

Since $a_1 = -a_3$, the small signal gain is reduced by $\frac{3}{2}a_3 A_2^2$. When $a_1 + \frac{3}{2}a_3 A_2^2 = 0$, the weak signal is said to be blocked by the interferer.

2.7 Port-to-Port Isolation

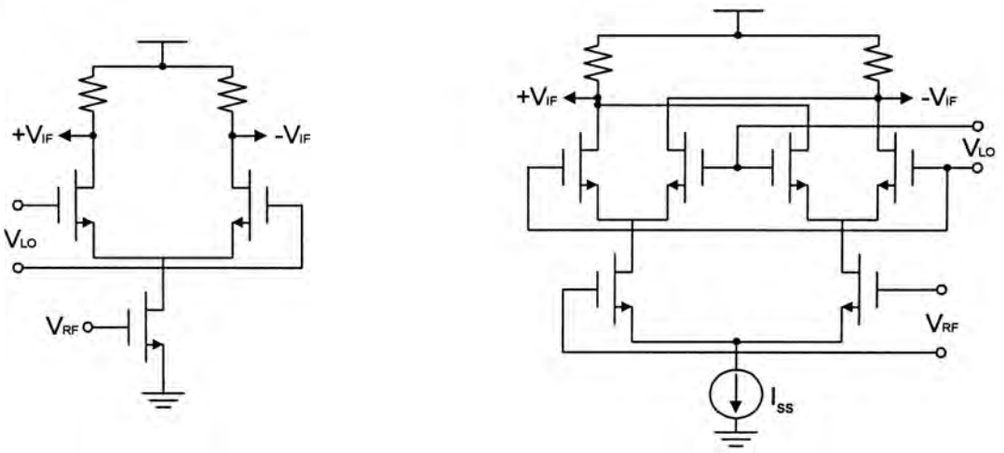
The isolation between each two ports of a mixer is critical. Even though the input or output port, any feedthrough leakage might collapse the whole system such as LO-RF feedthrough results in LO leakage to the LNA or antenna, whereas the RF-LO feedthrough allows strong interferers in the RF path to interact with the local oscillator driving the mixer.

Therefore, it is need to reach a certain required isolation levels to minimize this effect. If the isolation provided by the mixer is inadequate, the preceding or

following circuits must be modified to remedy the problem.

2.8 Single-Balanced and Double-Balanced Mixers

A mixer with a differential LO input signal and a single-ended RF input signal is called a "single-balanced" mixer (Figure 2.8a). If a mixer operates with both differential LO and RF inputs, then it is called a "double balanced" mixer (Figure 2.8b).



(a) (b)

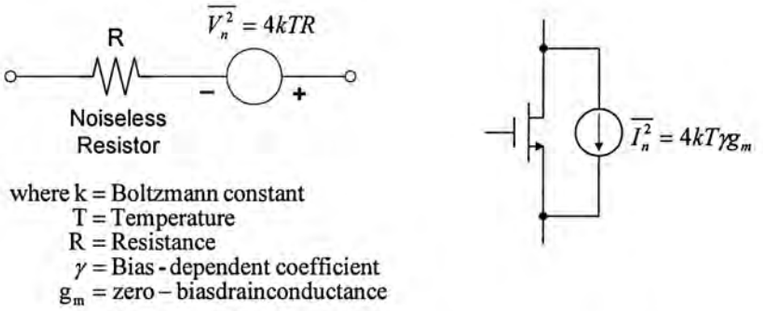
Figure 2.8: (a) Single-balanced mixer, (b) double-balanced mixer

Although the single-balanced configuration exhibits less input-referred noise for a given power dissipation, the double-balanced mixer would be prefer more. It is because it generates less even-order distortion after adding the differential output. Thus relaxing the half-IF issue in heterodyne receivers and lowering the beat components in homodyne architectures.

2.9 Noise

Noise can be loosely defined as any random interference unrelated to the signal of interest. It can take on several forms but usually we only consider in electrical

noise and thermal noise in RF system. Electrical noise arises as a result of random fluctuations in current flow. Thermal noise mainly generated by a resistor or channel resistance of the transistor. The thermal noise of the transistor is usually modeled as a current source connected between the drain and source. The thermal noise of resistors can also be expressed in terms of equivalent noise voltage in series with the resistor having mean squared amplitude (Figure 2.9).



where k = Boltzmann constant
T = Temperature
R = Resistance
γ = Bias - dependent coefficient
g_m = zero – biasdrainconductance

Figure 2.9: Thermal noise model of a resistor and transistor

2.9.1 Noise in the Local Oscillator

Besides the electrical and thermal noise, phase noise from the local oscillator is also a very important factor for designing mixer. Phase noise is a combination of electrical noise, thermal noise and circuit structure of an oscillator.

Figure 2.10 shows the real frequency spectrum of an LO signal. Usually an LO signal is very close to an RF signal. If a noisy LO is applied to a mixer, its noise components at the RF and the image frequency (IM) are downconverted to the IF. Thus, the noise power is raised, however, this universal noise can be removed by using a balanced mixer or bandpass filter.

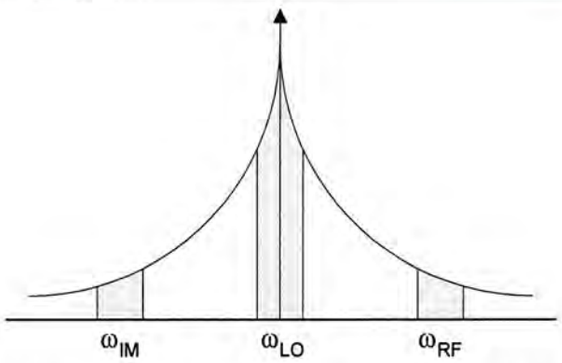


Figure 2.10: The frequency spectrum of the LO signal

The phase noise is also transferred to the received signal directly in the mixing process, RF and the LO frequencies can change the phase angle as well.

2.9.2 Noise Figure

Noise figure (NF) is a figure of merit to measure the noise performance of circuits. It is simply the noise factor expressed in decibels. NF can also be expressed as the amount of signal to noise ratio (SNR) degradation through a circuit block due to the added noise from the circuit block. That is,

$$NF = \frac{S_i/N_i}{S_o/N_o} = \frac{SNR_{in}}{SNR_{out}} \tag{2.22}$$

where S_i and S_o represent the input and output signal powers respectively

N_i and N_o represent the input and output noise powers respectively

SNR_i and SNR_o represent the signal to noise ratio of the input and output respectively

Chapter 3

Downconversion Mixer

3.1 Introduction

This chapter starts with reviewing and comparing different types of CMOS mixer topologies. We have designed two new mixer circuits based on the exciting architectures. The major advantage of the new designs is low operating voltage (1.5 V and 1.2 V). The quantitative theoretical analysis of the new designs will be discussed in detail in Chapter 4. Moreover, simulation results using SpectreRF® simulator based on ***AMS© 0.6 μm*** would be given. Finally, measurement setup and results will be presented and discussed in Chapter 7.

3.2 Review of Mixer Topology

We will give a brief review of some of the common mixer architectures in this section.

3.2.1 Square-Law Mixer

Most of the mixers use nonlinear property of transistors to implement the mixing action [15]. Square-law mixer (Figure 3.1) is one of the examples using this technique. In the mathematical sense, the input-output nonlinear function could be expressed as the equation (2.4). If we assume that the input signal v_i is the sum of two sinusoids,

$$v_i = v_{RF}\cos(\omega_{RF}t) + v_{LO}\cos(\omega_{LO}t) \tag{3.1}$$

After expanding it, we could find the cross-modulation (v_{cross}) output products,

$$\begin{aligned} v_{cross} &= 2a_2 v_{RF} v_{LO}[\cos(\omega_{RF}t)][\cos(\omega_{LO}t)] \\ &= a_2 v_{RF} v_{LO}[\cos(\omega_{RF} - \omega_{LO})t + \cos(\omega_{RF} + \omega_{LO})t] \end{aligned} \tag{3.2}$$

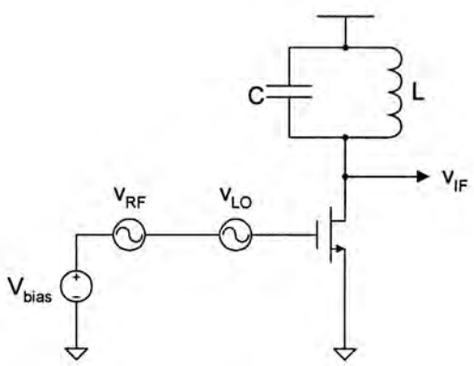


Figure 3.1: Square-law MOSFET mixer

In this schematic, the bias, RF, and LO voltage sources drive the gate in series. The summation of RF and LO signals is accomplished by a resistive or a reactive summers. The main advantage of a square-law mixer is the simple structure and the main disadvantage is the poor isolation between RF and LO signals which will cause problems at the subsequent stages of the system

3.2.2 CMOS Gilbert Cell

A CMOS version, a counter part of bipolar [[16], [17], [18]], of the popular Gilbert cell is shown in Figure 3.2.

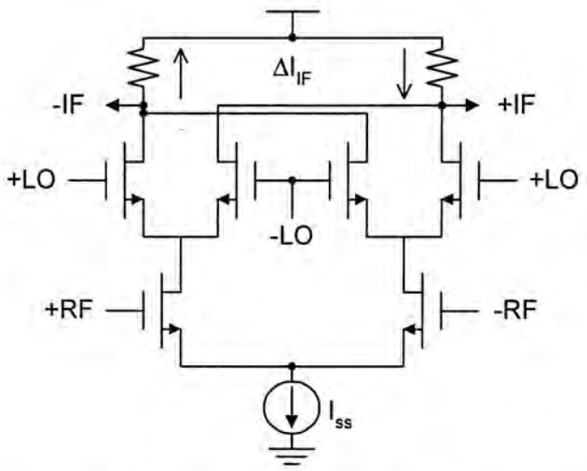


Figure 3.2: CMOS version of the Gilbert Cell Mixer

By assuming the sinusoidal RF input is commutated by a square wave LO signal (this assumption is valid if the LO signal strength is large enough to completely turn on/off the differential pair), the IF output current is

$$\begin{aligned} I_{IF} &= g_m V_{RF} \sin\omega_{RF}t \times sq(\omega_{LO}t) \\ &= g_m V_{RF} \sin\omega_{RF}t \times \left(\frac{4}{\pi}\right)\left(\sin\omega_{LO}t + \frac{1}{3}\sin\omega_{LO}t + \ldots\right) \\ &= \frac{2}{\pi} g_m V_{RF} \cos(\omega_{RF} - \omega_{LO}) \end{aligned} \tag{3.3}$$

As shown in Figure 3.2, the Gilbert Cell mixer is in stacked arrangement Therefore, a high supply voltage is needed for this architecture, which is a draw back for modern low voltage communication system.

3.2.3 Potentiometric Mixer

Another multiplier topology is the potentiometric mixer [19] shown in Figure 3.3. The four CMOS transistor operate in the triode region in order to give more linear voltage to current characteristic. As a result, the RF input signal is as if multiplied by the LO continuously. This architecture has the advantages of simple structure consisting of four CMOS transistors, independent input and output frequency responses, and low distortion. The mixer transfer characteristic can be shown to be,

$$V_{out}^{+} - V_{out}^{-} = K\left(V_{RF}^{+} - V_{RF}^{-}\right) \times \left(V_{LO}^{+} - V_{LO}^{-}\right) \tag{3.4}$$

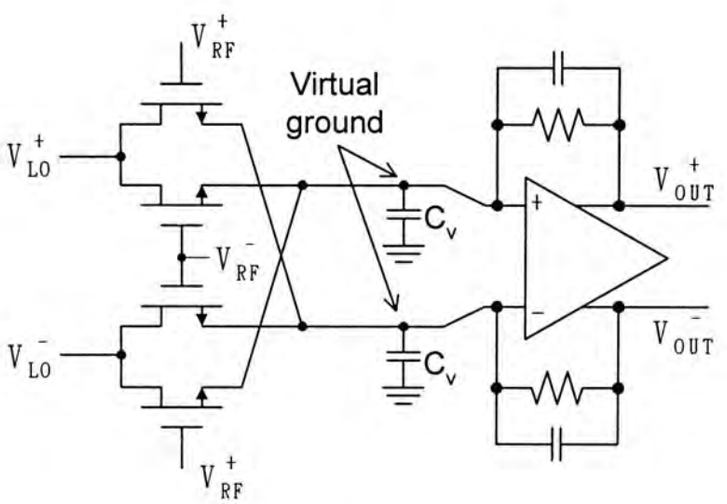


Figure 3.3: Schematic of poteniometric mixer

The vitural ground capacitor (C_v) must be added to the circuit to increase input frequency range, so the high frequency will be by-passed by the capacitor and only the down-converted frequency is fed into the opamp, which converts the output current of the mixing transistors back into voltage. However, the gain-bandwidth product of the opamp limits the ideal response of the virtual ground at high frequency,

thus, off-chip filtering capacitors is usually required. Another disadvantages of this circuit include the output bandwidth limitation due to the opamp's finite GBW and a relatively high noise figure [15].

3.2.4 Subsampling Mixer

Subsampling mixer is another class of mixer, which multiplies the input signal with a periodic switching LO signal such as square wave. The LO signal changes the polarities between positive and negative, and vice-versa. The input signal is effectively sampled at the switching frequency. Actually, this kind of technique has been adopted in the single, double-balanced diode mixers [15].

In Figure 3.4, the higher-frequency signal is sampled at the instants indicated by the dots, while the downconverted signal is shown as the lower frequency reconstruction. The theoretical advantage of this design is much easier to realize samplers that operate at a frequency well below the incoming RF signal.

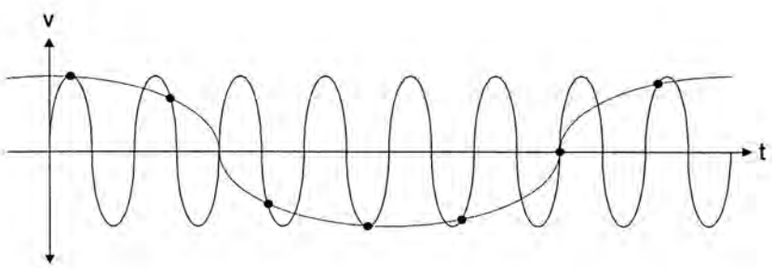


Figure 3.4: Illustration of subsampling

Although it is clocked at a relatively low frequency, the sampler must still possess good time resolution to avoid a large sampling error. Moreover, this design has a large noise figure, which is a major problem for the subsampling mixers.

Chapter 4

Proposed Downconversion Mixer

4.1 Analysis of Proposal Mixer

In the previous chapter, we have introduced different mixer architectures. However, most of the exciting architectures are not suitable for low voltage operation required by modern sub-micron CMOS technologies. Therefore, we have proposed two new mixers design, which are especially designed for ***low voltage supply***.

The two new designs are **(1) Current Folded Mirror method** and **(2) Current Mode method** respectively. These two new mixers designs are based on a double-balanced structure.

4.2 Current Folded Mirror Mixer

Conventional Gilbert Cell mixer (Figure 3.2) is difficult to operate at low supply voltage, because the series connected transistors. Since all the MOSFETs must be in saturation, neglecting body effect, each transistor requires at least 0.7 V between drain and source. Consequently, an operating voltage at least $3 \times 0.7\ V = 2.1\ V$ is required. Therefore, conventional Gilbert architecture cannot operate at low voltage.

The new current folded mirror mixer architecture has only two stacked

transistors compare to three or four transistors stack in conventional architecture. Therefore, we can reduce the supply voltage below to 1.5 V [[20], [21], [22], [23]]. The structure of the current folded mirror mixer is shown in Figure 4.1.

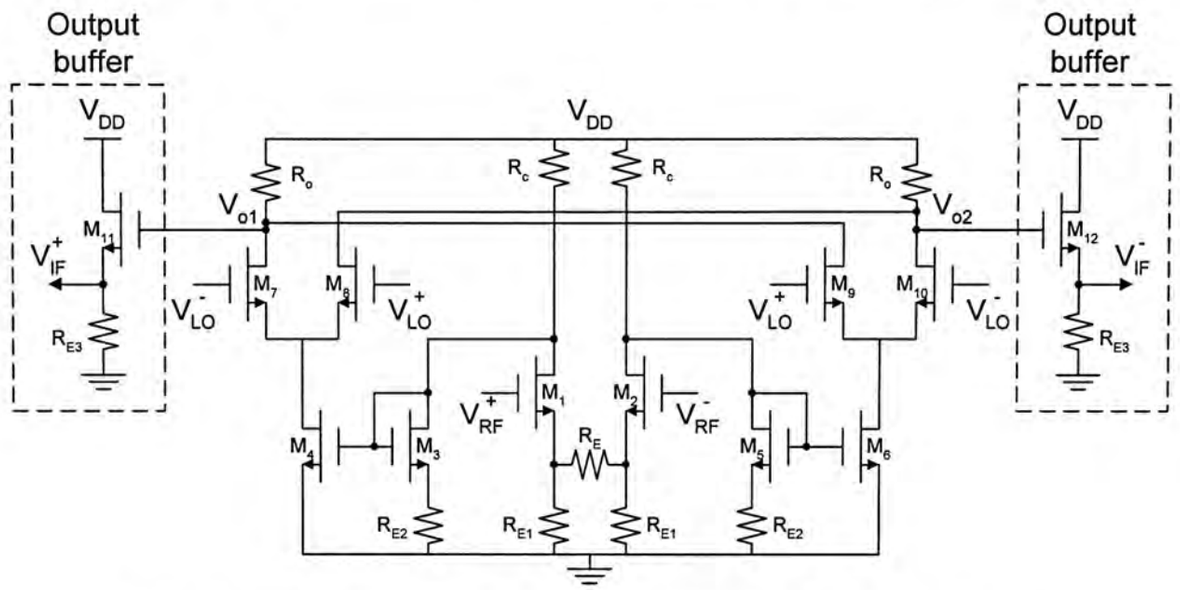


Figure 4.1: Schematic diagram of the current folded mirror mixer

4.2.1 Operating Principle

The circuit uses an emitter-coupled pair (M_1, M_2) with source degeneration resistors R_{E1} to form a differential folded mirror. M_3, M_4 and M_5, M_6 are two current mirrors to bias the Gilbert quad $M_7 - M_{10}$. It uses a pair of differential folded mirror, M_3, M_4 and M_5, M_6, to fold the RF part to the LO part in order to decrease the number of the stacked transistors. So, it could reduce the voltage supply down to less than 1.5 V.

Transistors $M_7 - M_{10}$ have to be biased in moderate inversion to accommodate the large LO input signal. Transistors $M_7 - M_{10}$ transistors are operating like a switch as illustrated in Figure 4.2 because of the large LO signal. Therefore, in the off-state V_{RF} is made lower than the transistor threshold voltage (V_{th}) and reverse in the on-state.

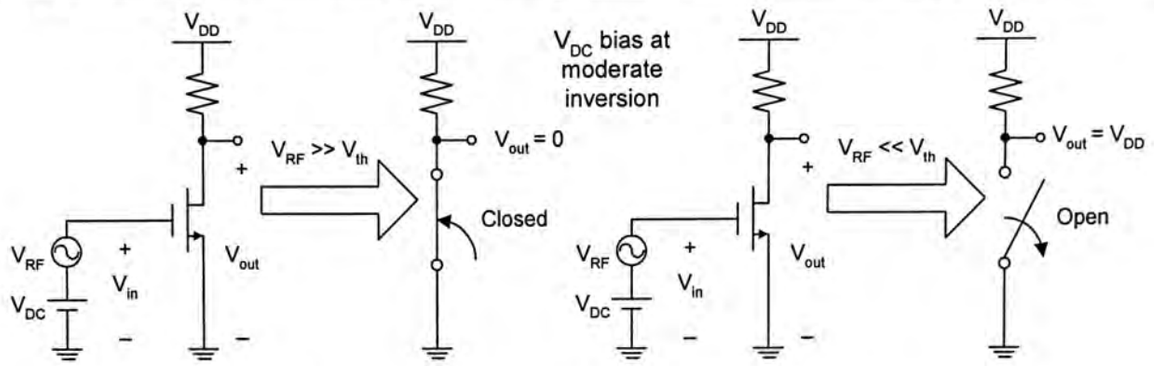


Figure 4.2: MOSFET working as a switch

Moreover, the double-balanced mixer is constructed in order to generate less even-order distortion after adding the differential IF output.

4.2.2 Large Signal Analysis

Due to the differential input into the transistors $M_7 - M_{10}$, only two of the four transistors in the Gilbert quad are conducting at any time. Therefore, the mixer can be considered as consisting of two identical pairs. All secondary effects such as channel-length modulation and body effect are neglected at this moment.

As illustrated in Figure 4.3, the proposed mixer relies on the three parts. In the derivation, assuming all CMOS transistors follow the simple current square law operation in the saturation region.

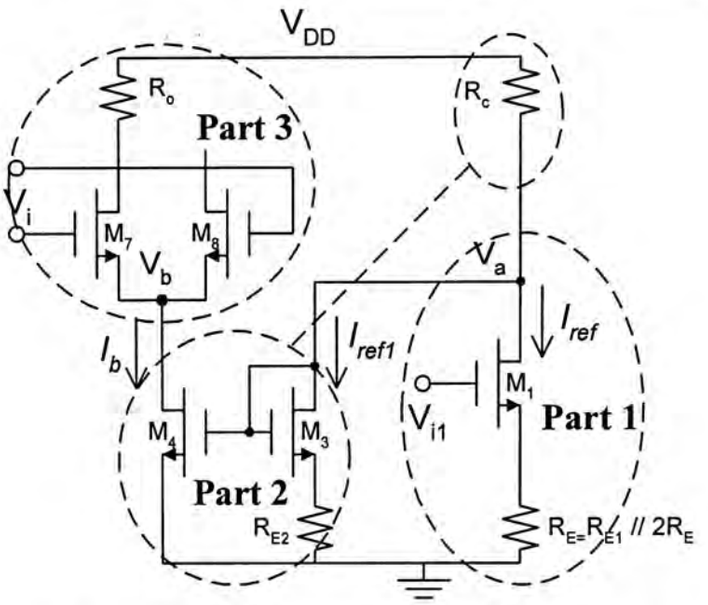


Figure 4.3: Simplified schematic of the downconversion mixer in a large signal analysis

Part 1: Common emitter

M_1 is bias in the saturation mode; therefore the I_{ref} is equal to

$$I_{ref} = \frac{K_n}{2}\left(\frac{W}{L}\right)_1 (V_{i1} - V_{s1} - V_t)^2 \tag{4.1}$$

Part 2: Current mirror

The current mirror consists of two CMOS transistors, M_3 and M_4, having equal threshold voltage V_t, but with different (W/L) ratios. M_3 is fed with the $I_{ref1} = mI_{ref}$ with m is constant. The output current I_b is taken at the drain of M_4, which must be operated in the saturation region. For M_3 we can write

$$I_{ref1} = \frac{K_n}{2}\left(\frac{W}{L}\right)_3 (V_{gs3} - V_t)^2 \tag{4.2}$$

Since M_4 is connected in parallel with M_3, it will have the same $V_{gs3} = V_{gs4}$[(1)]; thus

$$I_b = \frac{K_n}{2}\left(\frac{W}{L}\right)_4 (V_{gs3} - V_t)^2 \tag{4.3}$$

Equation (4.2) and (4.3) can be combined to obtain

$$I_b = mI_{ref}\frac{(W/L)_4}{(W/L)_3} \tag{4.4}$$

By substitute the Equation (4.1) into the (4.4), we could get

$$I_b = \frac{mK_n}{2}\left(\frac{W}{L}\right)_1\frac{(W/L)_4}{(W/L)_3}(V_{i1} - V_{s1} - V_t)^2 \tag{4.5}$$

[1]In the above calculations, in order to generate a close form solutions, we have ignored the small 100 Ω resistive connected to the source of M_3. Simulation results have concluded this resistor has very little affect on the output current.

Part 3: Gilbert quad pair

The schematic of the Gilbert quad pair is shown in Figure 4.4,

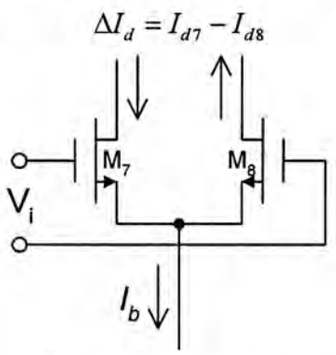


Figure 4.4: Schematic of the Gilbert quad pair

$$I_{d7} = \frac{K_n}{2}\left(\frac{W}{L}\right)_7(V_{G7} - V_{S7} - V_t)^2 \tag{4.6}$$

$$I_{d8} = \frac{K_n}{2}\left(\frac{W}{L}\right)_8(V_{G8} - V_{S8} - V_t)^2 \tag{4.7}$$

$$V_i = V_{G7} - V_{G8} \tag{4.8}$$

$$I_b = I_{d7} + I_{d8} \tag{4.9}$$

Solving this four equations and assume $\left(\frac{W}{L}\right)_7 = \left(\frac{W}{L}\right)_8$ and $V_{S7} = V_{S8}$, we could get

$$\Delta I_d = I_{d7} - I_{d8} = \frac{K_n}{2} V_i \sqrt{4\left(\frac{W}{L}\right)\frac{I_b}{K_n} - \left(\frac{W}{L}\right)^2 V_i^2} \tag{4.10}$$

where $I_b = \frac{mK_n}{2}\left(\frac{W}{L}\right)_1 \frac{(W/L)_4}{(W/L)_3}(V_{i1} - V_{s1} - V_t)^2$

A detailed mathematical derivation of the characteristic of the Gilbert quad pair could be found in Appendix A.

4.2.3 Small Signal Analysis

The new double balanced design has a symmetric structure, thus we only need to analysis half of the circuit shown in Figure 4.5.

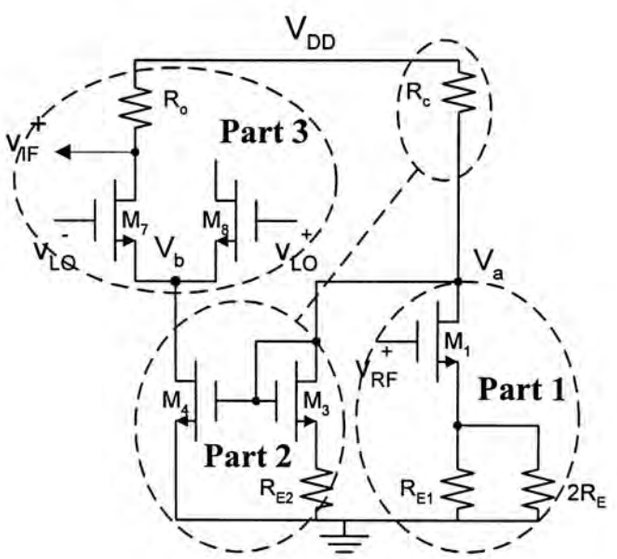


Figure 4.5: Half circuit of the current folded mirror mixer in a small signal analysis

We can divide the circuit into three separate parts for analysis as shown by the circuits in Figure 4.5. The first part is the common emitter with emitter resistance $2R_E$. The second part is the differential folded mirror and the third part is the Gilbert quad.

We use a source degenerations resistor R_E to increase linearity range of the mixer.

Moreover, the mixer is designed to operate with a small RF input signal and a relatively large LO signal. The conversion gain of the mixer is shown below:

Part 1: Common emitter with emitter resistance

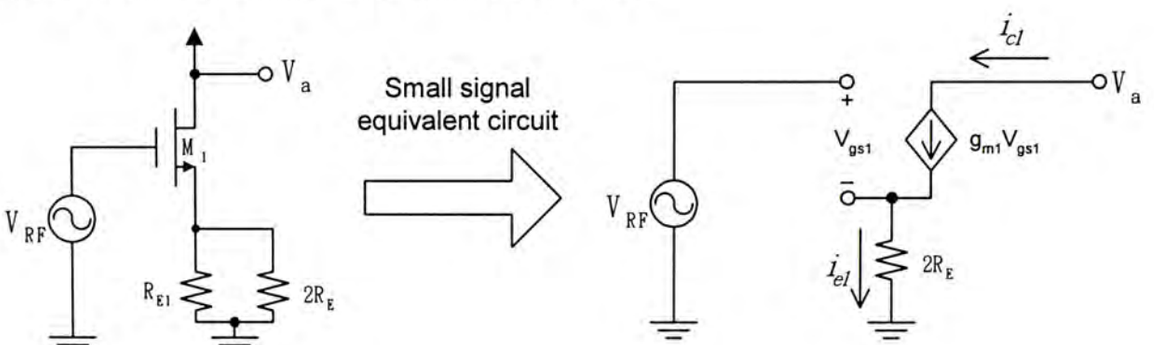


Figure 4.6: The small signal equivalent circuit of a common source amplifier with a source degeneration resistor

The current i_e:

$$i_{e1} = \frac{v_{RF} - v_{gs1}}{2R_E}$$

$$g_{m1}v_{gs1} = \frac{v_{RF} - v_{gs1}}{2R_E}$$

$$v_{RF} = v_{gs1}(2R_E g_{m1} + 1)$$

$$v_{gs1} = \frac{v_{RF}}{2R_E g_{m1} + 1} \qquad (4.11)$$

Therefore, the current i_{c1}:

$$i_{c1} = g_{m1} v_{gs1}$$

$$i_{c1} = \frac{v_{rf}}{2R_E + 1/g_{m1}} \tag{4.12}$$

Part 2: differential folded mirror

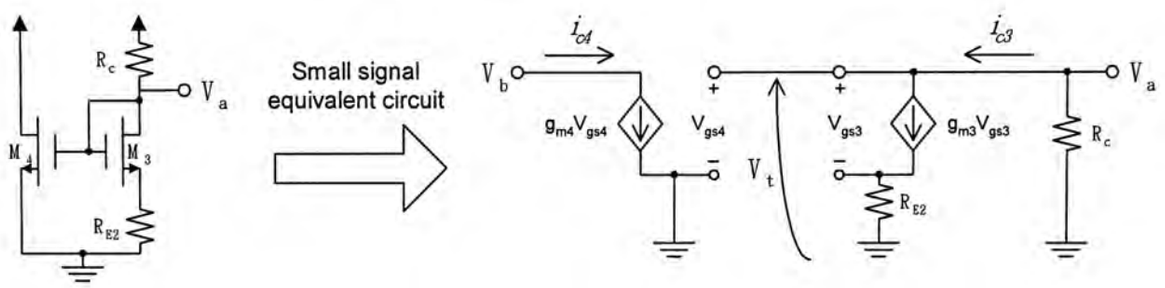


Figure 4.7: The small signal equivalent circuit of a differential folded mirror

The voltage V_t:

$$V_t = -i_{c3} R_c \tag{4.13}$$

$$V_t = v_{gs3} + g_{m3} v_{gs3} R_{E2}$$

$$v_{gs3} = \frac{-i_{c3} R_c}{1 + g_{m3} R_{E2}}$$

$$= \frac{-m i_{c1} R_c}{1 + g_{m3} R_{E2}} \tag{4.14}$$

where $i_{c3} = m i_{c1}$ and m is a constant

Therefore, the current i_{c4}:

$$i_{c4} = g_{m4} v_{gs4}$$

$$i_{c4} = g_{m4} V_t$$

by Equation (4.13) $$= -g_{m4} i_{c3} R_c = -g_{m4} g_{m3} v_{gs3} R_c$$

By Equation (4.14) $$= \frac{m g_{m3} g_{m4} R_c^2}{1 + g_{m3} R_{E2}} i_{c1} \tag{4.15}$$

Part 3: Gilbert quad

Since the transistors M_7 – M_{10} operate as a switch. Therefore, it is like to gate the input RF signal with a square wave.

Finally, the overall transfer function is:

$$v_{IF} = v_{IF}^{+} - v_{IF}^{-} = R_o(i_{c4} - i_{c6}) \times \text{square wave}$$
$$= 2R_o \frac{mg_{m3}g_{m4}R_c^2}{1+g_{m3}R_{E2}} \frac{v_{rf}}{1+2R_E g_{m1}} \times \frac{2}{\pi}$$

$$\frac{v_{IF}}{v_{RF}} = \frac{2}{\pi} \times \frac{mg_{m3}g_{m4}R_c^2}{1+g_{m3}R_{E2}} \times \frac{2R_o}{1+2R_E g_{m1}} \tag{4.16}$$

where the $2/\pi$ accounts for the conversion gain loss.

4.3 Current Mode Mixer

Although the current folded mirror mixer could operate at 1.5 V single voltage supply. Our goal is to design a mixer, which can operate at a single supply voltage at 1.2 V, because most portable telecommunication equipment is powered by a single 1.2 V battery.

We have modified the current folded mirror mixer into a current mode mixer [24] as shown in Figure 4.8.

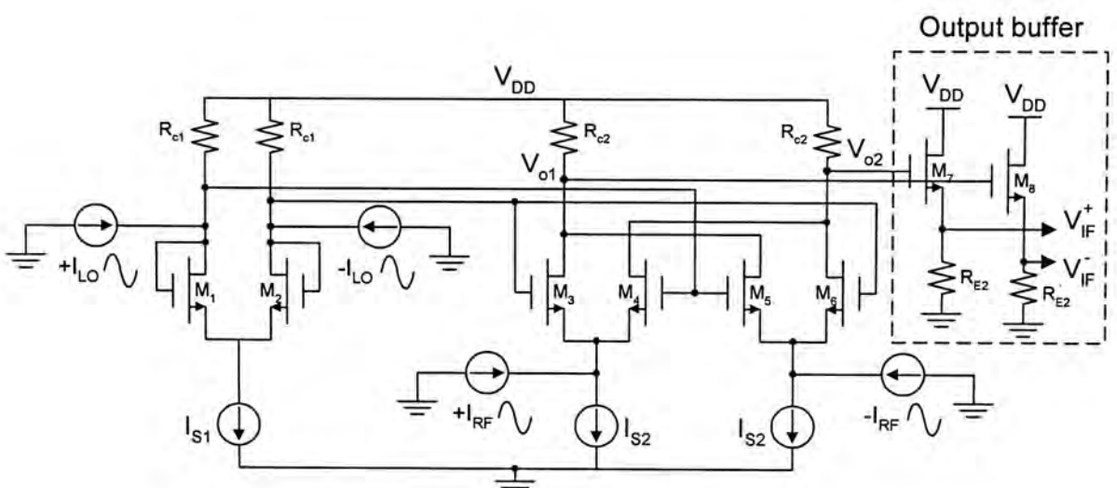


Figure 4.8: Schematic diagram of the current mode mixer

4.3.1 Operating Principle

The new design has eliminated the series connected transistors to reduce the supply voltage. Moreover, it uses current input instead of voltage input.

4.3.2 Large Signal Analysis

Transistors M_3 – M_6 are operated as a switch to generate a multiplications property using the non-linear characteristic of the transistors as shown in the equation (2.3). Therefore, only two of the four transistors (M_3 – M_6) are conducting at any time and we can consider the mixer as two identical pairs. The schematic of one of the differential pair is shown in Figure 4.9.

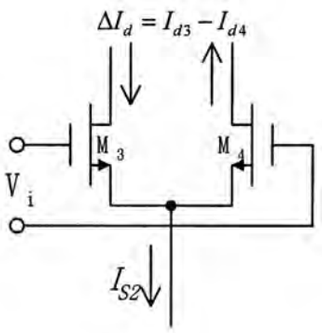


Figure 4.9: Schematic of the differential pair

$$I_{d3} = \frac{K_n}{2}\left(\frac{W}{L}\right)_3 (V_{G3} - V_{S3} - V_t)^2 \tag{4.17}$$

$$I_{d4} = \frac{K_n}{2}\left(\frac{W}{L}\right)_4 (V_{G4} - V_{S4} - V_t)^2 \tag{4.18}$$

$$V_i = V_{G3} - V_{G4} \tag{4.19}$$

$$I_{S2} = I_{d3} + I_{d4} \tag{4.20}$$

where I_{S2} is a constant current source. Solving this four equations and assume $\left(\frac{W}{L}\right)_3 = \left(\frac{W}{L}\right)_4$ and $V_{S3} = V_{S4}$, we could get

$$\Delta I_d = I_{d3} - I_{d4} = \frac{K_n}{2} V_i \sqrt{4\left(\frac{W}{L}\right)\frac{I_{S2}}{K_n} - \left(\frac{W}{L}\right)^2 V_i^2} \tag{4.21}$$

A detailed mathematical derivation of the characteristics of a differential pair could be found in Appendix A.

4.3.3 Small Signal Analysis

Based on the Figure 4.10, we could find the relationship between the differential output (I_1, I_2) and the two differential input (i_{x1}, i_{x2} and i_{y1}, i_{y2}). We can derive the relationship between the differential outputs current (I_1, I_2) and the two differential input currents (i_{x1}, i_{x2} and i_{y1}, i_{y2}) as shown in Figure 4.10.

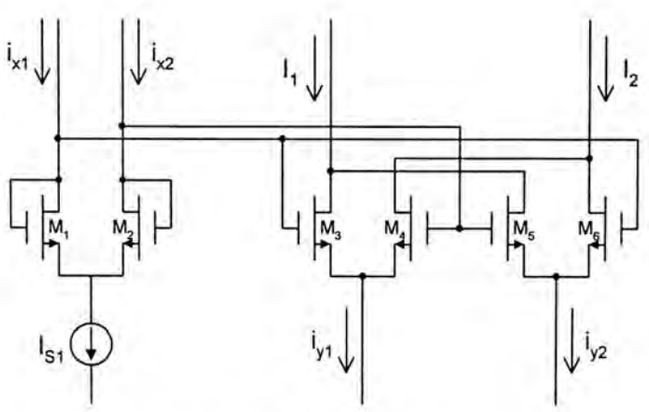


Figure 4.10: New parallel current mode mixer

The derivation step:

Consider the loop M_1-M_2-M_3-M_4 and M_1-M_2-M_5-M_6

$$\frac{i_{c1}}{i_{c2}} = \frac{i_{c3}}{i_{c4}} = \frac{i_{c6}}{i_{c5}} \tag{4.22}$$

Neglecting the base current, then equation (4.22) becomes

$$\frac{i_{x1}}{i_{x2}} = \frac{i_{c3}}{i_{c4}} = \frac{i_{c6}}{i_{c5}} \tag{4.23}$$

The differential output current (I_1-I_2) is equal to

$$I_1 - I_2 = (i_{c3} + i_{c5}) - (i_{c4} + i_{c6}) \tag{4.24}$$

For

$$\begin{cases} i_{y1} = i_{c3} + i_{c4} & (4.25) \\ i_{y2} = i_{c5} + i_{c6} & (4.26) \end{cases}$$

Substitute equations (4.25) and (4.26) into (4.24), we could get

$$I_1 - I_2 = (i_{y1} + i_{y2}) - 2(i_{c4} + i_{c6}) \tag{4.27}$$

Solving i_{c4} and i_{c6} in terms of i_{x1}, i_{x2}, i_{y1} and i_{y2}.

From Equation (4.25), $i_{c3} = i_{y1} - i_{c4}$

$$i_{c4} = \frac{i_{x2}}{i_{x1}}(i_{y1} - i_{c4})$$

$$i_{c4} = \frac{i_{x2} i_{y1}}{i_{x1} + i_{x2}} \tag{4.28}$$

By similar method,

$$i_{c6} = \frac{i_{x1} i_{y2}}{i_{x1} + i_{x2}} \tag{4.29}$$

So,

$$I_1 - I_2 = (i_{y1} + i_{y2}) - 2\left(\frac{i_{x2}i_{y1} + i_{x1}i_{y2}}{i_{x1} + i_{x2}}\right)$$
$$= \frac{(i_{x1} - i_{x2})(i_{y1} - i_{y2})}{i_{x1} + i_{x2}}$$
$$= \frac{I_x \times I_y}{I_{S1}} \qquad (4.30)$$

where I_x (Differential I_x current) = $(i_{x1} - i_{x2})$

I_y (Differential I_y current) = $(i_{y1} - i_{y2})$

$I_{S1} = (i_{x1} + i_{x2})$

From the result of the Equation (4.30), it could be seen that the differential output current, $(I_1 - I_2)$, is equal to the multiplication of the two differential input current (I_x and I_y).

4.3.4 V-I Converter

The new current mode mixer requires RF and LO current inputs. Therefore, we need to design a V-I converter. In this project, we use a V-I converter shown in Figure 4.11 [[25], [26]].

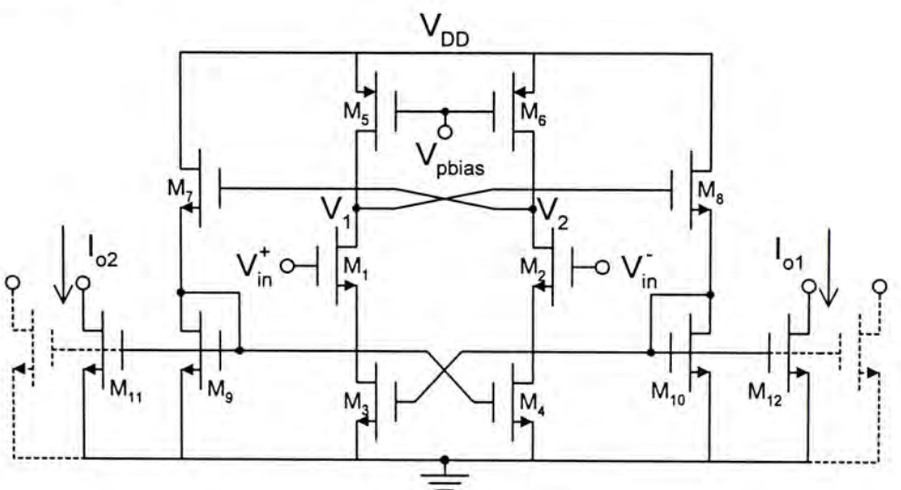


Figure 4.11: Schematic design of the V-I converter

In order to wider the differential-input voltage swing at low voltage supply, four transistors (M_3 - M_6) are stacked with the core transistors (M_1, M_2) and biased in triode region. Then V_{ds} of M_3, M_4 and M_5, M_6 are biased very close to V_{dd} and ground (several tens of mV) respectively. By setting bias input voltage properly, M_1, M_2 can operate in saturation region with $V_{ds,M1,M2} \geq V_{bias} \pm V_{voltage\text{-}swing}$, then the differential-input voltage could be up to $V_{voltage\text{-}swing}$. Where the feedback loop (M_7 - M_{10}) is used to bias the gates of M3, M4 to maintain triode operation. V_{in}^+, V_{in}^- would deliver V_1, V_2 to generate a differential-input signal of M_7, M_8 for the differential-currents. By mirroring this differential-currents through M_9 – M_{12} and differential output current could obtain.

4.3.4.1 Equation Analysis

We have mentioned in the previous section that M_1, M_2 are in saturation mode and M_5, M_6 are in triode mode. Therefore, we could define the following equation:

$$I_{M_1} - I_{M_2} = K_n\left(V_{CM} - V_{tn}\right)V_d = K_p\left(V_{pbias} - V_{tp}\right)\left(V_2 - V_1\right) \tag{4.31}$$

The left-hand side of Equation (4.31) is derived from the saturation mode of M_1, M_2, and the right-hand side of Equation (4.31) from triode mode of M_5, M_6. Thus,

$$\Rightarrow \quad V_2 - V_1 = \frac{K_n\left(V_{CM} - V_{tn}\right)}{K_p\left(V_{pbias} - V_{tp}\right)}V_d \tag{4.32}$$

where M_7, M_8 are biased at saturation mode. So

$$I_{out} = I_{M_7} - I_{M_8} = \frac{K_n K_n^{'}\left(V_{CM} - V_{tn}\right)\left(V_1 + V_2 - 2V_{tn}\right)}{K_p\left(V_{pbias} - V_{tp}\right)}V_d \tag{4.33}$$

where $V_d = V_{in}^+ - V_{in}^-$ and $V_{CM} = \frac{V_{in}^+ + V_{in}^-}{2}$.

From Equation (4.33), we can observe that the differential output current is a function of the differential input voltage V_d. Although the nonlinearity may be increased as the supply voltage is reduced, which could be compensated by increasing the aspect ratios of M_5, M_6. The detail derivation could be found in Appendix B.

4.4 Second Order Effects

In order to obtain a meaningful close-form solution, the simplified model is used in the qualitative analysis in Section 4.2.2 and Section 4.3.2. However, the device mismatch and body effect affects have not been discussed. The following section analysis the problem caused by device mismatch and body effect [27].

4.4.1 Device Mismatch

Device mismatch is a main source of error, which usually creates output offset voltage and harmonic distortions. It can be shown that the DC offset and the second order harmonic distortion is a function of the mismatch aspect ratio Δ(W/L) and the loading resistor ΔR_o.

$$\Delta V_{IF} = \frac{K_n}{2} V_i (R_o + \Delta R_o) \sqrt{4\left(\frac{W}{L} + \Delta\frac{W}{L}\right)\frac{I_{base}}{K_n} - \left(\frac{W}{L} + \Delta\frac{W}{L}\right)^2 V_i^2} \qquad (4.34)$$

Fortunately, the layout drawing could minimize this source of mismatch as much as possible.

4.4.2 Body Effect

In the above analysis, the effect of the substrate (or body) bias has been neglected for easier calculation. However, in N-well CMOS technology, NMOS transistors are usually experiencing the body effect, which result in the variation of the threshold voltage (V_t). To include this effect, the V_t equation is changed to:

$$V_t = V_{to} + \gamma\left[\sqrt{2\phi_f + V_{SB}} - \sqrt{2\phi_f}\right] \tag{4.35}$$

where V_{to} is the threshold voltage for $V_{SB} = 0$; γ is a process parameter; ϕ_f is a physical parameter.

4.5 Single-ended to Differential-ended converter

In usual case, in order to reduce the noise figure and power consumption, a single-balanced mixer would be used in the RF receiver. However, as mentioned in Section 2.8, in order to reduce the effect of the LO signal at the IF output port, the mixer would be implemented in the double balanced structure instead. Moreover, a double balanced design gives a better isolation between the LO and IF. As a result, a single-ended to differential-ended converter is needed to place before the mixer input port (Figure 4.12).

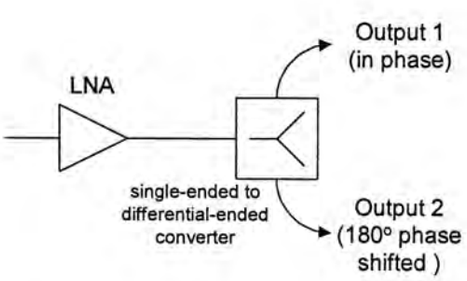


Figure 4.12: The function of the single-ended to differential-ended converter

Figure 4.13 shows the single-ended to differential-ended converter used in this project, which is consisted of a common source amplifier and a common drain amplifier pairs.

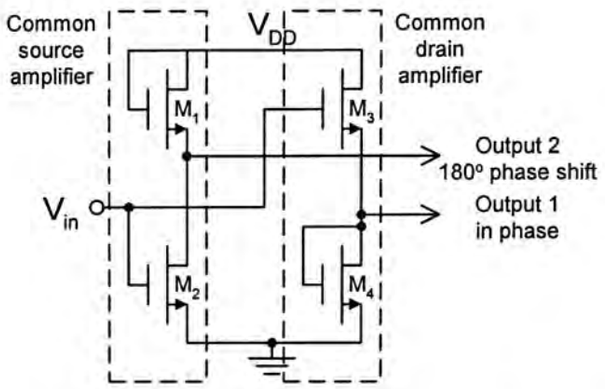


Figure 4.13: Schematic of the single-ended to differential-ended converter

The common source amplifier generates an output with 180° phase shift, while the common drain amplifier generate an output with no phase shift.

4.6 Output Buffer Stage

For experimental characterization purposes, the mixer core output signal has been buffered by means of an on-chip common drain amplifier (source follower), as shown in Figure 4.1 and Figure 4.8, to drive the instrument 50 Ω input impedance. Because of this, the conversion gain and third order intermodulation (IM3) measured on the spectrum analyzer are reduced with respect to the corresponding values of the core output. Therefore, we need to measure the conversion loss and subtract it from the total measured conversion gain.

4.7 Noise Theory

The major function of the mixer is frequency translation. During translation not only the narrow-band input signal is translated, but also the wide-band noise. As illustrate in Figure 4.14, the portion at $\omega_{LO} \pm \omega_{IF}$ are downconverted to ω_{IF} together. Thus, the resulting noise power spectral density is about twice of the original one assuming noise at different frequencies is not correlated [28].

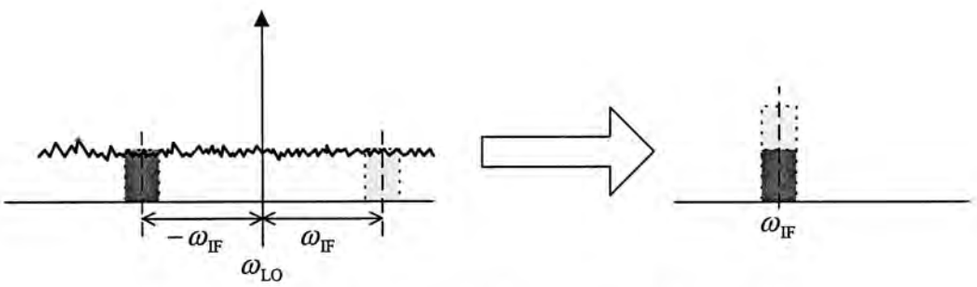


Figure 4.14: The concept of noise alias in mixing

If a square wave is employed at the LO, the situation is more complicated. As shown in Figure 4.15, each harmonic component of LO would downconvert a particular band of white noise to the IF with different conversion gain.

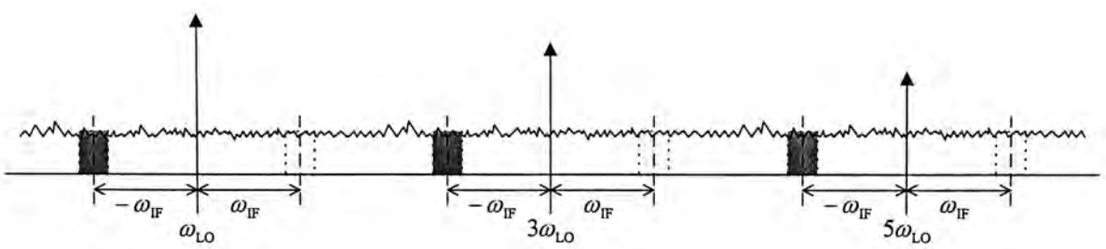


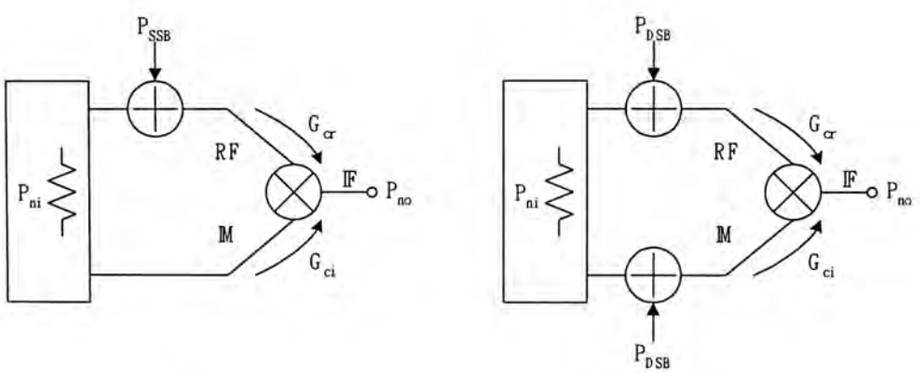
Figure 4.15: Noise contributions from the harmonics of LO

4.7.1 SSB and DSB Noise Figure

Noise figure is defined as the signal-to-noise (SNR) at the input (RF) port divided by the SNR at the output (IF) port. Figure 4.14 show that not only the desired RF signal with noise is downconverted, but also the image signal with noise. Therefore, it is important to differentiate the noise measurement into a single-sideband (SSB) and a double-sideband (DSB) noise figures.

In some systems, input signals at both RF and image frequencies are informative and used simultaneously. Then the SNR is determined by the total signal power in both sidebands and defined as Double-SideBand (DSB) noise figure. On the other hand, it is meaningful to refer the mixer noise to only one sideband of the system, which only uses signal at one of the two sidebands. This is defined as Single-SideBand (SSB) noise figure.

The noise models for SSB and DSB noise figure calculations are shown in Figure 4.16. For simplicity, the LO is omitted.



(a) (b)

Figure 4.16: Noise models for the mixer NF calculations,

(a) SSB NF and (b) DSB NF

In the SSB case, the SSB input-referred noise power, P_{SSB}, is given by,

$$P_{no} = P_{ni}(G_{cr} + G_{ci}) + P_{SSB}G_{cr}$$
$$P_{SSB} = \frac{P_{no} - P_{ni}(G_{cr} + G_{ci})}{G_{cr}} \quad (4.36)$$

where P_{no} is the output noise power, P_{ni} is the input noise power, and G_{cr} and G_{ci} are the conversion gains at the RF and the image frequency respectively. In the SSB case, only RF input noise is considered, thus the SSB noise figure is given by the ratio of output noise power to the noise power of one input sideband;

$$NF_{SSB} = \frac{P_{SSB}G_{cr} + P_{ni}G_{ci}}{P_{ni}G_{cr}} + 1 \quad (4.37)$$

In the DSB, the input noise comes from both sidebands equally. Therefore,

$$P_{no} = P_{ni}(G_{cr} + G_{ci}) + P_{DSB}(G_{cr} + G_{ci})$$
$$P_{DSB} = \frac{P_{no} - P_{ni}(G_{cr} + G_{ci})}{G_{cr} + G_{ci}} \quad (4.38)$$

and the DSB noise figure becomes,

$$NF_{DSB} = \frac{P_{DSB}}{P_{ni}} + 1 \quad (4.39)$$

If the conversion gain of the RF and the image frequency are same, that is, $G_{cr} = G_{ci}$, the NF_{SSB} will be 3 dB higher than the NF_{DSB}.

4.7.2 Noise Figure

Actually, it is hard to calculate noise figure by hand due to the time variance and frequency translation in mixers. Moreover, the translation of the RF noise components by switching stage of the Gilbert quad pair will prohibit the direct use of small-signal ac and noise analysis in simulator. Therefore, we will only use measured noise figure results.

Chapter 5

Simulation Results

5.1 Introduction

Simulation is an important procedure in IC design. We use simulation results to guide us through the design. Simulation can provide fast and accurate performance of the circuit.

In this project, we use SpectreRF© simulator, which can simulate steady state and small signal analyses of circuits designed for radio frequency applications.

The beginning of this chapter gives the simulation results of the two proposed mixers in different criteria as mention in Chapter 2. Then the peripheral part, such as single-ended to differential-ended converter, output buffer stage and V-I converter simulation results are discussed.

5.2 Current Folded Mirror Mixer

Figure 5.1 shows the W/L ratio used in each of the CMOS transistor. ***A single 1.5 V supply voltage*** is applied to the mixer. The mixer downconverts a 900 MHz RF signal to a 10 MHz IF signal.

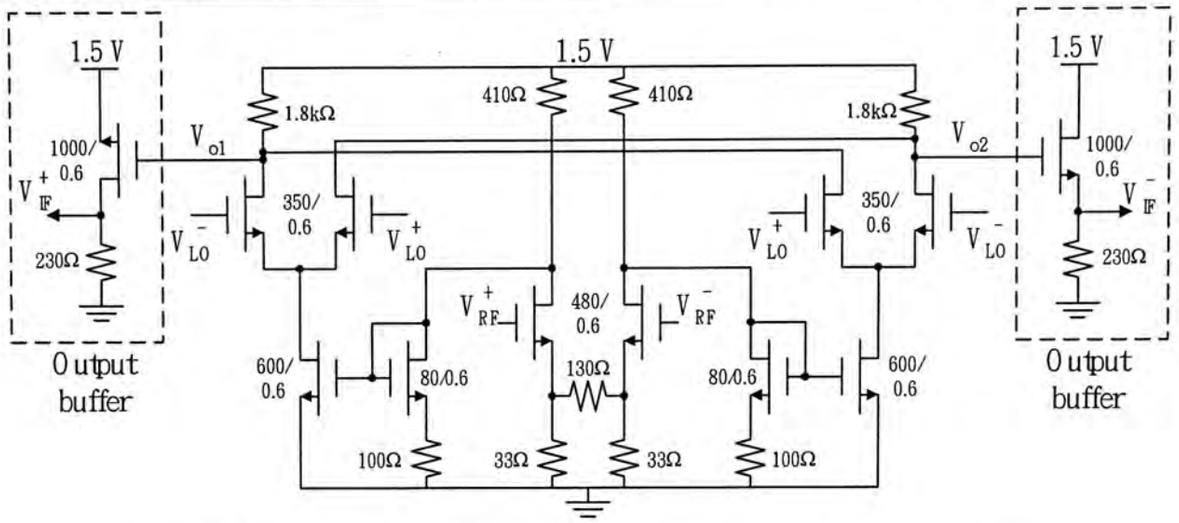


Figure 5.1: Electrical parameter used in current folded mirror mixer

5.2.1 Conversion Gain

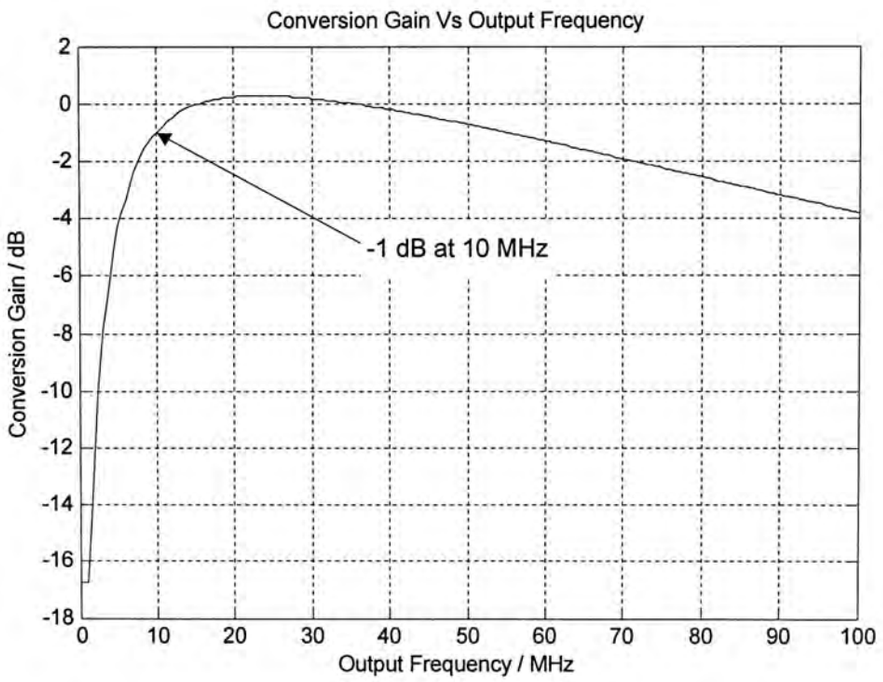


Figure 5.2: The simulated conversion gain against output frequency

The conversion gain is increasing as a function of the output frequency. Where the gain is equal to –1 dB at 10 MHz (the designed intermediate frequency). Afterwards, the conversion gain is dropping down.

5.2.2 Linearity

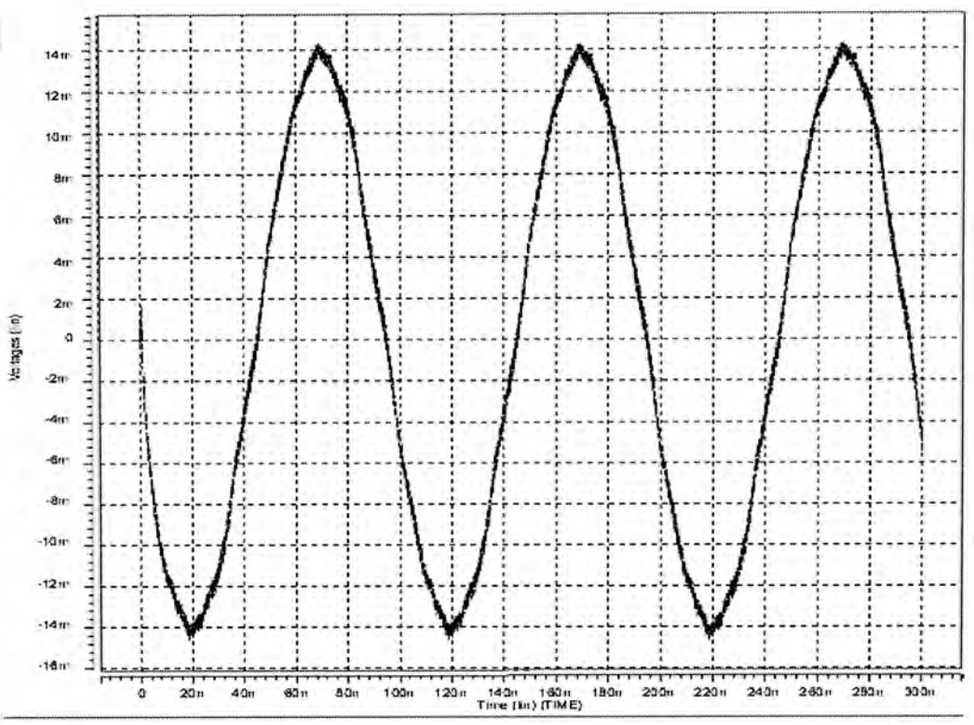
In this simulation, which will focus on two linearity terms: (1) 1-dB compression point, and (2) Third order intercept point (IP3). These measurements are widely used standard to measure the linearity of a tested circuit.

For 1-dB compression point simulation, a 900 MHz RF signal is applied to the RF input. Then, the corresponding output power at the IF signal (10 MHz) is measured and plotted on the graph as shown in Figure 5.5.

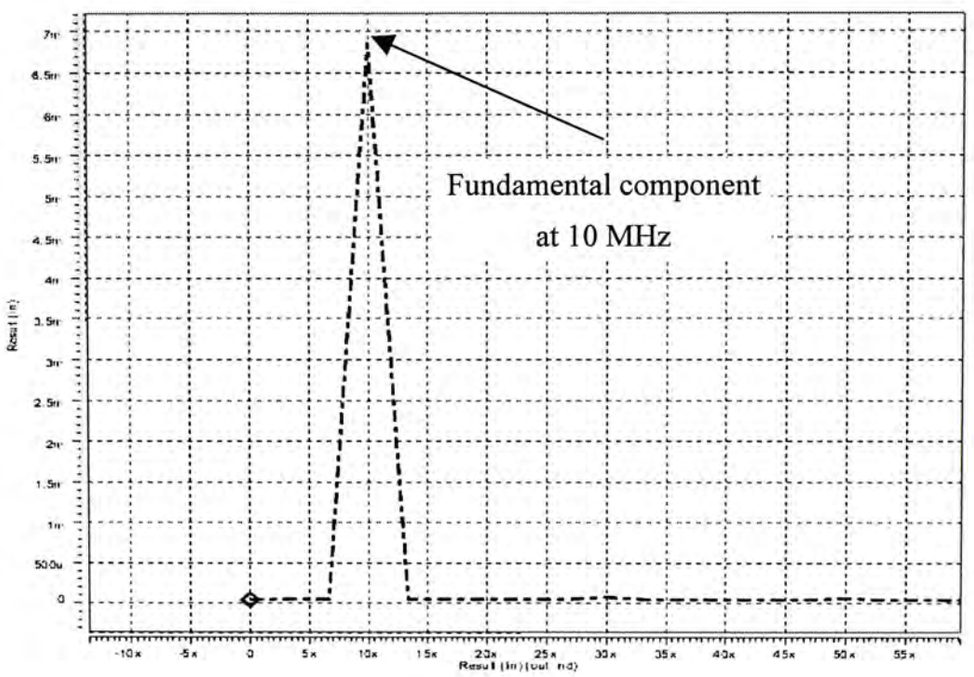
For IP3 simulation, input two tones RF test signals of very closed RF frequencies (900 MHz and 901 MHz) are applied. The corresponding third-order intermodulation products are measured at 8 MHz and 11 MHz respectively and plotted on the graph as shown in Figure 5.5.

At the same time, the LO signal is set at 910 MHz in both simulation.

Figure 5.3 and Figure 5.4 shown the transient and frequency response of the output signal with a pure sinusoid one tone RF input signal and two tones RF input signals respectively.

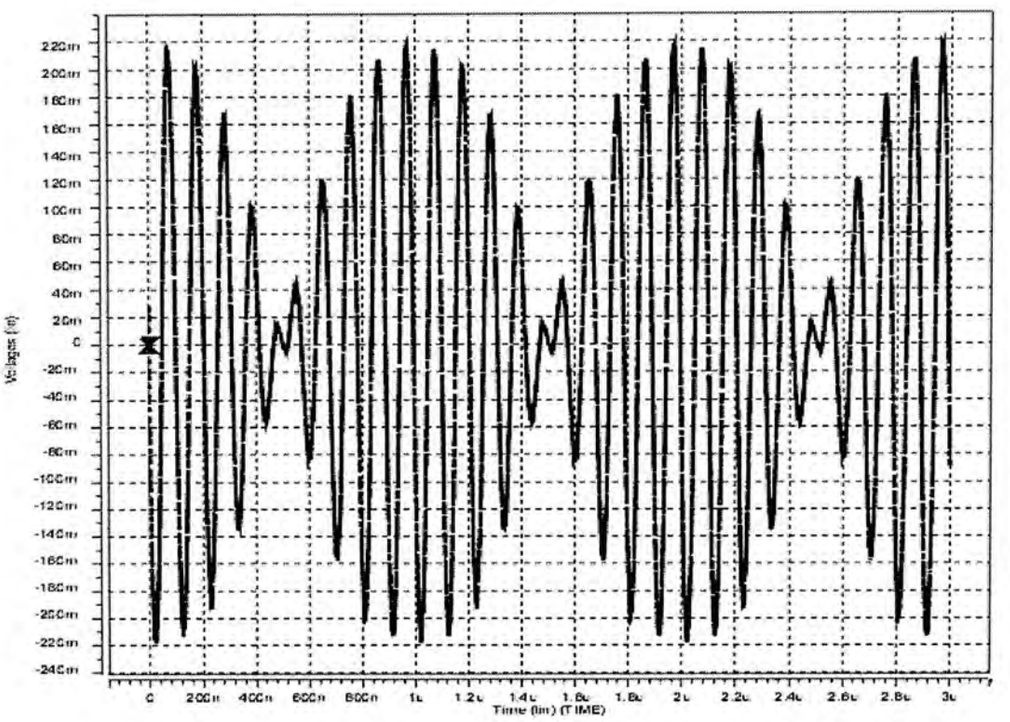


(a)

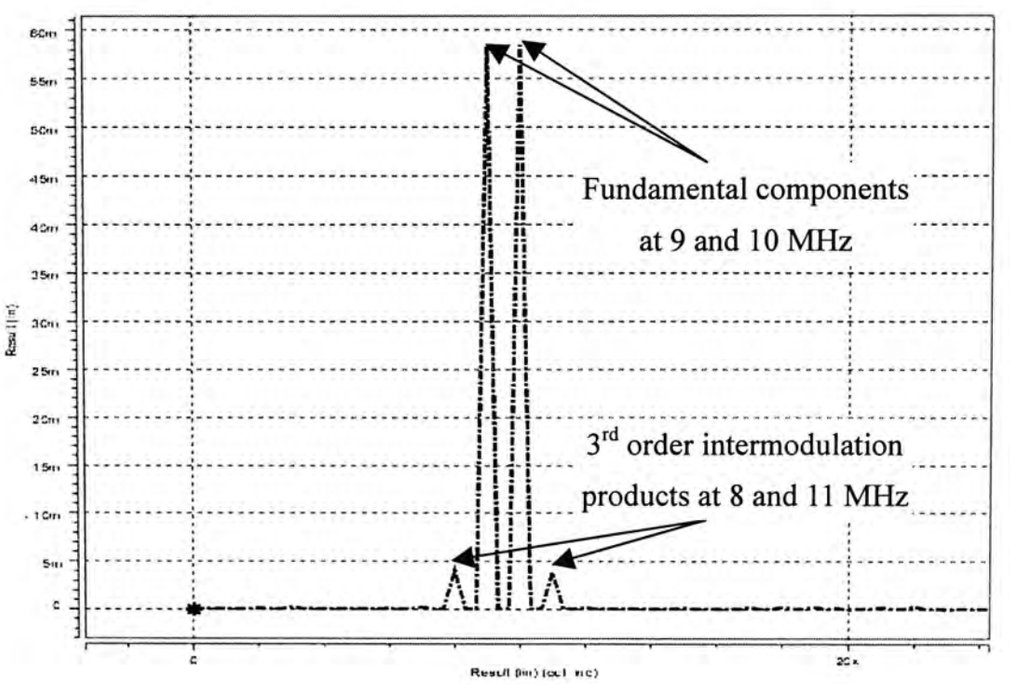


(b)

Figure 5.3: (a) The transient response and (b) the frequency response of the output signal with a pure sinusoid one tone input RF signal



(a)



(b)

Figure 5.4: (a) The transient response and (b) the frequency response of the output signal with two tones input RF signal

5.2.2.1 1-dB Compression Point and IIP3

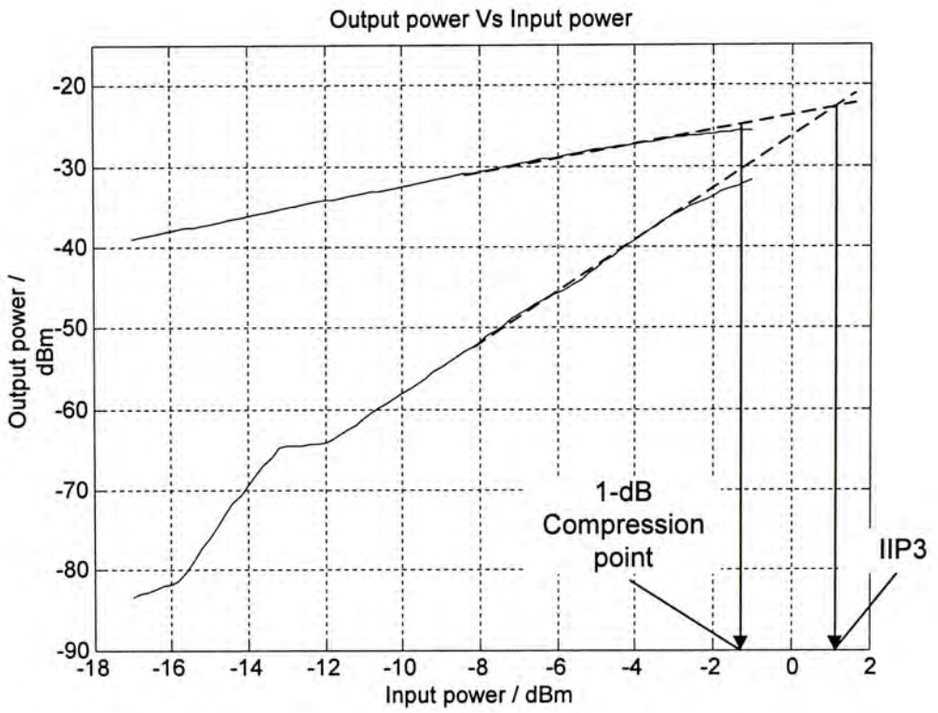
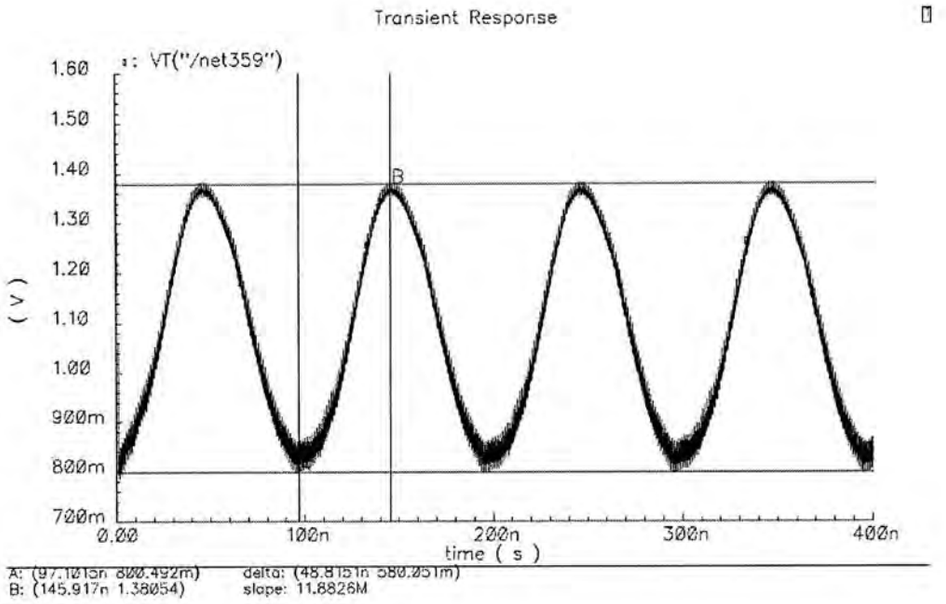


Figure 5.5: The simulated 1-dB compression point and IIP3 of the downconversion mixer

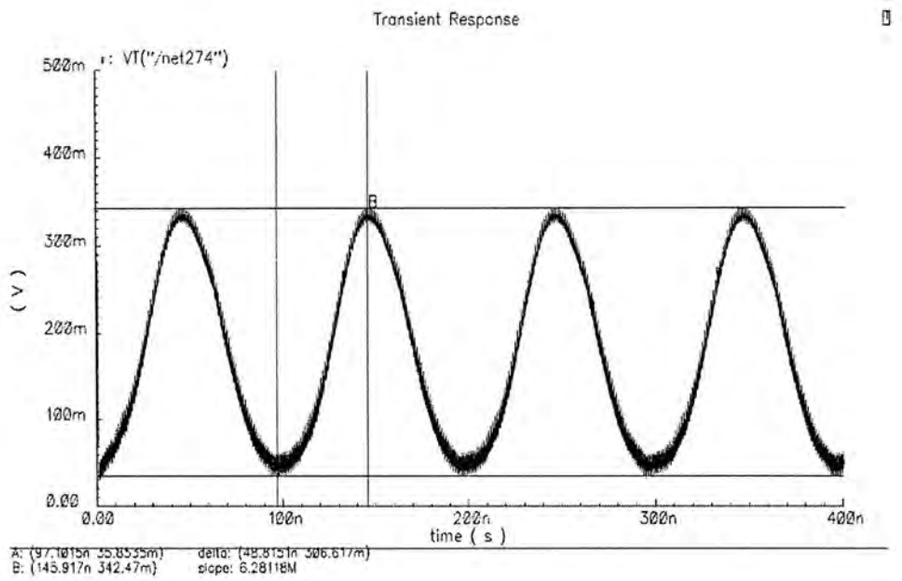
The simulation result shown that the 1-dB compression point and IIP3 equal to –1.2 dBm and 1.1 dBm respectively.

5.2.3 Output Buffer Stage

As mention in Section 4.6, although the output buffer stage (source follower) has conversion loss, it must be needed for experimental measurement. The transient response of the input and output signal of the output buffer are shown in Figure 5.6. The simulated conversion loss is about 5.56 dB. The conversion gain shown in Section 5.2.1 has cancelled out of this loss.



(a)



(b)

Figure 5.6: (a) The input and (b) the output transient response of the output buffer stage

5.3 Current Mode Mixer

The schematic diagram of a 900 MHz to 10 MHz current mode downconverter with all the transistor W/L ratio is shown in Figure 5.7 ***The supply voltage is a single 1.2 V.***

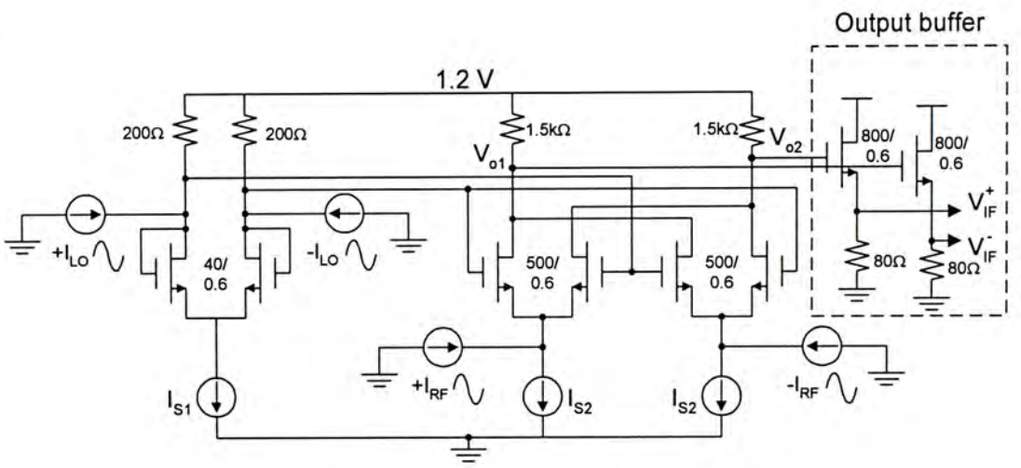


Figure 5.7: Electrical parameter used in current mode mixer

5.3.1 Conversion Gain

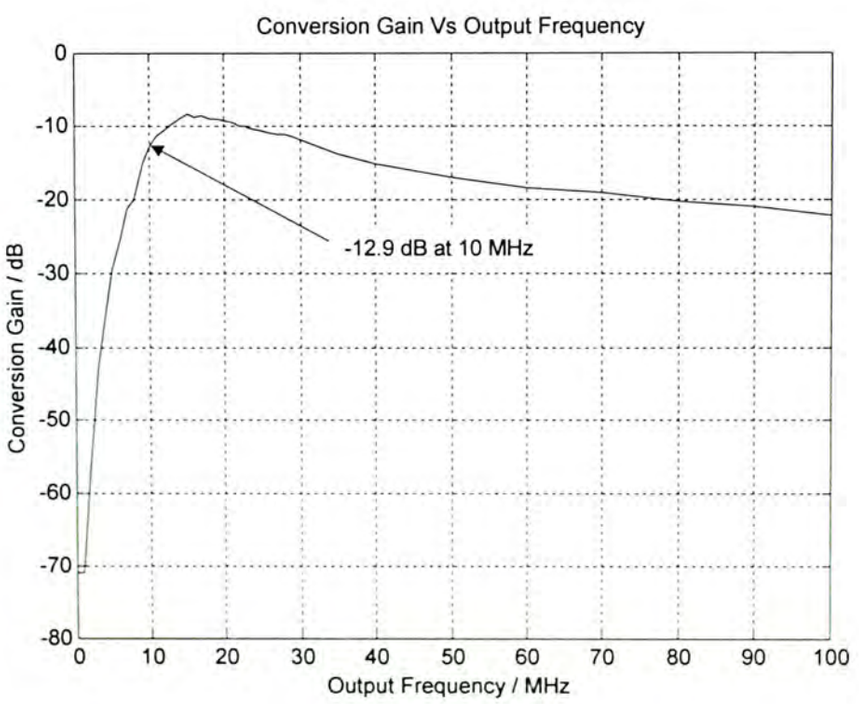


Figure 5.8: The simulated conversion gain against output frequency

The conversion gain is equal to –12.9 dB at 10 MHz (the designed intermediate frequency). Afterwards, the conversion gain is dropping down.

5.3.2 Linearity

The simulation procedure is same as mention in Section 5.2.2, we only focus on two linearity terms: (1) d-dB compression point, and (2) Third order intercept point.

5.3.2.1 1-dB Compression Point and IIP3

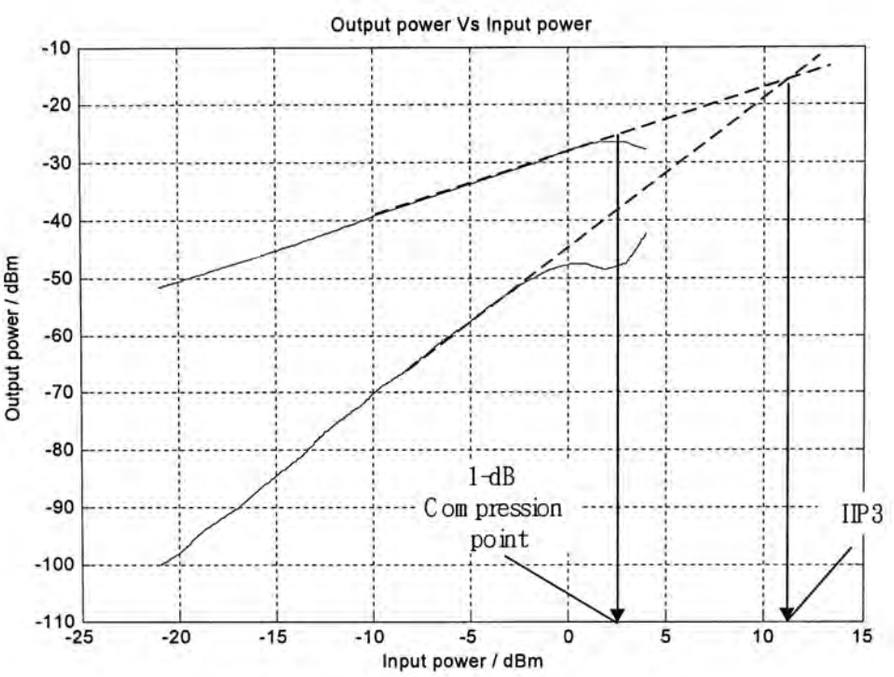
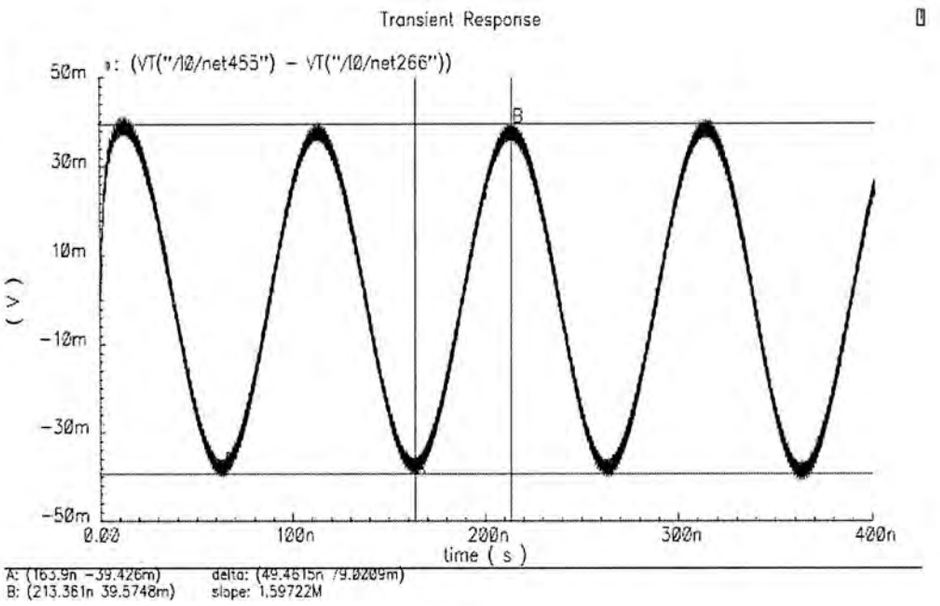


Figure 5.9: The simulated 1-dB compression point and IIP3 of the downconversion mixer

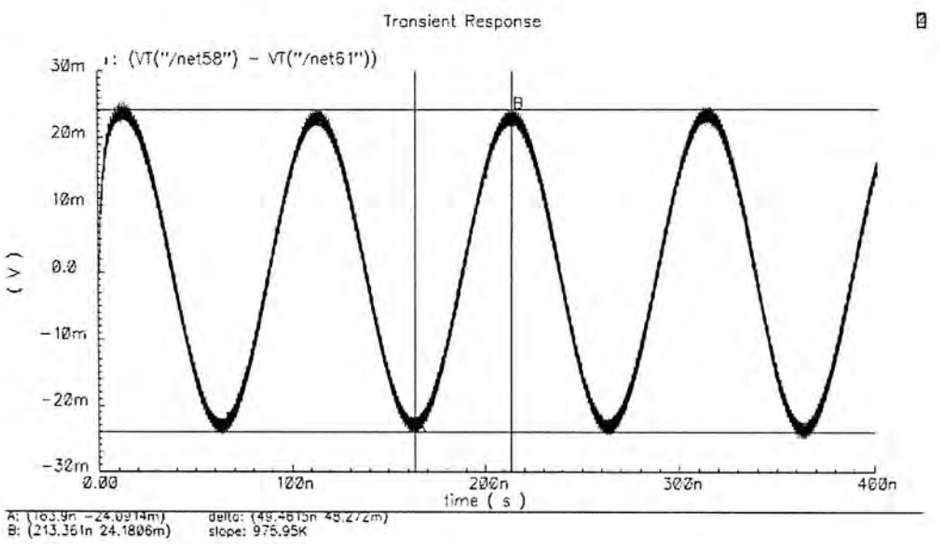
The simulation result shown the 1-dB compression point and IIP3 equal to 3 dBm and 11.5 dBm respectively.

5.3.3 Output Buffer Stage

The transient response of the output buffer is shown in Figure 5.10. From the marker in the two graphs, we can calculate the conversion loss and it is about 4.3 dB. The conversion gain shown in Section 5.3.1 has cancelled out of this loss.



(a)



(b)

Figure 5.10: (a) The input and (b) the output transient response of the output buffer stage

5.3.4 V-I Converter

Since the current mode mixer requires current inputs. Therefore, it is needed to have a V-I converter. The electrical parameter used in the V-I converter is shown in Figure 5.11.

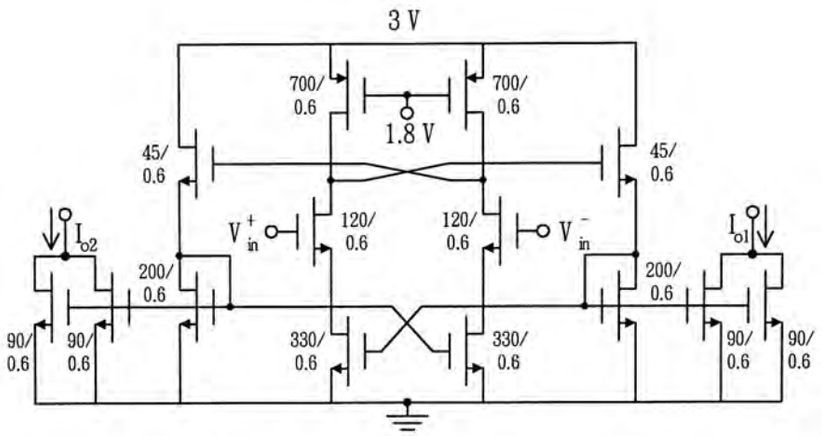


Figure 5.11: Electrical parameter used in V-I converter

V-I converter should have a high-linearity and a low signal distortion. Figure 5.12 shows the simulation result.

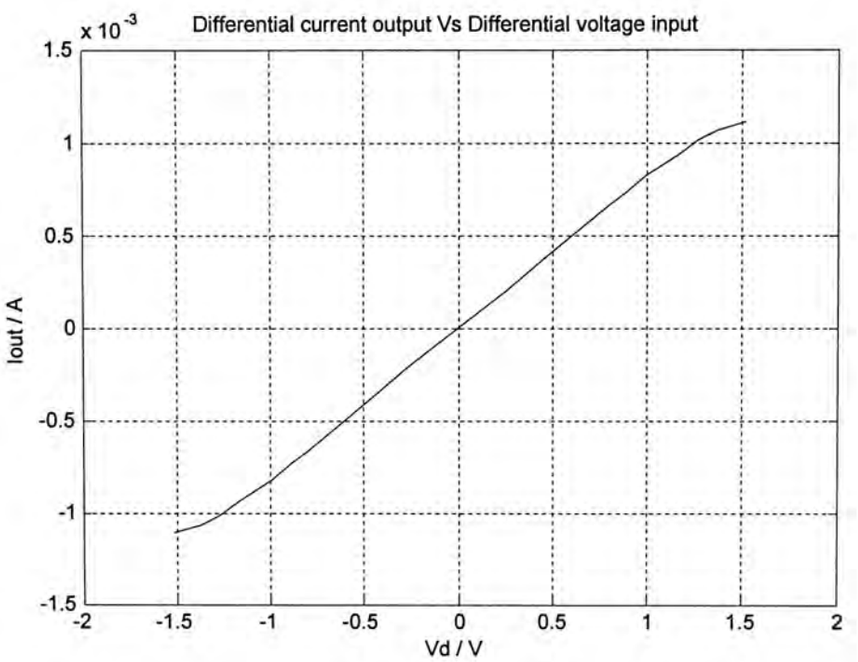


Figure 5.12: The simulated differential current output against differential voltage input

The simulation result of Figure 5.12 indicates the V-I converter has a high linearity between input and output signals.

5.4 Single-ended to Differential-ended Converter

As the previous two proposed mixers are double-balanced, a single-ended to differential-ended converter is needed. The electrical parameter used is shown in Figure 5.13. The simulation results are shown in Figure 5.14

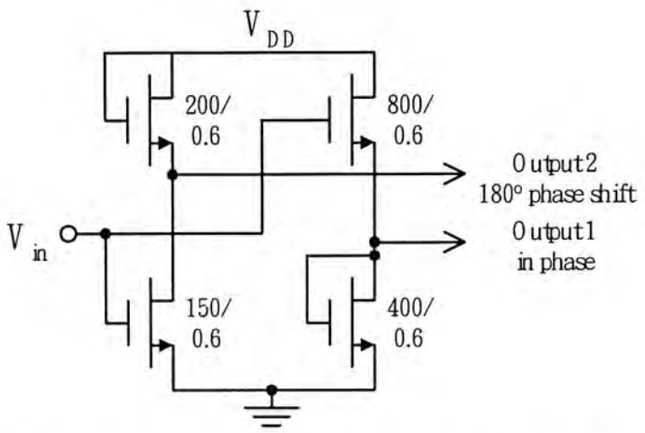
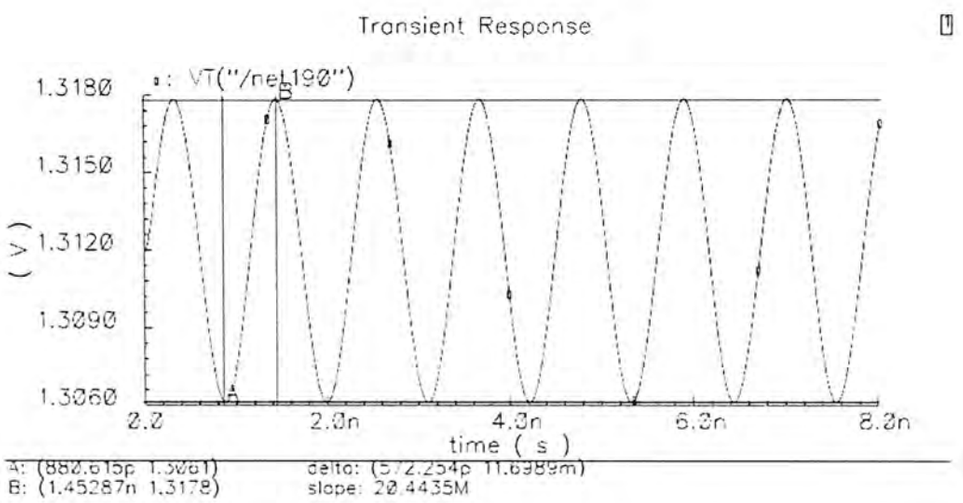
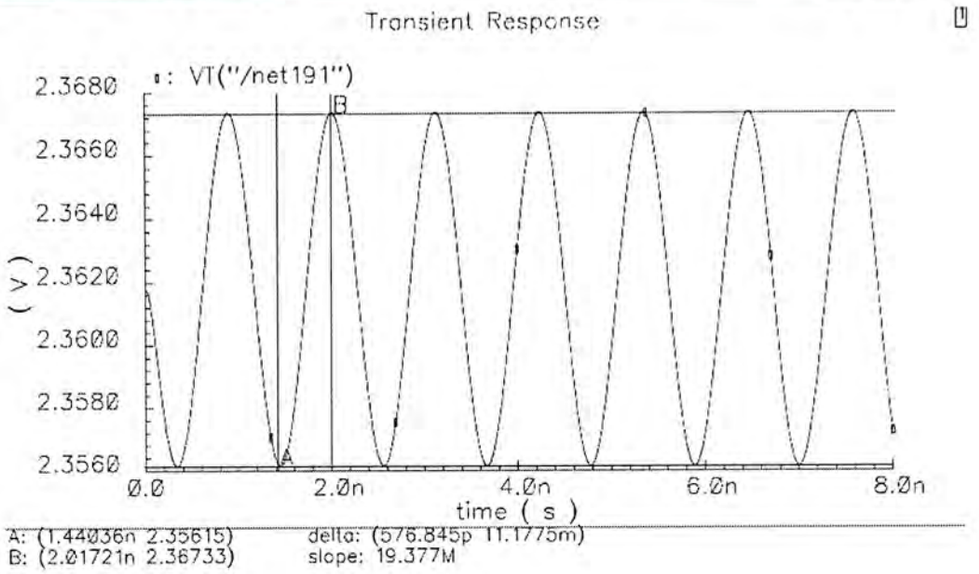


Figure 5.13: Electrical parameter used in single-ended to differential-ended converter



(a)



(b)

Figure 5.14: The transient response of the two output signals of the single-ended to differential-ended converter (a) output1, (b) output2

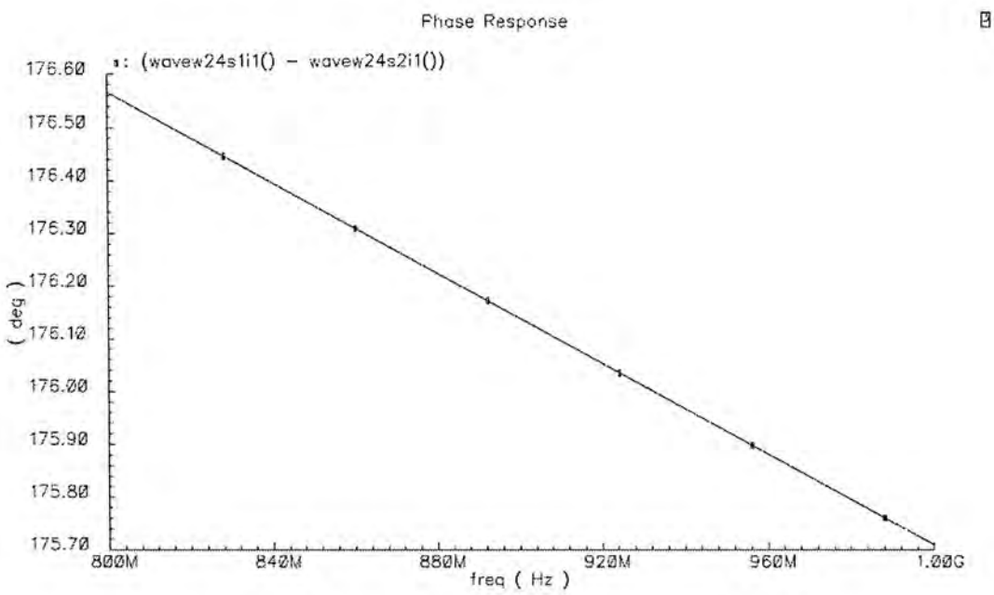


Figure 5.15:The phase difference of the two outputs

From the simulation result, it can be realized that the phase difference between two outputs is within 1-degree phase error between 800 MHz and 1 GHz and the amplitude difference between the two outputs is within 0.5m V.

Chapter 6

Layout Consideration

6.1 Introduction

Layout is the final design step in IC design, which transforms schematic design into physical representation. The performance of an RF circuits is very sensitive to the layout technique.

In this chapter, we will present the layout technique of transistors, resistors, capacitors, substrate tap and pad. The fabrication process used in this project is **AMS® 0.6 μm CMOS**.

6.2 CMOS transistor Layout

For analog applications, the aspect ratio (W/L) of transistors is much wider than transistors in digital circuits; therefore, it is necessary to design wide structures. However, as the aspect ratio of a transistor is very large, the resulting parasitic capacitor and resistor become very large. Which will degrade the performance of the circuit. In this case, it is good idea to lay out using multiple-gate fingers similar to the layout shown in Figure 6.1.

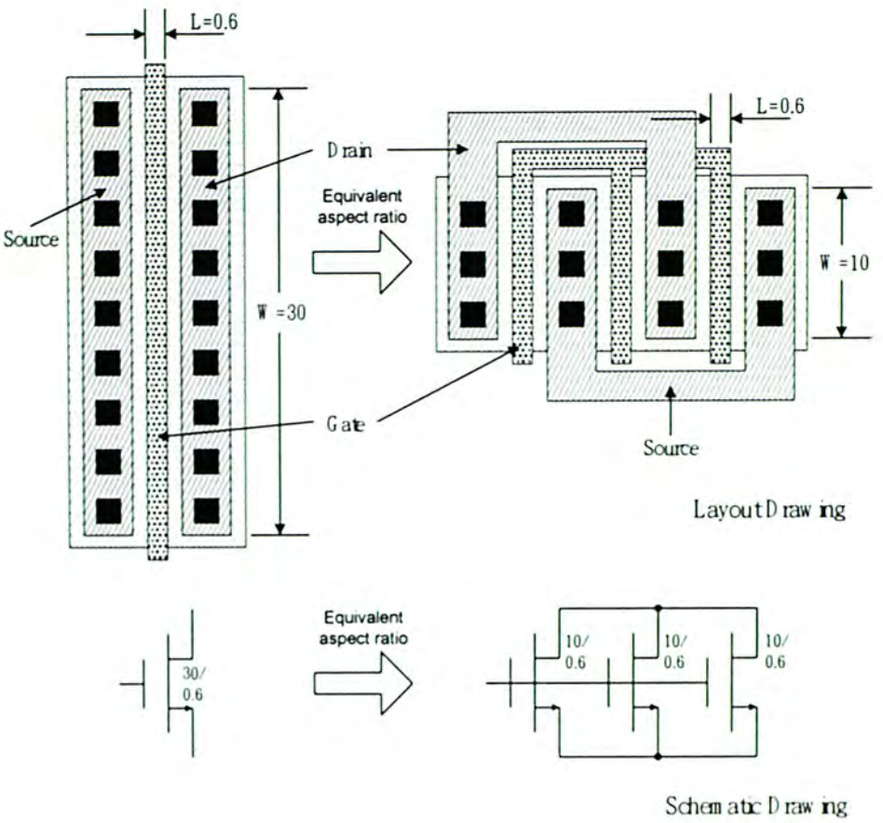


Figure 6.1: (a) One transistor in large aspect ratio,
(b) Split into 3 parallel parts connected it in multiple-gate fingers

The transistor layout in Figure 6.1(b) with number of elements, n, n=3 has a shape better than the one in Figure 6.1(a). This layout has the advantage that the parasitic capacitance is reduced. For a single transistor, the parasitic capacitances C_{sb} (source-bulk) and C_{db} (drain-bulk) are proportional to the width (W) of the transistor. For split transistors, C_{sb} and C_{db} are reduced by a factor of $n+1/2n$ if n is odd, however, if n is even C_{sb} is reduced by 1/2 while C_{db} is reduced by $n+2/2n$. This parasitic reduction is quite important for high-speed applications.

Moreover, the practice of splitting a transistor into the parallel connection is

also useful for improving the matching between elements. A major source of transistor mismatches is due to gradients that exist in the fabrication process. To minimize the gradient effect, two transistors that must be matched to each other should be placed very close to each other. Therefore, the use of multiple gate finger arrangements allow us to place matched transistors close to each other.

6.3 Resistor Layout

Integrated resistors can be realized using a wide variety of different conductors. For the **AMS®** fabrication process, polysilicon layer is used for resistor. The typical resistivity of the polysilicon layer used is 33 Ω/□. In order to obtain medium-sized resistors, one must use a serpentine layout similar to that shown in Figure 6.2.

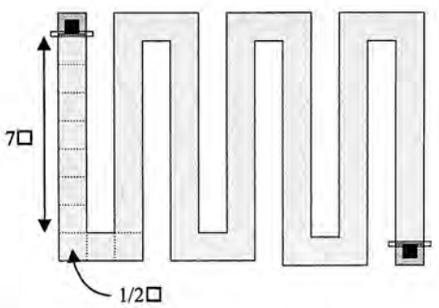
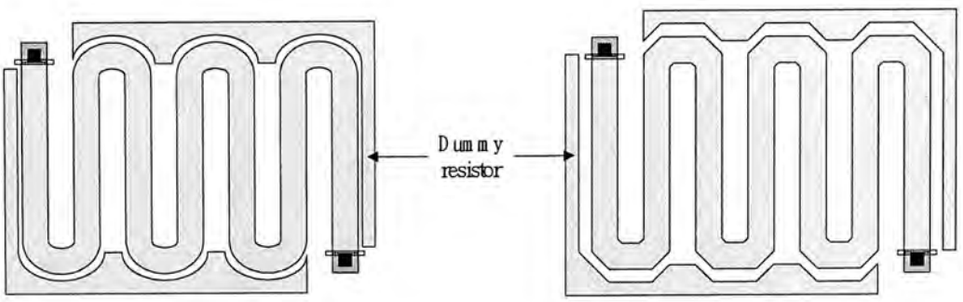


Figure 6.2: A typical layout for an integrated resistor

However, the layout structure in Figure 6.2 could not give a precise resistance. Since there is more active etching at the edges of the corner, which makes them rounded, and the shape is poorly controlled. For precise applications, it is a good practice to design rounded (Figure 6.3 (a)) (not available in the **AMS® 0.6 μm** fabrication process) or 45° (Figure 6.3(b)). With this solution, better shape control is achieved.



(a) (b)

Figure 6.3: Resistor layout (a) rounded corners with dummy resistor
(b) 45° corners with dummy resistor

Moreover, dummy resistor placed around, as shown in Figure 6.3, define the same boundary and help to improve resistor value control. Therefore, the effective width of the strip of the resistor will be reduced with respect to the designed value.

6.4 Capacitor Layout

Ideally, capacitor size is give by

$$C = \frac{\varepsilon_{ox}}{t_{ox}} A_1 = C_{ox} WL \tag{6.1}$$

However, in the fabrication, the major sources of errors in realizing capacitors are due to over etching and an oxide-thickness gradient across the surface of the microcircuit. The former effect is usually dominant and can be minimized by realizing larger capacitors from a parallel combination of smaller, unit-sized capacitors, similar to what is said in Section 6.2. Errors due to the gradient of the oxide thickness can then be minimized by interspacing the unit-sized capacitors in common-centroid layout so the gradient changes affect both capacitors in the same

way (Figure 6.4). Since oxide-thickness variations are not usually large in a reasonably small area.

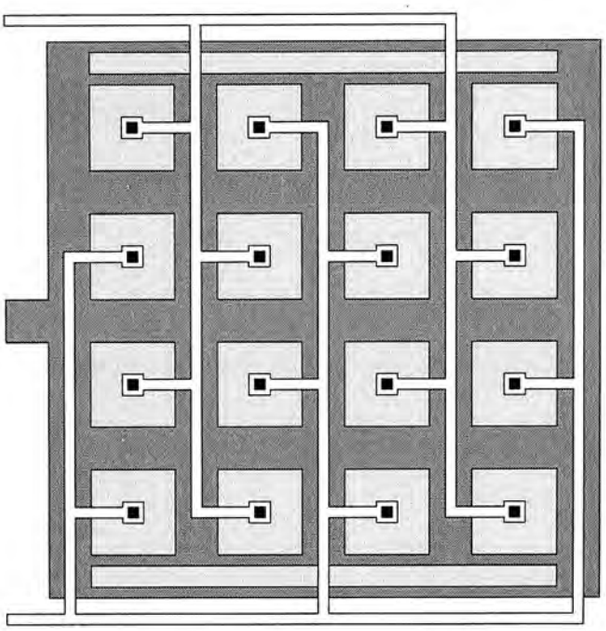


Figure 6.4: Layout of two matched capacitors with common centroid symmetry

If we assume that a capacitor has an absolute over etching of Δe and that its ideal dimensions are given by W and L, then its true dimensions are given by $W_1 =$ W - $2\Delta e$ and $L_1 =$ L - $2\Delta e$, and the true capacitor size is given by

$$C_e = C_{ox}(W - 2\Delta e)(L - 2\Delta e) \approx C_{ox}[WL - 2(W + L)\Delta e]$$
$$= C_{ox}[A - P\Delta e] \qquad (6.2)$$

where A is the designed area and P is the perimeter. Thus, the effective capacitance is smaller than the designed area by an amount proportional to the perimeter of the plate. Therefore, another way to minimize the errors in capacitor ratios due to over etching is to need the perimeter-to-area ratios the same, even when the capacitors are different sizes as shown in Figure 6.5.

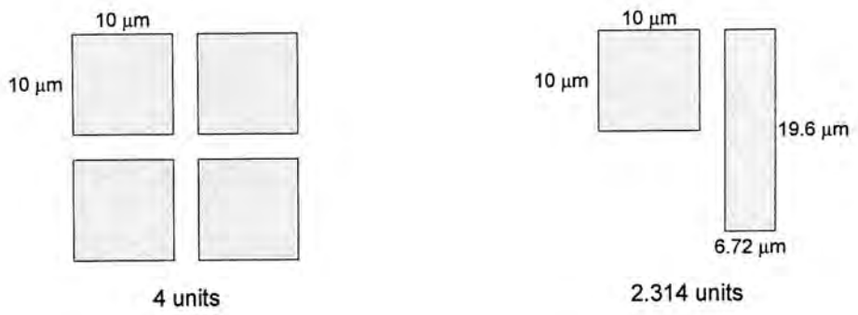


Figure 6.5: A capacitor layout with equal perimeter-to-area ratios of 4 units and 2.314 units

The routing parasitic capacitance can be calculated from the Equation (6.3), where 8.6×10^{-4} and 1.1×10^{-10} are process extracted parameters.

$$\text{Capacitance} = 8.6\times10^{-4} + 1.1\times10^{-10} \times \text{Perimeter} \qquad (6.3)$$

Parasitic resistance may be disastrous to the performance of the device. We can minimized the parasitic resistance by placing more contact windows.

6.5 Substrate Tap

In the **AMS® 0.6 μm** technology, p-type wafer is provided and the n-channel MOSFETs are fabricated directly on the p-type wafer. Substrate taps must be provided to connect the p-type substrate to the ground. Thermal noise also arise due to the substrate. However, the effect of this noise is small and can be neglected. In order to ensure that the effect of the noise is minimized, the number of substrate tap is increased to reduce the substrate resistance. Figure 6.6 shown a typical layout drawing of the substrate tap.

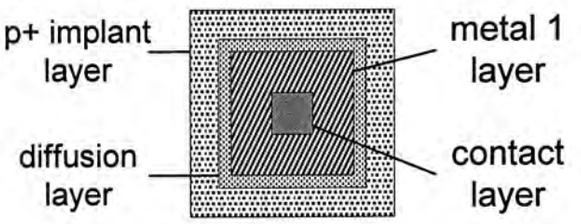


Figure 6.6: Layout of the substrate tap

6.6 Pad Layout

The pad structure used in the **AMS® 0.6 μm** technology is drawn in Figure 6.7 . It consists of a Pad layer as bonding layer to conduct the signal, Metal 3 at the bottom us used as shielding. Moreover, there are several layers in between in order to have better shielding. This structure has the advantage of reducing the capacitive coupling from the noisy substrate to the signal pads through the substrate spreading resistance.

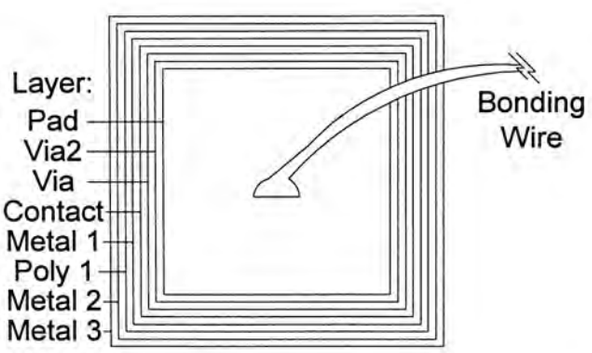


Figure 6.7: Layout of the bonding pad

6.7 Analog Cell Layout

Although the complexity of analog cells is limited, the performance of these circuits are strongly depending on the layout technique. Analog design is a very critical task that requires a certain amount of caution. Usually, there are some guidelines to follow in order to maximize the circuit performance:

- Use transistors with the same orientation;
- Use symmetries layout drawing in order to limit offset;
- Use low resistive paths when a current needs to be carried. So, it could avoid the parasitic drop voltages;

Chapter 7

Measurements

7.1 Introduction

In this chapter, the measurement results of the first and second downconversion mixer prototypes will be presented. We have test the following list of mixer parameters:

(i) Matching,

(ii) S-Parameter,

(iii) Conversion gain (loss),

(iv) 1-dB compression point,

(v) Input third-order intercept point (IIP3),

(vi) The effect of the LO power variation,

(vii) The effect of the IF variation.

At the same time, the measurement results of a single-ended to differential-ended converter will be given.

7.2 Downconversion mixer

Two testing prototypes have been fabricated in **AMS® 0.6 μm CMOS** technology. Since the probe station and the probe tip are not available during the measurement. Therefore, the first tested circuit (current folded mirror mixer) is in SOP (Small Outline Package) and solders it on a PCB for measurement. The second tested circuit (current mode mixer) uses silver epoxy to glue the circuit die on the PCB and bonds the wire from the die to the PCB. Moreover, a PCB layout design is needed to solder the circuit for high frequency measurement. The detail of the setup and fabrication of the PCB will be presented in the following section.

7.3 PCB Layout

The testing circuit is soldered on a PCB board, which can operate at high frequency (900 MHz). Therefore, the matching between the instrument port and the tested circuit port is very important. Usually, 50 Ω matching is required.

Firstly, we need to calculate the width (w) of the microstrip line on the PCB in order to give out the 50 Ω characteristic impedance of the line. Then the lumped surface mount elements, inductor (L) or capacitor (C), will be used to tune the input impedance to 50 Ω.

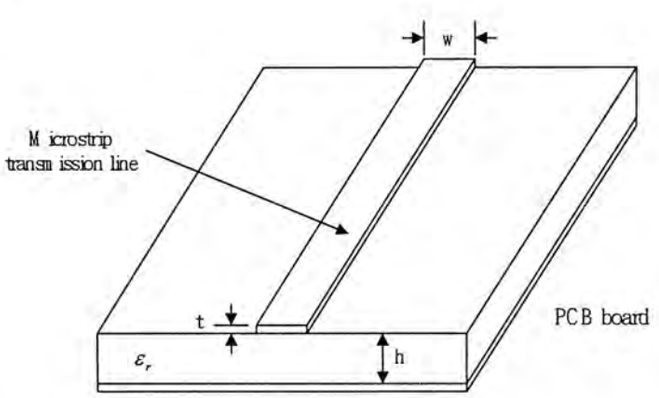


Figure 7.1: Microstrip transmission line on the PCB

FR4 (PCB) board is used in the experimental measurement. The height (h) and the dielectric constant (ε_r) of the board are 0.8 mm and 4.2 respectively. By solving the following two equations (Equation (7.1) and Equation (7.2)):

$$\varepsilon_{eff} = \frac{\varepsilon_r + 1}{2} + \frac{\varepsilon_r - 1}{2} \frac{1}{\sqrt{1 + 12h/w}} \tag{7.1}$$

$$Z_o = \frac{120\pi}{\sqrt{\varepsilon_{eff}}} \frac{1}{w/h + 1.393 + 0.667 \ln(1.444 + w/h)} = 50 \tag{7.2}$$

where w is the width of the microstrip line

h is the height of the substrate

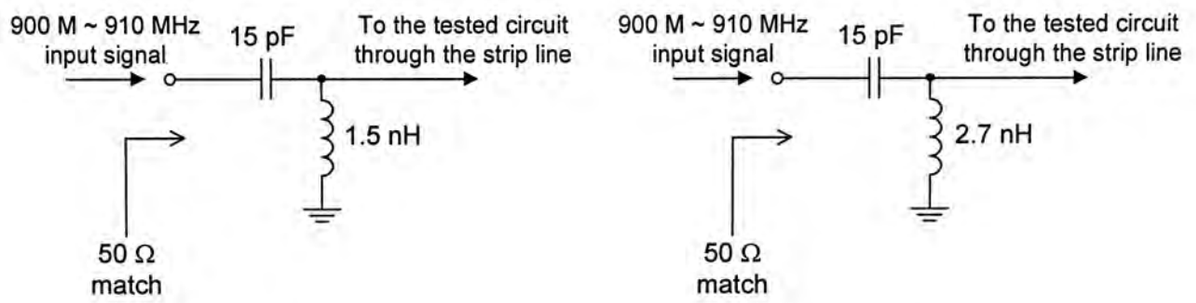
ε_r is the dielectric constant of the substrate

ε_{eff} is the effective dielectric constant

Z_o is the characteristic impedance

We could get the width (w) of the microstrip line is equal to 1.6 mm. Then the characteristic impedance is equal to 50 Ω.

Afterwards, using matching networks with different parameter value in the current folded mirror mixer (Figure 7.2 (a)) and the current mode mixer (Figure 7.2 (b)) to match a 50 Ω input impedance.



(a) (b)

Figure 7.2: The parameter value and the configuration of the matching networks used in (a) current folded mirror mixer and (b) current mode mixer

7.4 Test Setups

There are mainly three test setups for measuring the performance of the mixer. In Section 7.4.1, we will present a setup for measuring the matching and the S-Parameter value. Afterwards, two setups for measuring the 1-dB compression and the IIP3 would be given respectively.

7.4.1 Measurement Setup for S-Parameter

For the S-Parameter measurement, the S-Parameter test set (HP 85046A) accompanies with the network analyzer (HP 4396A) will be used. The connection setup is shown in Figure 7.3.

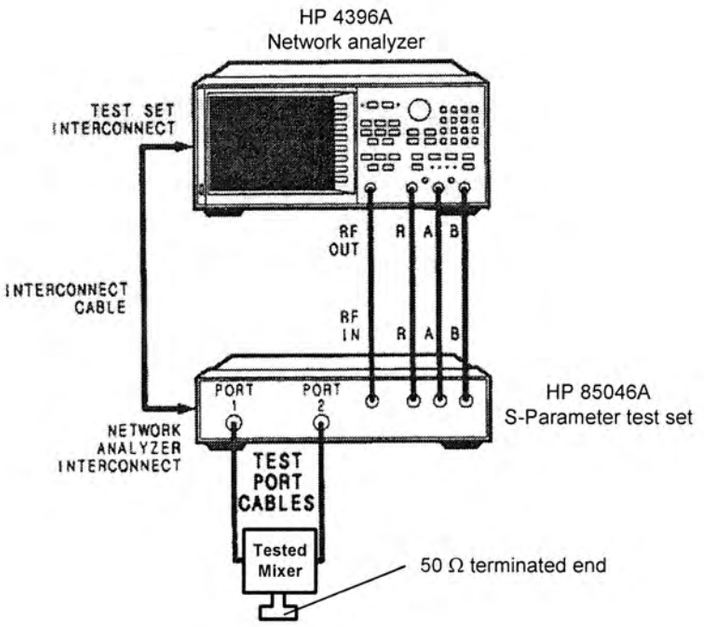


Figure 7.3: The test setup for S-Parameter measurement

The port of the tested mixer has been already matched to 50 Ω by Section 7.3 with SMA connectors. Since the mixer has three ports, RF, LO and IF port, so a 50 Ω terminator is needed to terminate one of port while the other two ports are being tested.

Figure 7.4: The 50 Ω terminated end

7.4.2 Measurement Setup for 1-dB Compression Point and IIP3

For the 1-dB compression point measurement, we need two signal generators (HP 8648C) and one spectrum analyzer (HP 8594EM). The RF (900MHz) and LO (910 MHz) input signals are generated by the two signal generators and feed into the tested mixer input ports respectively. The downconverted signal IF (10 MHz) is measured by the spectrum analyzer. The experimental setup is shown in Figure 7.5.

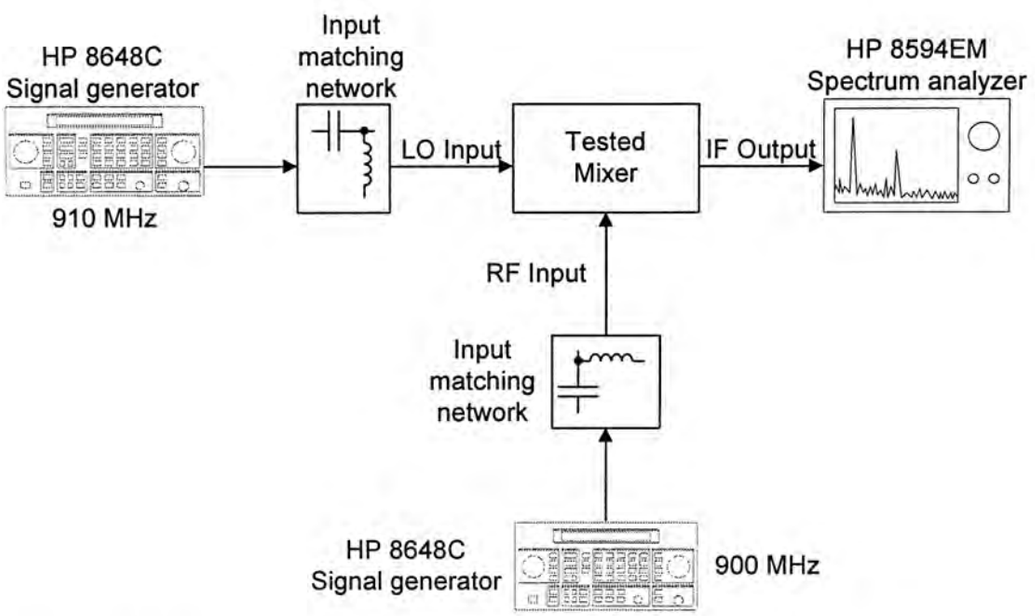


Figure 7.5: Experimental setup for 1-dB compression point measurement

Figure 7.6 shown the downconverted signal (IF) from the spectrum analyzer in the 1-dB compression point measurement.

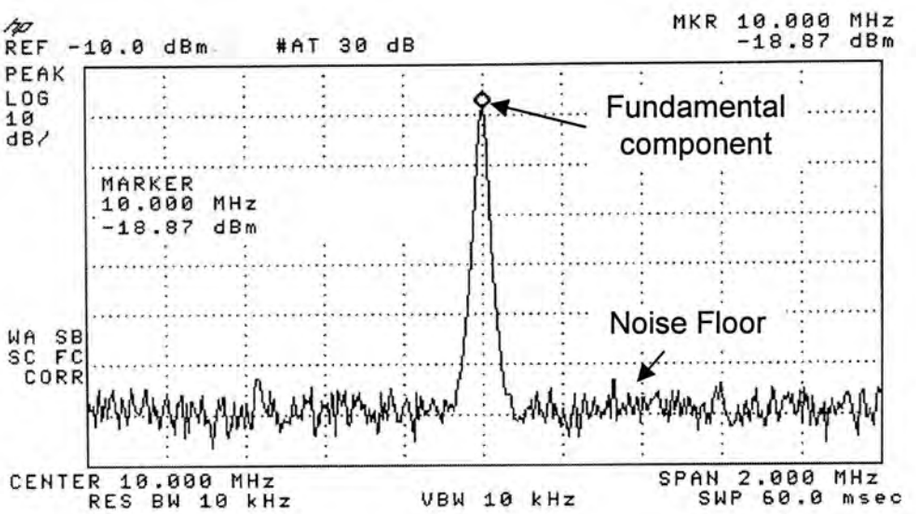


Figure 7.6: Measurement result of the 1-dB compression point of the mixer

For the IIP3 measurement, one more of the signal generator (HP 8656B) and a 2 way-0° power combiner (mini-circuits ZFSC-2-2500) are needed. Figure 7.7 shown the experimental setup used for IIP3 measurement.

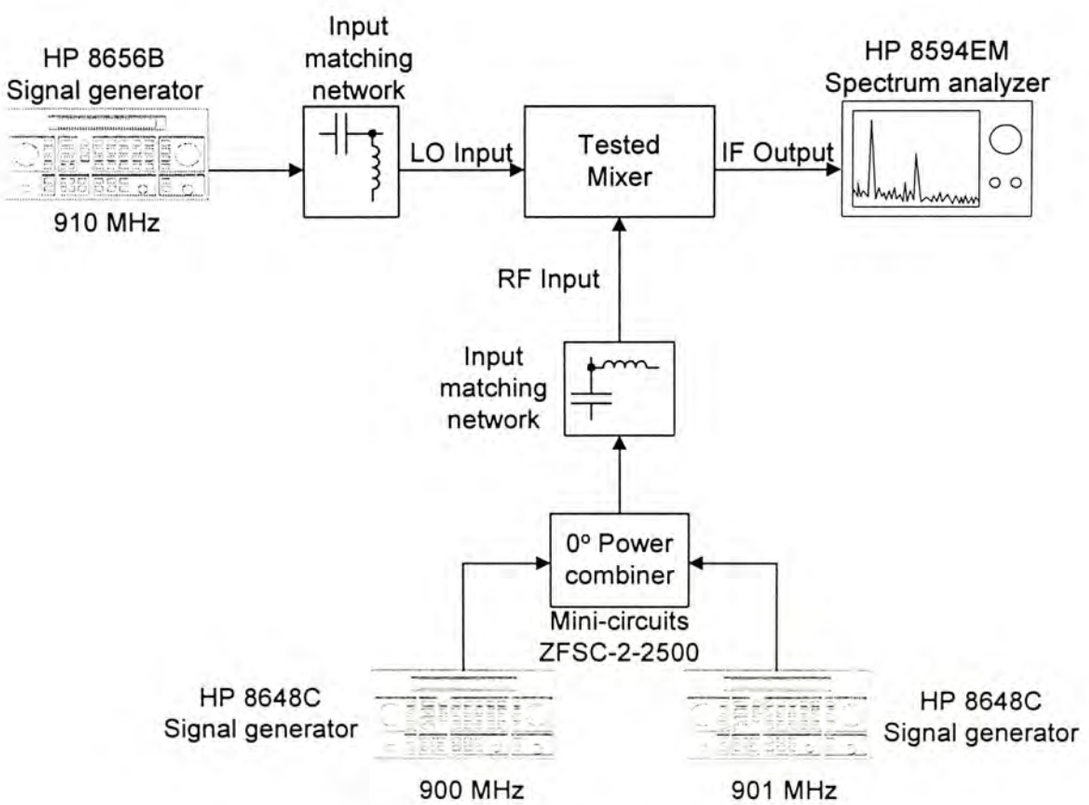


Figure 7.7: Experimental setup for IIP3 measurement

Two signal generators generate two closed frequency (900 MHz and 901 MHz) and combine with the power combiner to form an RF input in order to measure the third order intermodulation products in the spectrum analyzer.

Figure 7.8 shown the downconverted signal and the third-order intermodulation products on the spectrum analyzer in the IIP3 measurement.

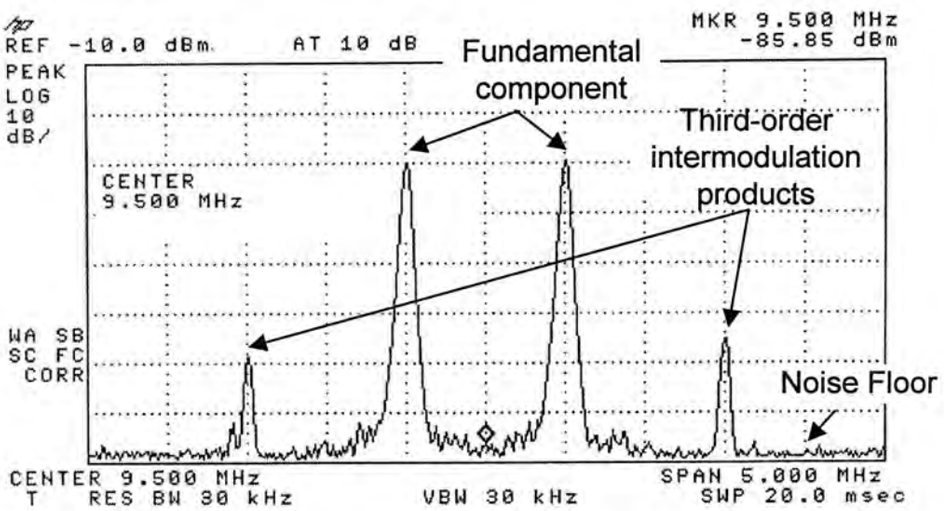


Figure 7.8: Measurement result of the IIP3 of the mixer

7.5 Measurement Result of the Current Folded Mirror Mixer

The microphotograph and the layout drawing of the current folded mirror mixer are printed in Figure 7.9 and Figure 7.10 respectively. It is operating with a single voltage supply of ***1.5 V***, the total power consumption of the mixer is ***7.5 mW***. The active die area is ***250 μm × 300 μm***.

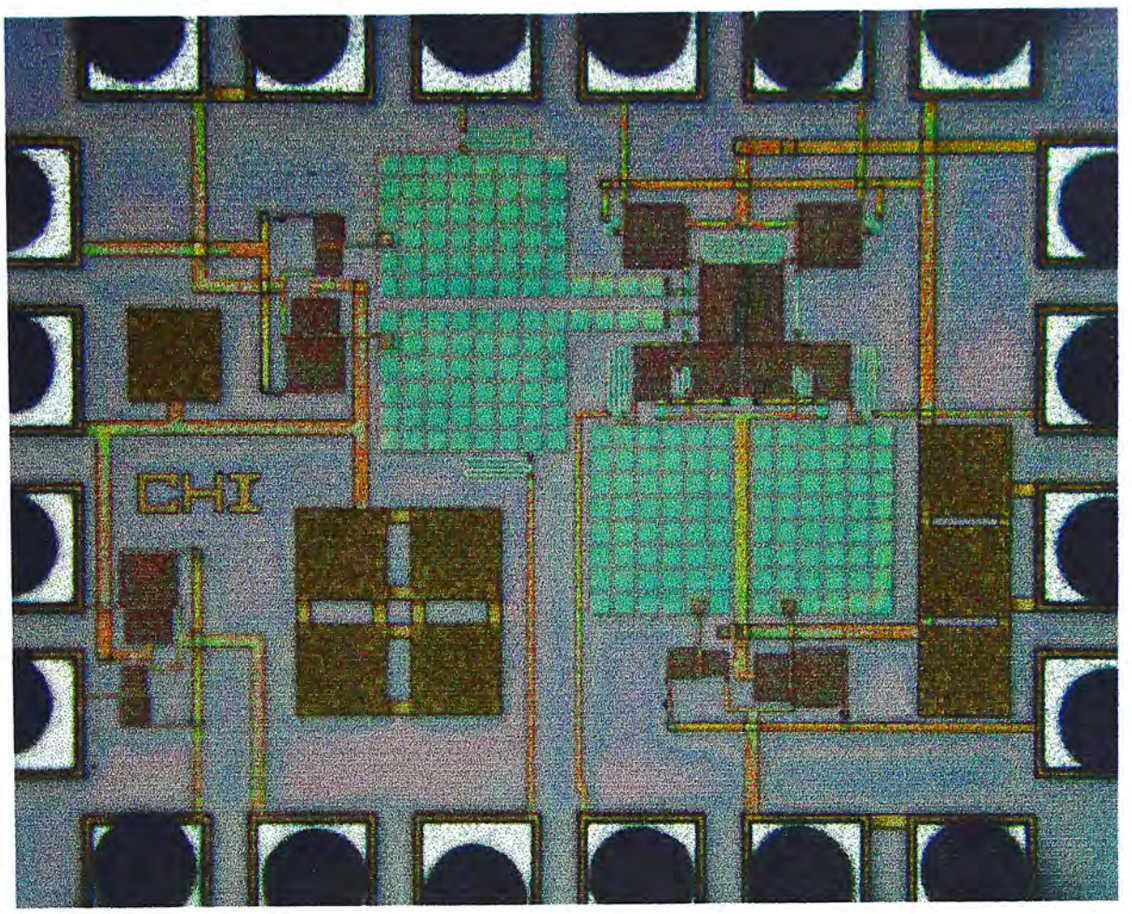


Figure 7.9: Microphotograph of the current folded mirror mixer

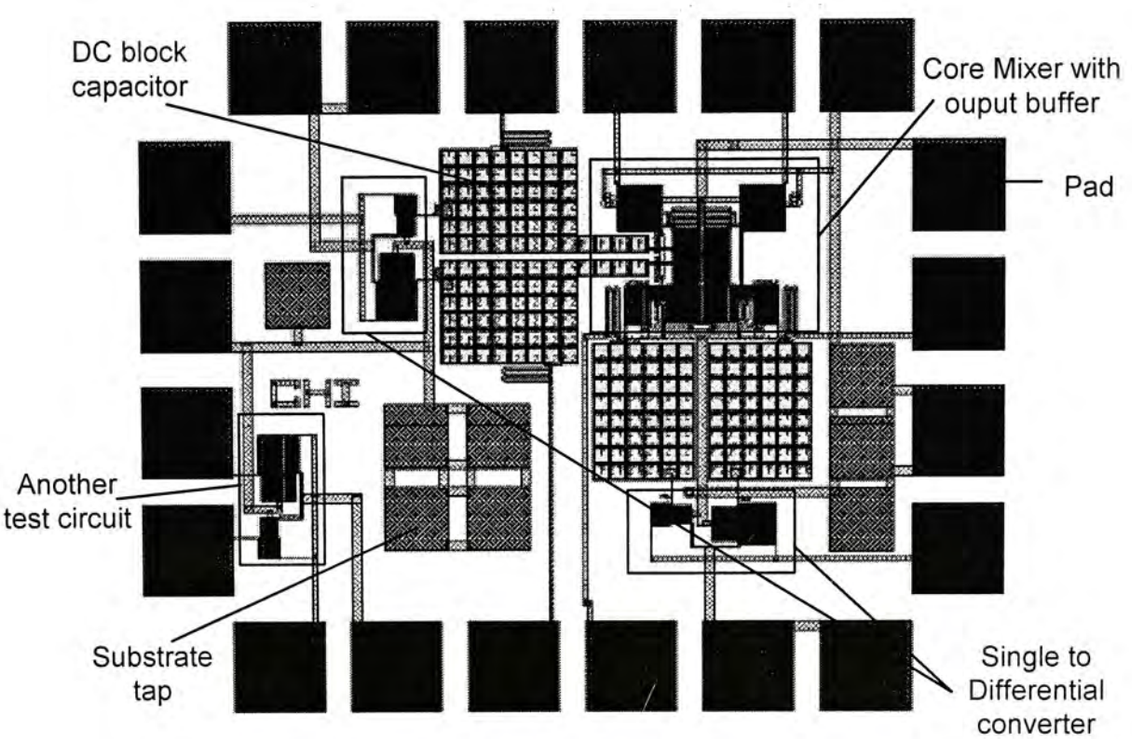


Figure 7.10: Layout drawing of the current folded mirror mixer

Figure 7.11 and Figure 7.12 show the top view of the current folded mirror mixer on the PCB and the experimental setup in the laboratory respectively.

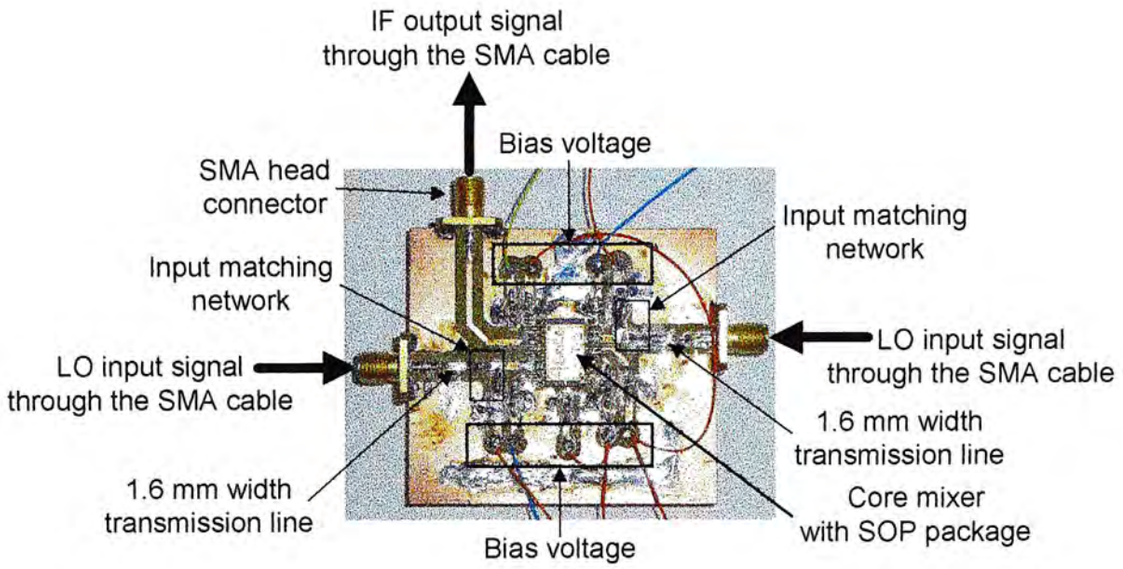


Figure 7.11: Top view of the current folded mirror mixer test board

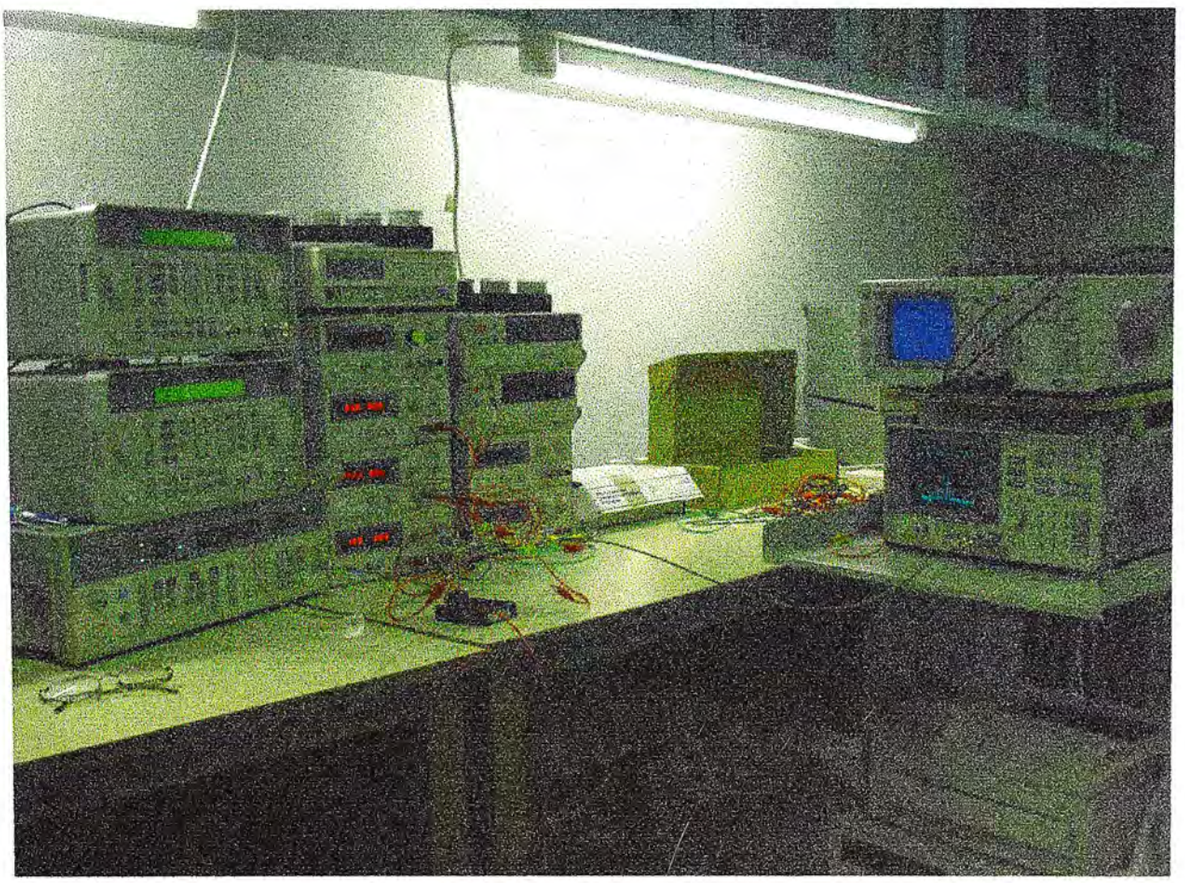


Figure 7.12: Experimental setup in the laboratory

7.5.1 S-Parameter Measurement

We use S-parameter measured for the following isolation measurement, LO-IF, LO-RF and RF-IF. Moreover, the RF port and LO port impedance matching was measured.

For the RF and LO impedance matching measurement, the LO, RF and IF port would be connected as shown in Figure 7.13.

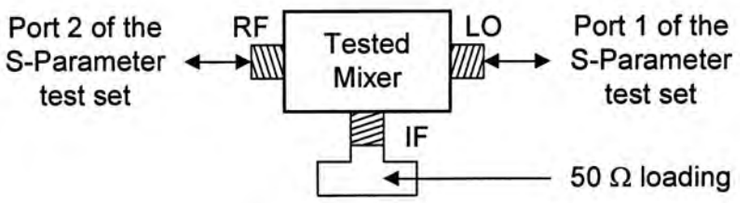


Figure 7.13: The connection configuration of the RF and LO S-Parameter measurement

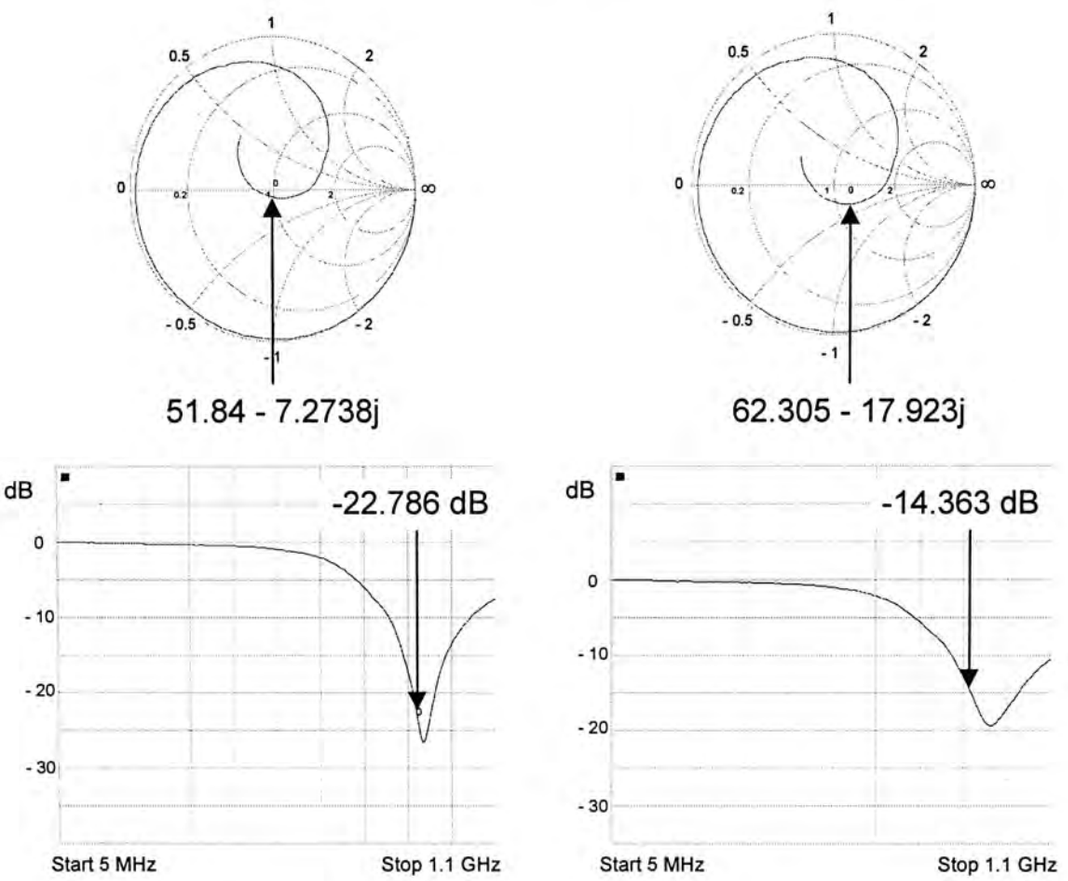
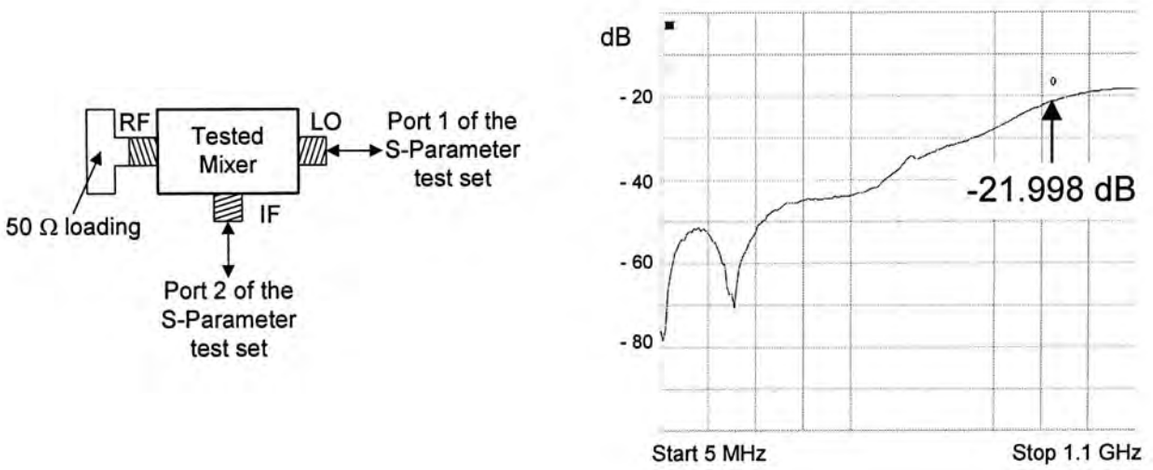


Figure 7.14: The impedance matching of the (a) S_{11} (LO port) and (b) S_{22} (RF port)

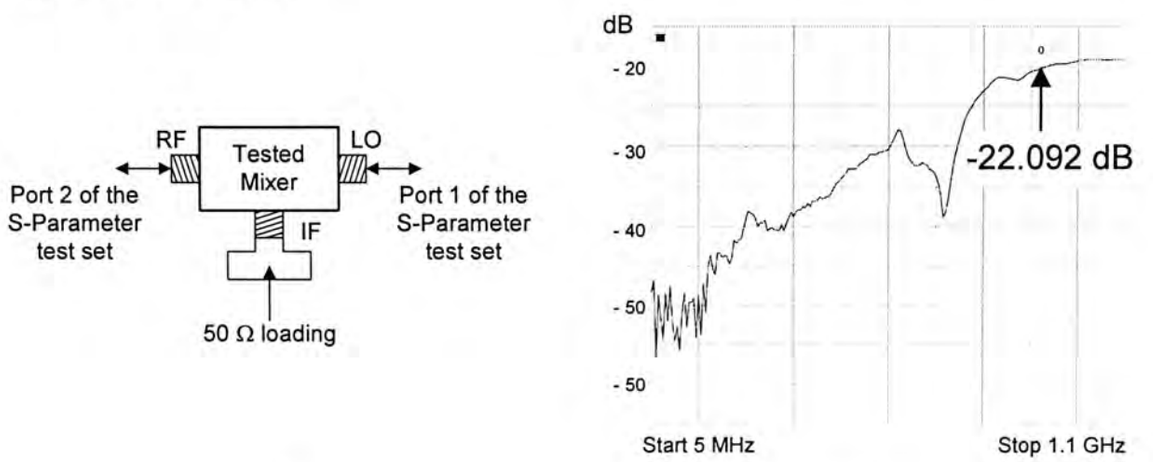
The connection configuration and the measurement results of the LO-IF, LO-RF, and RF-IF S-Parameter (isolation) as shown in Figure 7.15, Figure 7.16 and Figure 7.17 respectively



(a) (b)

Figure 7.15: (a) The connection configuration and
(b) the measurement result of the S_{21}

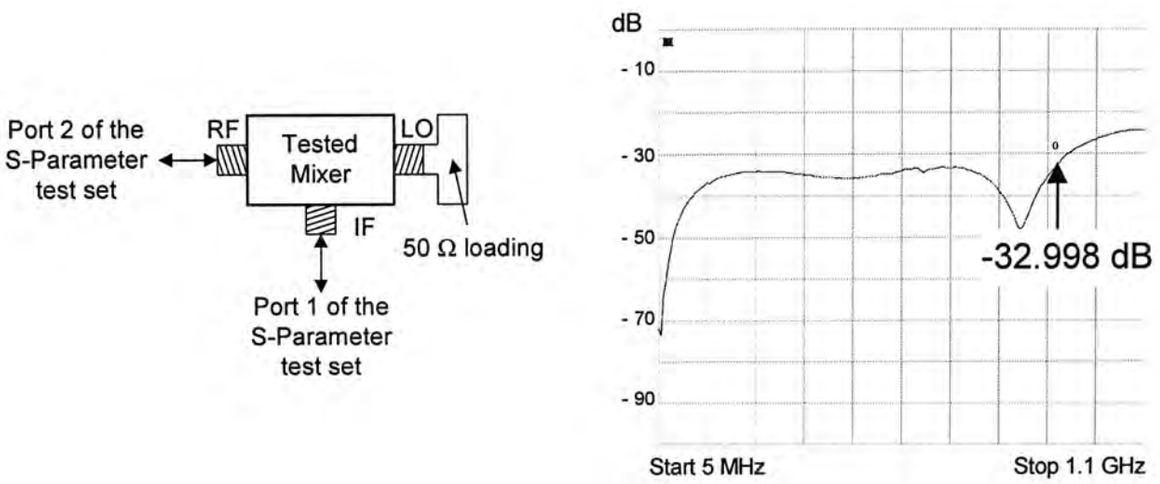
From the Figure 7.15, it is shown that the LO-IF isolation (S_{21}) is equal to 21.998 dB at 910 MHz.



(a) (b)

Figure 7.16: (a) The connection configuration and
(b) the measurement result of the S_{21}

From the Figure 7.16, it is shown that the LO-RF isolation (S_{21}) is equal to 22.092 dB at 905 MHz.



(a) (b)

Figure 7.17: (a) The connection configuration and
(b) the measurement result of the S_{12}

From the Figure 7.17, it is shown that the RF-IF isolation (S_{12}) is equal to –32.998 dB at 900 MHz.

7.5.2 Conversion Gain and the Effect of the IF Variation

The conversion gain is measured by using the same setup as shown in Figure 7.5. The LO input signal is fixed at 910 MHz with a power of –2 dBm. The RF input signal is fixed at –9 dBm and a frequency is swept from 810 MHz to 908 MHz.

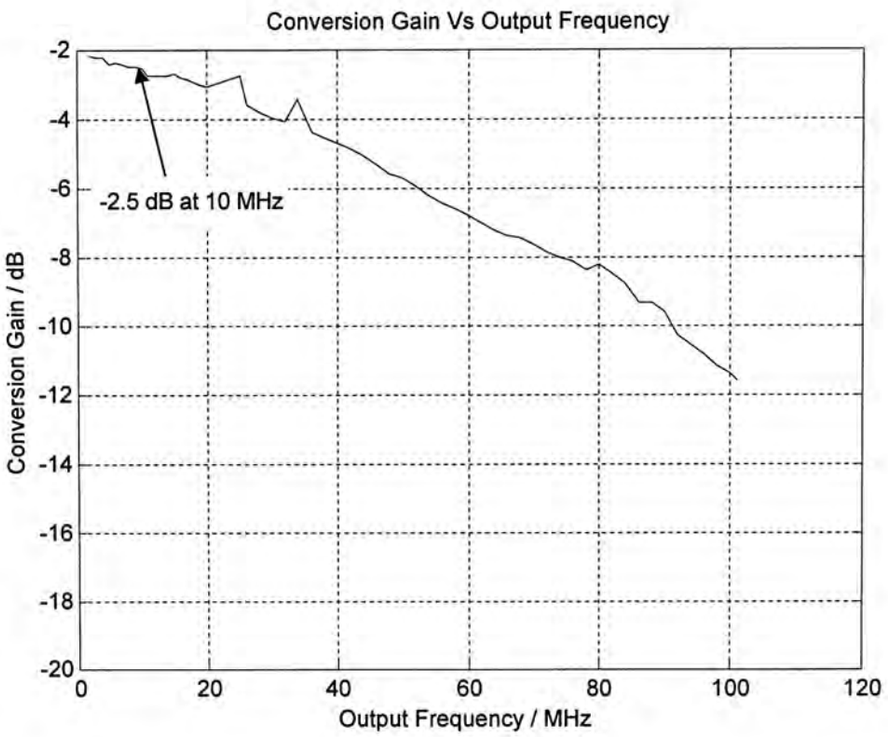


Figure 7.18: Experimental result of the conversion gain verse output frequency (IF)

Figure 7.18 shows the experimental result of effect of the conversion gain as the output (immediate) frequency in varying. The conversion gain starts from –2.1 dB to –3 dB when the immediate frequency rises from 1 MHz to 20 MHz. Afterwards, the conversion gain drop down to –11.8 dB as the IF up to 100 MHz.

7.5.3 1-dB Compression Point

For the 1-dB compression point measurement, the setup of the Figure 7.5 is used. The LO input signal is fixed at 910 MHz with a power of –2 dBm. The RF input signal is fixed at 900 MHz with a power swept from –53 dBm to 7 dBm.

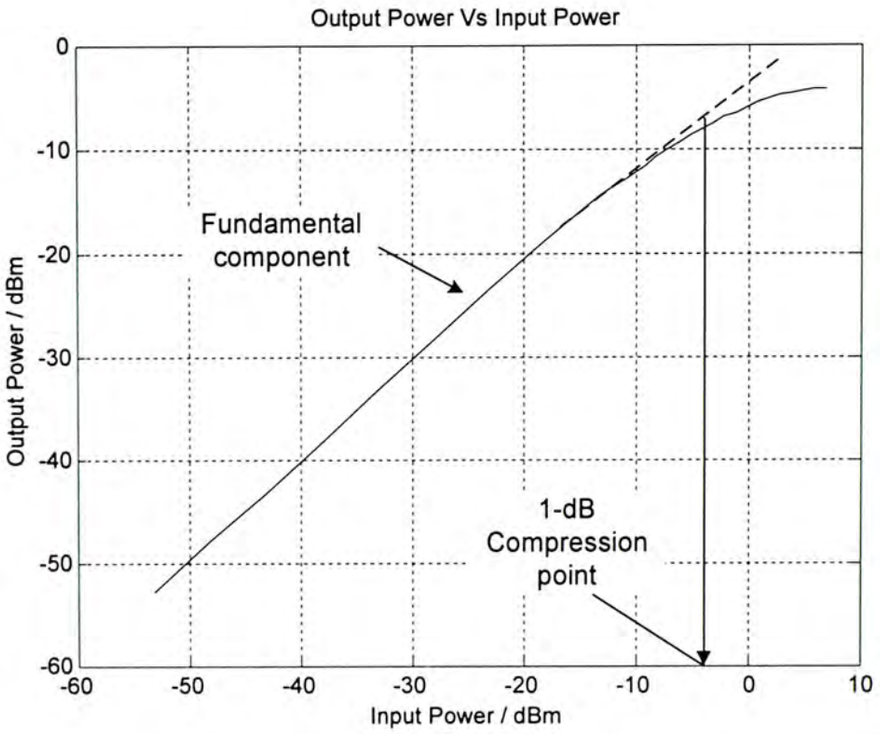


Figure 7.19: Experimental result of the 1-dB compression point

Figure 7.19 shows the measurement result of the 1-dB compression point of the current folded mirror mixer. The value of it is about –3 dBm.

7.5.4 IIP3

The experimental setup shown in Figure 7.7 is adopted for the measurement of the third-order input intercept point (IIP3). The LO input signal is fixed at 910 MHz with a power of –2dBm. Power combiner combines the fixed two-tone RF signals at 900 MHz and 901 MHz with a power swept from –28 dBm to 6 dBm. The noise floor measured from the spectrum analyzer is equal to –75 dBm.

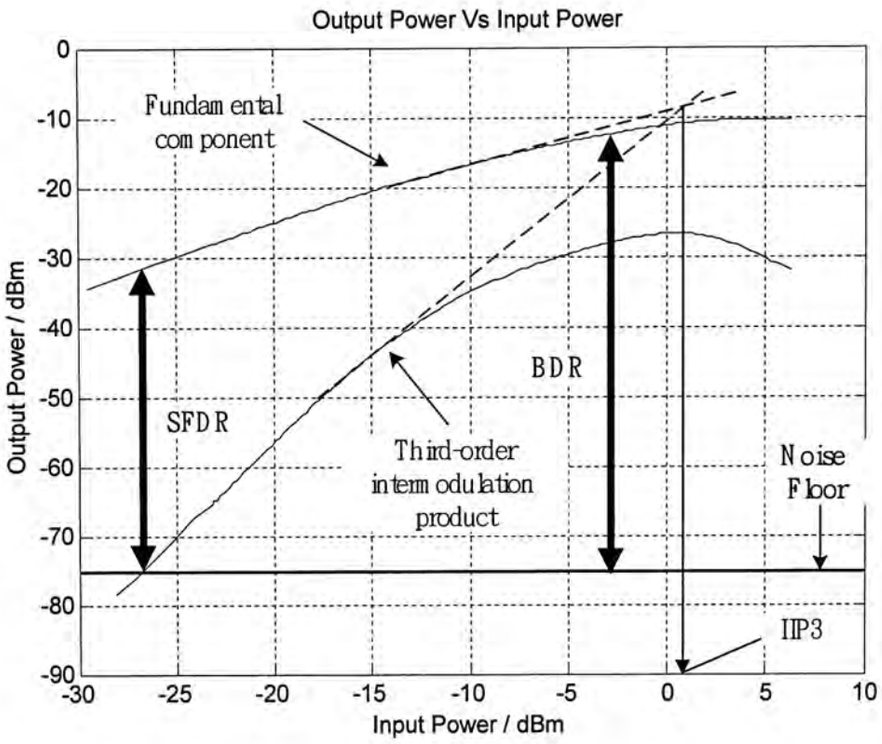


Figure 7.20: Experimental result of the IIP3, SFDR and BDR

The value of the measured IIP3 shown in Figure 7.20 is equal to 1 dBm. Moreover, from Section 2.5.1, it can be realized that the Spurious-Free Dynamic Range (SFDR) of the CMOS Current Folded Mirror Mixer is equal to

$$\begin{aligned} \text{SFDR} &= \frac{2}{3}\left(P_{IIP3} - P_{NiFlr}\right) \\ &= \frac{2}{3}\left[1-(-75)\right] \\ &= 50.7\ \text{dB} \end{aligned} \tag{7.3}$$

In addition, the blocking Dynamic Range (BDR) (Section 2.5.2) of the CMOS Current Folded Mirror Mixer is equal to

$$\begin{aligned} \text{BDR} &= P_{-1\text{dB}} - P_{\text{NsFlr}} \\ &= -3-(-75) \\ &= 72\ \text{dB} \end{aligned} \tag{7.4}$$

7.5.5 LO Power Effect to the Mixer

In Section 4.2.1, we have presented that a certain large amount of the LO signal power is needed at a moderate inversion dc bias in order to operate the CMOS Gilbert quad as a switch.

The experimental setup for measuring the effect of the LO power on conversion gain is same as that for measuring 1-dB compression point (Figure 7.5) except that instead of sweeping the RF input signal, we swept the LO input signal from –53 dBm to 6 dBm.

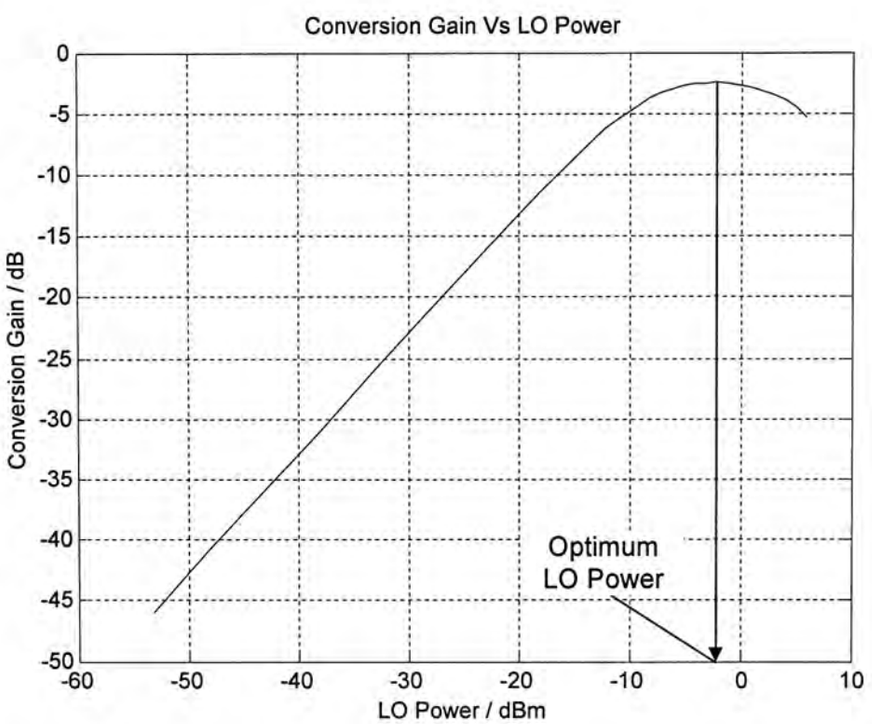


Figure 7.21: Experimental result of the effect of the LO power on conversion gain

From Figure 7.21, it can be realized that in order to achieve the maximum conversion gain, the optimum LO power should be equal to –2 dBm. As the LO power below or above –2 dBm, the conversion gain is dropping. It is due to the non-perfect switching of the Gilbert quad pair and the over driven of the CMOS pair.

7.5.6 Performance Summaries of the Current Folded Mirror Mixer

Specifications	Value
Supply voltage / V	1.5
Total power consumption / mW	7.5
LO port impedance / Ω	51.84 – 7.2738j
RF port impedance / Ω	62.305 – 17.923j
LO – IF isolation / dB	21.998
LO – RF isolation / dB	22.092
RF – IF isolation / dB	32.998
Conversion gain / dB	-2.5
1-dB compression point / dBm	-3
IIP3 / dBm	1
Active area[(1)] / μm × μm	250 × 300

Table 7.1: Performance summaries of the current folded mirror mixer

[(1)] Excluded the DC blocking capacitor

7.5.7 Discussion

Table 7.1 summaries the performance of the Current Folded Mirror Mixer. The measurement results of the circuit show good conformity to simulation. However, there are still some difference between the simulation and the measurement result in conversion gain and 1-dB compression point. It is due to the poor modeling of the circuit model in the substrate conductance and the capacitive coupling in the simulator. Moreover, the uneven bonding wires from the bond pads to the package pins contribute the phase difference and the voltage attenuation. Which is hard to eliminate in the package measurement.

From the experimental result, the current folded mirror mixer gives a similar or improves performance than [[1], [30], [31], [32]] at a low voltage supply of 1.5 V. Moreover, the circuit configuration of the current folded mirror is simple and no inductor is needed, which is more suitable for integrated circuit, because on chip inductor is difficult to fabricate and has very poor performance.

7.6 Measurement Result of the Current Mode Mixer

The microphotograph and layout drawing of the current mode mixer are shown in Figure 7.22 and Figure 7.23 respectively. The operating voltage is ***1.2 V***, the total power consumption of the mixer is ***3 mW***, and the active die area is ***400 μm × 400 μm***.

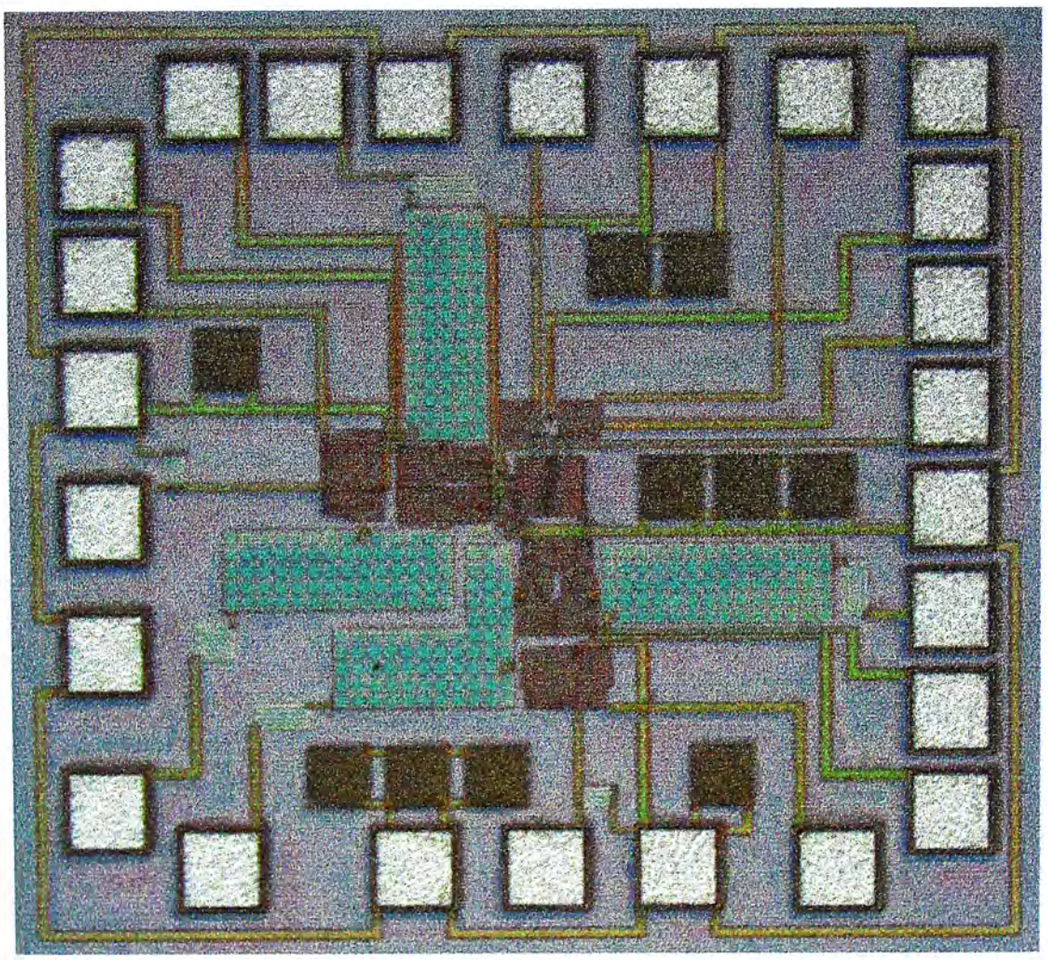


Figure 7.22: Microphotograph of the current mode mixer

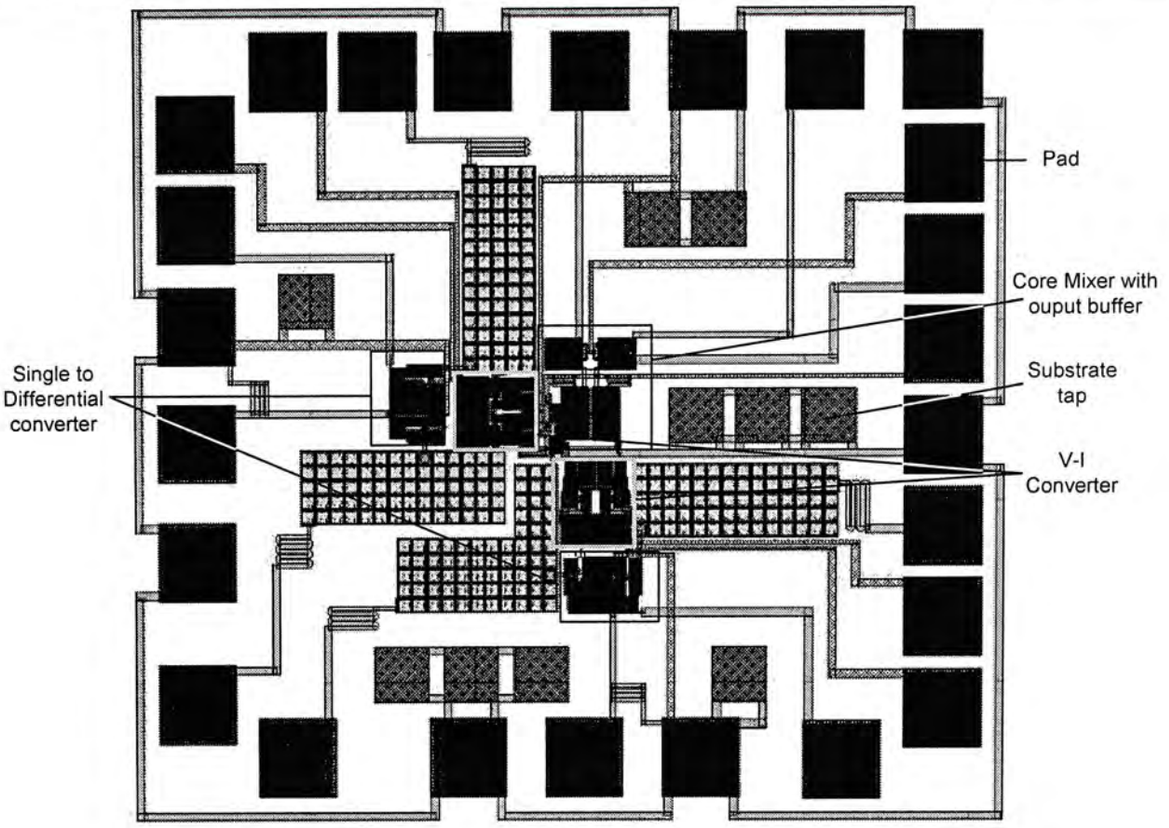


Figure 7.23: Layout drawing of the current mode mixer

Figure 7.24 to Figure 7.26 show the top and side view of the current mode mixer on the PCB and the experimental setup in the laboratory respectively.

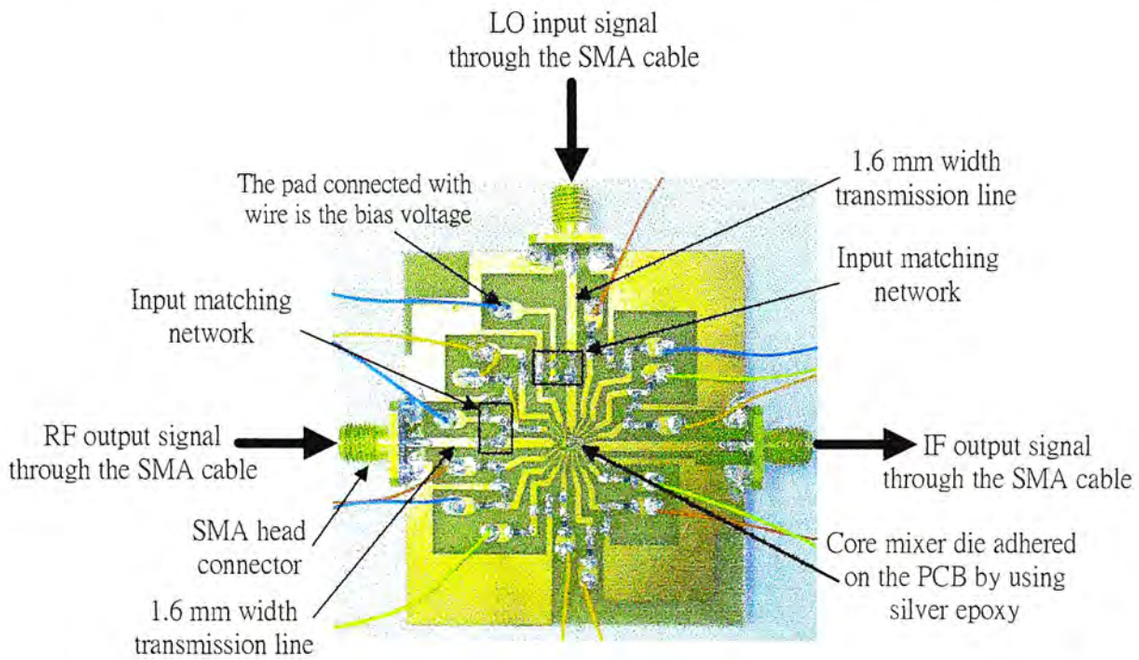


Figure 7.24: Top view of the current mode mixer test board

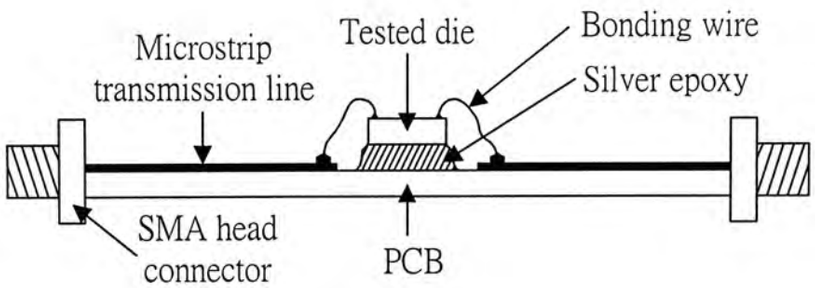


Figure 7.25: Side view of the current mode mixer test board

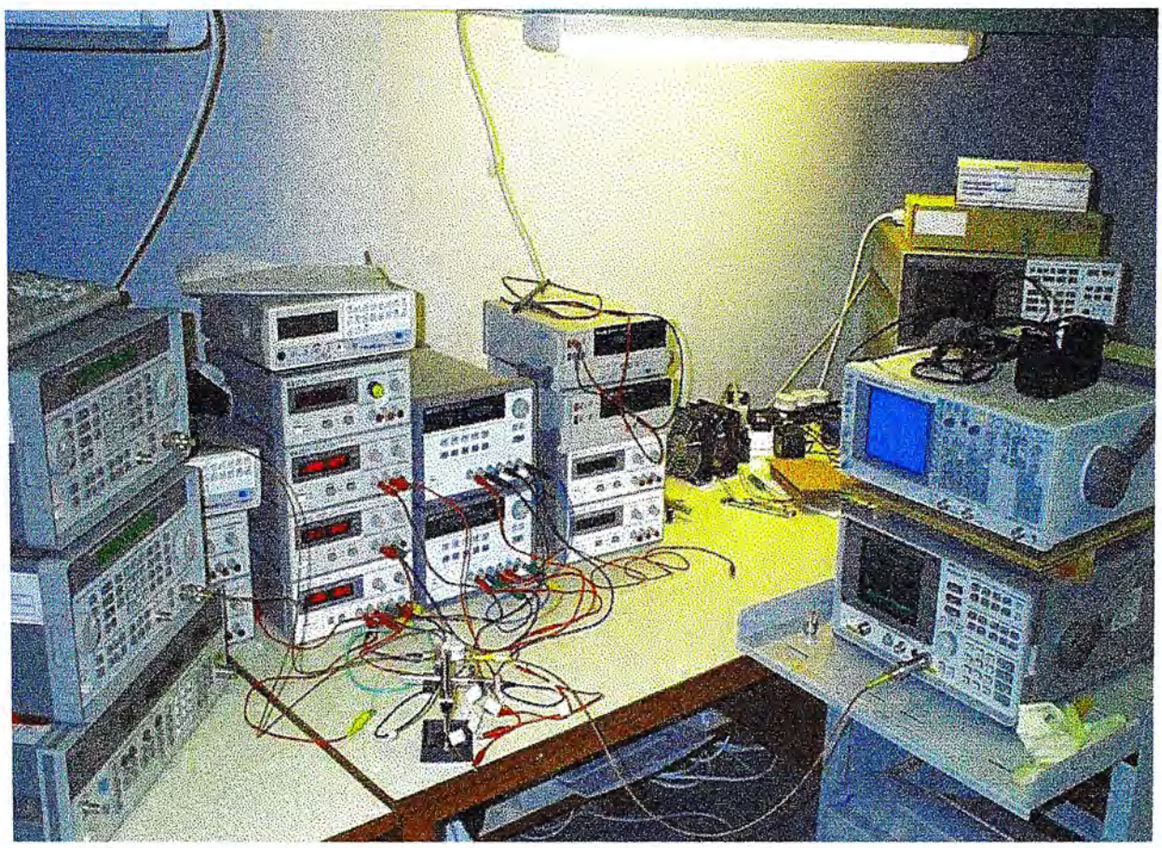


Figure 7.26: Experimental setup in the laboratory

7.6.1 S-Parameter Measurement

This is the same setup discussed in Section 7.4.1. We have measured the, LO-IF, LO-RF, and RF-IF isolation. Moreover, the RF port and LO port impedance matching was measured too.

For the RF and LO impedance matching measurement, the LO, RF and IF ports are connected as shown in Figure 7.27.

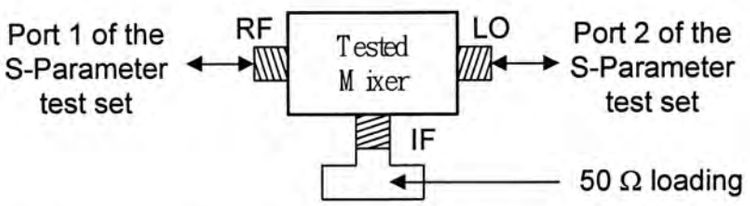


Figure 7.27: The connection configuration of the RF and LO S-Parameter measurement

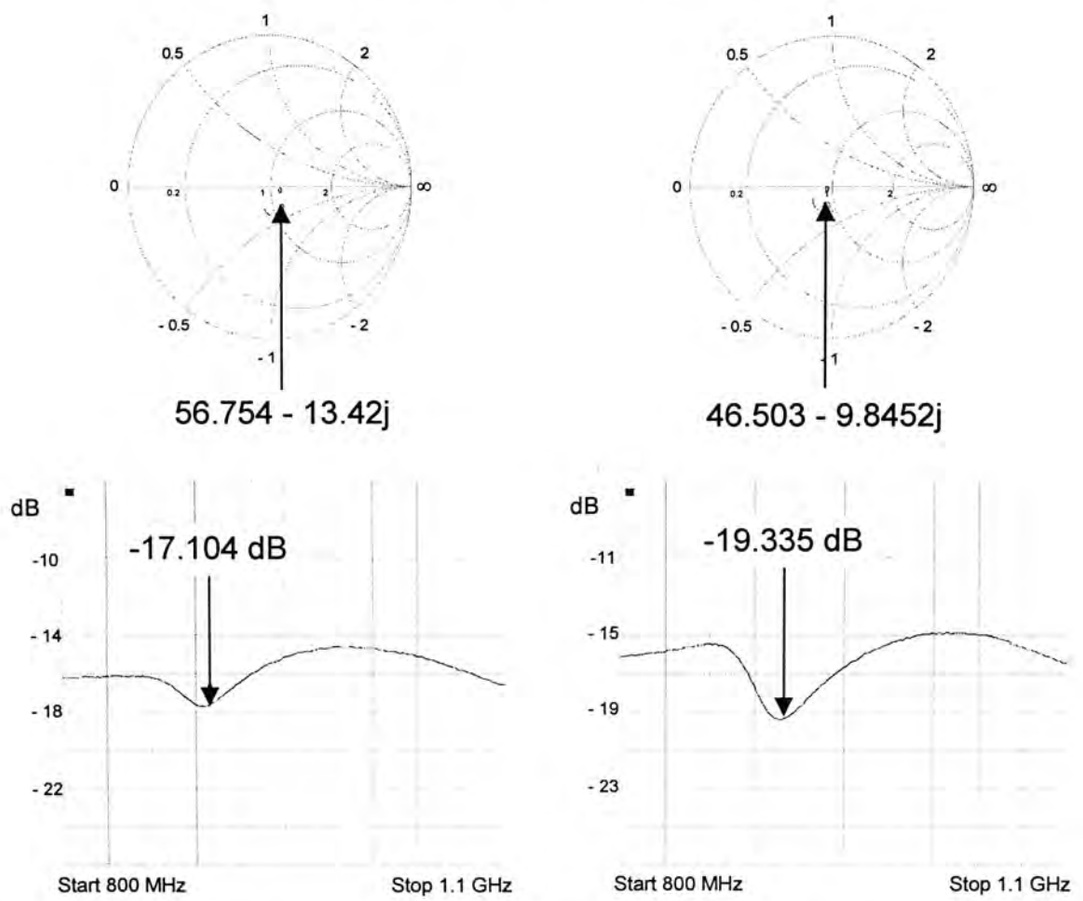
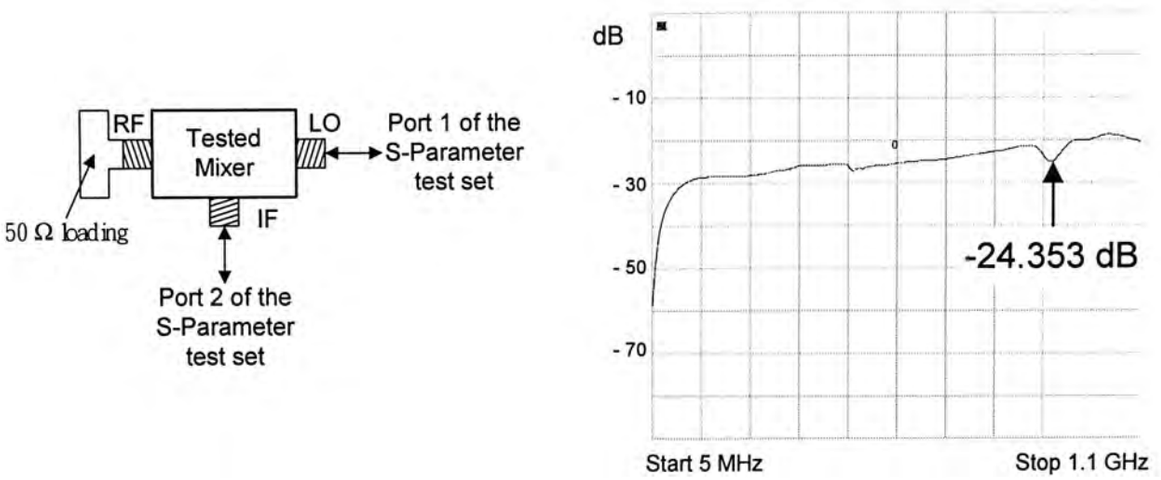


Figure 7.28: The impedance matching of the (a) S_{11} (RF port) and (b) S_{22} (LO port)

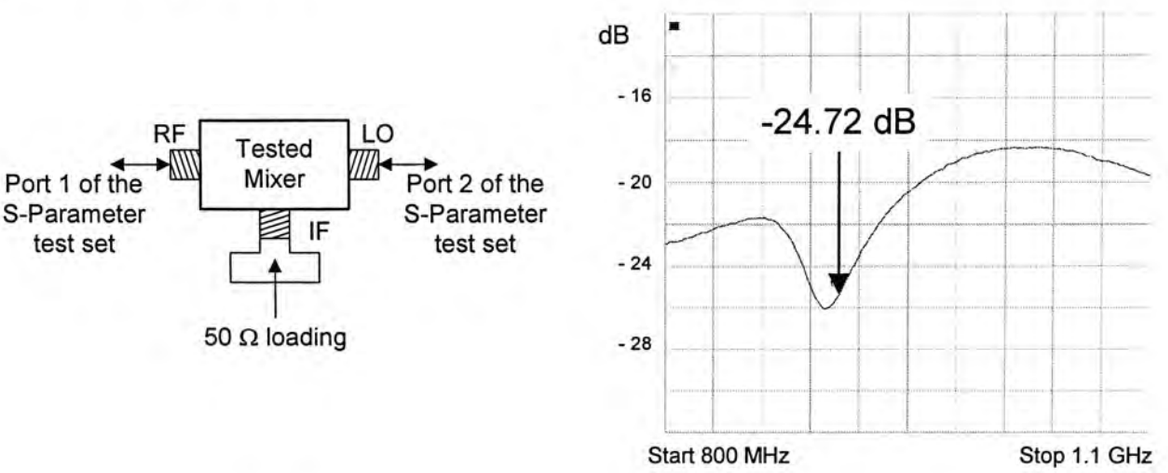
The connection configuration and the measurement result of the LO-IF, LO-RF and RF-IF S-Parameter (isolation) are shown in Figure 7.29 to Figure 7.31.



(a) (b)

Figure 7.29: (a) The connection configuration and
(b) the measurement result of the S_{21}

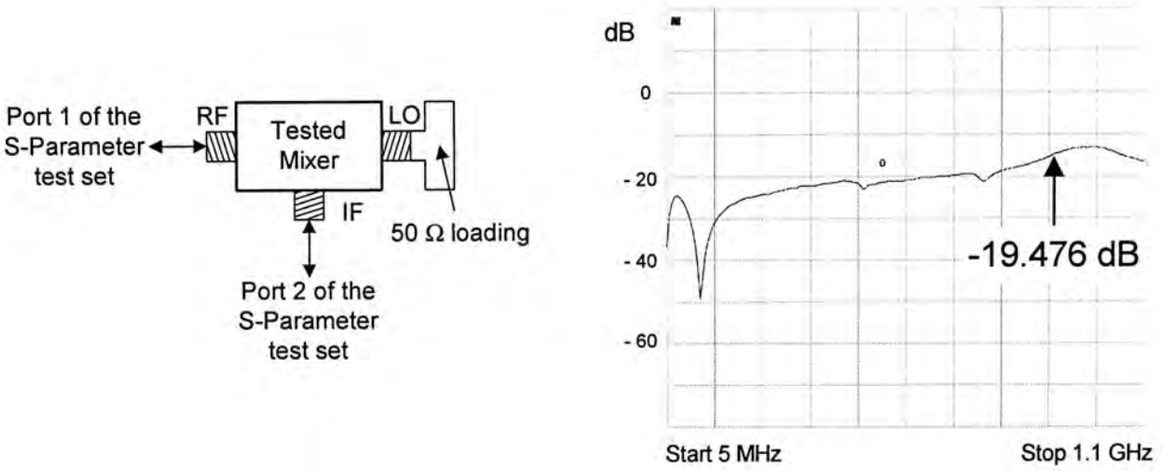
From the Figure 7.29, it is shown that the LO-IF isolation (S_{21}) is equal to 24.353 dB at 910 MHz.



(a) (b)

Figure 7.30: (a) The connection configuration and
(b) the measurement result of the S_{12}

From the Figure 7.30, it is shown that the LO-RF isolation (S_{12}) is equal to 24.72 dB at 905 MHz.



(a) (b)

Figure 7.31: (a) The connection configuration and
(b) the measurement result of the S_{21}

From the Figure 7.31, it is shown that the RF-IF isolation (S_{21}) is equal to 19.476 dB at 900 MHz.

7.6.2 Conversion Gain and the Effect of the IF Variation

The conversion gain is measured by using the same setup as shown in Figure 7.5. The LO input signal is fixed at 910 MHz with a power of 6 dBm. The RF input signal is fixed at –8 dBm and a frequency is swept from 810 MHz to 908 MHz.

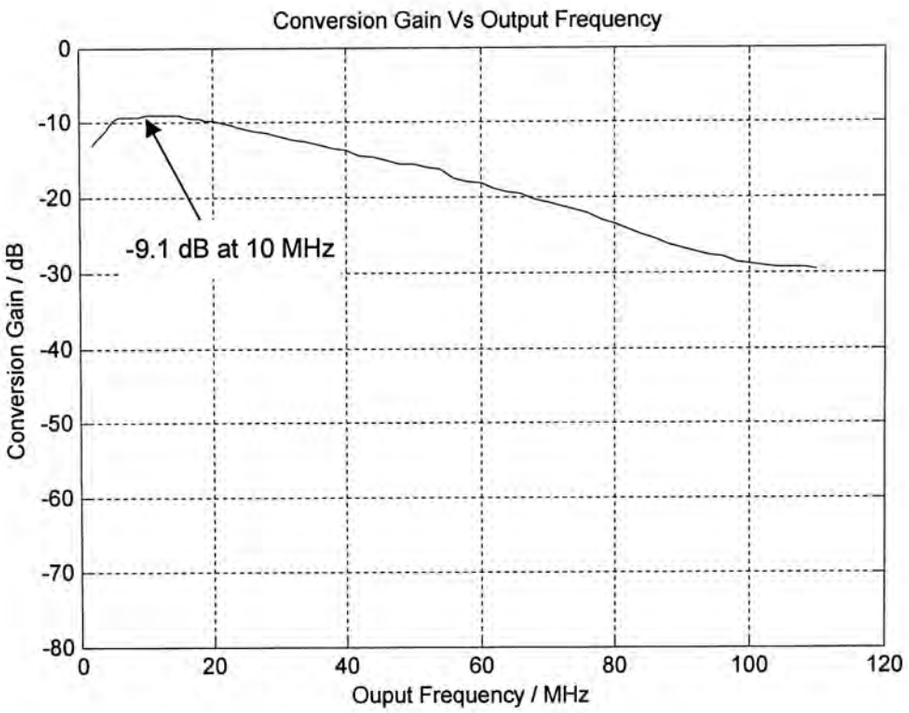


Figure 7.32: Experimental result of the conversion gain verse output frequency (IF)

Figure 7.32 shows the experimental result of the conversion gain as the output (immediate) frequency in varying. The conversion gain is increasing from –13 dB to the maximum –9.1 dB as the output frequency increasing from 2Mhz to 10MHz. Afterwards, the conversion gain is reduced down to –28.7 dB at 100 MHz output frequency.

7.6.3 1-dB Compression Point

For 1-dB compression point measurement, the setup of the Figure 7.5 is used. The LO input signal is fixed at 910 MHz with a power of 6dBm. The RF input signal is fixed at 900 MHz and a power swept from –48 dBm to 7 dBm.

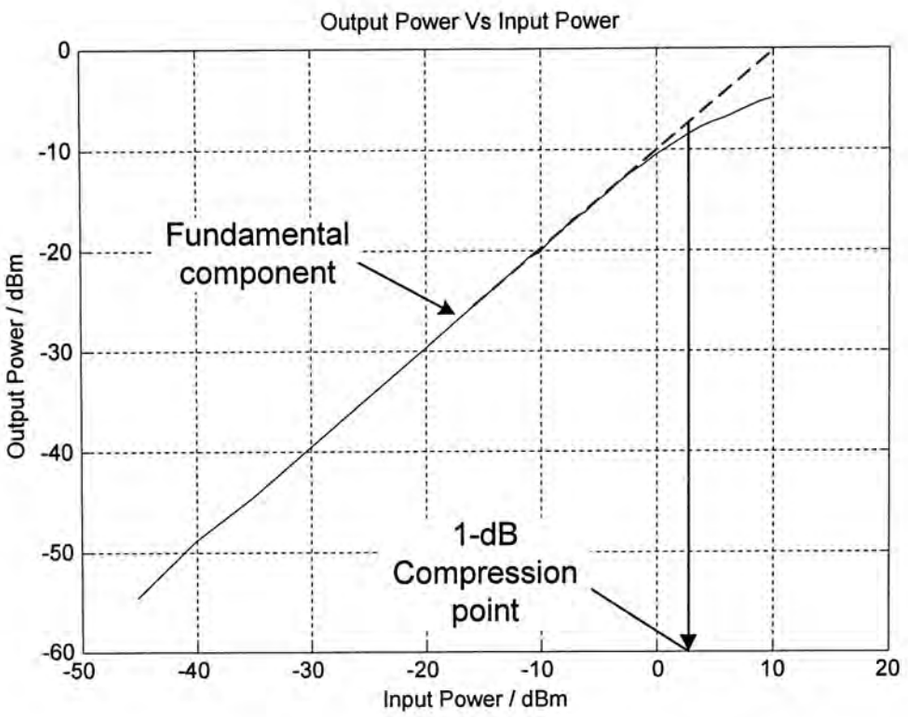


Figure 7.33: Experimental result of the 1-dB compression point

Figure 7.33 shows the measurement result of the 1-dB compression point of the current mode mixer. The 1-dB compression point is about 3 dBm.

7.6.4 IIP3

The experimental setup shown in Figure 7.7 is adopted for measurement of the third-order intercept point (IIP3). The LO input signal is fixed at 910 MHz with a power of 6dBm. Power combiner combines the fixed two-tone RF signals at 900 MHz and 901 MHz with a power swept from –13 dBm to 6 dBm. The noise floor measured from the spectrum analyzer is equal to –76 dBm.

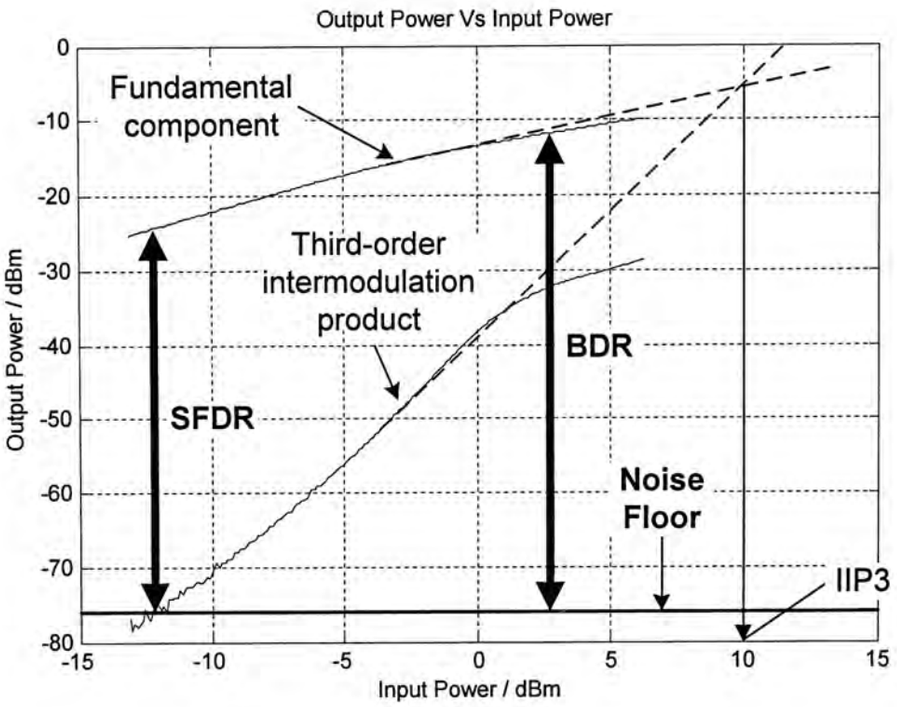


Figure 7.34: Experimental result of the IIP3, SFDR and BDR

The value of the measured IIP3 shown in Figure 7.34 is equal to 10 dBm. Moreover, from Section 2.5.1 it can be realized that the Spurious-Free Dynamic Range (SFDR) of the CMOS Current Mode Mixer is equal to

$$\begin{aligned} \text{SFDR} &= \frac{2}{3}\left(P_{IIP3} - P_{NiFlr}\right) \\ &= \frac{2}{3}\left[10-(-76)\right] \\ &= 57.3\,\text{dB} \end{aligned} \tag{7.5}$$

In addition, the blocking Dynamic Range (BDR) (Section 2.5.2) of the CMOS Current Mode Mixer is equal to

$$\begin{aligned} \text{BDR} &= P_{-1\text{dB}} - P_{\text{NsFlr}} \\ &= 3-(-76) \\ &= 79\,\text{dB} \end{aligned} \tag{7.6}$$

7.6.5 LO Power Effect to the Mixer

The experimental setup for measuring the effect of the LO power on conversion gain is same as that for measuring 1-dB compression point (Figure 7.5) except that instead of sweeping the RF input signal, we swept the LO input signal from –33 dBm to 14 dBm

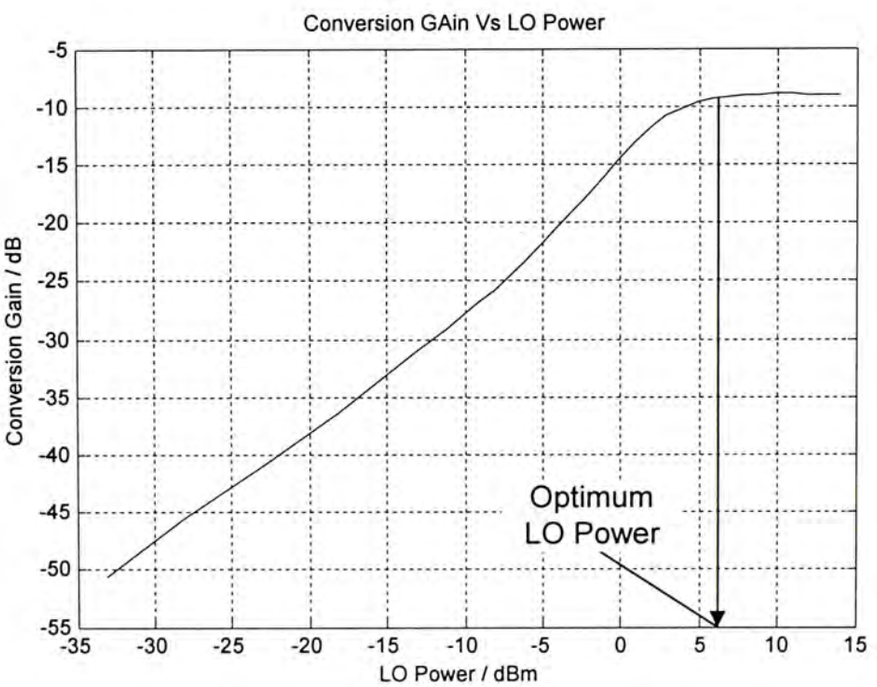


Figure 7.35: Experimental result of the effect of the LO power on conversion gain

From Figure 7.35, it can be found that the optimum LO power is equal to 6 dBm. At LO power below or above 6 dBm, the conversion gain is dropping. It is due to the non-perfect switching of the Gilbert quad pair and the over driven of that CMOS pair.

7.6.6 Performance Summaries of the Current Mode Mixer

Specifications	Value
Supply voltage / V	1.2
Total power consumption / mW	3
LO port impedance / Ω	46.503 – 9.8452j
RF port impedance / Ω	56.754 – 13.42j
LO – IF isolation / dB	24.353
LO – RF isolation / dB	24.72
RF – IF isolation / dB	19.476
Conversion gain / dB	-9.1
1-Db compression point / dBm	3
IIP3 / dBm	10
Active area[(1)] / μm × μm	400 × 400

Table 7.2: Performance summaries of the current mode mixer

[(1)] Excluded the DC blocking capacitor

7.6.7 Discussion

Table 7.2 summaries the performance of the Current Mode Mixer. The measurement result of the circuit shows good conformity to simulation result. The measurement indicates the new current mode mixer has a better linearity compared with the current folded mirror mixer and [[30], [31], [32], [33]]. Moreover, it can be operated by a single AA or AAA battery voltage supply of 1.2 V. The high linearity range of the V-I converter (Figure 5.12) is another important part that provides a large LO and RF current input range to the mixer.

The bonding wire length from the die's pad to the PCB is controlled by myself. Therefore, the phase difference and the voltage attenuation in each bonded wire are carefully controlled.

One drawback of this design is the low conversion gain. However, it can be compensated by adding a post amplifier.

7.7 Measurement Result of the Single-ended to Differential-ended converter

A microphotography and layout drawing of the single-ended to differential-ended converter are shown in Figure 7.36 and Figure 7.37 respectively.

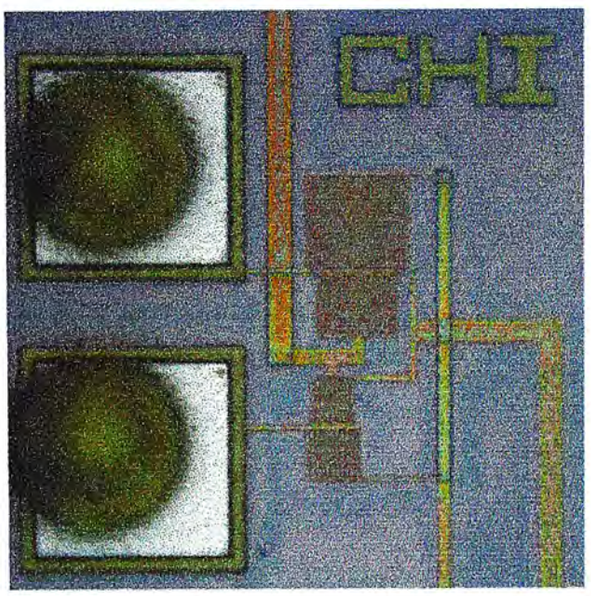


Figure 7.36: Microphotograph of the single-ended to differential-ended converter

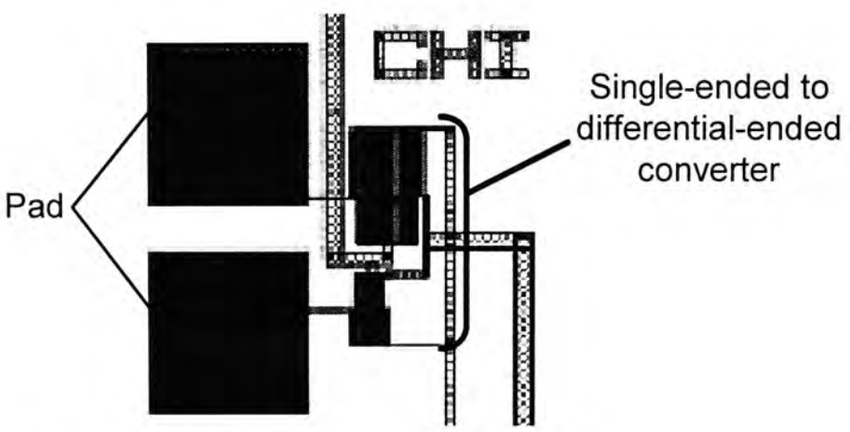


Figure 7.37: Layout drawing of the single-ended to differential-ended converter

The circuit is in a SOP package, which requires a PCB to mount the tested circuit package for high frequency measurement. Figure 7.38 shows the top view of the single-ended to differential-ended converter test board.

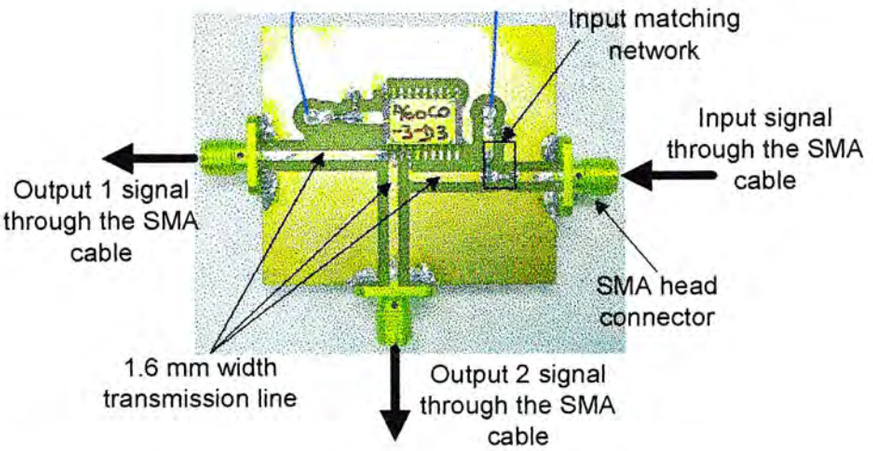


Figure 7.38: Top view of the single-ended to differential-ended converter test board

7.7.1 Measurement Setup for the Phase Difference

For the phase measurement, it is same as the 2-port S-parameter measurement. A S-Parameter test set (HP 85046A) accompanies with a network analyzer (HP 4396A) is used. The connection setup is shown in Figure 7.39.

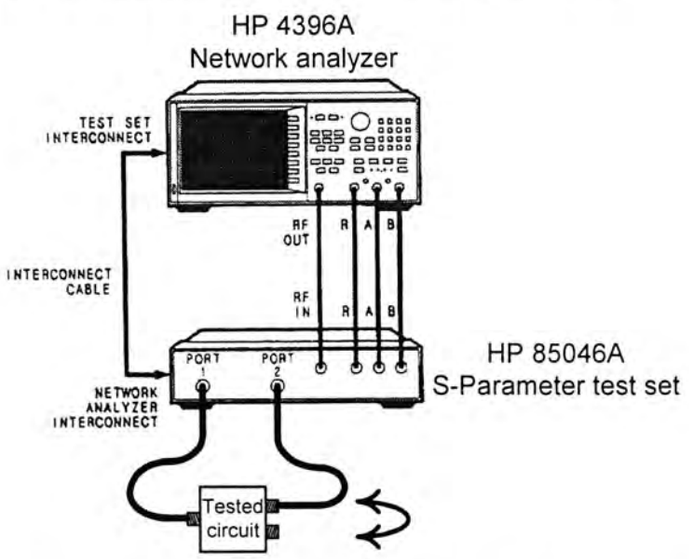


Figure 7.39: The test setup for phase measurement

The Port 1 of the S-Parameter test set is connected to the input port of the tested circuit. The Port 2 is connected to the two output ports of the tested circuit alternately in order to find out its phase value (S_{21}).

7.7.2 Phase Difference Measurement

Figure 7.40 shows the experimental result of the phase difference between the two output ports of the single-ended to differential-ended converter. It gives a 176° phase difference at 900MHz.

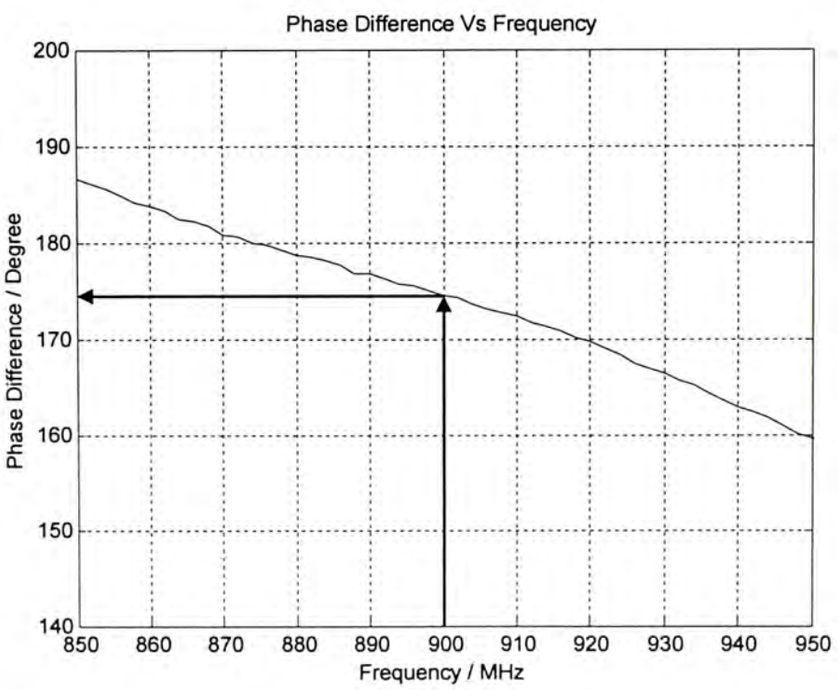


Figure 7.40: Experimental result of the phase difference between two outputs

7.7.3 Discussion

Compared the results between the simulation and the measurement, there are certain amount of the difference. It is due to the non-equal length of the bonding wire from the differential output pads to the two package pins of the SOP package. Therefore, it introduces an uneven phase shift in these two differential output through the unequal length of the bonding wire.

Chapter 8

Conclusion

Two proposed low voltage mixer architectures, **(1) Current Folded Mirror Mixer**, and **(2) Current Mode Mixer**, have been designed, fabricated and tested. The two new architectures reduce the series connected transistors to achieve low voltage operations of **1.5 V** and **1.2 V** voltages supply respectively. Moreover, only simple components, such as CMOS transistor, resistors and DC blocking capacitors are needed. No inductor is needed for the new designs. Thus, these new designs are more suitable for integrable circuits than [[31], [34]]

We use an **AMS© 0.6 μm** technology to fabricate the test circuits. We have found that the measurement results show good conformity to SpectreRF© simulation results. However, the unequal length bond wires from the die to the package pins or the PCB introduce uneven phase shift and voltage attenuation. Fortunately, the uneven bond wires only have minor affect on the performance of the two mixers.

The realized **current folded mirror mixer** achieves an downconverted a 900 MHz input to 10 MHz with a –2.5 dB conversion gain. It consumes 7.5 mW power from a single 1.5 V supply and exhibits a 1-dB compression point of –3 dBm. The IIP3 at 900 MHz is 1 dBm. The active die area is about 250 μm × 300 μm.

The second proposed mixer, **current mode mixer**, gives a better performance

than the first proposed mixer. Moreover, it can operate at 1.2 V. From the experimental results, the current mode mixer downconverts a 900 MHz signal to 10 MHz with a conversion gain of –9.1 dB. It consumes 3 mW power from a single 1.2 V supply exhibits a 1-dB compression point of 3 dBm. The measured IIP3 is 10 dBm. The active die area is about 400 μm × 400 μm.

We have designed two new low voltage mixers, which have compatible or better performance than other published mixers. To our knowledge, these are the first mixer architectures use current input instead of voltage.

Appendix A

Characteristics of the Gilbert Quad Pair

A.1 Large-Signal Analysis

The schematic of the Gilbert quad pair in Figure 4.4 and Figure 4.9 are reproduced in Figure A.1 for convenience.

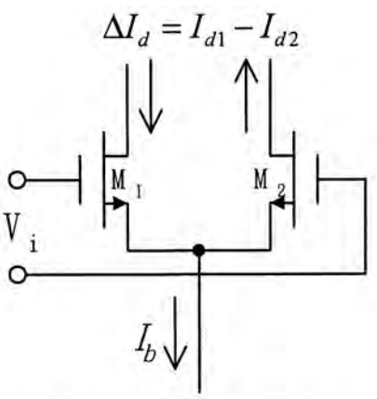


Figure A.1: Schematic of a Gilbert quad pair

Assuming the aspect ratios of M_1 and M_2 are $(W/L)_1$ and $(W/L)_2$ respectively, the drain currents of M_1 and M_5 in the saturation region can be written as,

$$I_{d1} = \frac{K_n}{2}\left(\frac{W}{L}\right)_1 (V_{G1} - V_S - V_t)^2 \quad \text{(A.1)}$$

$$I_{d2} = \frac{K_n}{2}\left(\frac{W}{L}\right)_2 (V_{G2} - V_S - V_t)^2 \quad \text{(A.2)}$$

where V_G and V_S are the gate and the source potentials of the transistor respectively and $K_n = \mu_n C_{ox}$, and the body effect has been neglected in the derived.

By expressing the input differential voltage as,

$$V_i = V_{G1} - V_{G2} \tag{A.3}$$

and writing the drain current in term of the biasing current I_b,

$$\begin{aligned} I_b &= I_{d1} + I_{d2} \\ I_{d1} &= I_b - I_{d2} \end{aligned} \tag{A.4}$$

By the Equation (A.1), Equation (A.2) and Equation (A.3), it follows that the input voltage becomes,

$$V_i = \sqrt{\frac{I_{d1}}{\frac{K_n}{2}\left(\frac{W}{L}\right)_1}} - \sqrt{\frac{I_b - I_{d1}}{\frac{K_n}{2}\left(\frac{W}{L}\right)_2}} \tag{A.5}$$

Squaring both sides twice and rearranging terms yield the following quadratic equation in I_{d1}

$$4{I_{d1}}^2 - 4I_b I_{d1} + \left[V_i^2 \frac{K_n}{2}\left(\frac{W}{L}\right)_{1,2} - I_b \right]^2 = 0 \tag{A.6}$$

where $(W/L)_1 = (W/L)_2$

Solving the quadratic equation (A.6), we could find the root is equal to,

$$I_{d1} = \frac{1}{2} I_b + \frac{K_n}{4} V_i \sqrt{4\left(\frac{W}{L}\right)_{1,2} \frac{I_b}{K_n} - \left(\frac{W}{L}\right)_{1,2}^2 V_i^2} \tag{A.7}$$

By inverting the sign of the second term in Equation (A.7), the drain current of M_2 can be obtained. As a result, the transfer characteristics of the Gilbert quad pair is

given by,

$$\Delta I_d = I_{d1} - I_{d2} = \frac{K_n}{2} V_i \sqrt{4\left(\frac{W}{L}\right)\frac{I_b}{K_n} - \left(\frac{W}{L}\right)^2 V_i^2} \qquad \text{(A.8)}$$

Appendix B

Characteristics of the V-I Converter

B.1 Large-Signal Analysis

The schematic of the symmetric V-I Converter in Figure 4.11 is reproduced in Figure B.1 for convenience.

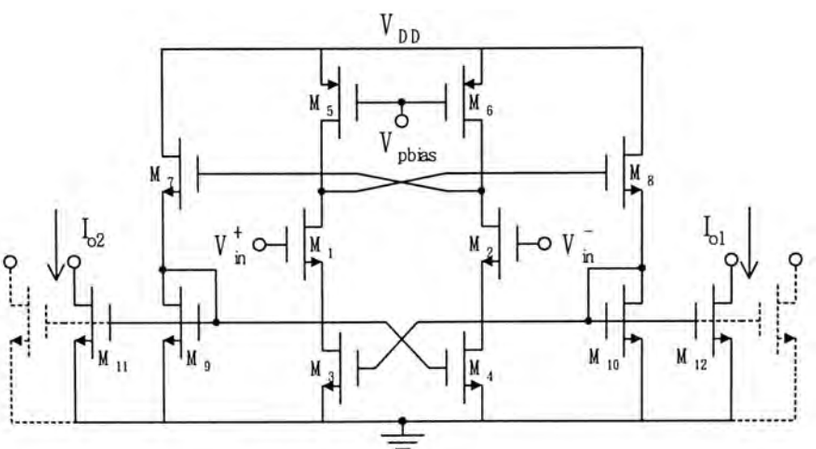


Figure B.1: The V-I Converter

Since the transistor M_1 and M_2 are biased in a saturation region, their differential current can be written as,

$$I_{d1} - I_{d2} = K_n\left(V_{in}^{+} - V_{tn1}\right)^2 - K_n\left(V_{in}^{-} - V_{tn2}\right)^2 \qquad \text{(B.1)}$$

where $V_{tn1} = V_{tn2}$ and $K_n = \frac{1}{2}\mu_n C_{ox}\left(\frac{W}{L}\right)_{1,2}$, by direct expanding of the Equation (B.1)

$$I_{d1} - I_{d2} = 2K_n(V_{CM} - V_{tn})V_d \tag{B.2}$$

where $V_d = V_{in}^+ - V_{in}^-$ and $V_{CM} = \frac{V_{in}^+ + V_{in}^-}{2}$

For the transistor M_5 and M_6 are biased in triode region, there differential current can be written as,

$$I_{d5} - I_{d6} = K_p\left[2(V_{pbias} - V_{tp5})(V_{DD} - V_1) - V_{DS}^2\right] - 2K_p\left[(V_{pbias} - V_{tp6})(V_{DD} - V_2) - V_{DS}^2\right] \tag{B.3}$$

where $V_{tp5} = V_{tp6}$ and $K_n = \frac{1}{2}\mu_p C_{ox}\left(\frac{W}{L}\right)_{5,6}$, by direct expanding of the Equation (B.3)

$$I_{d5} - I_{d6} = 2K_p(V_{pbias} - V_{tp})(V_2 - V_1) \tag{B.4}$$

From the Figure B.1, the transistor M_5 and M_6 is directly cascode connected to M_1 and M_2 respectively. Therefore the Equation (B.1) equal to Equation (B.4)

$$2K_n(V_{CM} - V_{tn})V_d = 2K_p(V_{pbias} - V_{tp})(V_2 - V_1)$$

$$V_2 - V_1 = \frac{K_n(V_{CM} - V_{tn})}{2K_p(V_{pbias} - V_{tp})}V_d \tag{B.5}$$

The voltage V_1 and V_2 would bias the transistor M_7 and M_8 in a saturation region. Therefore, the finalized differential output current is equal as,

$$I_{out} = I_{d8} - I_{d7} = K_n'(V_1 - V_{tn8})^2 - K_n'(V_2 - V_{tn7})^2 \quad \text{(B.6)}$$

where $V_{tn7} = V_{tn8}$ and $K_n' = \frac{1}{2}\mu_n C_{ox}\left(\frac{W}{L}\right)_{7,8}$, by direct expanding of the Equation (B.6) and substitute back the Equation (B.5). We could get

$$I_{out} = I_{d8} - I_{d7} = \frac{K_n K_n'(V_{CM} - V_{tn})(V_1 + V_2 - 2V_{tn})}{K_p(V_{pbias} - V_{tp})} V_d \quad \text{(B.7)}$$

Bibliography

[1] Karanicolas, Andrew N., "A 2.7 V 900 MHz CMOS LNA and mixer." Solid-State Circuits Conference, Digest of Technical Papers, 42nd ISSCC, IEEE International, 1996, Page(s): 50 – 51, 416

[2] Kinget, P.R.; Steyaert, M.S.J., "A 1-GHz CMOS up-conversion mixer," Solid-State Circuits, IEEE Journal of, Volume: 32 Issue: 3, March 1997, Page(s): 370 – 376

[3] Rezavi, B., "A 1.5 V 900 MHz downconversion mixer," Solid-State Circuits Conference, Digest of Technical Papers, 42nd ISSCC, IEEE International, 1996, Page(s): 48 –49

[4] Chung-Yu Wu; Shuo-Yuan Hsiao, "The design of a 3-V 900-MHz CMOS bandpass amplifier," Solid-State Circuits, IEEE Journal of, Volume: 32 Issue: 2, Feb. 1997, Page(s): 159 – 168

[5] Duncan, R.; Martin, K.W.; Sedra, A. S., "A Q-enhanced active-RLC bandpass filter," Circuits and System II: Analog and Digital Signal Processing, IEEE Transactions on, Volume: 44 Issue: 5, May 1997, Page(s): 341 – 347

[6] De Muer, B.; Itoh, N.; Borremans, M.; Steyaert, M., "A 1.8 GHz highly-tunable low-phase-noise CMOS VCO," Custom Integrated Circuits Conference, 2000. CICC, Proceedings of the IEEE 2000, Page(s): 585 –588

[7] Sato, A. Ohara; Y. Ogawa; M. Suzuki, "Lock-in amplifier with autotracking bandpass filter," Review of Scientific Instruments, Volume: 67, November 1996, Page(s): 4021 - 4022

[8] J. H. Scofield, "Frequency-domain description of lock-in amplifier," American Journal of Physics, Volume: 62, February 1996, Page(s): 129 – 133

[9] Rofougaran, A.; Chang, J.Y. –C.; Rofougaran, M.; Abidi, A.A., "A 1 GHz CMOS RF front-end IC for a direct-conversion wireless receiver," Solid-State Circuits, IEEE Journal of, Volume: 31 Issue: 7, July 1996, Page(s): 880 – 889

[10] J. Craninckx; M. Steyaert, "Wireless CMOS frequency synthesizer design," Kluwer Academic Publishers, 1st Edition, 1998, Page(s): 6 – 8

[11] L. Lessing, "Man of High Fidelity: Edwin Howard Armstrong," a biography, New York: Bantam Books, 1969

[12] Jan Crols; Michel S. J. Steyaert, "A signle-chip 900 MHz CMOS receiver front-end with a high performance low-IF topology," Solid-State Circuits, IEEE Journal, Vol. 30, No. 12, December 1995

[13] Abidi, A. A., "Direct-conversion radio transceivers for digital communications," Solid-State Circuits, IEEE Journal of, Volume: 30 Issue: 12, Dec. 1995, Page(s): 1399 – 1410

[14] Rudell, J.C.; Ou, J. – J.; Cho, T. B.; Chien, G.; Brianti, F.; Weldon, J. A.; Gray, P. R., "A 1.9-GHz wide-band IF double conversion CMOS receiver for cordless telephone applications," Solid-State Circuits, IEEE Journal of, volume: 32 Issue: 12, Dec. 1997, Page(s): 2071 – 2088

[15] Thomas H. Lee, "The Design of CMOS radio-frequency integrated circuits," Cambridge University Press, 1998

[16] Kimura, K., "An MOS four-quadrant analog multiplier based on the multitail technique using a quadrtail cell as a multiplier core," Circuits and Systems I: Fundamental Theory and Applications, IEEE Transactions on, Volume: 42 Issue: 8, Aug. 1995, Page(s): 448 – 454

[17] Ramirez-Angulo, J.; Ming-Shen, S., "The folded Gilbert cell: a low voltage high performance CMOS multiplier," Circuits and systems, 1992, Proceedings of the 35th Midewest symposium on 1992, Page(s): 20 –23 vol.1

[18] Seugwook Lee; Changsik Yoo; Wonchan Kim; Hyun-Kyu Ryn; Wonchul Song, "1 GHz COMS down-conversion mixer," Consumer Electronics, ISCE 97, Proceedings of 1997 IEEE International Symposium on 1997, Page(s): 125 – 127

[19] Crols, J.; Steyaert, M. S. J., "A 1.5 GHz highly linear CMOS downconversion mixer," Solid-State Circuits, IEEE Journal, Volume: 30, Issue: 7, July 1995, Page(s): 736 – 742

[20] G. Giustolisi; G. Palmisano; G. Palumbo; T. Segreto, "1.2-V CMOS op-amp with a dynamically biased output stage," Solid-State Circuits, IEEE Journal, Volume: 35, NO. 4, April 2000

[21] G. Fraello; G. Palmisano, "Low voltage folded-mirror mixer," Electronics Letters, Voluem: 33, No. 21, 9th October 1997

[22] G. Glustolisi; G. Palmisano; G. Palumbo; C. Strano, "A novel 1.5-V CMOS mixer," VLSI, Proceedings of the 8th Great Lakes Symposium, 1998, Pages(s): 113 –117

[23] Tsuneo Tsukahara; Masayuki Ishikawa; Masahiro Muraguchi, "A 2 V 2 GHz Si-bipolary direct-conversion quadrature modulator," Solid-State Circuits Conference, IEEE International, 1994

[24] Chan, C.F.; Hok-sun Ling; Choy, O. "A one volt four-quadrant analog current mode multiplier cell," Solid-State Circuits, IEEE Journal of, Volume: 30 Issue: 9, Sept. 1995, Page(s): 1018 - 1019

[25] Chi-Hung Lin; Ismail M.; Pimenta T., "A 1.2 V micropower CMOS class-AB V-I converter for VLSI cells library design," Circuits and Systems, Proceedings, 1998 Midwest Symposium, 1999, Page(s): 364 – 367

[26] Lin, C. –H.; Ismail, M., "Design and analysis of an ultra low-voltage CMOS class-AB V-I converter for dynamic range enhancement," Circuits and Systems, ISCAS '99, Proceedings of the 1999 IEEE International Symposium, Volume: 2, 1999, Page(s): 21 – 24

[27] Mohammed Ismail; Terri Fiez, "Analogy VLSI: Signal and Information Processing," McGraw – Hill, Inc., 1994

[28] Stephen A. Maas, "Microwave Mixer," Artech House, Inc., 1986

[29] Gonzalez, Gillermo, "Microwave transistor amplifiers: analysis and design," Prentice Hall, 1984, Page(s): 141 - 152

[30] Andrew N. Karanicolas, "A 2.7-V 900-MHz CMOS LNA and mixer," Solid-State Circuits, IEEE Journal, Vol. 31, NO. 12, December 1996

[31] Ari Vauhkonen; Esa Tarvainen, "Inductors allow low-voltage performance for IC mixers," Electronics, Circuits and systems, 1998 IEEE International Conference, Volume: 1, 1998, Page(s): 329 – 332

[32] P. J. Sullivan; B. A. Xavier; W. H. Ku, "Low voltage performance of a microwave CMOS Gilbert cell mixer," Solid-State Circuits, IEEE Journal, Vol: 32, No. 7, July 1997

[33] Jacob Pihl; Kare Tais Christensen; Erik Bruun, "Direct downconversion with switching CMOS mixer," Circuits and Systems, ISCAS 2001, The 2001 IEEE International Symposium, Volume: 1, May 2001, Page(s): 117 –120

[34] Leonard A. MacEachern; Eyad Abou-Allam; Lan Wang; Tajinder Manku, "Low voltage mixer biasing using monolithic integrated transformer de-coupling," Circuits and Systems, ISCAS 99, Proceedings of the 1999 IEEE International Symposium, Volume:2, 1999