RF CMOS Quadrature Voltage-controlled Oscillator Design using Superharmonic Coupling Method

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In modern transceiver architectures, quadrature local oscillator signals are required for performing image-rejection or vector modulation and demodulation. There are mainly three different methods to generate quadrature signals on chip, a) a differential oscillator followed by a quadrature divided-by-two divider, b) using a polyphase filter, and c) quadrature voltage-controlled oscillator (QVCO). The former two methods have the drawbacks of low operating frequency and high insertion loss. Therefore, it is common to generate quadrature signals from the mutual coupling between two differential oscillators as in QVCO design.

However, the coupling mechanisms used in QVCO, such as parallel-coupled and series-coupled are found to suffer from several drawbacks. The oscillator output at the fundamental frequency suffers from poor phase noise performance and lower oscillating frequency due to the presence of the extra coupling transistors. Super-harmonic coupling using a transformer to couple the second harmonic of two oscillators alleviates the above problems at the cost of chip area.

This thesis presents the design of a fully-integrated QVCO using CMOS technology for low-voltage, low power and high-frequency operation. The proposed QVCO employs the super-harmonic coupling through the back-gate injection instead of a transformer. The main objective of the proposed QVCO design is to develop a coupling mechanism without extra coupling transistor to generate qradrature signals. Also, this mechanism should benefit both the QVCO noise performance and higher oscillation frequency. For demonstration, the proposed QVCO is designed to operate at 5-GHz frequency range and is fabricated using 0.35μm standard CMOS process. Experimental results show that the QVCO core consumes 4mA at 1-V supply voltage. The measured phase noise is –111dBc/Hz at 1-MHz offset. The figure-of-merit (FoM) of the QVCO is 179dBc/Hz. The quadrature accuracy of the QVCO is verified by employing an integrated passive mixer.

摘要

在現代積體電路結構中，正交本地振盪器信號必需用作爲執行鏡頻抑制或調制和解調。在芯片中，主要有三個不同的方法產生正交信號，a) 一個差分振盪器被二分頻器跟隨，b) 使用多相過濾器，和 c) 正交壓控振盪器(QVCO) 。前二個方法有低操作頻率和高插入損耗的缺點，所以通常使用正交壓控振盪器中的兩個差分振盪器之間之相互耦合來產生正交信號。

不過，正交壓控振盪器中的耦合機制，例如平行耦合和串聯耦合都有著不同的缺點。由於額外耦合晶體管的出現，振盪器在基頻的輸出遭受差劣的階段噪聲表現和振盪頻率下降的問題。超級諧波耦合使用佔較大芯片面積的變壓器耦合兩個振盪器的第二諧波以緩和上述問題。

這份論文提出使用 CMOS 技術的高度整合正交壓控振盪器的設計來用作低電壓、低功率和高頻率操作。提出的正交壓控振盪器使用超級諧波耦合通過背門注入代替變壓器。提出的正交壓控振盪器設計的主要宗旨將開發一個沒有額外耦合晶體管的耦合機制沒來產生正交信號。並且，這個機制應該有利於正交壓控振盪器噪聲表現和更高的振盪頻率。提出的正交壓控振盪器被使用標準 0.35μm CMOS 製程製造，並設計在五千兆赫頻率範圍操作。實驗結果表示正交壓控振盪器的核心在 1V 電壓消耗 4mA。階段噪聲是 -111dBc/Hz 在 1 兆赫頻率偏置。正交壓控振盪器的價值參數(FoM) 是 179dBc/Hz 。正交壓控振盪器的正交相準確性使用一個聯合被動攪拌器作量度。

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Chapter 1

Introduction

1.1 Motivation

The market of mobile communication has expanded world-wide over the last decade. The evolution in microelectronics played critical roles in the boom of mobile communications. Much research has been focusing on the fully integrated solution of transceiver for various wireless applications, such as GSM, GPS and Bluetooth. Different circuit blocks in the radio frequency (RF) front-end including phase-locked loop, low noise amplifier and mixer, can now be implemented on-chip using complementary-metal oxide semiconductor (CMOS) technology. The growing demand from end-user applications like video-streaming and wireless data-link requires higher data -rate wireless connection which pushes operating frequency up to the 5 GHz range. IEEE Wireless Local Area Network (WLAN) offers standards like 802.11a to support higher data-rate at 5-GHz ISM band.

Meanwhile, continuing advances in the CMOS technology have allowed low-cost realization of transceiver designs in the multi-gigahertz frequency range. Lower cost per unit is the main drive for fully-integrated design including the voltage-controlled oscillator (VCO). However, the design of fully-integrated VCO is

not easy since there is no systematic design flow from specification to implementation. One of the main obstacles for designing high performance VCO is the low quality factor (Q-factor) of on-chip inductor due to the substrate loss. The resonator constructed by the low Q-factor inductor could affect the performance of a VCO in terms of poor phase noise.

Quadrature signals can be obtained on chip mainly by three different approaches, a) a differential oscillator followed by a quadrature divided-by-two divider, b) using a polyphase filter, and c) quadrature voltage-controlled oscillator (QVCO). The former two methods have the drawbacks of low operating frequency and high insertion loss respectively. Quadrature outputs can be obtained by employing proper coupling between two differential VCOs. A quadrature VCO (QVCO) consists of two differential VCOs and a coupling network. Due to the additional active devices embedded in the coupling network, overall performance of QVCO such as phase noise is inherently degraded in compared to differential VCO. In addition, the supply voltage of integrated circuits based upon advanced CMOS technologies must also be proportionately reduced so as not to damage the thin gate-oxide layer of the active devices. The reduced supply voltage poses new challenges in QVCO design with stacked transistors. The output voltage swing of a VCO therefore is limited by the supply voltage, which leads to degraded phase noise

performance of a VCO. The stringent phase noise requirement in LO design implies the need of a new coupling architecture which can operate at reduced supply voltage and consumes less lower power.

In this work, the design of a QVCO using novel coupling method with the second harmonics is presented. By this method, QVCO can be designed for low voltage and low power applications, while at the same time operating at higher frequency. As part of the research, a fully-integrated QVCO based upon the proposed superharmonic coupling method is implemented using 0.35um standard CMOS technology.

1.2 Receiver Architecture

The traditional superheterodyne receiver down-converts a RF signal to baseband in two or more mixer stages. A mixer in each stage down-converts the received signals to an intermediate-frequency (IF) for amplification and finally demodulation. The IF is defined as $|f_{LO} - f_{RF}|$. The main disadvantage of superheterodyne receiver is the image problem. After down-conversion, image signal falls into the same frequency as the desired signal. Figure1-1 shows the image problem for low-side injection. The image frequency, f_{IM}, locates at one IF frequency apart from the LO frequency $(f_{IM} = f_{LO} - f_{IF} = f_{RF} - 2f_{IF})$ for low-side injection. Image rejection

and channel selection are therefore required to attenuate unwanted signals before mixing. These processes require high quality-factor (Q-factor) resonators and multiple resonators in order to meet the stringent filter requirements. The low Q-factor of on-chip inductors results in prohibitively high passband insertion loss for multiple-poled integrated LC filters. Furthermore, since monolithic inductors and capacitors require large die area, these LC filters can become excessively large for on-chip integration.

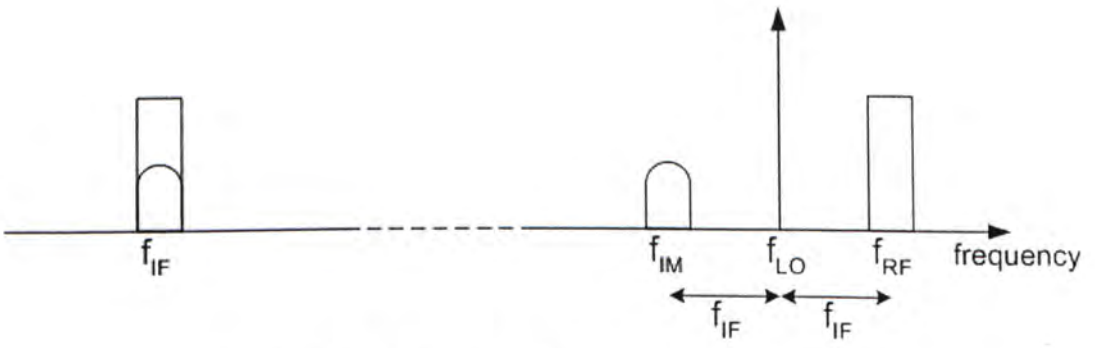


Figure 1-1 Image problem in superheterodyne receiver

1.2.1 Zero-IF Receivers

An alternative to the multi-stage superheterodyne approach is to down-convert the signal directly from RF to baseband, i.e. $f_{LO} = f_{RF}$ or $f_{IF} = 0$. This approach is known as zero-IF, direct conversion, or homodyne [1][2]. Since the signal is its own image, image rejection filters can be completely eliminated. In addition, channel selection can be performed at baseband, further reducing filter requirements. The

elimination of off-chip filters allows zero-IF receivers to attain a higher level of integration for the RF front-end.

Despite the above advantages, zero-IF receivers present several obstacles making them challenging to implement [3]. One of these problems is known as self-mixing. LO leakage may be transmitted to the RF input of the mixer through the LNA, the IC package, or the antenna. Since the LO is at the same frequency as the RF signal in direct-conversion receiver, the LO leakage may be picked up and amplified by the LNA, and mix with the strong LO signal to create a DC offset. Self-mixing can also occur when a large interferer leaks from the RF path to the LO input of the mixer. These DC offsets may be difficult to eliminate; in some cases they may vary with time due to changes in the LO reflections or interferers as the receiver itself or objects in the surrounding environment move.

In addition, low frequency noise makes it difficult to achieve low noise figure in zero-IF receivers. The low frequency noise of transistors is called "1/*f* noise" because it has a 1/*f* slope versus frequency. For Zero-IF, this results in higher receiver noise figures because the output frequency of the mixers lies within the 1/*f* noise region. More noise at the receiver output requires more gain and lower noise figure in the components at the input to attain the required overall noise figure for a particular application.

Another implementation challenge for zero-IF receivers is in-phase and quadrature (I/Q) mismatch. Direct conversion requires the signal down-converted into separate I and Q channels to recover the negative and positive frequency components of the signal. If the gain and phase of these two channels are not identical, the output of the receiver will have an I/Q mismatch, resulting in errors for the recovery of the transmitted data.

1.2.2 Low-IF Receivers

The low-IF receiver is an alternative to the zero-IF receiver which avoids the problems of DC offsets and $1/f$ noise, but still allows a high degree of integration [4][5]. As in a superheterodyne receiver, the RF and LO inputs to the down-conversion mixer of a low-IF receiver differ in frequency by a non-zero IF. However, low-IF receivers have an IF low enough to be easily sampled by an analog-to-digital converter (ADC). Once in the digital domain, the signal can be filtered and converted to baseband using a DSP.

On the other hand, low-IF receivers, while avoiding DC offset issues, have the same image problem as superheterodyne architecture. To deal with the image problem, Hartley and Weaver architectures can be used for low-IF receivers to avoid the need

for expensive off-chip image-reject filters. These image rejection architectures are not typically used for conventional receivers due to design limitations involving the bandpass and lowpass filters. Inductor and capacitor values for passive filters at the IF are too large to be implemented on-chip, so operational amplifier based active filters should be used. However, IF frequency in superheterodyne receiver exceeds the unity gain frequency of standard operational amplifiers. By decreasing the IF to a suitable range for the operational amplifier, active filters can be used in low-IF receivers to implement either the Hartley or Weaver image rejection architectures.

1.2.2.1 Hartley Architecture

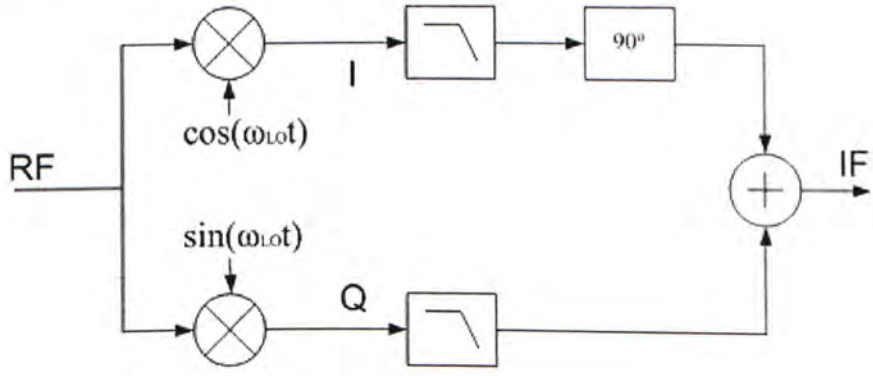


Figure 1-2 Hartley image-reject receiver

The Hartley architecture employs quadrature mixers that separate the signal into I and Q channels, as shown in figure1-2. The branches undergo a relative 90° phase shift and the two channels are summed to produce an image-free output. This is implemented in practice with a RC-CR or polyphase network.

Assuming low-side injection, the input is $x(t) = A\cos(\omega_{rf}t) + B\cos(\omega_{im}t)$, where $\omega_{im} = \omega_{rf} - 2\omega_{IF}$ and ω_{rf} is the signal frequency. After mixing with the quadrature LO, the output of the low-pass filters is:

$$x_{I,LPF}(t) = \frac{A}{2}\cos(\omega_{rf} - \omega_{LO})t + \frac{B}{2}\cos(\omega_{LO} - \omega_{im})t \qquad (1.1)$$

$$x_{Q,LPF}(t) = \frac{A}{2}\sin(\omega_{rf} - \omega_{LO})t - \frac{B}{2}\sin(\omega_{LO} - \omega_{im})t \qquad (1.2)$$

A phase shift 90° of is introduced, by making use $\cos(\omega + 90^{o}) = \sin(\omega)$, and equation (1.1) becomes

$$x_{I,90}(t) = \frac{A}{2}\sin(\omega_{rf} - \omega_{LO})t + \frac{B}{2}\sin(\omega_{LO} - \omega_{im})t \qquad (1.3)$$

Finally, summing equations (1.2) and (1.3) results in an image-free output:

$$x_{IF}(t) = A\sin(\omega_{rf} - \omega_{LO})t$$

The image rejection ratio (IRR), a measure of the receiver's ability to suppress images, depends on the accuracy of the 90° phase shift over signal bandwidth and the gain balance of the I and Q channels.

1.2.2.2 Weaver Architecture

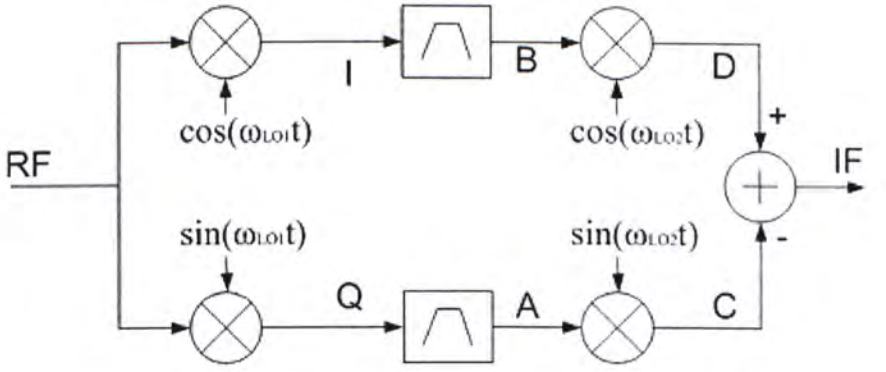


Figure 1-3 Weaver image-reject receiver

The Weaver architecture also has quadrature mixers to separate I and Q channels, but uses two IF stages, as shown in figure1-3. A second set of mixers is used to process the image through the I and Q channels so that it is cancelled out at the output summer at the second IF. Illustrated in figure1-3, the spectrum at point A is convolved with $j[\delta(\omega+\omega_{LO2})-\delta(\omega-\omega_{LO2})]/2$, yielding at point C the translated replicas with no factor j. Similarly, the spectrum at point B is convolved with $j[\delta(\omega+\omega_{LO2})+\delta(\omega-\omega_{LO2})]/2$ and hence is translated both up and down in frequency. Subtracting the spectrum at point C from that at point D, the replicas of the image that fall in the band of interest cancel each other, yielding the desired signal with no corruption. The IRR of the Weaver architecture depends on the gain and phase balance of the I and Q channels.

1.3 Image-rejection ratio

Due to the limitation of the measurement set-up, it is difficult to measure the phase accuracy in time domain at GHz frequency range. Instead of directly measuring at the oscillator output in time-domain, the image rejection ratio (IRR) is measured at frequency-domain to access the phase accuracy. The relationship between IRR and phase error is denoted by

$$IRR = \frac{(\Delta A / A)^2 + \theta^2}{4} \qquad (1.4)$$

where $\Delta A/A$ is the relative gain mismatch

θ is the phase mismatch

By using a single-sideband (SSB) mixer, the phase accuracy of a quadrature LO signal can be evaluated by measuring the desired band and image band signals in the up-converted frequency band. Figure1-4 shows the relationship between IRR and phase error with different relative gain mismatch.

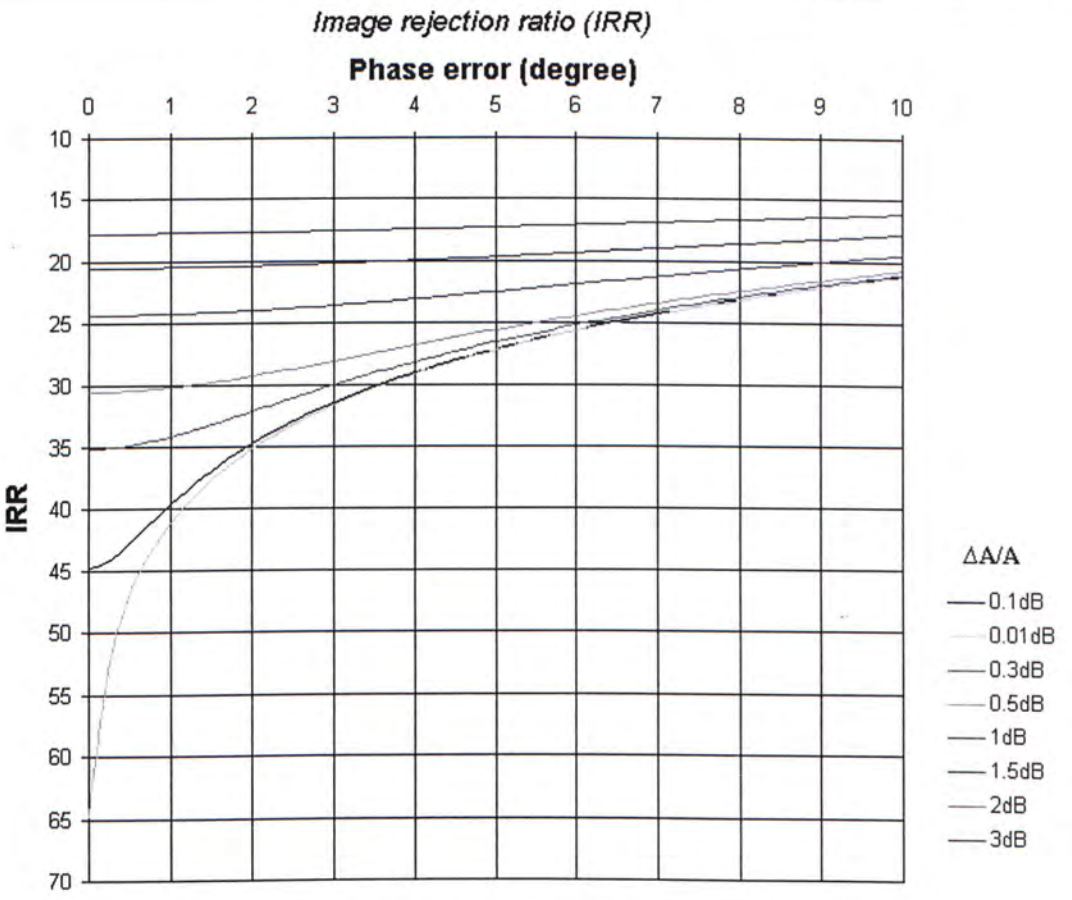


Figure 1-4 IRR caused by phase and amplitude mismatch

1.4 Thesis Organization

Chapter 1 discusses the motivation of this work and the importance of quadrature LO signal in modern transceiver architecture. Chapter 2 presents the basic oscillator theory and the implementation of on-chip components such as varactor and inductor. Two different phase noise models are also discussed in this chapter. Chapter 3 describes different topologies of fully-integrated oscillator, followed by conventional QVCO designs and their drawbacks. A new QVCO design using back-gate superharmonic coupling is proposed with in-depth discussion on circuit design and layout consideration. For comparison, simulation results of both proposed and parallel-coupled QVCO are presented. Chapter 4 describes the experimental results of the proposed and conventional QVCO. A comparison with recently published works is also provided. Finally, conclusions are given in chapter 5 with the recommendation for future research.

Chapter 2

Fundamentals of oscillator

2.1 Basic Oscillator Theory

Barkhausen's two-port model of an oscillator represetns the LC-VCO as an active element or amplifier *G* and a feedback network *H*, as shown in figure 2-1, where the $G(V, j\omega)$ represents the transfer function of the amplifier as a function of the input amplitude and angular frequency, and $H(j\omega)$ is the transfer function of the feedback network as a function of frequency. An oscillator must satisfy the Barkhausen's criteria in order to maintain the stable oscillation.

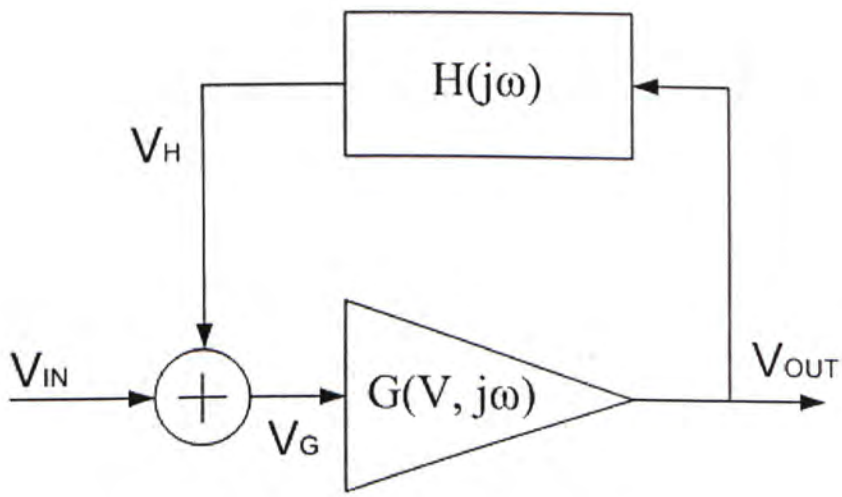


Figure 2-1 Two-port oscillator model

Obviously, when V_G is small, G can be considered as a linear function,

$$V_{OUT} = G(j\omega)V_G \quad \text{and} \quad V_H = H(j\omega)V_{OUT} \qquad (2.1)$$

With

$$V_G = V_{IN} + V_H \qquad (2.2)$$

the transfer function of the complete feedback network is calculated as:

$$\frac{V_{OUT}}{V_{IN}} = \frac{G(j\omega)}{1 - H(j\omega)G(j\omega)} \qquad (2.3)$$

which is unstable if

$$|H(j\omega)||G(j\omega)| \geq 1 \qquad (2.4)$$

As long as the left-hand side of the above expression > 1,oscillation amplitude will grow. Due to non-linear and saturation effects of the amplifier, steady-state amplitude will be reached when:

$$|H(j\omega)||G(j\omega)| = 1 \qquad (2.5)$$

and for the phase

$$\Phi_{G(j\omega)} + \Phi_{H(j\omega)} = 2\pi k \qquad k = 1 \ldots n \qquad (2.6)$$

where $\Phi_{G(j\omega)}$ and $\Phi_{H(j\omega)}$ are respectively the phase of $G(V, j\omega)$ and $H(j\omega)$. Equations (2.5) and (2.6) are known as Barkhausen oscillation criteria.

2.2 Varactor

Varactors are variable capacitors used to change the resonance frequency of a LC resonator. There are different types of varactor, e.g. junction diode and MOS varactor. One of the main parameters for varactor is the C_{max} / C_{min}, which is the ratio to determine the tuning range. Since junction diode features a small C_{max} / C_{min}, MOS varactor is often chosen for oscillator design.

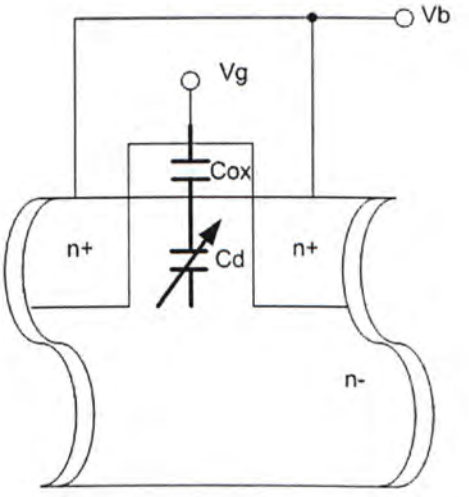


Figure 2-2 A cross-section of an accumulation MOS varactor

Figure 2-2 shows a cross-section of an accumulation-mode MOS varactor[6]. In this type of varactor, the drain/source and the n-well have the same doping type. C_{ox} is the gate oxide capacitance and C_d is the variable depletion region capacitance, thus the variable capacitance, C_v, between the nodes V_g ang V_b can be obtained by

$$\frac{1}{C_v} = \frac{1}{C_{ox}} + \frac{1}{C_d} \qquad (2.7)$$

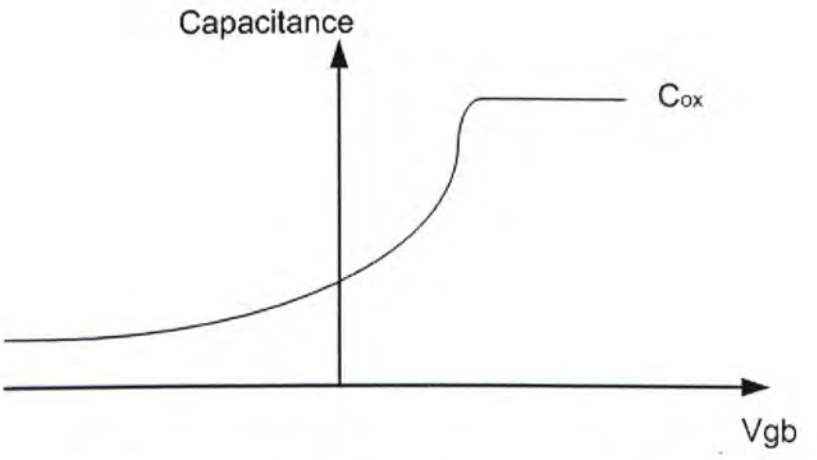


Figure 2-3 Characteristic of an accumulation-mode MOS varactor

Figure2-3 shows the capacitance variation of an accumulation-mode MOS varactor. As V_g increases, the capacitance varies due to the transition from depletion to accumulation. At low V_g, the capacitance of depletion layer and the gate oxide capacitance are in series, resulting a small value of capacitance. At high V_g, the device is in accumulation and the capacitance determined by the gate oxide is in large value. The model of the accumulation-mode MOS varactor is shown in figure2-4, where the R_s is the series resistance of the MOS varactor, C is the gate-bulk capacitance of a varactor, D_w is the diode in depletion capacitance of the well, and Rw is the series resistance of the well.

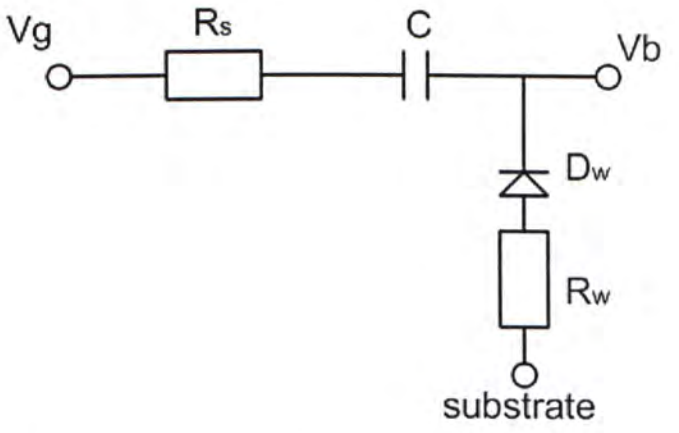


Figure 2-4 Model of accumulation-mode MOS varactor

2.3 Inductor

Inductors can be realized using bondwire or on-chip spiral inductor. The bondwire together with the varactor can form a LC resonator. However, the disadvantages of a bondwire inductor are the inductance variation due to the tolerances of the bonding process and questionable manufacturability. Therefore, on-chip spiral inductor is chosen for integrated oscillator design.

Spiral inductors are usually implemented by using the top metal layers of the process. They can come into different layout structures: squared, octagonal and circular, as shown in figure2-5. Due to the design rule of the foundry, the only structure available is the squared spiral inductor. The inductance of a spiral inductor depends on a number of parameters including the length, the width and the thickness of the metal, the winding spacing and the number of turns[7]. In [8], the

inductance of a spiral inductor is estimated using following equations.

$$L = \frac{\mu n^2 d_{avg} c_1}{2}\left[\ln(\frac{c_2}{\rho}) + c_3\rho + c_4\rho^2\right] \qquad (2.8)$$

$$d_{avg} = \frac{d_{out} + d_{in}}{2}$$

$$\rho = \frac{d_{out} - d_{in}}{d_{out} + d_{in}}$$

where d_{out} and d_{in} are the outer and inner diameter respectively,

ρ is the fill factor,

n is the number of turns,

c_1, c_2, c_3, c_4 are the coefficient obtained by measurement, i.e. for square spiral inductor, c_1=1.27, c_2=2.07, c_3=0.18, c_4=0.13.

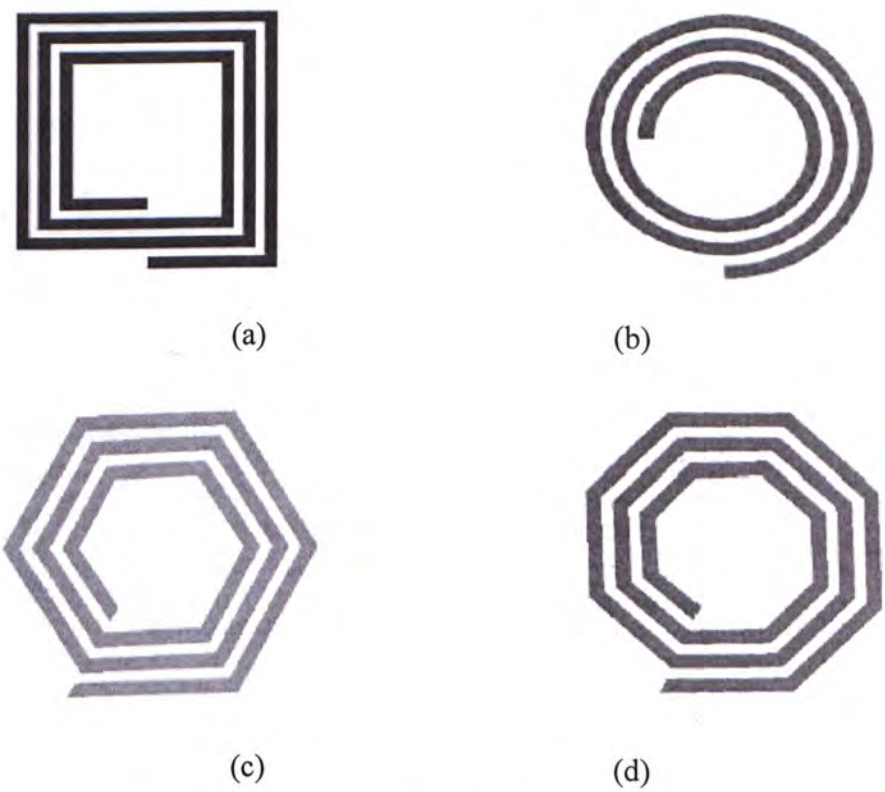


Figure 2-5 Spiral inductor layout (a) squared (b) circular (c) hexagonal (d) octagonal

Accurate modeling of a spiral inductor is difficult and time-consuming. A testchip of different values of spiral inductor occupying large chip area can be used to extract the lumped model from its measured parameters. Figure2-6 shows a π-model of a spiral inductor. The parameters in the lumped model are described as follows:

- L is the inductance
- R_s is the series resistance associated with the metal line and its value depends on the sheet resistance of the metal layer
- C_L is the capacitive coupling between the turns of the inductor
- C_{ox} is the parasitic capacitance between the inductor and substrate
- C_{sub} is the capacitance in the substrate
- R_{sub} is the ohmic losses in the substrate

Fortunately, given the layout of a spiral inductor, fast and acceptable models can be obtained by some simulators, e.g. ASICTIC and FASTHENRY[9].

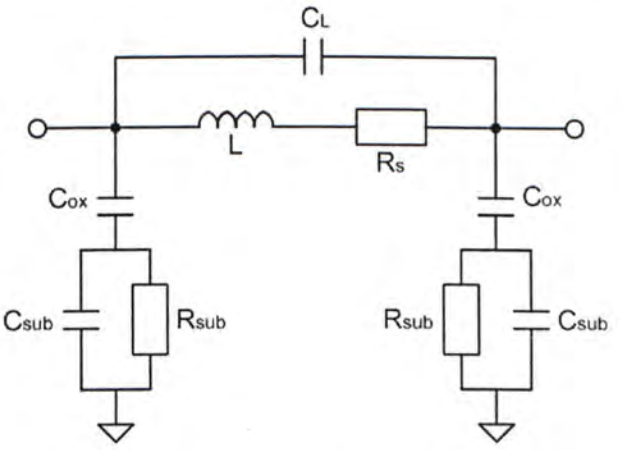


Figure 2-6 π-model of a spiral inductor

The main disadvantage of using on-chip spiral inductor is its low value of quality factor. The main reasons for low Q-factor are the substrate loss and eddy current in the low resistive substrate. To improve the Q-factor of a spiral inductor, the low resistive substrate underneath the spiral inductor can be etched away. However, this method is not cost-effective and another solution is to use patterned ground shield (PGS)[10]. The shield provides a shorted path to ground to prevent the inductor electric field from reaching the substrate eliminating energy dissipation. A solid conductive ground shield between the spiral and the substrate is quite effective for this purpose. However, image current in the shield, induced by the magnetic field of the inductor, flows in a loop with opposite direction to the main current, creating a negative mutual coupling effect to reduce the net magnetic field and thus the overall inductance. Narrow slots orthogonal to the spiral, patterned into shield as shown in

figure 2-7, act to disrupt the path of the induced loop current and prevent this negative mutual coupling. An important negative side effect of the PGS is the additional parasitic capacitance between the inductor and the shield, which acts to increase the capacitor loss factor severely[11].

Figure 2-7 Patterned ground shield for spiral inductor

2.4 Phase noise

The output of an ideal oscillator output is a periodic sinusoidal waveform, and it can be expressed as $v_o = A\sin(\omega_o t)$. However, there is a phase fluctuation in the output signal, such that $v_o = A\sin(\omega_o t + \varphi(t))$. The phase shift φ(t) is called phase noise in frequency domain and jitter in time domain. The oscillator shows the presence of phase noise in the output spectrum in the "skirt" shape instead of an ideal single frequency component, as shown in figure 2-8. Phase noise is usually expressed as the ratio of power at a particular offset frequency from the center frequency to power at the center frequency. And the noise power is measured in a 1-Hz bandwidth at the frequency offset from the carrier.

$$L(\Delta\omega) = \frac{\text{Noise power in 1Hz bandwidth at } \omega_o + \Delta\omega}{\text{Total carrier power at } \omega_o}$$

Phase noise is usually expressed as $L(\Delta\omega)$ and the units of phase noise are dBc/Hz.

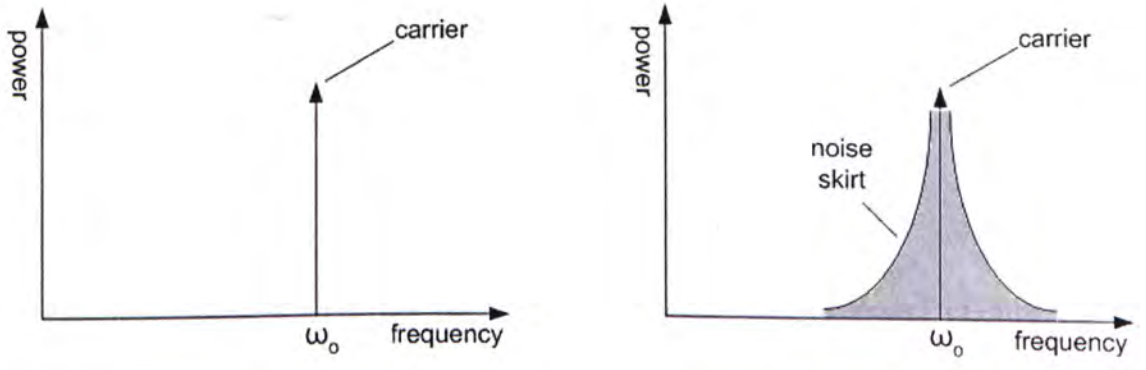


Figure 2-8 a) Ideal oscillator output spectrum b) Practical oscillator output spectrum

Phase noise is one of the most important parameters in the oscillator design. In a receiver, the phase noise deteriorates the signal to noise ratio after down-conversion, as illustrated in figure 2-9. The interfering channel is also down-converted and the associated noise will fall within the bandwidth of desired signal.

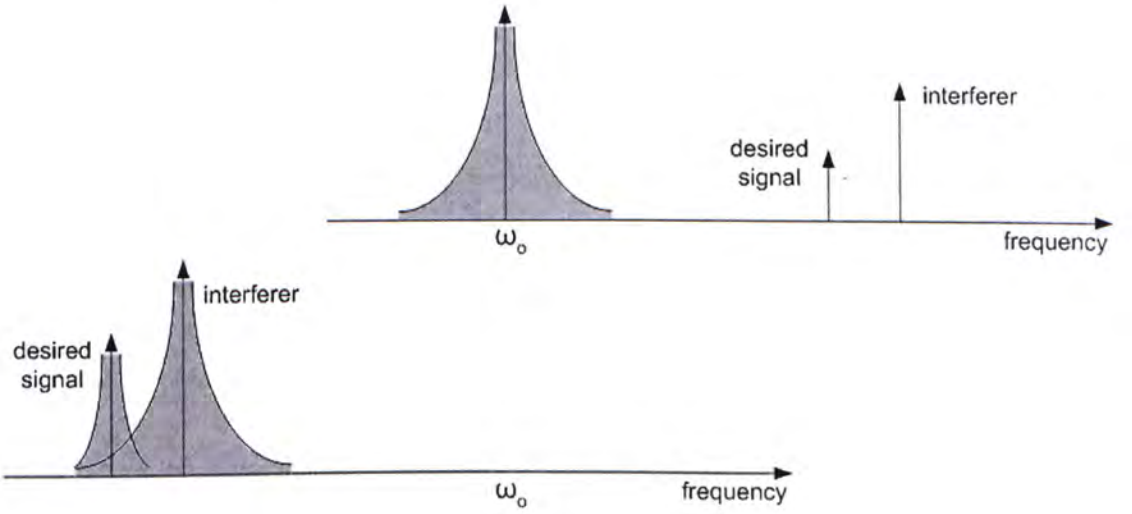


Figure 2-9 Down-conversion of a signal with an interferer in a receiver

Modeling of phase noise in oscillator help circuit design to estimate the circuit performance and provide insights to design trade-offs. In fact, generation of phase noise in an oscillator is a complex process due to the non-linearity of active and passive devices. There are several models of phase noise proposed in different literature and some of the widely accepted phase noise models are described in the next session.

2.4.1 The Leeson's phase noise expression

Leeson[12] proposed an expression for the phase noise of a resonator-based VCO. The phase noise of an oscillator can be calculated using the following expression:

$$L(\Delta\omega) = 10\log\left\{\frac{2FkT}{P_{sig}}\left[1+\left(\frac{\omega_o}{2Q\Delta\omega}\right)^2\right]\left(1+\frac{\Delta\omega_{1/f^3}}{|\Delta\omega|}\right)\right\} \qquad (2.9)$$

where Q is the loaded quality factor of the resonator,

$\Delta\omega$ is the angular frequency offset,

ω_o is the center frequency,

F is the empirical excess noise factor,

P_{sig} is the power of output signal,

$\Delta\omega_{1/f^3}$ is the flicker noise corner frequency,

k is the Boltzman's constant,

T is the absolute temperature

In equation (2.9), phase noise of an oscillator can be divided in two regions of $1/f^2$ and $1/f^3$ in which the phase noise deceases at 20dB and 30dB per decade respectively. From the expression, the phase noise can be reduced by increasing P_{sig} and Q. The output power or output amplitude of a practical oscillator is limited by the power supply voltage. Therefore, the loaded quality factor of the tank plays a

crucial role in the phase noise and a lot of effort has been put in order to increase the loaded quality factor in RF circuit design.

The main disadvantage of this model is the empirical factors of F and $\Delta\omega_{1/f^3}$. These two factors can only be obtained by measurement and this model provides no insight about them in circuit design. Also, it is worth to mention that the flicker noise corner frequency of an oscillator is not same as the device flicker noise corner.

2.4.2 Linear model

The linear LC oscillator model shown in figure 2-10 can provide insights to the Leeson's phase noise expression.

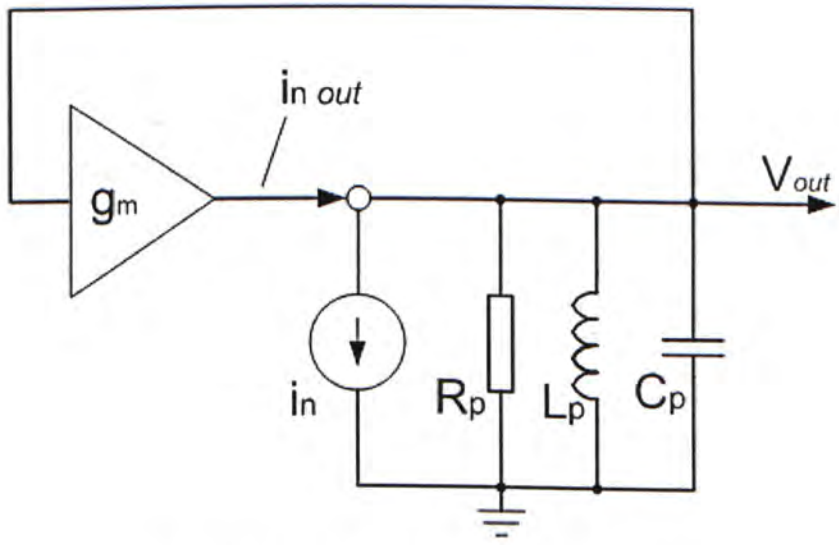


Figure 2-10 Linear LC oscillator model

The impedance of the parallel circuit of *Rp*, *Lp* and *Cp* is expressed as

$$Z_p(j\omega) = \frac{R_p}{1 + jvQ_p} \qquad (2.10)$$

where

$$v = \frac{\omega}{\omega_{osc}} - \frac{\omega_{osc}}{\omega} \qquad (2.11)$$

The closed-loop gain $H_{cl}(j\omega)$ in figure 2-10 can be written as

$$H_{cl}(j\omega) = \frac{g_m Z_p(j\omega)}{1 - g_m Z_p(j\omega)} \qquad (2.12)$$

Substitution of (2.10) in (2.12) yields,

$$H_{cl}(j\omega) = \frac{g_m R_p}{1 + jvQ_p - g_m R_p} \qquad (2.13)$$

Since the interested frequency range is near oscillation frequency, $|\Delta\omega| << \omega_{osc}$, and v can be simplified to $(2\Delta\omega)/\omega_{osc}$. Substitution of the gain condition of oscillation, $g_m R_p = 1$, and $v = (2\Delta\omega)/\omega_{osc}$ in (2.13) leads to a simplified expression for $H_{cl}(j(\omega_{osc} + \Delta\omega))$,

$$\left|H_{cl}(j(\omega_{osc} + \Delta\omega))\right| = \frac{1}{\frac{2\Delta\omega}{\omega_{osc}} Q_p} \qquad (2.14)$$

The output noise current $\overline{i_{n_{out}}^2}$ can be calculated as

$$\overline{i_{n_{out}}^2}(j(\omega_{osc}+\Delta\omega)) = \overline{i_n^2}\left(\frac{\omega_{osc}}{2Q_p\Delta\omega}\right)^2 \qquad (2.15)$$

The output noise current can be obtained with noise current $\overline{i_n^2} = \frac{4kFT}{R_p}$ to account for the excess noise factor F.

$$\overline{i_{n_{out}}^2}(j(\omega_{osc}+\Delta\omega)) = \frac{4kFT}{R_p}\left(\frac{\omega_{osc}}{2Q_p\Delta\omega}\right)^2 \qquad (2.16)$$

This noise is composed by both phase and amplitude noise. Therefore, phase noise of the oscillator is calculated as

$$L(\Delta\omega) = \frac{\frac{1}{2}\overline{i_{n_{out}}^2}(j(\omega_{osc}+\Delta\omega))}{i_{carrier}^2} \qquad (2.17)$$

Substitution (2.16) to the above phase noise expression,

$$L(\Delta\omega) = \frac{\frac{1}{2}\frac{4kFT}{R_p}\left(\frac{\omega_{osc}}{2Q_p\Delta\omega}\right)^2}{i_{carrier}^2} \qquad (2.18)$$

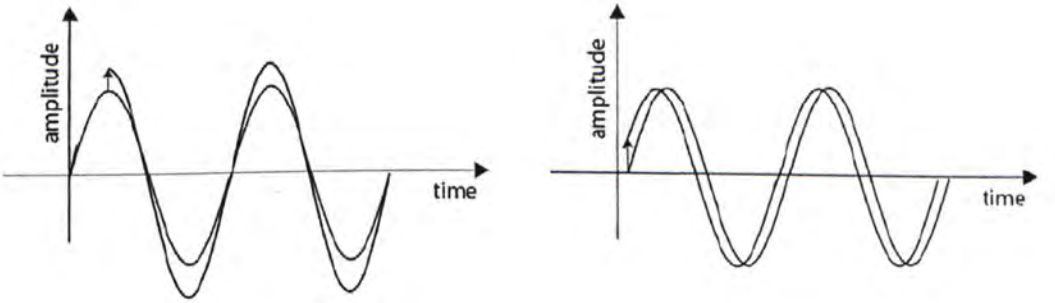
with $P_{sig} = i_{carrier}^2 R_p$

$$L(\Delta\omega) = \frac{2kFT}{P_{sig}}\left(\frac{\omega_{osc}}{2Q_p\Delta\omega}\right)^2 \qquad (2.19)$$

which is identical to the $1/\omega^2$ portion in Leeson's phase noise expression.

2.4.3 Linear Time-Variant phase noise model

Some of the problems with Leeson's model are solved by the Linear Time-Variant (LTV) model formulated by A. Hajimiri and T.H. Lee[13]. An important property of oscillators which is not accounted for in the Leeson model is the time variance and cyclo-stationary nature of noise. The response of an oscillator to device noise depends on which points in the period of oscillation this noise is applied. Rather than being time invariant, this observation indicates that LC oscillators are time-varying systems. This fact is illustrated in figure2-9 for an ideal oscillator.



(a) (b)

Figure 2-11 Phase impulse response of the ideal oscillator topology

The figure shows that different responses of an ideal oscillator to an impulse

applied at a point near, (a) a voltage maximum and, (b) a zero crossing of the output signal. In figure 2-11(a), it is noticed that when the impulse is applied, there is abrupt increase in the amplitude with little or no change in the phase of the sinusoidal waveform. Given the fact that all oscillators have some amplitude limiting mechanism, this change in the output voltage magnitude is removed and there is no phase noise. On the other hand, in figure 2-11(b), there is maximum change in the phase but little or no change in the amplitude of the output signal. Thus, it can be concluded that the oscillator is most sensitive to noise at the zero crossing or alternatively, when the amplitude of the output signal is at its mean value. In general, noise impulses occur throughout the period of oscillation and thus, there is always a combination of amplitude and phase perturbations. The response or susceptibility of the oscillator is defined by what is called an impulse sensitivity function (ISF), Γ. This function is obtained from simulations in HSPICE or SpectreRF by applying a series of small impulses at regular intervals within a period of oscillation and measuring the change in phase produced. The result is used to calculate the phase noise of the LC oscillator using the equation below:

$$L(\Delta\omega) = 10\log\left(\frac{\Gamma_{rms}^2}{q_{\max}^2}\frac{\overline{i_n^2}/\Delta f}{4\cdot\Delta\omega^2}\right) \qquad (2.20)$$

where Γ is the rms value of impulse sensitivity function

q_{max} is maximum charge swing

$\overline{i_n^2}/\Delta f$ is noise current power spectral density

$\Delta\omega$ is the offset frequency from carrier

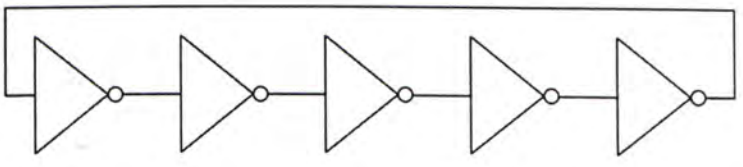
Note that there is no empirical factor which can only be obtained by measurement. Every term in (2.20) can be obtained by hand calculation and simulation. This is an obvious advantage over Leeson's formula. However, LTV model requires a lot of simulation time which increases with number of components and noise sources.

Chapter 3

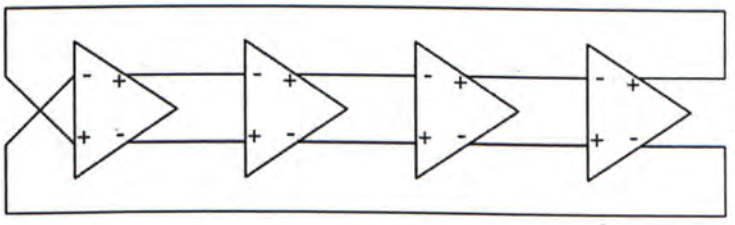
Fully-integrated CMOS Oscillator Design

3.1 Ring oscillator

Fully integrated oscillator implemented using CMOS technology is mainly divided into two groups: ring oscillator and LC oscillator. Ring oscillator[14][15] is firstly implemented on-chip due to its simple structure. A CMOS ring oscillator is composed by inverters using active elements only. The schematic of ring oscillators is shown in figure 3-1.



(a)



(b)

Figure 3-1 (a) Single-ended ring oscillator (b) differential ring oscillator

Odd number of inverters are connected in series and the output of the last inverters is feedback to the input of the first inverters. The oscillating frequency of the ring oscillator depends on the time constant (τ) in each inverter stage. Time constant of each inverter stage is dominant by the inverter output impedance ($1/g_m$) and gate capacitance (C_g).

$$\tau = \frac{C_g}{g_m}$$

The period of the oscillation is $2N/\tau$ since the signal passes through the odd number (N) of inverters twice and get back to its original value. In order to make the oscillating frequency tunable, the oscillating frequency can be varied by controlling the bias current (I_{ctrl}) of the ring oscillator. The relationship between bias current and oscillating frequency can be obtained by

$$f = \frac{I_{ctrl}}{2NV_oC_g}$$

Ring oscillator can also be implemented with even number of differential gain stage as shown in figure 3-1(b).

Since the oscillating frequency of ring oscillator is determined by the time constant of inverters, ring oscillator can operate at a higher frequency with more advanced technology due to the reduced gate capacitance and larger transconductance with given bias current. However, the main disadvantage of ring oscillator is its inherent poor phase noise performance. This is because there are more

active devices contributing noise to the output but no filtering to suppress the noise at the frequency of interest. Therefore, oscillator based on LC-tank is dominant in low-noise applications and the principle of operation will be described in the next section.

3.2 LC oscillator

Oscillator based on LC-tank architecture is widely adopted in RF applications due to its low-noise feature[16][17]. Schematic of LC oscillator is shown in figure3-2. There are two main parts in a LC oscillator: the LC-tank resonator and the negative resistance. This section discusses both parts based on the trade-offs between different oscillator design parameters.

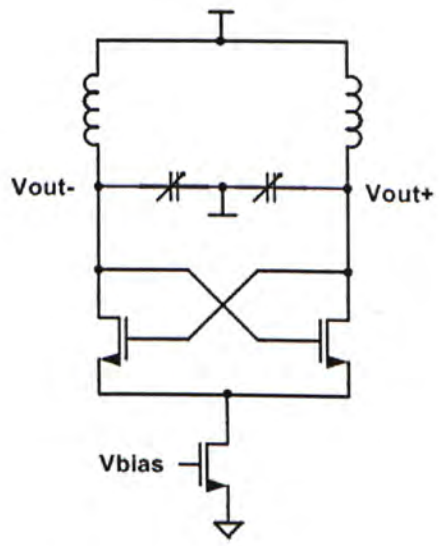


Figure 3-2 A schematic of a LC oscillator

3.2.1 LC-tank resonator

LC oscillator cannot be fully integrated without the on-chip inductor and capacitor. LC-tank is the most important element in this kind of oscillator since its parameters affect the oscillator performance greatly in terms of phase noise and tuning range.

High-Q MOS varactor can be easily obtained in CMOS process but it is not the case for the spiral inductor, so the Q-factor of a LC-tank is mainly limited by the spiral inductor. LC-tank is lossy in real implementation due to the parasitic resistance associated with spiral inductor and MOS varactor. The model of a lossy LC resonator can be transformed to an equivalent LC-tank model with a parallel resistance, as shown in figure3-3.

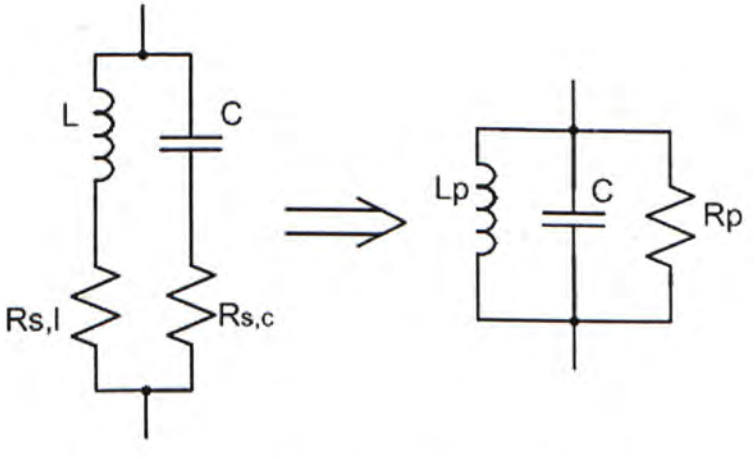


Figure 3-3 Conversion of a LC-tank to a equivalent parallel model

The equivalent parallel resistance depends on the quality factor of LC-tank and the inductor value as

$$R_p = Q\omega L$$

Therefore, the equivalent parallel resistance can be increased by increasing the quality factor or the inductor value. The consequence of larger parallel resistance is larger output amplitude. The output amplitude of the LC oscillator in figure3-2 can be estimated as

$$V_{out} = \frac{4}{\pi} R_p I_{bias}$$

where I_{bias} is the bias current of the LC oscillator. Since the phase noise is the ratio of output noise to output signal power, lower phase noise can be expected by simply using a larger inductor value[18]. However, the output amplitude cannot increase with the inductor value without limit and is bounded by the supply voltage ultimately.

Besides the inductor value, the capacitance value is also another important parameter that determine the oscillation frequency, such that $f = 1/\sqrt{L_p C}$. To operate at high frequency, small value of inductor should be implemented in the oscillator design. Furthermore, the tuning range of a LC oscillator is determined by the varactor tuning ratio ($\Delta C / C$). For a given application, the tuning range and

hence the varactor size can be calculated. By using a smaller value of inductor, the tuning range of a LC oscillator is larger for a given operating frequency.

Nevertheless, the inductor value plays a very important role in LC oscillator design. Larger value of inductor benefits the phase noise, but the operating frequency and tuning range for a given application limits the maximum value of inductance.

3.2.2 Negative transconductance

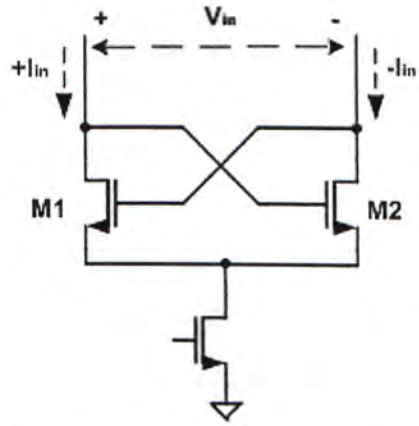


Figure 3-4 Negative resistance of a cross-coupled pair

As mentioned in previous chapter, the loss in the LC-tank is compensated by the negative resistance in order to maintain the oscillation. A cross-coupled pair of transistors can be used to provide the negative resistance. The negative resistance generation by the cross-coupled pair in figure3-4 is derived as follows:

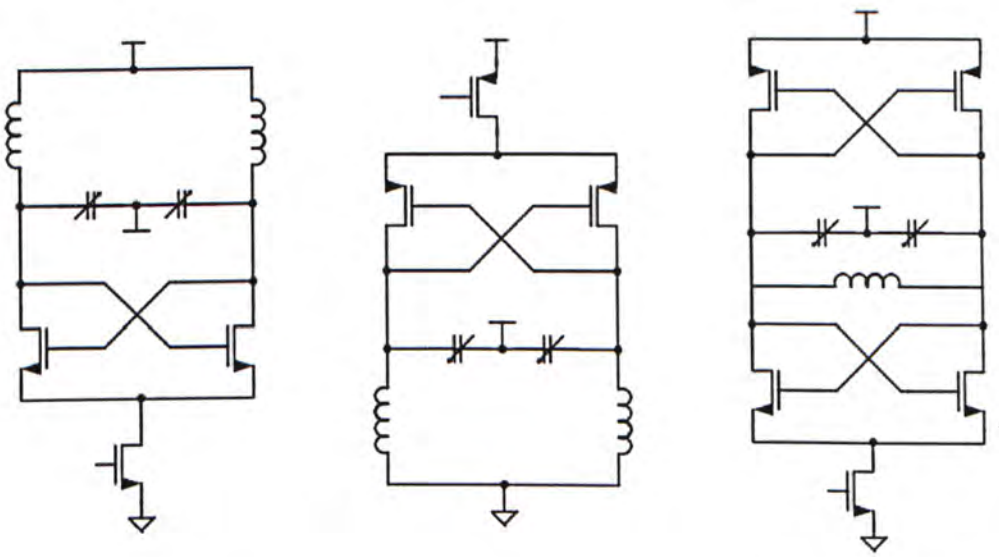
$$V_{in} = V_{gs2} - V_{gs1} = \frac{I_{d2}}{g_{m2}} - \frac{I_{d1}}{g_{m1}} \qquad (3.1)$$

$$I_{in} = I_{d1} = -I_{d2} \qquad (3.2)$$

Substitute (3.2) into (3.1), and assume gm1=gm2=gm to get

$$V_{in} = \frac{I_{d2}}{g_{m2}} - \frac{I_{d1}}{g_{m1}} = -\frac{2I_{in}}{g_m} \qquad (3.3)$$

$$R_{in} = \frac{V_{in}}{I_{in}} = -\frac{2}{g_m} \qquad (3.4)$$



(a) (b) (c)

Figure 3-5 (a) NMOS-only VCO, (b) PMOS-only VCO, (c) complementary VCO

There are three different kinds of cross-coupled pair structure: NMOS-only, PMOS-only and complementary cross-coupled pair using both NMOS and PMOS. Figure3-5 shows their schematic. NMOS-only and PMOS-only structures are very

similar. Both of them can operate at low supply voltage, but they are different in transconductance and phase noise performance. For a given bias current, NMOS-only structure can obtain a larger transconductance than PMOS-only. If PMOS-only structure is going to obtains the same transconductance , transistors should be sized about three times larger. This increases the paracitic capacitance at the VCO output, and hence reduces the tuning range. PMOS-only structure has the advantage of lower phase noise in $1/f^3$ region due to the lower flicker noise of PMOS transistor[19]. Complementary cross-coupled pair has the most symmetric output waveform. Also, this structure lowers the power consumption by current-reuse. PMOS cross-coupled pair and NMOS cross-coupled pair is biased with the same current source and more transconductance can be generated with a given current. There are more transistors in the stacking, so this structure is not popular for low voltage design.

3.3 Generation of quadrature phase signals

Quadrature signals can be obtained on-chip in different ways. By using a polyphase filter [20] as shown in figure 3-6 , quadrature signals can be obtained by injecting a differential signal into the input port. However, the phase accuracy of the quadrature signals generated highly depends on the matching of the passive elements. Also, the passive elements in a polyphase filter occupy large chip area. Another drawback is the high insertion loss. Since the polyphase filter consists of large resistance, the output voltage is greatly reduced due to the voltage divider.

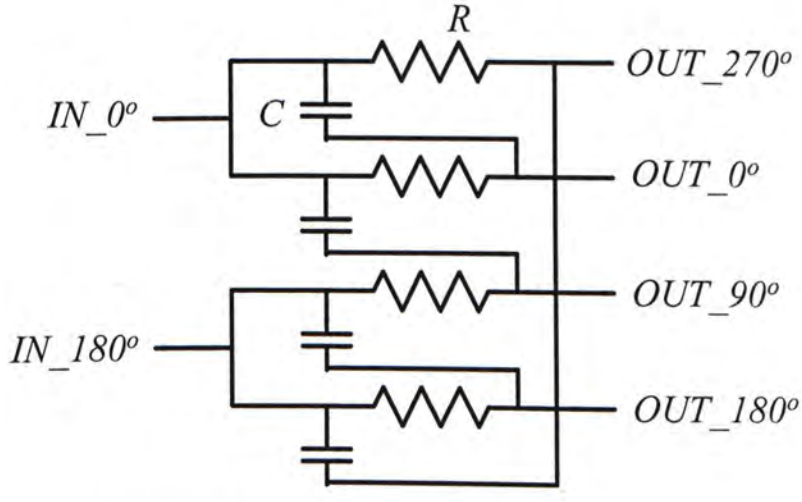


Figure 3-6 The schematic of a polyphase fillter

Another method to generate quadrature signals on-chip is using a differential VCO followed by a divide-by-two divider with quadrature outputs[21]. The

advantage of this method is the ease of implementation. However, the frequency of the quadrature signals is halved the operating frequency of the VCO. The halved operating frequency is the main drawback of this method since the trend of transceiver design is driven toward to higher operating frequency for higher data-rate transmission.

QVCO generates the quadrature signals by applying injection locking to two differential VCOs[22][23][24]. This method is the most common way to generate quadrature signals in fully-integrated transceivers at RF frequency range. Detailed discussion of QVCO will be given in the next section.

3.4 Quadrature VCO topologies

QVCO mainly consists of two differential VCOs and the quadrature signals can be obtained by the coupling between two differential VCOs. This section discusses different types of QVCO, such as parallel-coupled QVCO[22], series-coupled QVCO[24]and superharmonic-coupled QVCO using transformer[25].

3.4.1 Parallel-coupled QVCO

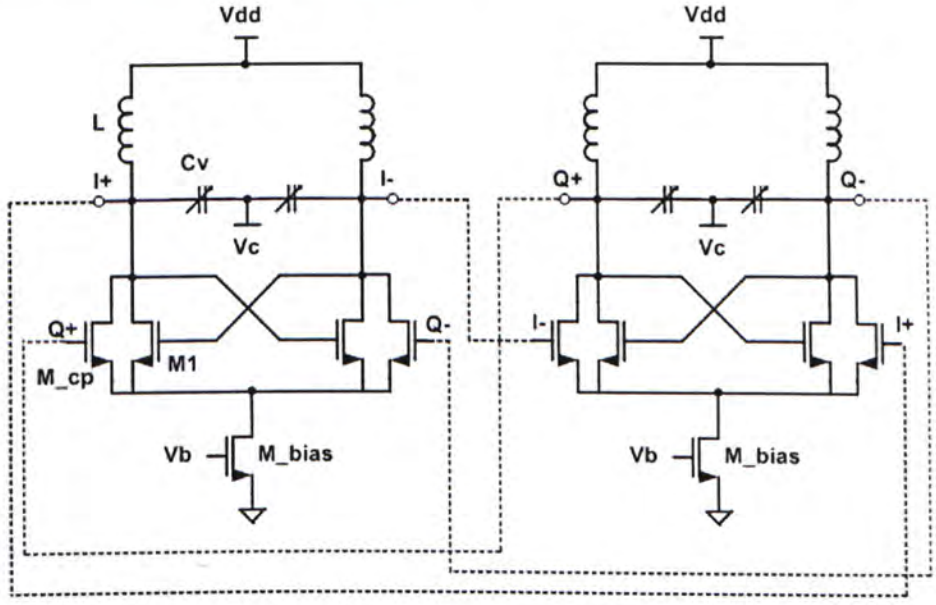


Figure 3-7 Schematic of a parallel-coupled QVCO

The schematic of the parallel-coupled QVCO is shown in figure3-6. It consists of two differential VCOs and four coupling transistors. Each VCO is composed of a LC-tank to operate at given oscillating frequency and tuning range and a cross-coupled to compensate the loss in the LC-tank in order to sustain the

oscillation. The coupling transistors are connected in parallel fashion to the cross-coupled pair. Both the cross-coupled pair and the coupling transistor are biased with the same current source, so the current passing through these transistors and, hence their transconductane are determined by the transistor size.

To obtain a qudrature phase in two oscillator outputs, the outputs of the first VCO are directly-connected to the second VCO through the coupling transistors and the outputs of the second VCO are crossly-connected to the first VCO. The generation of quadrature signals can be explained using the block diagram of the coupled VCO shown in figure3-8. Each oscillator is modeled by a positive feedback loop with open loop gain G_i for i = 1,2. Their output are coupled to each other with the coupling coefficients M_1 and M_2. If both oscillators synchronize to a single oscillation frequency at ω, in steady-state, the output of each oscillator must satisfy the following equations:

$$(X + M_2 Y)G_1(j\omega) = X \qquad (3.5)$$

$$(Y + M_1 X)G_2(j\omega) = Y \qquad (3.6)$$

where M_1 and M_2 are scalars, and X and Y are the output phasors for oscillator 1 and 2, respectively. Since the oscillators are identical, G_1=G_2=G and M_1=-M_2=M can be satisfied. Hence from (3.5) and (3.6), it can be shown that $X^2 + Y^2 = 0$, and

therefore $X = \pm Y$. The outputs of two oscillators are in quadrature phase. It is worth to mention that the oscillation frequency of a coupled VCO is different from a single VCO. The new oscilation freuqewncy ω can be found by substituting $X = \pm Y$ back into (3.5) or (3.6) to give,

$$(Y + M_1 X)G_2(j\omega) = Y$$

where $G(j\omega) = Z(j\omega)G_m$,and $\phi(Z(j\omega)) = \pm \tan^{-1} M$ are the possible conditions for the oscillation.

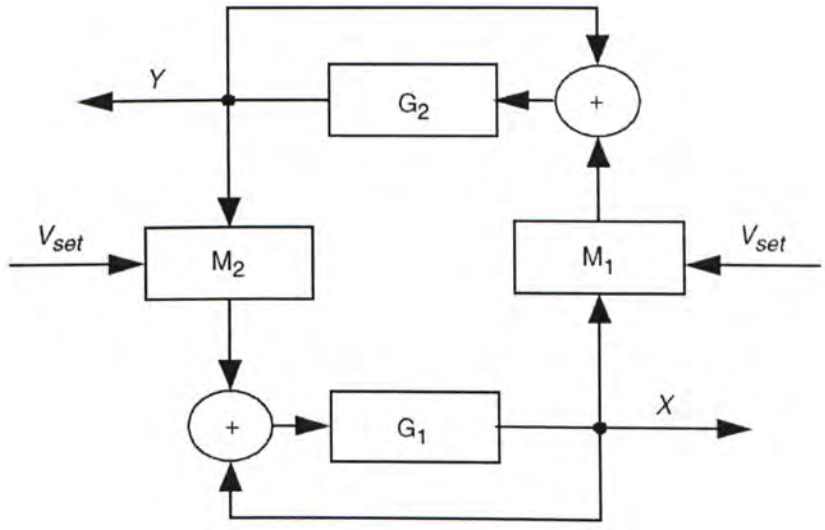
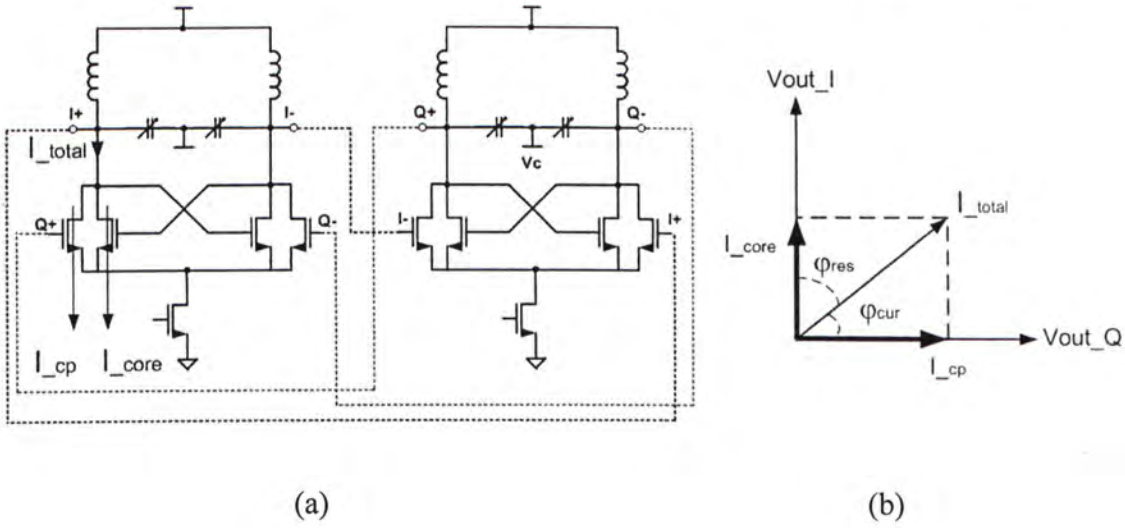


Figure 3-8Model of a coupled VCO

Although this QVCO topology is simple and straightforward, it has many drawbacks. The most obvious disadvantages are its high power consumption and low operating frequency. The transistor size of the four coupling transistors varies from one-third to same size as the cross-coupled pair in order to maintain sufficient phase

accuracy. Therefore, extra power is consumed by the coupling transistors. Furthermore, the parasitic capacitance associated with the coupling transistors lower the operating frequency and reduce the tuning range.

The introduction of coupling transistors also degrades the phase noise performance of VCO. Not only due to the extra active devices add noise to the output, but it also shifts the oscillating frequency off the tank resonance. As shown in figure3-9, the output voltage of in-phase oscillator (*Vout_I*), is in-phase with the bias current (I_{core}). In steady state, coupling transistor driven by the quadrature signal draws current (I_{cp}) from the same node as I_{core}. Therefore, the total current (I_{total}) passing through the LC-tank is the vector sum of these two components. In order to maintain the quadrature oscillation, a phase shift of φ_{res} is provided by the resonator. And the oscillation will oscillate at the frequency off the tank resonance where the impedance magnitude of the LC-tank is largest. Hence, the output swing is reduced and the phase noise performance degrades.



(a) (b)

Figure 3-9 Relationship between tank voltage and current in parallel-coupled QVCO

As mentioned before, there are two possible solutions for the oscillating frequency in QVCO. [23] discussed that the asymmetrical frequency characteristics of an LC-tank will make one of the modes more dominant than the other, and hence, the QVCO will be able to operate stably at one of these modes only. However, [27] shows that bimodal oscillation behavior. This is called the frequency ambiguity. Depending on whether X leads or lags Y, the operating frequency of a QVCO will be totally different.

3.4.2 Series-coupled QVCO

An alternative to parallel-coupled VCOs is the series-coupled QVCO [24] as illustrated in figure3-10. The coupling transistors are connected in series with the cross-coupled pair instead of connecting in parallel fashion. Like parallel-coupled QVCO, the output of the first VCO are directly-connected to the second VCO and the output of the second VCO is crossly-connected to the first VCO in order to generate the quadrature signals. The advantage of series-coupled QVCO is its better noise performance. Comparing with parallel-coupled QVCO, the phase noise of the series-couple QVCO is about 10dB lower [24].

It is shown in figure3-9 that there are three transistors stacking in the series-coupled QVCO, so the maximum output swing is one V_{ds} less than the parallel-coupled QVCO. Besides the transistor stacking, the size of coupled transistors connected in series fashion should be made five times larger than the cross-coupled pair to get a better phase noise performance. The large coupling transistors lower the oscillating frequency due the large parasitic capacitance associated with them. Therefore, this topology is not suitable for low-voltage and high frequency QVCO design.

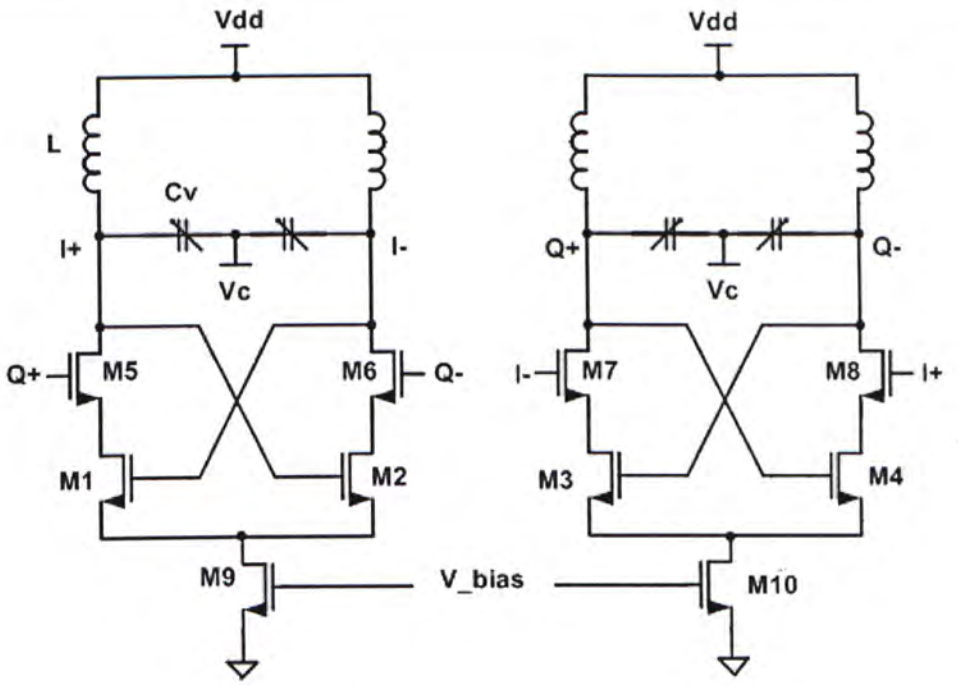


Figure 3-10 The schematic of a series-coupled QVCO

3.4.3 QVCO with Back-gate Coupling

In the previous two QVCO topologies, coupling transistors are required to maintain the quadrature phase relationship between two VCOs. In the case of housing the cross-coupled pair transistors in separate wells, their back-gate can be used as a coupling terminal. The schematic of QVCO with back-gate coupling is depicted in figure 3-11 [29]. The resistors R_b are added for the dc biasing of the bulk terminals and the capacitors C_b are inserted for ac coupling. Since applying coupling signal to the back-gate has the same effect as applying it to the gate, coupling can thus be

maintained without using any extra coupling transistors as in parallel-coupled QVCO.

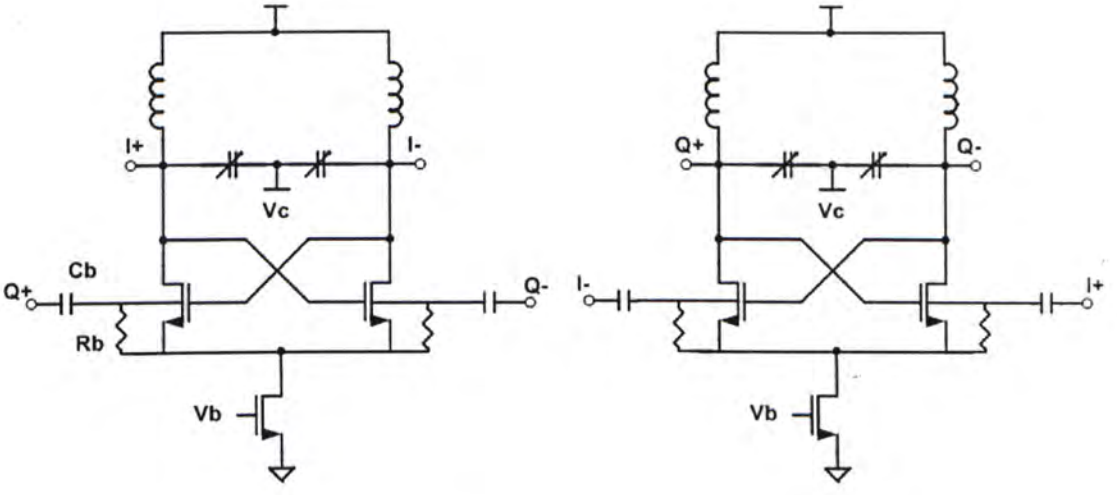


Figure 3-11 Schematic of QVCO with back-gate coupling

In contrast to parallel-coupled QVCO, the phase noise of the back-gate coupled QVCO is not degraded by variation in the transconductance of the coupling transistors. Comparing the series-coupled QVCO and parallel-coupled QVCO designs, this architecture consumes less power due to the absence of coupling transistors while the voltage headroom is not reduced. Moreover, the overall phase noise performance is expected to be the same as that of the conventional single transistor, since the 1/f noise of the transistor originates from the same location. That means the body-coupled transistor is added free of 1/f noise [29]. However, the extra parasitics added to the tank circuit cannot be avoided by using this topology.

3.4.4 QVCO using superharmonic coupling

For the QVCO designs described before, neither the parallel-coupled nor the series-coupled QVCO are able to operate at high frequency. The reason for the low operating frequency is the parasitic capacitance associated with the coupling transistors at the output of the QVCO. In parallel-coupled QVCO, the coupling transistors contribute one-third of the parasitic capacitance and the case is even worse in series-coupled QVCO since the coupling transistor size is five times larger than the cross-coupled pair. Therefore, most QVCO using these two topologies operate at frequency range lower than 3-GHz.

The second order harmonics can be extracted from the common-mode nodes. Also, the outputs of two VCOs run in qudrature phase when the common-mode node of two VCOs are driven differentially [25]. The anti-phase coupling is implemented by means of the coupled transformer shown in figure3-12. This type of QVCO is called superharmonic-coupled QVCO.

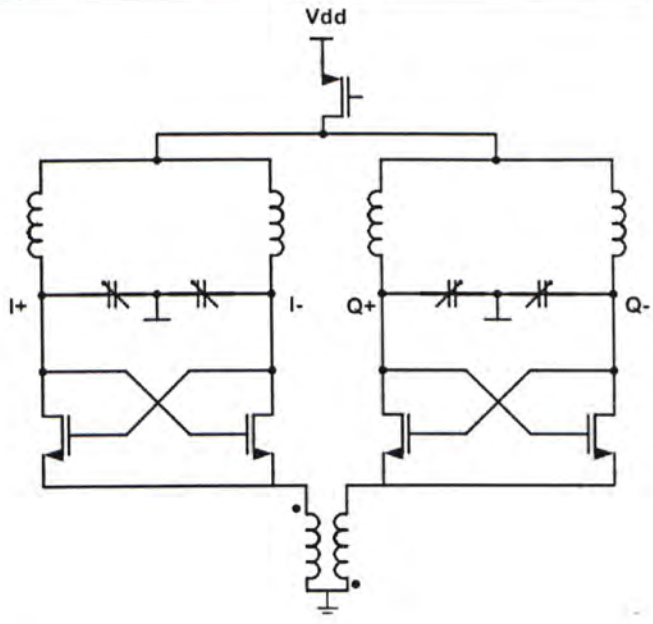


Figure 3-12 The schematic of a superharmonic-coupled QVCO using transformer

Besides the higher operating frequency, the superharmoinc-coupled QVCO gives a better phase noise performance. This coupling mechanism does not require the oscillating frequency deviate from the tank resonance frequency where the tank impedance is the largest. Moreover, since the qradrature coupling is established by means of coupled inductors rather than by transistors, the coupling devices introduce no significant extra noise sources.

In [26], the superharmonic coupling is obtained by using two coupling capacitors and additional biasing devices, as shown in figure 3-13. The second harmonic appeared at the two common-mode nodes are ac-coupled via capacitor to the gate input of the biasing transistors (Mn5, Mn6). Then, the two identical VCOs

are injection locked to each other and their outputs are in quadrature phase with differential common-mode signals.

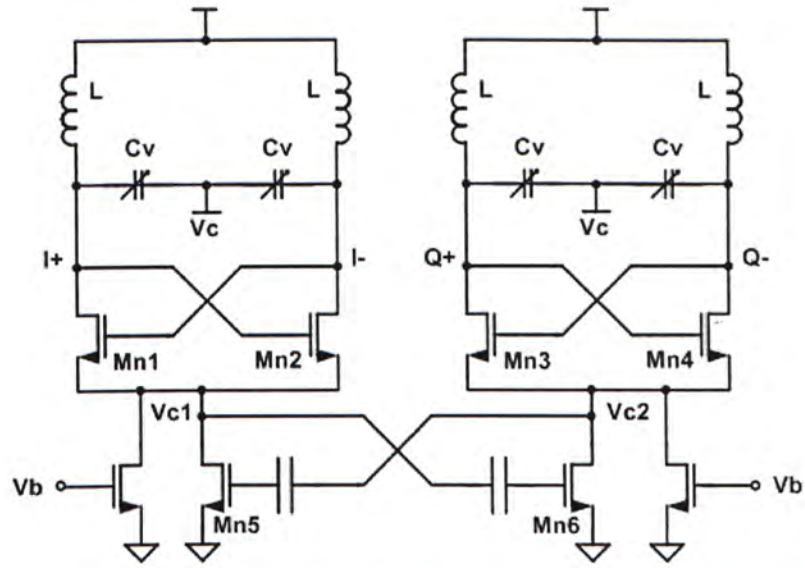


Figure 3-13 Schematic of capacitive superharmonic-coupled QVCO

Without using a transformer, QVCO using this topology occupies less chip area and more cost effective. However, this configuration is itself a cross-coupled pair and is susceptible to self-oscillation. If the closed-loop gain is larger than one, the common-mode node in two VCOs will oscillate and modulate the output of QVCO.

3.5 Novel QVCO using back-gate superharmonic coupling

In this section, a novel QVCO topology is proposed based upon super-harmonic coupling through the back-gate of the PMOS current source. This circuit offers low power, low voltage and high frequency operation with only standard CMOS process. Firstly, the working principle of the proposed QVCO is explained. Next, layout consideration is discussed due to its importance for high-frequency operation. A parallel-coupled QVCO is also implemented for comparison. This chapter is concluded with the simulation results of the proposed QVCO.

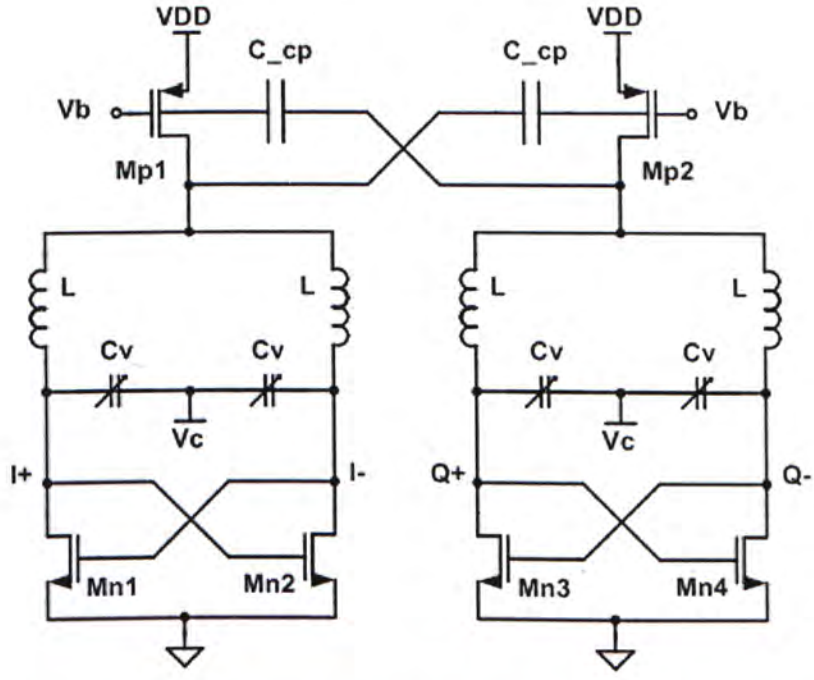


Figure 3-14 The schematic of novel QVCO using back-gate superharmonic coupling

Figure3-14 shows the schematic of the proposed QVCO circuit in CMOS

technology. For individual differential oscillator, negative resistance was generated from the NMOS cross-coupled pair to compensate for the loss associated with the resonant tank. Phase noise performance of the oscillator is mainly determined by the quality factor of the spiral inductors. The two MOS varactors control the oscillating frequency and hence the tuning range of the VCO.

To generate quduature output signals, the second harmonic signals were extracted from the center of two inductors and inject to the back-gate of the adjacent current source (PMOS) through the coupling capacitors. The back-gate/bulk of a transistor can be used as a second gate, because the drain current is a function of the bulk voltage. In saturation region,

$$g_{mb} = \frac{\partial I_D}{\partial V_{BS}} = \mu_n C_{ox}(V_{GS} - V_{TH})(-\frac{\partial V_{TH}}{\partial V_{BS}})$$

Also, $g_m V_{GS}$ and $g_m V_{GS}$ have the same polarity, so raising the gate voltage has the same effect as raising the bulk potential. The coupling capacitors are implemented by using the poly-poly capacitance and they occupy much smaller chip area than the on-chip transformer.

3.5.1 Tuning range

The oscillating frequency of an oscillator depends on the resonance frequency of the LC-tank. For tuneable oscillating frequency, the capacitance in the varactor is controlled by the control voltage. To tune between f_{max} and f_{min} at least a fraction ΔC of the total tank capacitance C_{total} must be variable, such that

$$\frac{\Delta C}{C_{total}} \geq \frac{2(f_{\max} - f_{\min})}{0.5(f_{\max} + f_{\min})}$$

The proposed QVCO is designed to cover 4.9GHz to 5.4GHz, and hence the required $\Delta C/C_{total}$ is 19.4%.

Also, the oscillating frequency can be obtained by the following equation

$$f = \frac{1}{2\pi\sqrt{LC_{total}}}$$

Assuming inductance value L=2nH, C_{min} is 434fF for f_{max}=5.4GHz and C_{max} is 527fF for f_{min}=4.9GHz. The total capacitance in LC-tank is composed of varactor and the parasitic capacitance of metal connection, cross-coupled pair and the output buffer. The required variable capacitance ΔC of value 93fF is provided by an accumulation-mode varactor consisting of eight fingers. The C_{min}/C_{max} of the designed varactor is 42fF/155fF, therefore leaving 372fF for the parasitic capacitance of metal connection, the cross-coupled pair and the output buffer.

3.5.2 Negative gm

The quality factor of the LC-tank is mainly limited by the spiral inductor. Therefore, the parallel resistance in the LC-tank can be expressed by

$$R_p = \omega L Q_L$$

For example, a 2nH spiral inductor with a Q-factor of 5.7 will have a R_p of 57Ω at 5GHz.

The loss in the LC-tank is compensated by using a cross-coupled pair. In order to start the self-oscillation, the value of gm must be fulfilled the following condition.

$$g_m = \frac{2\alpha}{R_p} = 70mS \text{ , for } \alpha=2$$

The required gm provided by the cross-coupled pair is given as

$$g_m = \frac{2I_D}{V_{GS} - V_t}$$

With a biasing current of 4mA, threshold voltage of 0.55V and V_{GS} of 0.66V obtained by using DC analysis, the value of g_m can be found equal to 72mS.

3.5.3 Phase noise calculation

The phase noise of the proposed QVCO in $1/f^2$ region can be estimated by using equation (2.9).

At the frequency offset of 1MHz, the phase noise of the QVCO

$$L(\Delta\omega) = 10\log\frac{2FkT}{P_{sig}}\left(\frac{\omega_o}{2Q\Delta\omega}\right)^2$$

$$= 10\log\frac{(2)(2)(1.38\times10^{-23})(300)}{(20\times10^{-3})^2/2}\left(\frac{5\times10^9}{(2)(5.7)(1\times10^6)}\right)^2$$

$$= -108dBc/Hz$$

The values of devices implemented in proposed QVCO is listed in table 1.

Mn1-4	Mp1-2	M_{buffer}	L	Cv (max)	C_cp
100/0.35	50/0.35	30/0.35	2nH	155fF	5pF

Table 1 Component values in the proposed QVCO

3.5.4 Coupling coefficient

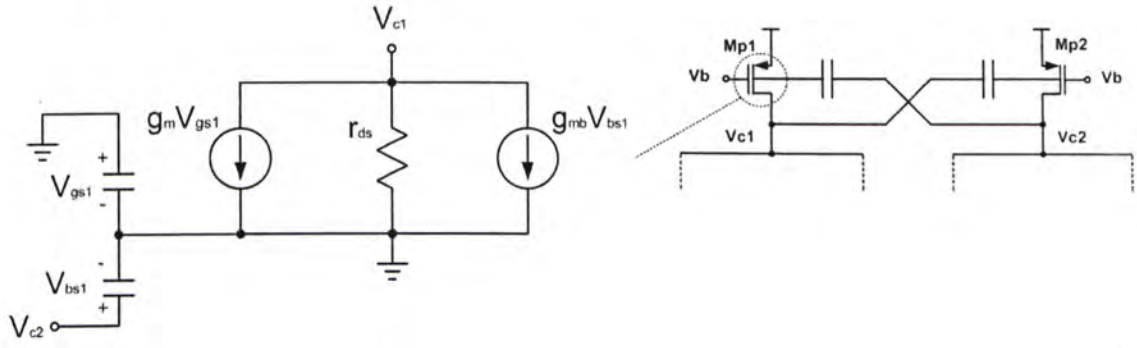


Figure 3-15 Small-signal model of the biasing transistor

The coupling of the two differential oscillators is accomplished by injecting the second harmonic signal of one oscillator into the common-mode node of another oscillator. Based on the small-signal model of the PMOS transistor shown in figure 3-15, the injected current can be obtained by

$$i_{b1} = -v_{c2} g_{mb}$$

Also, the relationship between the common-mode voltage (V_{c1}) and the injected current is

$$v_{c1} = i_{b1}\left[r_{ds,pmos} // \frac{r_{ds,nmos} + R_p}{2} \right]$$

Hence,

$$v_{c1} = -v_{c2} g_{mb}\left[r_{ds,pmos} // \frac{r_{ds,nmos} + R_p}{2} \right]$$

The above expression indicates that the second harmonic at the two common-mode nodes (V_{c1} and V_{c2}) are in 180° out-of-phase which lead to quadrature phase difference at their outputs. The coupling coefficient between two VCOs is $g_{mb}\left[r_{ds,pmos} // \frac{r_{ds,nmos}+R_p}{2}\right]$.

It is worth to note that self-oscillation may occur when the closed-loop gain of two biasing transistors is greater than unity. In order to avoid self-oscillation at the common-mode nodes, the following condition should also be fulfilled

$$g_{mb} < \frac{2}{\frac{r_{ds,nmos}+R_p}{2}} = \frac{4}{r_{ds,nmos}+R_p}$$

In [26], the gate terminal is used as the injection port for the second harmonics and the size of the biasing transistor is limited by the closed-loop gain to avoid the self-oscillation. As a result, the current delived by the current source may become too small for the cross-coupled pair to provide the required negative resistance. One possible solution to avoid undesired self-oscillation is to split the biasing transistor into two if a large biasing current is needed.

Since g_{mb} is smaller than g_m, the loop gain is smaller than using the gate as the injection port. It provides the flexibility in designing the biasing transistor as the coupling transistor for the second harmonics.

3.5.5 Low-voltage and low-power design

In this design, low voltage and low power operation is possible due to the absence of series-connected or parallel-connected coupling devices. The PMOS transistors in the proposed QVCO serve two functions as current sources and super-harmonic coupling transistors, therefore no additional power is needed in this method.

Voltage headroom is one of the important concerns in low-voltage design. The bulk terminal of the NMOS cross-coupled pair and the PMOS current source are connected to the ground and supply respectively. By using the back-gate of the PMOS device, body-effect is minimized without triple-well process for device isolation. If a NMOS device is employed, holes are attracted to the substrate connection transistor for $V_{SB} > 0$, leaving a larger negative charge behind and the depletion region becomes wider. Since threshold voltage is a function of the total charge in the depletion region because the gate charge must mirror the holes in depletion region before an inversion layer is formed. Thus, as bulk voltage drops and the depletion region charge increases, V_{TH} also increase. The relationship between V_{SB} and V_{TH} is shown in the following equation,

$$V_{TH} = V_{TH0} + \gamma(\sqrt{|2\Phi_F + V_{SB}|} - \sqrt{|2\Phi_F|})$$

where V_{TH0} is the threshold voltage when $V_{SB} = 0$, γ is the body effect coefficient and the value is about 0.3 to $0.4V^{1/2}$ and V_{SB} is the source-bulk potential difference. A smaller threshold voltage can offer more voltage headroom for the output swing and therefore, the proposed QVCO may operate as low as 1V.

3.5.6 Layout Consideration

The proposed QVCO is fabricated using AMS 0.35μm CMOS process that provides 4 metal layers and 2 poly-silicon layers. Since the circuit operates at around 5-GHz, many layout issues should be considered carefully.

3.5.6.1 Symmetrical Layout and parasitics

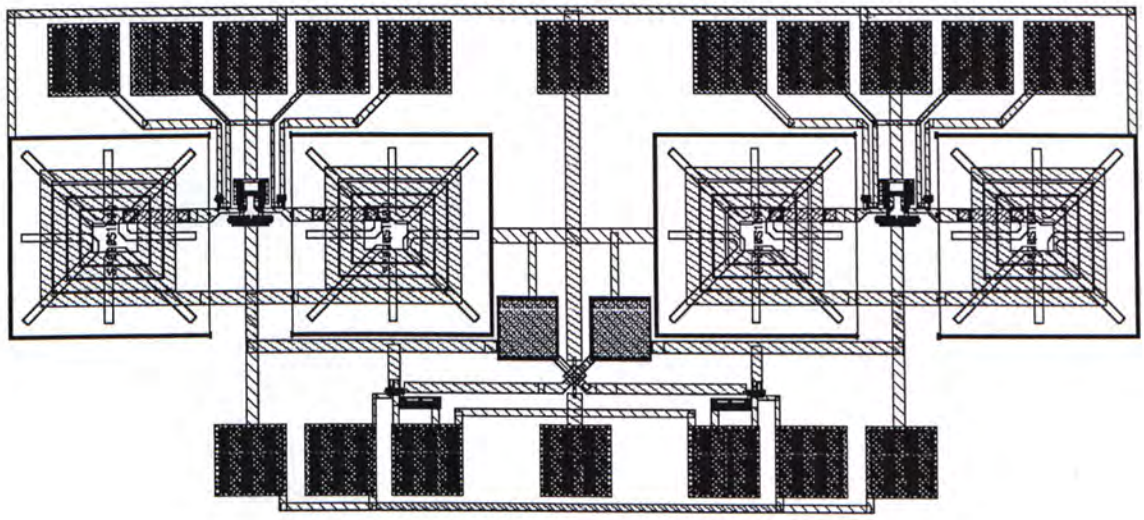


Figure 3-16 The overall layout of the proposed QVCO

Figure 3-16 shows the overall layout of the proposed QVCO using capacitive coupling network. The layout is highly symmetrical for better differential performance. The layout of coupling network is also symmetrical to maintain the matching of the differential coupling of the second harmonic between the two

oscillators.

The parasitic of the layout caused by the capacitance between metal layer and the substrate, especially at the node connecting the spiral inductor, the varactor and the cross-coupled pair, could affect the oscillating frequency. The parasitic capacitance at this node should be minimized for high frequency operation. As illustrated in figure3-17, the varactor, the spiral inductor and the cross-coupled pair are placed close together to keep metal layer at minimal length.

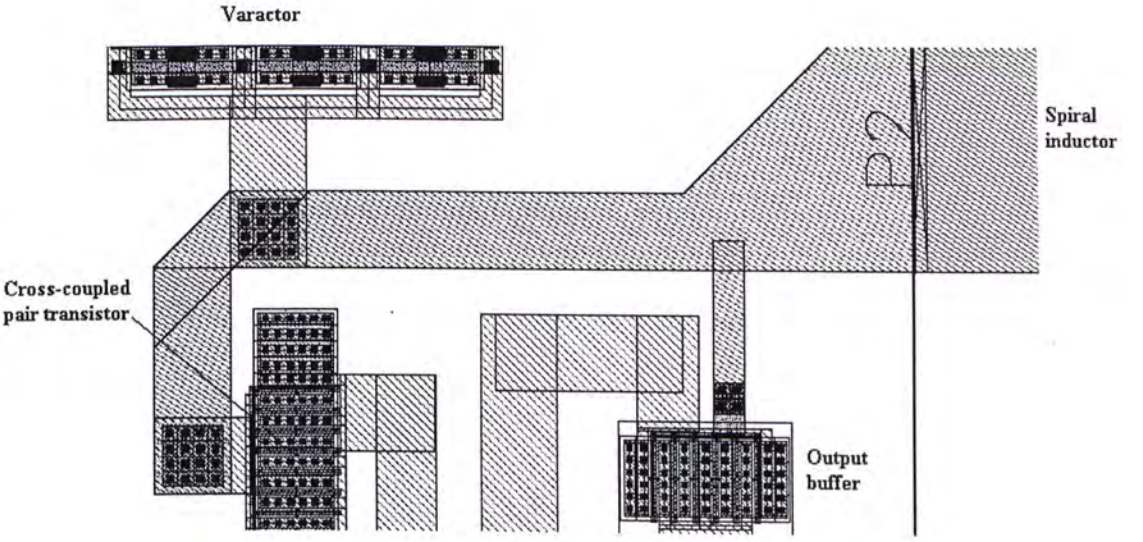


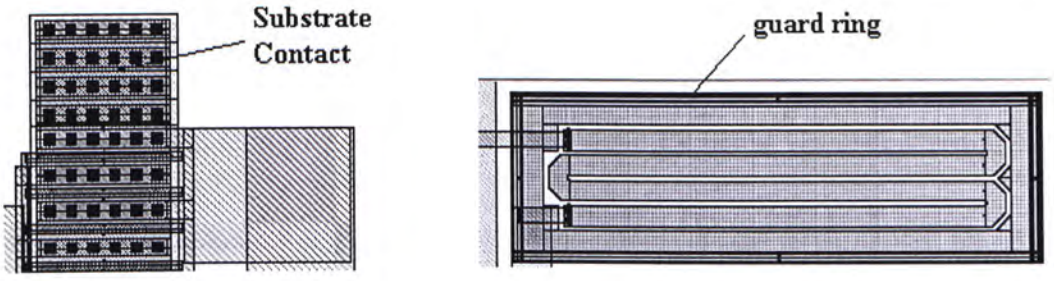
Figure 3-17 Layout of the output node before buffering

3.5.6.2 Metal width and number of vias

Bias current flows through the active and passive components through the metal wires. There are maximum current density for different metal layers and the vias connecting different metal layers. For example, maximum current density is 1.6mA/μm for metal 4 layer and 0.6mA/via for via connecting metal 1 and metal 2. Wider metal wire and more number of vias should be used for carrying higher current, especially for the metal wire connecting voltage supply to the common-node between two inductors.

3.5.6.3 Substrate contact and guard ring

Substrate contact is added near the on-chip components, especially the active devices. The substrate contact keeps the potential of the bulk to ground in order to prevent latch-up of transistors. Guard ring is a substrate contact in a closed-loop form. It is used to isolate the devices from the substrate noise. Substrate noise is usually generated by the digital part. Substrate contact and guard ring used in the circuit are shown in figure3-18.



(a) (b)

Figure 3-18 (a) Substrate contact (b) guard ring

3.5.7 Simulation Results

The simulation of proposed QVCO is done by using Cadence environment. Cadence Design System provides an integrated circuit design environment for circuit simulation, layout and parasitic extraction. Post-layout simulation using SpectreRF is performed after RC extraction. Bondwire model shown in figure3-19 is added to the circuit simulation in order to model the effect of bondwire.

Figure 3-19 Bondwire model

3.5.7.1 Frequency and output power

Figure3-20 shows the output of the proposed QVCO with quadrature-phase relationship. The buffered output of the proposed QVCO is terminated with 50Ω loading in the simulation. The output power and oscillating frequency is simulated using Periodic-Static State Analysis. Figure3-21 indicates that the output power is about –10dBm at an oscillating frequency of 5.23GHz.

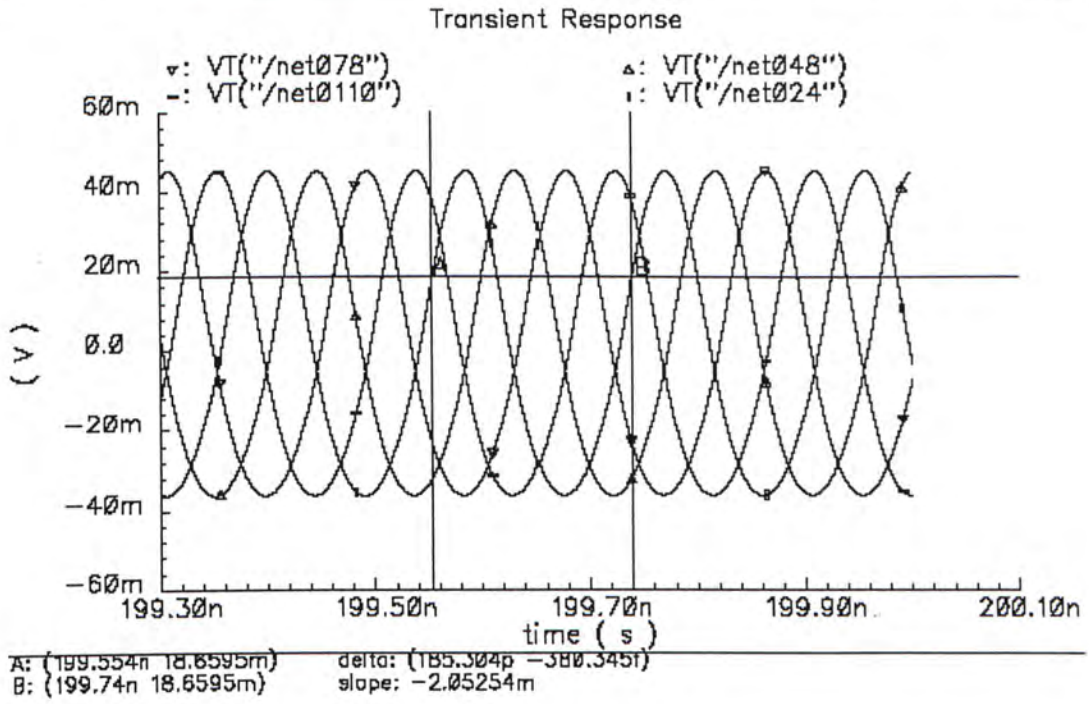


Figure 3-20 Simulated output waveform of the proposed QVCO

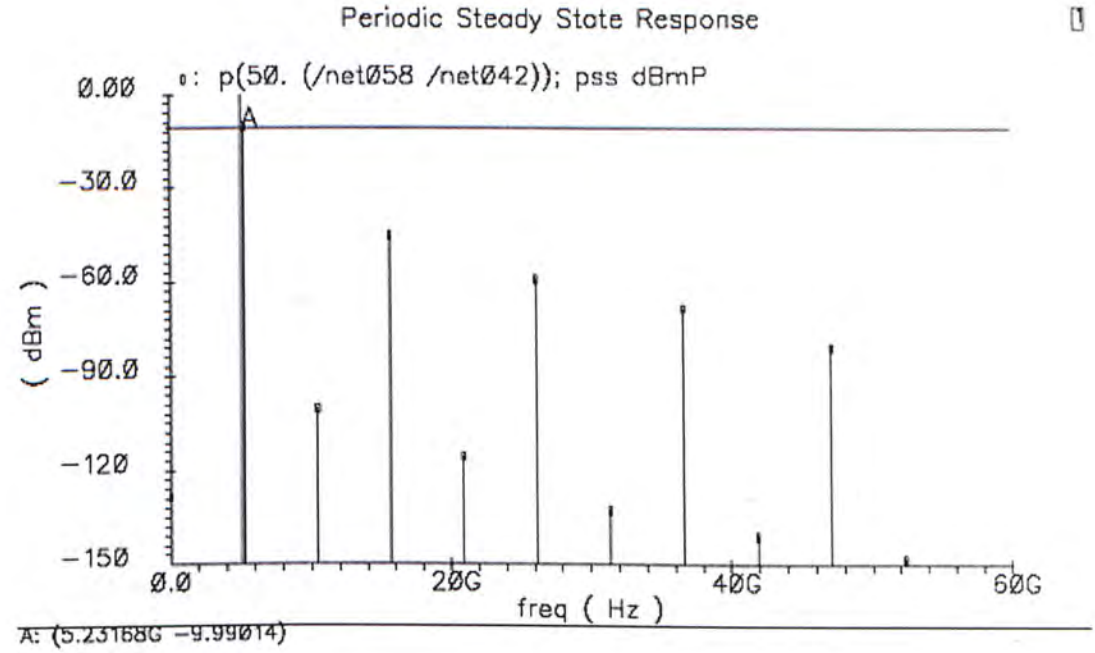


Figure 3-21 Simulated output spectrum of the proposed QVCO

3.5.7.2 Quadrature signal generation

The generation of quadrature signal requires that the second harmonic signals of two oscillators are in anti-phase. As shown in figure3-22, the anti-phase relationship is maintained by the cross-coupled pair through the back-gate of bias transistors.

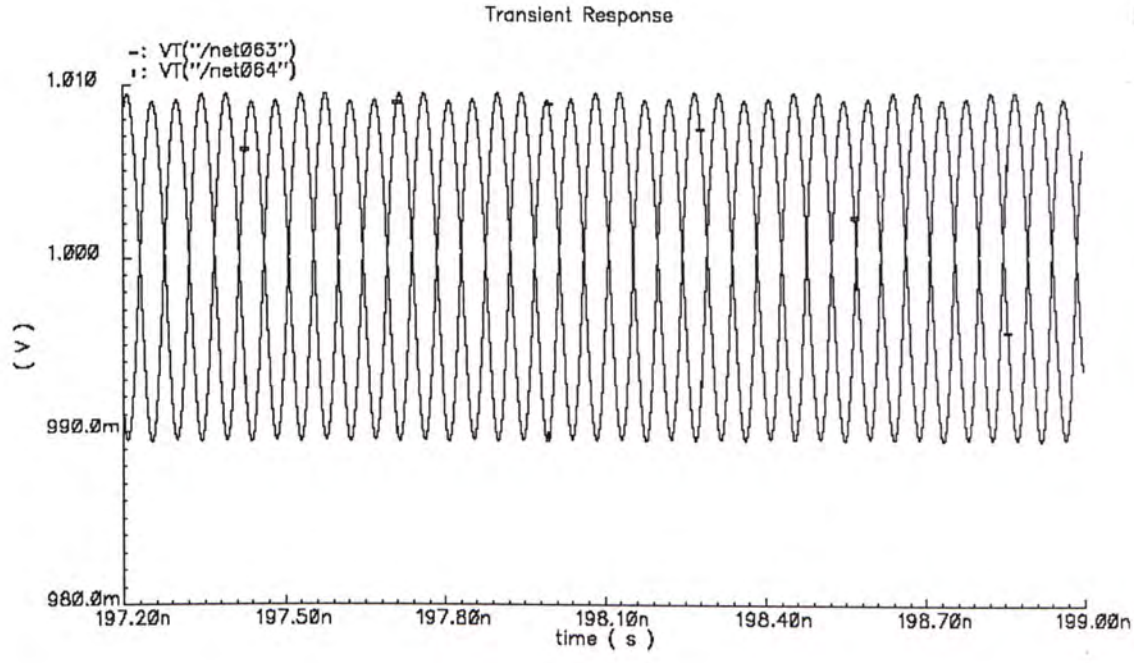


Figure 3-22 Simulated second harmonic of the proposed QVCO

3.5.7.3 Tuning range

The oscillating frequency ranges from 4.89GHz to 5.39GHz with control voltage varies between 0V and 1V (figure3-23). Tuning range is about 500MHz or 9.7% of the oscillating frequency. The proposed QVCO is able to use the whole

range of the varactor without using control voltage larger than the supply voltage.

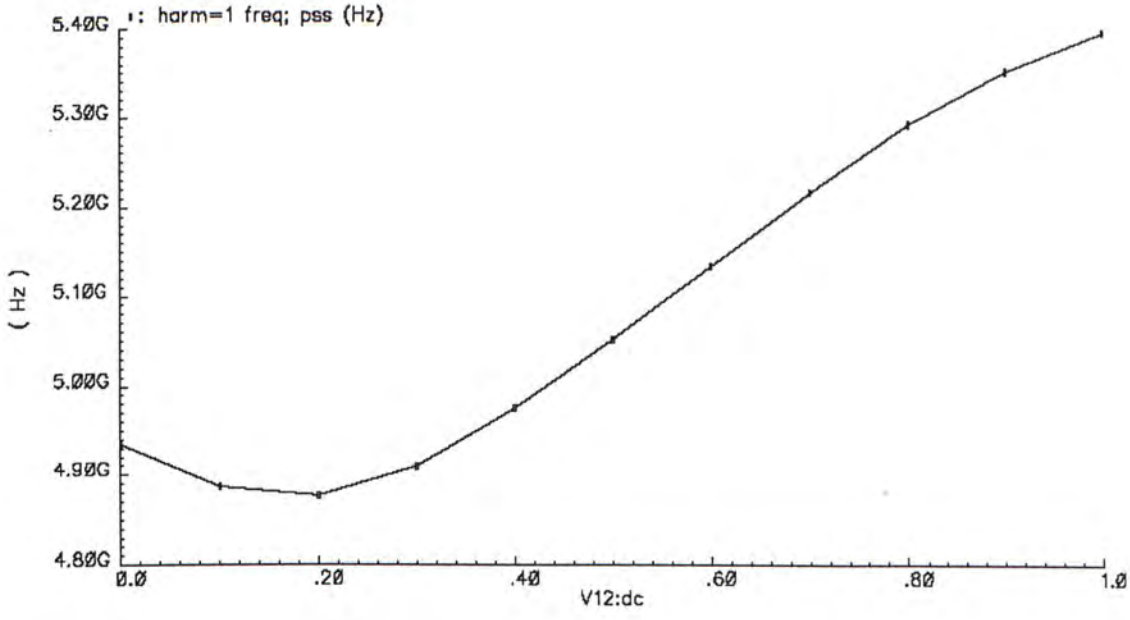


Figure 3-23 Simulated tuning range of the proposed QVCO

3.5.7.4 Power consumption

The simulated power consumption of the proposed QVCO is 3.4mW. New coupling mechanism without additional active devices and low supply voltage are the main reasons for the small power consumption. The four output buffers consume 4.9mW in order to drive the external load.

3.5.7.5 Phase noise

The phase noise of the proposed QVCO is simulated using Cadence Pnoise analysis. At 1MHz frequency offset from a 4.95GHz carrier, the phase noise is –111dBc/Hz as shown in figure 3-24. The Figure-of-Merit of the proposed QVCO can be calculated using equation (3.7) which equals 179dBc/Hz.

$$FoM = 10\log\left(\left(\frac{f_c}{\Delta f}\right)^2 \frac{1}{L(\Delta f)P}\right) \qquad (3.7)$$

$$= 10\log\left(\frac{4.95\times10^9}{1\times10^6}\right)^2 - 10\log(4) - (-111)$$

where f_c is the oscillation frequency, Δf is the offset frequency from carrier, $L(\Delta f)$ is the phase noise at Δf, and P is the power consumption.

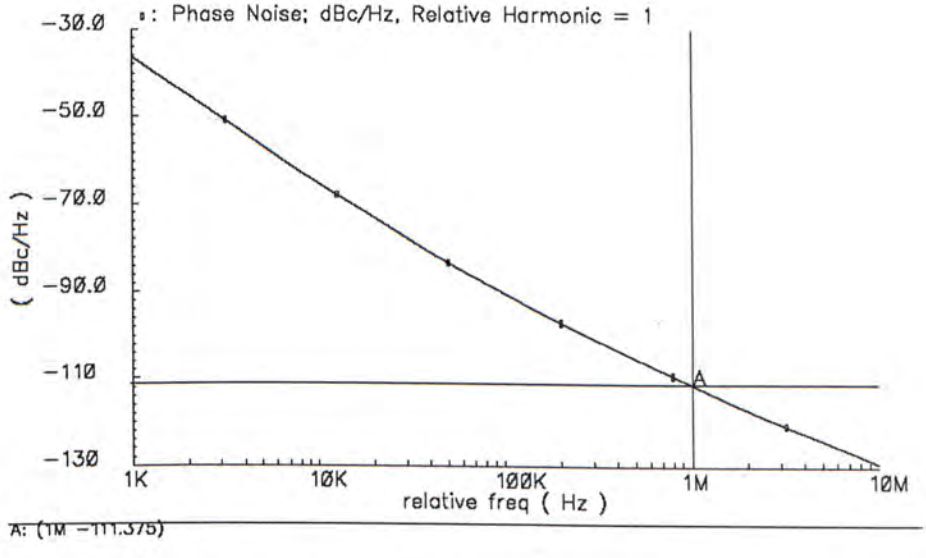


Figure 3-24 Simulated phase noise of the proposed QVCO

3.6 Polyphase filter and Single-sideband mixer design

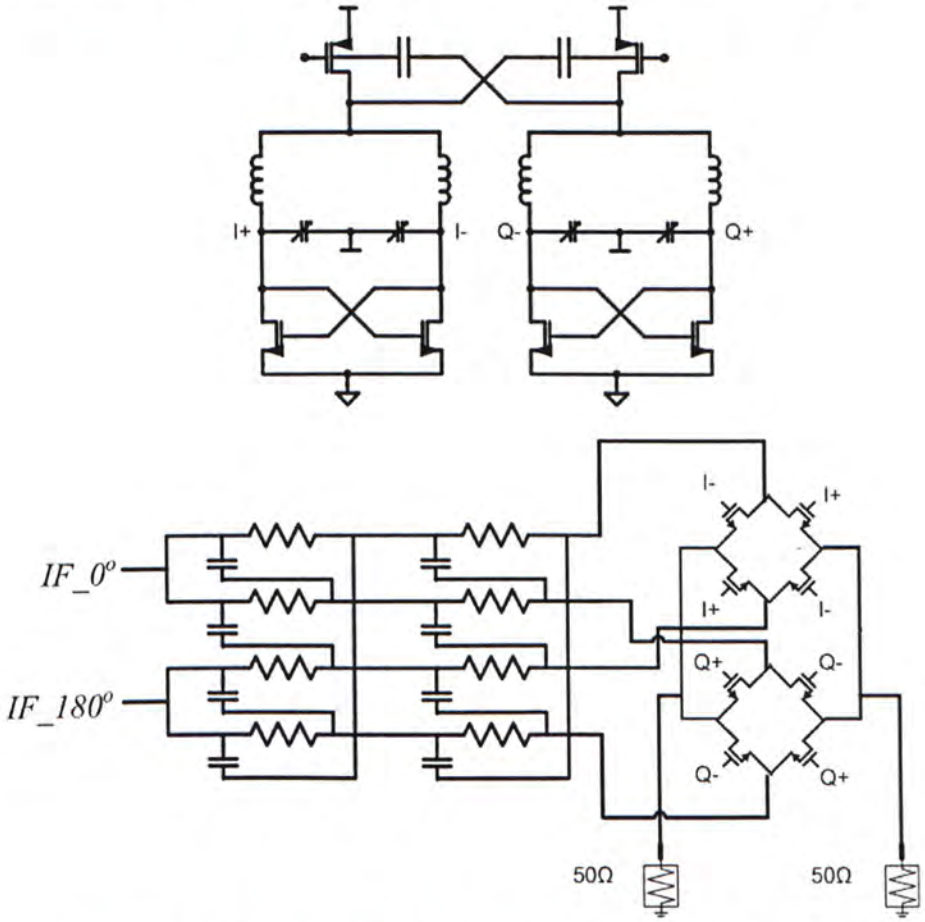


Figure 3-25 Schematic of the prototype measuring the IRR

In order to measure the phase error, a polyphase filter and a single-sideband mixer are used to measure the image-rejection ratio (IRR). Another prototype of the proposed QVCO is fabricated with on-chip IRR mixer and the baseband polyphase filter. A passive single-sideband mixer is composed of four commutating switches which up-converts the baseband quadrature signals with a 5-GHz carrier. As shown in figure 3-25, these two mixers are shorted together at the outputs to select only one

sideband. The mechanism of rejecting one of single-sideband generation starts with a baseband signal in quadrature,

$$BB-I = A_{BB}\sin(\omega_b t) \qquad (3.8)$$

$$BB-Q = A_{BB}\cos(\omega_b t) \qquad (3.9)$$

where A_{BB} is the amplitude of baseband signal. The LO signals are also in quadrature,

$$LO-I = \sin(\omega_{LO} t) \qquad (3.10)$$

$$LO-Q = \cos(\omega_{LO} t) \qquad (3.11)$$

After upconversion mixing, the outputs of the mixers become

$$RF-Q = A_{gain}A_{BB}\cos(\omega_b t)\bullet\cos(\omega_{LO} t) = \frac{A_{gain}A_{BB}}{2}(\cos((\omega_{LO}-\omega_b)t)+\cos((\omega_{LO}+\omega_b)t))$$

$$RF-I = A_{gain}A_{BB}\sin(\omega_b t)\bullet\sin(\omega_{LO} t) = \frac{A_{gain}A_{BB}}{2}(\cos((\omega_{LO}-\omega_b)t)-\cos((\omega_{LO}+\omega_b)t))$$

where A_{gain} is the conversion gain of the mixer. To select single-sideband, the I-Q mixer outputs are added together to yield,

$$RF = RF-I + RF-Q = A_{gain}A_{BB}\cos((\omega_{LO}-\omega_b)t)$$

Theoretically, the unwanted sideband can be completely rejected. However, due to the quadrature phase error in LO and IF and the mismatch in mixer, the unwanted sideband is not fully suppressed. The ratio between the wanted sideband and unwanted sideband can be used indirectly to measure the phase-error associated with LO signal, since it is much easier to reduce the mismatch at baseband. Hence, it may

be assumed that the IRR is mainly caused by the phase error in the LO signal.

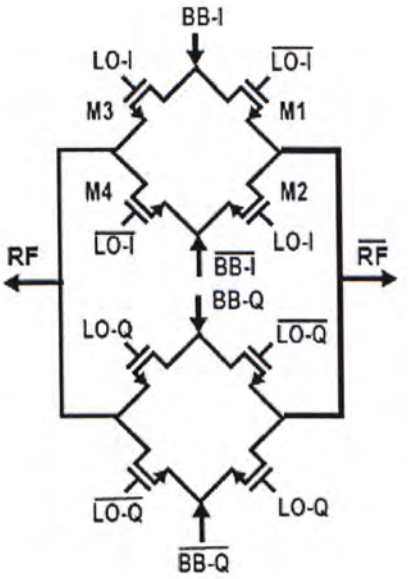


Figure 3-26 Schematic of a up-conversion single-sideband mixer

3.6.1 Polyphase filter

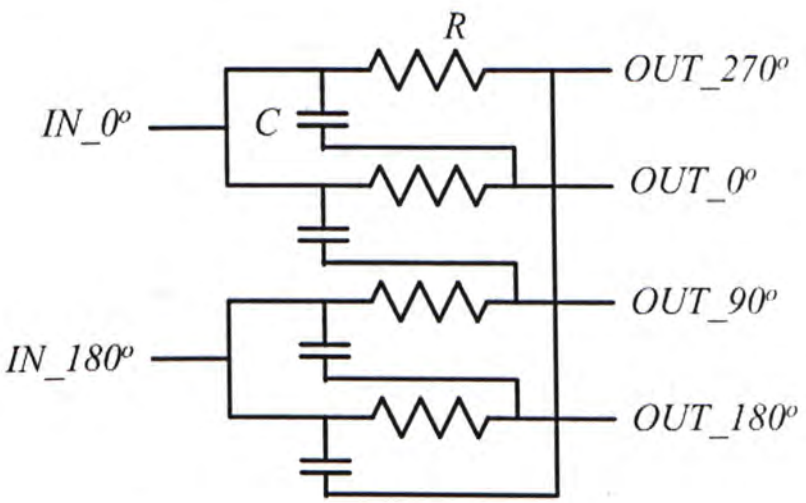


Figure 3-27 Schematic of a polyphase filter

The quadrature baseband signal is generated on-chip by using the polyphase

filter shown in figure 3-27 with differential input. At the frequency of 1/RC, the RC network shifts Vin_0o by -45° and Vin_180o by +45° to give,

$$V\_out = \frac{1}{\sqrt{2}} V_{in\_0} \angle -45^o + \frac{1}{\sqrt{2}} V_{in\_180} \angle +45^o$$

Polyphase filter is narrow-band since it generates the quadrature signals only at a frequency of 1/RC. As it is difficult to control value of passive on-chip components precisely and hence, hence cascade connection of two or more stages of polyphase filter may be needed for wider operating bandwidth. It is worth to note that the insertion loss of the polyphase filter is 3dB without output loading. With an output loading of 50Ω at the RF port of the mixer, the insertion loss is much larger than 3dB. In this work, a 2-stage polyphase filter is adopted and the center of operating frequency is 12MHz. The component values is listed in table2.

1st stage		2nd stage		
R	C	R	C	M_{mixer}
3kΩ	4.5pF	3.5kΩ	4.5pF	60/0.35

Table 2 Component values in 2-stage polyphase filter

3.6.2 Layout Consideration

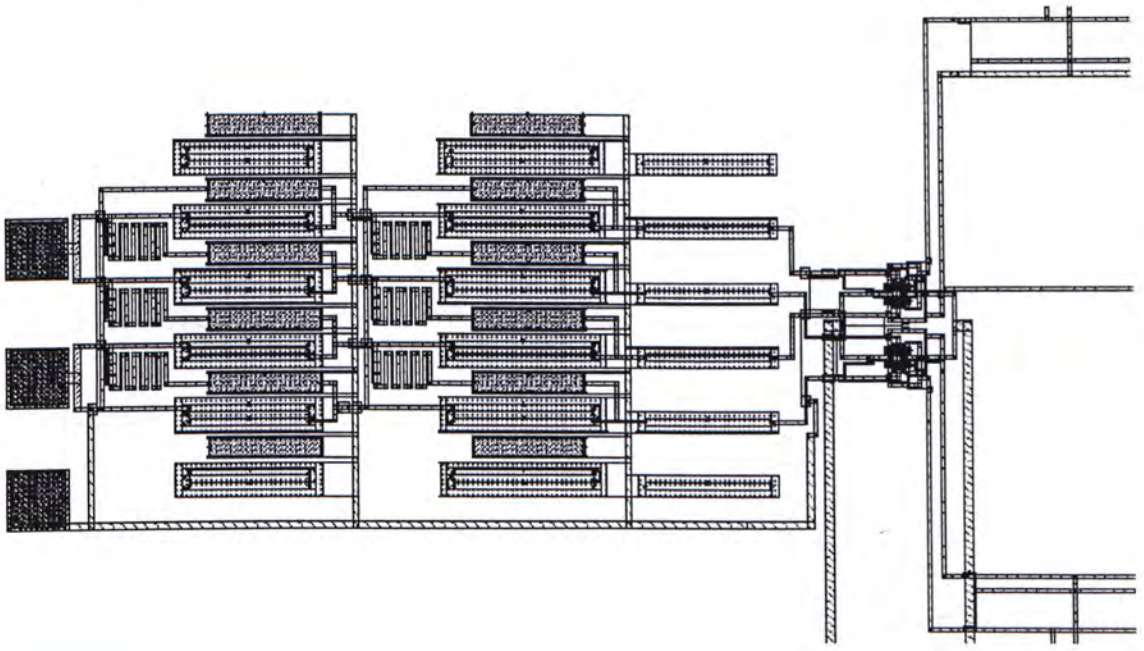


Figure 3-28 Layout of polyphase filter and SSB passive mixer

Layout of the polyphase filter and SSB passive mixer is shown in figure 3-28. Careful layout is important for the polyphase filter in order to produce quadrature IF signal accurately. All resistors and capacitors are laid out in the same orientation. As shown in figure 3-26, one of the four interconnections is much longer than the others and the number of crossing in four paths are different. Serpentine shape of interconnection [28] is used in order to provide design freedom to equalized different length and resistance. By scaling the length in each branch of the serpentine shape interconnection, four interconnections can be tuned to be equal in length.

Parasitic capacitance is caused by the crossing of different metal layers. It can be seen that in figure 3-29, the bottom path crosses the other three paths and its parasitic capacitance is different to the others. To equalize the parasitic capacitance associated with the four paths, a grounded isolating metal plate is inserted between different metal layers. Therefore, the parasitic capacitance between the metal line and ground is made equal for four paths.

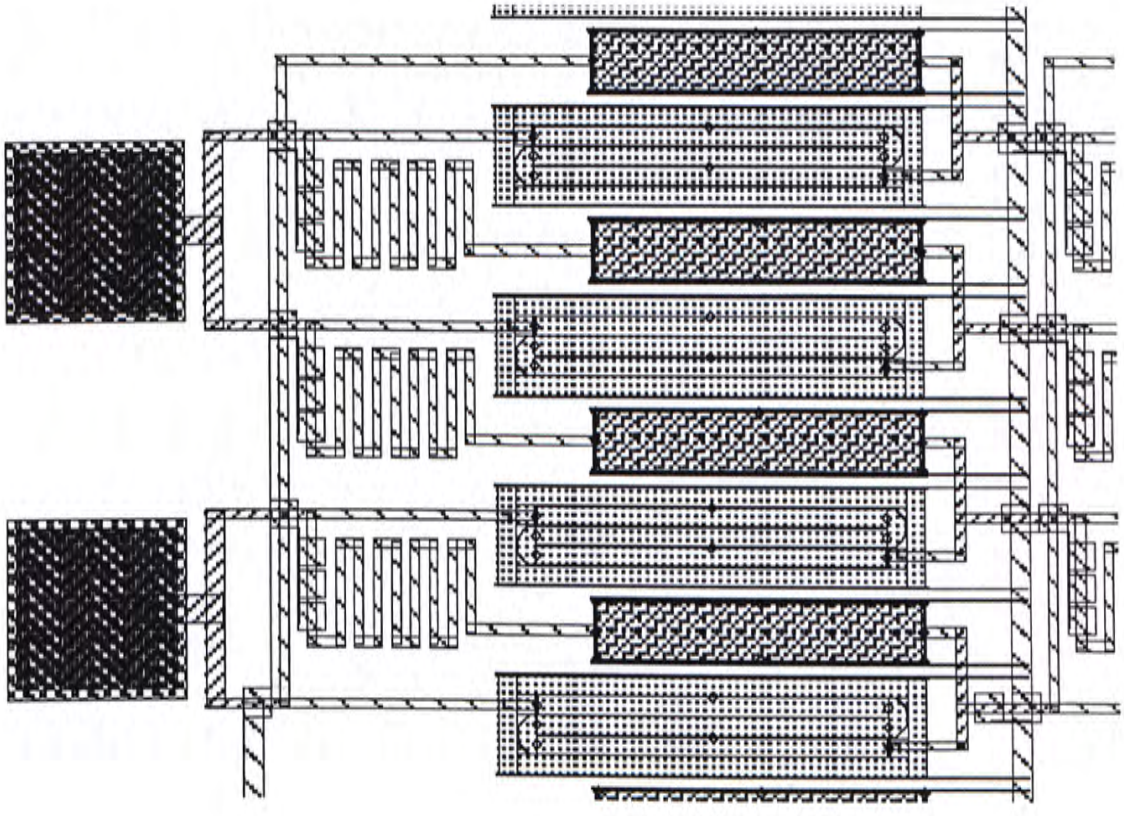


Figure 3-29 Serpentine shape interconnection and grounded metal plates

Besides, the physical dimension of the resistor and capacitor also plays an important role in polyphase filter design. Large value of resistance and capacitance is

used for improved matching but they occupy large chip area. Common-centroid is a common way to improve the matching of devices. However, this method complicates the interconnection and increases the number of metal crossing. Therefore, the polyphase filter is laid out in uncommon-centroid.

LO signals in quadrature phase drive the gate of the passive mixer. All four interconnection between the QVCO output buffer and mixer are equal in length (to equalize the parasitics). Also, grounded metal plates are added to ensure equal number of crossings. The layout of passive mixer (eight transistors) is highly symmetrical to improve the matching.

3.6.3 Simulation results

Post-layout simulation is done using the Cadence simulator. Since IRR depends on quadrature accuracy of both IF and LO signals, the quadrature signal generated by the polyphase filter is first examined. If ideal quadrature LO signal applied to the passive mixer, the resulting IRR will reflect the effect caused by the mismatch of polyphase filter and mixer. Simulation result shows that the polyphase filter and mixer is able to achieve an IRR of 41dB which corresponds to a phase error of 1^{o}. Therefore, it can be assumed that the overall IRR is mainly caused by the phase error

associated with the QVCO. Figure 3-30 indicates that the simulated IRR with proposed QVCO is approximately 33dB which corresponds to a phase error of 5^{o}.

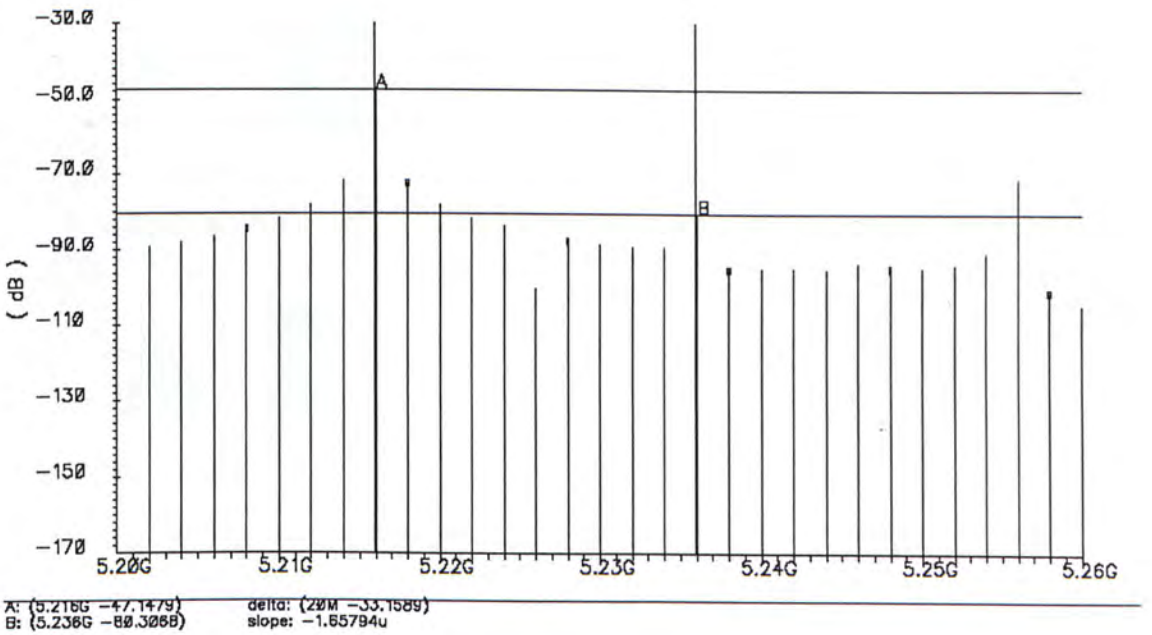


Figure 3-30 IRR of post-layout simulation with proposed QVCO

3.7 Comparison with parallel-coupled QVCO

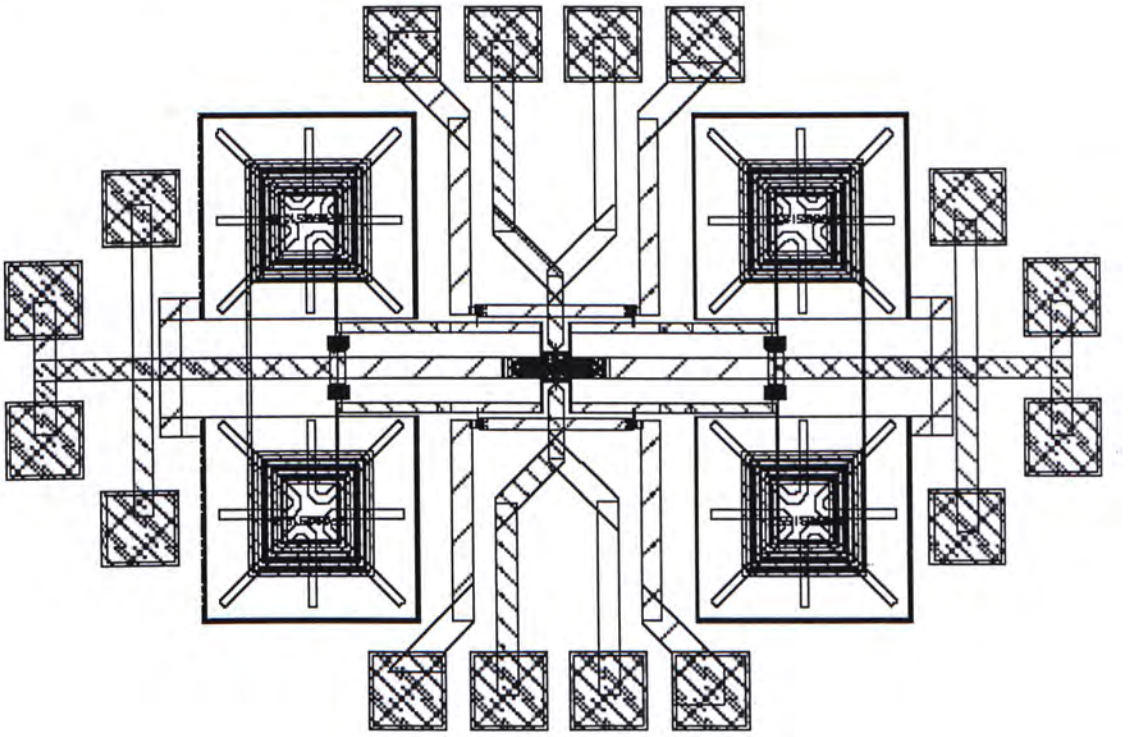


Figure 3-31 Layout of a parallel-coupled QVCO

A parallel-coupled QVCO is also simulated and its performance are compared with the proposed design. The layout of the parallel-coupled QVCO is given in figure 3-31. This QVCO is used to compare with proposed QVCO performance. Since the parallel-coupled architecture is not able to operate at 5GHz, a 1.8GHz version is designed using AMS 0.35μm CMOS technology. In table 3, the two QVCOs are compared in terms of operating frequency, power consumption and FoM.

	Proposed QVCO	**Parallel-coupled QVCO**
Operating frequency (GHz)	4.89-5.39	1.62 - 1.82
Power consumption (mW)	3.4	22.8
Supply Voltage (V)	1	2
Phase noise @ 1MHz offset (dBc/Hz)	-111	-114
FoM (dBc/Hz)	179	165
IRR (dB)	33	N.A.

Table 3 Simulated performance of proposed QVCO and parallel-coupled QVCO

The proposed QVCO exhibits superior performance, in compared to the conventional parallel-coupled QVCO, with higher operating frequency, lower power consumption and supply voltage. Phase noise of the proposed QVCO is 3dB higher than the parallel-coupled QVCO. FoM of the proposed QVCO is 14dB higher than the parallel-coupled QVCO. Since there is no on-chip passive mixer and polyphase filter implemented with the parallel-coupled QVCO, no information can be obtained to compare their quadrature accuracy.

Chapter 4

Experimental results

Three test circuits (proposed QVCO, QVCO with polyphase filter and SSB mixer, and parallel-coupled QVCO) are designed and fabricated using AMS 0.35μm 4M2P standard CMOS process. Microphotographs of three circuits are given in figure4-1, figure4-2 and figure4-3. These circuits are tested using FR4 test fixture. They are in form of bare die without package to minimize the parasitic effect of the package. Conductive silver epoxy is used to attach the bare die to the evaluation board. Bondwire is used to connect the pads of circuit and the evaluation board. The parasitic effect of bondwire has been considered in the simulation.

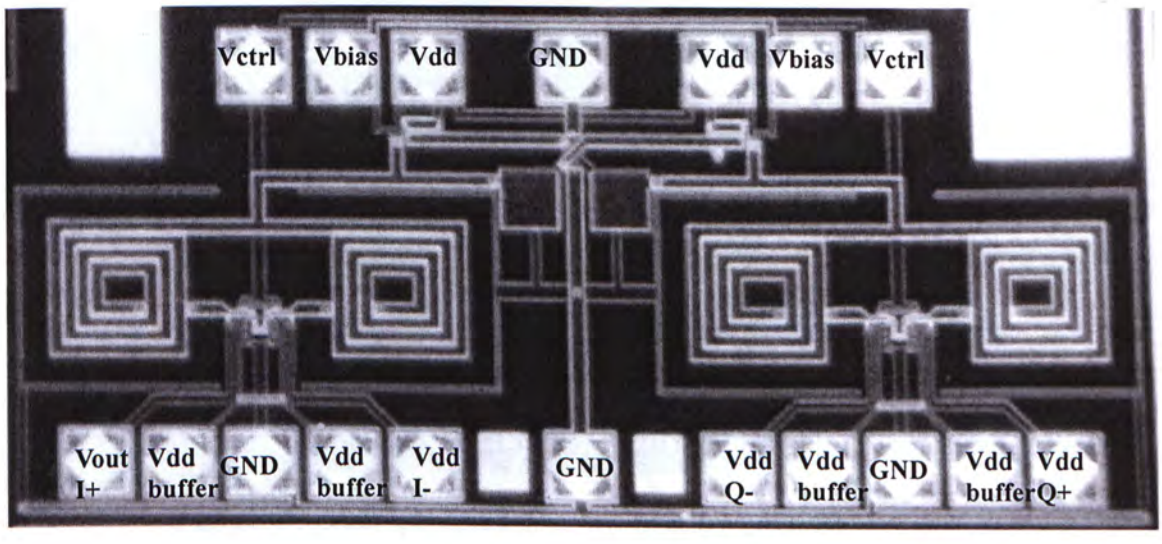


Figure 4-1 Microphotograph of the proposed QVCO

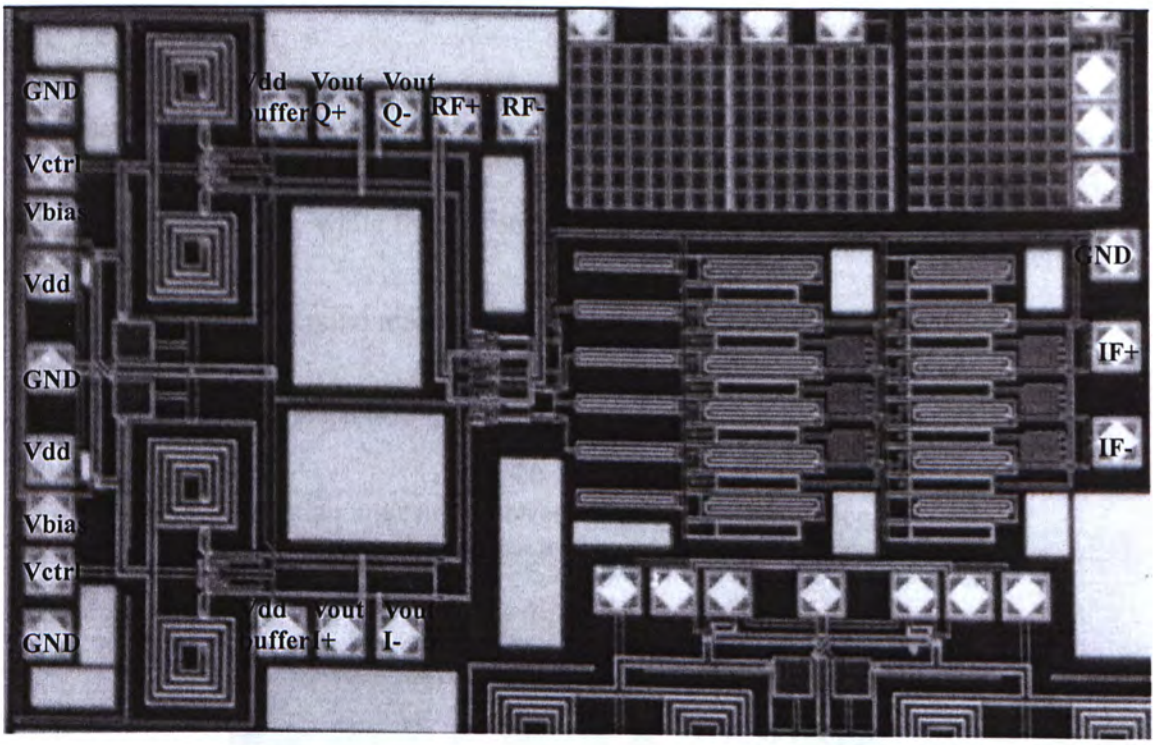


Figure 4-2 Microphotograph of the QVCO with polyphase filter and SSB mixer

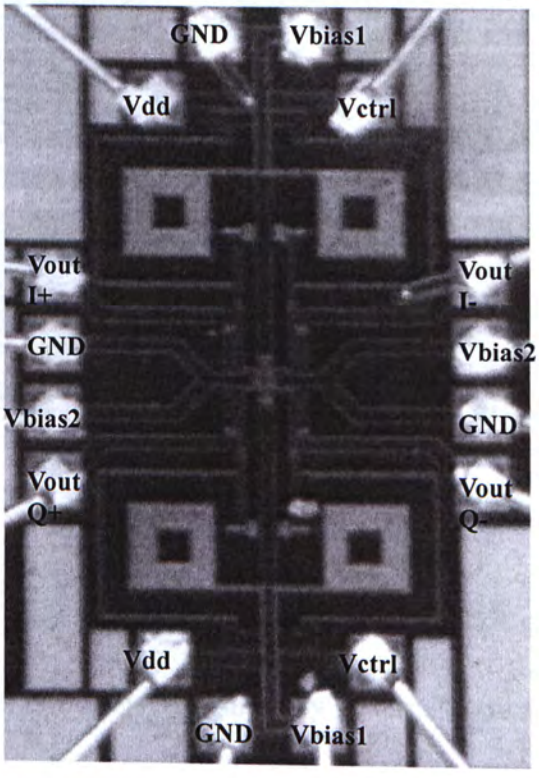


Figure 4-3 Microphotograph of the parallel-coupled QVCO

4.1 Test Fixture

Test fixture is made of the doubled-sided gold-plated FR4 PCB. The PBC layout is shown in figure 4-4, while the bottom layer is used as the ground plane. Vias are added to connect the ground made on the top layer and the ground plane. The ground pads of the chip is connected to the top ground plane using bondwire. All bondwires are kept short to minimize undesirable effect such as supply bounce.

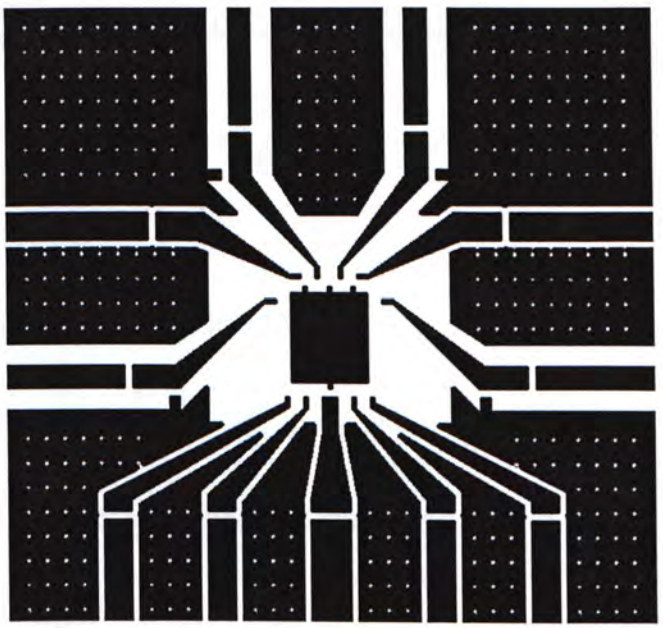


Figure 4-4 The layout of PCB for measurement

DC bias for the circuit is provided by external power supply. Decoupling capacitors are used to filter out the supply noise. Filtering of supply noise is important for VCO measurement, as the noise in the control voltage may modulate

the output frequency through the capacitance of the varactor. Similarly, noise in the bias voltage may modulates the bias current of the oscillator. Surface-mount capacitor of 10μF is used as decoupling capacitor.

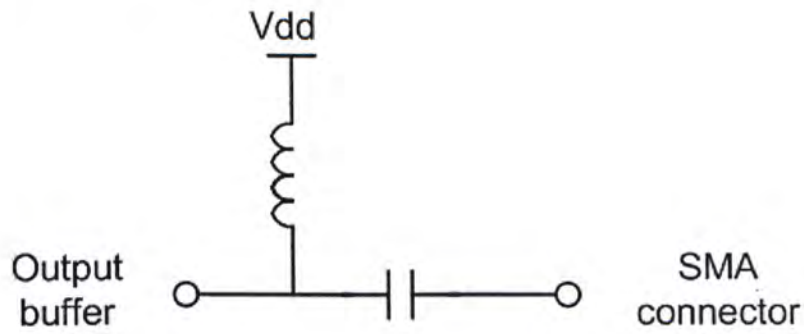


Figure 4-5 A schematic of bias-T

RF signal is delivered to the 50Ω input of the measurement equipment through a bias-T. Bias-T is composed of a RF choke and a DC blocking capacitor shown in figure4-5. Bias-T is used to provide bias current for the output buffer and allows the oscillator output signal to be coupled to the 50Ω. It is implemented using surface-mount passive components in this test fixture. SMA connectors are used to connect the output port of the QVCO to the measuring equipment.

4.2 Measurement set-up

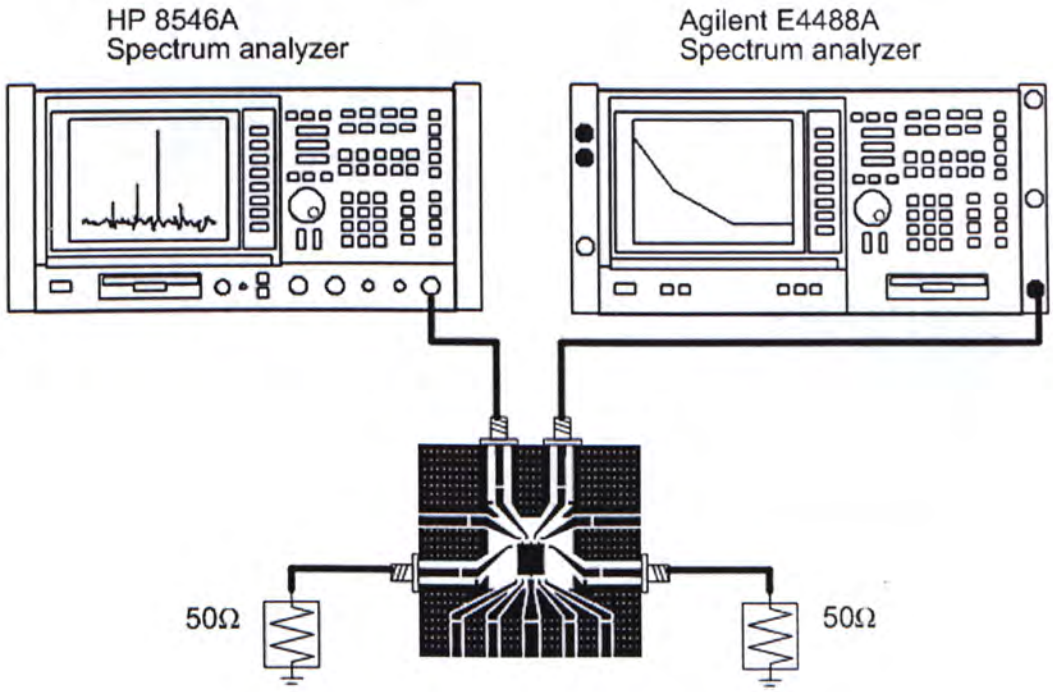


Figure 4-6 Measurement set-up for the output spectrum and phase noise

Figure4-6 shows the measurement set-up for output spectrum measurement and phase noise measurement. The single-end output of the QVCO is measured and the other outputs of QVCO are terminated with a match load. A spectrum analyzer (HP 8546A) is used to obtain the output spectrum of the QVCO output. Phase noise is measured with Agilent E4448A spectrum analyzer. The DC power supply (HP E3620A) is used to provide biasing voltage and biasing current to the DUT.

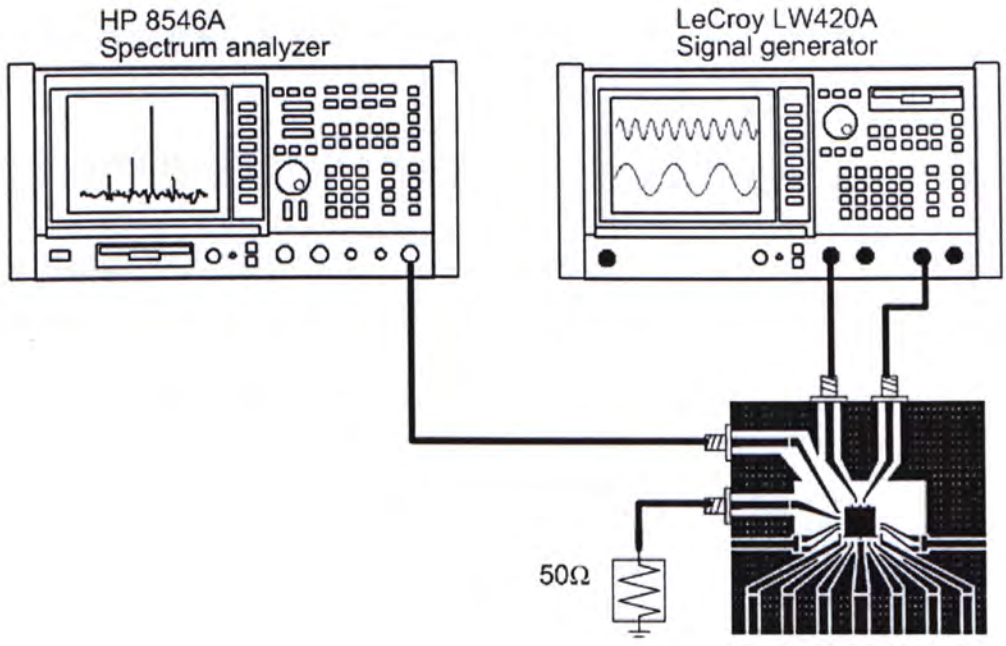


Figure 4-7 Measurement set-up for the image-rejection ratio

Figure4-7 shows the measurement set-up for image-rejection ratio. A signal generator (LeCroy LW420A) is used to generate the differential input signal to the polyphase filter. The DC power supply (HP E3620A) is used to provide biasing voltage and biasing current to the DUT. Spectrum analyzer (HP 8546A) shows the frequency spectrum of IRR at the output port of the upconversion passive mixer.

4.3 Measurement results

4.3.1 Proposed QVCO using back-gate superharmonic coupling

4.3.1.1 Output Spectrum

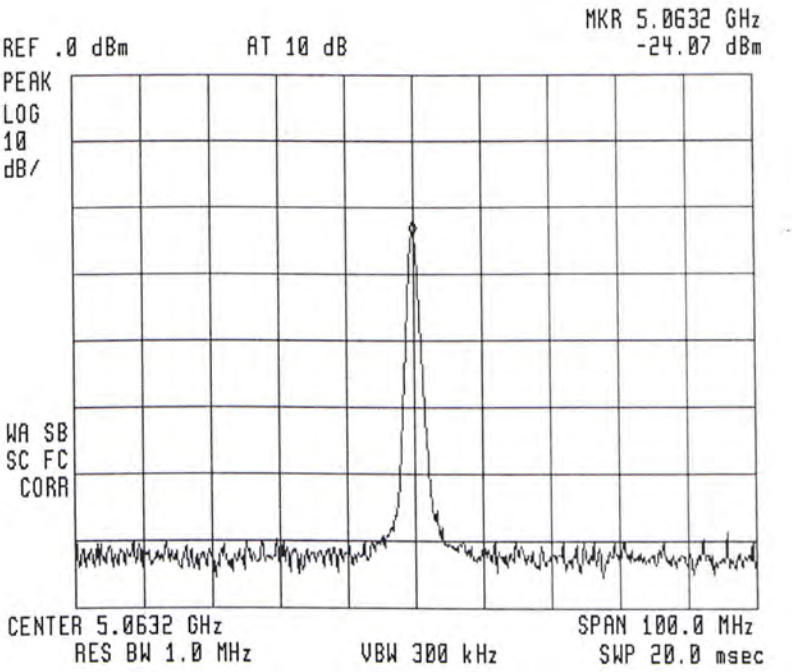


Figure 4-8 Measured output spectrum of proposed QVCO prototype

Figure4-8 shows the frequency output spectrum of the proposed QVCO prototype. The output power is –24dBm at an oscillating frequency of 5.06GHz. The output power can be increased by using a larger output buffer or more buffer stages.

4.3.1.2 Tuning range

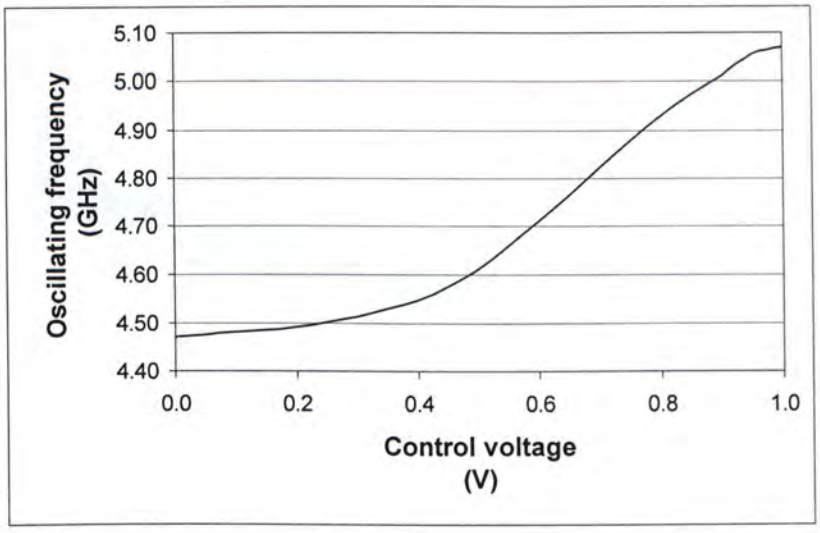


Figure 4-9 Measured tuning range of proposed QVCO

Figure4-9 shows the tuning range of proposed QVCO. The oscillating frequency of the proposed QVCO covers 4.47-5.08 for control voltage varying from 0V to 1V. The tuning range is about 12% of the oscillating frequency. Measured oscillating frequency is lower than the simulated results by about 300MHz. This 10% frequency shift corresponds to parasitic capacitance about 58fF at 5GHz frequency range. This small value of capacitance may come from inaccurate device models used in the simulation and inaccurate parasitic extraction in layout. A larger tuning range of QVCO can be designed to cover this variation.

4.3.1.3 Phase noise

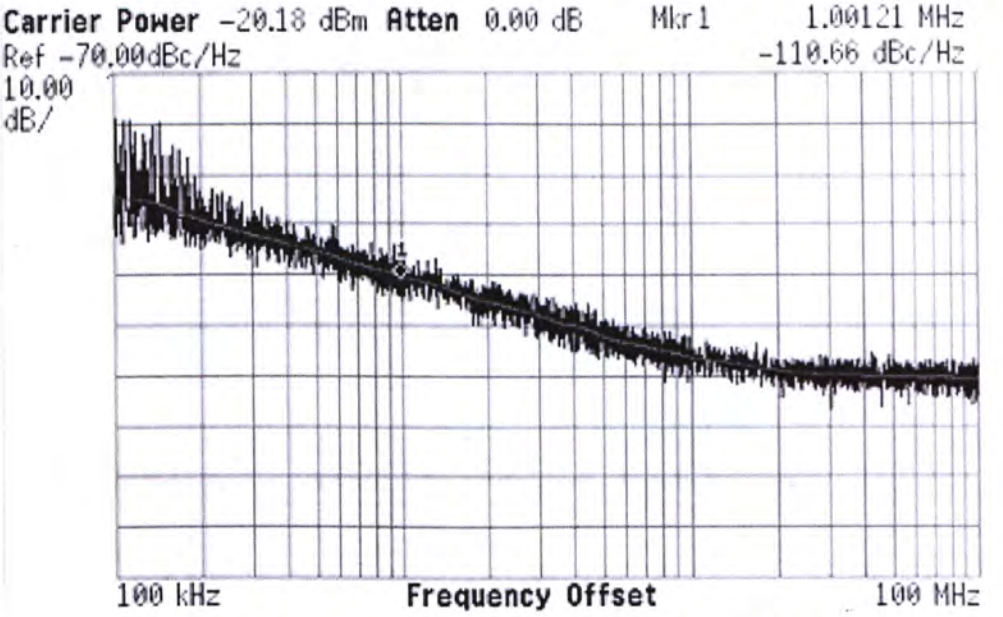


Figure 4-10 Measured phase noise of proposed QVCO

The measured phase noise is found (figure 4-10) to be –110.6dBc/Hz at 1MHz offset from a 4.83GHz carrier. The phase noise is measured at control voltage of 0.7V where the tuning characteristic is the steepest and the QVCO is most susceptible to noise in control voltage. The measured phase noise is 1dB higher than the simulated result.

4.3.1.4 Power consumption

The core of the proposed QVCO draws 4mA from a 1V power supply. Measured power consumption is 0.6mW higher than the simulation result.

4.3.1.5 Image-rejection ratio

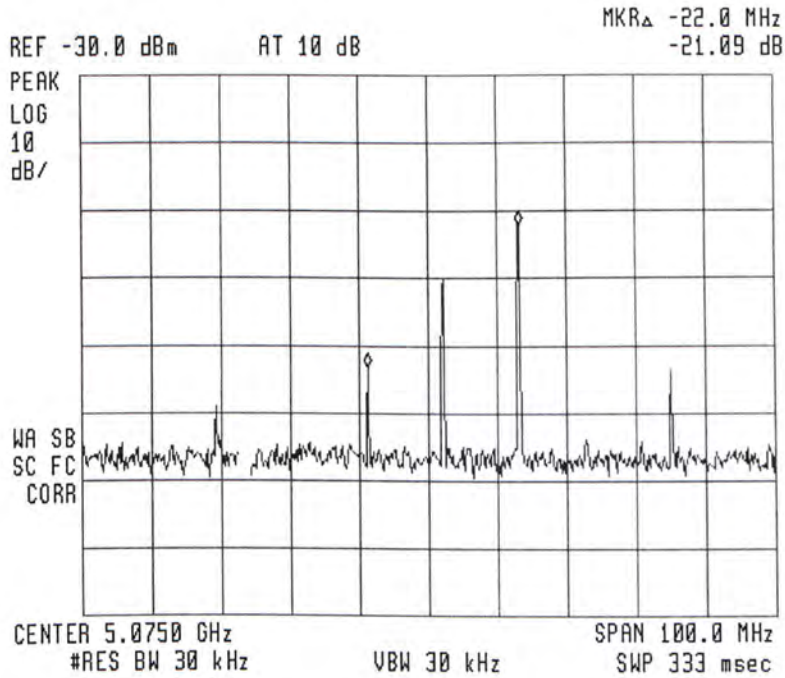


Figure 4-11 Measured image-rejection ratio

In this experiment, differential signal of 11MHz is injected into the input port of the polyphase filter. When the QVCO is oscillating at 5.07GHz, the measured image-rejection ratio is 21dB as depicted in figure 4-11. The measured image-rejection ratio is 12dB lower than the simulation result. It is believed that the discrepancy between simulated and measured IRR is caused by the external inductive loading. Since the bondwire, the external components and the PCB routing are hard to achieve a good matching, it is recommended to use on-chip inductor as load for output buffer or not to use output buffer in measuring the IRR.

4.3.2 Parallel-coupled QVCO

4.3.2.1 Output spectrum

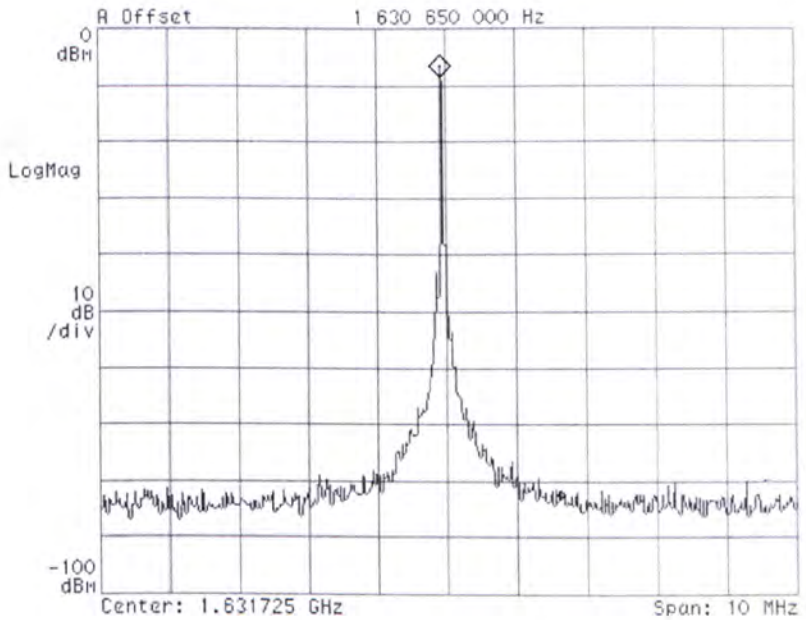


Figure 4-12 Measured output spectrum of the parallel-coupled QVCO

The measured output spectrum is given in figure 4-12. The output power is –8dBm at an oscillating frequency of 1.63GHz.

4.3.2.2 Power consumption

The parallel-coupled QVCO prototype draws 25.5mA from a 2V supply. The measured power consumption is 51mW and is 28.2mW larger than the simulation result. If the QVCO is forced to operate at a lower current, the two differential VCOs will give an unlocked output spectrum. For proper operation, the coupling between

two differential VCOs must be increased and hence, more current is drawn by the coupling transistors.

4.3.2.3 Tuning range

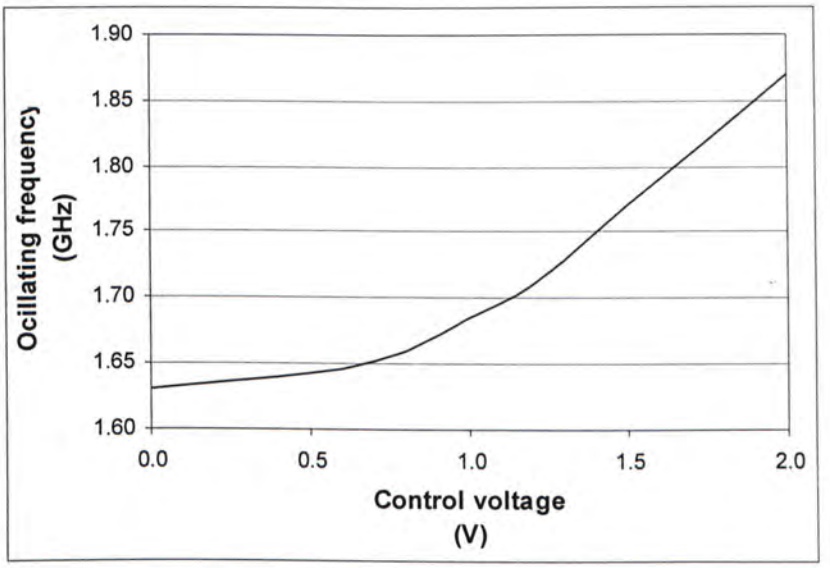


Figure 4-13 Measured tuning range of the parallel-coupled QVCO

Figure4-13 depicts the measured tuning range of the parallel-coupled QVCO. The oscillating frequency covers 1.63GHz to 1.87GHz with control voltage varying from 0V to 2V. The tuning range is 120MHz and is about 6.8% of the oscillating frequency.

4.3.2.4 Phase noise

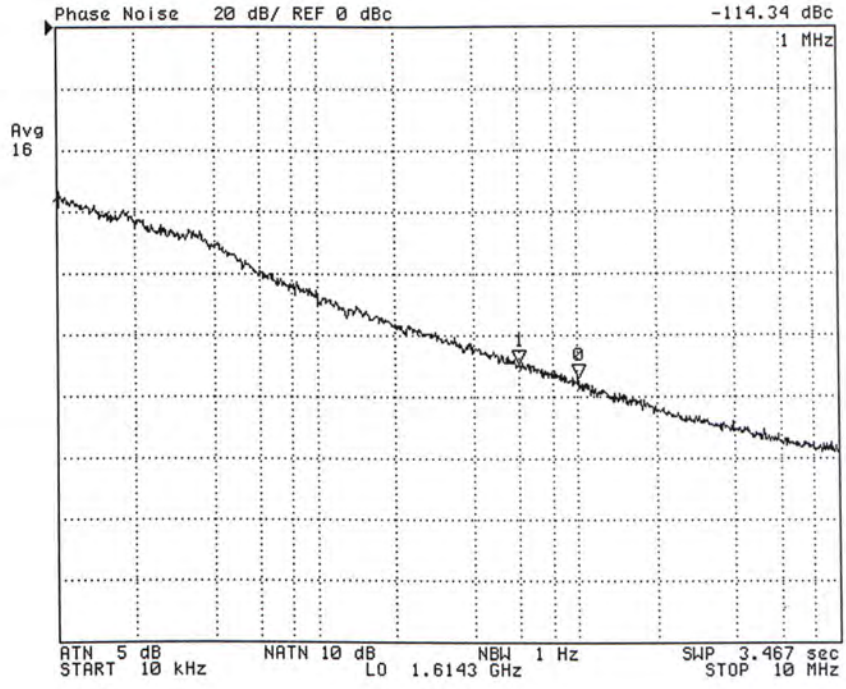


Figure 4-14 Measured phase noise of the parallel-coupled QVCO

The measured phase noise of the parallel-coupled QVCO is shown in figure4-14. The measured phase noise is –114.3dBc/Hz at 1MHz offset from a 1.61GHz carrier and is 0.3dB lower than the simulation result.

4.3.3 Comparison between proposed and parallel-coupled QVCO

	Proposed QVCO	Parallel-coupled QVCO
Operating frequency (GHz)	4.47-5.08	1.63-1.87
Power consumption (mW)	4	51
Supply Voltage (V)	1	2
Phase noise @ 1MHz offset (dBc/Hz)	-110.6	-114.3
FoM (dBc/Hz)	179	165
IRR (dB)	21	N.A.

Table 4 Summary of measurement results

Table 4 shows the comparison between the proposed QVCO using back-gate superharmonic coupling and the parallel-coupled QVCO. With the same fabrication process, the proposed QVCO can offer a new circuit topology to operate at a much higher frequency with lower supply voltage and power consumption Phase noise performance of the proposed QVCO is close to (2dB higher) the specification of IEEE WLAN 802.11a. The phase noise performance can be improved by increasing the power consumption or using a spiral inductor with higher quality factor.

The performance of the proposed QVCO is also compared with the recently published works (table 5). Most QVCO designs can only operate below 3GHz which is limited by the parasitic capacitance of coupling transistor, particularly for 0.35μm CMOS process in which the gate capacitance is too large for high frequency operation. The proposed QVCO provides a possible topology for 5GHz operation with 0.35μm standard CMOS process. The FoM of proposed QVCO is comparable to the recently published works.

Ref.	Oscillation Frequency (GHz)	FoM	Supply Voltage (V)	Power (mW)	Technology (μm)
[23]	0.79-0.91	149	3	30	1
[24]	1.64-1.97	178	2	50	0.35
[25]	4.60-5.20	184	2.5	22	0.25
[29]	1.05-1.39	174	1.8	5.4	0.18 triple-well
This Work	4.47-5.08	179	1	4	0.35

Table 5 Comparison between proposed QVCO and recently published works

Chapter 5

Conclusions

5.1 Conclusions

Modern transceiver architectures require quadrature LO signal for performing image-rejection, vector modulation and demodulation. Trade-off between different design parameters in QVCO for low noise, high operating frequency and low power consumption, has become a challenging problem in fully-integrated transceiver design. The main objective of this research is to seek for a new QVCO topology with high performance.

In this work, major components in focusing the resonator (varctor and spiral inductor) and different phase noise models of oscillators are studied. Design techniques for VCO and QVCO are also addressed. A QVCO using a novel superharmonic coupling is proposed for high frequency operation. The proposed coupling method adopts the back-gate injection to get rid of the coupling transistors or transformers. Back-gate of PMOS transistors is used for injection locking between two differential oscillators at the second harmonics. Improved phase noise performance is resulted with the smaller flicker noise of PMOS transistor having lower flicker noise. The proposed design also occupies less chip area than the

transformer-based super-harmonic coupling topology. The proposed circuit is simulated and fabricated using AMS 0.35μm double-poly four-metal standard CMOS process. The circuit occupies chip area of 0.5mm × 1.5mm. The measured results show that the proposed QVCO covers the frequency range from 4.47GHz to 5.08GHz. The core of the proposed QVCO draws 4mA from 1V supply. The proposed QVCO is found to have FoM of 179.

Phase error is measured by means of image-rejection ratio. Another prototype of proposed QVCO is fabricated with on-chip polyphase filter and passive SSB mixer. Experimental results show that the image-rejection ratio is 21dB after up-conversion to 5GHz frequency range. Also, a parallel-coupled QVCO is fabricated and tested for performance comparison.

5.2 Future work

QVCO is often used to generate LO signal for a fully-integrated transceiver. However, the output of a standalone QVCO is unstable and cannot meet the stringent phase noise requirement for most wireless applications. A solution is to implement a PLL-based LO synthesizer. Two critical components in a PLL deisgn are the VCO and the prescalar as they operate at the maximum frequency and consumes most power. By implementing a prescalar to operate at 5GHz and 1V supply voltage, a fully-integrated CMOS PLL can then be designed for 5GHz applications. Low-power and low voltage operation is the trend of RFIC design for longer battery and higher integration.

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