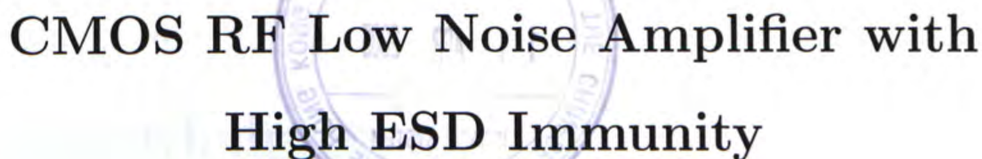

CMOS RF Low Noise Amplifier with High ESD Immunity

TANG SIU KEI

A THESIS SUBMITTED IN PARTIAL FULFILLMENT

OF THE REQUIREMENTS FOR THE DEGREE OF

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IN

ELECTRONIC ENGINEERING

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In this thesis, a new Electro-Static Discharge (ESD) protection method, which is called Common-Gate Input Stage Method (CGISM), is introduced for CMOS RF Low Noise Amplifier (LNA). It utilizes a common-gate amplifier as an input stage to reduce the possibility of the gate oxide breakdown. The major reason for this improvement is that the RF input is connected to the source of the transistor, instead to the gate in CGISM. As a result, it increases ESD immunity of the new LNA by preventing the ESD current from discharging through the thin gate oxide. In addition, the proposed method does not degrade of the LNA performance.

To verify the feasibility of the proposed CGISM circuit to protect CMOS RF LNA, a 1.8 GHz ESD-protected LNA with CGISM and a traditional common-source LNA have been fabricated using an AMS 0.35-μm CMOS technology. In the Human Body Model (HBM) ESD test, the proposed ESD-protected LNA is proved to be capable of surviving positive ESD pulse up to 1.5 kV and negative ESD pulse down to –3.5 kV. In contrast, the common-source LNA can only survive ESD pulse from -200 V to 200 V. These measurement results show the functionality of CGISM. It can substantially improve the ESD immunity of LNA.

Regarding the LNA performance, the measurement results show that the proposed LNA demonstrates a typical performance at 1.5 V low supply voltage.

The power gain, noise figure, input-referred 1-dB compression point and input third-order intercept point (IIP3) are approximately 13.7 dB, 5.3 dB, -16.6 dBm and -7.8 dBm, respectively. The new LNA has the measured performance as good as conventional designs.

摘要

本論文爲 CMOS 射頻電路中的低雜訊放大器提供了一種稱爲共柵輸入級 (CGISM) 的新靜電 (ESD) 保護技術。它使用了一個共柵放大器作爲輸入級，能夠大大減少柵氧化層被擊穿的概率。這是由於射頻電路的輸入不是連接在共柵輸入級中電晶體的柵極，而是連接在電晶體的源極。因此，通過阻止靜電電流經較薄的柵氧化層放電，這大大提高了低雜訊放大器電路的靜電保護性能。同時，提出的保護技術能維持低雜訊放大器的原有性能。

爲了驗證本文提出的 CMOS 射頻電路低雜訊放大器共柵輸入級技術的可實現性，我們使用 AMS 0.35 微米 CMOS 製造工藝設計了兩個低雜訊放大器，一個爲 1.8 千兆赫茲，帶有共柵輸入級靜電保護，另一個則是傳統的低雜訊放大器。在人體模型 (HBM) 靜電測試中，本文的設計能夠正常工作在-3.5kV~1.5kV 的靜電脈衝下；與此相比，傳統的共源低雜訊放大器只能工作在-200V~200V 的有限範圍內。測試結果證明了本文提出的共柵輸入級電路能夠有效的提高低雜訊放大器的靜電保護能力。

同時，在性能方面，測試結果顯示本文設計的低雜訊放大器在 1.5V 的低輸入電壓下顯示出普遍的性能。能量增益，雜訊形狀，輸入-1dB 功率飽和點以及輸入三階截距點（IIP3）分別爲 13.7dB，5.3dB，-16.6dB 和-7.8dB，這新的低雜訊放大器具有和傳統設計同樣的測量性能。

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Chapter 1

Introduction

1.1 Overview of Electrostatic Discharge

Electro-Static Discharge (ESD) is a rapid, spontaneous transfer of electrostatic charge induced by a high electrostatic field. Usually, the charge flows through a spark between two bodies at different electrostatic potentials as they approach to each other. When a charged object with a very high voltage touches a material of a low voltage, the ESD event occurs. In this situation, the electrostatic field built up across the material is very substantial. Thus, there is a sudden increase in current through the material. Even if the material is non-conductive, the hazardous ESD can lead to the insulator breakdown. Consequently, the insulator is destroyed.

1.1.1 Classification of Electrostatic Discharge Models

In the investigation of the ESD events, it is found that they can be classified into three groups of models [1], depending on the characteristics of the current pulses discharged. The three categories are: 1) Human Body Model, 2) Machine Model and 3) Charged-Device Model.

1) The Human Body Model (HBM) represents a charged human body, which discharges accumulated static charge through a device to ground. It is defined by the ESD association standard *ANSI/ESD STM5.1* [2]. Figure 1.1 shows the

schematic of HBM and the waveform of the ESD current pulse generated from the pre-charged capacitor, which discharges to device under test (DUT). Actually, HBM is a simple RC first-order circuit, so its current pulse is an approximate curve of exponential decay. The important parameters that are used to characterize the HBM ESD pulse are its peak current I_p and rise time tr, which are 1.33 A and 10 ns, respectively when the capacitor is pre-charged to 2 kV.

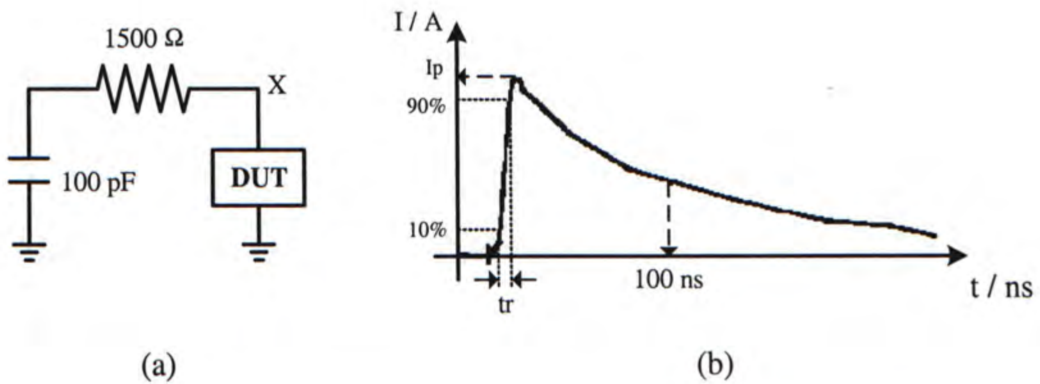


Figure 1.1: (a) The schematic of HBM and (b) the pulse waveform at X

The HBM ESD event is the most common scenario that is always considered in integrated circuit design. In practice, there are well-defined procedures for guiding the HBM ESD test, so that the maximum ESD level that the circuits can survive can be measured.

2) The Machine Model (MM) represents a charged machine body, which discharges accumulated static charge through a device to ground. It is defined by the ESD association standard *ANSI/ESD STM5.2* [3]. Since this model is composed of a resistor, inductor and a pre-charged capacitor, the ESD pulse generated by it is an underdamped oscillatory waveform. Figure 1.2 depicts the schematic and the waveform of the ESD current pulse produced from the MM ESD event.

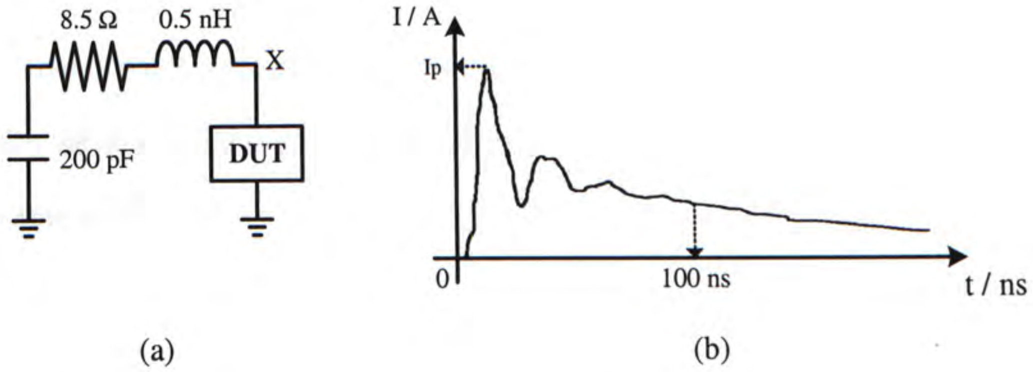


Figure 1.2: (a) The schematic of MM and (b) the pulse waveform at X

Typically, the peak current I_p and the rise time tr of the MM ESD pulse are 3.7 - 7 A and 15 - 30 ns, respectively when the capacitor is pre-charged to 400 V.

3) The Charged-Device Model (CDM) represents a device self-charging and then self-discharges directly to ground. It is defined by the ESD association standard *ANSI/ESD STM5.3.1* [4]. The modeling circuit and the corresponding ESD pulse produced from the CDM ESD event are shown in Figure 1.3.

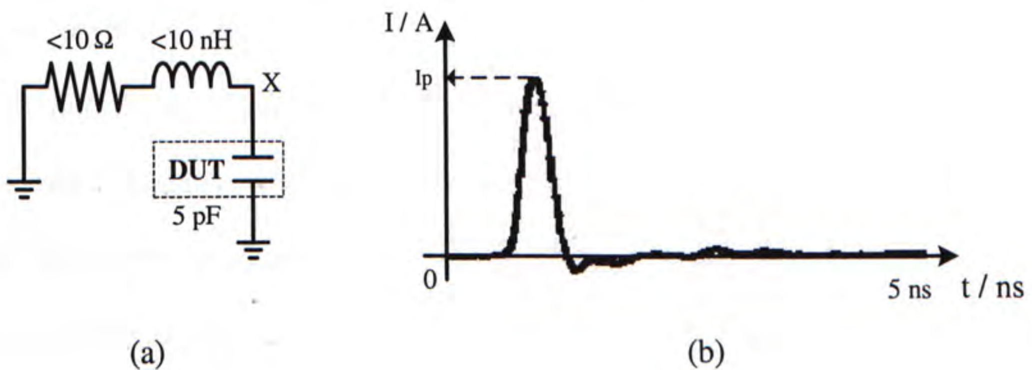


Figure 1.3: (a) The schematic of CDM and (b) the pulse waveform at X

Usually, the self-charging of an electronic device is due to field induction. In the case when DUT is charged to 1 kV by induced, the peak current I_p and the rise time tr of the resultant CDM ESD pulse are 10 A and 1 ns, respectively. This pulse is impulsive and disastrous that it is the hardest to protect against.

1.2 Electrostatic Discharge in CMOS RF Circuits

Traditional RF integrated circuit is dominated by GaAs and bipolar technologies. Due to the high speed and low noise properties, these technologies are widely used to implement RF front-end in wireless communication systems [5, 6]. As CMOS technology scales down to submicron process, it becomes possible to implement giga-hertz CMOS integrated circuits. It leads to an attractive solution of integrating a complete low cost receiver using CMOS [7, 8].

Unfortunately, the continuous down scaling in CMOS transistor makes the gate oxide layer becoming very thin. The thin oxide layer can be damaged easily by a high electrostatic field. Theoretically, the breakdown voltage of gate oxide layer (SiO_2) is 76 mV/Å. Therefore, the supply voltage should be reduced in order to avoid the gate oxide breakdown of the transistor. For example, TSMC 0.18-μm CMOS can only operate with a supply voltage of 1.5 V.

ESD damage is a serious concern in the semiconductor industry. It can degrade or destroy the electrical characteristics of a semiconductor device. In CMOS integrated circuit, ESD is a common source that causes the gate oxide breakdown. Usually, when human being touches the transistor gate terminal, the HBM ESD pulse discharged can lead to the gate oxide breakdown, which can damage the circuit forever.

In recent years, ESD protection has been a popular research topic in CMOS RF integrated circuits [9, 10, 11]. The objective is to provide a reliable single chip receiver solution for wireless communications. Figure 1.4 depicts an integrated RF CMOS front-end.

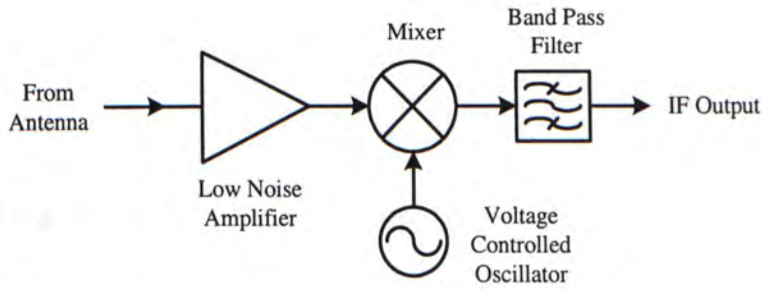


Figure 1.4: An RF front-end for wireless communications

To consider ESD protection of the whole RF integrated front-end, dual-diode circuits can be employed for taking care of all its DC and low frequency input and output terminals. A conventional dual-diode protection circuit is shown in Figure 1.5. This is a reliable ESD protection circuit for CMOS digital and mixed-signal circuits [12]. It is capable of removing the incoming ESD pulses, so that the integrated circuit can be protected.

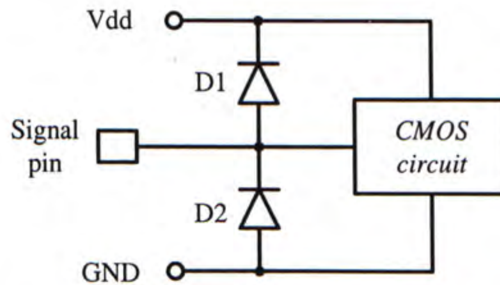


Figure 1.5: Dual-diode circuitry used in CMOS digital and mixed-signal circuits

However, the dual-diode ESD protection circuit is not suitable for RF applications, because of the large parasitic capacitances generated from the bulky protection diodes. At radio frequency, the shunt capacitances become a low impedance path that will short the RF input signal to ground. Consequently, the power gain and the noise figure of the LNA will be degraded [13, 14]. An ideal ESD protection circuit should be transparent to RF signal. Hence, most of the published CMOS RF receivers are operated without an ESD protection circuits. The yield and long-term

reliability of unprotected CMOS RF circuits are extremely low that prohibits single chip CMOS receiver from entering the commercial market.

1.3 Research Goal and Contribution

This research project is aimed to improve the ESD protection of CMOS RF LNA. The new design should not cause any degradation to LNA performance. It should operate at low supply voltage. Furthermore, it should be integrated in standard commercial CMOS process.

In this thesis, a new ESD protection method, called Common-Gate Input Stage Method (CGISM), is presented. This method uses a common-gate amplifier as an input stage for a LNA, so as to reduce the possibility of the gate oxide breakdown. In addition, the method does not degrade the performance of the new LNA. To demonstrate the feasibility of CGISM, a CGISM LNA is fabricated with a standard 0.35-μm CMOS technology. From the measurement results (Chapter 8), it shows that CGISM can improve the ESD immunity of the new LNA. Moreover, the new LNA can provide comparable performance as standard LNAs [15], even at low supply voltage of 1.5 V.

1.4 Thesis Outline

This thesis is divided into nine chapters. Chapter 2 defines the performance parameters of an RF amplifier. Chapter 3 reviews some ESD protection methodologies for LNA. The proposed CGISM will also be introduced. In Chapter 4, the theory and techniques used for the LNA design is explained. Chapter 5 derives the noise factor equations for LNA under two different noise analysis methods. The details of the proposed LNA design are described in Chapter 6.

Then, the considerations of the layout design are discussed in Chapter 7. The measurement results of two fabricated LNA circuits are reported in Chapter 8. Finally, Chapter 9 concludes this thesis and provides the recommendations for future work.

Chapter 2

Performance Parameters of Amplifier

In performance analysis of RF amplifiers, hardware functionality is described by a specification. The parameters included in the specification give a variety of information such as amplifier gain, noise, linearity, etc. According to these performance parameters, designers can justify whether the amplifier meets the application requirements or not [15, 16]. In this chapter, we will introduce some standard RF amplifier parameters.

2.1 Amplifier Gain

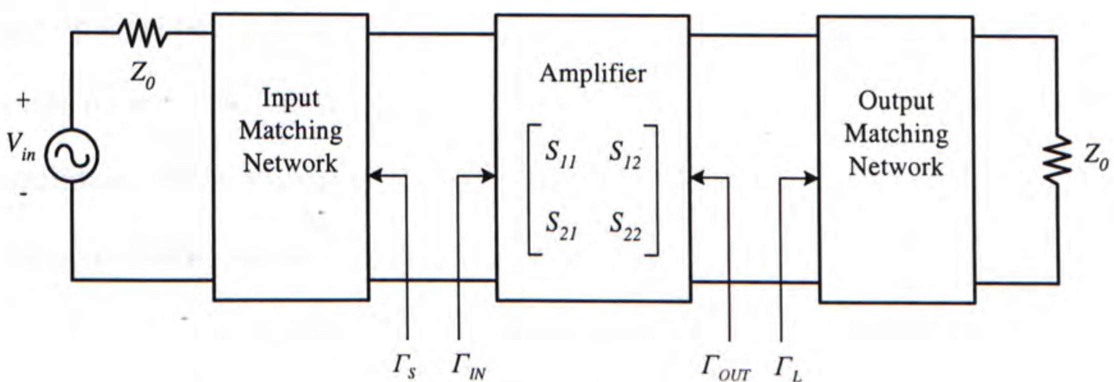


Figure 2.1: A microwave amplifier block diagram

Amplifier Gain refers to the ratio of the output power to the input power of an amplifier. It is one of the most important performance parameters for a microwave amplifier. In wireless communication, incoming signal to a receiver front-end is

always too weak to be processed. Therefore, amplifier is employed to increase the signal power level.

Figure 2.1 shows a typical microwave amplifier design diagram. In the design of an amplifier, there are three types of amplifier gains, including Transducer power gain G_T, Operating power gain G_P and Available power gain G_A. Their corresponding definitions are listed as follows [17]:

$$G_T = \frac{\text{Power delivered to the load}}{\text{Power available from the source}}$$
$$= \frac{1-|\Gamma_S|^2}{|1-\Gamma_{IN}\Gamma_S|^2}|S_{21}|^2\frac{1-|\Gamma_L|^2}{|1-S_{22}\Gamma_L|^2} = \frac{1-|\Gamma_S|^2}{|1-S_{11}\Gamma_S|^2}|S_{21}|^2\frac{1-|\Gamma_L|^2}{|1-\Gamma_{OUT}\Gamma_L|^2} \tag{2.1}$$

$$G_P = \frac{\text{Power delivered to the load}}{\text{Power input to the network}} = \frac{1}{1-|\Gamma_{IN}|^2}|S_{21}|^2\frac{1-|\Gamma_L|^2}{|1-S_{22}\Gamma_L|^2} \tag{2.2}$$

$$G_A = \frac{\text{Power available from the network}}{\text{Power available from the source}} = \frac{1-|\Gamma_S|^2}{|1-S_{11}\Gamma_S|^2}|S_{21}|^2\frac{1}{1-|\Gamma_{OUT}|^2} \tag{2.3}$$

Different definitions apply to the design of different amplifiers. For example, Equation (2.1) is used for high gain amplifier design. Equation (2.2) is used for power amplifier (PA) design. It is because the input of PA is assumed to be perfectly matched. In contrast, the output matching is assumed to be perfect in G_A definition, which is usually applied to LNA design. Nevertheless, all three gain variables will be identical for their maximum values, i.e.

$$G_{T,max} = G_{P,max} = G_{A,max} = G_{MAX} \tag{2.4}$$

2.2 Noise Factor

Noise Factor (NF) is a measure of the degradation in signal-to-noise ratio that an amplifier introduces. Noise figure is defined as noise factor in dB. To express

quantitatively this performance parameter, the following equation is defined.

$$NF = \frac{\text{Input } SNR}{\text{Output } SNR} = \frac{S_{in}/N_{in}}{S_{out}/N_{out}} \tag{2.5}$$

where S_{in} and S_{out} are the input and output signal power, respectively

N_{in} and N_{out} are the input and output noise power, respectively

Hence,

$$NF = \frac{S_{in}}{S_{out}} \frac{N_{out}}{N_{in}}$$

$$= \frac{N_{out}}{GN_{in}} \tag{2.6}$$

where G is the gain of the amplifier.

From the equation derived above, another definition of noise factor is obtained, which is:

$$NF = \frac{\text{Total output noise power}}{\text{Output noise power due to input source}} \tag{2.7}$$

The total output noise power is composed of the output noise power due to input source and circuit noise of the amplifier [18]. In transistor amplifier, the major contributions of the circuit noise are the active components such as transistor and diode. The passive components that contain a certain amount of parasitic resistance can also generate thermal noise.

Standard mobile communication requires a minimum value of noise factor for a receiver front-end, so as to provide a reasonable signal-to-noise ratio at the output. As most of the receiver front-ends use a cascaded architecture, Friis formula can be applied to calculate the overall noise factor. This formula is given by

$$NF = F_1 + \frac{F_2 - 1}{G_1} + \frac{F_3 - 1}{G_1 G_2} + \frac{F_4 - 1}{G_1 G_2 G_3} + \ldots \tag{2.8}$$

where F_i and G_i are the noise factor and the power gain of i-th stage, respectively. LNA is often placed in front of other RF modules in a receiver circuit. Thus, it requires high gain and low noise factor to keep the overall NF to a relatively low level.

2.3 Linearity

Linearity is an important issue in RF amplifier. Circuit designer will like the RF amplifier to be a linear system, i.e. $y(t) = \text{Gain} \cdot x(t)$. However, most RF transistor amplifiers are non-linear [19]. It means that when two sinusoidal signals are injected into the amplifier, the output signal not only contains these two fundamental frequencies, but also generates many additional harmonics and high-order frequency terms the output spectrum (see Figure 2.2).

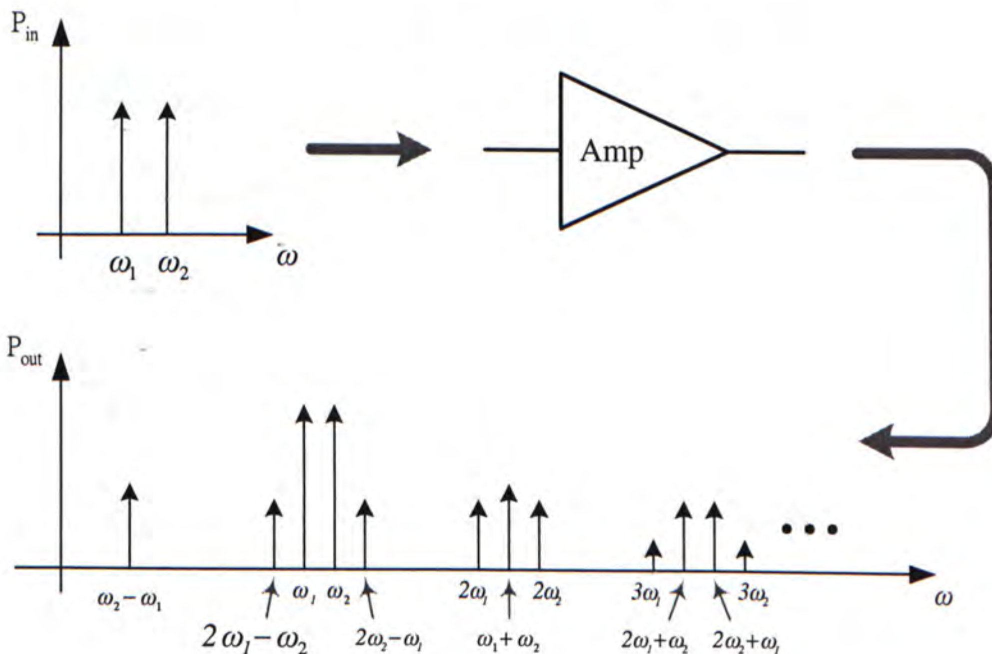


Figure 2.2: Non-linear effect of RF amplifier

In order to model the non-linear system mathematically, the following power series will be used.

$$y(t)=c_1\, x(t)+c_2\, x^2(t)+c_3\, x^3(t) \tag{2.9}$$

where c_1, c_2 and c_3 are constants with c_1 and c_3 are opposite in sign. By using this formula, the following derivation can help us to understand the non-linear phenomenon. Suppose a two-tone input signal is $x(t)=A\cos\omega_1 t+B\cos\omega_2 t$, then

$$
\begin{aligned}
y(t) &= c_1\left(A\cos\omega_1 t+B\cos\omega_2 t\right)+c_2\left(A\cos\omega_1 t+B\cos\omega_2 t\right)^2 \\
&\quad +c_3\left(A\cos\omega_1 t+B\cos\omega_2 t\right)^3 \\
&= c_1\left(A\cos\omega_1 t+B\cos\omega_2 t\right)+c_2\left(A^2\cos^2\omega_1 t+2AB\cos\omega_1 t\cos\omega_2 t\right. \\
&\quad \left.+B^2\cos^2\omega_2 t\right)+c_3\left(A^3\cos^3\omega_1 t+3A^2B\cos^2\omega_1 t\cos\omega_2 t\right. \\
&\quad \left.+3AB^2\cos\omega_1 t\cos^2\omega_2 t+B^3\cos^3\omega_2 t\right) \\
&= \frac{c_2\left(A^2+B^2\right)}{2}+\left(c_1A+\frac{3c_3A^3}{4}+\frac{3c_3AB^2}{2}\right)\cos\omega_1 t \\
&\quad +\left(c_1B+\frac{3c_3B^3}{4}+\frac{3c_3A^2B}{2}\right)\cos\omega_2 t \\
&\quad +c_2AB\left[\cos\left(\omega_1+\omega_2\right)t+\cos\left(\omega_2-\omega_1\right)t\right] \\
&\quad +\frac{c_2A^2}{2}\cos 2\omega_1 t+\frac{c_2B^2}{2}\cos 2\omega_2 t \\
&\quad +\frac{3c_3A^2B}{4}\cos\left(2\omega_1-\omega_2\right)t+\frac{3c_3AB^2}{4}\cos\left(2\omega_2-\omega_1\right)t \\
&\quad +\frac{3c_3A^2B}{4}\cos\left(2\omega_1+\omega_2\right)t+\frac{3c_3AB^2}{4}\cos\left(2\omega_2+\omega_1\right)t \\
&\quad +\frac{c_3A^3}{4}\cos 3\omega_1 t+\frac{c_3B^3}{4}\cos 3\omega_2 t
\end{aligned} \tag{2.10}
$$

Based on Equation (2.10), the output contains many high frequency harmonics, which included a DC term, fundamental, second and third-order intermodulation (IM) products of the input signals. Using Equation (2.10), the two linearity parameters, *1-dB compression point* and *third-order intercept point* are derived as follows [20].

2.3.1 1-dB Compression Point

When an input signal with low drive level is applied to a non-linear amplifier, its output power is directly proportional to its input power. However, as the power increases beyond a significant level, the contact gain relationship cannot keep linear and gain compression occurs. Eventually, the output power becomes saturated. The point at where the small-signal gain of the amplifier reduces from the expected linear gain by 1 dB is called 1-dB Compression Point. Figure 2.3 indicates the location of the 1-dB compression point in the graph of input-output power.

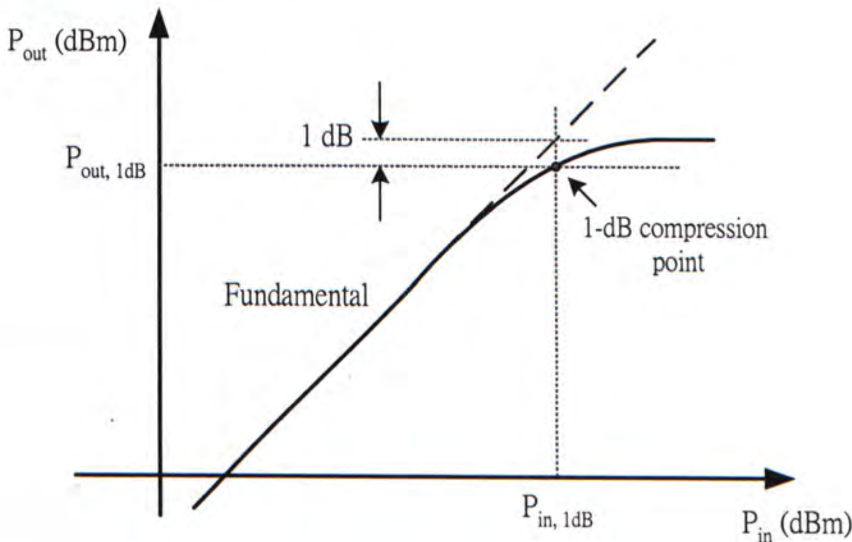


Figure 2.3: Determination of 1-dB compression point

From the mathematical point of view, when an input signal $x(t) = Acos\omega_0 t$ is injected into an amplifier, by modifying Equation (2.10), the output signal becomes

$$y(t) = \frac{c_2 A^2}{2} + \left(c_1 A + \frac{3 c_3 A^3}{4} \right) cos\omega_0 t + \frac{c_2 A^2}{2} cos\, 2\omega_0 t + \frac{c_3 A^3}{4} cos\, 3\omega_0 t \qquad (2.11)$$

We can observe from Equation (2.11) that the gain of the fundamental frequency is $\left(c_1 + 3 c_3 A^2/4 \right)$, instead of a constant. At small input amplitude A, $3c_3 A^2/4$ is

small compared to c_1 and can be neglected. So, the input-output power relationship remains linear. However, when A is large, $3c_3A^2/4$ becomes significant. Since c_1 and c_3 are opposite in sign, the gain decreases with A. The gain compression effect will become more series if the value of A becomes very larger. Finally, the gain will be equal to zero and the amplifier is said to reach the saturation region. Therefore, 1-dB compression point is a critical value used to characterize the power handling capabilities of an amplifier.

2.3.2 Third-Order Intercept Point

Another standard parameter employed to assess the linearity of an amplifier is Third-Order Intercept Point (IP3). When a two-tone signal, with the same power levels at slightly different frequencies (ω_1, ω_2), is applied to an amplifier, intermodulation distortion (IMD) appears at the output spectrum as shown in Figure 2.2. For the output frequency components that are far away from the fundamental frequencies, they can be removed by filtering. Unfortunately, there are two output IM products $(2\omega_1 - \omega_2)$ and $(2\omega_2 - \omega_1)$ caused by the third-order nonlinearities of the amplifier. They appear closely to the expected output frequencies and it is difficult to suppress them by simple filtering technique.

Equation (2.12) describes the content of the output signal $y(t)$ when the two-tone signal $x(t) = A(\cos\omega_1 t + \cos\omega_2 t)$ is applied to the amplifier.

$$
\begin{aligned}
y(t) = {} & c_2A^2 + \left(c_1A + \frac{9c_3A^3}{4}\right)(\cos\omega_1 t + \cos\omega_2 t) \\
& + c_2A^2\left[\cos(\omega_1+\omega_2)t + \cos(\omega_2-\omega_1)t\right] \\
& + \frac{c_2A^2}{2}(\cos 2\omega_1 t + \cos 2\omega_2 t) + \frac{3c_3A^3}{4}\left[\cos(2\omega_1-\omega_2)t + \cos(2\omega_2-\omega_1)t\right] \\
& + \frac{3c_3A^3}{4}\left[\cos(2\omega_1+\omega_2)t + \cos(2\omega_2+\omega_1)t\right] + \frac{c_3A^3}{4}(\cos 3\omega_1 t + \cos 3\omega_2 t)
\end{aligned}
\tag{2.12}
$$

Similar to the single-tone input, gain compression occurs and the small-signal gains of the fundamental frequencies are equal to $\left(c_1 + 9c_3A^2/4\right)$. So, the output powers are approximately proportional to the corresponding input powers at small amplitude A. For the third-order IM products, the output amplitudes are $3c_3A^3/4$. This means that the output powers are the cube of the input powers. Therefore, if the fundamental and the third-order IM product are plotted on the input power verse output power graph in log scale, the slope of the third-order IM product will be three times that of the fundamental in the linear region. This property is depicted in Figure 2.4.

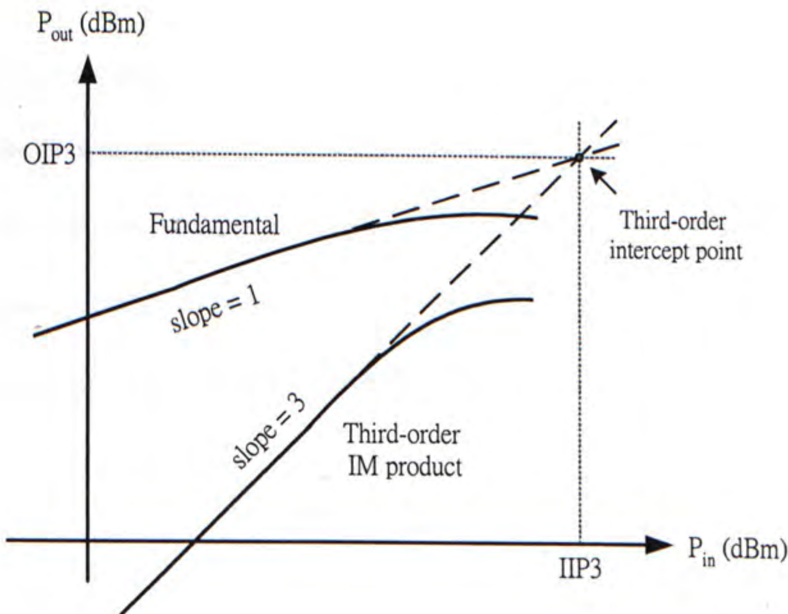


Figure 2.4: Determination of third-order intercept point

From Figure 2.4, IP3 is the point where the linear extension of the Third-order IM product curve intersects the linear extension of the Fundamental curve.

IP3 indicates how well an amplifier performs in the presence of strong nearby interference, because the gain of the fundamental component is dependent of interferer's amplitude. Also, the IMD performance determines the extent to which the generated interference corrupts the adjacent channels.

In a multistage amplifier, the total IIP3 power $P_{IIP3,tot}$ can be calculated by the following formula:

$$\frac{1}{P_{IIP3,tot}} = \frac{1}{P_{IIP3,1}} + \frac{G_1}{P_{IIP3,2}} + \frac{G_1 G_2}{P_{IIP3,3}} + \ldots \quad (2.13)$$

where $P_{IIP3,i}$ and G_i are the IIP3 power and the power gain of i-th stage, respectively. It implies that the linearity of a multistage amplifier is limited by the number of stages and their corresponding power gains.

2.4 Return Loss

Return Loss (RL) is a measure of the ratio of signal power transmitted into a system to the power reflected. This parameter indicates the amount of impedance mismatch between the source and the system. In fact, any variation in impedance from the source results in some returned power. Therefore, large RL means that there is less energy reflected and the impedance mismatch is less.

For the system impedance Z_A with the source impedance Z_0, RL is defined as:

$$RL(dB) = -20 \log_{10} |\Gamma_A| \quad (2.14)$$

where

$$\Gamma_A = \frac{Z_A - Z_0}{Z_A + Z_0} = \text{Reflection Coefficient} \tag{2.15}$$

When Z_A is equal to Z_0, Γ_A will be zero and RL becomes infinity. In this condition, the system is said to perfectly match the source. As a result, all the power transfers to the system and there is no power reflection.

Figure 2.5 demonstrates how the matching network helps to improve RL.

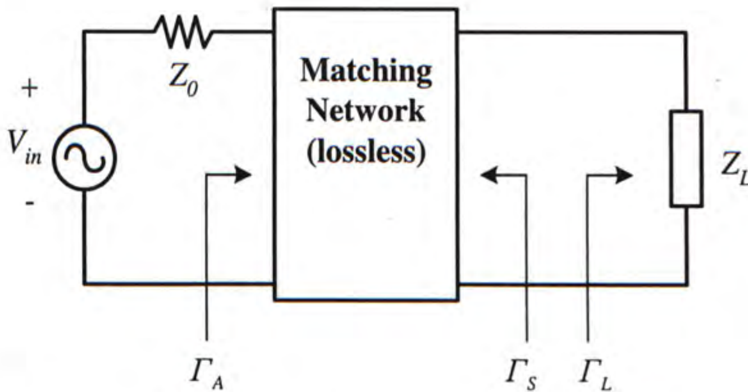


Figure 2.5: Impedance transformation by matching network

Since the impedance Z_L is connected to a lossless matching network, its reflection coefficient is transformed from Γ_L to Γ_A which is expressed as:

$$|\Gamma_A| = \left| \frac{\Gamma_L - \Gamma_S^*}{1 - \Gamma_L \Gamma_S} \right| \tag{2.16}$$

On the other hand, the matching network transforms the source impedance to Z_S with the reflection coefficient of Γ_S. By tuning the matching network in such a way that Γ_S is equal to Γ_L^*, $|\Gamma_A|$ will be zero and RL seen from the source impedance becomes infinity. This technique is called conjugate matching.

In microwave amplifier design, the matching networks are usually constructed at both input and output terminals for impedance transformation (see Figure 2.1).

Thus, there are two parameters for measuring how well the matching networks transform both input and output impedances to Z_0, they are:

$$Input\ RL(dB) = -20\log_{10}\left|\frac{\Gamma_{IN} - \Gamma_S^*}{1 - \Gamma_{IN}\Gamma_S}\right| \quad (2.17)$$

and

$$Output\ RL(dB) = -20\log_{10}\left|\frac{\Gamma_{OUT} - \Gamma_L^*}{1 - \Gamma_{OUT}\Gamma_L}\right| \quad (2.18)$$

respectively. The minimum acceptable value is 15 dB. In some applications, a passive filter is required to precede a LNA, so it is necessary for the LNA to present a high RL at the input terminal, because the filter transfer characteristic is very sensitive to the mismatch of the termination impedance.

2.5 Power Consumption

During the operation of an RF circuit, a current $i_{dd}(t)$ is drawn from the battery of V_{DD} and there is some power dissipated. The amount of power consumed is calculated by:

$$P_{av} = V_{DD}\, I_{\mathrm{av}} \quad (2.19)$$

where

$$I_{av} = \frac{1}{T}\int_T i_{dd}(t)\,\partial t \quad (2.20)$$

In an RF amplifier circuit, $i_{dd}(t)$ is composed of AC and DC signals, i.e. $i_{dd}(t) = i_{ac}(t) + i_{dc}$. From Equation (2.20), I_{av} will be equal to i_{dc} and Equation (2.19) is simplified as:

$$P_{av} = V_{DD}\, i_{dc} \tag{2.21}$$

Most of the current portable mobile communication devices have the feature of long battery lifetime. In circuit design aspect, power consumption becomes a challenge issue. To attain this feature, designer can [21]:

1. use low V_{DD} to reduce the low power consumption and battery size;
2. design the circuit with low i_{dc}.

However, these methods will affect the performance of an amplifier, such as lower power gain, higher noise figure, poorer linearity and so on. There is always a trade-off between power consumption and performance.

2.6 HBM ESD Withstand Voltage

In the design of an ESD-protected LNA, HBM ESD Withstand Voltage is a well-known parameter to indicate the ESD protection capability. According to ESD Association standard test method for HBM component level [2], HBM ESD withstand voltage is defined as the maximum ESD level that does not cause component failure. The component can be a resistor, diode, transistor, integrated circuit or hybrid. When component failure occurs, the component under test does not meet one or more specified data sheet parameters, including:

- static parameters - input leakage current, input breakdown voltage, output drive current and supply current;
- dynamic parameters - full functionality, output rise and fall times under a specified load condition and dynamic current drawn.

In this condition, the component is said to be permanently destroyed and never functions again.

HBM ESD withstand voltage is measured in term of a pair of experimental data, one comes form the positive ESD voltage stress, another comes form the testing for negative ESD voltage stress. Based on the HBM ESD withstand voltage, ESD sensitive components are classified, regardless of polarity. Table 2.1 shows the HBM ESD sensitive (ESDS) component classification levels under ESD Association standard.

Class	Voltage Range (V)
0	< 250
1A	250 to < 500
1B	500 to < 1000
1C	1000 to < 2000
2	2000 to < 4000
3A	4000 to < 8000
3B	≥ 8000

Table 2.1: HBM ESDS component classification

In IC industry, most manufacturers specify the highest HBM ESD voltage level that a device can withstand. Use another word, the device must undergo testing with the HBM discharge waveform under the ESD Association standard requirements.

Chapter 3

ESD Protection Methodology for Low Noise Amplifier

ESD protection circuit is required to protect the input gate oxide of CMOS integrated circuits. In this chapter, two well-known ESD protection methods realized in the LNA are reviewed. They are dual-diode circuitry and shunt-inductor method. At the beginning, their working principles and major limitations associated with each method are discussed. After that, we will present a new ESD protection method for LNA that uses a common-gate amplifier as an input stage. The basic concept of this novel ESD protecting mechanism will be introduced at the end of this chapter.

Ideally, ESD protection circuitry designed for CMOS RF LNA should have the following features:

1. It should provide an effective path for removing all ESD current without damaging the core circuit;
2. It should be long-lasting and not be destroyed during a normal ESD protection process;
3. It should be transparent to RF signal and does not affect the LNA performance.

3.1 Dual-Diode Circuitry

Dual-diode circuitry is the most common ESD protection circuit that is used in CMOS digital and mixed-signal circuits [12]. As CMOS technology scales down to submicron process, the implementation of CMOS RF integrated circuits becomes possible. The dual-diode circuitry is adopted to CMOS RF LNA for ESD protection [10].

3.1.1 Working Principle

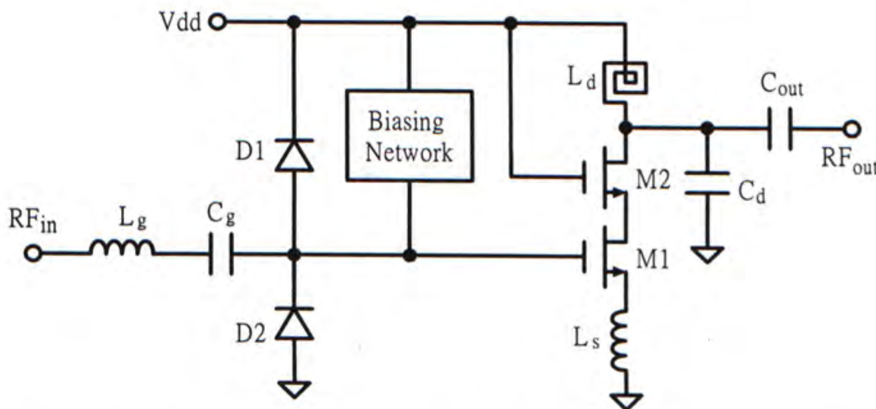


Figure 3.1: LNA with dual-diode ESD protection circuitry

The dual-diode circuitry consists of two diodes (D1 and D2) connected in reverse bias. One of them is connected from RF input of LNA to the power supply V_{dd}, another is connected from ground to the RF input, as illustrated in Figure 3.1. Since these diodes are reversely biased under normal operation, they behave like an open circuit that will not affect the performance of the LNA. However, when a hazardous static voltage is applied to the input terminal, one of the two diodes will turn on and short the input to ground. Thus, the CMOS circuits are protected from the ESD current. The detailed operation of the protection circuit is described in the following section.

When there is a positive ESD pulse at the RF input port, the potential of RF_{in} increases. As the voltage across D1 reaches its threshold V_{th}, it will turn on as illustrated in Figure 3.2(a). As a result, the gate potential is clamped to a safe level. In contrast, when there is a negative ESD pulse at the RF input port, the potential of RF_{in} decreases. In this case, D2 turns on as the voltage across D2 reaches its threshold V_{th}. The ESD current passes through D2 in the direction as illustrated in Figure 3.2(b). Similarly, the gate potential is also clamped to a safe level.

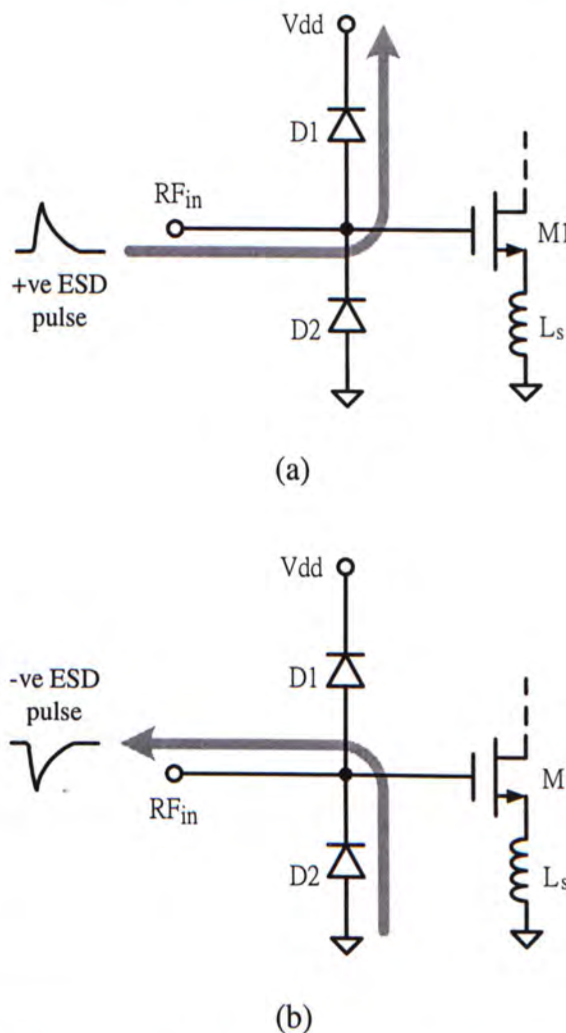


Figure 3.2: ESD current flow in dual-diode circuitry in the case of (a) positive ESD pulse; (b) negative ESD pulse

In both cases, the gate potential is clamped to either $V_{dd}+V_{th}$ or $-V_{th}$ to protect the gate oxide of M1 from breakdown. In particular, the ESD protection capability of the dual-diode circuitry is related to the sizes of the two diodes. The amount of ESD current that can be bypassed to ground is proportional to the diode size. That is why most of the ESD protection diodes occupy thousands of square micron of area.

3.1.2 Drawbacks

Although the dual-diode protection circuit works well with low frequency CMOS circuits, we are facing the following problems when it is applied to RF CMOS:

1. The clamping diodes are the bulky devices in CMOS process. They generate large shunt parasitic capacitances at the LNA input port. At radio frequency, the shunt capacitances become a low impedance path that will short the input RF signal to ground. Consequently, the power gain and the noise figure of the LNA will be degraded [13, 14]. Even though numerous researches have proposed modified circuitries to reduce the degradation, however, none of these methods have been proved feasible [22, 23].
2. In standard protection circuit, there is a series resistor of few hundred ohms between the dual-diode circuit and the LNA input. This resistor provides additional time delay to the ESD pulse, which serves as a secondary protection circuit. However, this small resistor will cause performance degradation to the RF circuit. Therefore, it must be omitted that will reduce the protection efficiency of the dual-diode circuit.

3.2 Shunt-Inductor Method

Shunt-inductor method is a modified ESD protection technique [11]. Figure 3.3 demonstrates a CMOS LNA using this protection method. Basically, this method uses the shunt inductor L_{ESD} at the RF input to provide a low impedance path to the high frequency ESD current. At the same time, it can tune out all the parasitic capacitance C_p that comes from the input bonding pad and normal ESD protection network. As a result, the LNA performance is improved. Practically, L_{ESD} should be realized by the on-chip inductor so as to provide a stand-alone chip protection.

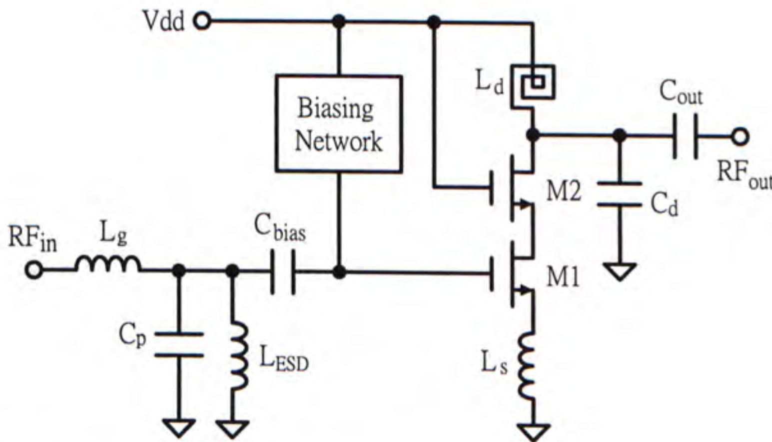


Figure 3.3: LNA with shunt inductor as ESD protection

3.2.1 Working Principle

This method makes use of the natural property of ESD current pulse to design an inductor-based protection circuitry. Under normal condition, the frequency of most ESD pulses is much lower than the RF input signal. Thus, L_{ESD} acts as a low pass filter and provides a low impedance path at the ESD frequency. In contrast, since the blocking capacitor C_{bias} is selected under the consideration of RF signal

frequency, its value is usually in the order of 0.1 pF. Hence, it behaves as a high pass filter and impedes the ESD current from entering the transistor M1. The incoming ESD current is forced to pass through L_{ESD} to ground, instead of passing through C_{bias}. Consequently, the entire ESD current is removed by L_{ESD} and M1 is protected.

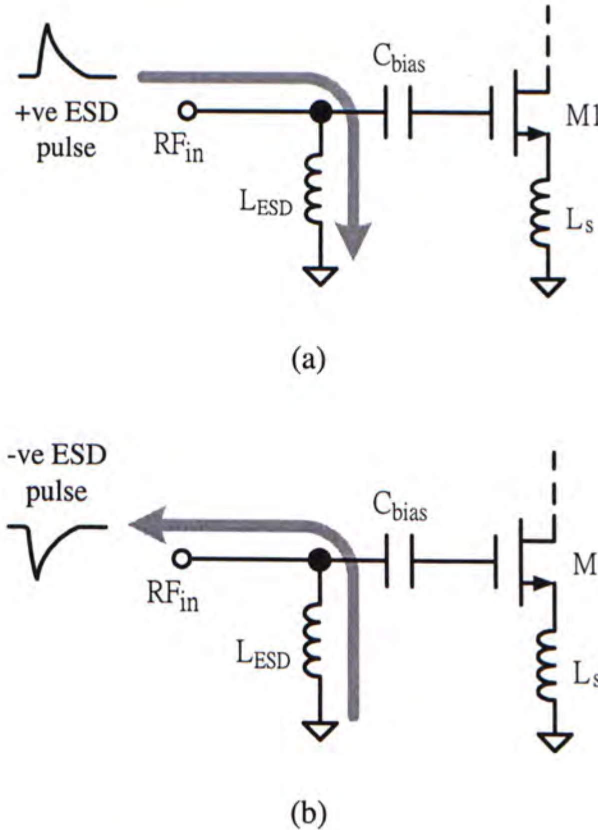


Figure 3.4: ESD current flow in shunt-inductor circuitry in the case of (a) positive ESD pulse; (b) negative ESD pulse

Figure 3.4(a) and (b) illustrates the protecting mechanism of the shunt-inductor method for positive and negative ESD pulses, respectively.

3.2.2 Drawbacks

General speaking, shunt-inductor method has the following problems:

1. The on-chip inductor realized in CMOS integrated circuit is a low-Q passive component. This inevitably leads to some power loss and performance degradation.
2. Since the shunt inductor connects directly to ground, any DC biasing voltage at the input terminal will be shorted to ground. To prevent this problem, blocking capacitors should be added at both sides that makes the input matching network bulky and introduces high power loss.
3. The ESD protection capability of this method is dependent on the metal width of the shunt inductor L_{ESD}. Wider metal track can handle higher ESD current and improves the ESD withstand voltage. However, the inductance of L_{ESD} is pre-defined by the matching network, thus, the designers have very little control to the width of the metal tracks.

3.3 Common-Gate Input Stage Method

In this project, a new ESD protection method has been developed which is called Common-Gate Input Stage Method (CGISM). This proposed method eliminates all the drawbacks listed in the preceding methods. Besides, there is no any additional ESD protection circuitry required. It is because the circuit used to implement CGISM is a single-stage LNA. Figure 3.5 shows a typical common-gate amplifier that is used to achieve the project goal.

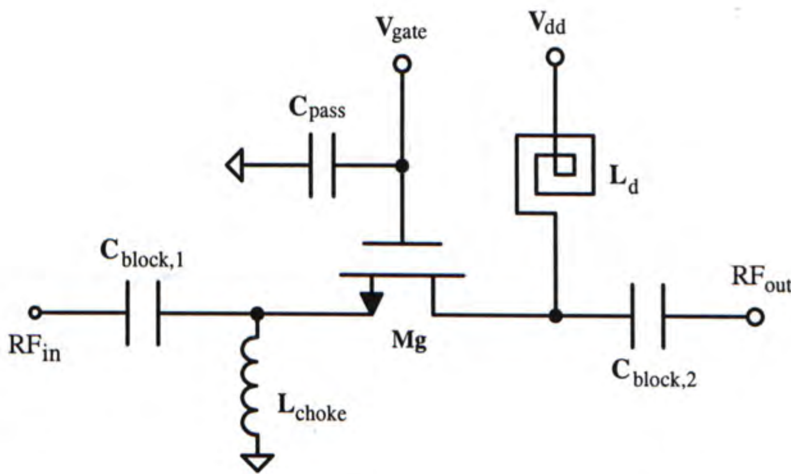


Figure 3.5: Schematic diagram of a common-gate amplifier

The major advantage of the common-gate amplifier is that its RF input is connected to the source terminal of the transistor Mg. For conventional LNA, its RF input is connected to NMOS gate terminal. Any ESD current can attack its gate oxide layer easily. Thus, its ESD immunity is quite low. However, by using CGISM, it greatly improves the ESD immunity of the LNA by preventing the hazardous ESD current from discharging through the thin gate oxide of Mg. Moreover, there is a built-in ESD protecting mechanism that can effectively take off all the ESD current at the RF input. In the following section, this built-in mechanism is introduced.

3.3.1 Built-In ESD Protecting Mechanism

A normal NMOS transistor has two diodes (D1 and D2) at its drain-substrate and source-substrate junctions as illustrated in Figure 3.6.

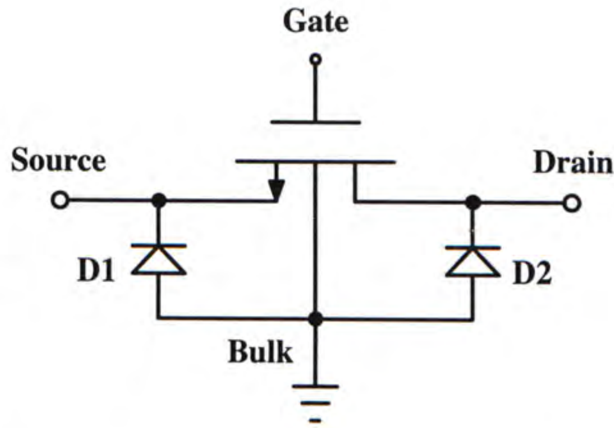


Figure 3.6: Simplified circuit model of a NMOS transistor

When there is a positive ESD pulse at the source terminal of a common-gate amplifier, the transistor Mg turns off initially because both its gate-to-source voltage V_{gs} and gate-to-drain voltage V_{gd} are negative. In this case, D1 is reversely biased and a space-charge layer is formed at the source-substrate junction. However, as the source terminal is forced to a high ESD potential, D1 will reach the breakdown potential. Near the breakdown potential, D1's space-charge layer generates a large amount of electron-hole pairs. The free electrons drift to the source region while the free holes drift to the substrate, which increases the substrate's potential with respect to the drain junction. Eventually, D2 switches on by the increasing substrate potential and all the ESD current passes through the transistor substrate from source-to- substrate -to-drain.

On the other hand, when a negative ESD pulse is applied to the input port, the transistor Mg and the diode D1 turn on because of the positive V_{gs}. Therefore, all the ESD current flows through the channel from drain-to-channel-to-source and from

substrate-to-source. Figure 3.7 shows the scenarios of how the hazardous ESD can be removed by a common-gate amplifier.

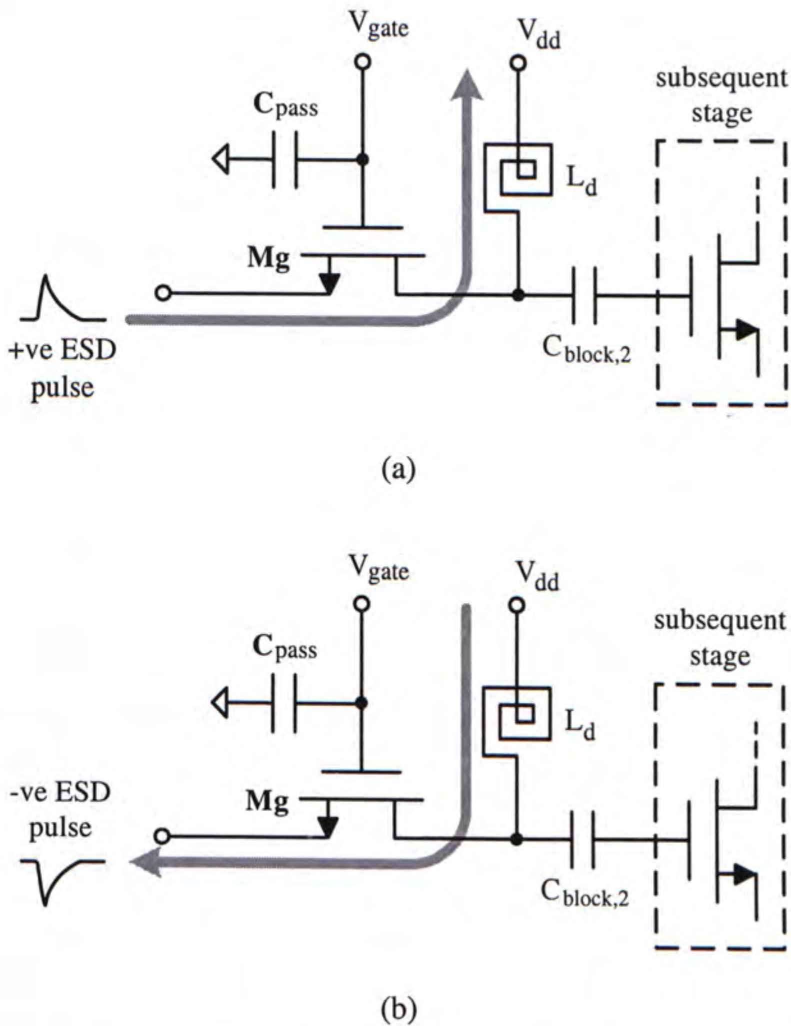


Figure 3.7: Built-in ESD protecting mechanism of CGISM

In summary, common-gate LNA can provide higher ESD immunity than conventional common-source LNA because of the built-in ESD protecting mechanism.

For an ESD pulse with a fast rise time, its high frequency components may leak off to the successive stage through the output capacitor $C_{block,2}$. To tackle this problem, an on-chip spiral inductor L_d is placed before $C_{block,2}$ as illustrated in Figure 3.5. Its working principle is similar to how the shunt-inductor method does.

Under normal condition, the ESD frequency is lower than the RF input signal. L_d and $C_{block,2}$ form a high pass filter to force the ESD signal to V_{dd} through L_d. Furthermore, there is no ESD signal coupling to the gate of the transistor Mg through the gate-to-source capacitor C_{gs}. It is because the capacitance of C_{gs} is in the order of 0.1 pF that it gives high impedance at the ESD frequency. Therefore, the LNA is completely saved against all ESD.

3.3.2 Competitiveness

By comparing with the preceding ESD protection methods, CGISM has many competitive factors that can enhance the ESD immunity of CMOS RF LNA to protect CMOS RF receiver chip.

1. The method is simple, there is no additional clamping device required to install at the LNA input. Thus, it does not increase the production cost.
2. There is no any bulky parasitic capacitance associated at the RF input. The performance is not degraded.
3. Besides the ESD protection functionality, the common-gate input stage can provide a certain amount of power gain. The amplification requirement of the subsequent-stage amplifier can be reduced. It benefits the low voltage design.
4. The ESD handling capability is proportional to the size of the transistor Mg. Larger width can support higher channel current. More ESD current can be handled as a result.
5. Mg controls the amount of current passing through its channel. The shunt inductor and the blocking capacitor form a high pass filter to prevent the ESD current from leaking off to the subsequent transistor.

Chapter 4

Design Theory of Low Noise Amplifier

Low noise amplifier (LNA) is the first stage in the receiving path of a receiver. Typically, its function is to provide enough gain to overcome the noise of subsequent stages. According to Friis formula of Equation (2.8), its noise figure directly adds to that of the receiver. Thus, the LNA should generate as little noise as possible.

Aside from the noise consideration, linearity is another parameter that should be concerned. At normal power range, the LNA should amplify the incoming signal without any distortion. On the other aspect, the LNA needs to present a well-defined input impedance, such as 50 Ω. It is due to the transfer characteristic of the antenna preceding the LNA that is very sensitive to the LNA termination.

In this chapter, we will present some basic LNA design techniques. These include the methods of input termination, gain enhancement and improvement of reverse isolation. By mastering these techniques, a variety of LNA designs can be developed to meet the system specifications.

4.1 Small-Signal Modeling

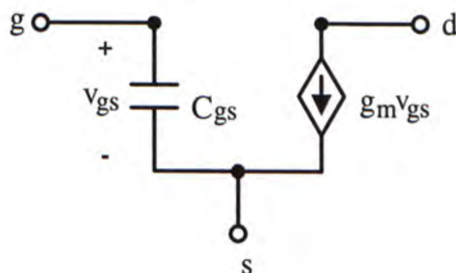


Figure 4.1: Small-signal model of a MOS transistor

For the purpose of small-signal analysis, active devices are usually modeled with a number of lumped elements, including RLC passive elements, dependent and independent sources, which give the necessary approximation in frequency domain. Figure 4.1 gives the simplified small-signal model of a MOS transistor, where g_m is the transistor transconductance.

4.2 Method of Input Termination

Presentation of a good match to the external world is a critical requirement in RF design. Since the input impedance of MOS transistor is inherently capacitive, providing a 50-Ω input impedance without degrading noise performance is always a challenging topic. Fortunately, there are four common circuit topologies that are able to accomplish this goal [24]. In the section, the fundamentals of these four topologies are reviewed.

4.2.1 Resistive Termination

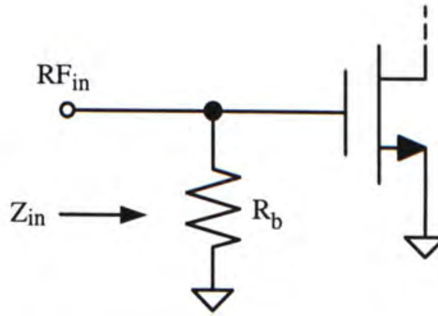


Figure 4.2: Input impedance matching by resistive termination

Resistive termination is a straightforward approach to present a broadband 50-Ω impedance at an amplifier input. Simply speaking, when a 50-Ω shunt resistor R_b is connected across the input terminal, the stable input impedance can be realized. Figure 4.2 illustrates this technique applied to a common-source amplifier.

However, the resistor R_b not only adds thermal noise to the amplifier, but also leads to high power loss at the input. The amplifier performance will be greatly degraded if this topology is implemented at high frequency. Therefore, this topology is not recommended for RF LNA design.

4.2.2 Shunt-Series Feedback

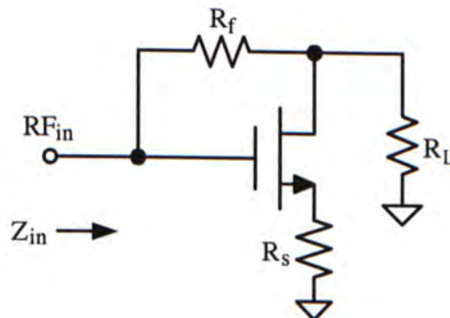


Figure 4.3: Input impedance matching by shunt-series feedback

Figure 4.3 shows the schematic of a shunt-series amplifier that employs the

feedback technique to provide a broadband real input impedance. Since there is no any shunt resistor that attenuates the input signal, its noise figure is expected to be better than the previous approach. Nevertheless, the resistor R_f still contributes some thermal noise to the amplifier. The resistive feedback network also limits the gain of the amplifier. Therefore, this topology is not recommended to implement in RF LNA.

4.2.3 $1/g_m$ Termination

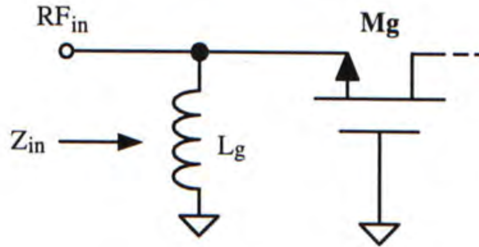


Figure 4.4: Input impedance matching by $1/g_m$ termination

The third method used to realize a stable 50-Ω input impedance is $1/g_m$ termination. Its working principle is to use a common-gate topology to achieve this goal. Figure 4.4 demonstrates the implementation of this method. The shunt inductor L_g is tuned to resonate with the capacitor C_{gs} at the operating frequency.

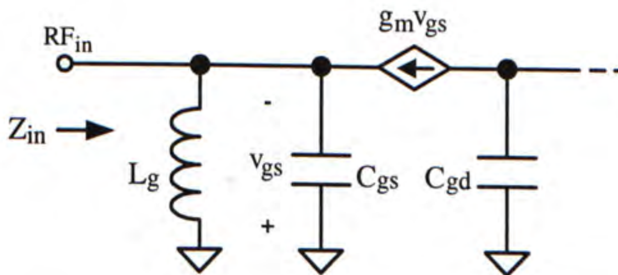


Figure 4.5: Small-signal analysis of a common-gate topology

From the small-signal circuit shown in Figure 4.5,

$$\frac{1}{Z_{in}} = \frac{1}{j\omega L_g} + j\omega C_{gs} + \frac{g_m v_{gs}}{v_{gs}}$$
$$= \frac{1-\omega^2 L_g C_{gs}}{j\omega L_g} + g_m \quad (4.1)$$

At resonance, $\omega_0^2 L_g C_{gs} = 1$, then

$$Z_{in}(\omega_0) = \frac{1}{g_m} \quad (4.2)$$

where ω_0 is the operating frequency. By a proper selection of the transistor size and bias current, the desired 50-Ω input impedance appears at ω_0.

Different from the preceding approaches that rely on the resistor, $1/g_m$ termination provides the desired input impedance with acceptable noise performance. Therefore, it becomes one of the most common methods in LNA implementation [25, 26].

4.2.4 Inductive Source Degeneration

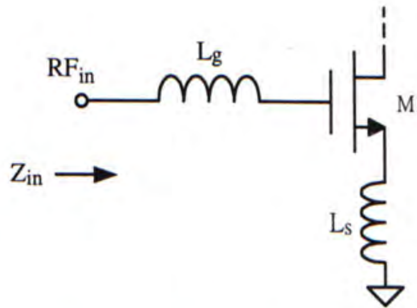


Figure 4.6: Input impedance matching by inductive source degeneration

Another popular method employed used to design standard input impedance is called Inductive Source Degeneration [27]. Figure 4.6 illustrates a common-source amplifier with this method. Actually, the advantage of this method is that the

resistive part of the input impedance is generated by the source inductor L_s, instead of using noisy resistor. Theoretically, inductor does not introduce any thermal noise, which satisfies the noise requirement of LNA. Figure 4.7 shows the small-signal model of an inductively source degenerated amplifier.

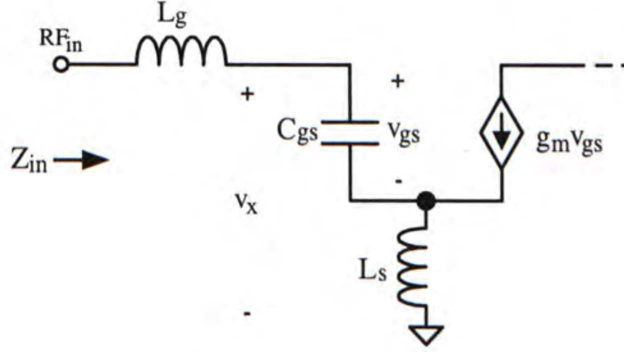


Figure 4.7: Small-signal analysis of inductively source degenerated amplifier

From the figure,
$$v_x = v_{gs} + j\omega L_s \left(j\omega C_{gs} v_{gs} + g_m v_{gs} \right)$$
$$= \left(1 - \omega^2 L_s C_{gs} + j\omega g_m L_s \right) v_{gs} \tag{4.3}$$

$$Z_{in} = j\omega L_g + \frac{\left(1 - \omega^2 L_s C_{gs} + j\omega g_m L_s\right) v_{gs}}{j\omega C_{gs} v_{gs}}$$
$$= j\omega \left(L_g + L_s \right) + \frac{1}{j\omega C_{gs}} + \frac{g_m L_s}{C_{gs}}$$
$$= \frac{1 - \omega^2 \left(L_g + L_s \right) C_{gs}}{j\omega C_{gs}} + \frac{g_m L_s}{C_{gs}} \tag{4.4}$$

At resonance, $\omega_0{}^2 \left(L_g + L_s \right) C_{gs} = 1$, then

$$Z_{in}(\omega_0) = \frac{g_m L_s}{C_{gs}} \tag{4.5}$$

Therefore, by choosing the suitable values of L_s, L_g, the transistor size and bias current, the input impedance can be adjusted to 50 Ω.

4.3 Method of Gain Enhancement

Amplifier gain is an important parameter in CMOS LNA specifications. High gain LNA provides sufficient amplification to the incoming signal. Moreover, it overcomes the noise of the subsequent stages, such as mixer. As a result, the overall noise figure of the receiver front-end can be reduced. Conventionally, tuned amplifier and multistage amplifier are usually implemented in CMOS LNA to enhance its amplifier gain. These methods are described in this section.

4.3.1 Tuned Amplifier

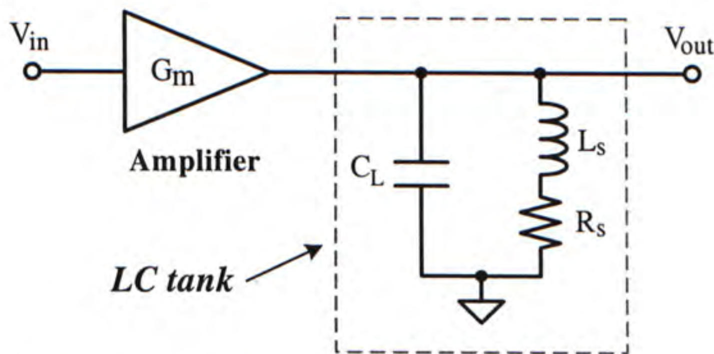


Figure 4.8: Tuned amplifier with LC tank circuit

Tuned amplifier is an amplifier that uses a LC resonant tank to accomplish high-gain performance [28]. At the resonance frequency, the LC tank becomes a high impedance load that will enhance the amplifier gain. From Figure 4.8, the gain of the tuned amplifier at a given frequency ω is given by

$$Gain = \frac{V_{out}(\omega)}{V_{in}(\omega)} = G_m \, Z_L(\omega) \tag{4.6}$$

where G_m, $Z_L(\omega)$ are the amplifier transconductance and the loading impedance of the LC tank at ω, respectively. In order to understand the resonant effect of the LC tank on the gain, considering the transformation diagram in Figure 4.9, where

R_s is the parasitic resistance of the inductor L_S.

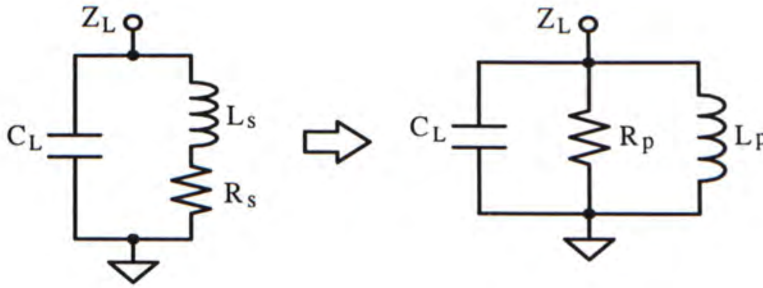


Figure 4.9: Transformation of LC tank

At a certain frequency ω, the LC tank circuit can be converted into a RLC parallel circuit. Mathematically, the necessary variables for the transformation are expressed as

$$R_p = R_s\left(1+Q^2\right),\ L_p = L_s\left(1+Q^{-2}\right) \tag{4.7}$$

where $Q = \dfrac{\omega L_s}{R_s}$ (4.8)

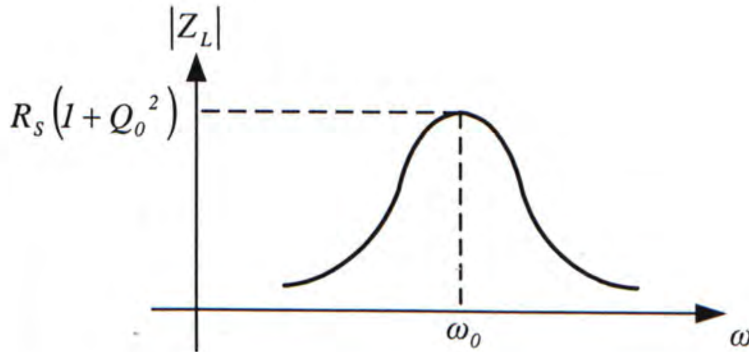


Figure 4.10: Frequency response of the LC tank impedance

Figure 4.10 shows the function of $|Z_L|$ against ω. It can be observed that Z_L reaches its maximum magnitude at the resonant frequency ω_0, which is

$$\omega_0 = \frac{1}{\sqrt{L_p C_L}} \tag{4.9}$$

As a result, the amplifier gain is maximum at ω_0, the corresponding value is

$$\frac{V_{out}(\omega_0)}{V_{in}(\omega_0)} = G_m R_p(\omega_0) = G_m R_s\left(1+Q_0^{\ 2}\right) \quad (4.10)$$

where $Q_0 = \dfrac{\omega_0 L_s}{R_s}$ (4.11)

As Q_0 increases, the parallel resistance $R_p(\omega_0)$ increases. Thus, the gain of the tuned amplifier increases at ω_0 and its bandwidth decreases. Ideally, if R_s is equal to zero, Q_0 will be infinite and the gain will be infinite too. Nevertheless, it is impossible to realize an inductor without any parasitic resistance. Therefore, the gain of a tuned amplifier is dependent on the CMOS technology.

4.3.2 Multistage Amplifier

In CMOS LNA design, it is a common that a single-stage LNA cannot provide sufficient gain, especially for low voltage design. In practice, cascading a number of stages to form a multistage amplifier becomes a feasible solution. Figure 4.11 illustrates the configuration of a multistage amplifier.

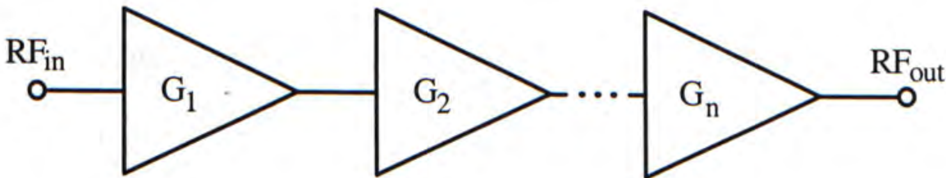


Figure 4.11: Multistage amplifier using cascading technique

The total power gain G_{total} of the multistage amplifier is determined by

$$G_{total} = G_1 G_2 \cdots G_n \quad (4.12)$$

where n is the total number of stages used.

In order to get the maximum value of G_{total}, it is necessary to present a suitable impedance match between each stage. It means that the output impedance of each single-stage amplifier should match with the input impedance of the next stage amplifier. Therefore, signal power reflection at each connection can reduced.

Since both the power consumption and the noise figure of a multistage amplifier increase with n. The value of n should not be greater than 3 so as to achieve high gain with acceptable noise figure.

4.4 Improvement of Reverse Isolation

Reverse isolation is another concern in LNA. In wireless receiver system, LO leakage from mixer to LNA often occurs. If the reverse isolation of the LNA cannot meet a certain level of attenuation, the excess LO signal from the LNA input will radiate through the antenna.

For the LNA itself, it is difficult to realize both input and output matching network for simultaneous conjugate match if the reverse isolation is poor. It is because both of the matching networks are highly dependent on each other. In addition, good reverse isolation can make the amplifier more stable. In this section, some basic techniques for improving the reverse isolation are reviewed.

4.4.1 Common-Gate Amplifier

Theoretically, poor reverse isolation of an amplifier is due to the presence of a capacitive path between input and output ports. If this feedback path is absent, the reverse isolation of the amplifier can be improved substantially. Common-gate amplifier provides better reverse isolation than common-source amplifier because of this reason [25, 29].

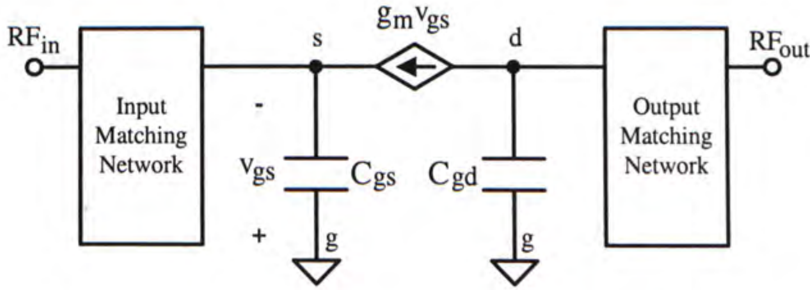


Figure 4.12: Small-signal model of a common-gate LNA

Figure 4.12 shows the small-signal model of a common-gate LNA. As the gate terminal is shorted to ground, both C_{gs} and C_{gd} become shunt capacitors. There is no significant capacitance between input and output terminals. Therefore, high reverse isolation is achieved in this configuration.

4.4.2 Cascoded Amplifier

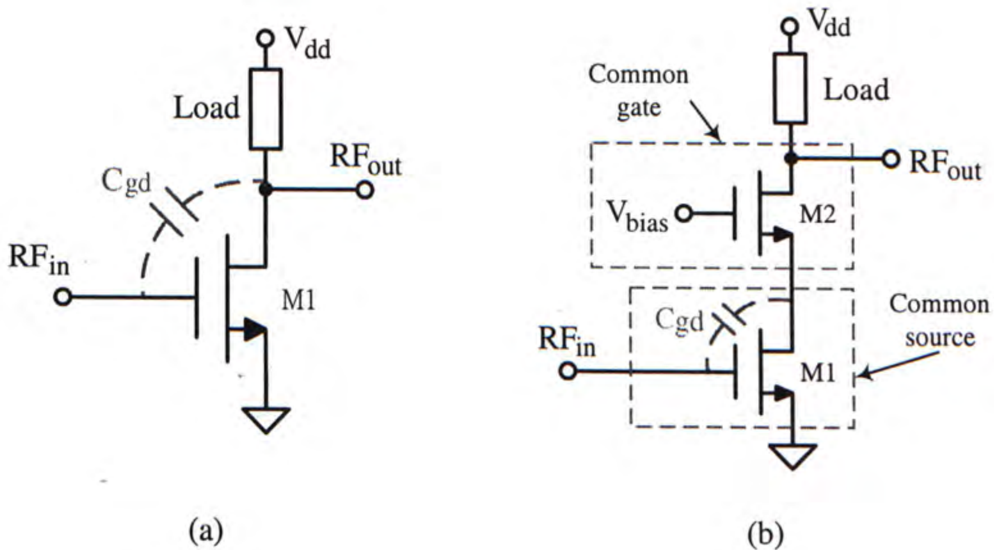


Figure 4.13: Common-source LNA (a) without cascoding transistor, (b) with the cascoding transistor M2

Traditionally, common-source LNA always associates with the poor reverse isolation. Although it can offer good performance in both power gain and noise

figure, the presence of the gate-to-drain capacitor C_{gd} makes the reverse isolation very poor. This capacitor is called Miller capacitor which is shown in Figure 4.13(a).

To solve this problem and improve the common-source configuration, the cascoding transistor M2 is added above the transistor M1 as shown in Figure 4.13(b). M2 acts as a common-gate amplifier to isolate the Miller capacitor C_{gd} from the output port. Without the feedback network, the reverse isolation of the modified common-source LNA is enhanced. To make the circuit simple and keep M2 in saturation region, V_{bias} is usually set to V_{dd}. However, the additional transistor M2 will contribute extra noise to the circuit, thus, cascoded LNA provides better reverse isolation at the cause of poorer noise figure.

Chapter 5

Noise Analysis of Low Noise Amplifier

There are two popular techniques for noise analysis of LNA, *noisy two-port analysis* and *small-signal noise analysis*. These two techniques analyze noise factor from different approaches. In this chapter, the origin of MOS transistor noise is described first, and two noise analysis approaches are introduced.

5.1 Noise Sources of MOS Transistor

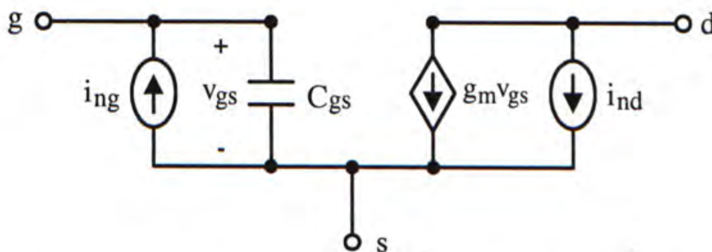


Figure 5.1: Noise model of MOS transistor

Figure 5.1 illustrates a simplified noise model of a MOS transistor where i_{nd} and i_{ng} represent drain noise current and gate noise current, respectively [30]. In MOSFET, the drain noise is composed of thermal noise and $1/f$ noise. The thermal noise is due to agitated carriers in the channel that cause a randomly varying current. For the $1/f$ noise, since $1/f$ noise corner is usually less than 1 MHz,

this noise can be neglected at radio frequency. The gate noise is induced by the fluctuating channel potential that couples capacitively into the gate terminal. i_{ng} can be expressed as the sum of two components, the first of which is fully correlated with i_{nd}, called $i_{ng,c}$, the second of which is uncorrelated with i_{nd}, called $i_{ng,u}$.

Hence,
$$i_{ng} = i_{ng,c} + i_{ng,u} \tag{5.1}$$

with the correlation coefficient
$$c = \frac{\overline{i_{ng}\, i_{nd}^{*}}}{\sqrt{\overline{|i_{ng}|^2}\;\overline{|i_{nd}|^2}}} \tag{5.2}$$

The drain noise power $\overline{|i_{dn}|^2}$ and the gate noise power $\overline{|i_{ng}|^2}$ can be expressed as

$$\overline{|i_{dn}|^2} = 4kT\gamma\, g_{do} \Delta f, \tag{5.3}$$

$$\overline{|i_{ng}|^2} = 4kT\delta \left(\frac{\omega^2 C_{gs}^{\ 2}}{5 g_{do}} \right) \Delta f \tag{5.4}$$

where k is Boltzmann's constant, T is the absolute temperature, γ and δ are called the excess noise factor and the noise coefficient, respectively. g_{do} is the transistor tranconductance with v_{ds} equal to zero. Δf is the noise bandwidth.

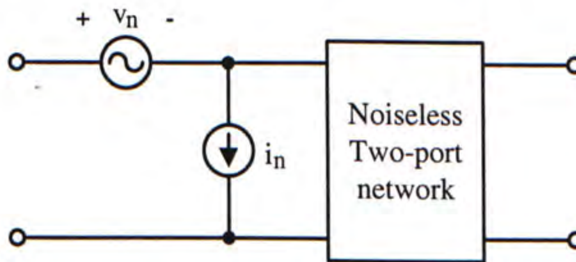


Figure 5.2: Representation of a noisy two-port network

Alternatively, the noisy MOSFET can be modeled as a noiseless two-port network with the external noise sources i_n and v_n [17], as shown in Figure 5.2.

To express the relation between i_n and v_n, i_n is written as

$$i_n = i_{nu} + Y_c\, v_n \tag{5.5}$$

where i_{nu} is the uncorrelated noise source, Y_c is correlation admittance. It implies that i_n contains both uncorrelated and correlated noise currents. Moreover, the necessary noise powers can be expressed as

$$\begin{cases} \overline{|\, i_{nu} \,|^2} = 4\, kTG_u \Delta f & (5.6) \\ \overline{|\, v_n \,|^2} = 4\, kTR_n \Delta f & (5.7) \end{cases}$$

where G_u and R_n are the uncorrelated noise conductance and the equivalent noise resistance, respectively.

5.2 Noise Calculation using Noisy Two-Port Network

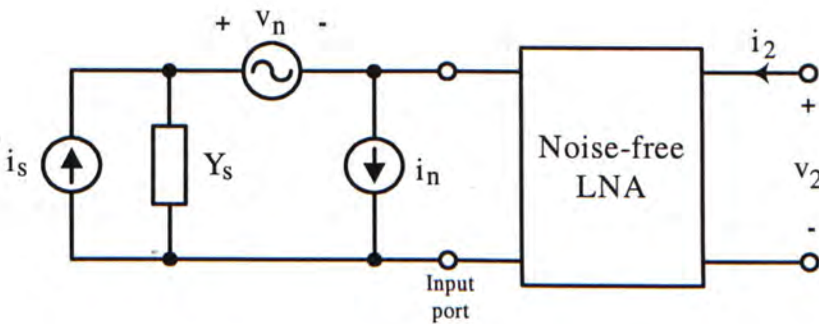


Figure 5.3: Noise model for calculation of LNA noise factor

To determine the noise factor of a LNA using noisy two-port analysis, a complete two-port model is required. It is shown in Figure 5.3. i_s and Y_s are noise current and admittance of the source, respectively. Conceptually, the noise factor F is defined as

$$F = \frac{\overline{|i_{sc}|^2}}{\overline{|i_s|^2}} \tag{5.8}$$

where i_{sc} is the short-circuit current at the input port of the noise-free LNA with upward direction. From the circuit shown,

$$\begin{aligned} i_{sc} &= i_n + v_n Y_s - i_s \\ \overline{|i_{sc}|^2} &= \overline{(i_n + v_n Y_s - i_s)(i_n + v_n Y_s - i_s)^*} \\ &= \overline{(i_n + v_n Y_s)(i_n + v_n Y_s)^*} + \overline{|i_s|^2} - 2\,Re\left\{ \overline{(i_n + v_n Y_s) i_s^*} \right\} \end{aligned} \tag{5.9}$$

Since $(i_n + v_n Y_s)$ and i_s are uncorrelated,

$$\overline{(i_n + v_n Y_s) i_s^*} = 0 \tag{5.10}$$

$$\overline{|i_{sc}|^2} = \overline{(i_n + v_n Y_s)(i_n + v_n Y_s)^*} + \overline{|i_s|^2} \tag{5.11}$$

By substituting (5.5) into (5.11),

$$\begin{aligned} \overline{|i_{sc}|^2} &= \overline{[\,i_{nu} + v_n (Y_s + Y_c)\,][\,i_{nu} + v_n (Y_s + Y_c)\,]^*} + \overline{|i_s|^2} \\ &= \overline{|i_{nu}|^2} + |Y_s + Y_c|^2\, \overline{|v_n|^2} + \overline{|i_s|^2} \end{aligned} \tag{5.12}$$

By substituting (5.12) into (5.8), the noise factor F is given by

$$\begin{aligned} F &= \frac{\overline{|i_{nu}|^2} + |Y_s + Y_c|^2\, \overline{|v_n|^2} + \overline{|i_s|^2}}{\overline{|i_s|^2}} \\ &= 1 + \frac{\overline{|i_{nu}|^2} + |Y_s + Y_c|^2\, \overline{|v_n|^2}}{\overline{|i_s|^2}} \end{aligned} \tag{5.13}$$

Let $Y_s = G_s + jB_s$, $Y_c = G_c + jB_c$, and using (5.6), (5.7) and $\overline{|i_s|^2} = 4\,kTG_s\Delta f$, then F is simplified as

$$F = 1 + \frac{4kTG_u\Delta f + |(G_s + G_c) + j(B_s + B_c)|^2 4kTR_n\Delta f}{4kTG_s\Delta f}$$

$$= 1 + \frac{G_u}{G_s} + \frac{R_n}{G_s}\left[(G_s + G_c)^2 + (B_s + B_c)^2\right] \quad (5.14)$$

By differentiating F with respect to G_s and B_s, the minimum noise factor F_{min} and the corresponding optimum noise source admittance Y_{opt} can be obtained, which are

$$\begin{cases} F_{min} = 1 + 2R_n\left(G_{opt} + G_c\right) & (5.15) \\ Y_{opt} = G_{opt} + jB_{opt} = \sqrt{G_c^2 + \frac{G_u}{R_n}} - jB_c & (5.16) \end{cases}$$

The expression for F is re-arranged as

$$F = F_{min} + \frac{R_n}{G_s}\left|Y_s - Y_{opt}\right|^2 \quad (5.17)$$

Equation (5.17) provides an important information about the noise optimization of a two-port LNA. If Y_s is transformed to be exactly equal to Y_{opt}, the minimum noise factor F_{min} can be achieved, no matter what output matching network is connected. This technique is known as Low Noise Matching. However, it is very difficult, but not impossible, that low noise matching and conjugate matching occurs simultaneously [31].

5.3 Noise Calculation using Small-Signal Model

5.3.1 Low Noise Amplifier with Inductive Source Degeneration

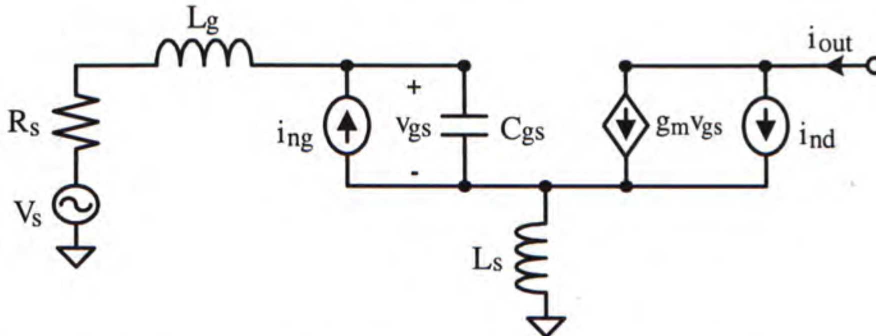


Figure 5.4: Small-signal noise model of an inductively source degenerated LNA

By using small-signal noise analysis, the noise factor of a LNA with inductive source degeneration is determined [32, 33]. Its full small-signal noise model is shown in Figure 5.4. To simplify the analysis, all the parasitic resistances and the output stage are neglected.

According to the analysis, each output noise current due to the individual independent noise source should be determined first. Then, by substituting them into the noise formula, the resultant noise factor can be obtained.

a) Considering the output noise current due to the input source V_s, $i_{out,s}$, the following noise model can be used.

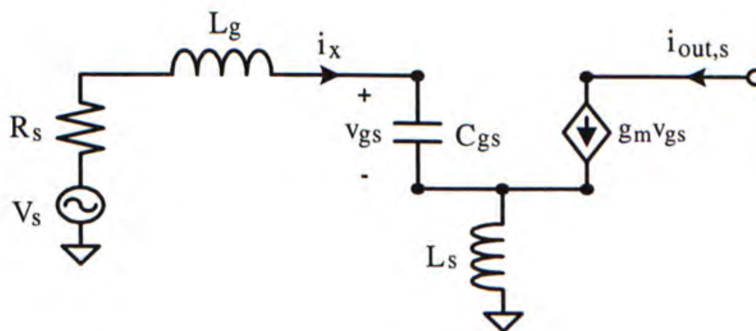


Figure 5.5: Small-signal noise model with V_s only

$$i_x = \frac{V_s}{R_s + \frac{g_m L_s}{C_{gs}} + \left[j\omega\left(L_g + L_s\right) + \frac{1}{j\omega C_{gs}} \right]}$$

$$i_{out,s} = g_m v_{gs} = \left(\frac{g_m}{j\omega C_{gs}} \right) \frac{V_s}{\left\{ R_s + \frac{g_m L_s}{C_{gs}} + j\left[\frac{1-\omega^2 C_{gs}\left(L_g + L_s\right)}{j\omega C_{gs}} \right] \right\}} \tag{5.18}$$

At resonance, $\omega_0{}^2\left(L_g + L_s\right)C_{gs} = 1$, Equation (5.18) becomes

$$i_{out,s} = \left(\frac{\omega_T}{j\omega_0} \right) \frac{V_s}{\left(R_s + \omega_T L_s\right)} \tag{5.19}$$

where the cut-off frequency $\omega_T = \frac{g_m}{C_{gs}}$. (5.20)

Hence, $$\overline{\left| i_{out,s} \right|^2} = \left(\frac{\omega_T}{\omega_0} \right)^2 \frac{4kTR_s \Delta f}{\left(R_s + \omega_T L_s\right)^2} \tag{5.21}$$

b) Considering the output noise current due to i_{nd} and i_{ng}, $i_{out,nd,ng}$, the noise model can be modified as follow.

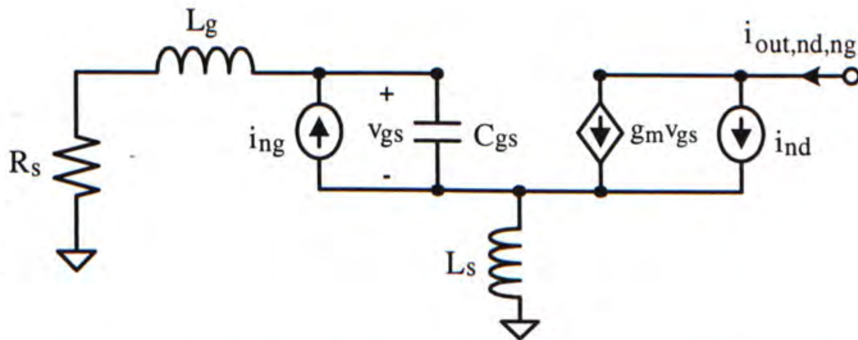


Figure 5.6: Small-signal noise model with i_{nd} and i_{ng} only

To determine $i_{out,nd,ng}$, principle of superposition can be applied and it is found that

$$i_{out,nd,ng} = \left[\left(\frac{\omega_T}{j\omega_0} \right) (1 + jQ_L) i_{out,ng} + i_{nd} \right] \left(\frac{R_s}{R_s + \omega_T L_s} \right) \tag{5.22}$$

where $$Q_L = \frac{\omega_0 (L_g + L_s)}{R_S} = \frac{1}{\omega_0 C_{gs} R_S} \tag{5.23}$$

$$\therefore \overline{|i_{out,nd,ng}|^2} = \overline{\left[\left(\frac{\omega_T}{j\omega_0} \right) (1 + jQ) i_{ng} + i_{nd} \right] \left[\left(\frac{\omega_T}{j\omega_0} \right) (1 + jQ) i_{ng} + i_{nd} \right]^*} \times \left(\frac{R_s}{R_s + \omega_T L_s} \right)^2$$

$$= \left(\frac{R_s}{R_s + \omega_T L_s} \right)^2 \left\{ \left(\frac{\omega_T}{\omega_0} \right)^2 (1 + Q_L^2) \overline{|i_{ng}|^2} + \overline{|i_{nd}|^2} + 2 Re \left[\left(\frac{\omega_T}{j\omega_0} \right) (1 + jQ_L) \overline{i_{ng} i_{nd}^*} \right] \right\} \tag{5.24}$$

Since $\overline{i_{ng} i_{nd}^*} = c \sqrt{\overline{|i_{ng}|^2}\, \overline{|i_{nd}|^2}} = j |c| \sqrt{\overline{|i_{ng}|^2}\, \overline{|i_{nd}|^2}}$,

$$\overline{|i_{out,nd,ng}|^2} = \left(\frac{R_s}{R_s + \omega_T L_s} \right)^2 \left\{ \left(\frac{\omega_T}{\omega_0} \right)^2 (1 + Q_L^2) \overline{|i_{ng}|^2} + \overline{|i_{nd}|^2} + 2|c| \sqrt{\overline{|i_{ng}|^2}\, \overline{|i_{nd}|^2}} \left(\frac{\omega_T}{\omega_0} \right) \right\} \tag{5.25}$$

By substituting (5.3) and (5.4) into (5.25),

$$\overline{|i_{out,nd,ng}|^2} = \left\{ \frac{\delta \alpha^2}{5\gamma} (1 + Q_L^2) + 1 + 2|c| \sqrt{\frac{\delta \alpha^2}{5\gamma}} \right\} \frac{4kT\gamma g_{d0} R_s^2 \Delta f}{(R_s + \omega_T L_s)^2} \tag{5.26}$$

where $$\alpha = \frac{g_m}{g_{do}} \tag{5.27}$$

c) Finally, the noise factor can be determined by

$$F = \frac{\overline{\left| i_{out,s} \right|^2} + \overline{\left| i_{out,nd,ng} \right|^2}}{\overline{\left| i_{out,s} \right|^2}} = 1 + \frac{\overline{\left| i_{out,nd,ng} \right|^2}}{\overline{\left| i_{out,s} \right|^2}} \tag{5.28}$$

By substituting (5.21) and (5.26) into (5.28), then F becomes

$$F = 1 + \frac{\left\{ \frac{\delta\alpha^2}{5\gamma}\left(1+Q_L^{\,2}\right) + 1 + 2\left| c \right| \sqrt{\frac{\delta\alpha^2}{5\gamma}} \right\} \frac{4kT\gamma g_{d0} R_s^{\,2} \Delta f}{\left(R_s + \omega_T L_s\right)^2}}{\left(\frac{\omega_T}{\omega_0}\right)^2 \frac{4kTR_s \Delta f}{\left(R_s + \omega_T L_s\right)^2}}$$

$$= 1 + \frac{\gamma}{\alpha Q_L}\left(\frac{\omega_0}{\omega_T}\right)\left\{ \frac{\delta\alpha^2}{5\gamma}\left(1+Q_L^{\,2}\right) + 1 + 2\left| c \right| \sqrt{\frac{\delta\alpha^2}{5\gamma}} \right\} \tag{5.29}$$

5.3.2 Common-Gate Low Noise Amplifier

The small-signal noise model of a common-gate amplifier is shown in Figure 5.7.

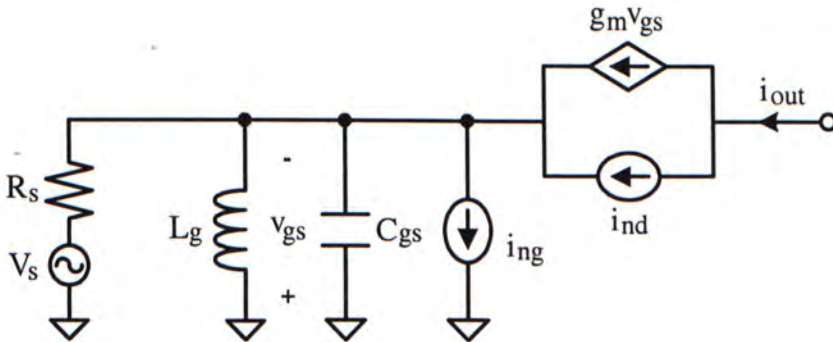


Figure 5.7: Small-signal noise model of a common-gate LNA

Similar to the derivation steps in section 5.3.1, the following equations can be

obtained.

$$\overline{\left| i_{out,s} \right|^2} = \frac{4kTR_s \Delta f}{\left(R_s + \dfrac{1}{g_m} \right)^2} \tag{5.30}$$

$$\overline{\left| i_{out,nd,ng} \right|^2} = \left\{ \frac{\delta \alpha^2}{5\gamma} \left(\frac{\omega_0}{\omega_T} \right)^2 R_s^{\,2} + \frac{1}{g_m^{\,2}} \right\} \frac{4kT \gamma g_{d0} \Delta f}{\left(R_s + \dfrac{1}{g_m} \right)^2} \tag{5.31}$$

By substituting (5.30) and (5.31) into (5.28), consequently,

$$F = 1 + \frac{\left\{ \dfrac{\delta \alpha^2}{5\gamma} \left(\dfrac{\omega_0}{\omega_T} \right)^2 R_s^{\,2} + \dfrac{1}{g_m^{\,2}} \right\} \dfrac{4kT \gamma g_{d0} \Delta f}{\left(R_s + \dfrac{1}{g_m} \right)^2}}{\dfrac{4kTR_s \Delta f}{\left(R_s + \dfrac{1}{g_m} \right)^2}}$$

$$= 1 + \frac{\gamma g_m}{\alpha R_s} \left\{ \frac{\delta \alpha^2}{5\gamma} \left(\frac{\omega_0}{\omega_T} \right)^2 R_s^{\,2} + \frac{1}{g_m^{\,2}} \right\} \tag{5.32}$$

Chapter 6

Design of an ESD-Protected CMOS Low Noise Amplifier

In this project, we will present a new ESD-protected CMOS LNA circuit. The new design is a two-stage LNA with the operating frequency at 1.8 GHz. The supply voltage of smaller than 2 V is preferred for low voltage design. The most important issue in this work is to demonstrate a new concept of using CGISM to do ESD protection. The proposed LNA is constructed to verify its functionality. At the same time, it will show that CGISM does not affect the performance of LNA.

The detailed description of the design of the proposed LNA is shown in the following. Most of the design techniques used are mentioned in Chapter 4. The implementation is based on an AMS 0.35-μm CMOS technology. Moreover, all the simulations are carried out with Cadence SpectreRF and the results are reported below.

6.1 Design of DC Biasing Circuitry

LNA requires DC biasing circuitry, a good DC biasing circuit can give a stable operating point to the LNA, so that a steady performance is achieved. Ideally, the DC biasing circuit should not deteriorate the LNA performance. At the same time, it should ensure that there is no RF signal coupling into the DC supply. Figure 6.1 gives a DC biasing circuit that is used for the proposed LNA.

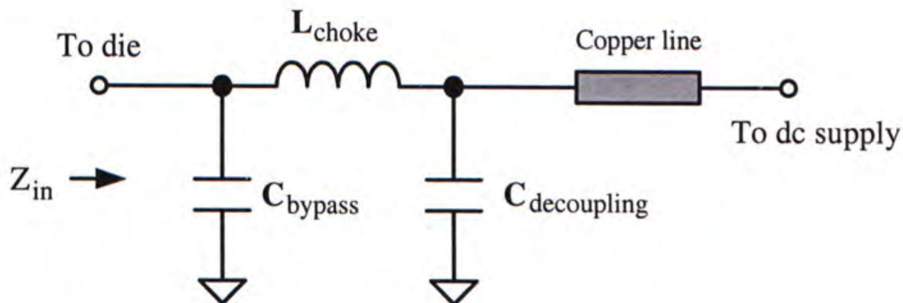


Figure 6.1: DC biasing circuitry of the LNA

Each of the components involved in this circuit plays an important role in stabilizing the LNA.

1. The RF bypassed capacitor C_{bypass} provides RF ground at 1.8 GHz;
2. The RF choke L_{choke} provides a high impedance path to prevent high frequency signal from entering the DC supply. Likewise, it provides a low impedance path for DC signal to bias the LNA;
3. The decoupling capacitors $C_{decoupling}$ short the unwanted low frequency coupling signals to ground.

In practice, it is difficult to implement these components in CMOS process, because of their bulky sizes. Alternatively, they are realized by surface-mount capacitors and inductor. Table 6.1 lists out the practical values used for implementing the

designed circuit. The resultant circuit is simulated to verify its impedance Z_{in}, and the result is given in Figure 6.2.

Component	Value
C_{bypass}	8 pF
L_{choke}	39 nH
$C_{decoupling}$	100 pF
	100 nF

Table 6.1: Surface-mount components used to realize the DC biasing circuit

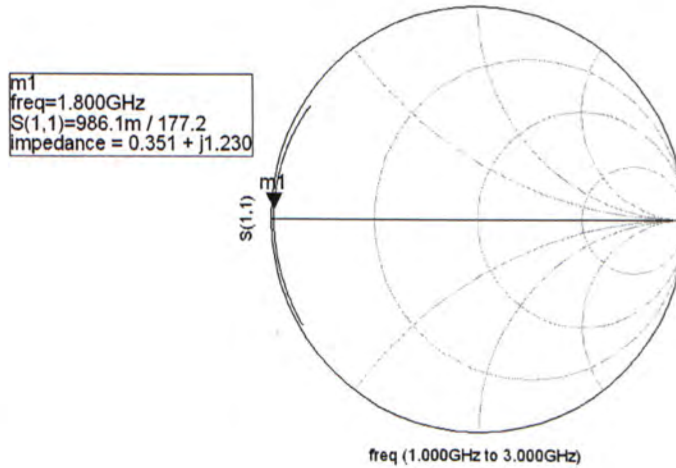


Figure 6.2: Simulated impedance of the DC biasing circuit

In the proposed LNA, the impedance of the ideal DC biasing circuit should be zero at 1.8 GHz. From the simulation result, it is found that Z_{in} is equal to 0.351+j1.230, which is very close to zero. In addition, Z_{in} remains constant no matter how long the copper line is constructed. This implies the DC biasing circuitry is very stable and is not affected by the external DC power line.

6.2 Design of Two-Stage Architecture

As stated in the project requirements, the proposed new LNA must present similar performance as a conventional design. Since the objective focuses on the new ESD protection method, there is no need to do noise optimization of the LNA. The expected power gain should not be less than 10 dB, a single-stage common-gate LNA with a low supply voltage is not enough to provide a sufficient power gain. Therefore, a two-stage architecture is designed.

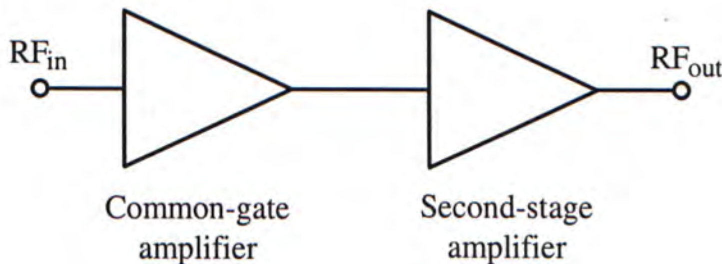


Figure 6.3: Architecture of the proposed LNA

Figure 6.3 shows the architecture of the proposed LNA where two amplifiers are cascaded to provide the high power gain. The common-gate amplifier is placed at the first stage to implement CGISM. Then, the second-stage amplifier is employed to enhance the power amplification. The whole LNA is designed with maximum gain, thus, the two amplifiers should have a good impedance match.

6.2.1 Design of Common-Gate Input Stage

The first stage of the LNA is a common-gate amplifier as illustrated in Figure 6.4. It is used to provide ESD protection based on CGISM. There is basically no difference between this circuit and a conventional common-gate LNA, except the value of the loading inductor L_d. Its inductance should be chosen to form a low impedance path for the fast ESD pulse. Table 6.2 tabulates the component values

used in the common-gate input stage. The supply voltage V_{dd} is 1.5 V.

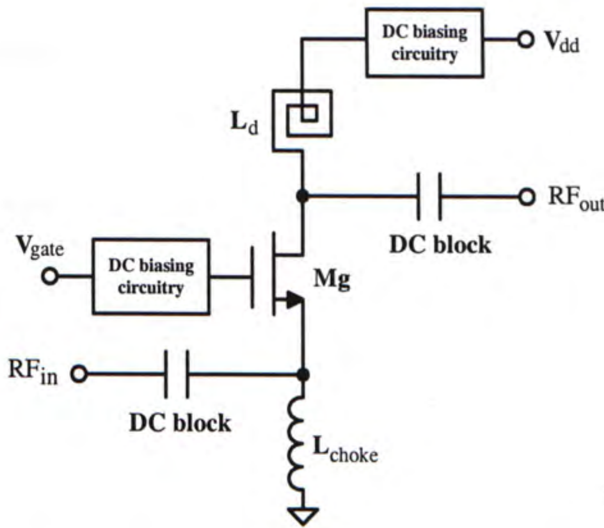
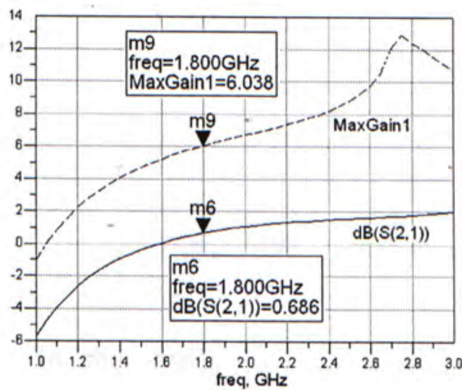


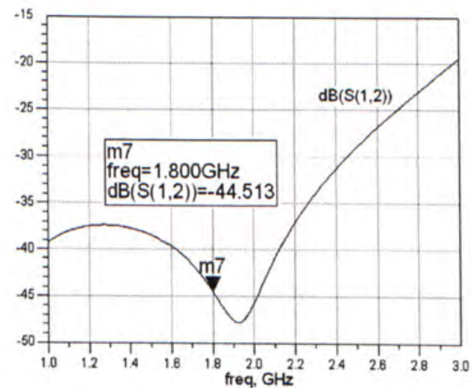
Figure 6.4: Schematic of the common-gate input stage

Component	Value
$(W/L)_{Mg}$	240/0.35
L_g	5.1 nH
L_{choke}	39 nH
DC block	Ideal in simulation

Table 6.2: Component values used in the common-gate input stage



(a) Power gain *S(2,1)* & maximum power gain *MaxGain1*



(b) Reverse gain *S(1,2)*

Figure 6.5: Simulation results of the common-gate input stage

Figure 6.5 shows the simulated power gain, maximum power gain and reverse gain of the common-gate input stage. It is observed that the maximum power gain of the designed circuit is about 6 dB at 1.8 GHz, assumes both input and output ports are perfectly matched to 50 Ω. The reverse isolation is more than 44 dB. This high reverse isolation is attributed to the common-gate topology. Unfortunately, there is a lack of an accurate simulator to perform an ESD simulation. Therefore, the ESD protection capability of the proposed CGISM can only be verified by measurement which will be addressed in Chapter 8.

6.2.1 Design of Second-Stage Amplifier

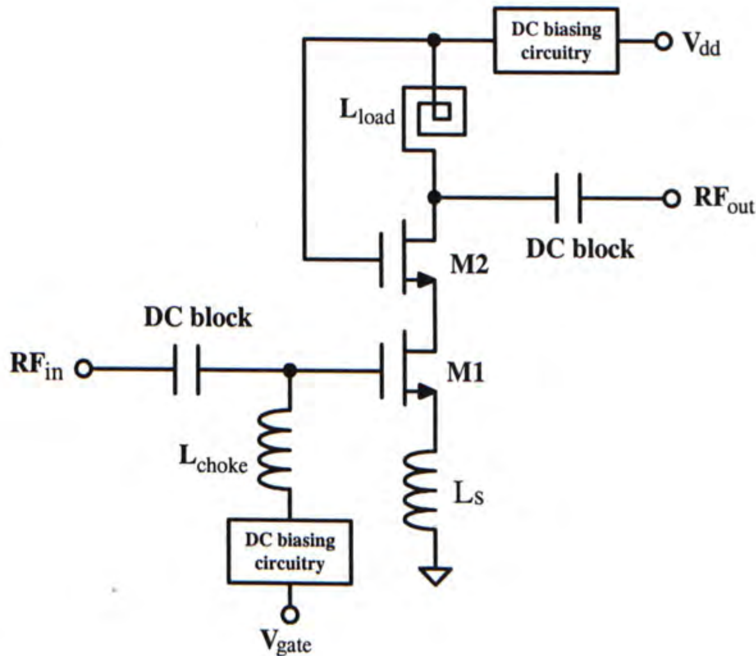


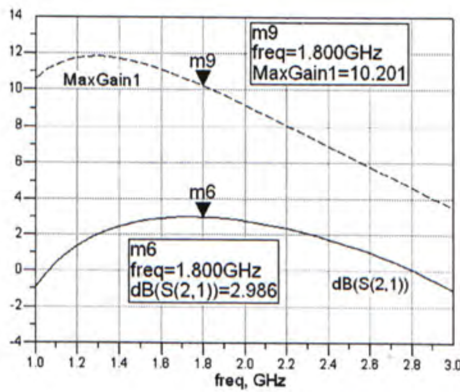
Figure 6.6: Schematic of the second-stage amplifier

In the design of the second-stage amplifier, a cascoded common-source amplifier is chosen to achieve high gain. Figure 6.6 illustrates the schematic diagram of the second-stage amplifier. All the components shown are integrated in the test chip, except for the DC biasing circuitries and L_s. L_s is implemented by a

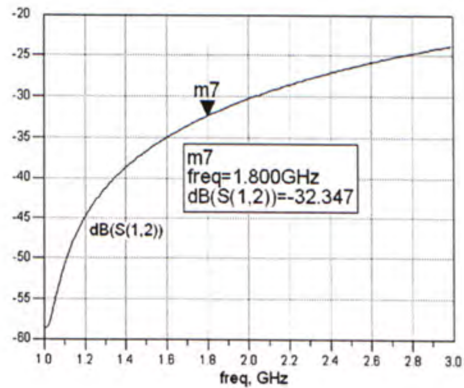
bondwire of 2 nH. Table 6.3 tabulates the component values for the second-stage amplifier. The same as the first-stage amplifier, V_{dd} is 1.5 V.

Component	Value
$(W/L)_{M1,2}$	300/0.35
L_{load}	4.25 nH
L_{choke}	Ideal in simulation
DC block	Ideal in simulation

Table 6.3: Component values used in the second-stage amplifier



(a) Power gain *S(2,1)* & maximum power gain *MaxGain1*



(b) Reverse gain *S(1,2)*

Figure 6.7: Simulation results of the second-stage amplifier

Figure 6.7 shows the simulation results of the second-stage amplifier. By observing the plot of MaxGain1, the maximum power gain of the designed common-source amplifier is found to be 10.201 dB at 1.8 GHz. It is higher than that of the common-gate input stage mentioned above. For the reverse isolation, it is found that the simulation result is 32.347 dB, which it is lower than the common-gate input stage.

6.3 Stability Consideration

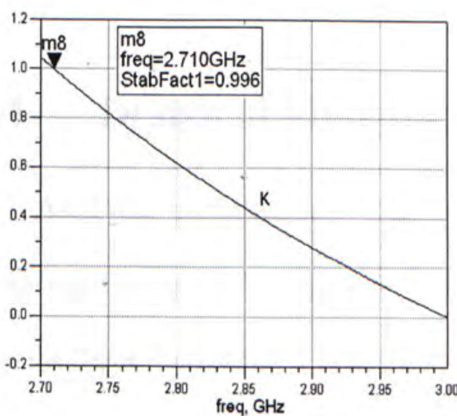
Stability of an amplifier is an inevitable consideration in design process. Mathematically, we can determine the stability from the S-parameters, matching networks and terminations [17, 20, 34]. It is desirable to have an amplifier that is unconditionally stabile over a wide range of frequencies.

The necessary and sufficient conditions for unconditional stability of the amplifier are: (1) the stability factor K is greater than unity and, (2) the stability measure B is positive, i.e.

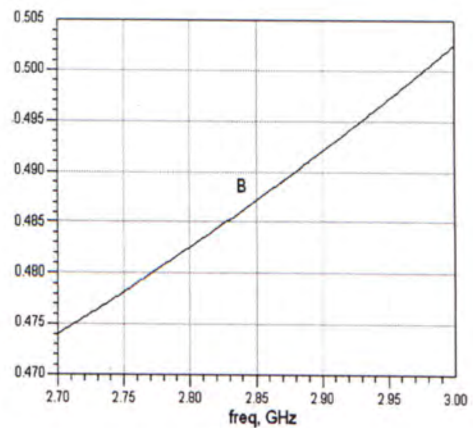
$$K = \frac{1 - |S_{11}|^2 - |S_{22}|^2 + |S_{11}S_{22} - S_{12}S_{21}|^2}{2|S_{12}S_{21}|} > 1 \tag{6.1}$$

$$B = 1 + |S_{11}|^2 - |S_{22}|^2 - |S_{11}S_{22} - S_{12}S_{21}|^2 > 0 \tag{6.2}$$

In this research project, the proposed LNA is required to be unconditionally stable from DC to 3 GHz. Before cascading the first and second-stage amplifier together, the stabilities are checked.



(a) Stability factor K



(b) Stability measure B

Figure 6.8: Unstable region of the common-gate input stage

Referring to Figure 6.8, by analyzing the common-gate input stage, it is found that its stability factor is less than 1 from 2.71 GHz to 3 GHz, even though its stability measure is greater than zero. In this condition, the amplifier is said to be potentially unstable within this frequency range and it may oscillate at some source and load terminations. To stabilize the amplifier so that the conditions of unconditional stability within the desired frequency range are achieved, there are two methods that can be applied, which are:

1. to add resistors at both input and output ports;
2. to choose the proper input and output matching networks according to the source and load stability circles.

Adding resistors to the common-gate input stage will greatly degrade the gain and noise performance, thus, it is not recommended. Therefore, (2) is preferred.

In the stability analysis of the second-stage amplifier, both its K and B are greater than 1 and 0, respectively. Therefore, it is proved to be unconditionally stable for all passive source and load terminations. All the information analyzed above will be used for the design of the matching networks.

6.4 Design of Matching Networks

After the preparation of the two single-stage amplifiers, we need to cascade them together using the suitable matching networks to maximize the power gain of the resultant two-stage LNA [6, 35]. Furthermore, standard impedance can be presented at both the input and output ports. Figure 6.9 illustrates the block diagram of how the two single-stage amplifiers are connected to form the proposed LNA.

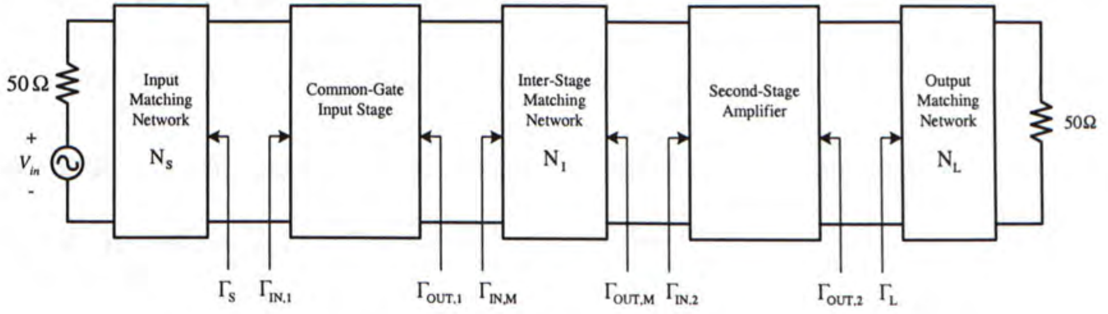


Figure 6.9: Block diagram of the overall proposed LNA

Figure 6.9 illustrates the connection and matching networks between the two single-stage amplifiers, such as the inter-stage matching network N_I, input matching network N_S and output matching network N_L. They are employed to satisfy the following conditions:

$$\Gamma_S = \Gamma_{IN,1}^* \tag{6.3}$$

$$\Gamma_{OUT,1} = \Gamma_{IN,M}^* \tag{6.4}$$

$$\Gamma_{OUT,M} = \Gamma_{IN,2}^* \tag{6.5}$$

$$\Gamma_{OUT,2} = \Gamma_L^* \tag{6.6}$$

Mathematically, the coefficients Γ_S, $\Gamma_{IN,M}$, $\Gamma_{OUT,M}$ and Γ_L can be calculated by using the following pair of equations based on Figure 2.1, which assumes the condition for simultaneous conjugate match of an amplifier [17, 20].

$$\Gamma_S = S_{11} + \frac{S_{12} S_{21} \Gamma_L}{1 - S_{22} \Gamma_L} = \Gamma_{IN}^* \tag{6.7}$$

$$\Gamma_L = S_{22} + \frac{S_{12} S_{21} \Gamma_S}{1 - S_{11} \Gamma_S} = \Gamma_{OUT}^* \tag{6.8}$$

These equations are applied to find the necessary reflection coefficients in the following section.

6.4.1 Design of Inter-Stage Matching Network

We have solved Equation (6.7) and (6.8) to determine $\Gamma_{IN,M}$, $\Gamma_{OUT,M}$ for simultaneous conjugate matches between the two single-stage amplifiers at 1.8 GHz, and the results are listed in Table 6.4.

$\Gamma_{IN,M}$	0.5396-j0.5882
$\Gamma_{OUT,M}$	0.7451+j0.2999

Table 6.4: $\Gamma_{IN,M}$, $\Gamma_{OUT,M}$ for simultaneous conjugate matches between the two amplifiers and the inter-stage matching network at 1.8 GHz

Based on these values, the required inter-stage matching network is realized using lumped capacitors and inductor as shown in Figure 6.10. The necessary values for the lumped components C_d, C_{block} and L_m are tabulated in Table 6.5.

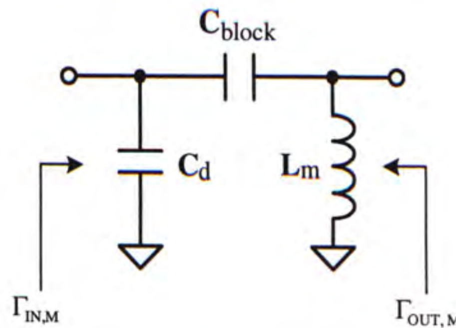


Figure 6.10: Schematic of the inter-stage matching network

Component	Value
C_d	580 fF
C_{block}	330 fF
L_m	6.8 nH

Table 6.5: Component values used in the inter-stage matching network

Besides providing simultaneous conjugate matches, the inter-stage matching network also serves other functions, namely,

1. C_d combines with the loading inductor of the common-gate input stage to form a LC tank circuit for gain enhancement;
2. C_{block} prevents the DC signals from distorting the operating points of each other, and provides a high impedance path to prevent the ESD from coupling into the second-stage amplifier;
3. L_m provides the DC path for the DC biasing circuitry to bias the second-stage amplifier.

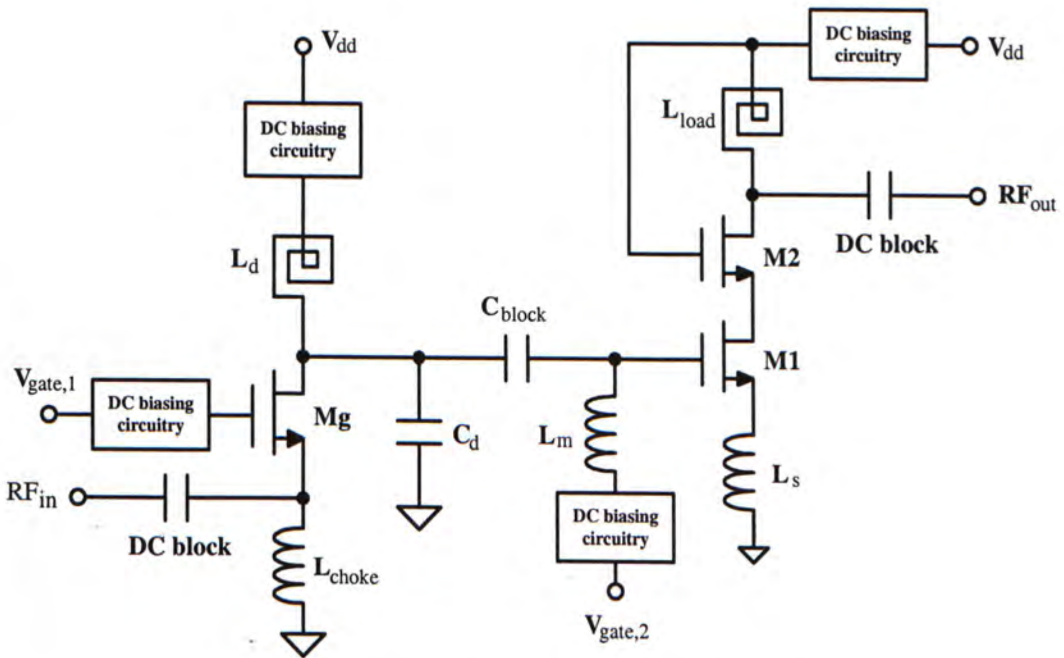
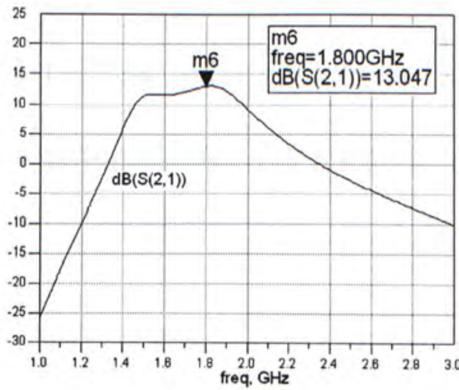
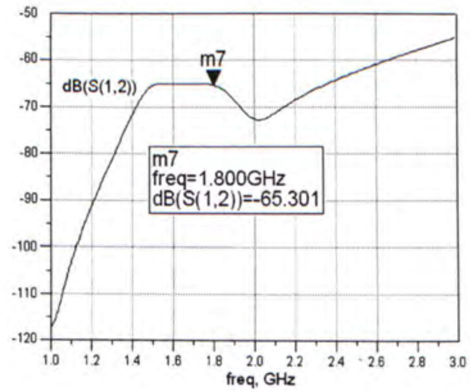


Figure 6.11: Schematic of the core LNA

A completed schematic diagram of the new two-stage LNA is shown in Figure 6.11. In this project, all the components shown are integrated on the single test chip, except for L_{choke}, DC block and DC biasing circuit. However, the passive input and output matching networks are not integrated on the test chip, because the quality of the on-chip passive networks is not good enough.



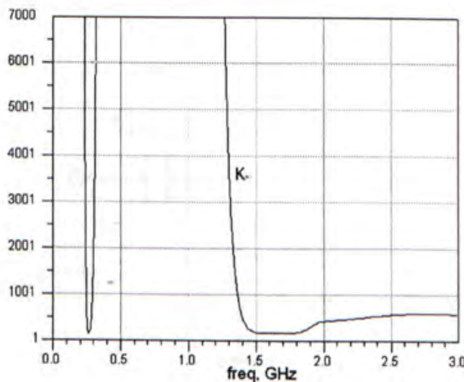
(a) Power gain *S(2,1)*



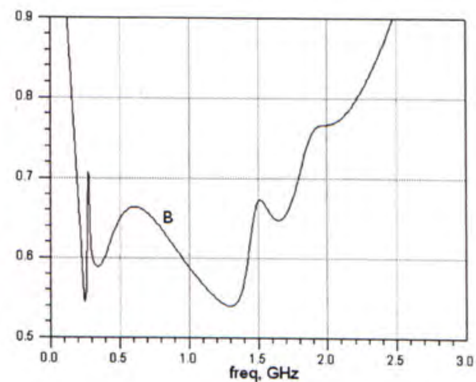
(b) Reverse gain *S(1,2)*

Figure 6.12: Simulation results of the core LNA

Figure 6.12 shows the simulation results of the core LNA. At 1.8 GHz, the circuit gives a power gain of more than 13 dB. Its reverse isolation is found to be about 65.3 dB. The stability of the core LNA is checked so as to ensure that the inter-stage matching network does not cause instability of the common-gate input stage. The simulation results shown in Figure 6.13(a) and (b) indicates that the necessary and sufficient conditions for unconditional stability from DC to 3 GHz are achieved, as K is greater than 1 and B is positive.



(a) Stability factor *K*



(b) Stability measure *B*

Figure 6.13: Determination of the stability conditions for the core LNA

6.4.2 Design of Input and Output Matching Networks

The final process is to design the input and output matching networks for the gain maximization. The matching network parameters are listed at Table 6.6.

Γ_S	-0.2971-j0.3654
Γ_L	0.5798-j0.2496

Table 6.6: Γ_S, Γ_L for simultaneous conjugate match of the core LNA at 1.8 GHz

Since $1/g_m$ termination is not applied to the common-gate input stage, the input impedance of the core LNA is not 50 Ω. The reason is that this method will make g_m too small to provide the enough gain for the first stage. As a result, a large value of g_m is designed and the resultant input impedance is transformed to 50 Ω by the external input matching network.

Figure 6.14 (a) and (b) shows the schematics of the input and output matching networks, respectively. They are realized by surface-mount components with the values tabulated in Table 6.7.

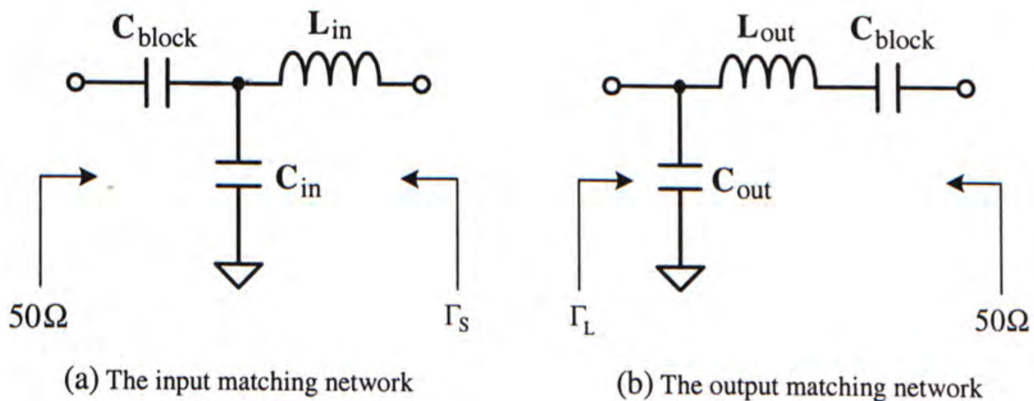
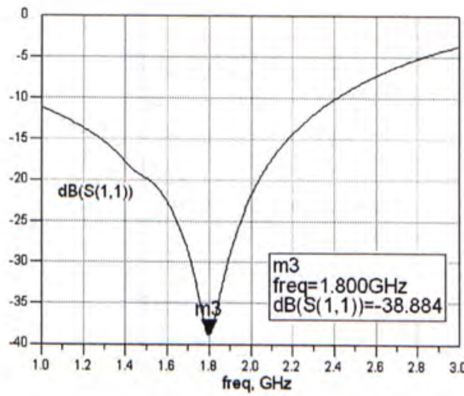


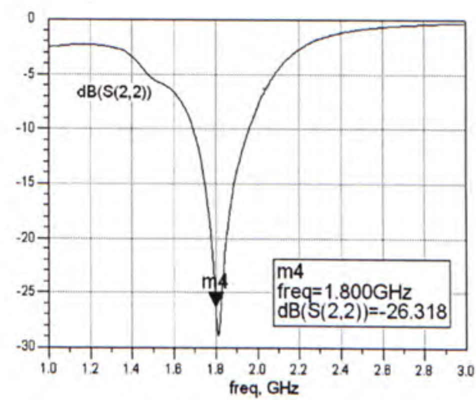
Figure 6.14: Schematics of the two matching networks

Component	Value
C_{in}	1.5 pF
L_{in}	0.75 nH
C_{out}	1 pF
L_{out}	6.8 nH
C_{block}	8 pH

Table 6.7: Surface-mount components used to realize two matching networks

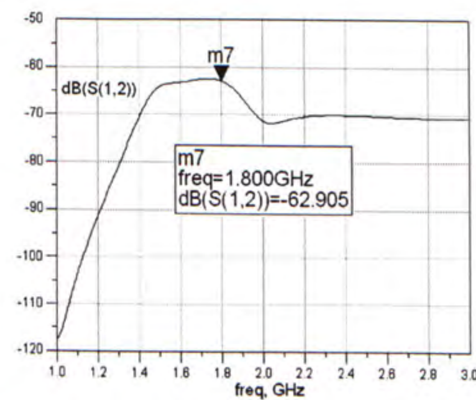


(a) Input return gain *S(1,1)*



(b) Output return gain *S(2,2)*

(c) Power gain *S(2,1)*



(d) Reverse gain *S(1,2)*

Figure 6.15: Simulation *S*-parameter of the proposed LNA

Figure 6.15 shows the simulated *S*-parameter of the proposed LNA. The input return loss, output return loss, power gain and reverse isolation are about 39 dB, 26.3 dB, 15.4 dB and 62.9 dB, respectively. The overall simulation results are summarized in Table 6.8.

Parameter	Value
Supply Voltage	1.5 V
Power Dissipation	30 mW
Operating Frequency	1.8 GHz
Power Gain	15.4 dB
Noise Figure	3.58 dB
NFmin	2.8 dB
Reverse Isolation	62.9 dB
Input Return Loss	39 dB
Output Return Loss	26.3 dB
Input (Output) 1-dB compression point	-17.5 dBm (-3.7 dBm)
Input (Output) IP3	-8.63 dBm (6.61.dBm)

Table 6.8: Simulated performance summary of the LNA

Chapter 7

Layout Considerations

Layout is the final step in integrated circuit design. It involves complicated knowledge to transform a circuit from schematic level to its physical representation [36]. The layout of an RF circuit is more difficult because the performance is highly sensitive to layout parasites. Therefore, in this chapter, the layout techniques of some basic devices and components are discussed, including that of MOS transistor, capacitor and spiral inductor.

In this project, the proposed LNA was fabricated with an AMS 0.35-μm CMOS C35 process. It is a 3-metal, 2-poly process. Attaching to the design kit, there are some special libraries for supporting RF circuit design. The layout of the proposed LNA is described in the following. Moreover, the post-layout simulation results are reported.

7.1 MOS Transistor

MOS transistor layout is a fundamental and widely used device in integrated circuit design. Its physical structure may have great influence on the final performance of the circuit. In particular, MOS transistor layout is concerned with the methods to reduce its area, parasitic resistances and capacitances. Among these methods, transistor fingering becomes a popular method [37, 38]. If a large

transistor is layout as a single unit, it will consume large area and produce large parasitic capacitance. By dividing it into small fingers and connecting them in parallel, as illustrated in Figure 7.1, the resultant device will be more compact. Thus, the efficiency of the area usage is improved.

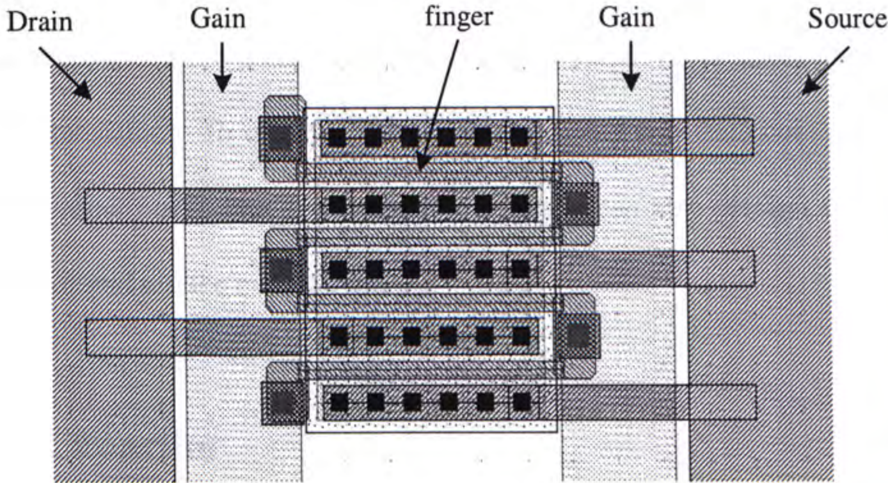


Figure 7.1: Layout design of the MOS transistor

Most CMOS RF circuits use very large gate width compared to mixed-signal and digital circuits. Because large gate width produces better linearity and power gain. However, the long polysilicon gate with high resistance generates large thermal noise that will degrade the noise performance. Fortunately, fingering technique reduces the overall resistance of the polysilicon gate. For a fingered transistor, the equivalent gate resistance R_g is determined by

$$R_g = \frac{R_{sh} W}{12 n^2 L} \tag{7.1}$$

where R_{sh} is the sheet resistance of the polysilicon. W and L are the gate width and the gate length of the MOS transistor, respectively. n is the number of gate fingers. It is found that R_g is inversely proportional to n^2. If n increases, R_g decreases rapidly. Likewise, fingering layout also reduce the total areas of drain

and source terminals because some of the drain and source terminals are overlapped. As a result, the parasitic capacitances associated with the drain and source terminals are also reduced.

We also use wide metal lines at the common-gate input to reduce the line resistances because of the large ESD current at the input. On the other hand, the substrate resistance should also be reduced so as to improve the noise performance of the MOS transistor. To deal with this purpose, many substrate contacts are placed around the transistor. The extra substrate contacts can also prevent the latch-up of the transistor and reduce body effect.

7.2 Capacitor

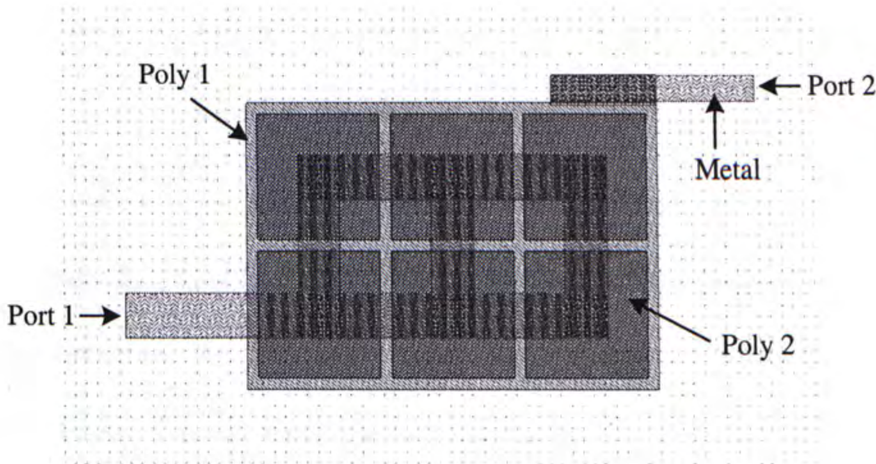


Figure 7.2: Layout design of the poly-poly capacitor

Capacitor is a useful passive component in RF circuits. It is used for matching, DC blocking and AC decoupling. In CMOS process, a capacitor can be realized by using two polysilicon layers in Figure 7.2. It demonstrates that the poly-poly capacitor is divided into several small unit capacitors and then, connected together in parallel. It is a popular method to implement large capacitor in a silicon wafer. As

different areas of polysilicons have different etch rates during the fabrication process, it may easily cause over-etching and leads to errors. To reduce etching effect, identical smaller capacitors are connected in parallel to form larger capacitor.

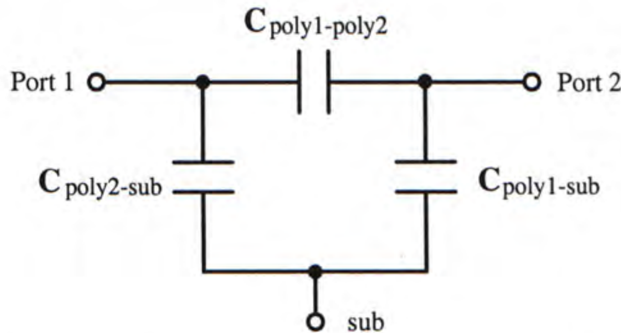


Figure 7.3: Schematic modeling of the poly-poly capacitor

Another important design issue is the parasites associated with the poly-poly capacitor. In the analysis of RF behaviour, the poly-poly capacitor can be modeled by a pi network as depicted in Figure 7.3. There are two parasitic capacitors $C_{poly1-sub}$, $C_{poly2-sub}$ formed at the ends of the main capacitor. Their capacitances depend on the areas of the two polysilicon layers. If the poly-poly capacitor is used in shunt connection, these parasites become part of the total capacitance. However, for series connection, the two parasitic capacitors will cause power loss through the substrate. Especially for large capacitor, the parasitic capacitances increase and more RF signal will lose through the substrate. As a result, the Q factor of the designed capacitor will be degraded substantially. In other words, it is difficult to design an on-chip high Q capacitor of greater than 10 pF.

Note that the entire capacitor is enclosed by many substrate contacts. It can reduce the substrate resistance and improve the noise performance of the capacitor.

7.3 Spiral Inductor

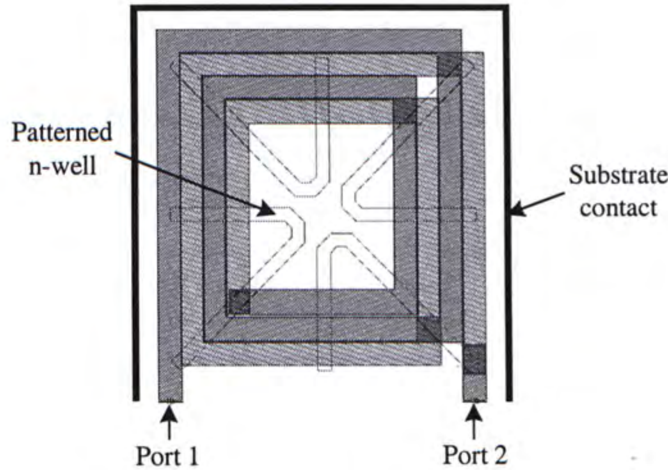


Figure 7.4: Layout design of the spiral inductor

The layout design of an inductor is a difficult task in high frequency circuit design. For the design of a low noise circuit, it is necessary to have ideal inductor which does not generate any noise. Figure 7.4 illustrates a spiral inductor realized in CMOS process. Practically, it is always recommended to use the top layer of metal for the inductor realization. This is because the top layer has the highest current density that minimizes the line resistance. Moreover, the separation between this layer and the substrate is the highest. Thus, the lowest signal power loses to the substrate and the Q factor can be improved.

Figure 7.5 shows the model of an on-chip inductor, where L_S, R_S and C_S are the series inductance, the line resistance and the coupling capacitance between two ports, respectively. C_{OX} is the oxide capacitance between the inductor metal and the substrate. R_{si} and C_{si} are the substrate resistance and the substrate coupling capacitance, respectively. Since the on-chip inductor is very bulky in CMOS integrated circuit, there is a strong capacitive coupling by C_{OX} to the substrate.

Consequently, it degrades the quality of the inductor.

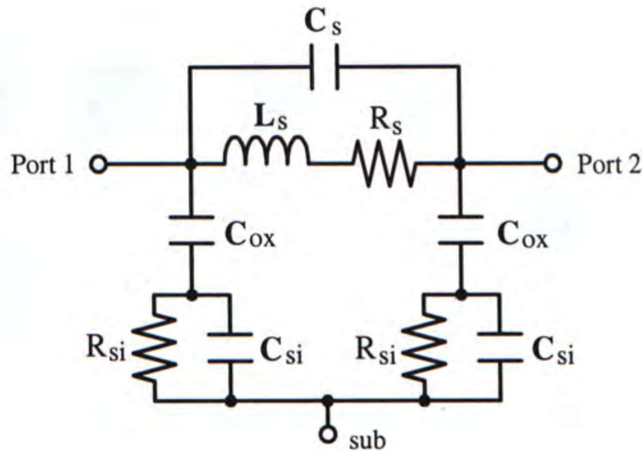


Figure 7.5: Schematic modeling of the spiral inductor

On the other hand, owning to the lossy silicon substrate, there is a strong eddy current induced by the magnetic field from the spiral inductor. This loop current formed in the substrate flows in a direction opposite to that of the current in the inductor. As a result, the magnetic field is reduced and the power loss of the inductor occurs. In order to reduce this power loss, one can place alternating wedges of n-well undernearth it [39] as shown in Figure 7.4. As the path of the induced loop current is cut off by these wedges of n-well, it reduces the effect of the eddy current on the magnetic field of the inductor. As a result, power loss is reduced and the Q factor can be increased.

Similar to the MOS transistor and poly-poly capacitor, the entire spiral inductor is enclosed by many substrate contacts. This arrangement reduces the substrate resistance and improves the noise performance of the inductor.

7.4 Layout of the Proposed Low Noise Amplifier

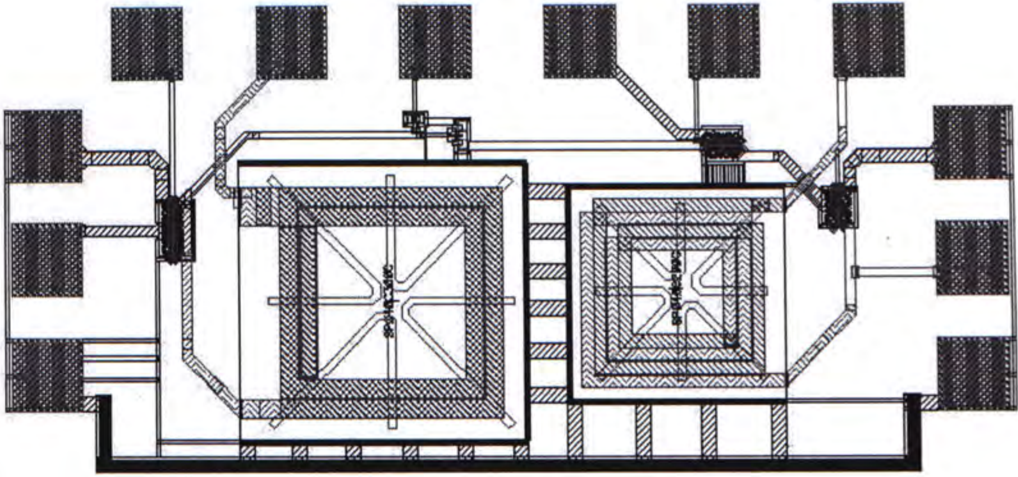
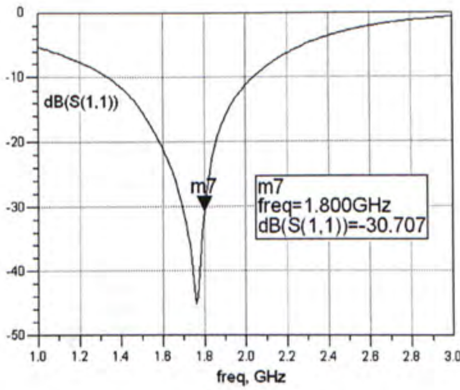


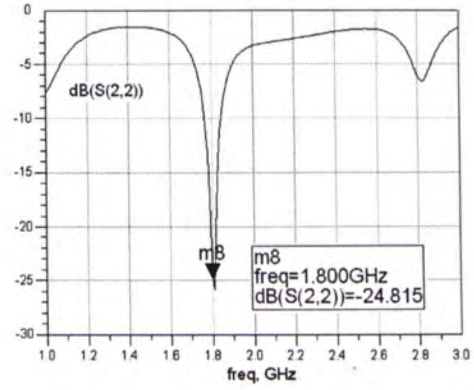
Figure 7.6: Layout design of the proposed LNA

Figure 7.6 illustrates the finalized layout of the proposed LNA. All the active transistors and the passive components shown in Figure 6.11 are drawn in the layout except for the DC biasing circuitries. The active area is 460 μm x 970 μm. From the layout consideration, there are two additional precautions that should be taken:

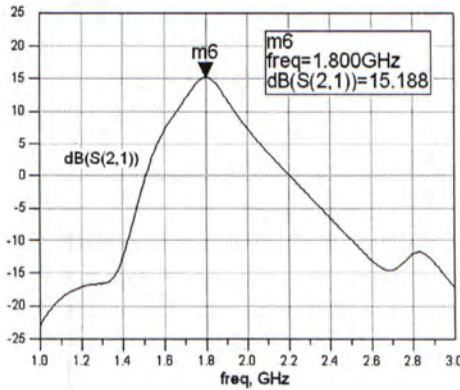
1. The adjacent spiral inductors should be placed in such a way that the high frequency currents are flowing through them in opposite directions with each other. It helps to reduce the magnetic coupling.
2. The design circuit should be bounded by a long substrate contacts if there are other circuits on the same die. As there may be some unwanted signals generated from these circuits, the substrate contacts can short them to ground and prevents them from coupling to the main circuit.



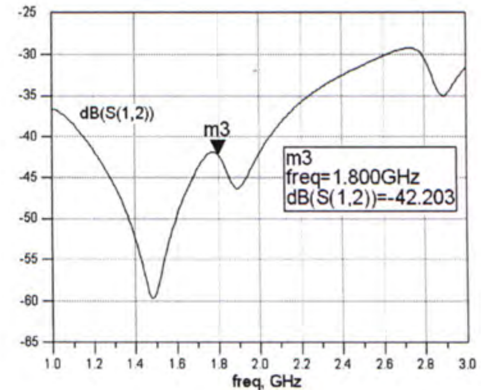
(a) Input return gain *S(1,1)*



(b) Output return gain *S(2,2)*



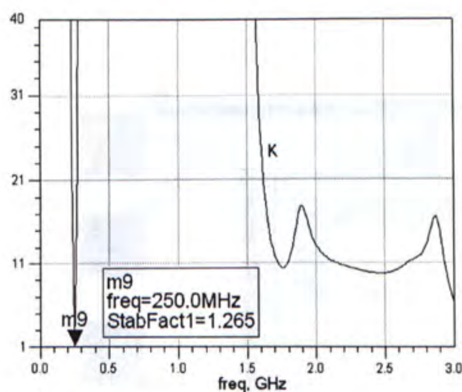
(c) Power gain *S(2,1)*



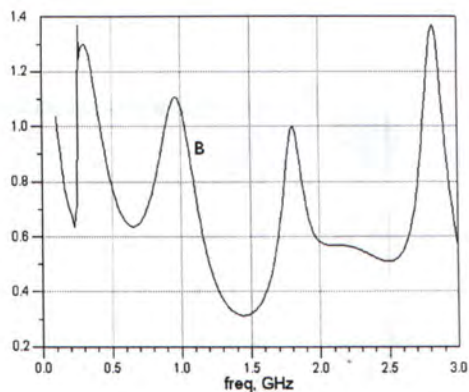
(d) Reverse gain *S(1,2)*

Figure 7.7: *S*-parameter of the proposed LNA in post-layout simulation

Figure 7.7 illustrates the post-layout simulation *S*-parameter of the proposed LNA. The input return loss, output return loss, power gain and reverse isolation are approximately 30.7 dB, 24.8 dB, 15.2 dB and 42.2 dB, respectively. The parameters K and B for the stability conditions are given in Figure 7.8(a) and (b). The results imply that the LNA is unconditionally stable from DC to 3 GHz. The overall results of the post-layout simulation are summarized in Table 7.1.



(a) Stability factor K



(b) Stability measure B

Figure 7.8: Determination of the stability conditions for the proposed LNA in post-layout simulation

Parameter	Value
Supply Voltage	1.5 V
Power Dissipation	29 mW
Operating Frequency	1.8 GHz
Power Gain	15.2 dB
Noise Figure	3.97 dB
NFmin	3.1 dB
Reverse Isolation	42.2 dB
Input Return Loss	30.7 dB
Output Return Loss	24 8dB
Input (Output) 1-dB compression point	-17.6 dBm (-3.83 dBm)
Input (Output) IP3	-8.6 dBm (6.45 dBm)

Table 7.1: Performance summary of the proposed LNA in post-layout simulation

7.5 Layout of the Common-Source Low Noise Amplifier

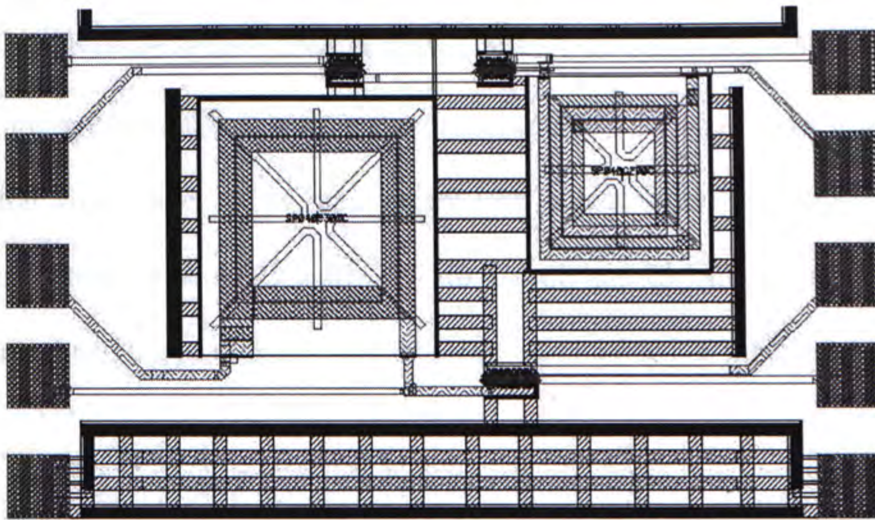
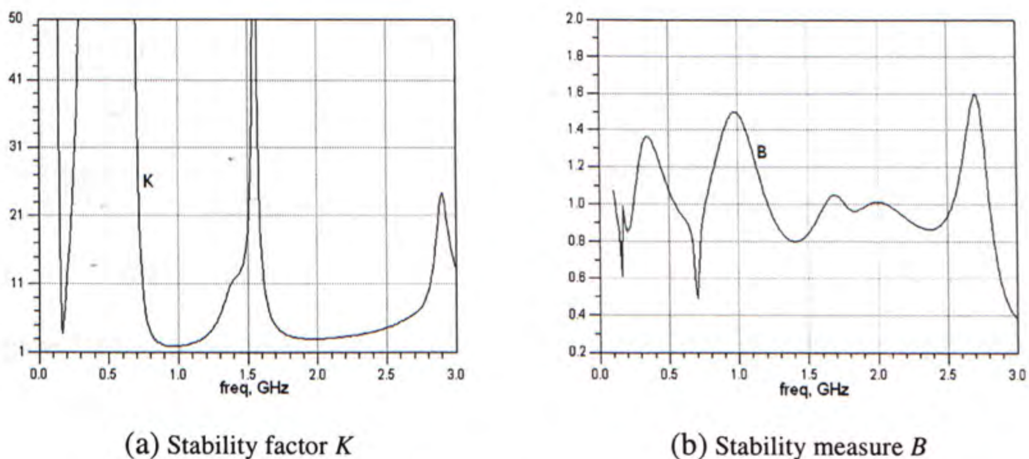


Figure 7.9: Layout design of the common-source LNA

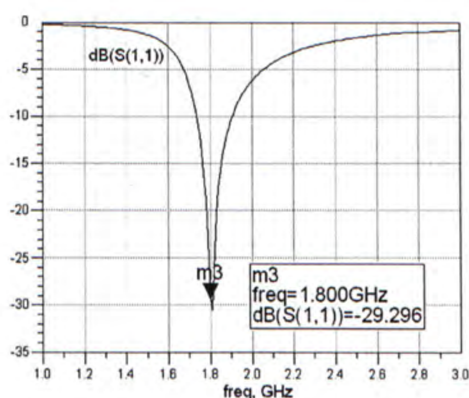
To evaluate the ESD protection of the proposed LNA, a common-source LNA is designed as a control. Figure 7.9 illustrates the layout of the common-source LNA. It is designed based on the schematic shown in Figure 6.6. It has only the transistors and the loading inductor, and no ESD protection circuitry. The active area is 560 μm x 900 μm.



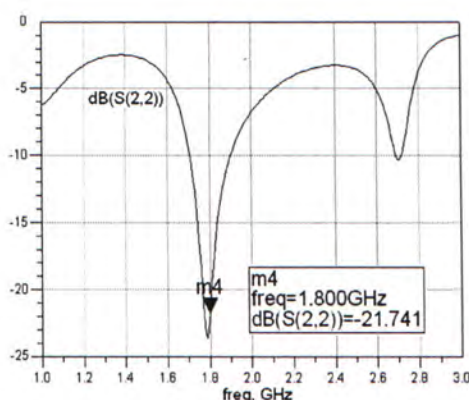
(a) Stability factor K (b) Stability measure B

Figure 7.10: Determination of the stability conditions for the common-source LNA in post-layout simulation

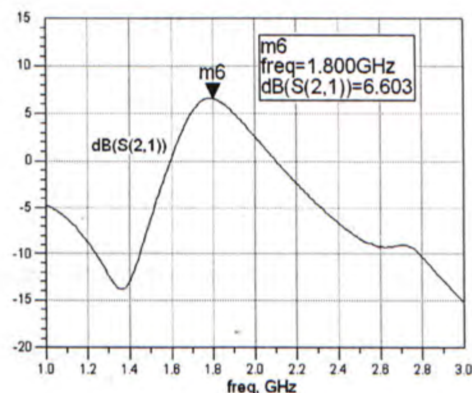
Figure 7.10(a) and (b) show K and B for the stability check of the common-source LNA operating at 1.2 V supply voltage. From the simulation results, the common-source LNA is proved to be unconditionally stable, because K and B are greater than 1 and positive, respectively. Figure 7.11 illustrates its simulation *S*-parameter. The input return loss, output return loss, power gain and reverse isolation are about 29.3 dB, 21.7 dB, 6.6 dB and 23.1 dB, respectively. The overall results of the post-layout simulation are summarized in Table 7.2.



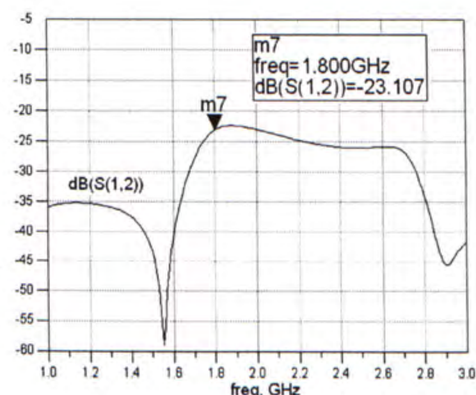
(a) Input return gain *S(1,1)*



(b) Output return gain *S(2,2)*



(c) Power gain *S(2,1)*



(d) Reverse gain *S(1,2)*

Figure 7.11: *S*-parameter of the common-source LNA in post-layout simulation

Parameter	Value
Supply Voltage	1.2 V
Power Dissipation	4.8 mW
Operating Frequency	1.8 GHz
Power Gain	6.6 dB
Noise Figure	1.94 dB
NFmin	1.89 dB
Reverse Isolation	23.1 dB
Input Return Loss	29.3 dB
Output Return Loss	21.7 dB
Input (Output) 1-dB compression point	-12.4 dBm (-6.95 dBm)
Input (Output) IP3	-2.85 dBm (3.42 dBm)

Table 7.2: Performance summary of the common-source LNA in post-layout simulation

7.6 Comparison between Schematic and Post-Layout Simulation Results

The overall results of the post-layout simulations for the two designed LNA agree with the schematic simulation results. There is only a little difference between them. It is partially due to the finite impedance of the interconnections between the components. Moreover, the parasitic substrate capacitors extracted from the layout circuits increase the power loss through the substrate.

Chapter 8

Measurement Results

In this chapter, the experiments of the proposed ESD-protested LNA and the conventional common-source LNA fabricated in this research project are described. The experimental setups are illustrated first, and then the measurement results are reported. The experimental contents include the measurements of the standard LNA performance parameters, which are:

a) *S*-parameter;

b) Noise figure

c) 1-dB compression point;

d) Third-order intercept point (IP3).

Besides, the measurement of the HBM ESD withstand voltage is presented. It is the most important results for this project.

8.1 Experimental Setup

Before the measurements of the testing circuit are carried out, the evaluation boards and the experimental setups should be prepared. In this section, the overview of the circuit board and the necessary setups are described.

8.1.1 Testing Circuit Board

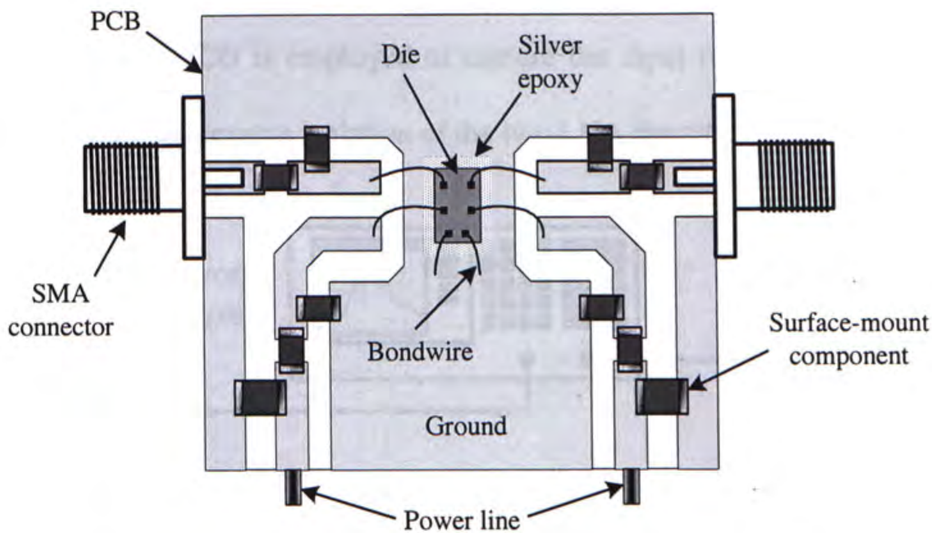


Figure 8.1: A testing circuit board for measurement

In RF measurement, CMOS circuit is always tested without package. The reason is due to the large parasitic capacitances and inductances generated from the package that will degrade the circuit performance. Figure 8.1 illustrates a typical testing circuit board prepared for CMOS RF measurement. The testing die shown in the figure is mounted on the printed circuit board (PCB) with silver epoxy. Bondwires are used to connect the bonding pads to the copper tracks so that the necessary signals can enter the die through the PCB. There are also other peripheral components soldered on the PCB. The surface-mount components are placed for matching and biasing. The power lines which are connected to the DC supplies for providing the biasing signals. Furthermore, SMA connectors are used to connect the input and output ports to external instrument for measurement.

8.1.2 Experimental Setup for *S*-parameter

Figure 8.2 shows the *S*-parameter measurement setup. A network analyzer *ADVANTEST R3767CG* is employed to capture the input return loss, output return loss, power gain and reverse isolation of the two LNA circuits.

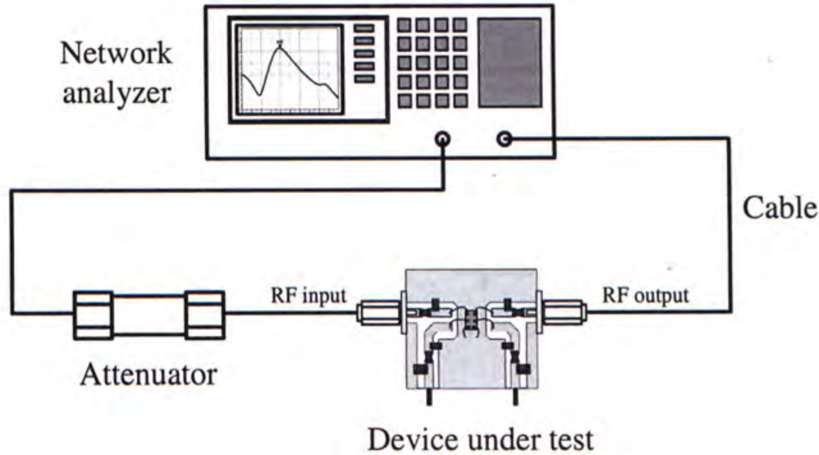


Figure 8.2: The setup for the *S*-parameter measurement

It is observed from the figure that an attenuator is added in this setup. Its function is to reduce the input power level before entering to the testing LNA. If the input power level is too high, the testing LNA will be saturated. The gain compression will occur in this case and the measurement data may be distorted.

Before the measurement is carried out, we need to calibrate the network analyzer and the attenuator together. It can eliminate the impedance of the attenuator which may affect the measurement results.

8.1.3 Experimental Setup for Noise Figure

Figure 8.3 shows the noise figure experimental setup. The setup is composed of a noise figure meter *HP 8970B* and a standard 50-Ω noise source *HP 346B*. The noise source generates a reference noise input to the LNA, which is measured by the noise meter at a particular frequency. To increase the accuracy of the measurement

and reduce the background interference, the experiment can be carried out in an EMC chamber. Moreover, the setup is required to calibrate before the measurement so as to eliminate the noise contributed from the coaxial cable.

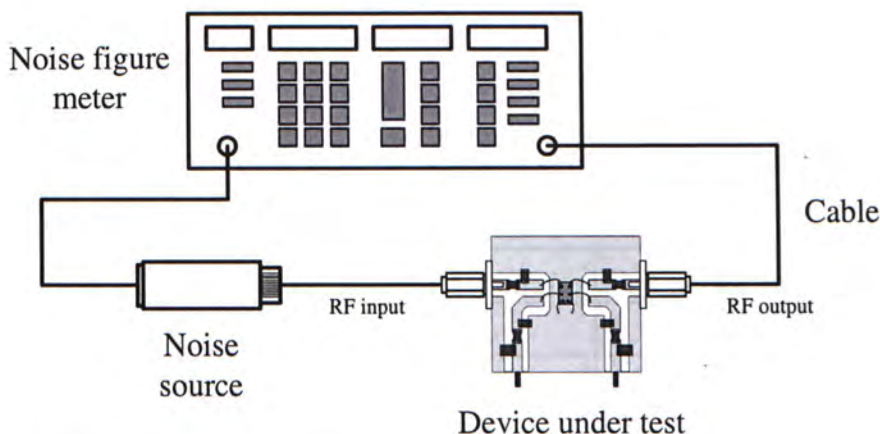


Figure 8.3: The setup for the noise figure measurement

8.1.4 Experimental Setup for 1-dB Compression Point

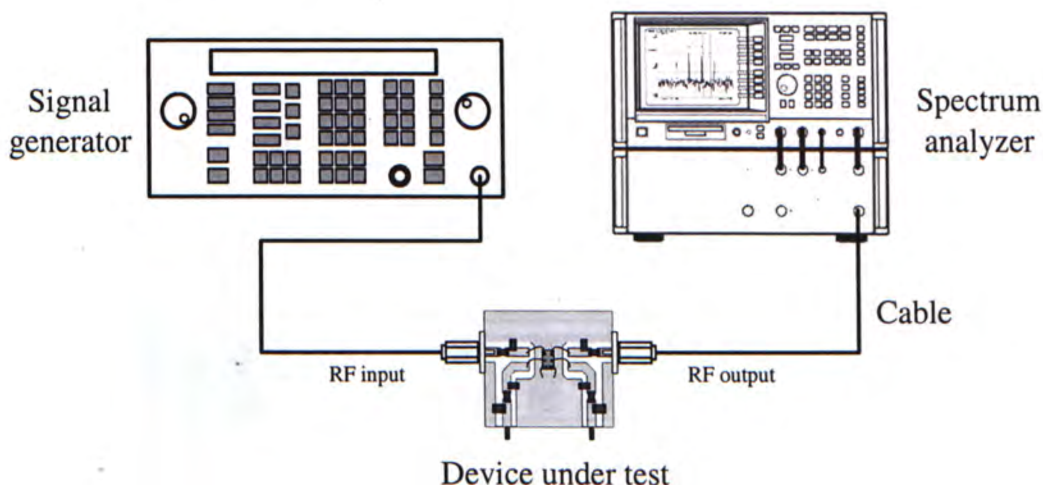


Figure 8.4: The setup for the measurement of the 1-dB compression point

The setup illustrated in Figure 8.4 is used in the 1-dB compression point measurement. In this test, a signal generator *HP 8648C* provides a single tone to the device under test and the output signal power is measured by a spectrum analyzer

HP 8546A with EMI receiver. Figure 8.5 shows the output spectrum captured from the spectrum analyzer in this test. By collecting the data of the output power levels for different input power levels, the 1-dB compression point of the device can be determined.

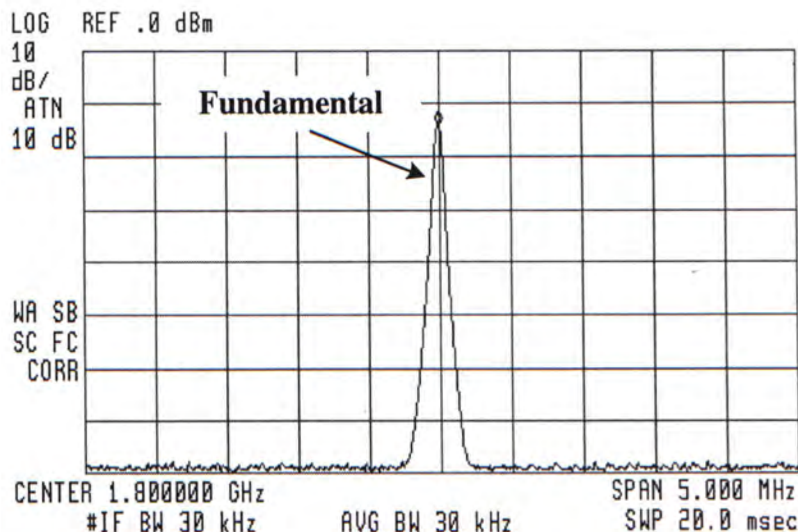


Figure 8.5: The output spectrum captured in the measurement of the 1-dB compression point

8.1.5 Experimental Setup for Third-Order Intercept Point

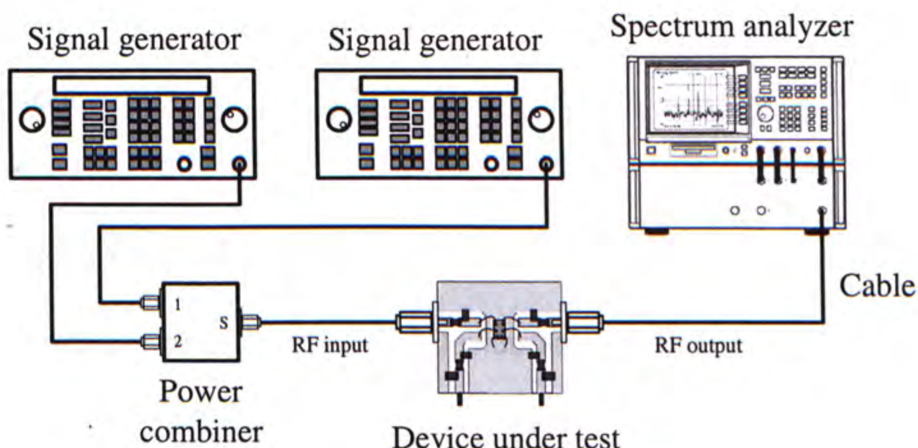


Figure 8.6: The setup for the two-tone linearity measurement

In the measurement of the third-order intercept point (IP3), a two-tone test is

performed. The experimental setup is illustrated in Figure 8.6. The two signal generators *HP 8648C* and a $2-\text{way}\ 0^{\circ}$ power combiner *Mini-circuits ZN2PD-1900* are connected to provide a two-tone signal. This signal is injected to the testing LNA and the power levels of the output fundamentals and the third-order IM products are measured by the spectrum analyzer *HP 8546A* with EMI receiver. Figure 8.7 shows the output spectrum in the two-tone test for IP3 measurement.

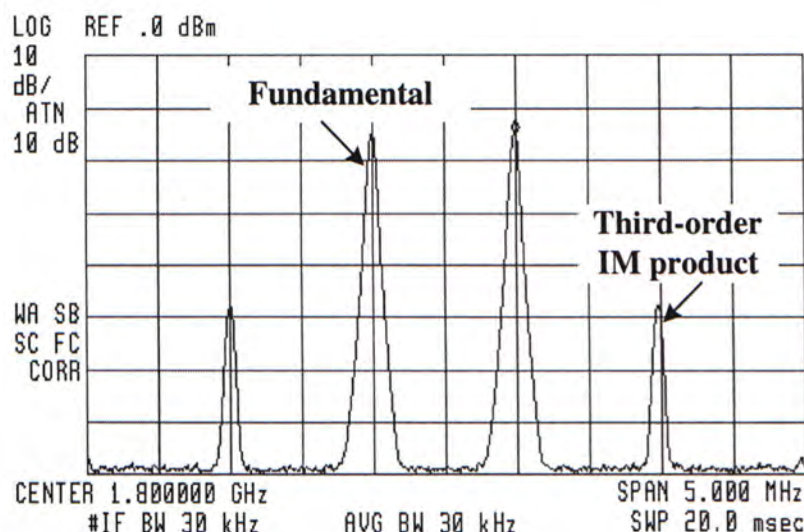


Figure 8.7: The output spectrum captured in the two-tone linearity measurement

By changing the input two-tone power and the corresponding output powers of the fundamentals and third-order IM products are measured, IP3 of the testing LNA can be determined.

8.1.6 Setup for HBM ESD Test

In the measurement of the HBM ESD withstand voltages, the standard test setup according to ESD Association standard [2] illustrated in Figure 8.8 is used. In this experiment, the circuit can be tested with package. It is because the ESD frequency is relatively low compared with the radio frequency. A KeyTek Zap Master is used

to measure the HBM ESD withstand voltages. This tester can be controlled with the software installed in the computer. The end-user can carry out a variety of functions such as the assignment of a particular voltage to each pin, the selection of the testing pin and the device checking through this software.

During the testing, the switch SW1 is opened and the ESD pulse of a particular voltage is injected to the RF input port of the testing LNA. After the injection, SW1 is closed for 10 to 100 milliseconds to discharge the LNA through the 10-kΩ resistor. Then, the LNA is checked with its I-V characteristic to see whether it is damaged or not. We can determine the HBM ESD withstand voltage by slowly increasing the ESD voltage until the device is destroyed.

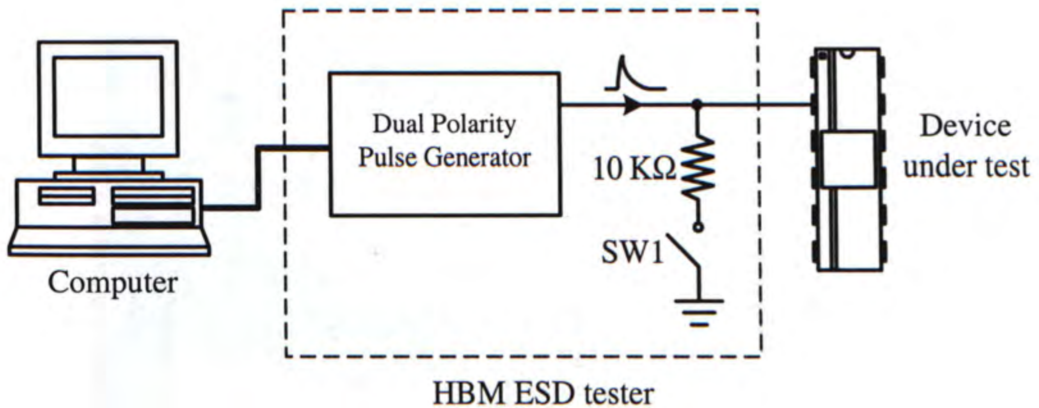


Figure 8.8: The setup for the HBM ESD test

8.2 Measurement Results of the Proposed Low Noise Amplifier

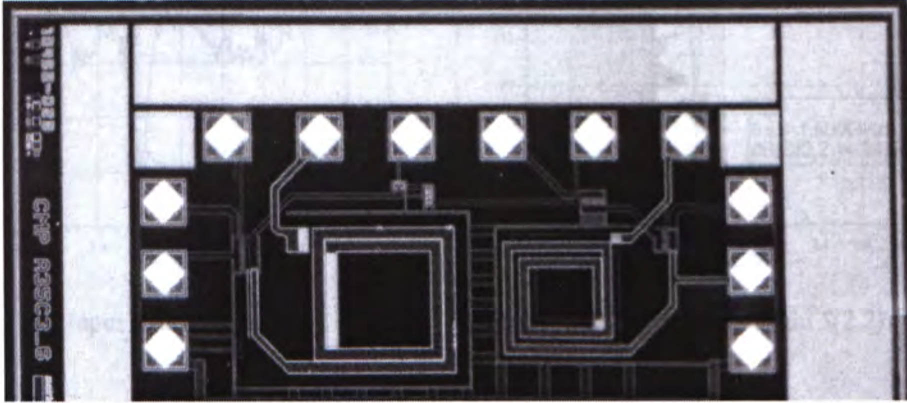


Figure 8.9: A microphotograph of the proposed LNA

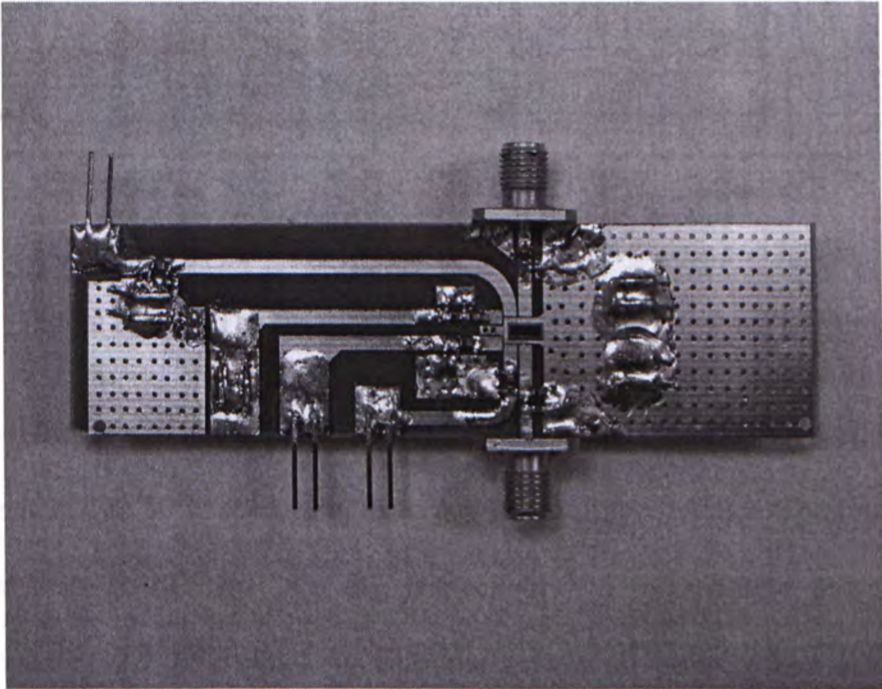
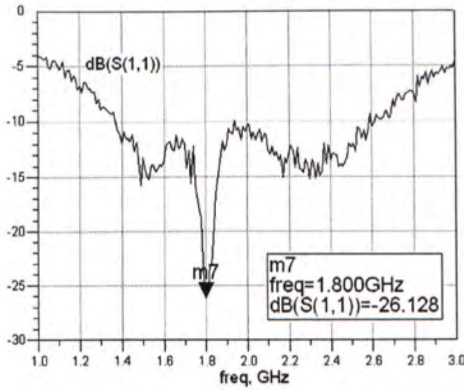


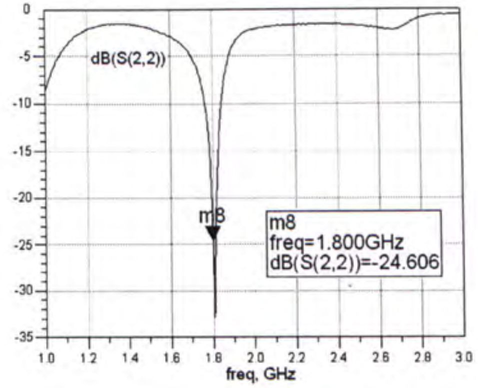
Figure 8.10: An evaluation board of the proposed LNA

Figure 8.9 and 8.10 depict the microphotograph and the evaluation board of the proposed 1.8 GHz ESD-protected LNA prepared for the measurement, respectively. The circuit is powered by 1.5 V and the measured power consumption is 29 mW.

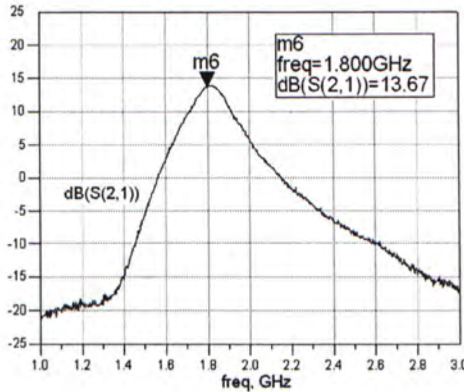
8.2.1 *S*-parameter Measurement



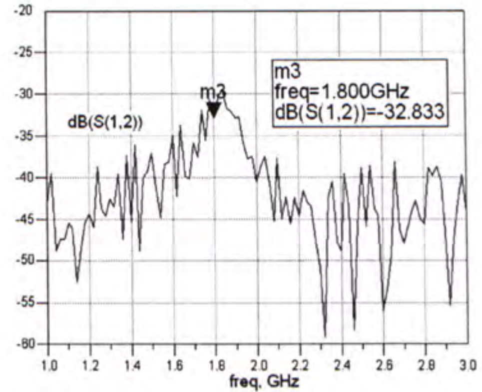
(a) Input return gain *S(1,1)*



(b) Output return gain *S(2,2)*



(c) Power gain *S(2,1)*



(d) Reverse gain *S(1,2)*

Figure 8.11: The measured *S*-parameter of the proposed LNA

From the measurement results of the *S*-parameter at 1.8 GHz, the proposed LNA is well matched to 50 Ω at both its input and output impedances. The return losses are more than 26 dB and 24.6 dB, respectively. The measured power gain is approximately 13.7 dB, which is near the maximum point. The *S(2,1)* curve shows a good agreement with the post-layout simulation result given in Figure 7.7(c). The measured reverse isolation is about 32.8 dB, which is sufficient to prevent the output signal from reflected back to the input port.

8.2.2 Noise Figure Measurement

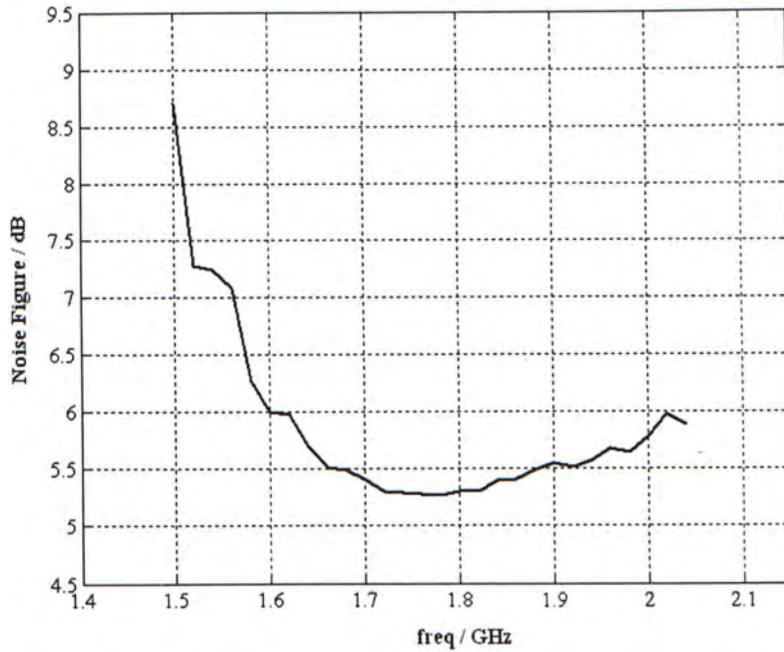


Figure 8.12: The measured noise figure of the proposed LNA

Figure 8.12 shows the measurement result of the noise figure. The minimum value of the noise figure of the proposed LNA appears at 1.8 GHz, which is 5.3 dB. It is higher than the 3.97 dB simulated noise figure. The difference may be due to:

1. the noise contributed from the PCB and the external components;
2. the noise generated from the bonding pads;
3. the substrate noise coupling effect;
4. inadequate modeling of the transistor noise in the simulator.

8.2.3 Measurement of 1-dB Compression Point

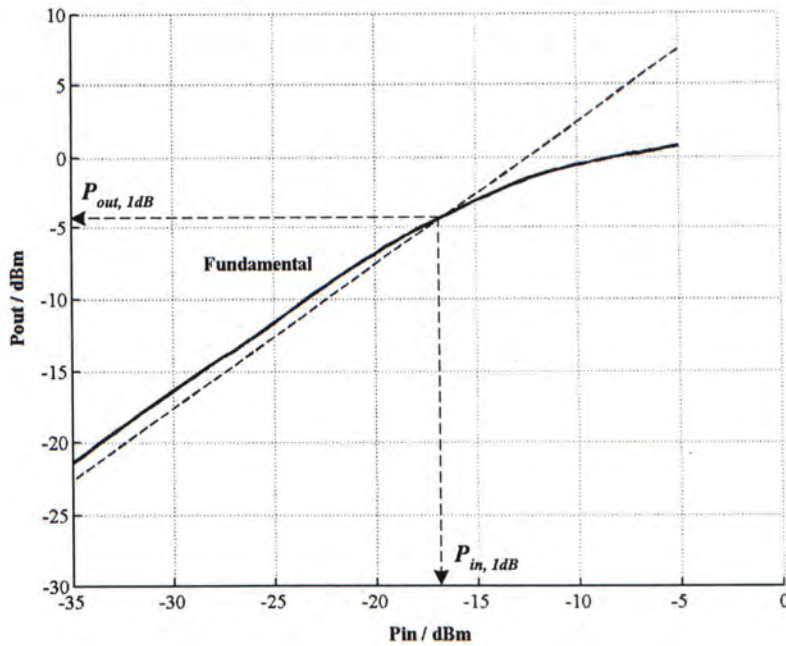


Figure 8.13: The measured $P_{in,1dB}$ and $P_{out,1dB}$ of the proposed LNA

In the measurement of the power handling capability, the frequency of the single-tone signal injected to the proposed LNA is 1.8 GHz. The range of the input power is from -35 dBm to -5 dBm. The measurement results are plotted in Figure 8.13. From the relationship of the input and output power levels of the LNA, it is found that the input power at the 1-dB compression point $P_{in,1dB}$ is approximately -16.6 dBm, and the corresponding output power $P_{out,1dB}$ is about -4.2 dBm.

8.2.4 Measurement of Third-Order Intercept Point

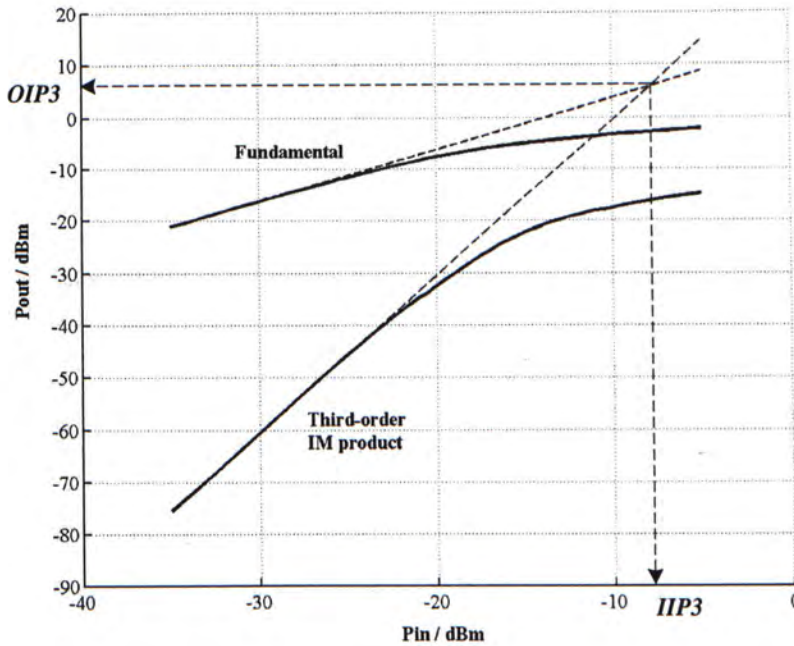
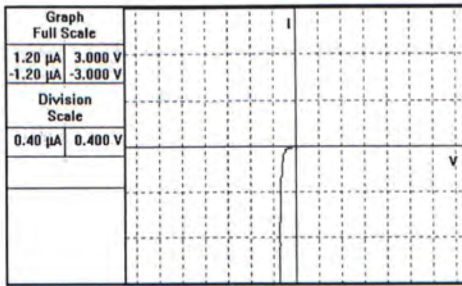


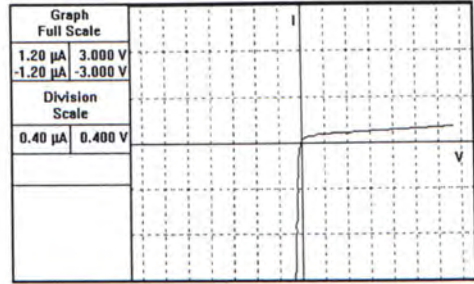
Figure 8.14: The two-tone testing results of the proposed LNA

In the two-tone test for the linearity measurement, the two-tone signals injected to the proposed LNA are at 1.7995 GHz and 1.8005 GHz. Their input power levels are the same and swept from -35 dBm to -5 dBm. The relationship of the input and output power levels for the fundamental components and third-order IM products are plotted in Figure 8.14. From the measurement results shown in the figure, IIP3 and OIP3 are approximately -7.8 dBm and 6 dBm, respectively.

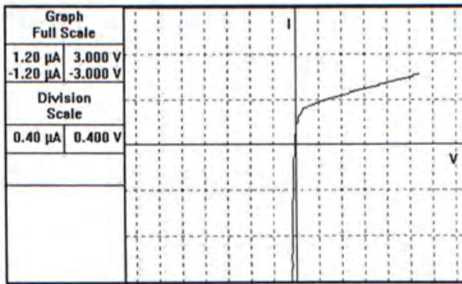
8.2.5 HBM ESD Test



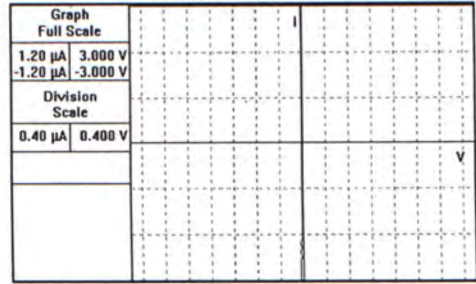
(a) Before the HBM ESD pulse injected



(b) After a -3.6 kV HBM ESD pulse injected



(c) After a -4 kV HBM ESD pulse injected



(d) After a -5.3 kV HBM ESD pulse injected

Figure 8.15: The I-V characteristic curves measured at the RF input of the proposed LNA in the negative HBM ESD test

For the HBM ESD test, Figure 8.15 shows the negative HBM ESD testing results, which is composed of the four I-V characteristic curves measured at the RF input of the proposed LNA before and after the HBM ESD pulses with different voltages are injected to it. Since there is a pn junction at the source terminal (see Figure 3.6), the I-V characteristic at the RF input is similar to that of a diode at normal condition, as shown in Figure 8.15(a). There is no significant change observed after a weak ESD pulse injection. However, the curve starts deviating after the -3.6 kV HBM ESD pulse is injected, as shown in Figure 8.15(b). Furthermore, the deviation increases with the strength of the ESD pulse. Finally, the pn junction at the RF input is broken down after the -5.3 kV HBM ESD pulse is injected. A short-circuit I-V characteristic curve is obtained, as illustrated Figure

8.15(d). Therefore, the negative HBM ESD withstand voltage is -3.5 kV.

Table 8.1 lists out the overall measurement results of the HBM ESD test for the proposed LNA. These results are the typical values measured from 8 testing samples. The minimum step resolution of the tests is 50 V.

Negative HBM ESD withstand voltage	-3.5 kV
Positive HBM ESD withstand voltage	1.5 kV

Table 8.1: The measurement results of the HBM ESD test for the proposed LNA

8.2.6 Summary of Measurement Results

Parameter	Measured value
Supply Voltage	1.5 V
Power Dissipation	29 mW
Operating Frequency	1.8 GHz
Power Gain	13.7 dB
Noise Figure	5.3 dB
Reverse Isolation	32.8 dB
Input Return Loss	26 dB
Output Return Loss	24.6 dB
Input (Output) 1-dB compression point	-16.6 dBm (-4.2 dBm)
Input (Output) IP3	-7.8 dBm (6 dBm)
Negative HBM ESD withstand voltage	-3.5 kV
Positive HBM ESD withstand voltage	1.5 kV

Table 8.2: Performance summary of the proposed LNA

8.3 Measurement Results of the Common-Source Low Noise Amplifier

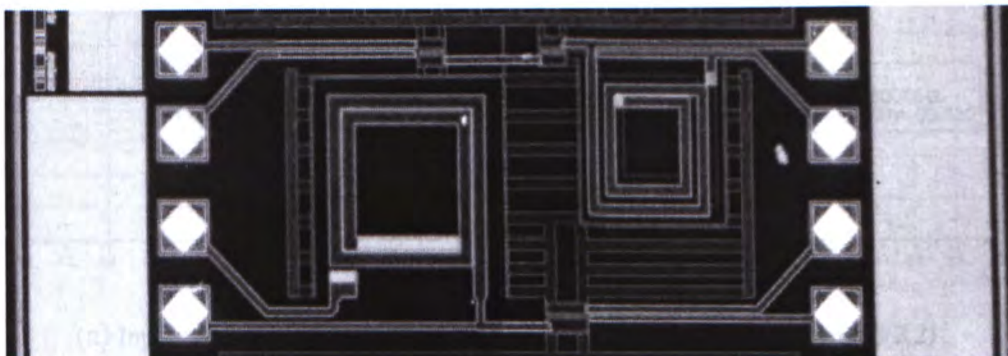


Figure 8.16: A microphotograph of the common-source LNA

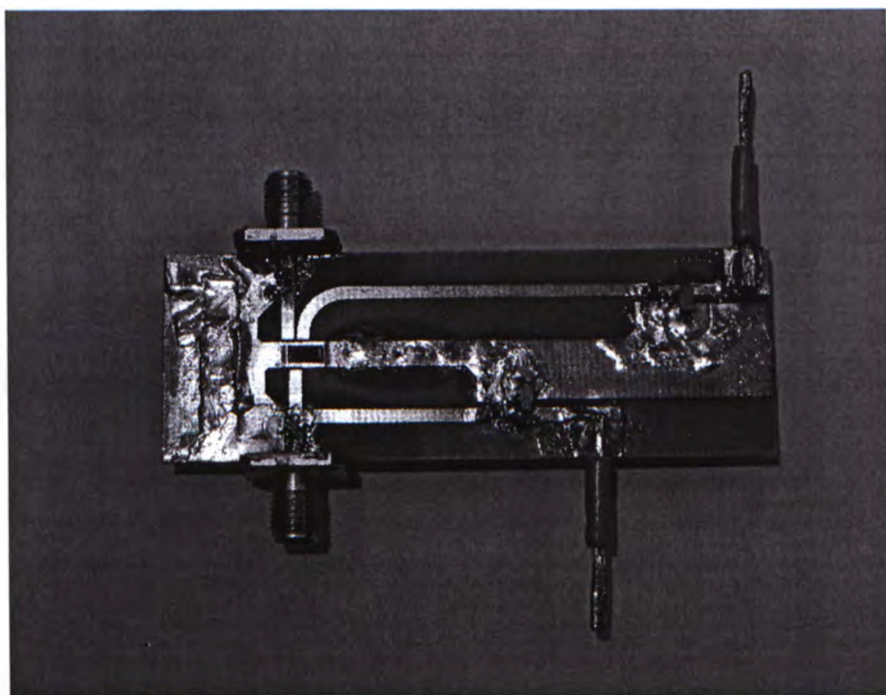
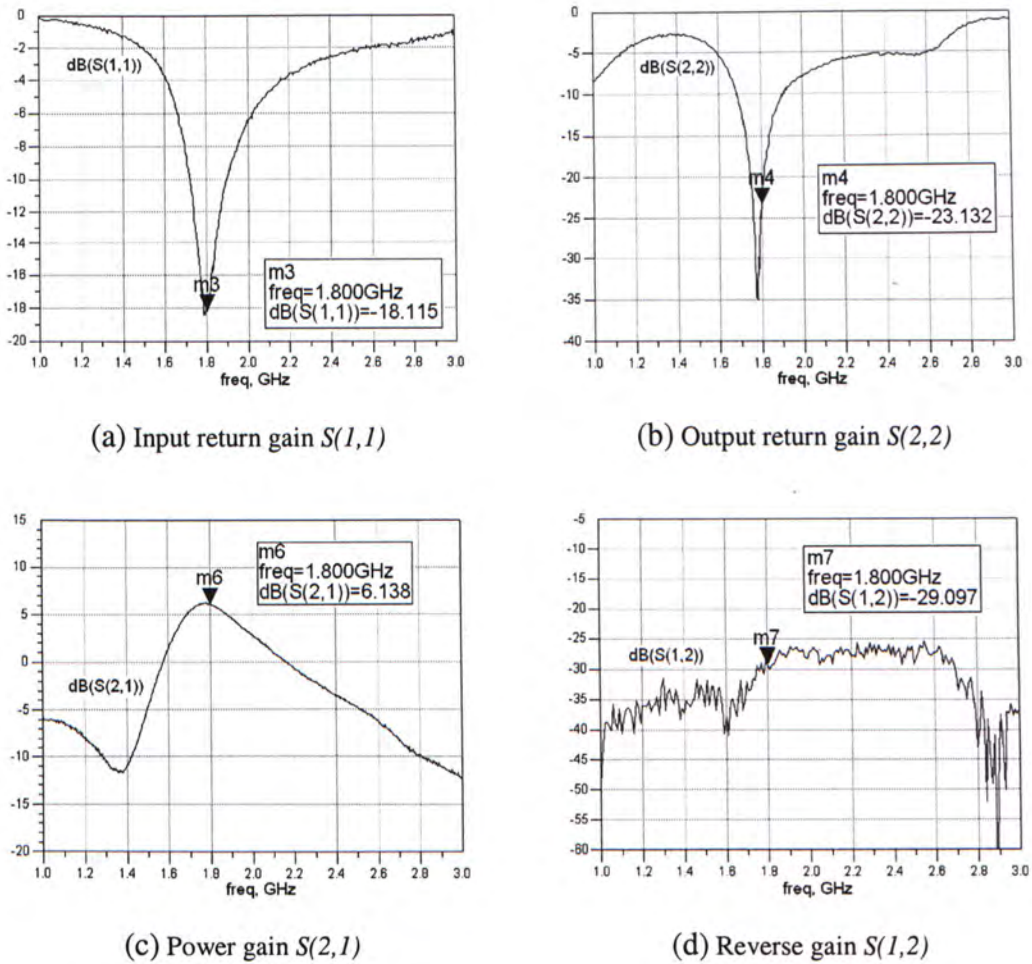


Figure 8.17: An evaluation board of the common-source LNA

Figure 8.16 and 8.17 depict the microphotograph and the evaluation board of the 1.8 GHz common-source LNA prepared for the ESD control experiment, respectively. The supply voltage is 1.2 V and the measured power consumption is 5 mW.

8.3.1 *S*-parameter Measurement



(a) Input return gain *S(1,1)*

(b) Output return gain *S(2,2)*

(c) Power gain *S(2,1)*

(d) Reverse gain *S(1,2)*

Figure 8.18: The measured *S*-parameter of the common-source LNA

In the *S*-parameter measurement as illustrated in Figure 8.18, the measured input and output return losses of the common-source LNA are approximately 18.1 dB and 23.1 dB at 1.8 GHz, respectively. It implies that the input and output impedances are well matched to 50 Ω. The measured power gain is more than 6.1 dB, which agrees with the simulation result shown in Figure 7.11(c). The measured reverse isolation is about 29.1 dB, which is sufficient to prevent the output signal from reflected back to the input port.

8.3.2 Noise Figure Measurement

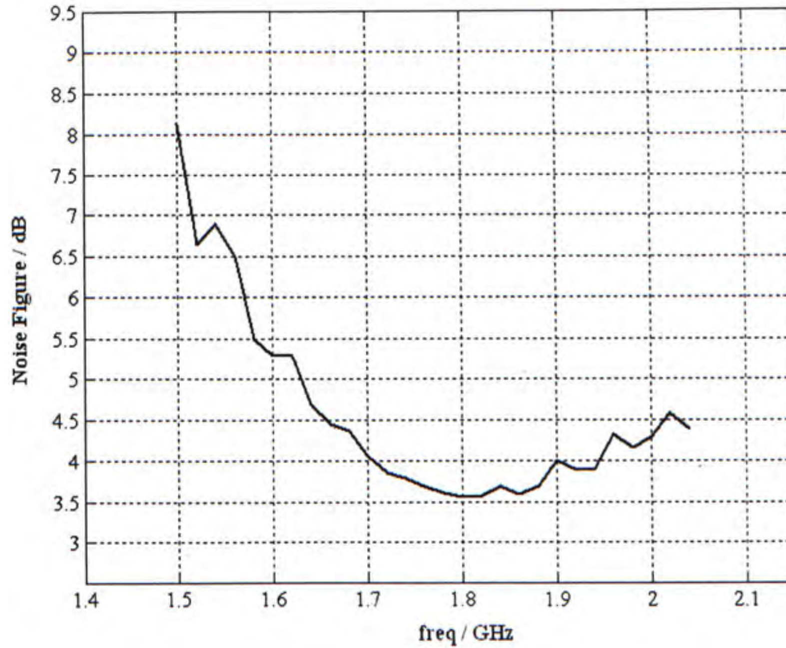


Figure 8.19: The measured noise figure of the common-source LNA

Figure 8.19 shows the measurement result of the noise figure. It is observed that the common-source LNA achieves the noise figure of 3.6 dB at 1.8 GHz, which is the minimum value over the frequency from 1.4 GHz to 2.04 GHz. By comparing with the proposed LNA, the noise figure of the common-source LNA is smaller. It is because the common-source LNA is only a single-stage amplifier, while the proposed LNA is a two-stage amplifier. The increase in the number of cascading stages will increase the total noise figure of the multistage amplifier, based on Friis formula. However, there is also a significant difference between the measured value and the corresponding simulation value given in Table 7.2. It may attribute to the noise coupled from the substrate, bonding pads and external components. The inaccurate noise model of the transistor in the simulator is also the possible reason that causes the difference.

8.3.3 Measurement of 1-dB Compression Point

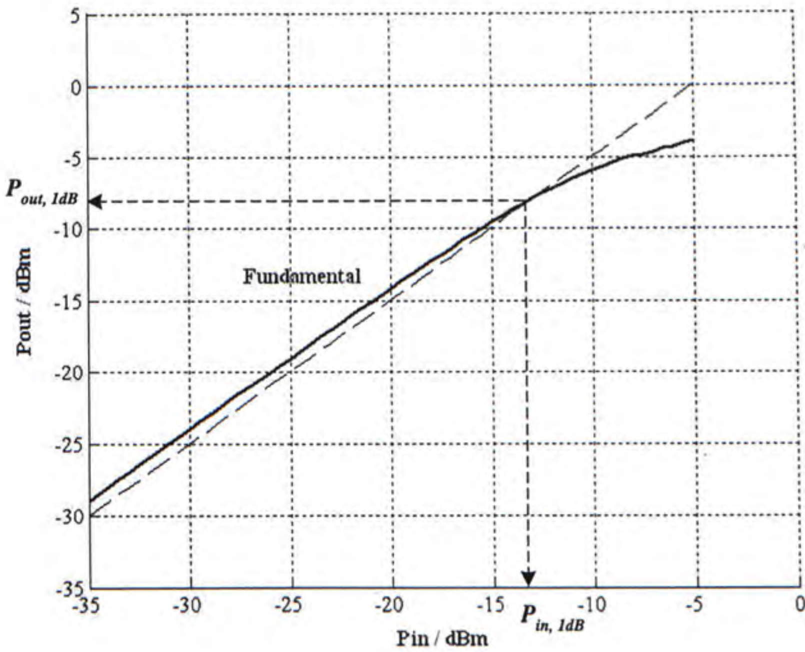


Figure 8.20: The measured $P_{in,1dB}$ and $P_{out,1dB}$ of the common-source LNA

In the measurement of the 1-dB compression point, the frequency of the single-tone signal injected to the common-source LNA is 1.8 GHz. The input power is swept from -35 dBm to -5 dBm. The measurement results are plotted in Figure 8.20. In the graph of the measured output power against the input power of the LNA, it is found that the input power at the 1-dB compression point $P_{in,1dB}$ is -12.9 dBm, and the corresponding output power $P_{out,1dB}$ is -7.8 dBm.

8.3.4 Measurement of Third-Order Intercept Point

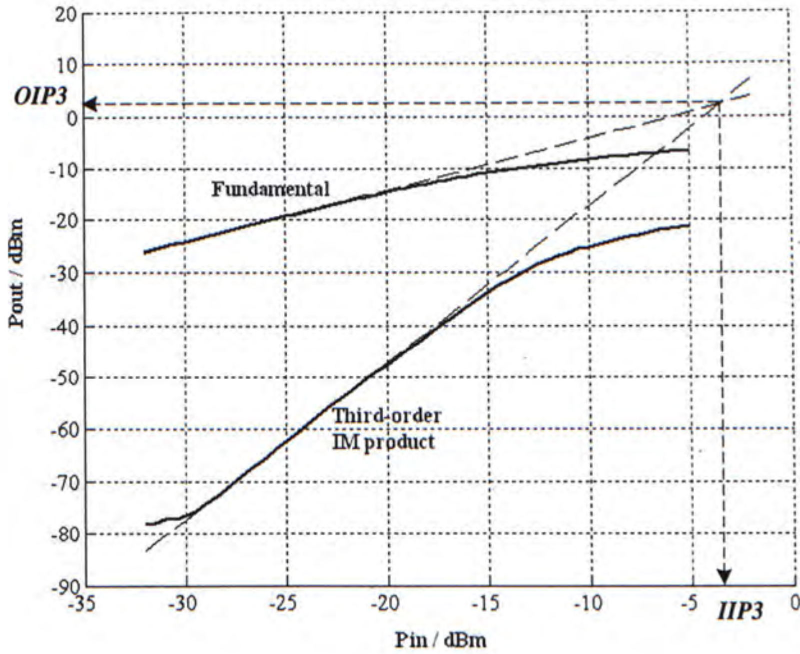
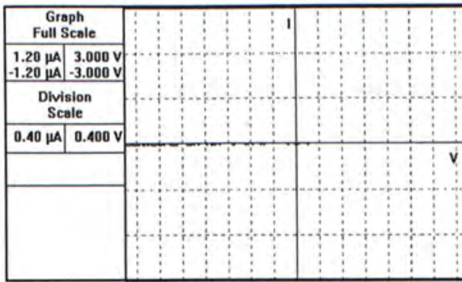


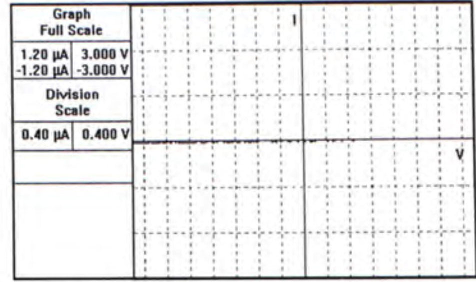
Figure 8.21: The two-tone testing results of the common-source LNA

In the two-tone test for the linearity measurement, the two-tone signals injected to the common-source LNA are the same power levels at 1.7995 GHz and 1.8005 GHz, respectively. The input power range is from -32 dBm to -5 dBm. The relationship of the input and output power levels for the fundamental components and third-order IM products are plotted in Figure 8.21. From the measurement results shown in the figure, IIP3 and OIP3 are approximately -3.5 dBm and 2.3 dBm, respectively.

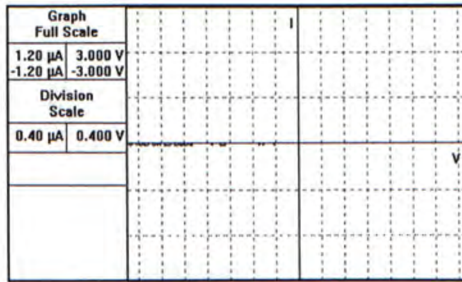
8.3.5 HBM ESD Test



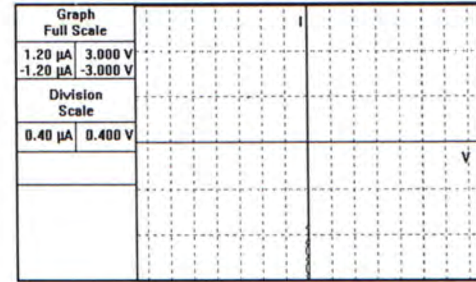
(a) Before the HBM ESD pulse injected



(b) After a 100 V HBM ESD pulse injected



(c) After a 200 V HBM ESD pulse injected



(d) After a 250 V HBM ESD pulse injected

Figure 8.22: The I-V characteristic curves measured at the RF input of the common-source LNA in the positive HBM ESD test

For the HBM ESD test, the four I-V characteristic curves measured at the RF input of the common-source LNA for the positive HBM ESD pulses are illustrated in Figure 8.22. Since the RF input is the transistor gate terminal, an open-circuit I-V characteristic curve is obtained before the ESD injection, as illustrated in Figure 8.22(a). When the strength of the HBM ESD pulse is not higher than 200 V, the I-V characteristic curve remains unchanged after the ESD injection. However, after the 250 V HBM ESD pulse injected, a short-circuit I-V characteristic curve is observed in Figure 8.22(d). It indicates that the gate oxide breakdown happens. Therefore, the positive HBM ESD withstand voltage is 200 V

Table 8.3 lists out the overall measurement results of the HBM ESD test for the common-source LNA. These results are the typical values measured from 8 testing

samples. The minimum step resolution of the tests is 50 V.

Negative HBM ESD withstand voltage	-200 V
Positive HBM ESD withstand voltage	200 V

Table 8.3: The measurement results of the HBM ESD test for the common-source LNA

By comparing with the results in Table 8.1, the achievements of the proposed LNA are greater that of the common-source LNA. These results show that CGISM can effectively increase the ESD immunity of the LNA.

8.3.6 Summary of Measurement Results

Parameter	Measured value
Supply Voltage	1.2 V
Power Dissipation	5 mW
Operating Frequency	1.8 GHz
Power Gain	6.1 dB
Noise Figure	3.6 dB
Reverse Isolation	29.1 dB
Input Return Loss	18.1 dB
Output Return Loss	23.1 dB
Input (Output) 1-dB compression point	-12.9 dBm (-7.8 dBm)
Input (Output) IP3	-3.5 dBm (2.3 dBm)
Negative HBM ESD withstand voltage	-200 V
Positive HBM ESD withstand voltages	200 V

Table 8.4: Performance summary of the common-source LNA

8.4 Performance Comparison between Different Low Noise Amplifier Designs

Parameter	Proposed LNA	3-Stage Common-Gate LNA [25]	2-Stage Common-Source LNA [40]
Supply Voltage	1.5 V	1.5 V	3.6 V
Power Dissipation	29 mW	24 mW	54 mW
Operating Frequency	1.8 GHz	24 GHz	1.9 GHz
Power Gain	13.7 dB	22 dB	15 dB
Noise Figure	5.3 dB	6 dB	2.8 dB
Input IP3	-7.8 dBm	-	2 dBm

Table 8.5: Performance comparison between published LNA designs and the proposed LNA

Table 8.5 shows a comparison of the performance between the proposed LNA in this research project and the two published LNA designs. Referring to this table, the 2-stage common-source LNA has the excellent noise figure and sufficient power gain. However, it requires high supply voltage and has the highest power dissipation. Although the 3-stage common-gate provides the best power gain among the three LNA designs, its noise figure is quite high and the circuit is bulky. In contrast, the proposed LNA can achieve the average value in each performance parameter. It implies that the proposed LNA provides comparable performance as conventional designs.

Parameter	Proposed LNA	LNA specifications in DECT System [15]
Operating Frequency	1.8 GHz	1.88 GHz – 1.897 GHz
Power Gain	13.7 dB	12 dB
Noise Figure	5.3 dB	5 dB
Input IP3	-7.8 dBm	-10 dBm

Table 8.6: Performance comparison between the proposed LNA and the standard LNA specifications

By comparing the performance of the proposed LNA with the standard LNA specifications from DECT system as listed in Table 8.6, their parameter values are very close. This shows that the design of the proposed LNA meets the standard LNA specifications.

Chapter 9

Conclusion and Future Work

9.1 Conclusion

The design and implementation of a new ESD-protected method, called CGISM, in a LNA is developed in this thesis. CGISM utilizes a common-gate amplifier as the input stage of the LNA. The RF input is directly connected to the source of the transistor, instead of the gate. It will provide higher ESD protection than conventional common-source LNA by preventing the ESD current from discharging through the thin gate oxide. Moreover, the method does not give any degradation to the LNA performance. It is because there is no extra ESD-protection circuitry required in the LNA design.

Two LNA circuits have been fabricated and tested. The first circuit is a 1.8 GHz ESD-protected LNA with the proposed CGISM. It is operating at low supply voltage of 1.5 V with a power consumption of 29 mW. In the HBM ESD test, it is capable of surviving positive ESD pulse up to 1.5 kV and negative ESD pulse down to –3.5 kV. These results show the ESD protection capability of CGISM. The proposed LNA can achieve the power gain of 13.7 dB, the noise figure of 5.3 dB, the input-referred 1-dB compression point of -16.6 dBm and IIP3 of -7.8 dBm.

The second circuit is a 1.8 GHz common-source LNA. It acts as a control experiment in the ESD test. The LNA is operating at 1.2 V with a power

consumption of 5 mW. In the HBM ESD test, the measured results are +/-200 V. By comparing with the proposed LNA, it indicates that CGISM can substantially improve the ESD immunity of LNA. It can achieve the power gain of 6.1 dB, the noise figure of 3.6 dB, the input-referred 1-dB compression point of -12.9 dBm and IIP3 of -3.5 dBm.

In the comparison of the simulation and measurement results, they show a good agreement with each other in both the two designed LNA circuits, except the noise figures. The measured noise figures are obviously higher than their simulation results. It may be due to the noise contributed from the PCB, surface-mount components, bonding pads and substrate coupling effect. The inadequate modeling of the transistor noise in the simulator is also the possible reason for this deviation.

9.2 Future Work

In this thesis, it is observed that the positive HBM ESD withstand voltage of the proposed LNA is lower than its negative one. For future work, the reason for this difference should be found out, so as to modify the LNA and increase the overall ESD handling capability. Moreover, it is recommended to design the LNA with a lower supply voltage of 1 V.

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