An IF Input Continuous-time Sigma-delta Analog-digital Converter with High Image Rejection

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Abstract

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Highly integrated wireless receiver has long been a research focus for its low cost and compactness. Traditional receiver usually employs external filters to help achieve high signal to noise ratio, image rejection ratio, etc. If the internal analog to digital converter (ADC) of a receiver can handle large dynamic range signals as well as suppress much stronger image signals, the ADC can move closer to the antenna by removing some external components like filter, etc.

This work mainly aims at improving the Image Rejection (IR) of the Intermediate Frequency (IF) input quadrature ADC, which is widely adopted in receivers for its intrinsic image rejection property. Continuous time (CT) sigma delta ($\Sigma\Delta$) technique is adopted to implement the ADC for its high resolution, high tolerance to analog components' nonidealities and inherent antialiasing filtering, etc. Integrated In-phase (I) and Quadrature-phase (Q) mixer are employed to down-convert the IF input signal to baseband, thus a baseband instead of bandpass sigma delta modulator is entailed, which is more power efficient.

A novel resistor time-sharing technique is proposed to achieve higher image rejection in this work. Furthermore, new effective zero order hold instead of impulse invariant transformation is applied to transform a discrete time loop filter transfer function into a continuous time one. A third order CT ΣΔ modulator with current feedforward compensation is thus built up. An original current input comparator as well as a digital clock tree with phase fine-tuning ability for generating accurate LO signals are designed. Novel signal scaling approach of the ΣΔ modulator is presented to scale up or down the internal signal swings. Finally, biasing circuit and wide output swing OTA in ΣΔ modulator are carefully studied and several original methods are brought forward to achieve robust performance.

This design deals with signal with 200KHz bandwidth. The Oversampling Ratio (OSR) of ΣΔ modulator is 128. It is implemented in a 0.35um double-poly quadruple layer metal CMOS technology. The active area is $1mm^2$ and the power consumption is 14.8mW from a 3.3V supply. Postlayout simulation with 25MHz IF and 50KHz offset frequency shows that no image signal is present for 4096 sampled output points, the corresponding IR ratio and SNDR are 69dB and 61dB respectively.

摘要

高集成度接收機因爲其低成本和緊湊性成爲長期以來的研究焦點。傳統接收機通常採用外置濾波器來幫助獲得高信噪比，象頻抑制比等等。如果接收機內部的類比數位轉換器能處理大動態範圍信號和抑制強象頻信號，一些外置器件比如濾波器等就可以移除，從而使得類比數位轉換器可以更靠近接收天線。

這篇論文主要目標是進一步提高中頻輸入的、被廣泛採用的具有象頻抑制特性的正交類比數位轉換器的象頻抑制比。連續時間 ΣΔ 技術因爲它的高解析度，對模擬元件非理想特性的高容忍性，以及固有的抗混疊濾波等而被採用來做類比數位轉換器。集成的同相和正交相混頻器被用作降頻轉換中頻輸入信號到基帶，這樣能量利用更高效的低通 ΣΔ 調節器而不是帶通 ΣΔ 調節器是必需的。

在這篇論文中，爲了獲得更高的象頻抑制，一種嶄新的電阻時間共用技術被提出。此外，新的有效的零階保持方法取代脈衝不變轉換被應用在轉換離散時間環路濾波傳輸方程到相應的連續時間傳輸方程。一個採用電流前饋補償的三階連續時間 ΣΔ 調節器被設計完成。一個原創的電流輸入比較器和一個用來輸出精確本振信號且具有相位精密調控能力的數位時鐘樹也已被設計。新的 ΣΔ 調節器的信號縮放方法被提出來縮放內部信號的擺幅。最後，ΣΔ 調節器裏的偏置電路和大輸出擺幅的誇導運算放大器被仔細研究且幾種原創的方法被提出來以獲得穩定的工作性能。

這個設計用於處理 200KHz 的信號帶寬。ΣΔ 調節器的過採樣率是 128。它採用 0.35um 雙層多晶矽四層金屬互補金屬氧化物半導體工藝。晶片有效面積是 $1mm^2$，在 3.3V 電源供應下，功耗是 14.8mW。在 25MHz 中頻 50KHz 偏置頻率輸入的情況下，後版圖類比輸出的 4096 採樣點顯示象頻信號不再存在，相應的象頻抑制比和信噪比分別是 69dB 和 61dB.

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1. Chapter 1

Introduction

1.1. Overview

During the last century, wireless communications have been developed extensively and have accelerated the advancement of the society to the information era. Wireless systems include broadcast and television transmission, cellular telephones, wireless local area networks, etc. The design of high performance, low cost, highly integrated receiver has long been the focus of generations of engineers.

Radio had a long history before it was finally commercially used and became our first mass medium, which is able to disseminate information instantly from one to many. It has been a technology that has influenced the whole planet, and changed the world. In 1600, William Gilbert suggested a link between static electricity and magnetism. After more than 200 years' development, in 1864, James Clerk Maxwell formulated "Maxwell's Equations", which account for the actions of electromagnetic waves. Immediately after that year, Mahlon Loomis transmitted wireless telegraph messages between two mountains in Virginia in 1865. In 1898, Marconi installed the worlds first commercial radio service on Rathlin Island off the coast of Ireland. In 1923, the first portable radio receiver was invented by Edwin Armstrong, which is shown in Fig. 1.1.

Fig. 1.1 First Portable Radio Receiver in History

Radio technology developed rapidly in the following decades of years, it is estimated that there are 584,900,000 radio receivers in use in the end of last century. As for the size of the modern tiny radio, it is only of the order of 10 square centimeters. Fig. 1.2 shows the illustrative diagram.

Fig. 1.2 Current Highly Compact Radio Receiver

The amazing volume reduction just reflects the advancement of the technology, especially of the modern CMOS technology and receiver design techniques.

The similar situation occurs for mobile phone development. In the early years when mobile phone was commercialized, it was a very heavy "big guy". Now mobile phones are normally less than 100g, and there are more than 1 billion mobile phone users in the world.

The radio has ever been one of the main commercial products that drive the research on high performance receivers. Now cellular phone is definitely one of the market drivers. It accounts for a significant portion of the communication industry. Advancement of analog electronics also benefits a lot from this sector.

Various receiver architectures have been proposed and some commercially used. All

of them should meet many requirements for practical use. Generally, the function of a receiver is to detect the desired signal among noise and other sources of electromagnetic radiation. Since all wireless systems usually operate in a troublesome environment and interferers always exist, the resulted eligible receiver is inevitably complicated and involves many analog, digital integrated circuits and external components, especially in the early days. Even in several years ago, normally a mobile receiver was comprised of around 500 components. This number didn't count in the post processing units of a receiver. Now, a common mobile receiver normally consists of around 100 components. The direction of better designing the receiver is quite obvious, that is to reduce the components as many as possible. Or, put it in another way, to integrate as many components as possible in a single chip, and improve the performance of the critical components to eliminate some others. By using advanced VLSI technology, all the functionalities of a receiver could possibly be integrated on a single chipset. Thus make the receiver more compact, energy efficient and lighter.

Since this work is part of a receiver, we would like to go into more details of the basics of general receivers. A traditional heterodyne receiver is shown in Fig. 1.3. It normally consists of the following parts:

Antenna — It receives the signal from the environment and also provides some selection function.

Radio Frequency (RF) Filter — It selects the desired band of signal. For GSM (global system for mobile telecommunication) application, the signal band lies in 935MHz – 960MHz.

Low Noise Amplifier (LNA) — Because the received signal is usually very weak, LNA is essential here for proper subsequent signal processing.

Image Rejection (IR) Filter and Mixer — This is used to convert the RF signal to a reasonable Intermediate Frequency (IF) signal. IR filter is added to avoid the image signal to corrupt the desired one.

Channel Selection Filter — After signal being down converted, a desired channel is selected and other adjacent channels are suppressed.

Automatic Gain Control (AGC) — Due to different environments and various distances from the base station and receiver, the signal strength appeared at the receiver antenna could vary as much as around 100dB. Thus AGC is indispensable for the receiver to handle all these possible signals.

Analog to Digital Converter (ADC) — Though nowadays digital modulation is dominantly used, the signal always transmits in analog form. ADC is needed for following digital postprocessing.

Digital Signal Processing (DSP) — The advancement of CMOS technology makes the integration level of digital integrated circuits higher and higher, complex digital functions can be relatively easily implemented and with higher performance than analog counterpart. Thus, more and more functions are moved to digital part for lower cost, higher integration, and compact size. DSP here deals with the output of ADC and mainly decodes the received signal.

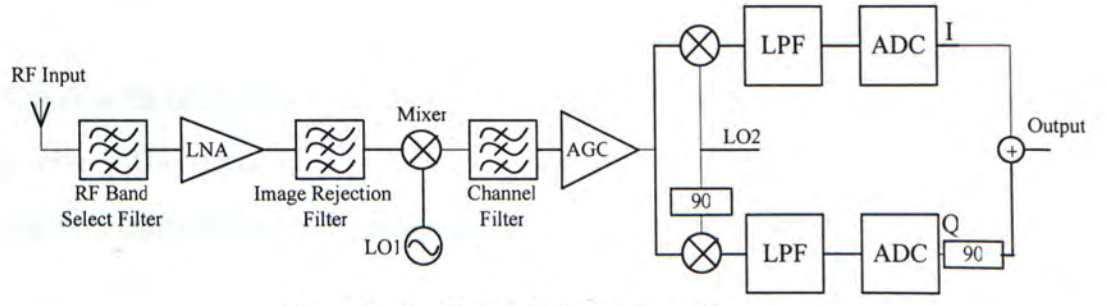


Fig. 1.3 Traditional Heterodyne Receiver

As we can see, the traditional receiver contains many building blocks. Some of them are difficult to integrate, like the channel select filter. Thus the receiver is relatively large and the cost is more. But this filter is critical because it suppresses the undesired channels and together with the AGC it can substantially ease the dynamic range requirement of the following ADC. But on the other hand, if we could build an ADC with sufficient dynamic range, image rejection, signal to noise ratio and so on, we could reasonably eliminate the external channel select filter, AGC, etc. put it

further, if the performance of the ADC is really good enough, so that we can convert the analog signal to digital one in the RF frequency, then possibly only one analog to digital converter is needed in the RF and baseband in the receiver. Practically there are many technical problems regarding the high dynamic range ADC and RF range ADC, the requirement is really too harsh to reduce the receiver to a single ADC (except for postprocessing). But this ultimate objective always drives many engineers to dive into the research of high integrated receiver. Currently, many of the engineers are trying to move the analog to digital converter nearer and nearer to the antenna, in other words, the high performance ADC is actively being studied in the hope of reducing as many other components as possible in a receiver.

This work is conducted in such a situation. Receiver related design is always a hot field, it speeds up the progress to the aim that we can communicate at any time, anywhere. Any attempt that could facilitate the high integration of the receiver is desirable. And finally, high integrated, low cost, low area receiver will come into use, benefit us all and the advancement of the society.

Sigma delta modulation technique is adopted as the analog to digital converter in a receiver. This technique is widely used in the last decade due to its desirable characteristics that we will go into details in the following context.

Without any doubt, wireless technology will continue to evolve at a rapid pace, in the end, a person only need to bring one pocketable communication terminal to receive multiple of high quality services anywhere he goes and at any time.

1.2. Motivation and Objectives

As described in the previous section, receiver is an important integral part of the information industry. Various mobile terminals and radio terminals, etc, are the

essential equipments for people at large. Improving the performance and increasing the integration level of the receiver are one of the key research areas in the high-tech field, in order to reduce the cost of the receiver, make it more compact, lighter and easier to be integrated in any other possible equipment.

The objective of this work is to improve the performance of the critical part of the receiver, that is, the analog to digital converter part. In particular, the image rejection problem is being studied and alleviated in a targeted IF input complex analog to digital converter.

As described in the last section, image rejection is a critical receiver parameter which partially determines the performance of the receiver [1]. Specifically, it indicates the influence of the adjacent image channel or interferer. In order to achieve better performance and high integration of receiver, the IR ratio should be kept as small as -60dB - -80dB for many receiver architectures[2]. Even for zero IF down-conversion scheme where image problem is not serious [3], high IR ratio is mandatory to process all signal channels in the front end and leave channel selection to the following digital circuit [4].

1.3. Original Contributions of This Work

In this work, an IF input complex baseband continuous time sigma delta modulator is designed and implemented. A resistor time sharing technique is proposed to improve substantially the image rejection performance. In addition to this, new transformation approach from discrete time sigma delta modulator to continuous time one is presented; Arbitrary scaling of internal signal swings of sigma delta modulator is obtained based on the theoretical transfer function; LO clock generator is designed with phase fine-tuning ability, which is critical in helping eliminate image signal; Wide output swing operational transconductance amplifier (OTA) is studied and two

novel schemes are proposed to achieve near rail to rail output swing. One is the capacitor bypass technique, the other is resistor splitting technique. Both will be analyzed in the related sections of this thesis. Besides, simple current comparator, remedies for stable operation of certain biasing circuitry, comparison of models of RC integrator, etc, are also presented in this thesis.

1.4. Organization of the Thesis

The thesis is organized into six chapters. Chapter 1 gives the introduction, which covers the background and the fundamentals of the closely related topics. The motivation and objectives are also given in this chapter.

Chapter 2 introduces the sigma delta modulation technique and the theory, both discrete time and continuous time sigma delta modulator are dealt with. The IF input baseband sigma delta modulator with integrated mixer is also briefly discussed.

Chapter 3 presents the high level modeling of the sigma delta modulator and the traditional IF input continuous time sigma delta modulator. Some nonidealities are also attempted to be modeled in high level simulation.

The proposed techniques in designing the work is given in chapter 4, transistor level implementation of individual components and whole architecture are presented. layout considerations are also discussed here.

PCB board design and measurement appears in chapter 5, discussion of the measurement result is also given. Conclusion is in the last chapter, chapter 6.

Finally, the bibliography is given.

2. Chapter 2

Sigma-delta Modulation and IF A/D Conversion

2.1. Introduction

This chapter reviews the properties of the sigma delta modulator. Bandpass sigma delta converter and IF input baseband sigma delta converter are also briefly described.

Sigma delta converters was introduced by Inose et al. in 1962 [5], it oversamples the input signal with a low resolution quantizer, then the output is fedback and subtracted from the input, the large loop gain make the feedback signal (or output signal) trace the input signal. On the other hand, the noise is shaped by the noise transfer function (NTF) of the system, the quantization noise at low frequency is suppressed and moved to higher frequency. Because of oversampling, the higher frequency component of the output can be filtered out using digital circuit. Sigma delta modulator achieves high resolution at the cost of oversampling and complex subsequent digital circuit. But as the VLSI technology advances aggressively, digital circuits are extensively used due to their simplicity of design and test, robustness, accuracy, flexibility and easy programming. And the important factor that digital circuits can take full advantage of the fine line VLSI technology to achieve high integration, low power consumption and low cost. Moving as more traditionally analog functions as possible to digital part is highly desirable. The oversampling characteristic of the sigma delta modulator restricted its application to relatively low frequency signal conversion. However, bandpass sigma delta modulator can handle

high frequency signal as well. As technique advances, high frequency application like video processing can also employ sigma delta techniques. The major advantage of sigma delta technique over other conventional ADC is the high tolerance of the noise and nonidealities of the analog components, thus it is more suitable for highly integrated mixed signal circuits where digital noise coupling is serious.

IF input baseband sigma delta modulator is an alternative to bandpass sigma delta modulator, but low power consumption is needed. Integrated mixer provides flexibility of the IF input modulator. Image rejection problem is discussed and in phase and quadrature phase modulators are firstly touched upon in this chapter.

2.2. Fundamentals of Sigma-delta Modulation

2.2.1. Feedback Controlled System

The idea of sigma delta modulator can be dated back to 1954, a feedback system with a low resolution quantizer was invented by Cutler [6]. The principle of improving the resolution of a coarse quantizer by applying a negative feedback to the input is the essence of the sigma delta modulator. The basic feedback controlled converter has no noise shaping property until in 1962, Inose et al. [5] creatively added a filter in the forward path.

The system is called sigma delta modulator, because sigma means summation, which refers to the low pass filter or integrator in the loop, delta means subtraction, which refers to the subtraction of input signal and feedback signal. The general diagram of a single loop sigma delta modulator is shown in Fig. 2.1.

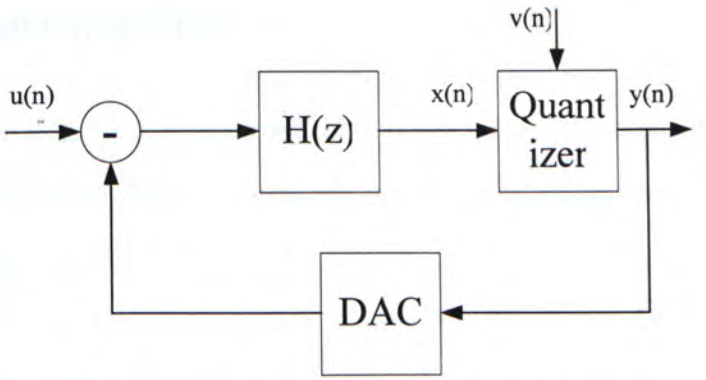


Fig. 2.1 Single Loop Sigma Delta Modulator

Sigma delta modulator is essentially a nonlinear system because of the quantizer in the loop. This makes the analysis complicated and even difficult to subtly study some of its properties. An easy way to understand the working principle of sigma delta modulator is artificially linearize it and analyze it in frequency domain. As illustrated in the above diagram, the quantizer can be modeled as an adder of the filtered input signal and quantization noise. Thus we can write out the transfer function of the system:

$$y(n) = STF * u(n) + NTF * v(n) \tag{2.1}$$

where

$$STF(z) = \frac{H(z)}{1+H(z)}$$
$$NTF(z) = \frac{1}{1+H(z)} \tag{2.2}$$

The loop filter H(z) has high gain at low frequency, thus signal transfer function (STF) approximates to 1 at low frequency, while noise transfer function (NTF) approximates to 0. In this way, the feedback system elegantly converts the analog signal to digital one and suppresses the noise in low frequency band which is of interest.

2.2.2. Quantization Noise

The quantization noise can be assumed to be white if the input signal is busy enough and the input signal amplitude covers the whole input range of the quantizer. The quantization noise uniformly distributes across $-\Delta/2$ - $\Delta/2$, where Δ represents the distance between two quantization levels. Fig. 2.2 shows the ideal probability density function of the quantization noise.

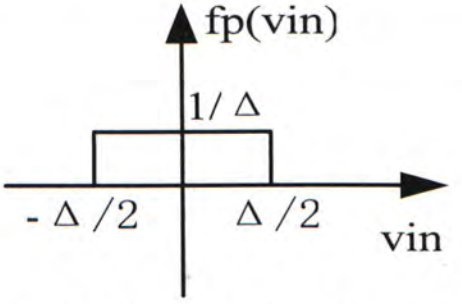


Fig. 2.2 Ideal Probability Density of Quantization Noise

The mean square value or noise power (normalized to 1 Ω) is given by

$$\sigma^2(e) = \int_{-\Delta/2}^{\Delta/2} e^2 fp(vin)de = \int_{-\Delta/2}^{\Delta/2} e^2 \frac{1}{\Delta} de = \frac{\Delta^2}{12} \tag{2.3}$$

For a common ADC the noise is dominated by quantization noise, thus signal to noise ratio (SNR) is equal to

$$SNR(dB) = 10\log_{10}(\frac{Sin}{\sigma^2(e)}) = 10\log_{10}\frac{2^{2n}\Delta^2/8}{\Delta^2/12}$$
$$= 10\log_{10}\frac{3}{2}2^{2n} = 1.76 + 6.02n \tag{2.4}$$

For high performance sigma delta modulators, the quantization noise at the band of interest can be neglectable, the next section will give the explanation.

2.2.3. Oversampling and Noise-shaping

The high resolution requirements for modern signal processing cannot be met by many conventional ADC, partly because they do not exploit the merits of

oversampling the signal. Most of them sample signal at Nyquist rate, which can barely represent the signal without introduce aliasing. The corresponding quantization noise power is derived in the last section. The reason why oversampling can increase the resolution is because the quantization noise spreads out between $-\frac{f_s}{2} \sim \frac{f_s}{2}$, while the signal band is far smaller than $\frac{f_s}{2}$, so we can eliminate the noise lying out of the band by means of a high accuracy digital filter. Fig. 2.3 depicts the quantization noise and signal in Nyquist converter and oversampling converter respectively. Note that the total quantization noise keeps constant.

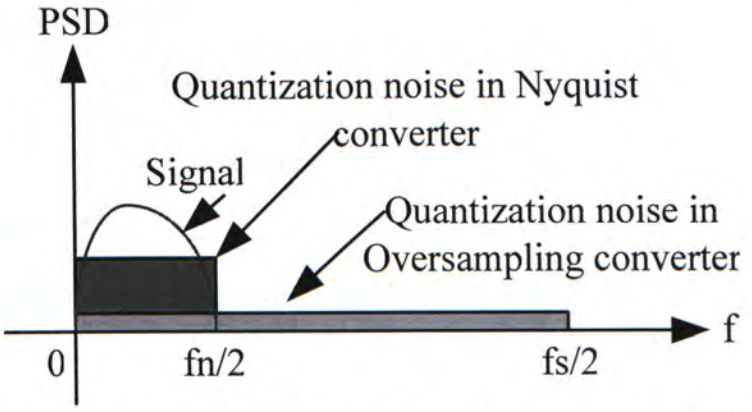


Fig. 2.3 Qantization Noise in Nyquist and Oversampling Converter

A measure of the oversampling is the ratio R, which is defined as following:

$$R = \frac{f_S}{f_N} \tag{2.5}$$

Accordingly, for an oversampling ratio of R, the SNR can be rewritten as

$$\begin{aligned} SNR(dB) &= 10\log_{10}\left(\frac{Sin}{\sigma^2(e)/R}\right) \\ &= SNR_{Nyquist} + 10\log_{10}(R) \end{aligned} \tag{2.6}$$

This equation shows that the SNR can be increased by 3dB if the sampling rate is doubled, that means, every four times of the sampling rate equals to one bit increase in resolution. The concept also indicates that we could theoretically increase the resolution indefinitely by increasing the sampling frequency. But in reality, the sampling frequency would become unreasonably large. Suppose we want to use a

one bit ADC to achieve 12 bit accuracy of a signal with up bound frequency of 20kHz, the sampling frequency should be $20\text{kHz}\times 2\times 4^{11}\approx 168\text{GHz}$, this sampling rate is not realizable even in the foreseeable future.

In order to further increase the resolution of an ADC with reasonable sampling frequency, noise shaping is introduced to move the quantization noise in the signal band to higher frequency. The noise shaping function is realized by the loop filter in the sigma delta modulator. It's one of the most important features of the sigma delta modulator to achieve extreme high resolution. To illustrate the working principle of noise shaping of sigma delta modulator, let's briefly revisit the noise transfer function and signal transfer function of a single stage sigma delta modulator,

$$STF = \frac{H(z)}{1+H(z)}$$
$$NTF = \frac{1}{1+H(z)} \tag{2.7}$$

We can replace H(z) with a standard first order integrator

$$H(z) = \frac{1}{z-1} \tag{2.8}$$

The power spectrum density of the quantization noise after being shaped by the NTF is depicted in Fig. 2.4. The signal transfer function is also illustrated with dashed line.

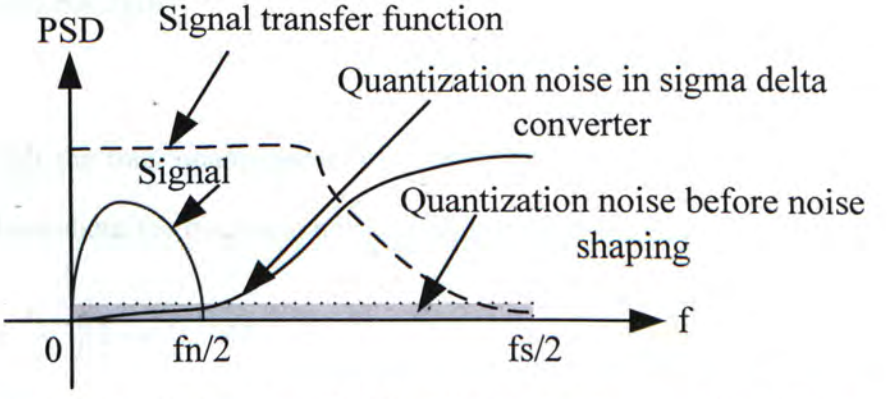


Fig. 2.4 Signal Transfer and Noise Shaping in Oversampling Converter

If we apply a higher order loop filter, the more low frequency quantization noise will be suppressed, even to an extent that quantization noise can be ignored. This is the

very reason that sigma delta modulator can obtain very high resolution.

So how much does the noise shaping suppress the in band quantization noise? We can analyze this through a simple first order sigma delta modulator.

Since $H(z)=\frac{1}{z-1}$, then

$$\begin{aligned} STF(z) &= \frac{1}{z} \\ NTF(z) &= \frac{z-1}{z} \end{aligned} \tag{2.9}$$

It's clear that the STF only introduces one period delay of the input signal, while the NTF high passes the quantization noise, assume oversampling ratio is R, signal band is $0 \sim f_b$, f_s is the sampling frequency. We also take the quantization noise as white noise in this case.

The total noise power after noise shaping is

$$\begin{aligned} Pn,tot &= \frac{1}{f_s}\int_{-f_s/2}^{f_s/2} |\, NTF(e^{j2\pi f/f_s})\,|^2 \, P_e df \\ &= \frac{1}{2\pi}\int_{-\pi}^{\pi} |\, NTF(e^{j\theta})\,|^2 \, P_e d\theta \\ &= \frac{P_e}{\pi}\int_{0}^{\pi} |\, 1-e^{j\theta}\,|^2 \, d\theta \\ &= \frac{P_e}{\pi}\int_{0}^{\pi} (2-2\cos\theta) d\theta \\ &= 2P_e \end{aligned} \tag{2.10}$$

We see that the total quantization noise becomes one times larger than not shaped one. So how about the fractional noise in the band of interest? $P_{e,inband}$ comes here

$$\begin{aligned} P_{e,inband} &= \frac{P_e}{\pi}\int_{0}^{\pi/R} |\, 1-e^{j\theta}\,|^2 \, d\theta \\ &= \frac{2P_e}{\pi}\left(\frac{\pi}{R}-\sin\frac{\pi}{R}\right) \end{aligned} \tag{2.11}$$

If R>>π, then sine function can be expanded using Taylor series around zero. This yields

$$P_{e,inband} \approx \frac{2P_e}{\pi}[\frac{\pi}{R} - (\frac{\pi}{R} - \frac{\pi^3}{6R^3})] \\ = P_e \frac{\pi^2}{3R^3} \tag{2.12}$$

While if no noise shaping is applied, the in band noise would be

$$P_{e,oversampling} = \frac{P_e}{R} \tag{2.13}$$

We can easily derive that

$$\frac{P_{e,inband}}{P_{e,oversampling}} = \frac{\pi^2}{3R^2} \quad (R >> \pi) \tag{2.14}$$

This equation shows noise shaping is very effective in attenuate the quantization noise in the band of interest, especially when R is large.

If the loop filter is a higher order one, the noise shaping will become even more aggressive, making it virtually neglectable.

2.2.4. Stability

Sigma delta modulators are basically feedback controlled systems, their stability should be studied carefully. Universally, instability of sigma delta modulator will occur when two conditions are satisfied

i: closed loop gain is equal to 1

ii: total phase shift in the loop is 2π or its multiples

Because sigma delta modulator is fundamentally a complicated nonlinear system, guaranteed loop stability is still not possible for high order sigma delta modulator. Take a simple second order sigma delta modulator as an example, its loop filter has -180 degrees phase shift at high frequency if not compensated, it's very dangerous to have such a phase shift in a negative feedback system, the oscillation condition could easily be met. Thus, to make the system more reliable, at least a zero should be introduced to compensate for the poles. In another word, feedforward paths or

additional feedback paths should be added.

Instability is detected from the behavior of its internal signals. To obtain stable operation of a sigma delta modulator, the internal quantizer shouldn't be overloaded. Once the modulator is unstable, it's hard to return to stable operation. When a sigma delta modulator is unstable, the output of the system shows low frequency oscillation, that is, many consecutive 1s followed by many consecutive 0s, and the process repeats. Instability doesn't necessarily occur at the beginning of its operation. We can force the modulator back to stable state by adding some detection mechanism. For instance, reset the whole modulator once unstable condition is detected, or clip the outputs of latter stages in an effort not to overload the quantizer.

Stability analysis of sigma delta modulator is difficult because of the internal nonlinear quantizer. We can model the quantizer with a gain k and a phase shift θ [7], root locus of particular modulator can be obtained through numerical analysis, if there are poles located outside of the unit circle or to the right of imaginary axis in discrete time modulator and continuous time one respectively, the system is unstable. This kind of modeling and analysis can only provide us an intuitive knowledge about the stability of sigma delta modulator, because the two unknown k and θ are not fixed value, they change at each sampling instant.

Stability is an important issue in designing sigma delta modulator, we should select appropriate NTF to obtain an optimal and stable modulator. Many stability criteria have been developed empirically based on extensive simulations [8], two of them are i: The sum of the absolute value of each term in the impulse response of NTF is bounded to

$$S_h = \sum_{0}^{\infty} | h_i | = 3 - x_{\max} \tag{2.15}$$

where x_{max} is the maximum signal amplitude that the modulator remains stable.

ii: The maximum value of the NTF is smaller than c, which approximates to 2.

$$M = \max[NTF(z)] < c \tag{2.16}$$

Though the above criteria achieve stable performance to some extent, the SNR seems to be low. A rule of thumb derived from many researchers states that the out of band gain of NTF should be about 1.5. The larger this gain, the more it tends to be unstable, but the better SNR will result if it remains stable. The input of the sigma delta modulator should restrict itself to below around 0.6Vref for high order sigma delta modulator, otherwise the quantizer is prone to be overloaded [8,9].

2.2.5. Noise Sources

Up to now only quantization noise is considered in sigma delta modulator, other components are assumed to be ideal. But in practice it is not true, all the implemented building blocks have nonidealities. Some of them noticeably affect the overall performance of the sigma delta modulator. Though we mentioned that sigma delta modulator is somewhat immune to circuit nonidealities, as design specification become more and more demanding, we have to carefully take them into account.

Generally, sigma delta modulator has high tolerance of noise in the loop of the modulator, because they are more or less attenuated by the loop gain ahead of them, this is true especially for noise introduced in latter stages, including quantization noise, as long as the loop gain before them are large enough. Unfortunately, any noise or error found at the input of the modulator are not shaped by noise transfer function and reflects at the output directly. The system just regards them as part of the input signal.

The special feature of sigma delta could result in a modulator whose output noise power is not determined by quantization error but other error sources. This is different from its Nyquist converter counterpart. The known important noise sources

include thermal noise, flicker noise, clock jitter, excess loop delay, intersymbol interference, DAC error and nonideal opamp, which has finite settling time, finite gain, finite unit gain bandwidth, finite output swing, etc. Since the errors introduced in the latter stages are usually neglectable compared with them in the first stage, we will concentrate ourselves on the circuitry connect to the input and first stage opamp of the sigma delta modulator.

I: Thermal Noise and Flicker Noise

Thermal noise is caused by random motion of electrons in conductor. They have a Gaussian distribution and are white up to Terahertz. The power spectrum density (PSD) of thermal noise is

$$P_t(f) = 4kTR \tag{2.17}$$

It is proportional to the resistance R. Usually the input differential pair of first opamp is important in contributing thermal noise and flicker noise. The mechanism of flicker noise is not very clear up to now, but they are believed to be related to the imperfection of channel surface of MOS transistor. The flicker noise PSD can be modeled as

$$P_f(f) = \frac{K_f}{WLC_{ox}f} \tag{2.18}$$

From the formula we can see that flicker noise power is inversely proportional to frequency, it's the dominant noise source at low frequency. W, L are dimensions of MOS transistor, C_{ox} is the capacitance of the gate per unit area. K_f is highly technology dependent and may vary from one wafer to another.

At a certain frequency, flicker noise falls down to the value of thermal noise, where the corresponding frequency is called corner frequency, we can easily derive that

$$f_{CF} = \frac{K_f}{4WLC_{ox}kTR} \tag{2.19}$$

Usually noise in MOS transistor can be modeled by a thermal noise voltage source

and flicker noise voltage source, since they are uncorrelated, The joint PSD of them can be put in this way:

$$\frac{\overline{v_{in}^{2}}}{\Delta f} = 4kT\gamma\frac{1}{g_m} + \frac{K_f}{WLC_{ox}f} \tag{2.20}$$

Since at low frequency, the flicker noise dominates, we should try to avoid the adverse effect. Clearly, if we increase the area of the input transistor pair, the flicker noise will decrease accordingly. This should be enough for most designs. Besides, we can adopt two other well known techniques to handle this problem. One of them is chopper stabilization, which converts the low frequency noise to higher frequency while keeping desired signal unchanged through up conversion and down conversion. The other popular technique is correlated double sampling (CDS). It finds wide applications in switched capacitor circuits. CDS can not only significantly reduce the flicker noise but also remove DC offset and errors due to finite gain of opamp.

In continuous time sigma delta modulator, RC integrator is usually adopted at the first stage for its high linearity. The input resistor here also directly contributes to the total thermal noise. Though thermal noise spreads out at a very wide frequency range, in the case of continuous time sigma delta modulator, the thermal noise introduced at the input stage will be low passed by the internal loop filter. Thus when the quantizer samples the filter output, the aliasing problem will not occur, since sampling frequency is normally much larger than the cut off frequency of the loop filter. As a result, the thermal noise introduced by the input resistor equals

$$P_{t,inR} = 4kTR_{in}\frac{f_s}{2OSR} \tag{2.21}$$

In discrete time sigma delta modulator, aliasing occurred because the thermal noise is directly sampled by switched capacitor circuit. The total thermal noise is inversely proportional to the value of sampling capacitor.

II: Clock Jitter

Clock jitter refers to the time uncertainty at each rising or falling edge of a clock

signal. This may result in erroneous sampling which is triggered by edges of clock signal or other noises. Jitter is unavoidable because of the intrinsic noise of pulse generating circuitry. The impact of clock jitter is more severe in continuous time sigma delta modulator than in discrete time sigma delta modulator. We will analyze this in detail as follows.

In discrete time sigma delta modulator, suppose the input signal is $A\sin\omega t$, clock edge uncertainty Δt is uniformly distributed in the range [-τ , τ], input signal is practically sampled at $nT_s + \Delta t$ instead of ideal nT_s

, this introduces the sampling noise power:

$$\begin{aligned} P_{jitter} &= E\{[x(nT_s + \Delta t) - x(nT_s)]^2\} \\ &\approx E\{[x'(nT_s)\Delta t]^2\} \\ &= \frac{A^2\omega^2}{2}E(\Delta t^2) \\ &= \frac{A^2\omega^2\tau^2}{6} \end{aligned} \tag{2.22}$$

If the frequency of input signal is $\omega_s / 2OSR$, since the signal is oversampled by OSR, the noise lies in the band of interest is

$$\begin{aligned} P_{jitter,in} &= \frac{A^2(\omega_s / 2OSR)^2\tau^2}{6OSR} \\ &= \frac{A^2\omega^2\tau^2}{24OSR^3} \end{aligned} \tag{2.23}$$

In continuous time sigma delta modulator where RC integrator is adopted, the feedback pulses of DAC are integrated by the RC integrator, the jitter in the feedback pulses affects the integration time of the integrator. With the presence of jitter, the error power at the output of the RC integrator is given as

$$
\begin{aligned}
P_{j,RC} &= E[v_e(n)^2] \\
&= E[(\frac{1}{RC}\int_{t_1+\Delta t_1}^{t_2+\Delta t_2} V_{ref}\,dt - \frac{1}{RC}\int_{t_1}^{t_2} V_{ref}\,dt)^2] \\
&= \frac{{V_{ref}}^2}{(RC)^2}(E({\Delta t_1}^2) + E({\Delta t_2}^2) + E(-2\Delta t_1 \Delta t_2)) \\
&= \frac{2{V_{ref}}^2 \tau^2}{3(RC)^2}
\end{aligned}
\tag{2.24}
$$

During the derivation, we assumed that the jitter is white noise and they are equally distributed in the range of [-τ , τ], Δt1 andΔt2 are thus uncorrelated. The noise power in the signal band is simply divided by OSR

$$
P_{j,RC,inband} = \frac{2{V_{ref}}^2 \tau^2}{3OSR(RC)^2} \tag{2.25}
$$

Now we obtain the jitter noise power at the output of the integrator, its input referred noise can be calculated as follows, again assume the noise is white and the in band power distributes uniformly in the signal band [0 , f_b].

$$
\begin{aligned}
P_{j,inputref} &= \int_0^{f_b} \frac{P_{j,RC,inband} / f_b}{|1/RCS|^2} df \\
&= \frac{8(V_{ref}\tau\pi f_b)^2}{9OSR}
\end{aligned}
\tag{2.26}
$$

The formula shows that input referred in band jitter power of continuous time sigma delta modulator is inversely proportional to the oversampling ratio, while the corresponding jitter noise power in discrete time modulator is inversely proportional to the cube of OSR. Their numerators are of the same order. We can safely conclude that the jitter requirement of continuous time modulator is much more demanding than that of discrete time counterpart, if comparable performances are to be achieved.

III: Intersymbol Interference

This effect is also due to the nonideal pulses like jitter. It is especially of concern in continuous time sigma delta modulator. The feedback pulses have different rising time and falling time, in addition, the pattern of feedback signals also varies, thus the integration time of the RC integrator varies for different sequences of feedback

signals. Fig. 2.5 gives the illustration

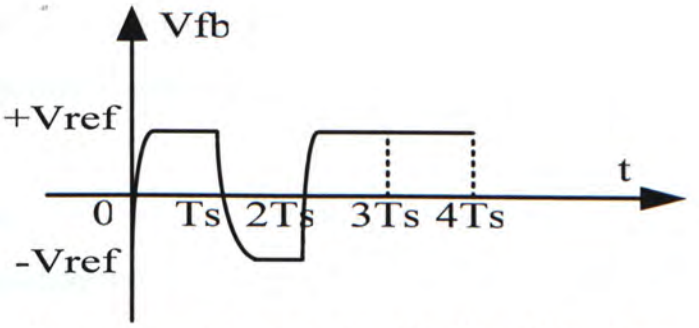


Fig. 2.5 None Return to Zero Feedback Waveform

As shown in the diagram, the feedback signals have slightly different forms according to different feedback patterns, the first feedback signal experience a finite rising time while the second one a longer falling time, while the fourth one are ideal feedback signal due to the same level adjacent feedbacks. This kind of feedback signals will inevitably introduce noise similar to that of jitter. If the sampling frequency of the modulator is not very high and the clock has neglectable rising and falling time, then this effect can be ignored. Otherwise some correction techniques should be employed to conquer this problem. Note that this intersymbol interference noise is added to the input of the system, thus has direct effects at the performance of the modulator. Return to Zero feedback signals can be used to eliminate the asymmetry of the signals. Now the feedback takes the form shown in Fig. 2.6.

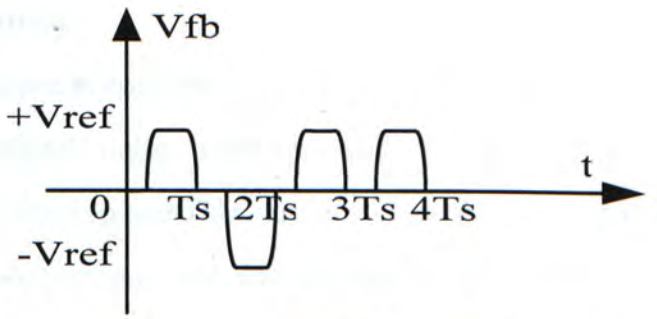


Fig. 2.6 Return to Zero Feedback Waveform

Each feedback signal returns to zero at two ends of a period, thus all of them experience the same rising time and falling time. This can guarantee that the

area(integration operation) under each waveform are the same, intersymbol effect can be removed nicely. The possible side effect is the feedback reference voltage should be scaled up to keep the total charge to the integration capacitor the same. We can also scale down the feedback resistors to solve this problem.

IV: DAC Errors

Sigma delta modulator usually adopt single bit DAC, because two level digital to analog converter is essentially linear, the only error source of such DAC is unmatched reference voltages, they are reflected at the output of the modulator as DC offset, which can easily be eliminated in digital postprocessing. If multi-bit internal analog to digital converter is adopted to enhance the performance of the modulator [8,10], we should pay special care to the multi-bit DAC thus involved, because the error associated to each level is somewhat random and highly depends on the fabrication, after tape out, the errors are probably fixed and will introduce harmonics or tones in the output spectrum. According to the features of the multi-bit DAC error, we could randomizing the error by dynamically use the elements which set the reference levels, in this way, the modulator only sees near white noise at the input [2,11]. Other techniques that can relieve the problem can be referred to [12], we will not go into this issue further because it involves too much and the design in this work adopts single bit DAC.

V: Excess Loop Delay

This issue will happen in continuous time sigma delta modulator, it refers to the extra delay of the feedback pulses compared with the sampling clock. Because the quantizer, digital flip flop and DAC are not ideal, they will unavoidably introduce some delay, this phenomenon will alter the transfer function of the designed system, much work has been done by researchers on this issue [13,14,15,16], It is found that if the excess loop delay is less than about 20% of a sampling period, the degradation of performance that it causes is not that severe [16].

In discrete time sigma delta modulator, since only the signal at sampling instant is of concern, excess loop delay doesn't make any difference to the overall performance of the system as long as the delay is less than one sampling period.

VI: Finite OTA Gain and Bandwidth

Ideal OTA have infinite gain and bandwidth, but real OTA do not. In the case of RC integrator that is adopted in this design, the transfer function alters due to these nonidealities. Suppose the OTA can be modeled as a single pole system

$$A(s) = \frac{A}{1 + s/\omega_p} \tag{2.27}$$

Where A is the finite DC gain of the OTA, ω_p is the pole of the OTA, it's easy to deduce transfer function of the RC integrator shown in Fig. 2.7.

$$H(s) = \frac{v_o(s)}{v_i(s)} = \frac{-A\omega_p}{RCs^2 + (RC(A+1)\omega_p + 1)s + \omega_p} \tag{2.28}$$

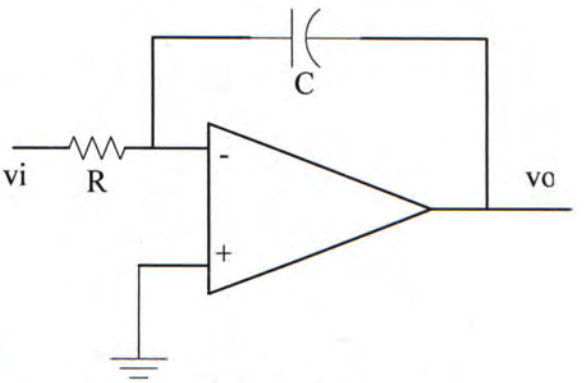


Fig. 2.7 RC Integrator

Ideally, the transfer function is

$$H(s)_{ideal} = \frac{1}{-RCs} \tag{2.29}$$

The pole of the transfer function has been changed, which affects the zeros of the noise transfer function. The attenuation of noise around DC will be decreased. Anyway, the sigma delta modulator is quite robust to the finite gain and bandwidth of OTA. Below comes the brief analysis of these two effects.

For a first order continuous time sigma delta modulator where RC integrator is adopted, other parts of the modulator being considered as ideal,

$$NTF = \frac{1}{1+H(s)} \tag{2.30}$$

For four situations, ideal OTA, ideal bandwidth (dominant pole) but finite gain, ideal gain but finite bandwidth, finite gain and bandwidth, the respective noise transfer functions are plotted in Fig. 2.8.

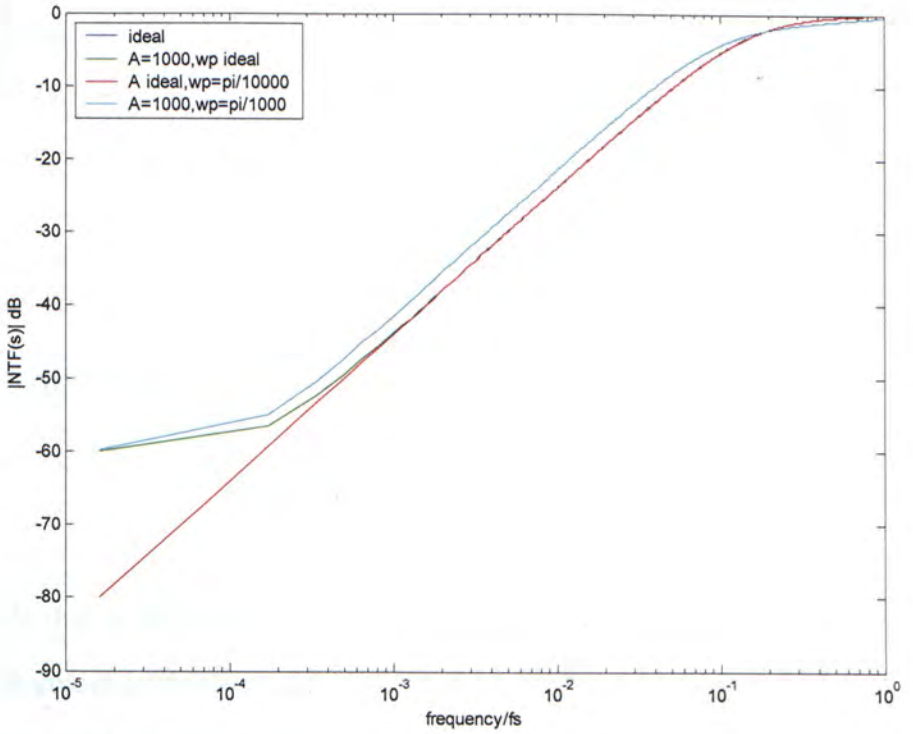


Fig. 2.8 NTF for Different Gains and Bandwidths

Judging from the diagram, if gain of the OTA is large enough, the position of the pole has little effect on the NTF, since now unit gain bandwidth is also ideal. If gain is relatively small, then the low frequency attenuation will decrease. The smaller the pole, the less the attenuation will be. We can also conclude from the plot that if the oversampling ratio is not very large, the sigma delta modulator is very tolerant to finite gain and bandwidth.

From another perspective, we fixed the gain to 1000, and study the influence of

different unity gain bandwidth (UGW or GBW). Fig. 2.9 shows the plots of three NTFs under different relations between sampling frequency ω_s and UGW.

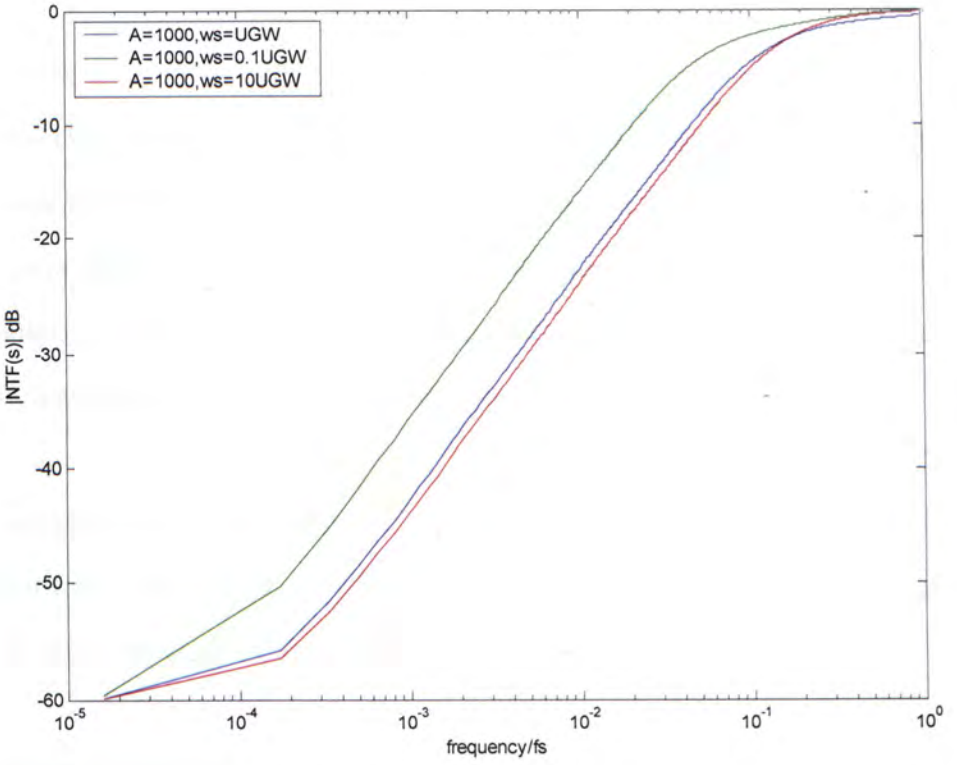


Fig. 2.9 NTF For Different GBWs

It reveals that if the UGW is of the order of sampling frequency, the performance hardly degrades compared with ideal UGW, but when the UGW is only one tenth of the sampling frequency, the SNR will decrease substantially.

VII: Finite Settling Time and Slew Rate

Finite settling time is due to finite unit gain bandwidth, there exists a charging time constant τ. This process is linear because if the steady output value is larger, the rising speed will correspondingly increase. This can be understood by relating the settling process to a simple serial RC circuit, suppose a pure step signal with amplitude V is applied to the RC circuit, initial value the voltage across the capacitor is zero.

$$V_o = V - Ve^{-t/RC} \tag{2.31}$$

Clearly, the output is proportional to the input, which results in a linear settling.

Slew rate is limited by finite output current of OTAs, approximately,

$$SR = \frac{I_{bias}}{C} \tag{2.32}$$

Once the OTA is slew rate limited, the output doesn't respond to the input signal magnitude accordingly. Thus it's highly nonlinear and undesirable. In discrete time sigma delta modulator, this nonlinearity can be ignored as long as the final settling at the sampling instant is enough. But in continuous time modulator, harmonic distortion and additional noise will be introduced to the output spectrum [12].

For a pure sine wave input $A\sin\omega t$, the largest slope is Aω, to make the OTA slew rate limit free for this input, the SR should be bigger than Aω, which usually dictates large biasing current, and thus increasing the power consumption.

VIII: Finite Output Swing

Ideal sigma delta modulators with optimal performance always assume the building blocks are perfect. In reality, their optimal performances are often based on large swing at each component's output. As technology scaled down constantly, the supply voltage also decreases to keep the MOS transistor from breaking down and to save power. Ultimately, the output signal swing is severely limited. Signal scaling should be conducted to avoid distortion at the output of each component. But this may result in a set of coefficients with large variance or unreasonable value, which is difficult to implement. In addition, process, temperature, power supply variation may easily change the swing range of integrator's output in such a complex system. Therefore, increase the linear output swing as much as possible is highly desirable in designing robust, high performance sigma delta modulator.

2.2.6. Baseband Sigma-delta Modulation

Sigma delta modulator has two main characteristics, namely noise shaping and oversampling. These two features make it possible to achieve extreme high resolution. On the other hand, oversampling also implies the sigma delta modulator is mainly for converting low frequency signals. Otherwise the sampling frequency would be too large to be dealt with, the active components cannot operate properly at very high frequency. The baseband sigma delta modulator consists of loop filter, quantizer, DAC, etc. Sampling frequency f_s equals OSR times the up bound frequency f_b of input signal.

2.2.7. Bandpass Sigma-delta Modulation

Bandpass sigma delta modulator was introduced to convert the intermediate frequency (IF) signal directly. The signal covers a narrow band centered at IF, the transfer function can be derived using low pass to band pass filter transformation $z \rightarrow -z^2$

The derived band pass modulator possesses the same performance as its baseband counterpart. [12] It also indicates that to achieve the same performance, band pass modulator need to be twice the order of baseband one.

By adopting band pass modulation, high frequency or even RF application are possible while good behaviors are kept [12]. The high demanding of building active units should be recognized and dealt with carefully. Usually the available time for settling is shortened, the gain is not large enough at high IF, clock jitter problem become even more serious, etc.

2.3. Discrete-time Sigma-delta Modulation

We have thus far dealt with the basics of sigma delta modulator. They are mainly divided into two categories, i.e. discrete time sigma delta modulator and continuous time sigma delta modulator. Both of them have their merits and drawbacks. For discrete time one, it is most suited for high integration because capacitors ratios which are utilized in implementing switched cap integrator can be accurately realized in modern VLSI technology. In addition, switched capacitor integrator has high linearity and the building block is robust. But discrete time modulation also has some undesirable features. The most important one is the limited sampling frequency. For proper settling and other operation of OTA, the GBW of the OTA has to be at least 5-7 times larger than the sampling frequency. This makes it difficult for high speed application. Besides, the power consumption of discrete time sigma delta modulator tends to be higher [17].

2.4. Continuous-time Sigma-delta Modulation

In the last decades, continuous time sigma delta modulator receives much attention for their desirable characteristics. Compared with discrete time counterpart, continuous time sigma delta modulator can realize much higher sampling frequency because sampling occurs at the quantizer stage, the preceding OTAs are relieved to some extent. Antialiasing filter is not needed in continuous time implementation, the internal loop filter can perform such function as a by product, while for discrete time one, sampling is at the input of the modulator, additional filter is needed to prevent aliasing from happening. In addition, sampling noise is suppressed by the loop gain also due to the fact that sampling is performed internally.

Nonetheless, the continuous time modulator also suffers from numerous side effects. Such as nonlinear integrator, clock jitter, excess loop delay, etc. Continuous time

integrators are usually implemented using the following three methods

Active RC integrator — which has high linearity but not very suitable for VLSI integration, because the process variation of resistor and capacitor is large, of the order of 20-30%. So tuning is needed if circuit is sensitive to the time constant RC.

Mosfet C integrator — mosfet operate in the linear region can be approximated as a resistor,

$$I_{ds} = \frac{\beta}{2}[2(V_{gs} - V_{th})V_{ds} - V_{ds}^{\ 2}]$$
$$R = \frac{dV_{ds}}{dI_{ds}} \approx \frac{1}{\beta(V_{gs} - V_{th})} \tag{2.33}$$

Here we assumed that $V_{ds}<<1$. It shows that the resistance is not related to V_{ds} to a first order approximation. To improve the linearity of MOSFET resistor, complementary structure can be used. But the integrated time constant using this technique can also vary about 30%.

G_m-C Integrator — This method employs G_m unit instead of opamp or OTA, G_m is different from OTA in that the output current must be linearly proportional to the input voltage, and transconductance must be controllable. From another perspective, G_m is designed for large signal application, usually it is for open loop application. OTAs are always for closed loop application where only small signal input of the OTA is concerned. A simple diagram of a G_m-C integrator is shown in Fig. 2.10.

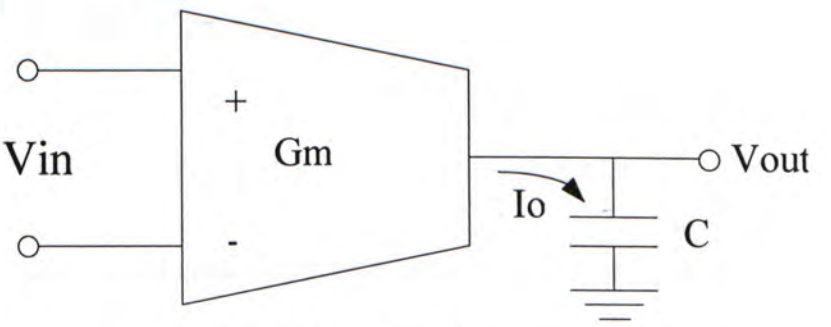


Fig. 2.10 G_m-C Integrator

$$I_o = G_m V_{in}$$
$$I_o = CsV_{out} \tag{2.34}$$
$$\Rightarrow V_{out} = \frac{G_m / C}{s} V_{in}$$

Unfortunately, like the above two methods, G_m/C has a large variation of 30% during fabrication. And the input swing is relatively small due to the limited linear input range of the G_m. The merits of this technique are the operation speed is high and power consumption is relatively low.

In this work, the RC integrator and G_m-C integrator will be utilized to build a high performance sigma delta modulator.

2.5. IF-input Complex Analog to Digital Converter

This work concentrates on the design of IF-input Complex ADC. I path and Q path are employed to solve the image problem which will be analyzed in the next section. IF input is for applications of superheterodyne receivers, in the hope of moving the analog to digital converter nearer and nearer to the antenna of the receiver. The general architecture of this design is given in Fig. 2.11.

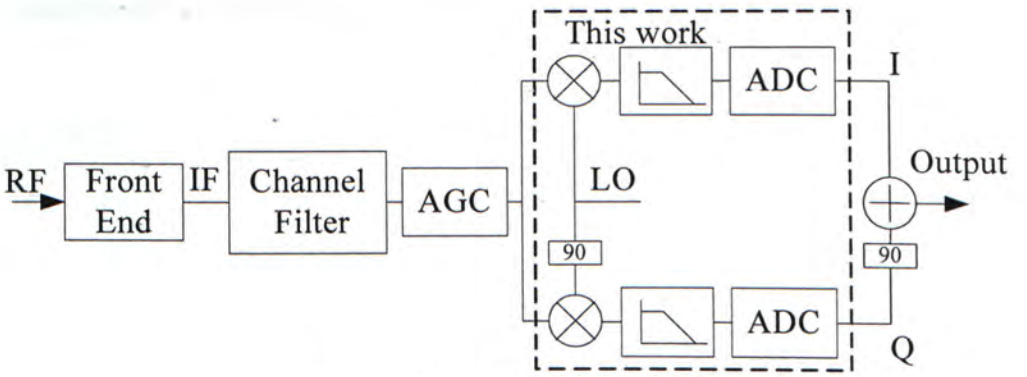


Fig. 2.11 IF Input Complex ADC

Integrated mixer is adopted for saving area and power. ADC is realized using baseband sigma delta modulator due to its high resolution, high linearity and

tolerance of analog components' mismatch. Besides, compared with bandpass sigma delta modulator, baseband modulator consumes less power and is easier to design. This is why the scheme of baseband sigma delta modulator with integrated mixer is adopted instead of bandpass sigma delta modulator.

2.6. Image Rejection

Image signal is an interference signal that lies at the other side of the local oscillator (LO) signal with the same distance as that of desired signal from LO signal. When converted down or up, the image signal will corrupt the desired one since their distances from LO are the same. Suppose there are two signals $A\cos\omega_s t$, $B\cos\omega_i t$, the LO signal is $C\cos\omega_{LO} t$. If

$$\omega_{LO} - \omega_s = \omega_i - \omega_{LO} = \omega_{IF} \tag{2.35}$$

Then after down converting, mixer output Y equals

$$\begin{aligned} &\frac{AC}{2}[\cos(\omega_{LO} - \omega_s)t + \cos(\omega_s + \omega_{LO})t \\ &+ \frac{BC}{2}[\cos(\omega_i - \omega_{LO})t + \cos(\omega_i + \omega_{LO})t \end{aligned} \tag{2.36}$$

Higher frequency signals can be filtered, but $\omega_{LO} - \omega_s = \omega_i - \omega_{LO}$, the desired signal is interfered by the image signal. Fig. 2.12 depicts this problem clearly

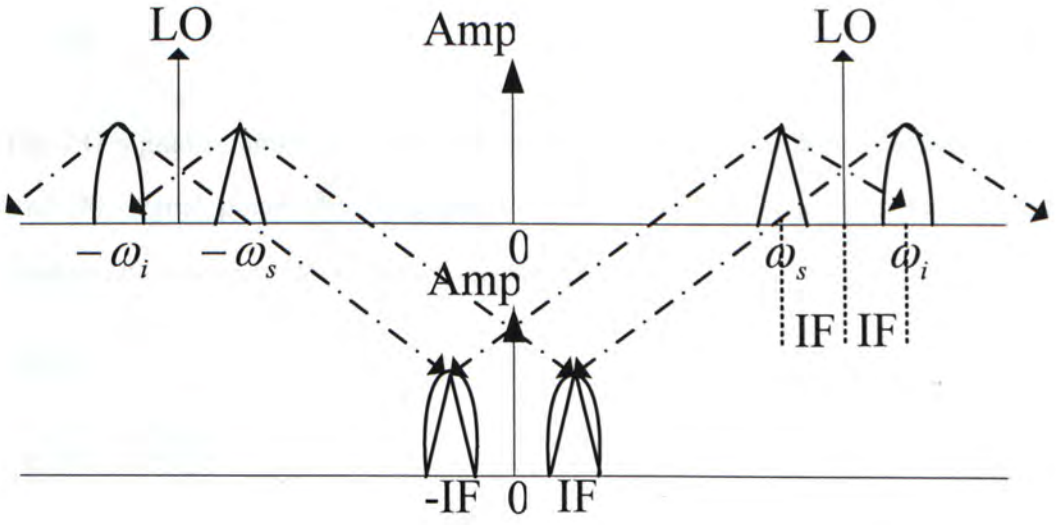


Fig. 2.12 Image Inteference during Down Conversion of IF Signal

The desired signal and image signal overlaps. To conquer this problem, we must filter out the image signal totally before conversion, but practical filters can only attenuate the adjacent images, they cannot be removed. Receivers have harsh requirement on image rejection for reconstructing the desired channel properly. Besides, for a specific application, the signal band usually consists of many channels, each channel could be the image of another channel, since they are close to each other and the image maybe much larger in magnitude than desired one, large image rejection ratio is required. Part of the image rejection is done by a filter, others are achieved by a nice circuit architecture called Hartley, which is the well know quadrature phase conversion. We can refer to Fig. 2.11 for easy understanding. Now let's explain why this architecture can reject image signals.

Let's first review the basics of Fourier series of periodical signals

$$f(t) = \sum_{n=-\infty}^{\infty} C_n e^{jnwt} \tag{2.37}$$

Where C_n and C_{-n} are complex numbers

$$C_n = A_n + jB_n \tag{2.38}$$

$$C_{-n} = A_n - jB_n \tag{2.39}$$

The phase information is shown here

$$\varphi = \tan^{-1}\frac{B_n}{A_n} \tag{2.40}$$

The LO signal is applied to one path of the complex converter, another LO signal with 90 degree phase shift is applied to the other path. They can be denoted as $\sin\omega_{LO}t$ and $\cos\omega_{LO}t$. After Fourier series expansion

$$\sin\omega t = \frac{e^{j\omega t} - e^{-j\omega t}}{2j}$$
$$\cos\omega t = \frac{e^{j\omega t} + e^{-j\omega t}}{2} \tag{2.41}$$

Fig. 2.13 illustrates the two basic trigonometric functions

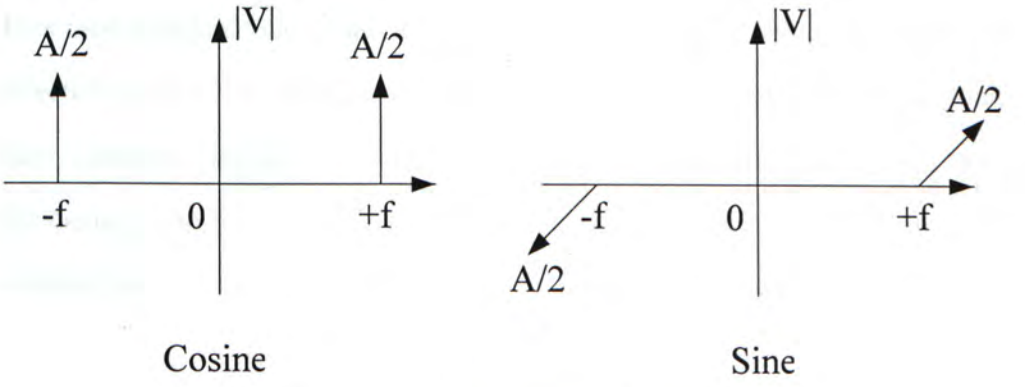


Fig. 2.13 Spectrum of Cosine and Sine

At the output of the complex converter, one path is fed into a 90 degree phase shifter again. This results in, take the simplest form, jsin(ωt), which is shown in Fig. 2.14.

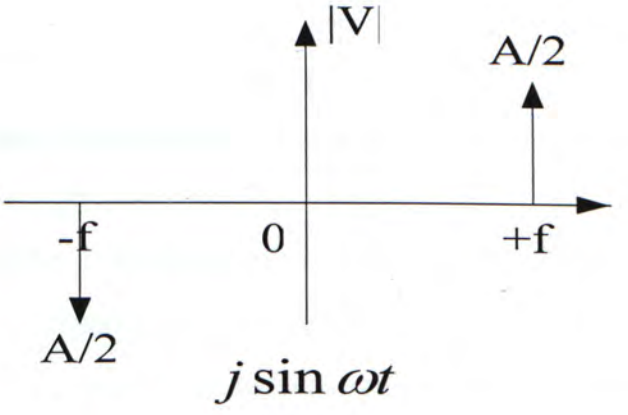


Fig. 2.14 Spectrum of jsin(wt)

Finally, the cosωt and jsinωt are summed, clearly, only positive frequency pulse is reserved, the image cancelled out. Fig. 2.15 shows the result

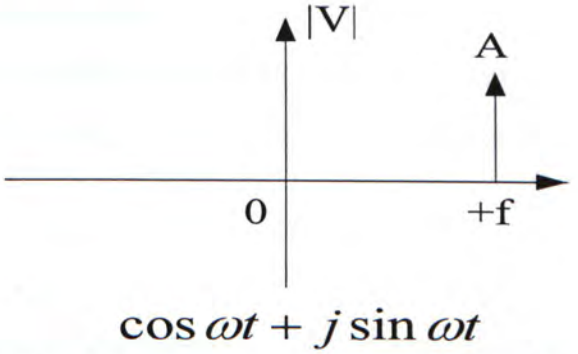


Fig. 2.15 Spectrum of cosωt + jsinωt

This nice mathematical characteristic is applied to the LO signal, thus, the LO signal effectively only have positive (or negative) pulse to convert the input signal, which have symmetry frequency information. Consequently, image signal will not corrupt the desired one any more. Fig. 2.16 shows the downconversion employing Hartley architecture

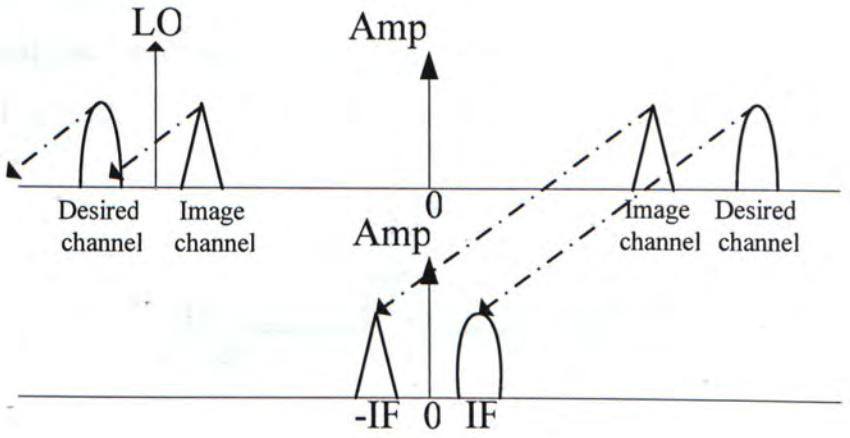


Fig. 2.16 Down Conversion of IF Signal Employing Hartley Architecture

If the complex converter is ideal, i.e., I path and Q path are identical, 90 degree phase shift is perfect, then image signal will be completely removed. But in real circuit implementation, errors can only be reduced rather than eliminated due to nonideal function blocks.

2.7. Integrated Mixer

Mixer is a three port device, the local oscillator (LO) port drives the mixer to up convert or down convert the input signal, normally RF or IF signal, to IF or baseband signal. The LO signal switches or modulates the mixer device(s). The conversion is highly nonlinear. For instance, if the device is switched between perfect on and off states,

$$V_o = V_{in}(\frac{2}{\pi}\cos(\omega t) - \frac{2}{3\pi}\cos(3\omega t) + \frac{2}{5\pi}\cos(5\omega t) + ... \quad (2.42)$$

The output will contain odd harmonics, which will introduce some error in the following signal processing, filter is needed immediately after the mixer.

There are several kinds of mixers, passive mixers, single balanced mixer, double balanced mixer, etc. Below are the brief introduction of these mixers and their pros and cons.

I: Passive Mixer

The simplest mixer is only composed of a switch, normally an NMOS transistor, with the LO signal driving the gate of the transistor, drain and source are the input IF/RF signal and output baseband/IF signal respectively. A diagram of the mixer is shown in Fig. 2.17.

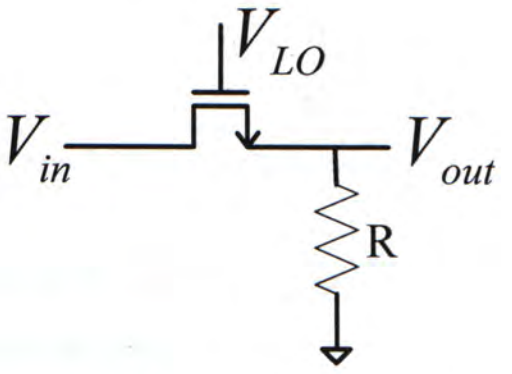


Fig. 2.17 Switching Mixer

Obviously, this kind of mixer is very easy to implement and saves much area, but equivalent resistance shown by the transistor is nonlinear and the output amplitude is

influenced by the LO signal magnitude.

II: Single Balanced Mixer

It can be built using passive components like diodes or using active components. Inductors and diodes can be combined to form a single balanced mixer, but due to the characteristic of the inductor, they are targeted mainly at high frequency application. For active single balanced mixer, on the other hand, they are more suitable for low frequency application. Fig. 2.18 shows the standard schematic of the single balanced mixer.

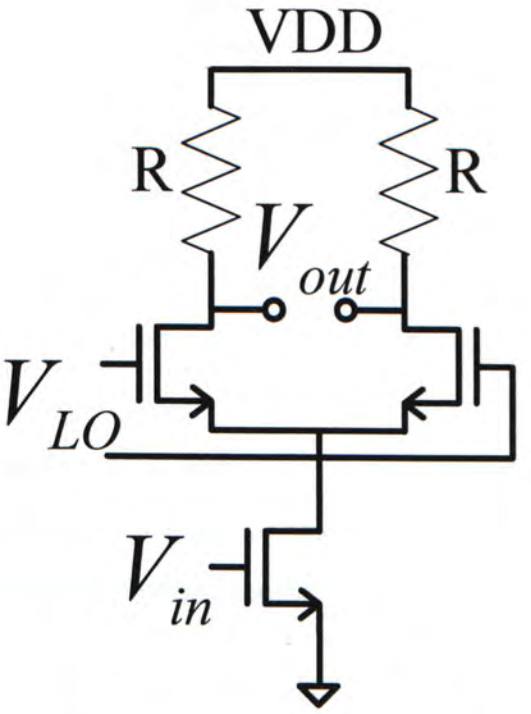


Fig. 2.18 Single Balanced Mixer

The operation principle is the same as the switching mixer. Basically, a square waveform V_{LO} modulates the input V_{in}.

III: Double Balanced Mixer

Similarly this sort of mixer can also be realized using passive components or active ones. In order to solve the problem of LO signal's impact on the output, the

following architecture in Fig. 2.19 is employed

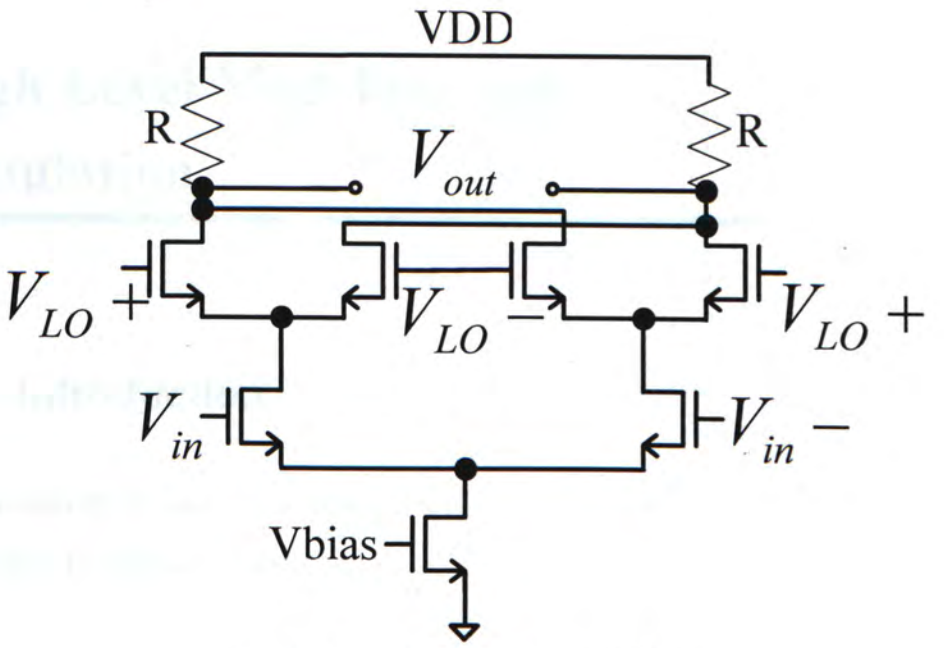


Fig. 2.19 Double Balanced Mixer

As we can analyze from the diagram, the output is immune to the amplitude of the input and LO signals. But the circuit is relatively complex.

Mixer is an important part in the design of IF input sigma delta modulator. It down converts the IF input signal to baseband for processing of the following sigma delta modulator. Detailed design issue of the adopted mixer will be discussed later.

3. Chapter 3

High Level Modeling and Simulation

3.1. Introduction

Sigma delta modulator is a complex and highly nonlinear system. Top down design is imperative for the following reasons.

First, transistor level simulation usually costs formidably long time to get reasonable amount of output samples. This is due to the mixed signal essence of the circuit and its high complexity. Though transistor level simulation can give us a relatively faithful result compared with high level simulation, it's not proper to go to this stage at the very beginning. Ideally, low level simulation functions as verification of a work that has been studied thoroughly through numerous high level modeling and simulation.

Second, it's a good practice to following the procedure of top down design since many problems can be found and resolved at high level stage, which saves us considerable time. In addition, some proposed ideas can be validated first through high level simulation, in case it fails we can think some new ideas or remedies without wasting time building the detailed circuit and doing simulation.

Third, transistor level simulation usually use spice like simulators, which has a limitation of accuracy, we can reduce the step size to increase the accuracy, but simulation time also increases accordingly. Furthermore, if we further reduce the step

size to a certain extent, the errors tend to increase [18]. On the other hand, high level simulation has much higher accuracy like using Matlab, and it's more flexible to set various options like maximal step size, algorithms, etc.

In short, as far as this design is concerned, the transistor level simulation normally takes several days for processing several periods of input signal during transient simulation. In contrast, Simulink in Matlab only needs several seconds for same amount of simulation. Though many nonidealities are difficult to be modeled in Simulink, it does provide us an intuitive understanding of the whole system and excludes ineligible candidates for us. Most importantly, it allows us to do various simulations iteratively and deliberately change certain parameters to see their influence on the overall circuit.

3.2. System Level Sigma-delta Modulator Design

In this work, Simulink of Matlab is chosen for conducting high level simulation. Because of the strong numerical power of Matlab and abundant models provided by Simulink, the tool can well suffice our needs. Before modeling the sigma delta modulator we should first and foremost design the noise transfer function of the modulator, which is of critical importance for successful implementation of the sigma delta modulator and its stable operation.

A desirable sigma delta modulator should be stable for relatively large input signal and achieves high SNR. The basic requirement for NTF of low pass sigma delta modulator is it must be a high pass one which attenuates the low frequency in band noise. The NTF can be designed using traditional Butterworth, Chebyshev or inverse Chebyshev functions. Zeros of NTF can simply be placed at DC to near optimally suppress low frequency quantization noise. On the other hand, poles of NTF should be far away from the zeros to further increase the SNR. However, this leads to

increasing magnitude at high frequency of NTF, which may result in unstable modulator as described before. Among others that we should consider in designing the NTF are, the first term h0 of the impulse response of the NTF should be equal to 1 [8], which guarantees it to be a causal system. It can be easily understood since the first output only contains quantization noise, which is assumed to be the input of NTF, the signal now at the input of the quantizer is still zero. The cutoff frequency is another concern to maximize the SNR, it's also related to the signal transfer function. The order of the NTF should be chosen carefully, the higher it is, the more quantization noise can be suppressed, but the more unstable it tends to be. In fact, low order is preferred as long as its performance can meet the requirements being set.

The inband noise power as a function of the order of the sigma delta modulator is given as [12]

$$P_{qn\_inband} \approx \frac{P_e}{M}\frac{1}{e}A^{-(L-1)} \tag{3.1}$$

P_e is the noise power before noise shaping, e is the base of natural logarithm. A is the amplification factor of the noise power after shaping. M is the OSR of the NTF. Clearly the larger the order L, the more attenuation of in band noise will result.

In fact the design of NTF is somewhat arbitrary [19], we finally turn to the excellent toolbox developed by Richard Schreier [20], which is embedded into Matlab. It can help us generate the noise transfer function of specified order and oversampling ratio. The out of band gain of the NTF thus generated is set to be 1.5, which is a quite optimal value based on past experience [8]. After obtaining the NTF, SNR can be calculated in this way.

$$\begin{aligned} P_{qn\_inband} &= \frac{P_e}{2\pi}\int_{-\pi/R}^{\pi/R} |NTF(e^{j\omega})|^2 \, d\omega \\ P_{signal} &= V_{\max}{}^2/2 \\ SNR_{\max} &= P_{signal}/P_{qn\_inband} \end{aligned} \tag{3.2}$$

Take a first order sigma delta modulator as an example, the characteristic equation in terms of input signal and quantization noise is

$$Y(z) = z^{-1}X(z) + (1 - z^{-1})Q_n(z) \tag{3.3}$$

The shaped in band quantization noise is derived as follows, first the magnitude of the NTF:

$$\begin{aligned} |H_Q(f)| &= |(1 - z^{-1})(1 - z)|^{1/2} \\ &= |(1 - e^{-j2\pi fT_s})(1 - e^{j2\pi fT_s})|^{1/2} \\ &= |2 - 2\cos(2\pi fT_s)|^{1/2} \\ &= 2\sin(\pi fT_s) \end{aligned} \tag{3.4}$$

The quantization noise before noise shaping is assumed to be white, thus in band noise power

$$\begin{aligned} S_{qn\_inband} &= \int_{-f_B/2M}^{f_B/2M} |H_Q(f)|^2 \times \frac{\Delta^2}{12 f_s} df \\ &\approx \frac{\pi^2 \Delta^2}{36 M^3} \end{aligned} \tag{3.5}$$

Where $M = f_s / 2f_B$ is oversampling ratio, the approximation $\sin \pi fT_s \approx \pi fT_s$ is employed because normally M>>1.

Finally the maximum SNR or dynamic range can be obtained

$$DR = \frac{S_{signal}}{S_{qn\_inband}} \approx \frac{\Delta^2 / 8}{\pi^2 \Delta^2 / 36 M^3} = \frac{9M^3}{2\pi^2} \tag{3.6}$$

It indicates that the dynamic range increases 9dB in the first order modulator for every octave increase of OSR M, while modulator only employing oversampling technique has only 3dB improvement for double of M.

Generally, for Lth order sigma delta modulator, its dynamic range can be calculated in a similar way as that of first order one. Below gives the formula

$$DR \approx \frac{3}{2}\left(\frac{2L+1}{\pi^{2L}}\right) M^{2L+1} \tag{3.7}$$

It reveals that increasing the order will enhance the dynamic range exponentially.

Knowing the relationship between the OSR, Order, and DR, the choice of OSR and order is facilitated for specified DR requirement. In this work, since dynamic range is not the main objective of the design, we initially set it to be 80dB. Various high level simulations are conducted with the aid of aforementioned sigma delta toolbox and Matlab. OSR of 128 is chosen not only for high attenuation of in band quantization noise, but also for lowering the in band jitter noise, thermal noise etc. Sigma delta modulators with order 1 to 5 are simulated to get their theoretical SNRs. Fig. 3.1 shows the diagram with reference to the input amplitude.

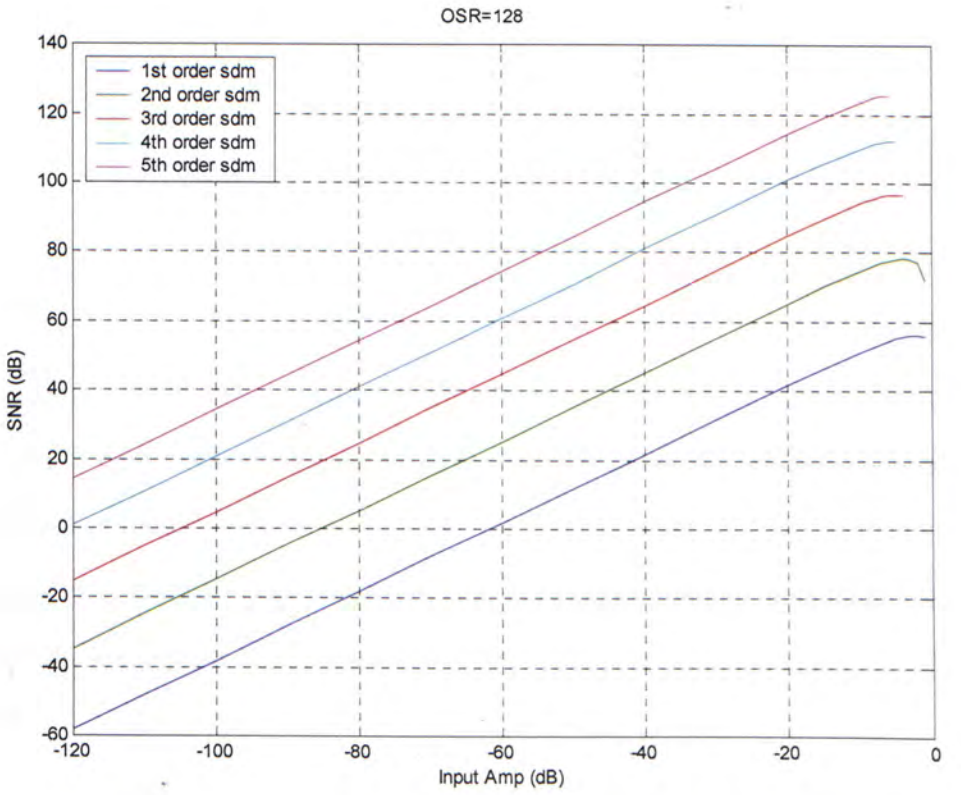


Fig. 3.1 SNR versus Input Amplitude for Different Order SDMs

It shows that the third order sigma delta modulator with OSR of 128 can achieve maximal SNR of over 90dB. We further investigated the performance of third order sigma delta modulator with different OSRs, which is indicated in the following Fig. 3.2.

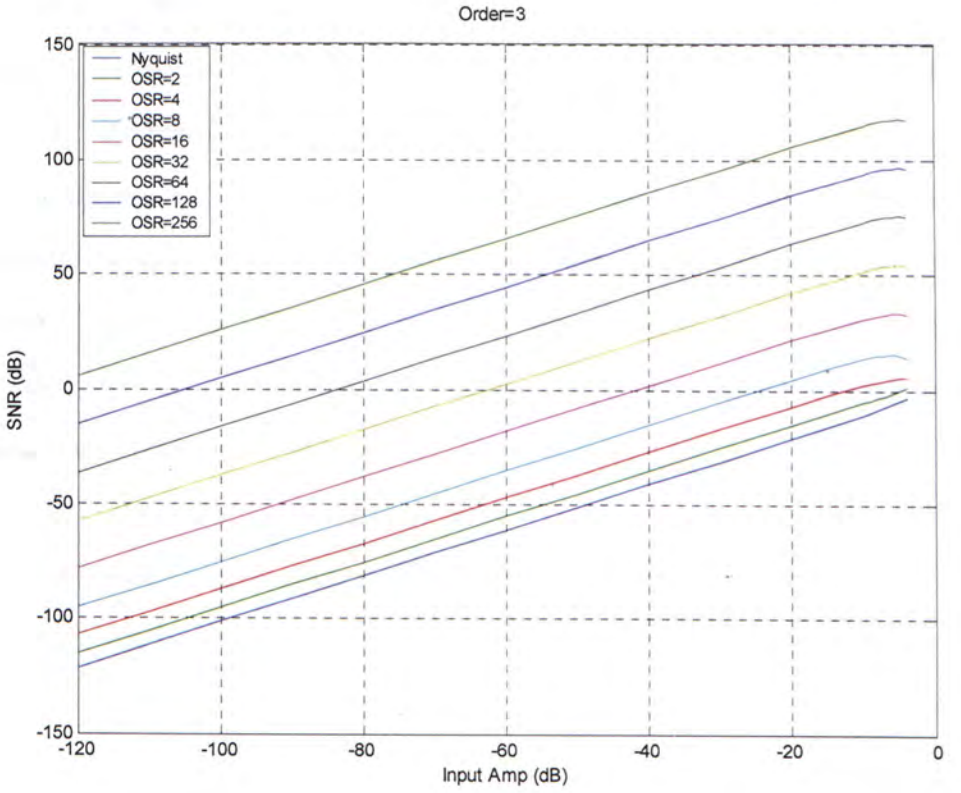


Fig. 3.2 SNR versus Input Amplitude for Different OSRs

It reveals that third order modulator with OSR of 64 can only obtain around 75dB SNR, while with OSR of 256 the SNR can well exceeds 100dB. It also reveals that these kinds of modulators are not suitable for low oversampling. Because the internal quantizer are relative coarse, often with only 1 bit. After extensive high level simulation, third order sigma delta modulator with an oversampling ratio of 128 is chosen.

Next, the choice of structure of the sigma delta modulator is carried out. Sigma delta modulator mainly falls into two categories, the widely used and basic structure is single loop or single stage one. A general diagram and its characteristic equation have already been given early in this thesis. Another type of sigma delta modulator is called cascade modulators or multi-stage, MASH [21,22]. This kind of modulator are normally cascaded with several first order or second order single loop sigma delta modulator, thus their stabilities can be guaranteed, In addition, the quantization noise produced by one stage is modulated again by the subsequent stage and so on. Finally

the quantization noise is cancelled to a large extent in digital domain. Though this structure is robust and can achieve high SNR by cascading several single loop modulators, its performance is based on the good matching of different stages, otherwise incomplete cancellation will result in digital processing. Continuous time sigma delta modulators are difficult to achieve good matching of related resistors, integrators, etc. Thus, they are basically not suitable to be implemented in multi-stage architecture. Therefore we will not analyze the detailed working principle of multi-stage sigma delta modulator.

For a single stage sigma delta modulator we can adopt feedback or feedforward architecture. The basic forms are shown in Fig.3.3 and Fig.3.4 respectively

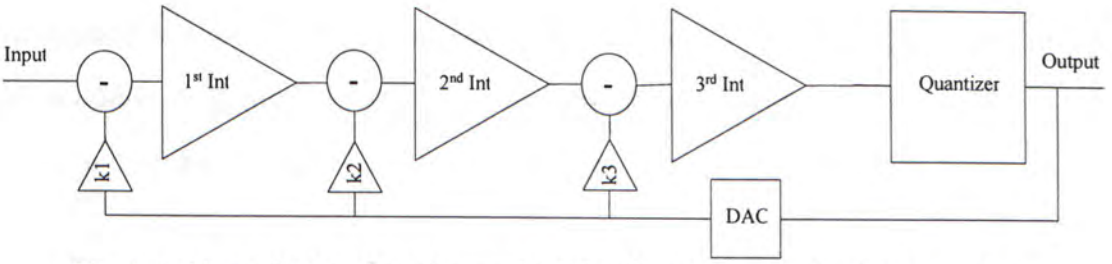


Fig. 3.3 Sigma Delta Modulator with Distributed Feedback Compensation

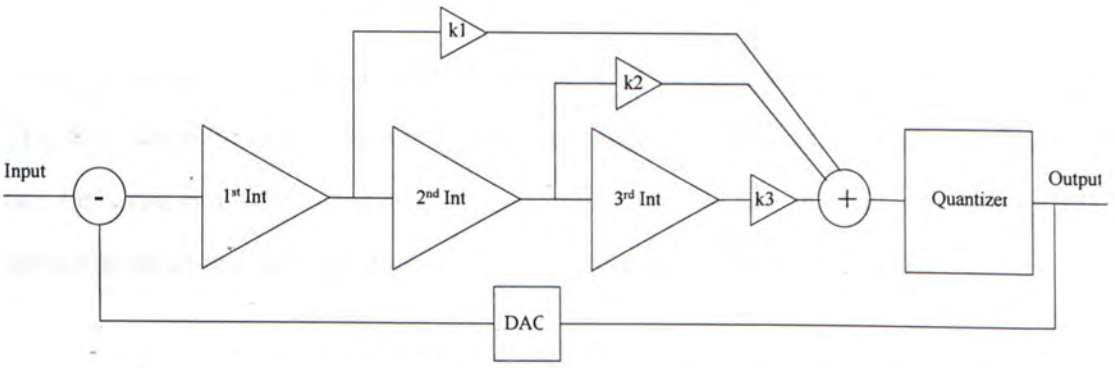


Fig. 3.4 Sigma Delta Modulator with Feedforward Compensation

The multi-feedback or feedforward paths are employed to establish proper noise transfer function and compensate the sigma delta modulator, otherwise it will be unstable. Both schemes have their cons and pros, sigma delta modulator employing multi-feedback tends to be more sensitive to noise in the internal loop, because

signals distribute at each of the stages' output, thus, the gain of each integrator cannot be too large to avoid signal saturation distortion. This results in less attenuation of the internal errors. The modulator with feedforward compensation on the other hand doesn't experience such problem, besides, it's less sensitive to integrator's linearity [23], this architecture is thus adopted in our design.

Other architecture like cascade of resonator instead of integrator is not chosen in our design because it makes the system more complex and more sensitive to various parameters, though they increase the SNR by placing some zeros near the signal band edge to achieve more noise suppression.

In summary, after iterative high level simulation as well as due to the characteristics of various architecture of sigma delta modulator, we choose to design a third order sigma delta modulator with feedforward compensation, whose OSR is 128. This module functions as a baseband analog to digital converter in our whole design.

3.3. Continuous-time NTF Generation

There are generally two approaches to design continuous time sigma delta modulator. The first one is to design directly based on general topologies, the transfer function can be write out with some coefficients which are to be set. The coefficients are chosen to meet the requirements of in band attenuation, out of band gain, etc.

The other approach to design continuous time modulator is to transform from a discrete time sigma delta modulator counterpart. Discrete time sigma delta modulator has been well studied and numerous software been developed to facilitate the design [24]. Every continuous time sigma delta modulator has an exactly equivalent discrete time one. Because a continuous time delta sigma modulator has a discrete time component quantizer inside the loop, if we take the output of the quantizer as an

input to a black box, and the output of the black box is the input of the quantizer, the black box can be expressed using discrete time transfer function due to the fact that the input and output of the black box are discrete signals. In short, they can be guaranteed to be identical because they share the same input and output. The diagram is shown in Fig. 3.5 to illustrate this.

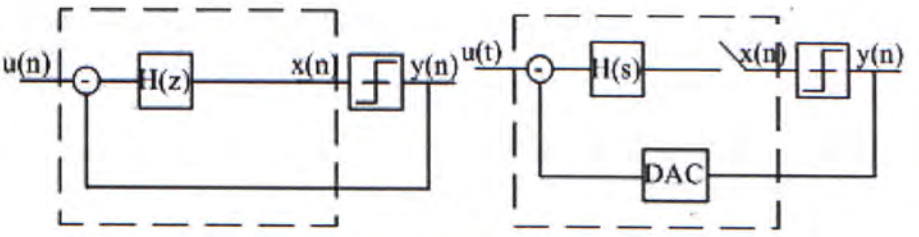


Fig. 3.5 Equivalence between DT and CT SDM

The well known mapping relations between the s-domain and z-domain of this circuit is

$$H(z) = Z[L^{-1}[DAC(s) \times H(s)]|_{t=nT}] \tag{3.8}$$

This formula assumes that the input signals of discrete time modulator and continuous time modulator are identical, which requires that the continuous time input is sampled before entering the system.

For the second approach, there are some other methods to transform the discrete time sigma delta modulator to its equivalent continuous time one. We will introduce them briefly here.

I: State Space Equation Equivalent

We can describe the discrete time sigma delta modulator using state space equations, then find its continuous time counterpart, finally circuit based on the continuous time state space equations can be built up [25]. The state space equations for continuous time and discrete time sigma delta modulators are

$$x_c' = A_c x_c + B_c \begin{bmatrix} u_c \\ v_c \end{bmatrix}$$
$$x(n) = Ax(n-1) + B \begin{bmatrix} u(n-1) \\ v(n-1) \end{bmatrix} \tag{3.9}$$

II: Bilinear Transformation

This method is based on the relation that

$$z = e^{sT} \tag{3.10}$$

Thus

$$Z = e^{sT} = \frac{e^{\frac{sT}{2}}}{e^{\frac{-sT}{2}}} \cong \frac{1+\frac{sT}{2}}{1-\frac{sT}{2}} = \frac{2+sT}{2-sT} \tag{3.11}$$

Since mapping between s-domain and z-domain is nonlinear, prewarping is needed to indicate an exactly mapped frequency.

$$R = \frac{2}{T}\tan\frac{\omega_c T}{2} \tag{3.12}$$

ω_c is the matched frequency.

In this work, discrete time sigma delta modulator's NTF is first generated using sigma delta toolbox developed by Richard Schreier, then transformation to continuous time counterpart is conducted by utilizing a Matlab function d2c.

There are several methods provided by that function to perform transformation, including zoh which stands for zero order hold, bilinear with or without prewarping and zero pole matching. Bilinear transformation is essentially nonlinear thus introduce substantial errors, besides, a constant is induced after transformation, which entails additional circuitry. Matched zero pole conversion and aforementioned impulse response invariant method will result in complicated continuous time transfer function. Zero order hold is chosen and applied not to the conversion of NTF

but to the loop filter H(z). It is thought that by adopting this method, we can rather faithfully convert the discrete time loop filter function H(z) to H(s). The only minor error is that zero order hold is assumed, the zero order held input signal is not identical with the real continuous time input. Fortunately, since the sampling frequency of sigma delta modulator is very large compared with the input signal, and the feedback signal is essentially digital where zero order hold doesn't introduce any error, thus the difference between the obtained continuous time modulator and discrete time modulator is minimal. Simulation results show good matching about the performance of those corresponding sigma delta modulators.

For a third order discrete time sigma delta modulator with OSR of 128, we obtain the noise transfer function using Schreier's toolbox which is given below

$$\frac{(z-1)^3}{z^3-2.2002z^2+1.6886z-0.4444} \tag{3.13}$$

Since

$$NTF=\frac{1}{1+H(z)} \tag{3.14}$$

Then transfer function of the loop filter is

$$H(z)=\frac{0.7998z^2-1.3114z+0.5556}{(z-1)^3} \tag{3.15}$$

By applying zero order hold transformation, we get

$$H(s)=\frac{0.6704s^2+0.2442s+0.044}{s^3} \tag{3.16}$$

This loop filter transfer function is well suited for sigma delta modulator implementation with feedforward compensation. We can rearrange H(s) to

$$H(s)=\frac{0.6704}{s}+\frac{0.2442}{s^2}+\frac{0.044}{s^3} \tag{3.17}$$

The three numerators are the feedforward coefficients we want. Note that this transfer function is normalized to sampling frequency 1Hz. Fig. 3.6 shows the derived NTF.

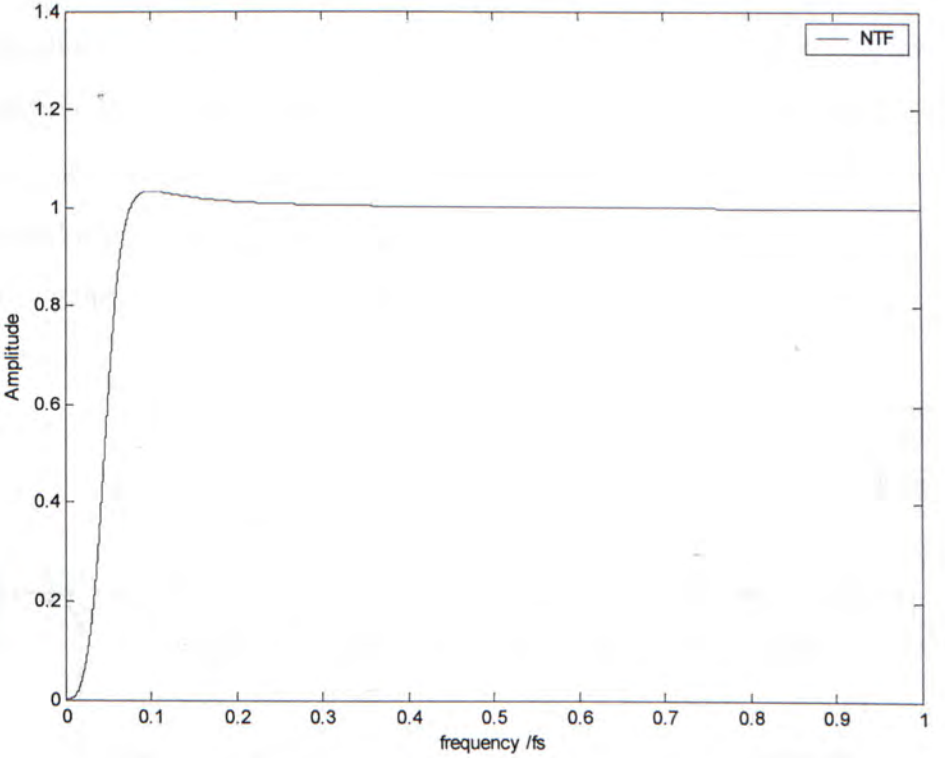


Fig. 3.6 Noise Transfer Function of This Design

3.4. Discrete-time Sigma-delta Modulator Modeling

In the following several sections, modeling of sigma delta modulator using Simulink will be given, their simulation results are presented as well.

Discrete time sigma delta modulator is well suited for modeling using Simulink because the simulator is based on digital signal processing. Simulink is a software package for modeling, simulating, and analyzing dynamic systems. It supports linear and nonlinear systems, modeled in continuous time, sampled time, or a hybrid of the two. Simulink provides a graphical user interface (GUI) for building models as block diagrams, it also allows user to create new blocks.

In order to model the sigma delta modulator, we need to split the system into various components and employ the available blocks in Simulink. For those function blocks

that are not provided by Simulink we should build them up by ourselves. The basic building block of discrete time modulator is discrete time integrator, which realizes the function 1/(z-1). The coefficients can be implemented using gain blocks, Sine wave source is adopted to be fed into the sigma delta modulator, and transient output of the modulator is saved to workspace as an array. Besides, scope is very useful in monitoring the waveform at any node. The whole architecture is shown in Fig. 3.7.

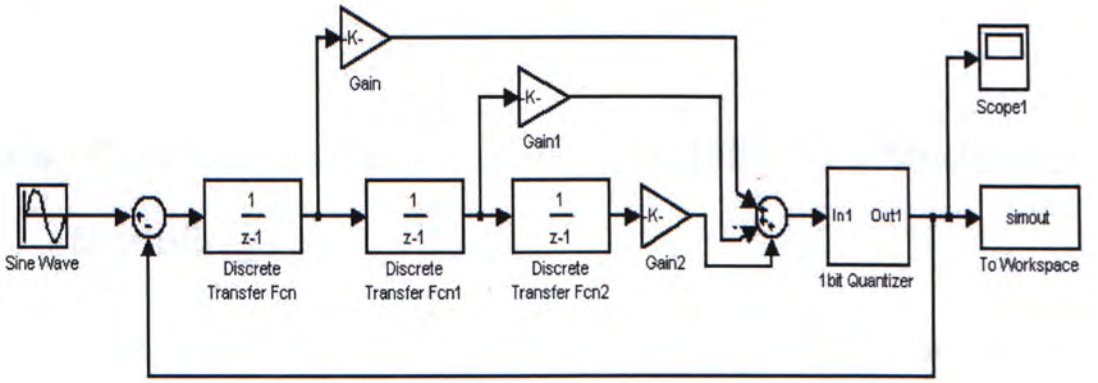


Fig. 3.7 Model of Third Order DT SDM

The two level quantizer is built up using several sub blocks. Fig. 3.8 shows the diagram

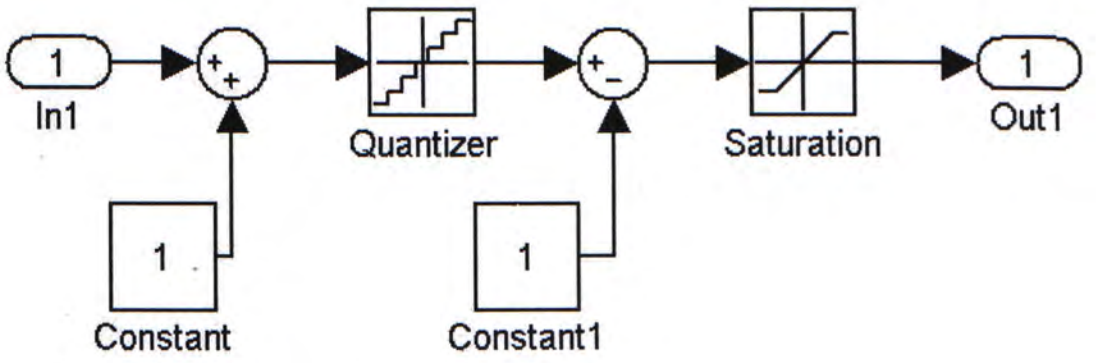


Fig. 3.8 Model of Quantizer

The input signal is first added with a constant 1, then fed into a multilevel quantizer with interval 2, thus all input less than 0 will get an output 0 all smaller level, while input with value larger than 0 will get an output 2 or larger level. After being subtracted by 1 and going through a saturation block, the whole subsystem acts

exactly as a 1 bit quantizer.

The 1 bit quantizer can also be implemented with a simple block named sign. Though this block will produce output 0 in case that the input is 0, it will not affect the performance of the sigma delta modulator, because it's virtually impossible for the loop filter to generate an exact zero with complicated input. Another method to implement the quantizer is using the block relay, which can serve the needs as well.

3.5. Continuous-time Sigma-delta Modulator Modeling

The continuous time sigma delta modulator is similar in modeling as that of discrete time one. The major difference is the building block integrator is continuous time one, that is, the integrator is implemented in s-domain instead of z-domain. Besides, an internal sampler is needed to sample the continuous time signal. A triggered subsystem is needed to perform the function of sampling. The whole architecture is given in Fig. 3.9.

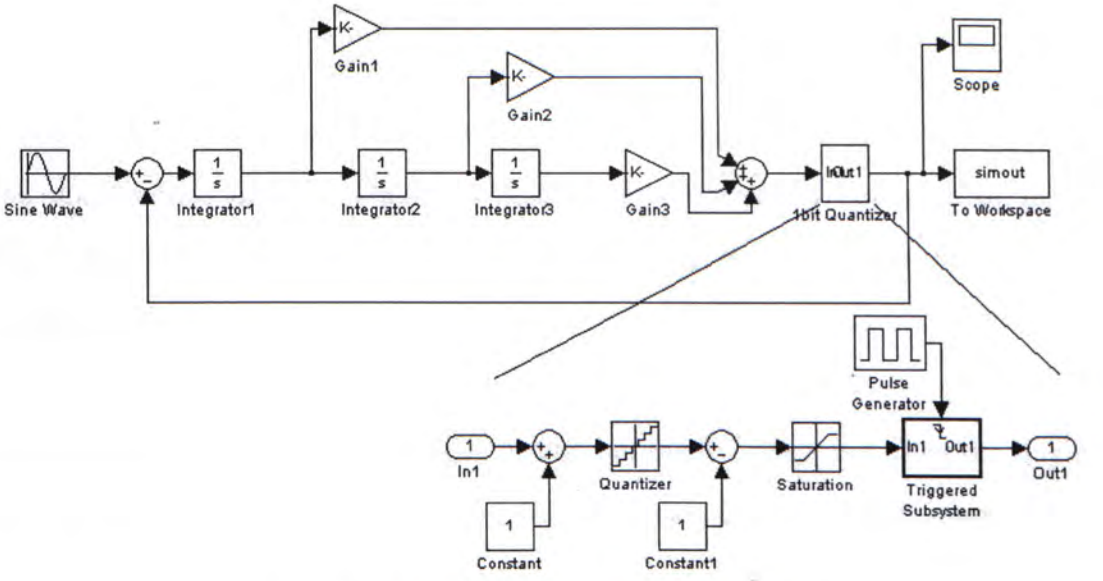


Fig. 3.9 Model of Third Order CT SDM

The coefficients are different from those of discrete time one, and the pulse generator sets the sampling frequency of the continuous time sigma delta modulator.

3.6. Modeling of Nonidealities

Up to now we modeled the general sigma delta modulator, be it continuous time or discrete time one. Several nonidealities of the system should also be considered to give a more accurate modeling. In this section, the finite output swing of OTA, finite OTA gain, settling time, Clock jitter and thermal noise are briefly modeled in order to give us a general idea about the effect of those nonidealities.

An OTA has finite gain and bandwidth, we can use a single pole model to represent the OTA.

$$H_{OTA}(s) = \frac{A}{1 + s/\omega_p} \tag{3.18}$$

A is the finite DC gain, ω_p denotes the pole of the OTA. This model can describe the OTA well for single stage OTA because they normally only have one major pole

at the output. The second pole is far away from the unity gain bandwidth.

Since continuous time sigma delta modulator is adopted in this work, we will analyze the nonidealities only in s-domain. First stage as described before is of most importance for good overall performance. Thus the first RC integrator will be emphasized in analyzing these effects.

First we directly write out the transfer function of the RC integrator using the single pole model, which is shown in Fig. 3.10. The derivation is very straightforward

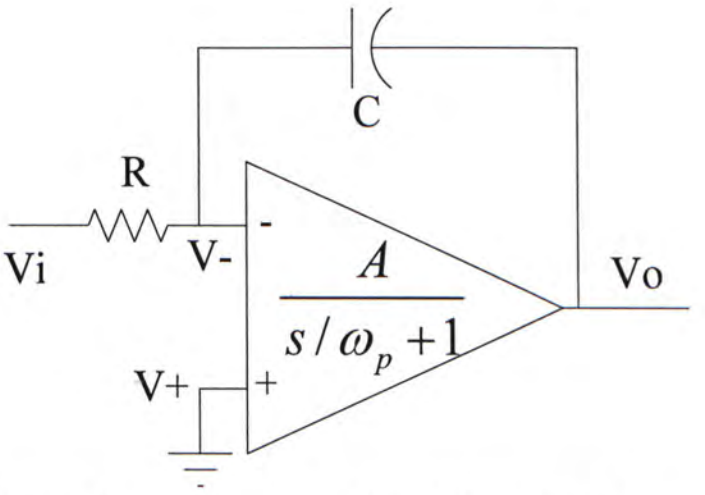


Fig. 3.10 RC Integrator Using None Ideal Opamp

$$\frac{V_{in}(t)-V_{-}(t)}{R}=C\frac{d(V_{-}(t)-V_{out}(t))}{dt} \tag{3.19}$$

$$V_{out}(s)=V_{-}(s)\frac{-A}{1+s/\omega_p} \tag{3.20}$$

By applying laplace transformation at both sides of equation, solving two equations we can get the final transfer function

$$\frac{V_{out}(s)}{V_{in}(s)}=\frac{-A\omega_p}{RCs^2+((A+1)RC\omega_p+1)s+\omega_p} \tag{3.21}$$

Replacing the first ideal integrator model 1/s with this one, the finite gain and bandwidth of a real OTA can be modeled.

The second way to model the RC integrator employing real OTA is more direct, i.e., use the circuit model shown below in Fig. 3.11.

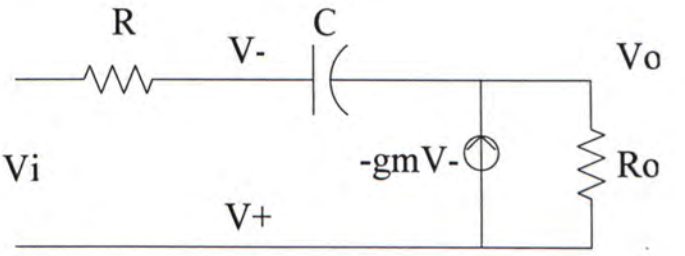


Fig. 3.11 Simple Model of RC Integrator

The OTA converts its input V- into current g_m V-. R_o is the output impedance of the OTA. Some parasitic capacitors are omitted for simplicity. The corresponding transfer function is derived below, suppose reference V+ is 0.

$$\frac{V_i - V_-}{R} = g_m V_- + \frac{V_o}{R_o} = C\frac{d(V_i - V_o)}{dt} \tag{3.22}$$

By solving these two equations, we finally get

$$H(s) = \frac{V_o(s)}{V_i(s)} = \frac{R_o Cs - g_m R_o}{(R_o C + RC(1 + g_m R_o))s + 1} \tag{3.23}$$

Where $g_m R_o$ equals the gain of the OTA.

In the model shown in Fig. 3.11, we omitted the loading capacitor in light of the real situation where only parasitic loading exists, which is neglectable compared with the integrating capacitor. Now we'd like to analyze the model with a loading capacitor to get a deeper understanding. The third model diagram is shown in Fig. 3.12.

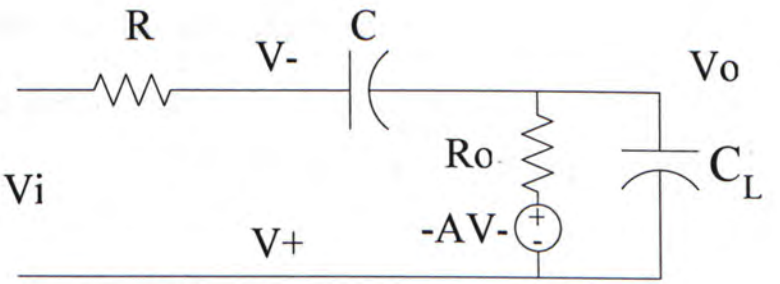


Fig. 3.12 Practical Model of RC Integrator

We can write out the transfer function of this model with the aid of KCL.

$$\frac{V_i - V_-}{R} = C\frac{d(V_- - V_o)}{dt} = \frac{AV_-}{R_o} + \frac{V_o}{R_o} + C_L\frac{dV_o}{dt} \tag{3.24}$$

$$H(s) = \frac{V_o(s)}{V_i(s)} = \frac{R_oCs - A}{R_oRC_LCs^2 + (RC + ARC + R_oC + R_oC_L)s + 1} \tag{3.25}$$

Compare equation (3.25) with equation (3.21), we find that the two models do not match, though the third model is also based on single pole modeling. The first model is not valid, at least, conceptually. Because now $V_o \neq \frac{-A}{sR_oC_L + 1}V_-$, instead, $V_o = \frac{R_oCs - A}{R_o(C_L + C)s + 1}V_-$. This is due to the feedback circuitry imposed on the OTA. The result shows that in addition to that the loading value is changed, a zero is introduced as well. Some past works normally adopt the first model, actually the third model analyzed here is the faithful one to model the nonidealities of the RC integrator.

If C_L is zero, the transfer function can be reduced to equation (3.23), where no OTA loading C_L is included. If output impedance R_o is also set to zero, the function reduces to

$$H(s) = \frac{-A}{(A+1)RCs + 1} \tag{3.26}$$

which is the model when only finite gain of OTA is considered. This transfer function can also be derived using the widely used finite gain model shown in Fig. 3.13. But note that the deduction based on the model in Fig. 3.13 is never true for an OTA, because OTA has very large output impedance R_o. R_o simply cannot be ignored. This transfer function has been misused in some past work where OTA is adopted.

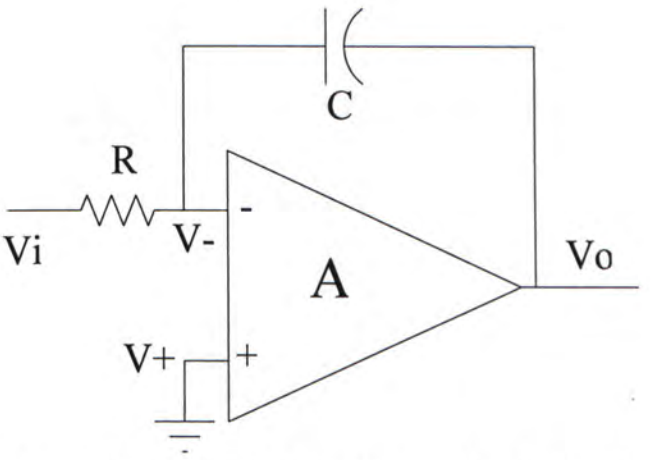


Fig. 3.13 Model of RC Integrator with Finite Gain Opamp

Simulation results comparison of the first and third models will be given in next section.

For finite swing of OTA, a simple saturation block is added to the output of each integrator, the upper and lower bound can be set freely according to the output swing of practically designed OTA. Though the method is simple straightforward, we should set stringent requirement of the output swing of OTA, since the smaller the signal swings at the output of OTA, the more linear it is.

The effect of thermal noise and jitter can be regarded as the consequence of a constant noise source at the input. The input resistor in the first stage contributes most to the input referred thermal noise, clock jitter noise is roughly derived in the previous context. Thermal noise can be calculated using the equation $\overline{v^2} = 4kTRB$ as mentioned before.

For illustration of the effects of thermal noise and jitter, let's take an example here. Suppose a continuous time sigma delta modulator has sampling frequency 10MHz, oversampling ratio is 128, which means the signal band is about 40kHz. We also assume that τ which denotes the range that clock edge varies within is 0.1 percent of one clock period, that is, $(1\times10^{-3})\times(1\times10^{-7})=1\times10^{-10}$(s). Input resistor has a large

value of 100kohm. V_{ref} is simply 1. Then we can obtain approximately the input referred noise source in root mean square value.

$$\bar{v}_{thermal} = \sqrt{4kTRB} \approx 8.1\times10^{-6}(V)$$

(3.27)

$$\bar{v}_{jitter} = \sqrt{\frac{8(V_{ref}\tau\pi f_b)^2}{9OSR}} \approx 1\times10^{-6}(V)$$

(3.28)

They are uncorrelated noises, so we totally get 9.1×10^{-6}(V) equivalent noise source at the input. This set the maximum SNR we could possibly get, suppose largest magnitude of input signal is half of V_{ref}

$$SNR_{\max} = 20\log\frac{(V_{ref}/2)/\sqrt{2}}{V_{noise}} \approx 92dB \qquad (3.29)$$

For continuous time sigma delta modulator, jitter and thermal noise are often the most significant noise source, especially for those adopting RC integrator.

3.7. High Level Simulation Results

In this section, simulation settings and results will be given for the models built up in previous sections. For the purpose of illustration, only 4096 output points are taken. Their SNRs are calculated for comparison.

For the discrete time sigma delta modulator model given in Fig. 3.7, the input frequency of sine wave is set to be 2* π /512 rad/s, amplitude is 0.5 while feedback reference is 1. The sampling frequency of the modulator is normalized to 1Hz. The feedforward coefficients are obtained according to the relationship of NTF and loop filter transfer function. They are 0.7998, 0.2882, 0.044 respectively. Simulation time is from 0 to 4096, fixed step solver is selected for simulation of this discrete time modulator. The output spectrum from 4096 output points is shown in Fig. 3.14.

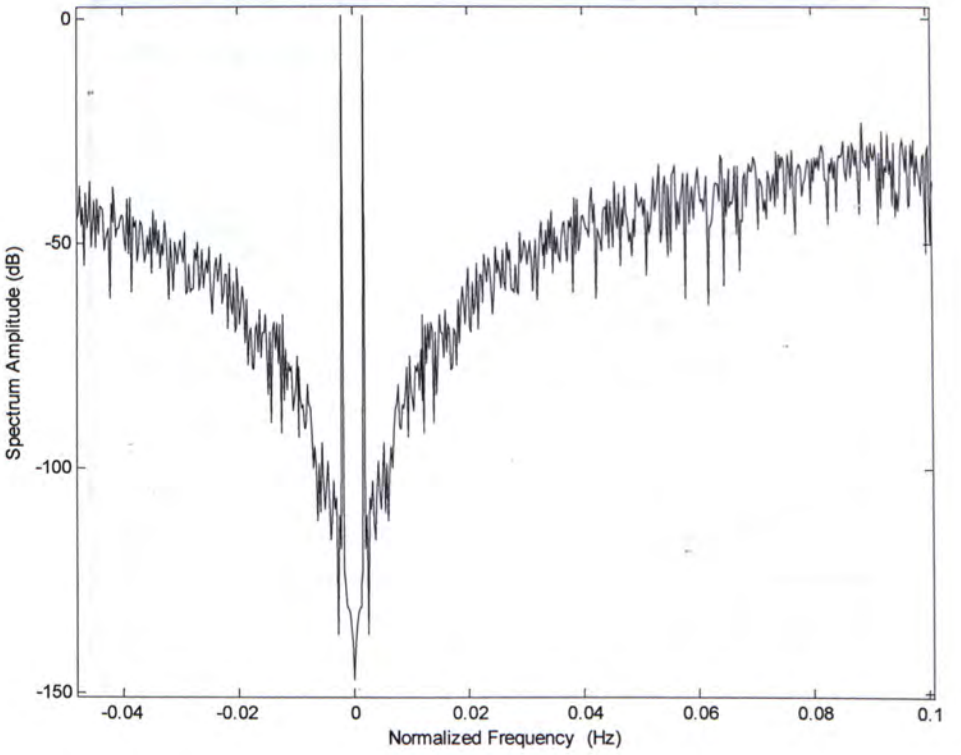


Fig. 3.14 Output Spectrum of the Modeled DT SDM

SNR is calculated assuming out of band noise is ideally filtered out. In this case, the SNR equals 100.6dB.

For continuous time sigma delta modulator model shown in Fig. 3.9, similar setting is given except those of simulation options. Variable step solver is selected, the method for solving differential equation is ode45 (Dormand-Prince). Relative tolerance should be set small enough to get accurate simulation result, though at the cost of simulation time. Besides, the output option should use 'produce specified output only' for this mixed mode system. The window for setting simulation options is extracted below in Fig. 3.15. Feedforward coefficients, as calculated before, are 0.6704, 0.2442, 0.044 respectively. Spectrum of the simulation result of this continuous time modulator is given in Fig. 3.16.

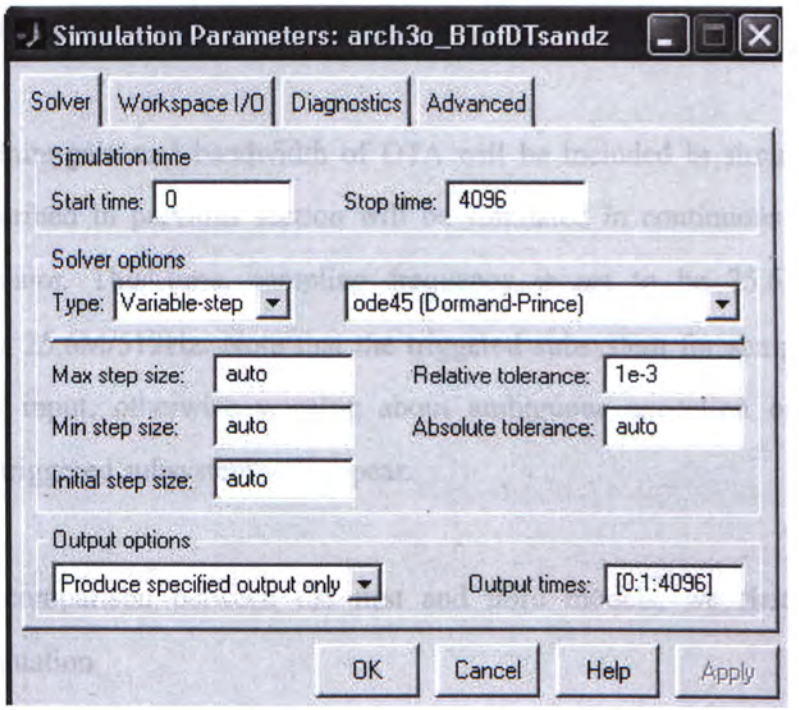


Fig. 3.15 Settings For CT SDM Simulation in Simulink

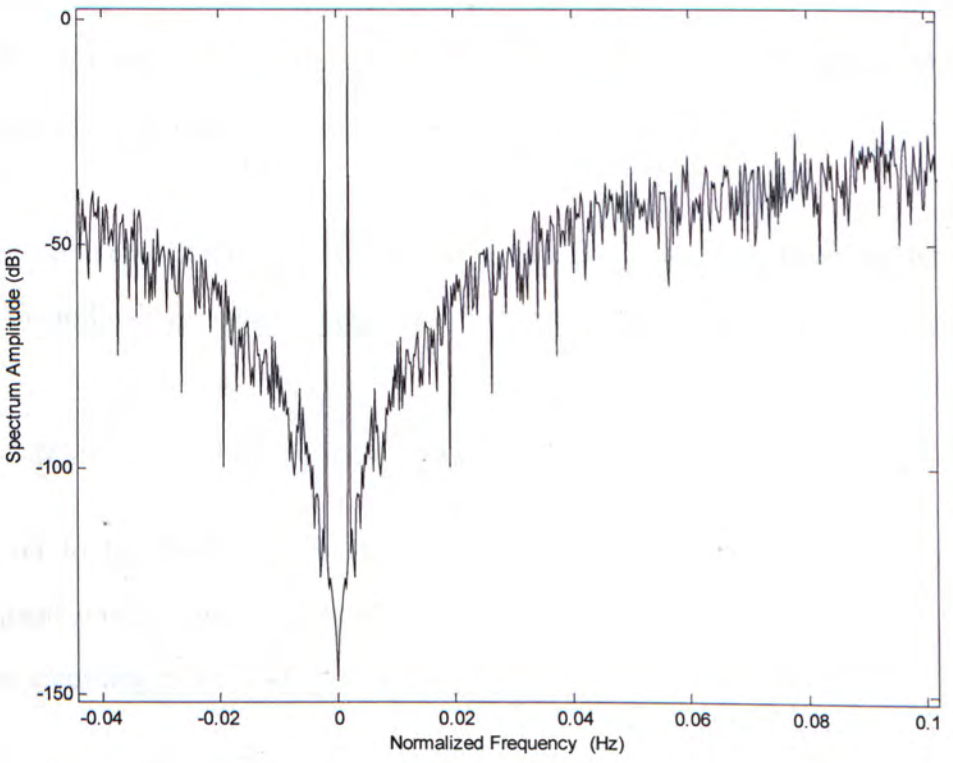


Fig. 3.16 Output Spectrum of the Modeled CT SDM

The corresponding SNR is 101.6dB within the band of interest. It's very close to the discrete time sigma delta modulator counterpart. This also corroborates that the

transformation method we propose is very effective.

Next, the finite gain and bandwidth of OTA will be included in simulation. Both models described in previous section will be simulated in continuous time sigma delta modulator. This time, sampling frequency is set to be 25.6MHz, input frequency is 25.6M/512Hz. Note that the triggered subsystem for sampling should use latched input, otherwise warning about ambiguous execution order due to nonlatched triggered subsystem will appear.

For better comparison between the first and third models, we first utilize the following equation

$$R_o = \frac{1}{\omega_p C} \tag{3.30}$$

Note that here ω_p is not the real pole of the transfer function. Without losing generality, it is assumed that these two models use an identical OTA, whose pole lies at ω_p with loading capacitor C. So equation (3.30) holds.

Replace Ro in equation (3.25) with the above equation, after some manipulations, we obtain the following transfer function for the third model.

$$H(s) = \frac{s - A\omega_p}{RC_L s^2 + ((A+1)RC\omega_p + 1 + \frac{C_L}{C})s + \omega_p} \tag{3.31}$$

C_L is set to be 200fF, which approximately models the parasitic capacitors of subsequent stages' input transistors. C is assumed to be 1pF, R can be calculated as follows according to the NTF of this design

$$R = \frac{1}{Cf_s} = \frac{1}{10^{-12}10^7} = 10^5\,\Omega \tag{3.32}$$

Now we have two free parameters gain A and dominant pole frequency ω_p which features a real OTA. First we fix ω_p to 2π*10k rad/s, A is swept from 100 to 10000. Simulation result is given in Fig. 3.17.

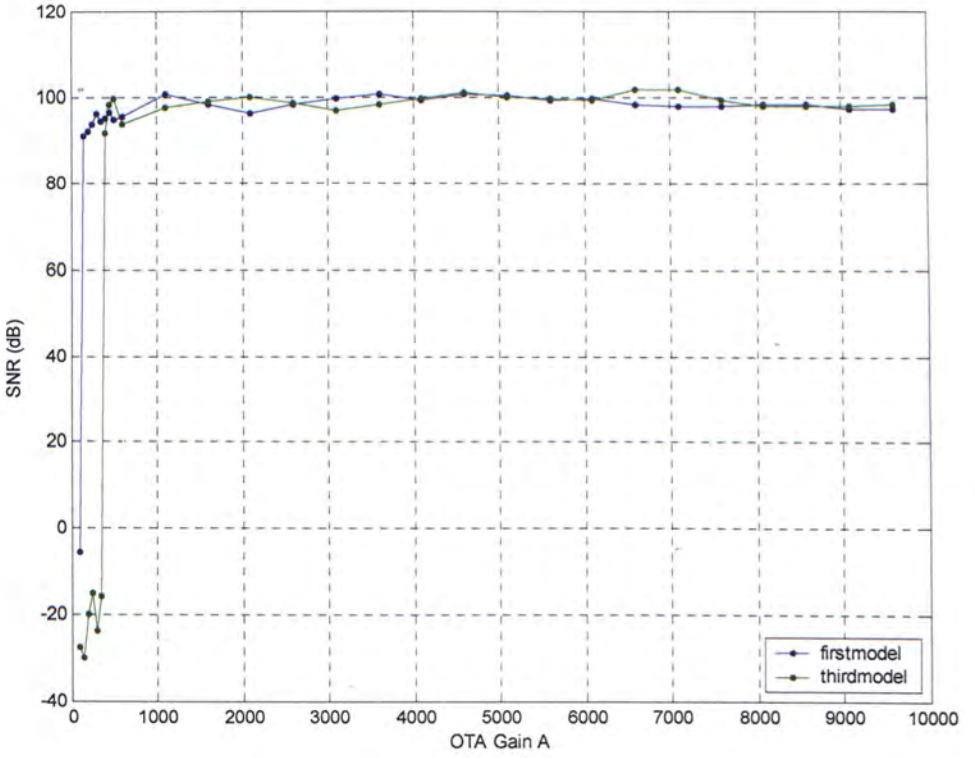


Fig. 3.17 Simulation Result for 1st and 3rd Models with Different Gains

Judging from the simulation result, the SNR degrades sharply when OTA gain A is around 100 for first model, while for the third model, the critical point of gain is about 400. Further simulation and observation reveal that the sigma delta modulator becomes unstable below these certain gains, i.e. the quantizer is overloaded and the output shows repeated long sequence of 1s and 0s. For both cases, when the gain is above the critical point, performance of sigma delta modulator doesn't degrade considerably as gain decrease. This is because sigma delta modulator is very tolerant to finite OTA gain, take a first order sigma delta modulator for example, as long as the OTA gain A>OSR/ π , the SNR degradation is very little. This can be easily derived by writing out the NTF. In the above cases, even gain 100 is much greater than 128/ π , thus it's sensible to see little performance variance above these critical points. What we should be cautious of is too little gain may result in unstable sigma delta modulator, as observed in this case. The first model is absolutely more optimistic in predicting the performance for different OTA gains. The third model, which is the correct one, as analyzed before, shows us a much higher critical OTA

gain. None the less, the latter is more credible.

Next, OTA gain is fixed to 1000, ω_p is swept from 2π*1k to 2π*10k rad/s. Fig. 3.18 gives the simulation result

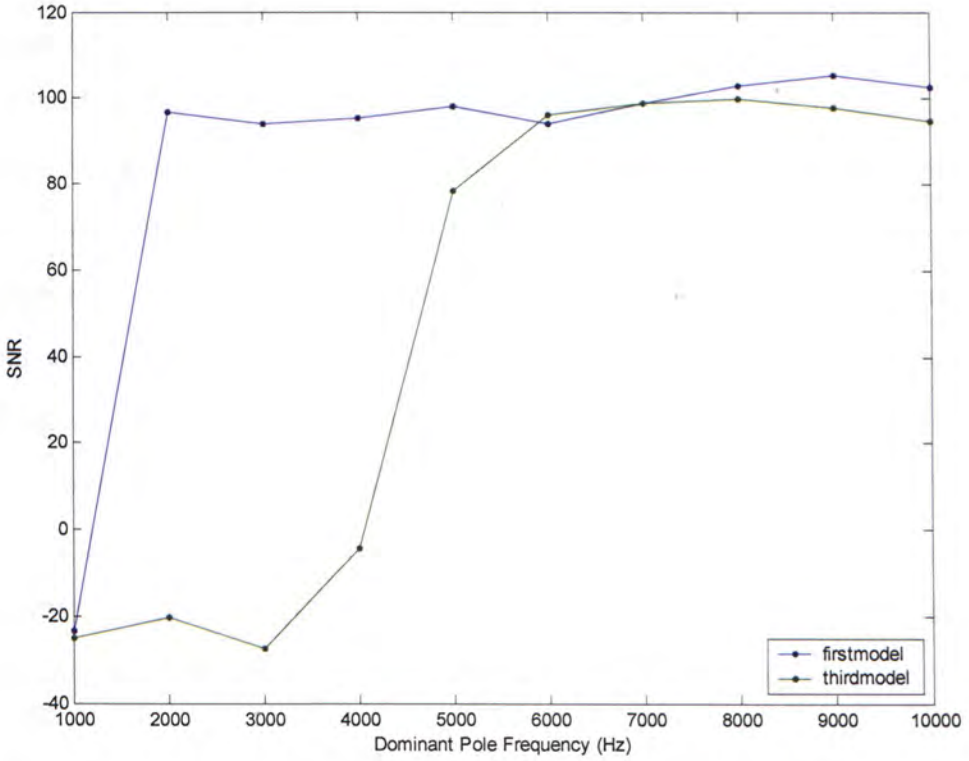


Fig. 3.18 Simulation Result for 1st and 3rd Models with Different ω_p

Again the third model shows a much higher frequency below which performance degrades sharply. Further detailed simulation shows that the unity gain bandwidth (GBW/UGW) of the OTA somewhat dictates the above mentioned critical OTA gain and pole frequency, which is around 4MHz, besides, when the gain A is very small (ω_p is very large to guarantee minimal GBW), the SNR also degrades considerably but still stable. The simulation results of the third model shown above also indicate such a critical GBW, which is $A*\omega_p = 400* 2\pi *10000 = 1000*2\pi *4000 = 2\pi *4M$ (rad/s). Since the sampling frequency of the modulator is 10MHz, we conclude that, at least roughly, unit gain bandwidth of the first OTA should be larger than around half of the sampling frequency to get stable sigma delta modulator operation. Besides, we should be careful of using the first model, which wrongly predicts a four times

less minimal GBW.

Finite output swing is another serious problem in real OTA, because models in Simulink are ideal, we should manually set upper and lower bound of each integrator's output in the sigma delta modulator, in case the output signal of integrator varies in a larger range than the real OTA can handle, we should make some remedies like redesign the NTF, signal scaling, enlarge the output swing of OTA, etc. Signal scaling and design of wide swing OTA will be addressed in the next chapter. Simulation result with limited output swing of the continuous time sigma delta modulator shows it degrades little compared with previous simulation result of the same modulator with unlimited output swing. In fact, the signal output swing of the designed continuous time sigma delta modulator is mainly within ± 1, ± 1.5, ± 1.6 for three integrators respectively. Only few slightly exceed the limit ± 1.65. Thus limited output swing is not a big issue for ideally implemented building blocks with ± 1.65 swing limits. Nonetheless, this problem can be severe when transistor level implementation is conducted. We will revisit this in next chapter.

For the jitter and thermal noise, as described above, they can be approximately treated as an equivalent constant noise source. The example given in last section shows that the maximal achievable SNR is 92dB for that set of parameters. Thermal noise and jitter are probably the dominant error sources for high performance continuous time sigma delta modulator, we should be aware of this during the process of designing.

4. Chapter 4

Transistor Level Implementation of the Complex Modulator and Layout

4.1. Introduction

In the previous chapter, high level design of continuous time sigma delta modulator is conducted, as well as modeling and simulation. In this chapter, the design, simulation and layout of the whole system will be presented, namely, IF input complex baseband continuous time sigma delta modulator. A novel input resistor sharing technique is proposed and wide output swing OTA is studied. Design of various building blocks is also elaborated.

4.2. IF Input Complex Modulator

As described in previous section, IF input baseband modulator finds wide application in various receivers and other fields. It is advantageous over direct bandpass modulator for its low power consumption, flexibility, etc. Complex modulator is adopted for its intrinsic image rejection property as explained before. Integrated passive mixer converts the IF input signal to baseband signal which is fed into subsequent baseband modulator. Sigma delta modulator is most suitable ADC here for its high performance [8,26,27]. Besides, its high tolerance of noise and analog circuits' nonidealities makes it the best candidate in today's highly integrated mixed signal systems, where digital noise could easily be coupled to analog part via power

supply or substrate, etc. Continuous time sigma delta modulator is chosen for its high speed, low power consumption, low sampling noise, inherent antialiasing filter, etc. Most important of all, the sampling frequency is not related with the input IF, thus the ΣΔ modulator can deal with an extended range of input IF signals, possibly up to a few hundred mega hertz. While for discrete time counterpart, sampling frequency and IF have certain relationship [1], which severely affects the flexibility of the IF input modulator.

The design is mainly comprised of two pair of passive mixers and continuous time baseband sigma delta modulators. The first stage of the modulator employs RC integrator for its high linearity, which is critical for the overall performance. The whole architecture of this design is depicted in the following Fig. 4.1.

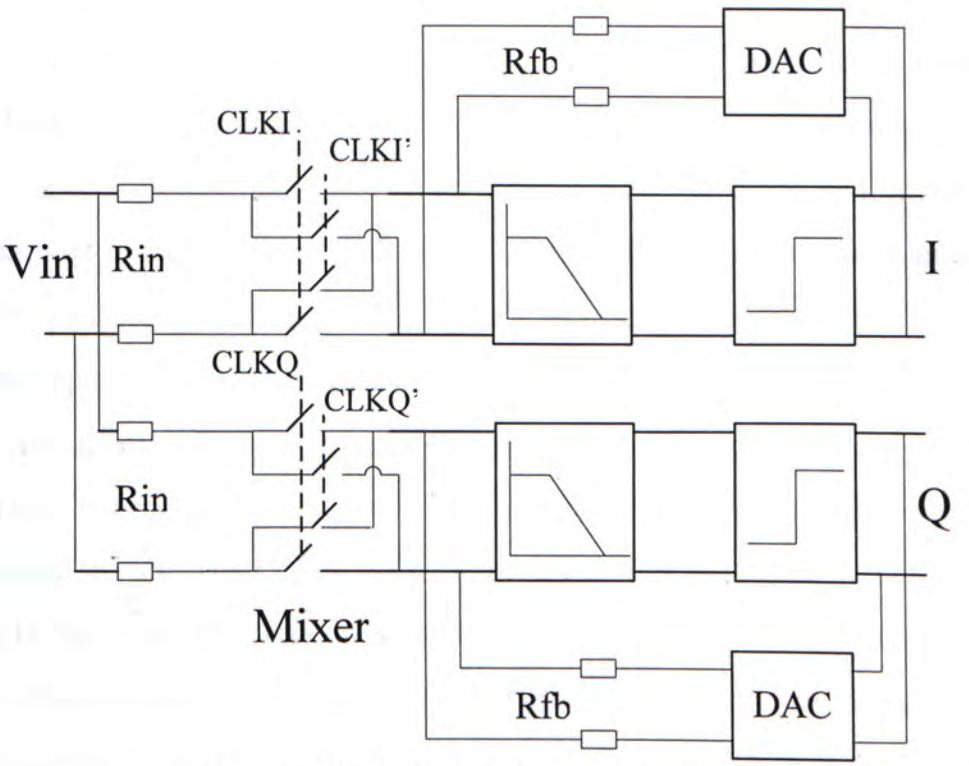


Fig. 4.1 Whole Architecture of This Work

As shown in the diagram, loop filter, quantizer and feedback circuitry form the sigma delta modulator. The input resistors are deliberately put in front of the mixers thus the mixers are connected to the virtual ground of first stage OTAs, which could

improve the linearity of the mixer due to their fixed gate source voltage of NMOS switches [28].

4.3. High IR IF Input Complex Modulator Design

In previous section, we presented the whole structure of the IF input complex modulator. Ideally, the image rejection is perfect if I path and Q path are exactly the same except for 90 degree LO clock phase shift. But in practical implementation, many nonidealities and errors occur especially for analog circuit design. Though sigma delta modulator is well know for its high tolerance of those error sources, they are still vulnerable for errors introduced at the input stage of the modulator, because these errors are simply not shaped by NTF, they are directly reflected at the output of the modulator together with the input signal. So any mismatch at the input stages of I and Q paths can affect the result considerably, thus the image signal can no longer be completely eliminated. Intentioned ideal IR is actually impossible. Fortunately, the internal mismatches of the pair of sigma delta modulator is suppressed by the high gain in front of them, thus they are only secondary effects. Let us now examine the circuitry connected to the input of the sigma delta modulator in this design. It is clear that the input resistors, feedback resistors, current mixers, LO drivers and DAC are most critical components in terms of IR performance. The on impedance of mixers and DAC is neglectable compared with input and feedback resistors. As for the quadrature signals, a four times clock can accurately produce the desired phase shift using D flip flops. Error introduced by the mismatch of the feedback paths, mainly the feedback resistors in I/Q channels, has been overcome by the data dependent dynamic element matching (DEM) technique presented in [2]. Now the only main limiting factor of IR performance is the mismatch of input resistors. Though we can use high quality polysilicon resistors and carefully doing the layout job, it's very hard to guarantee high precision of resistors ratio in today's technology. Even 0.1 percent of mismatch will limit the IR ratio to around 60dB. To solve this problem, the most

effective way is to guarantee the resistors used in I and Q channel are identical.

The conventional way of implementing the input stages of I/Q channels are totally separate, as shown in Fig. 4.1. Two set of input resistors are connected to I/Q respectively. The local clocks have nearly fifty percent pulse width, which are shown in Fig. 4.3. As discussed before, the resistors will inevitably have small deviations. A novel input resistor time-sharing technique is proposed to ultimately get rid of the mismatch. This method is illustrated in Fig. 4.2. Only two resistors are used in this scheme, and they are shared by I/Q channels. The clocks of complex mixers are designed in such a way that at the same time, only one channel is put through, thus the pulse width of each clock is required to be at most twenty-five percent of a period. Clocks in accordance with this time-sharing technique are shown in Fig. 4.4.

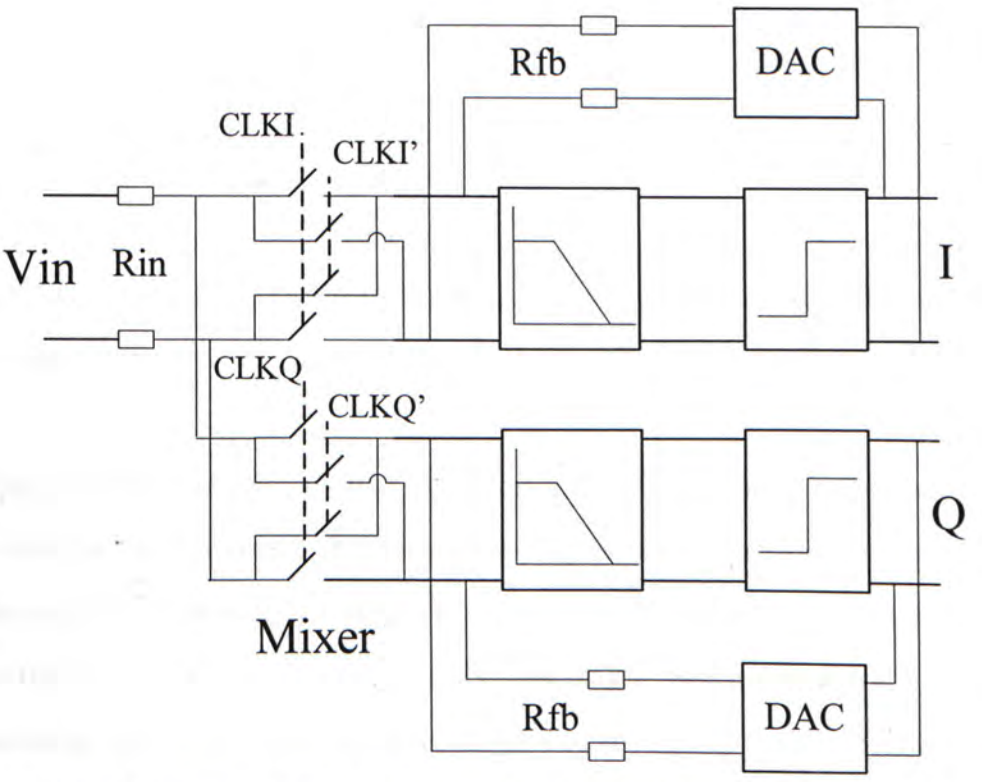


Fig. 4.2 Block Diagram of the Proposed CT I/Q ΣΔ Modulator with Integrated Mixers

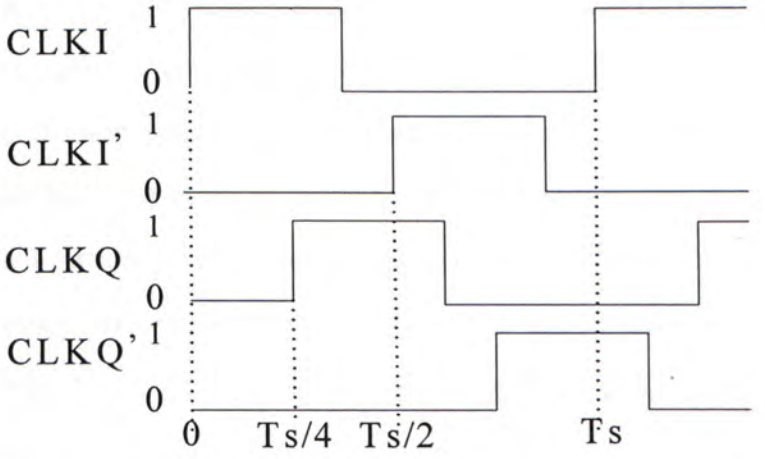


Fig. 4.3 Clock Signals for the Conventional CT I/Q ΣΔ Modulator

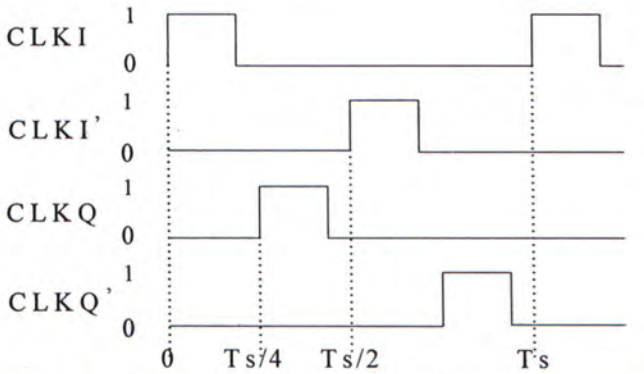


Fig. 4.4 Clock Signals for the Proposed CT I/Q ΣΔ Modulator

In this way, resistors in both channels are bound to be the same. After addressing this major limiting factor, extreme high IR ratio can possibly be achieved.

The proposed method also involves some drawbacks. One is the charging time of the first integrator is shortened by half, since the pulse width is narrowed. But this can be compensated by adjusting the values of resistors and capacitors. The other issue is when the IF is very high, the transistor's switching speed may become a concern. Fortunately, in most of the applications, the IF will not exceed the speed limit.

High level simulation is first conducted to get a general idea about the performance improvement by employing the new technique. Continuous time sigma delta modulator has already been modeled using Simulink. Here modeling of the effect of

resistors and mixer is carried out. Since in Simulink, there is no concept of voltage and current, we cannot directly model the resistors which convert the input voltage to current in circuit implementation. But we can simply use gain block to model the resistor, this has the same effect as different value of resistors. For the mixer, we use clock controlled switches, which act in a way that the positive input and negative input pass through alternatively. For the traditional implementation, we apply the clock signals which have ideal phase shifts as depicted in Fig. 4.3. The input resistors are independent. The whole diagram is shown in Fig. 4.5.

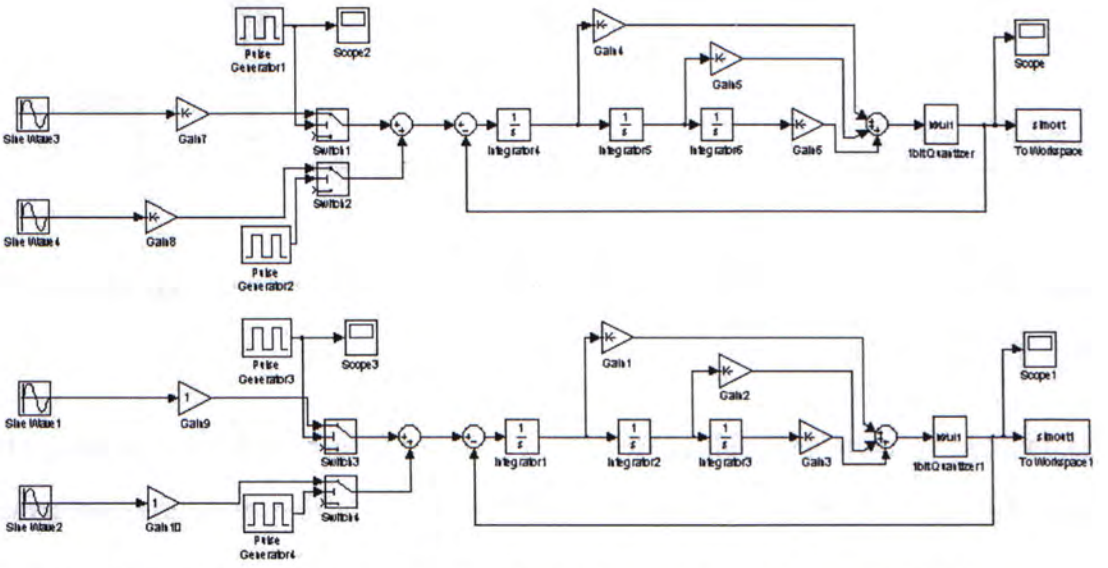


Fig. 4.5 Model of Traditional CT I/Q ΣΔ Modulator with Integrated Mixers

Suppose there is 0.1 percent mismatch of the resistors between I and Q paths. The LO frequency and sampling frequency are all normalized to 1, while input frequency is 1+1/512Hz. The output spectrum, which is obtained by Fourier transform of I path output plus 90 degree phase shifted Q path output, i.e. F(I+j*Q), is shown in Fig. 4.6.

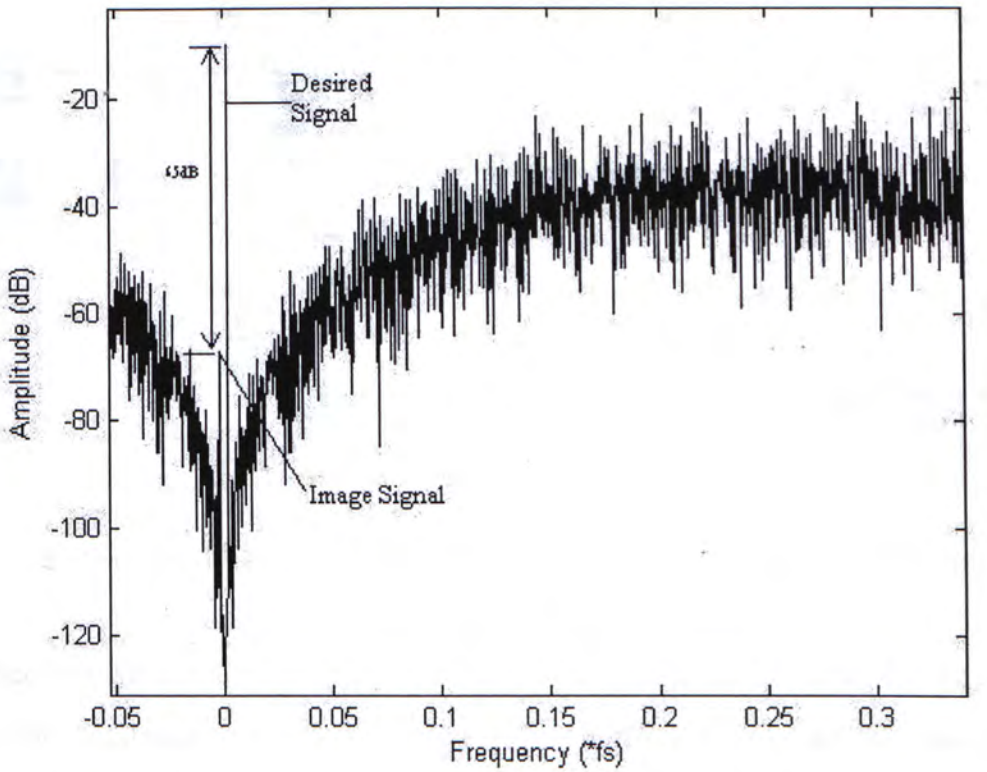


Fig. 4.6 Output Spectrum of the Traditional Approach with 0.1 Percent Input Resistor Mismatch

It is observed that 65dB image rejection is obtained in this simulation, since all other circuitries are ideal, only 0.1 percent resistor mismatch is added, we can see how important the matching of the input resistors is.

For the proposed method, the model is presented in Fig. 4.7, note that the clock signal now take the form as shown in Fig. 4.4.

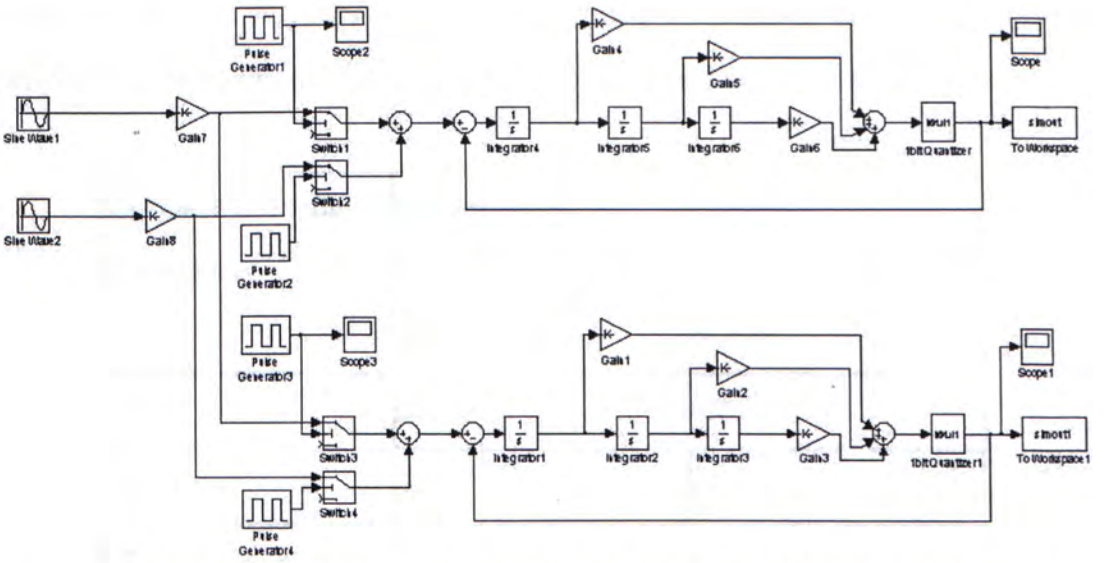


Fig. 4.7 Model of Proposed CT I/Q ΣΔ Modulator with Integrated Mixers

Since now the resistors in I path and Q path are bound to be the same. We are safe to get the simulation result shown in Fig. 4.8, simulation settings are the same as the above one.

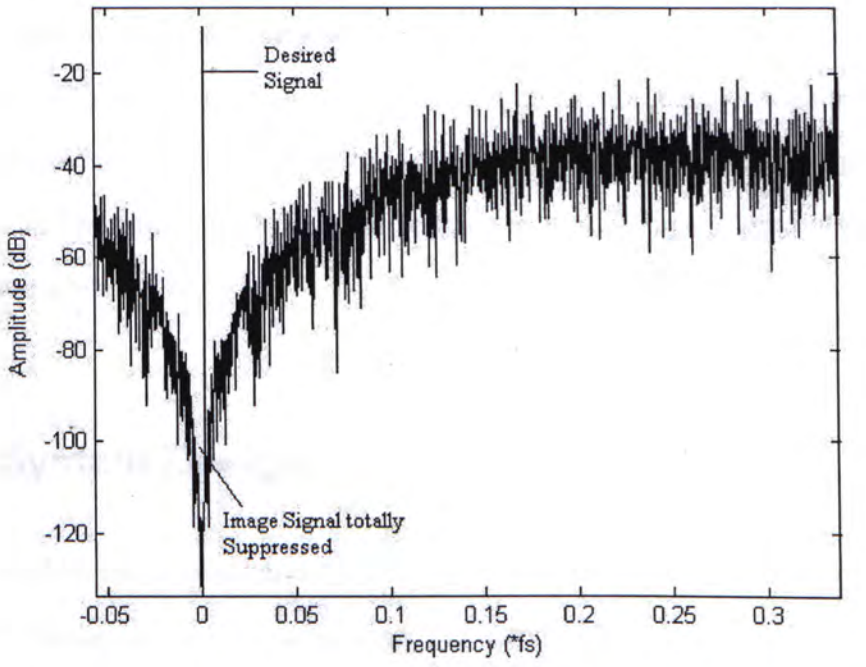


Fig. 4.8 Output Spectrum of the Proposed Approach with Resistor Time Sharing

The picture shows no image signal exists at all. SNR of complex output is 84dB for 128 OSR. The technique proposed effectively eliminates the image signal caused by

mismatch of input resistors. The following table 1 compares the image rejection performance of traditional implementation and proposed one.

Mismatch of Input Resistors	Conventional Method (Resistors not Shared)	Proposed Method(Resistor Shared)
0.1%	65dB	ideal
1%	46dB	ideal
10%	26dB	ideal

Table 1. Comparison of IR Performance between Traditional and Proposed Architecture

As indicated above, after integrating the mixer, the signal to noise ratio degrades considerably, only 84dB SNR is achieved for the architecture adopting new clock scheme. Generally, there are around 10-15dB SNR loss for traditional architecture and 15-20dB for proposed one compared with corresponding single path sigma delta modulator without integrated mixer, depending on LO frequency, its pulse width, etc. This phenomenon is mainly due to signal attenuation after mixing and harmonic distortions. The timing of LO signal relative to that of input signal also affect the SNR quite a bit.

4.4. System Design

In this section, the detailed architecture of the whole design will be presented. Signal scaling is studied to ease the requirement of output signal swings of three integrators. General blocks of the work have been described in previous sections. Here we would like to make the design more concrete.

First, the whole architecture with various building components is shown in Fig. 4.9.

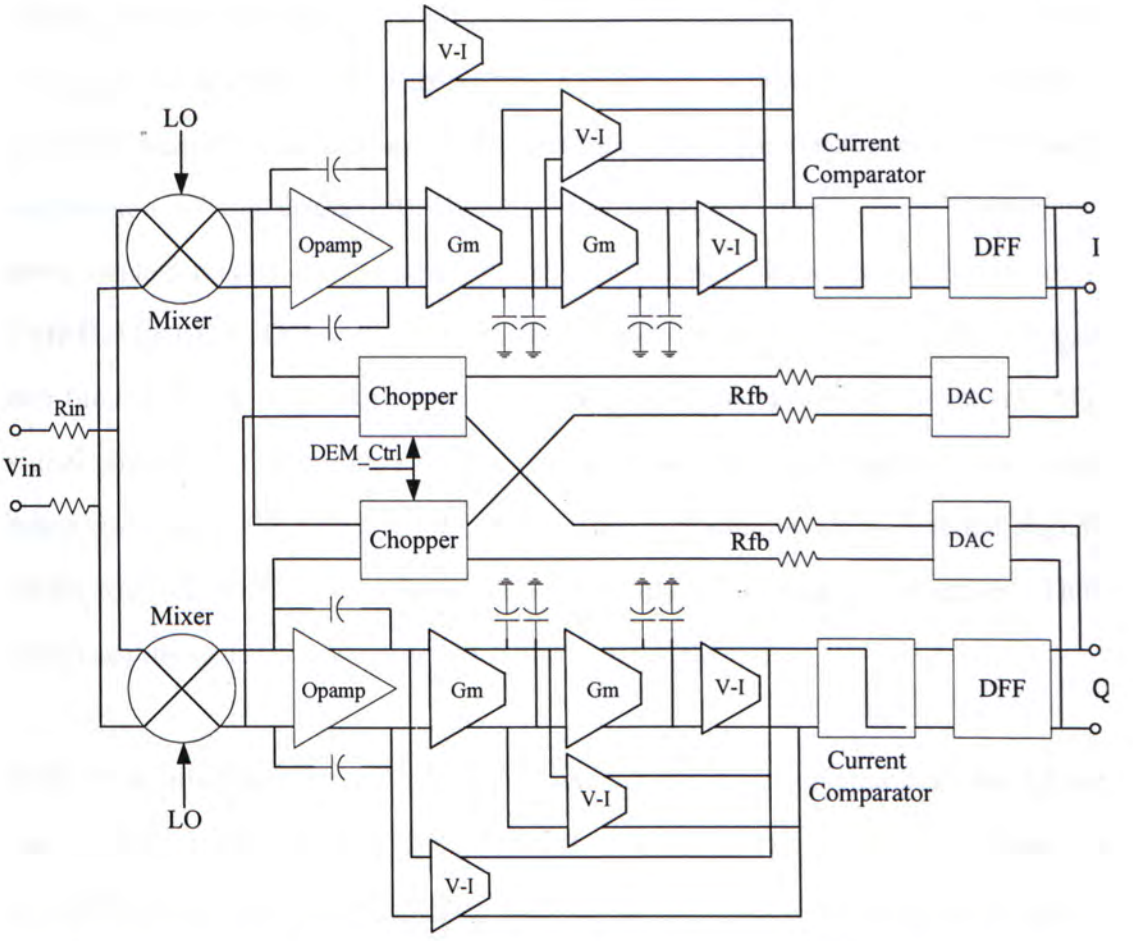


Fig. 4.9 Detailed Architecture of the Design with Proposed Resistor Time Sharing

The I path and Q path are identical in terms of building blocks. They share the feedback dynamic element matching circuitry, which effectively spreads out the error caused by mismatches of feedback circuits, mainly of unequal values of two pairs of feedback resistors. D Flip Flop is employed to latch the quantizer output at the rising edge of the clock signal, which is a delayed version of the one that controls the comparator, or in other words, the one that functions as sampling clock of the continuous time sigma delta modulator. The feedforward coefficients are implemented using V-I converter, in this way, we can manage to avoid the use of voltage adder preceding the comparator. Instead, three current outputs can simply be shorted and share the same loading. Correspondingly, current comparator is dictated to process the current signal. The feedforward coefficients are determined using the method described in last section, they are 0.6704, 0.2442, 0.044 respectively. For three integrators in sigma delta modulator, ideally they should realize the function

10M/S, 10M corresponds to the sampling frequency of the design. Their linear input ranges should be made as large as possible to minimize distortion. The first integrator should be designed carefully and high gain of the first opamp/OTA is desired for high suppression of the errors introduced in the following stages. Fully differential implementation is adopted to suppress the even order harmonics, as well as increase CMRR, PSRR[29]. Output signal swing and signal to noise ratio can also be enlarged one time. Because noise is normally uncorrelated, their powers add together, while signal power is fourfold. Since limited output signal swing of integrators may cause much distortion, it is mandatory that we design a modulator whose internal signals swing within a small range, which can be well handled by designed integrator. Thus signal scaling is usually necessary to achieve this goal.

High level simulation in last chapter tells us that ideally this sigma delta modulator has internal signal swing mainly within ± 1.65V, which coincidently corresponds to 0-3.3V in transistor level design. But such rail to rail swing is actually impossible in real circuit design, let alone keeping high linearity at the same time. So we must come up with some method to resolve this issue. Careful study shows that for this particular architecture of sigma delta modulator with feedforward compensation, the gain of the first integrator can be scaled without affecting the output of the modulator, thus the internal signals will scale correspondingly, theoretically, we can limit the internal signals to an arbitrary small range. We will analyze this as follows.

First we give the characteristic equation of a general sigma delta modulator again,

$$Y(z) = \frac{H(z)}{1+H(z)} V_{in}(z) + \frac{1}{1+H(z)} Q_n(z) \tag{4.1}$$

If V_{in} is timed by a constant a1, suppose the second part at the right hand side is sufficiently small, then the output is also about a1 times the original output. Thus feedback signal/output signal and input signal scale the same amount, this is equivalent to scale the gain of the first stage of the sigma delta modulator while

keeping the input unchanged, since both feedback signal and input are fed into the first stage. The above analysis seems to be not precise. We will try to explain this from another perspective. Assume V_q is the input of the internal quantizer, let other assumption be the same, then ideally the operation of a sigma delta modulator strictly follows the equations below

$$V_q(n) = [V_{in}(n) - Y(n)] * H(n) \tag{4.2}$$

$$Y(n) = sign[V_q(n)] \tag{4.3}$$

By observing the two equations, the magnitude of $V_q(n)$ doesn't affect the output, thus $V_{in}(n)$ and $Y(n)$ could arbitrarily scale up or down, the two formulas still hold, i.e. if $V_{in}(n)$ scales, $Y(n)$ would scale the same amount according to the set of equations above. Since magnitude of $Y(n)$ is set by the feedback reference voltages, they are fixed once implemented, we resort to scaling the gain of the first stage, which has the same effect as mentioned before. By doing this, the input and feedback signals are set free while the output is unchanged. Most importantly, the internal signal swings scale correspondingly as the gain of the first stage scales. Similarly, scaling the gain of H(n) will not alter the output either, but it's relatively complicated compared with the former one.

The proposed scaling method is ideal as long as the aforementioned two equations hold. But for real implementation, they do not exactly follow those equations, say, the quantizer is not ideal, there is excess loop delay in the feedback path, the integrators are not perfectly linear and their transfer functions vary a little bit for different input, etc. The other limiting factor is if we intend to scale down the internal signal swings aggressively, the gain of the first integrator, which is determined by RC constant, should decrease comparably. This means the value of R or C should be increased dramatically. In VLSI technology, large resistor and capacitor are area hungry, what's worse, the large resistor contributes more thermal noise to the overall

circuits. Based on simulated swings of internal signal and the facts described above, we finally choose 3 times larger RC constant to scale down the signal.

Besides the effective scaling method presented above, the gain of the third integrator is also scaled to make its output signal swing comparable to that of the other integrators. The third feedforward coefficient is scaled up correspondingly. Since the third feedforward coefficient is relatively small, it's desirable to scale it up in order to make the feedforward coefficients' values about the same order. This can result in higher quality VLSI fabrication. Theoretically, we can get a set of optimal coefficients which lead to smallest signal swings without changing the transfer functions of the sigma delta modulator. But practically, time domain transient simulation of transistor level implementation differs much from that of high level one, the internal signal swings also change a lot. Under this situation, we need to scale the coefficients mainly based on transient simulation results. The gain of last integrator is eventually reduced to 1/7 of the original value, third feedforward coefficient is then 7*0.044=0.308.

Design of building blocks and simulation of the whole system will be shown in the following sections

4.5. Building Blocks Design

4.5.1. Transconductor Design

Operational transconductor amplifier (OTA) is the most basic and important building block in this work. The first stage of the sigma delta modulator uses OTA to build the RC integrator, the second and third stage employ degenerated OTA as g_m cell. Feedforward coefficients are also realized by transconductors with different g_m values. In this section, design of OTA will be described and general procedure is

given.

OTA can be thought of as a kind of opamp who has very large output impedance. But strictly speaking, opamp normally refers to those amplifiers with neglectable output impedance, none the less, opamp is a more general term, researchers sometimes use opamp to refer to all amplifiers, which also include OTA, etc. G_m is another similar cell but functions as voltage to current converter. Its input linear range should be as large as possible. G_m will be dealt with in a following section.

There are two general architectures for single stage OTA, one is telescopic, the other is folded cascode. Both architecture can achieve high gains while only one stage is employed, which means only one dominant pole exists, the speed can be much higher than another less used two stage OTA. Telescopic has higher gain and wider bandwidth for the same current level compared with folded cascode counterpart, but its output swing is limited because at least five MOS transistors cascade in a single path. Input common mode is also restricted to a small range to guarantee all the transistors operate in saturation region. Folded cascode architecture artfully moves the input differential pair out of that multi-stacking path while the desired characteristics are minimally affected. The output swing is thus enlarged and input common mode range increases substantially. In practice, folded cascode OTA is more widely used. Here we'll briefly describe how to design folded cascode OTA using Spectre in Cadence. The procedure provided below is based on my design experience and heavily relies on simulator.

The general architecture of folded cascode OTA is shown in Fig. 4.10.

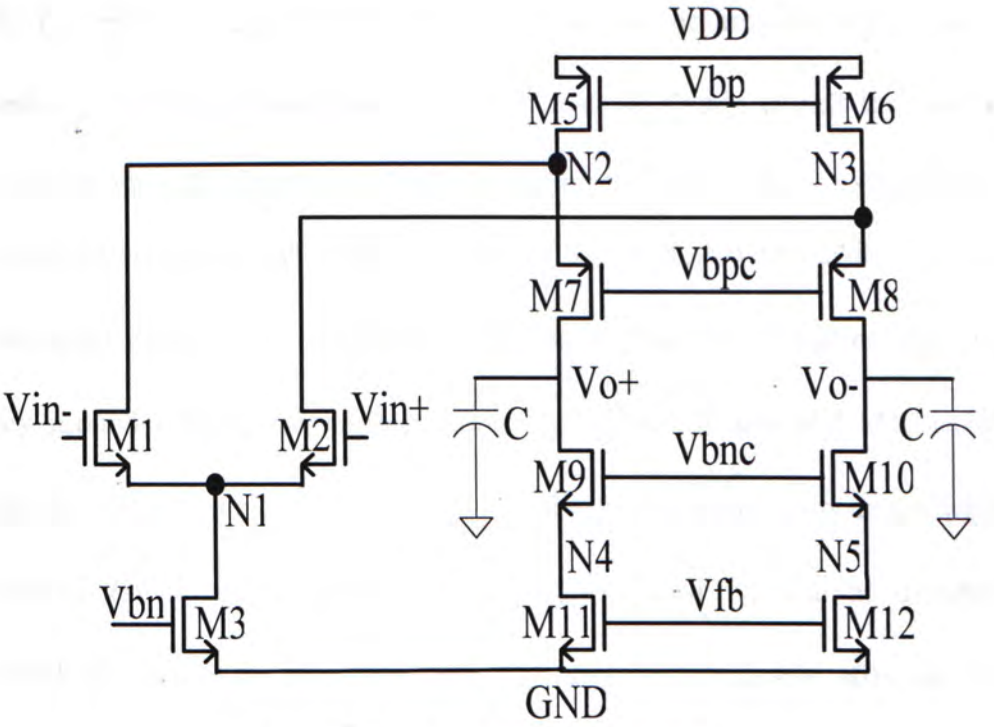


Fig. 4.10 Folded Cascode OTA

We can choose NMOS input folded cascode OTA for higher gain because transconductance of NMOS is about 3 times larger for same drain current and W/L aspect ratio. But the second pole located at N2/N3 is lower also due to larger equivalent impedance $1/g_m$ of PMOS transistor. Besides, if we intend to connect the source and substrate of input differential pair to avoid body effect, PMOS should be used in P-substrate process. The gain of this OTA can be described as $A_v \approx g_{m1}(g_{m8}R_{ds8}R_{ds6} // g_{m10}R_{ds10}R_{ds12})$. Here we use NMOS input differential pair as an example. Suppose supply is 3.3V. Minimal length of transistor is 0.35um.

1. Allocating current. For a given power consumption requirement, set the current flowing through M5 and M6, remember to take into account the needed current in biasing circuitry and CMFB. For input pair and cascode branches, we can allocate equally the total current that comes from M5/M6, or, if we'd like to design a high gain OTA, the input pair could sink more current for higher g_m and the cascode branches take less current to larger output impedance. But if we desire an OTA with high unit gain bandwidth, the cascode branches should absorb more current.

2. Set the biasing voltage. Refer to the process manual for threshold voltages of V_{tn} and V_{tp}, but it is strongly recommended that we should extract the threshold voltages through simulation. Be cautious of the body effect, extract various threshold voltages under different values of V_{bs}. If high output swing is desired, overdrive voltage V_{od} of transistors in cascode branches should be kept small, say, around 100mV. The corresponding V_{ds} of M5/M6 and M11/M12 is better chosen to be around 1.5 times of V_{od} for larger output impedance without costing too much voltage drop. Now V_{fb}, V_{bp} and V_{bn} can be determined based on known V_t, V_{od}. V_{bpc} and V_{bnc} are also obtainable after allocating V_{ds} of M5/M6 a`nd M11/M12.
3. Design the biasing circuitry to get the desired biasing voltages. This will be introduced later.
4. Roughly calculate or assign the W/L ratios of all the transistors. Based on the first order approximation formula $I_{ds} = \frac{\mu C_{ox}}{2}\frac{W}{L}(V_{gs} - V_t)^2$, we can get the very rough values of W/L of all the transistors except for the input pair, since all other variables in the formula are known up to now, μC_{ox} can refer to process manual. Note that the resulted W/L of PMOS is approximately 3 times of those of NMOS in cascode branches. Since mobility μ of electrons is about 3 times of mobility of holes. For absolute value of W and L, we can set L to be 1 times to several times larger than minimal L, in order to alleviate short channel modulation thus to obtain high gain. L shouldn't be too large, otherwise parasitic capacitors would degrade much the AC response of the OTA, the second pole could deteriorate the phase margin. The remaining input pairs should use minimal length for low parasitics and large W for high g_m.
5. Tune the OTA with the aid of simulator. Simulate the OTA, it's almost certain

that the OTA will not work now. Pay attention to the current flowing through M5/M6 and M11/M12, one pair of them must be in triode region, which is not desired. Note that M5 and M6 are current sources, M3, M11 and M12 are current sinks, they should strictly meet the requirement $I_{M3} + I_{M11/M12} = I_{M5/M6}$, otherwise M5/M6 or M11/M12 would enter triode region to lower the current in order to meet that requirement. M3 normally will not go into triode region since otherwise Vgs of input pair would be too large, not enough current can be provided to sink into input transistors. Knowing all these, we are ready to tune the W/L of transistors. Normally we choose to tune W/L of M5/M6 provided that power consumption is not strictly defined. Or similarly, M3 and M11/M12 can also be chosen to tune their W/L. Parametric sweep of analog design artist in Cadence can be employed to easily sweep W, thus effectively change the ratio of W/L. Remember, our objective is to meet the above current equation while keep all these five transistors in saturation region. AC analysis is chosen while doing parametric sweeping, monitor the DC gain of the OTA, when all these transistors are in saturation region, the DC gain would be quite large, usually >60dB. Large range large step size W sweeping is conducted first, we will find that DC gain changes monotonically as W increase and to a certain value of W, the gain begins to decrease monotonically. This phenomenon can easily be explained by analyzing the folded cascode OTA. Then, we limit the sweep range to W1, W2, which result in highest gain in precious parametric sweep simulation. This process repeats several times, finally we'll get very high gain and all the transistors are in saturation region.

6. Remedies if fails. Sometimes if the initial guess of biasing voltage and W/Ls based on first order approximation equation deviate too much from workable ones, the above procedure may not work or can only obtain a marginally work OTA, i.e. only fair DC gain is achievable. (other aspects of performance not considered yet). For example, if V_{bpc} is too large or M7/M8 has too small W/L ratio, M7/M8 can never let specified current (defined by M11/M12) go through

without forcing M5/M6 into triode region. In such cases, we should tune the W/Ls of these concerned transistors. Then redo step 5.

7. Check other aspects of performance. This mainly includes the phase margin of the OTA, if less than 60 degree for certain loading capacitor, pay attention to M5-M8 and M1/M2, smaller area of M1/M2 and M5/M6 is preferred for less parasitic capacitors, larger g_m of M7/M8 is desired to lower the equivalent impedance seeing into sources of M7/M8. If DC gain is still not enough, consider reasonably increasing L of transistors in cascode branches or use gain boosting technique [30]. And pay attention whether impedance looking into PMOS part from output is similar to that of NMOS part. Increasing W/L of input pairs further usually has less effect. Other considerations like input referred noise, we should pay attention to M1/M2 and M5/M6. For the important parameter of unit gain bandwidth, in addition to allocating more current to cascode branches and increasing the g_m of input pair, the second pole frequency of the OTA should be guaranteed to be far larger than the UGW.
8. CMFB design. This issue will be handled later in this section.
9. Corner analysis and Monte Carlo simulation. After the whole OTA has been designed and proved that it functions well under normal condition, extreme case analysis and random case analysis with consideration of process variation and mismatch should be carried out. Normally the OTA can pass corner analysis since the various parameters like V_t, μ of main circuitry and biasing circuitry changes simultaneously, together with the well defined common mode voltage at the outputs, the transistors in the cascode branches can remain in saturation region, thus only little performance variation is observed. On the other hand, for Monte Carlo simulation, the parameters changes randomly for different transistors, we should set the correlation between symmetric transistors and so forth to make the simulation result more reasonable, otherwise only part of the cases of Monte Carlo simulation can work well.

The procedure presented above is for general purpose design, for OTA with special requirements we should put more effort on those aspects. For OTA with other architectures we could easily develop other set of procedures, the first stage OTA designed in this work is shown in Fig. 4.11, other ones will be presented in following sections.

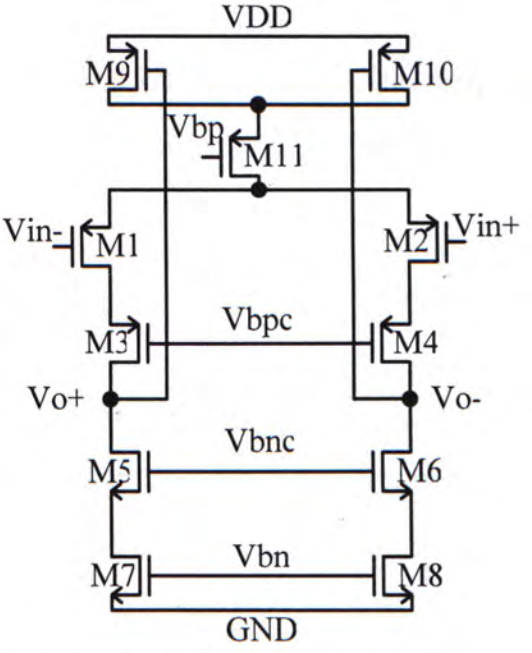


Fig. 4.11 First Stage OTA

M11 is the current source of the main part of OTA, PMOS input differential pair is employed to reduce flicker noise of the first stage, which could be dominant low frequency error source, but at the cost of lower gain. M9 M10 performs as common mode feedback circuitry, CMFB will be explained later. The performance of the OTA is tabulated in Table 2.

Vdd	3.3V
GBW	22MHz
DC Gain	77.5dB
Phase Margin	81degree
Power Consumption	0.67mW

Table 2. Design parameters of the First Stage OTA.

First stage is of most importance in the sigma delta modulator, so high gain of OTA is desired for high suppression of subsequent noise and high linearity of RC integration, though theoretically DC gain can be very small as described before. Unity gain bandwidth is close to sampling frequency, which is much larger than 0.4fs as deducted in last chapter.

The main part of the OTA need various biasing voltages as shown in Fig. 4.11, The biasing circuitry adopted in this work is given in Fig. 4.12.

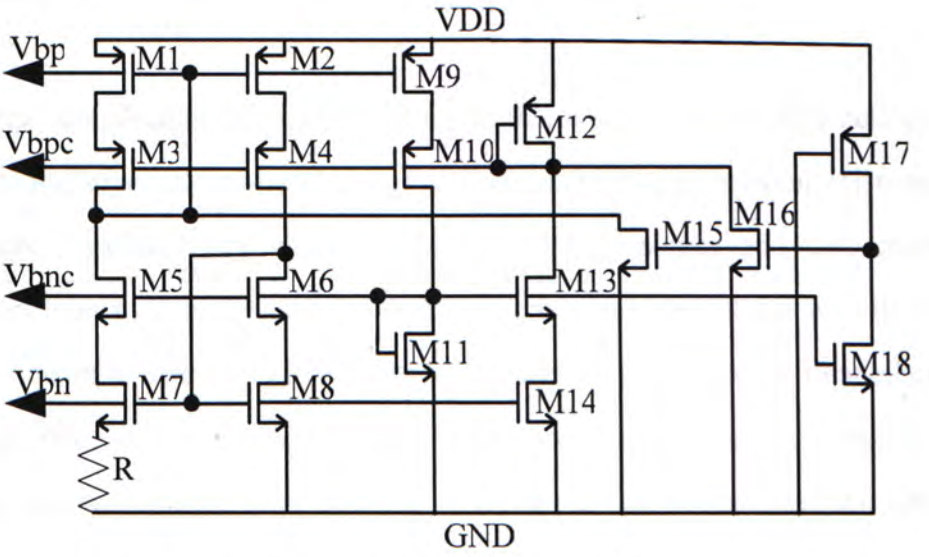


Fig. 4.12 Wide Swing Constant G_m Biasing Circuit

This is a wide swing constant g_m biasing circuit, the P channel wide swing cascode current mirror comprises M1-M4 which use diode connected M12 as the biasing transistor. Similarly, N channel cascode current mirror consists of M5-M8 and biasing transistor M11. M9 M10 and M13 M14 provide current for two biasing transistors. M15-M18 compose the start up circuitry, without which, the biasing circuit could stabilize at a state where no current flows at each branch.

By observing the biasing circuit, we could see that biasing voltage V_{bnc} of cascode transistors M5/M6 is $V_{th6}+V_{od6}+V_{dsat8}$, thus the minimum voltage drop over

M6/M8 or M5/M7 in Fig. 4.12 is only $V_{d6} = V_{th6} + V_{od6} + V_{dsat8} - V_{th6} \approx 2V_{dsat}$, wide output swing is therefore possible. For the property of constant transconductance, we can easily derive the following equation by analyzing M7,M8 and R.

$$g_{m8} = \frac{2[1 - \sqrt{\frac{(W/L)_8}{(W/L)_7}}]}{R} \tag{4.1}$$

It's obvious that g_m is independent of power supply and insensitive to absolute W/L values. Since g_m is one of the most important parameters which determine the performance of OTA, it's highly desirable to keep it stable.

The output common mode voltage of fully differential OTA is not well defined. This is due to the large output impedance of an OTA, any process variation, mismatch and temperature variation etc will affect a little bit the source and sink current of cascoded branch, thus the output common mode would go all the way up to near VDD or down to near GND to balance the source and sink currents. In another point of view, since common mode gain of OTA is very small, output common mode voltage is almost independent of input voltages, thus additional feedback loop with high common mode gain is needed to control the output common mode voltage.

A straightforward method is to detect the output common mode voltage by two equal resistors connecting differential output nodes, then the output common mode voltage at the middle of these two resistors is compared with the desired CM voltage, their difference is amplified and fedback to control the main OTA. In this way the output CM voltage can be well defined and is equal to reference CM voltage when the feedback gain is very large. This approach has the drawback that the sense resistors severely load the OTA unless they are much larger than the output impedance of OTA. Another disadvantage associated with this method is additional pole appears due to loading resistor and parasitic capacitor of feedback amplifier.

In this work, two kinds of CMFB circuits are adopted. One is CMFB using transistors in the triode region, as shown in Fig.4.11, the other is CMFB using transistors in saturation region, the circuit is shown in Fig. 4.13. The latter CMFB is employed in the feedforward transconductors.

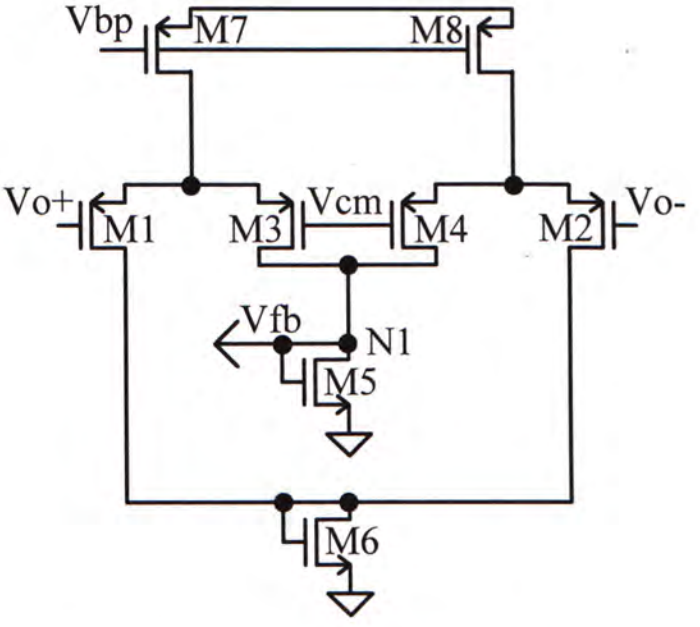


Fig. 4.13 Common Mode Feedback Circuit

For CMFB shown in Fig. 4.11, the sum of the drain currents of M9 and M10 is

$$I = I_{M9} + I_{M10} = \beta_{M9}[(|V_{o+} - V_{DD} - V_{thp}|)V_{dsM9} - \frac{V_{dsM9}^2}{2}]$$
$$+ \beta_{M10}[(|V_{o-} - V_{DD} - V_{thp}|)V_{dsM10} - \frac{V_{dsM10}^2}{2}] \qquad (4.2)$$
$$= 2\beta(-V_{OC} + V_{DD} + V_{thp} - \frac{V_{ds}}{2})V_{ds}$$

We assumed that transistor M9 and M10 are identical. We can see that the total current is dependent on output common mode voltage, while it is independent on the differential output voltages, they simply cancel out. We can understand this CMFB in this way, since total current is already set by M7 and M8 in that OTA, then I in the above equation is fixed, Voc is a function of I, so consequently, its value is also well defined. On the other hand, the output differential voltage will not be affected by this CMFB circuit, as reflected in the above equation. The limitation of this scheme is the

output swing is limited, since when the output is large enough, M9/M10 could be turned off, thus the output swing can't exceed the range $V_{th} \sim (VDD - V_{th})$.

The other CMFB circuit shown in Fig. 4.13 is briefly analyzed here. M1-M4 sense the output CM voltage. The current I_{M5} is generated which is proportional to the difference of desired V_{cm} and output CM voltage Voc. I_{M5} is then mirrored by a current sink in main OTA, in this manner, it exerts control on the output CM voltage. Assume small signal operation,

$$I_{M5} = I_{M3} + I_{M5} = \frac{I_{M7}}{2} + g_{mM3}(\frac{V_{o+} - V_{cm}}{2}) + \frac{I_{M8}}{2} + g_{mM4}(\frac{V_{o-} - V_{cm}}{2}) \quad (4.3)$$
$$= I_{M7} + g_{mM3}(V_{oc} - V_{cm})$$

Where $V_{oc} = \frac{V_{o+} + V_{o-}}{2}$. Transistor M7 and M8 are matched. The CMFB works in a following way, suppose if Voc increases, then I_{M5} and the mirrored current increase as well, this will in turn pull down the Voc and counteract the assumed increase in Voc. In steady state, $V_{oc} \approx V_{cm}$.

Switched capacitor CMFB circuit [29] does not limit the output swing of the main OTA, but due to the digital noise produced by switching clocks, it is generally not used in continuous time circuit. Besides, if the clock frequency is too fast at high frequency application, the CMFB will load the OTA heavily due to equivalent CMFB resistance T/C. The OTA gain will thus be limited.

4.5.2. RC Integrator Design

Continuous time sigma delta modulator adopts RC integrator as the first stage for its high linearity. The characteristics of the RC integrator have been analyzed extensively in last chapter, main constituent OTA has also been presented in last

section. Here transistor level simulation of the designed RC integrator is given.

Ideally, if we apply a sine wave at the input of the RC integrator, we expect a cosine wave output with the same frequency, only amplitude changes.

$$V_o = \frac{1}{RC}\int V_1 \sin \omega t dt \tag{4.4}$$

For the purpose of test, we impose differential input sine waves with magnitude V_1=100mV, frequency f = 100kHz, R and C are 100k Ω and 4pF respectively. The differential transient output of the RC integrator using the OTA presented above is shown in Fig. 4.14.

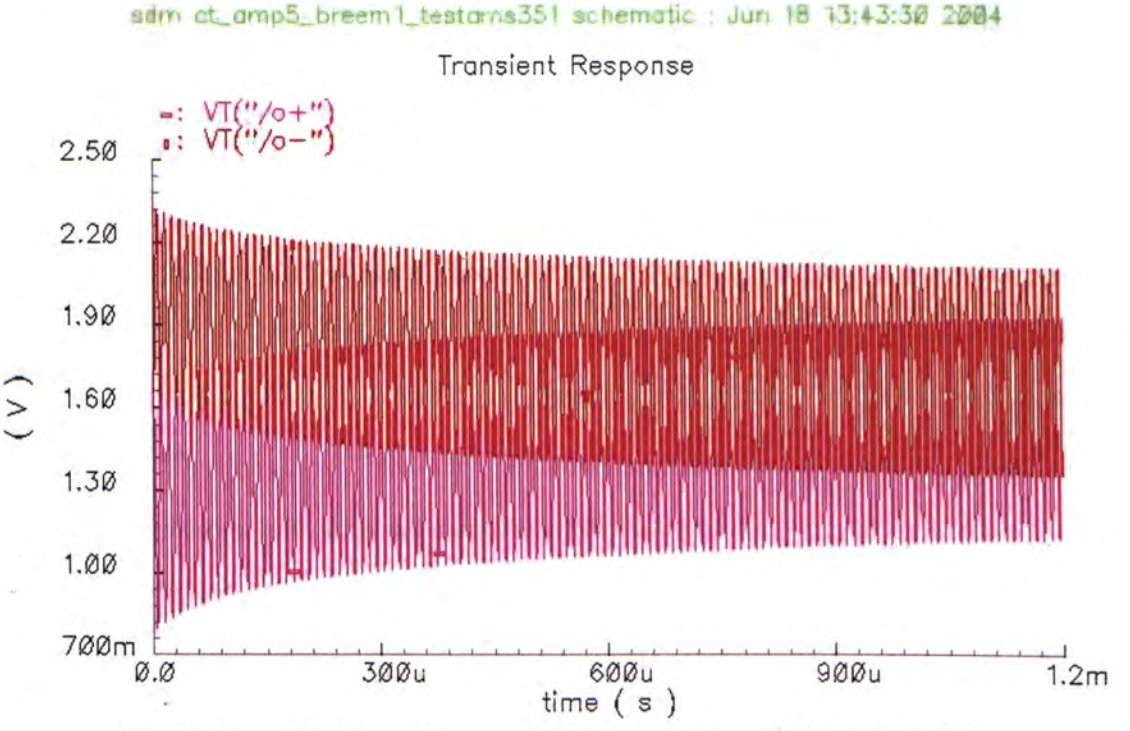


Fig. 4.14 Transient Output of RC Integrator with Practical OTA

The resulted waveforms are quite ideal sinusoidal, except that they are initially centered at different DC voltages which approach to the output common mode voltage gradually. This phenomenon can be analyzed below.

Consider the RC integrator model only with nonideality of finite opamp gain, which equals A. Refer to Fig. 3.13, we can write out the following differential equation

$$C\frac{A+1}{A}\frac{dV_o}{dt}+\frac{V_o}{AR}=-\frac{V_i}{R} \tag{4.5}$$

The homogeneous solution of this equation is

$$V_{oh}=A_1 e^{-t/[RC(A+1)]} \tag{4.6}$$

where A_1 is a constant determined by initial or boundary value.

Suppose input $V_i=V_1\sin\omega t$, The particular solution of the equation should be of the form $V_{op}=A_o\sin\omega t+B_o\cos\omega t$, replacing V_i and V_o in equation 4.5 with these two equations, we get

$$A_o=\frac{-AV_1}{1+[RC\omega(A+1)]^2} \tag{4.7}$$

$$B_o=\frac{RC\omega A(A+1)V_1}{1+[RC\omega(A+1)]^2} \tag{4.8}$$

If gain A is infinity, the output reduces to $\frac{V_1}{RC\omega}\cos\omega t$, generally A_o is sufficiently small.

$$V_o=V_{oh}+V_{op} \tag{4.9}$$

Initial V_o is equal to 0, thus we can obtain the value of A_1

$$A_1=-B_o \tag{4.10}$$

Till now, we can see that the homogeneous part, namely the transient part of the solution determines the bias voltage of the output sinusoidal waveform. When A approaches infinity, A_1 equals $-V_1$, which matches well with the waveform shown in Fig. 4.14. Then absolute value of the transient part decrease gradually, which corresponds to the biasing voltage of sinusoidal output. The misunderstanding that the bias gradually stabilize to the preset output common mode voltage is due to the CMFB circuitry should be avoided.

Various simulations under different magnitudes and frequencies of input signal are

conducted. The integrator gain doesn't strictly match with the theoretical value, normally there are several percent deviation due to numerous secondary effects of the real OTA. The lower the input frequency and magnitude, the less the deviation tends to be.

4.5.3. G_m-C Integrator Design

G_m-C integrator is employed in this work for its high speed while adding little extra loading to previous stage. Since G_m-C integrator is an open loop integrator, it has the potential for very high speed application. The major problem of this kind of integrator is limited input linear range. We know that opamp are usually used in closed loop applications, where small signal response is of most importance and can often be assumed linear. But for G_m cell, it deals with large input signals, extended input linear range is dictated. There are several commonly used methods to effectively increase the linear range. They are source degeneration technique, cross coupled quad configuration, adaptively biasing scheme, V-I conversion with fixed drain source voltage of triode region transistor [31,32,33,34], etc. All these methods try to stabilize equivalent G_m of the designed circuit over a large input range, thus output current linearly tracks the input voltage. Source degeneration is the most simple and neat method to achieve this goal while sacrificing little other performance, compared with other methods. The simple diagram to illustrate the principle is shown in Fig. 4.15.

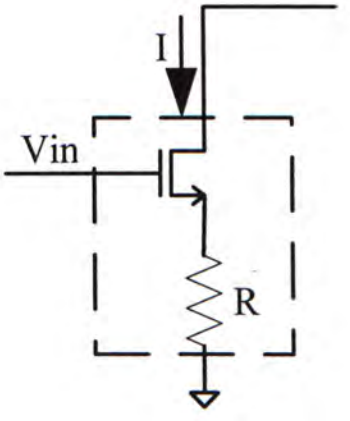


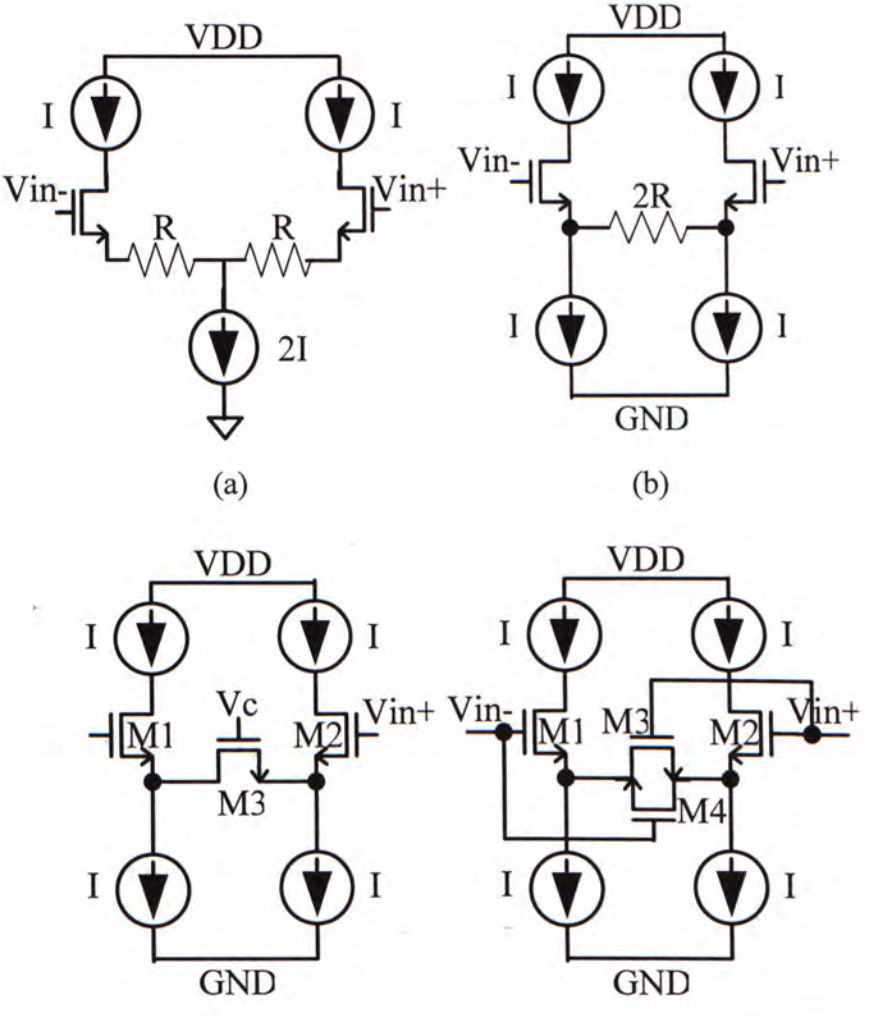
Fig. 4.15 Source Degeneration Circuit

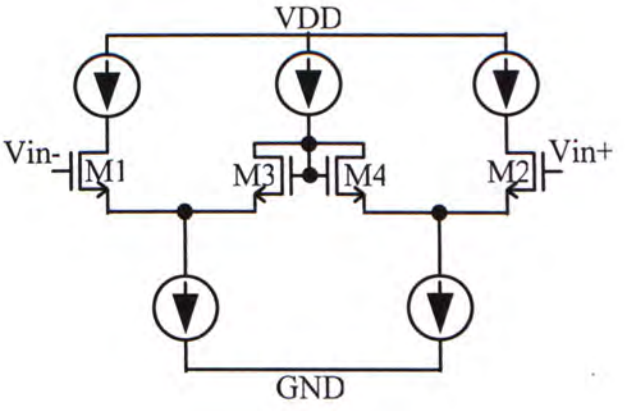
Suppose g_m is the transconductance of the amplifying transistor. Without the resistor connecting to its source terminal, $I = g_m * V_{in}$. Otherwise we can derive the equivalent transconductance of the part in the dashed box is

$$G_m = \frac{g_m}{1 + g_m R} \approx \frac{1}{R} \tag{4.11}$$

Here we assume $g_m R$ is much larger than 1. In this way, the varying g_m due to different inputs affects little the equivalent G_m, which is determined by the value of the resistor. Thus wide linear input range can be achieved.

Practical implementation of differential pair with source degeneration has many variations, they are illustrated in the following Fig. 4. 16.





(e)

Fig. 4.16 Source Degeneration Circuits. (a)(b) Resistor Degeneration Circuit. (c)(d) Triode Region Transistor Degeneration Circuit. (e) Saturation Region Transistor Degeneration Circuit

Fig. 4.16 (a),(b) realize the same overall transconductance, but other properties are a little bit different. For Fig. 4.16 (a), the noise contribution of current sink is divided by both branches, common mode noise is observed at both outputs. While for Fig. 4.16 (b), the noise of each current sink injects to single output appearing as differential noise. Another drawback for Fig. 4.16 (a) is the voltage drop at each resistor reduces input common mode range, which could be severe and limit the linear input range. The relationship between input voltage and output current is given in the following equation [33]

$$i_o = \sqrt{1-(\frac{v_{id}}{2(1+N)V_{DS(sat)}})^2} \times (\frac{\sqrt{2\mu C_{ox}\frac{W}{L}I_B}}{1+N}) \times v_{id} \qquad (4.12)$$

where N is equal to gmR, namely the source degeneration factor. It is obvious that the small signal transconductance is reduced by 1+N, the third harmonic distortion is reduced by the square of 1+N.

Since resistor occupies considerable area in VLSI implementation, MOS transistors are sometimes used to replace it. They are shown in Fig. 4.16 (c) (d) (e). For scheme shown in Fig. 4.16 (c), it is highly sensitive to common mode input signals, tuning of gate voltage V_c is required and larger V_c is desired for better linearity. By employing

two degenerative MOS transistors whose gate is controlled by the input differential signals, the sensitivity to common mode input signals is substantially reduced but the linear range is restricted to $V_{ds(sat)}$ [33]. Fig. 4.16 (e) shows the method where saturation region MOS transistors are utilize, unfortunately the linearity improvement is limited.

In this work, scheme shown in Fig. 4.16 (b) is adopted for its high linearity and simplicity, the degenerated OTA for second stage of sigma delta modulator is given in Fig. 4. 17.

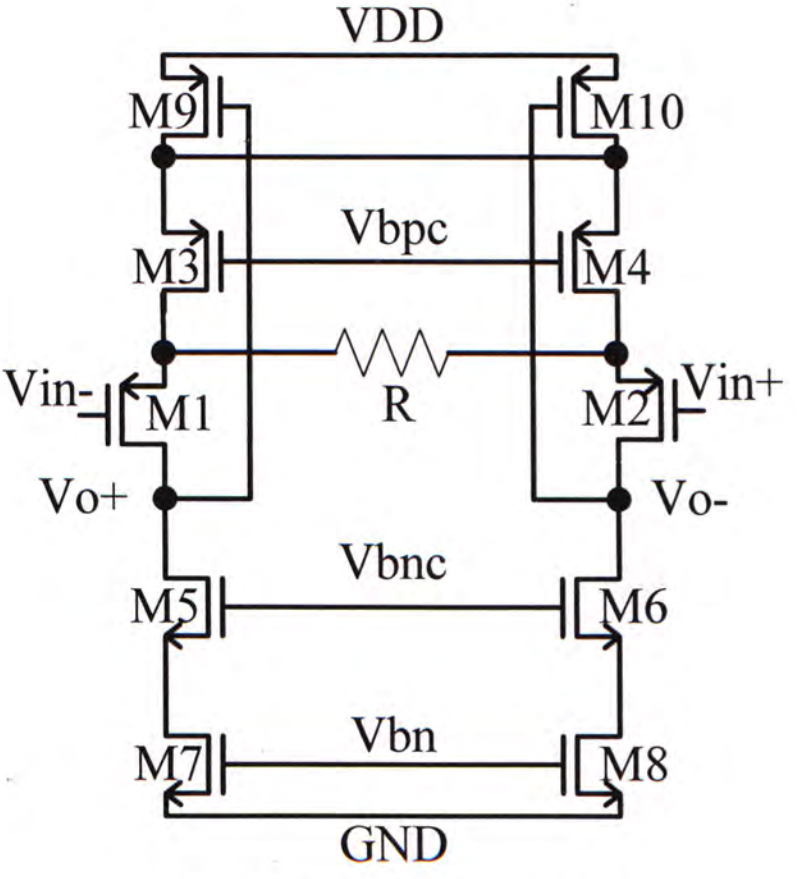


Fig. 4.17 Second Stage OTA

It's a simplified telescopic OTA, the gain requirement of the second and third stages is relaxed due to sigma delta modulator's property. 44dB DC gain is achieved with this structure, which is sufficient in the application [35]. The relationship between the output current and input voltage is found through simulation and shown in Fig. 4.18.

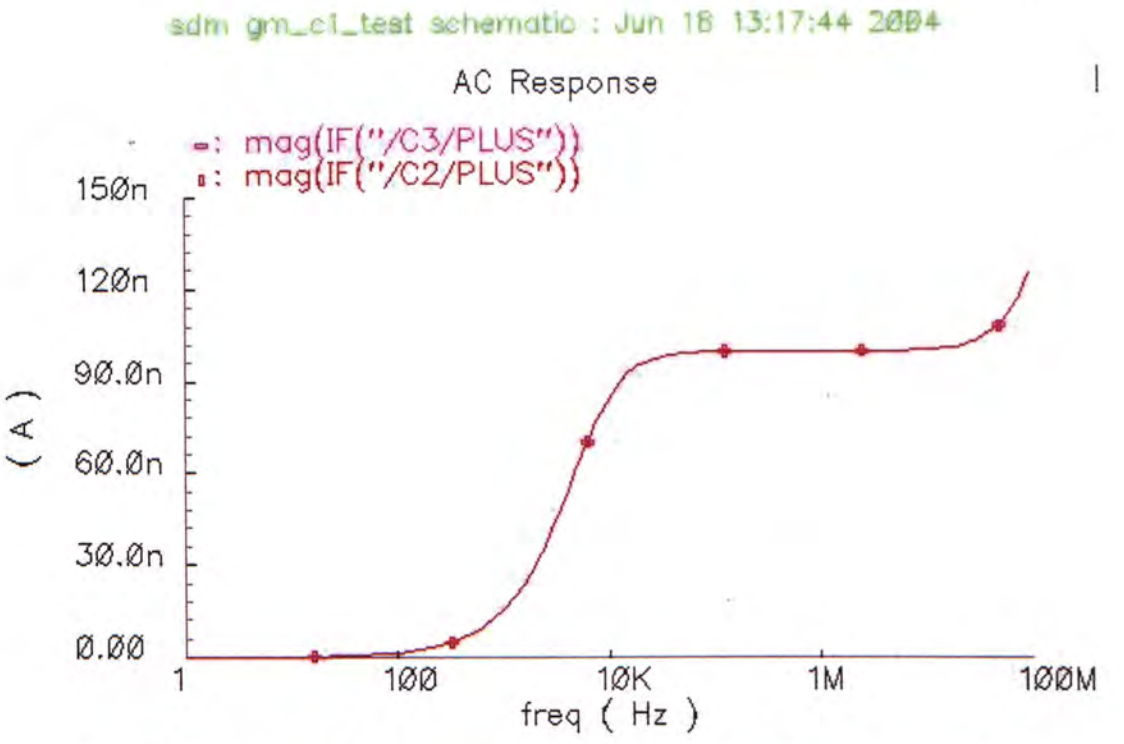


Fig. 4.18 Output Current versus Input Frequency of Second Stage OTA

This is an AC response curve to input with 1mV magnitude. The equivalent G_m can be calculated as G_m=i/v. For input signal with frequency range from around 10kHz to 100MHz, the G_m is almost constant. But for frequency less than 10kHz, G_m decreases monotonously. This is due to the finite output impedance of OTA, if ideally the output impedance is infinity, than all the current will flow into the loading capacitor, but in reality, the loading capacitor shows much larger equivalent impedance than OTA output impedance at very low frequency, thus, only a small amount of current is drawn by the capacitor, which corresponds to a smaller G_m. At higher frequency, the equivalent impedance of the capacitor is much lower than OTA output impedance, thus, nearly all the current flows into the capacitor, constant G_m therefore is resulted. The inability of G_m-C integrator in dealing with low frequency input signal is a severe drawback in applications where very low frequency signal is also of concern. Of course remedies like gain boosting technique can be applied to relieve this problem.

4.5.4. Voltage to Current Converter

Transconductance cell is again used to realize the voltage to current conversion, which constitutes the feedforward circuits. Three folded cascode OTAs with different source degeneration factors are designed. The architecture is shown in Fig. 4.19.

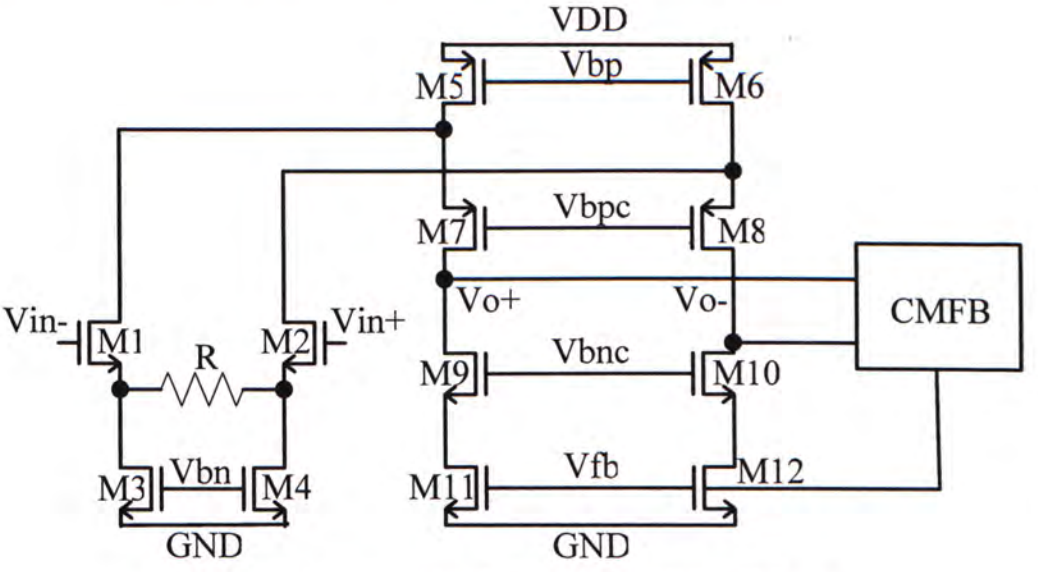


Fig. 4.19 Tansconductor in Feedforward Path

The transconductance is approximately the reciprocal of the value of degeneration resistor. The values of three degeneration resistors in these OTAs are 20.6kΩ, 60kΩ, 47.1kΩ respectively. The ratio of there reciprocals matches the ratio of three feedforward coefficients, which are 0.6704, 0.2442, 0.308 as derived before. We will not elaborate again on the design of these OTAs. There proper operation dictates the loading has much smaller impedance than the output impedance, otherwise the voltage current converter will function as a voltage amplifier. The cascode branch current of these OTA are set after considering the input signal magnitude and its trade off with g_m, which cannot be too small otherwise resistor will become extremely large. Besides, smaller current may affect the speed and the judgement of the following comparator. The outputs of these three transconductance cells are shorted and fed into the following current comparator, which will be described in the next section.

4.5.5. Current Comparator Design

Comparator in this design acts as a single bit quantizer. For commonly used voltage comparators, we can use high gain differential amplifier, whose resolution is defined as $\frac{V_{OH}-V_{OL}}{A_v}$, where A_v is the gain of the amplifier. This kind of comparator is speed limited due to its low dominant pole. Another more widely used comparator is called regenerative comparator, It has very low propagation time delay and high resolution. This is due to the fact that a latch is adopted which is conceptually illustrated in Fig. 4.20.

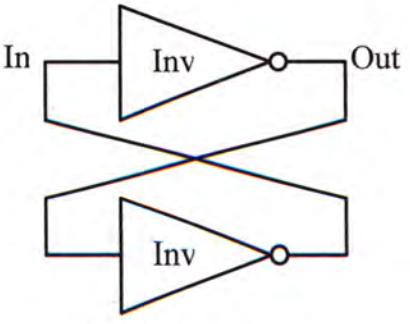


Fig. 4.20 Latch

This is basically a positive feedback architecture. Even if the input In is very small, the positive feedback could quickly put the output Out to full swing.

A high speed low gain opamp is usually included preceding the regenerative comparator to avoid kick back and further increase the resolution [36]. In this case, current to voltage conversion is required to handle the current input generated from the feedforward circuits. Diode connected MOS transistor is considered mainly due to its current sinking ability and low impedance looking into the shorted drain/gate terminal. Additional current source is added to set the output biasing voltage of the I-V converter. The whole structure of the current comparator is depicted in Fig. 4.21.

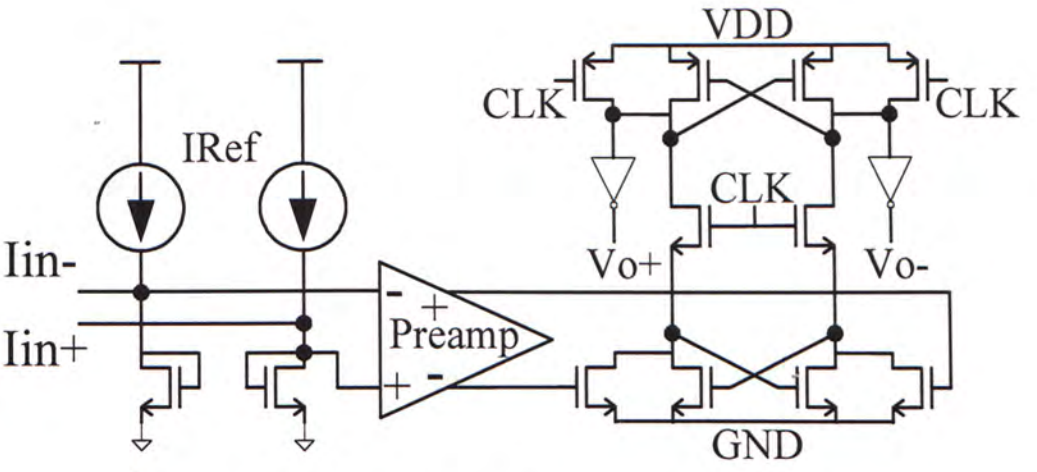


Fig. 4.21 Current Input Comparator

Two 10kHz current inputs with 8uA and 10uA magnitudes are fed into I_{in-} and I_{in+} respectively for testing purpose. CLK of the comparator is set to be 25.6MHz. The input and output waveforms are shown in Fig. 4.22.

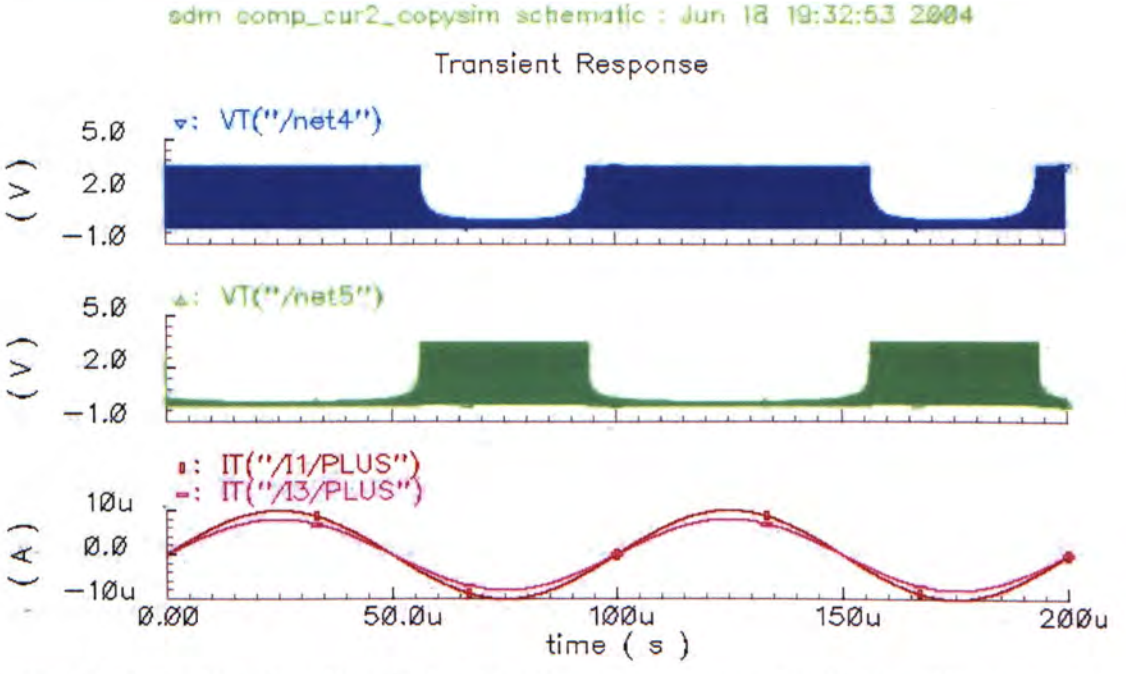


Fig. 4.22 Transient Simulation Result of the Regenerative Current Comparator

By observing the simulation result, we see that the propagation delay is only around 200ps. And the minimal detectable current difference is 0.7u with the 25.6MHz sampling clock.

4.5.6. Dynamic Element Matching Design

As mentioned before, the feedback circuitry of the sigma delta modulator connects to the input stage, where any noise introduced can not be suppressed, thus we should guarantee the feedback circuits of I path and Q path are matched. Practically, the feedback resistors of two paths, which is the main contributor of mismatch, cannot be identical, because of process variation. Furthermore, interleaving technique in layout cannot be applied to the feedback resistors because they conduct different signals, parasitic delay and cross talk should be avoided in these sensitive paths. Thus we resort to dynamic element matching (DEM) to reduce the effect caused by resistor mismatch.

The principle of DEM is to average out the noise caused by mismatch through shared using of mismatched components. Take a circuit with two mismatched paths as an example, a chopper is added immediately before or after these two paths, if the control voltage of the DEM algorithm is high, then the chopper straightly couple signals in these two paths, if control voltage is low, chopper cross coupled the signals. Thus effectively for each output signal, it may come from any of the two paths depending on the DEM algorithm. A simplest DEM control signal is a clock with fifty percent duty cycle. In this case, two paths are equally used for each input, thus the mismatch between these two paths are averaged out. But the clock signal could mix with the large out of band quantization noise and therefore increase the inband noise [2]. Even if we apply pseudorandom DEM control signal, the resulted noise is spreaded out over the whole band, which also dominates the low frequency noise [2].

In this work, the DEM algorithm proposed in [2] is employed. To understand the working principle of this DEM algorithm, we first briefly describe the method here. The mismatch of feedback resistors manifest itself as gain mismatch, suppose the gain mismatch is Δ, then the output of the complex modulator approximately becomes

$$Y \approx (I + jQ) + \Delta(I - jQ) \tag{4.13}$$

The first part at the right hand side is the desired one, while the second part represents the image signal, which is caused by the mismatch of feedback resistors.

The algorithm presented in [2] controlled the DEM chopper in this way: if the output bits of the I and Q paths are the same, the chopper is cross coupled, otherwise, it is coupled straight through. In mathematical forms,

$$Y \approx (I + jQ) + \Delta(I - jQ) \times I \times Q \tag{4.14}$$

Gain mismatch is modulated by the product of output bits of I and Q, here note that I and Q outputs have two levels 1 and -1. Both of their squares equal +1. Thus we can reduce the above equation to

$$Y \approx (I + jQ) - j\Delta(I + jQ) \tag{4.15}$$

It is evident that the error spectrum now is identical with the desired one, only with a phase shift of 270 degree. Image signal term shown in equation (4.13) is totally removed.

Obviously, the DEM signal can be generated using simple exclusive OR gate and NOT gate, the whole transistor level feedback circuitry with DEM is shown in Fig. 4.23.

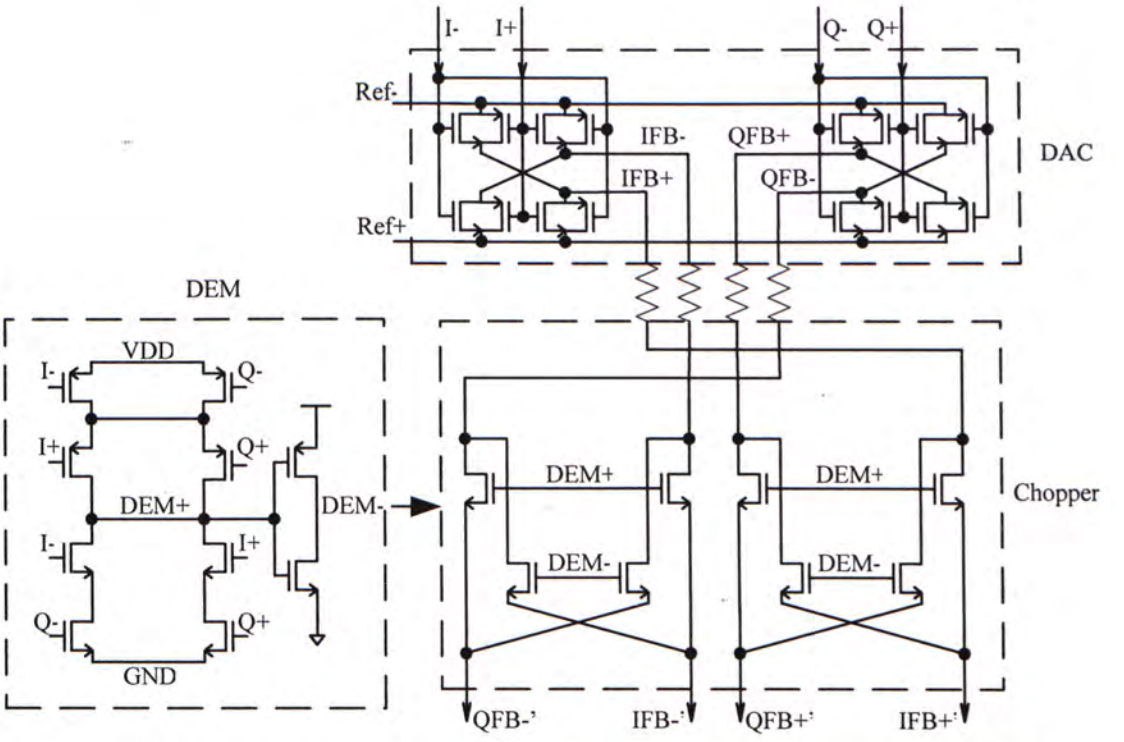


Fig. 4.23 Feedback Circuits for I/Q paths with Dynamic Element Matching Scheme

Minimum length of transistors is used to minimize parasitic capacitors, transistor width W is chosen to be around several micrometers to 10um to keep the internal impedance neglectably small. CMOS switches set widths of NMOS and PMOS to be 4um and 10um respectively to get nearly constant internal impedance regardless of V_{ds}.

4.5.7. Mixer Design

Mixer is an important part of the IF input complex sigma delta modulator. It converts the IF input signal to baseband signal, which is fed into the following sigma delta modulator. The noise introduced in this stage goes through the sigma delta modulator directly without any noise shaping, so it's mandatory to keep the inband noise as less as possible.

The mixer adopted in this work takes the same structure of a chopper as shown in Fig.

4.23 except that the gate control signals are different. Here LO signals already shown in Fig. 4.4 drive the transistor gates. Clock feedthrough could be a serious problem in such case, dummy transistors or CMOS switches can be employed to relieve this issue, but they require additional clock signal which may complicate the design. Practically, fully differential implementation is sufficient to suppress the clock feedthroughs and other common mode noises. Besides, nonlinear internal impedance of switch also introduces noise, fortunately, the input resistors have much larger resistance, thus the distortion can be kept very small [7].

Simulation of the RC integrator with the integrated mixer and without are conducted respectively, the settings are as follows:

For RC integrator with integrated mixer, the frequency of input differential signals is 20.05MHz, Two LO signals (For single I path or Q path) are square waves and 180 degrees output of phase, as shown in Fig. 4.3. Frequency is set to be 20MHz, their duty cycles are 24%, which models the real clock signals for proposed resistor sharing technique.

For pure RC integrator, the input frequency is 50kHz. Other settings are the same with the above one. R equals 100kΩ, C equals 4pF, magnitude of input signal is 50mV, W/L of switching transistors is 3um/0.35um. The spectrum of differential output is given in Fig. 4.24, the plot on the left hand side corresponds to the pure integrator, while the right picture corresponds to integrator with integrated mixer. It is observed that the desired output signal of pure integrator is about 7dB stronger than the other one. This makes sense because even for LO signals with 50% duty cycle the theoretical desired output magnitude will decrease to $2/\pi$ times of the pure one. The main difference between these two plots is that odd harmonics exist in the integrator with mixer, while the other one sees no distortion. This is due to cross modulation between input signal and harmonics of LO signal caused by finite internal impedance of switches. Even harmonics doesn't exist thanks to the fully differential architecture. The third order harmonic distortion of the right plot is 79dB below the desired signal. Further simulation with full range input signal shows the

third order harmonic distortion is 82dB. When referred back to the input, the maximum input SNR is around 73dB. 9dB loss is due the amplification of desired signal is 3 times that of third order harmonic, which corresponds to 9.5dB. The above derivation is a rough estimation when full scale input is applied. For various magnitudes of input signals, the results vary, but deviate within several dB. If we increase the value of the resistors or W/L of switches while keeping other settings unchanged, the resulted input SNR is larger. This is reasonable because now voltage drop over the internal impedance is smaller and thus harmonic distortion is reduced.

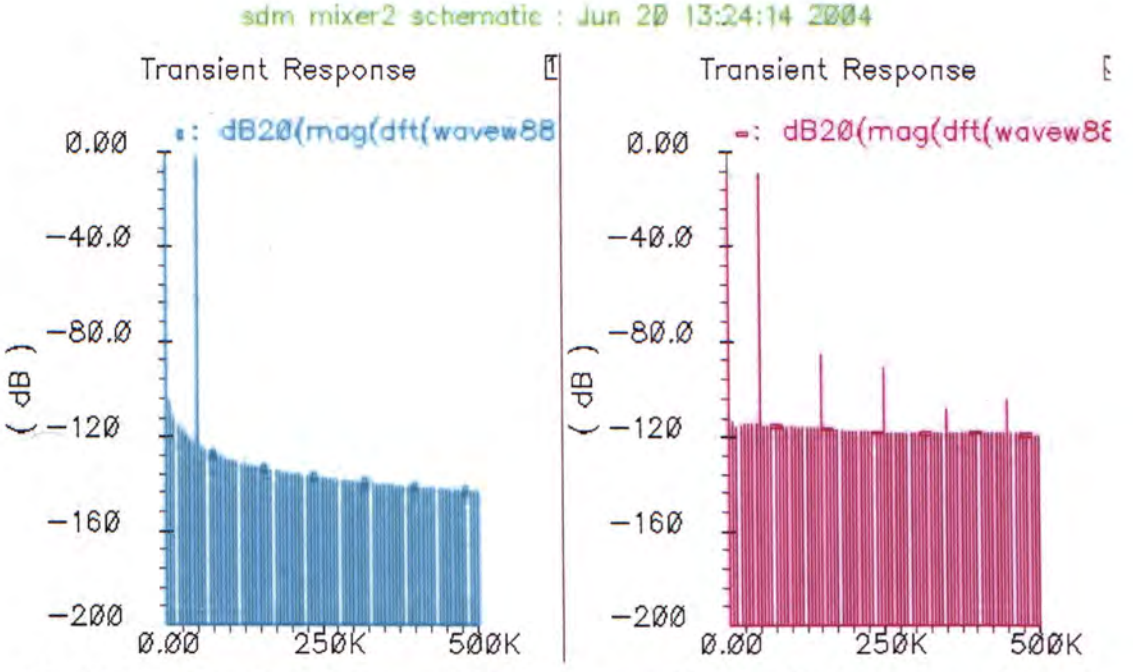


Fig. 4.24 Transient Outputs of RC Integrator without and with Integrated Mixer

The noise floor shown in the above figure is mainly due to the transient part of the output described by equation 4.6 and windowing effect of Fourier transform. Actually the gain of the OTA should be very large in order to make the transient part sufficiently small and its spectrum doesn't cover up the harmonics. Ideal fully differential OTA are used in the above simulation and the gain is set to be 10M to minimize the noise floor caused by transient part. Note that increasing the gain further may results in singular matrix error when doing simulation.

Simulation results show that if the switches in the mixer are controlled by traditional clock scheme, i.e., clock signals with 50% duty cycle, the output desired signal is about 3dB stronger than proposed one, noise floor and harmonics are about the same.

4.5.8. Clock Generator

The proposed resistor time sharing technique requires new clock scheme, which is shown in Fig. 4.4. For easy reference, it is given here again in Fig. 4.25. The most critical issue here is to guarantee the specified phase shifts as shown in the diagram. 90 degree phase shift between I path and Q path is mandatory to theoretically eliminate the image signal. Besides, the four clock signals cannot be overlapped, that means, at the same time at most one switch is on, otherwise cross coupling between I path and Q path would occur at the overlapping intervals. A four times fast reference clock is utilized to accurately generate the desired quadrature clock signals. In another word, if the external clock is accurate enough, the produced clock signals would have the same accuracy theoretically. The clock generator is shown in Fig. 4.26.

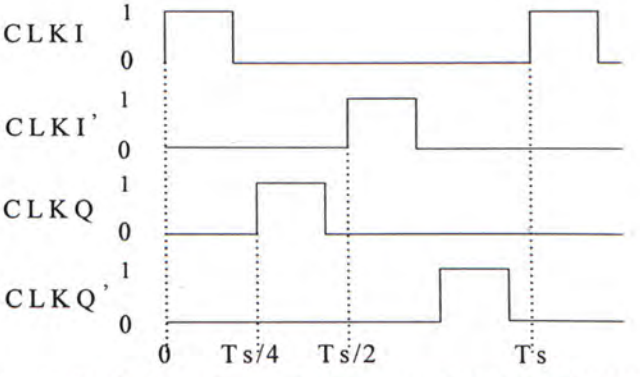


Fig. 4.25 Clock Signals for the Proposed CT I/Q ΣΔ Modulator

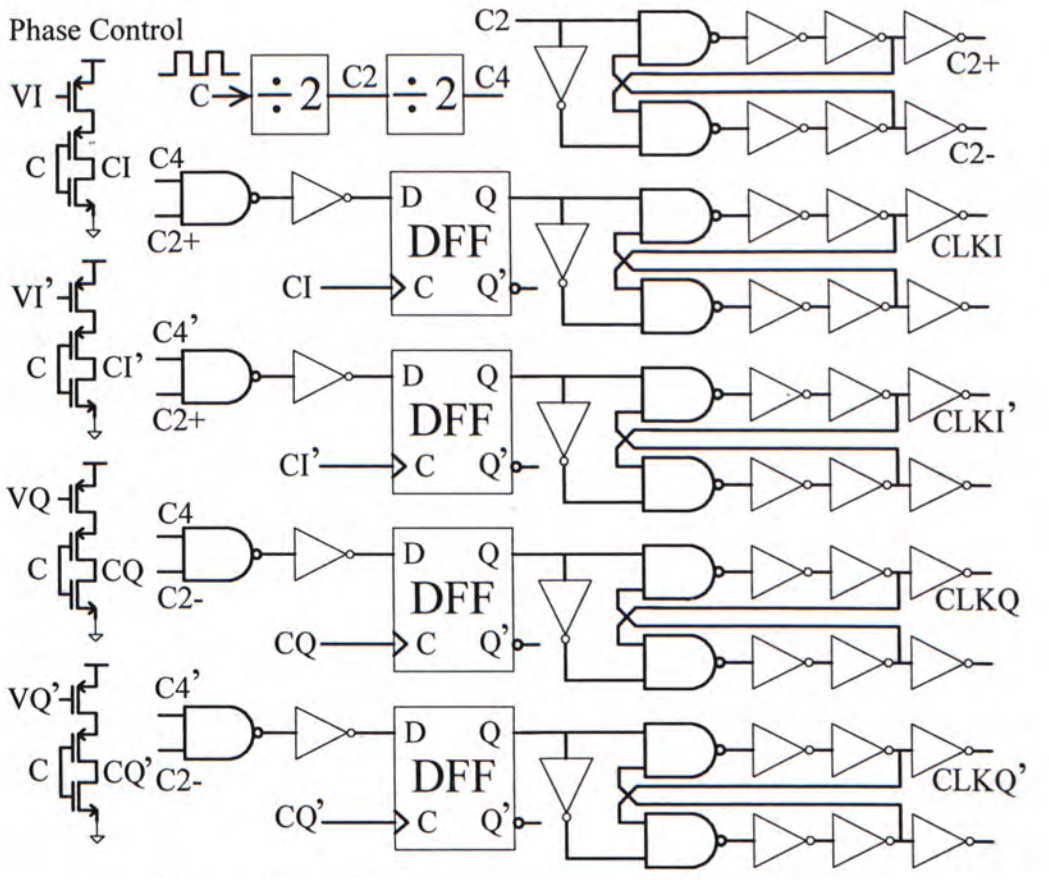


Fig. 4.26 Clock Generator with Accurate Phase Tuning Circuit

The delay loops on the right of DFFs narrow a little bit the pulse width of their input signals. C2 goes through a delay loop and thus the outputs C2+ and C2- possess less than 50% duty cycles. Then C2+/C2- and C4/C4' go through AND gate at each of the four clock producing paths. The DFFs can produce square waveforms with accurate 25% duty cycles as long as the reference triggering clock has stable period, 25% duty cycle is guaranteed in stead of 50% duty cycle since the data input of DFF has less than 25% duty cycle. Finally, the outputs of DFF go through delay loops again to generate nonoverlapping clock signals with specified phase shifts.

In practice, process variation and mismatch will cause minor phase error of the generated clock signals. Even 1 percent of phase deviation will result in considerable image signal as analyzed before. Thus a phase tuning circuit is desirable to reduce phase mismatch between quadrature signals. Since only trivial phase mismatch exists provided that layout job is carefully done, only fine tuning circuit is useful here. The

phase tuning circuit proposed is also shown in Fig. 4.26, on the left of the main clock generator. A PMOS transistor is cascaded on top of an inverter, control voltage is imposed on the gate of the cascaded transistor. Four copies of such tuning circuit are needed to deal with four clock signals as well as for symmetry. Initially all control voltages are connected to ground, thus they only introduce an inversion operation before triggering the DFFs. The final outputs of the four clock signals all shift 90 degrees as compared with original output when no tuning circuit is added. If we change one or some of the control voltages of the tuning circuit, the phase(s) of corresponding path(s) will delay accordingly, depending on the amount of voltage changing. In principle, increasing the tuning voltage increases the internal impedance of the cascaded transistor, thus charging time also increases to get an output logic 1. In addition, since the loading is small parasitic capacitor, the charging time is virtually very short, tuning the gate voltage of cascaded transistor only slightly increases the charging time unless the gate voltage is set to a quite big value, then after reshaping by the following logical gates, the amount of phase shift changes while the waveforms keep exactly the same. In this way, fine tuning can be realized which is important in such a phase sensitive circuit.

Simulation is conducted to test the clock generator and the tuning circuit. The input reference clock frequency is 80MHz. All tuning voltages are set to be 0V and 1V respectively. Two sets of output clock signals nearly overlap as shown in Fig. 4.27. For each set, the clock signals are identical except for phase shifts of integer times of 90 degrees. The subfigure on the right zooms in a time slot when rising edge and falling edge occur, it can be seen that imposing 1V tuning voltage results in around 80ps delay, which account for 0.65% of a clock period. Increasing or decreasing the tuning voltage will lead to different clock delays.

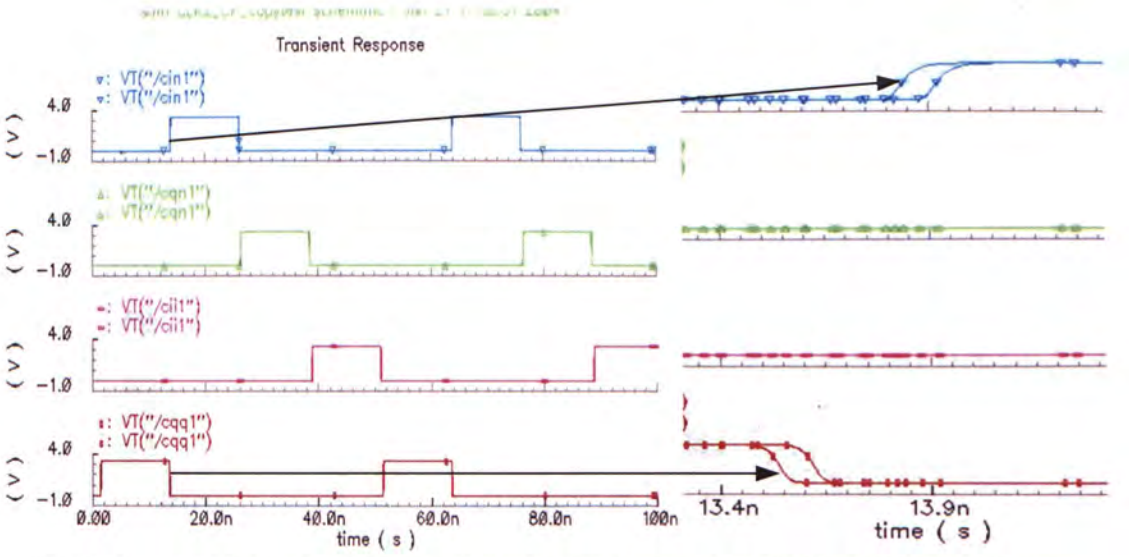


Fig. 4.27 Simulation Result of the Clock Generator with Phase Tuning Ability

4.6. Transistor Level Simulation of the Design

Up to now, most of the building blocks have been designed and presented. The remaining component of D flip flop is a standard one, it will not be elaborated here. The whole system is comprised of all the cells described thus far in this chapter. We can refer to Fig. 4.9.

First, a single path (I/Q) without integrated mixer is built up and simulated, it is basically a continuous time baseband third order sigma delta modulator. The coefficients and performance of building blocks have been presented before. The targeted application is GSM receiver, for which 100kHz bandwidth is required for each path of the complex modulator. 25.6M sampling frequency is adopted for the oversampling ratio of 128, as chosen during high level design. Input signal is a 50kHz sine wave with amplitude of 0.5V, which is half of the feedback reference voltage. Transient simulation time is set to process eight periods of input signal, which would result in 4096 digital output data. Matlab is used to help us analyze the simulated transient output from cadence by plotting its spectrum. Fig. 4.28 shows the output spectrum with the settings shown above.

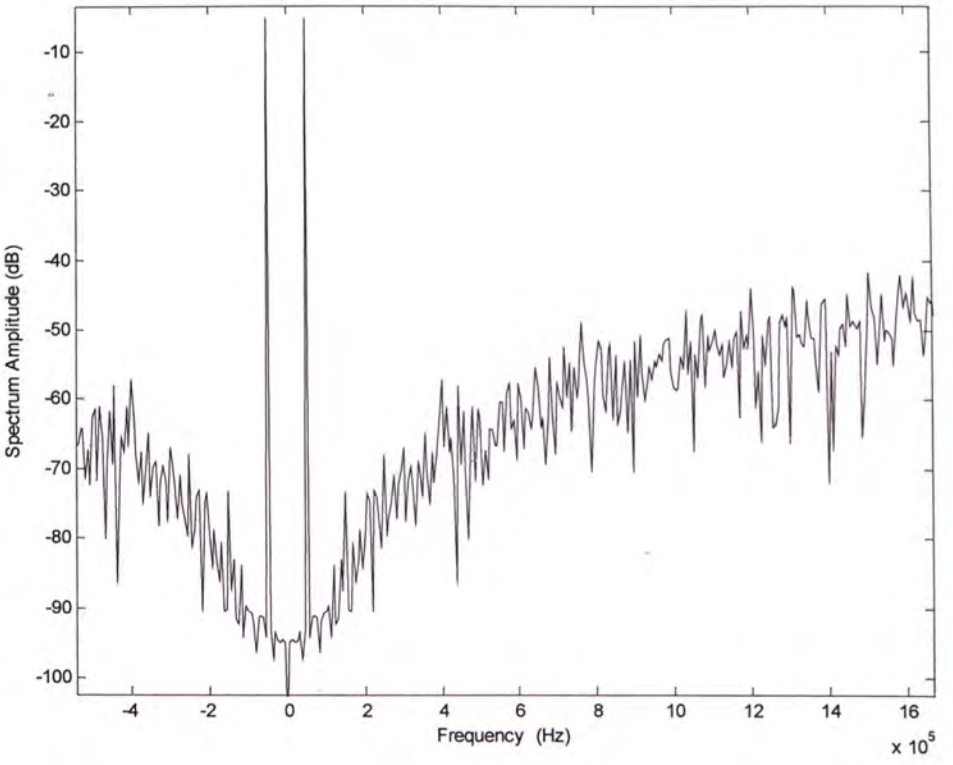


Fig. 4.28 Output Spectrum of Designed Third Order Sigma Delta Modulator

It is found that the noise floor is limited to -95dB, thus the calculated SNR with 100kHz band of interest is only around 80dB. It degrades 20dB compared with ideal simulation in Simulink. In order to identify the major noise source, ideal components like voltage controlled voltage source (VCVS) are used to replace the real OTAs and also the feedforward circuitry, thus only the quantizer and feedback DAC are real. But simulation result also shows that noise floor can hardly exceed -100dB. The noise introduced by quantizer is heavily attenuated thus it shouldn't be the dominant noise source, careful observation also shows it functions correctly and the resolution is very high. It seems that the remaining DAC which is connected to the input stage is most suspicious for limiting the performance, but even if we eliminate the use of DAC and take the DFF outputs as feedback signal directly, the situation doesn't improve a bit. It is doubted that all the secondary effects like finite gain(even for ideal VCVS), excess loop delay, initial sampling time, simulator accuracy, etc contribute together to the limited noise floor compared with ideal one. This issue could be further explored but for this work, we mainly concern about image rejection

of complex modulator, relative low SNR is also acceptable.

After building up the main third order sigma delta modulator with fairly good performance, mixer is integrated and subsequent simulation shows over 10dB SNR is lost, where the LO frequency is comparable to the sampling frequency. This is reasonable as explained previously during high level design.

Finally, the whole IF input complex sigma delta modulator with proposed time sharing technique is simulated, with the same simulation settings as before, we get the following output spectrum in Fig. 4.29.

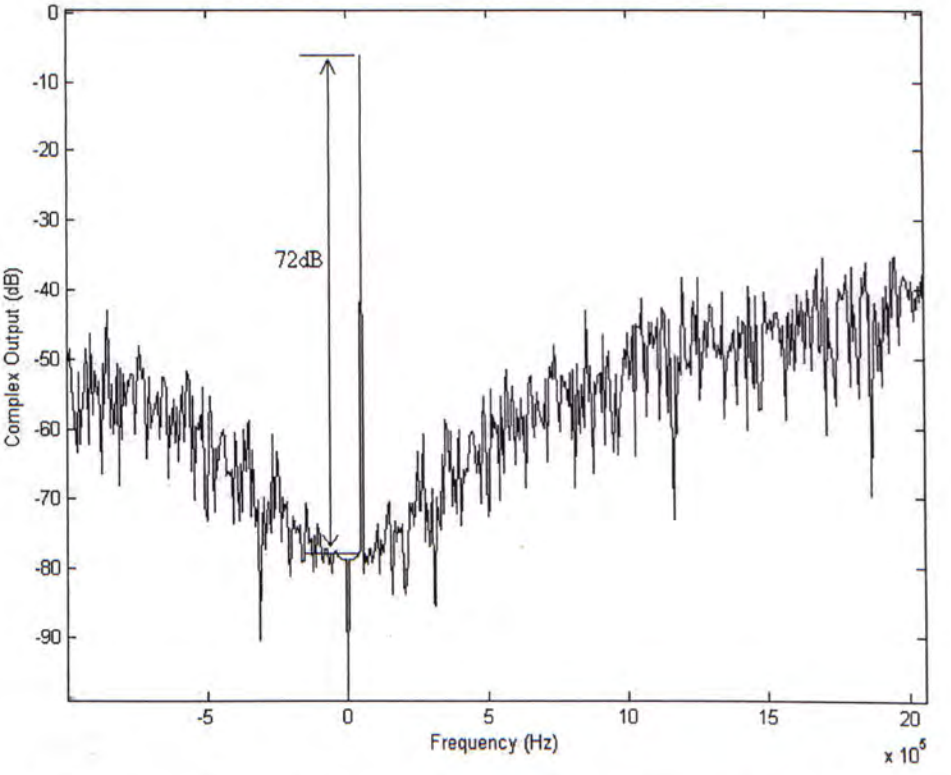


Fig. 4.29 Output Spectrum of the IF Input CT I/Q ΣΔ Modulator

Image signal is not present (at least 72dB) judging from the output spectrum. Since I path and Q path are identical copies and input resistors are shared, the image signal is theoretically eliminated as long as LO signals are 90 degree out of phase. The calculated SNR is 61dB, which is 23dB less than the ideal result from high level simulation. The SNR loss here is similar to the loss of single path sigma delta

modulator compared with its corresponding ideal one.

Power consumption of the designed work is also simulated, the current flowing out of VDD is integrated over a whole period of input signal. The average power is calculated via the equation below

$$P = \frac{V \int_0^{T_S} I_{VDD} dt}{T_s} \tag{4.16}$$

Total power consumption of the whole system is 14.8mW.

4.7. Layout of the Mixed Signal Design

4.7.1. Layout Overview

Layout is the bridge between factory fabrication and chip designer. After finish designing in the transistor level, the schematic is not ready for fabrication. A certain format is required for foundry to mass produce the chip. This kind of format is referred to as layout. In essence, layout consists of polygon wires, metal wires, vias, silicon transistors, etc. The layout normally has several metal and polygon layers, for the convenience of complex interconnections.

Chip layout can be implemented using many different techniques including gate arrays, standard cells and full custom designs. Full custom design is suitable for analog and mixed signal design, and is also widely used where large volume is required. But as a drawback, the turnaround time is usually longer.

For analog and mixed signal circuit layout, automation cannot play an important role by far due to the intricate pattern of the circuit. Thus thorough understanding of the circuit theory, semiconductor fabrication and device physics is needed to successfully do the layout jobs for analog and mixed signal circuits.

For this mixed signal design, great care should be paid to the crosstalk between analog and digital signals. Careful layout is very important for successful fabrication. Otherwise the performance of the design may degrade by a great extent, or even the chip will not work.

In this layout design, generally bottom up approach is adopted, which means the individual components are drawn first, and finally combine them in the whole layout. None the less, initial floor planning were conducted and polished for several times. At this stage, the size of the whole design, the pad layout and individual component's location were roughly predicted and planned. The important issues are that we should keep the area as small as possible, and the crosstalk between components, wires and analog, digital parts should be kept at lowest level. Of course, since this design is a symmetry one, we should try our best to make the whole layout as symmetric as possible. This also applies to the individual unit.

The following sections first elaborate the layout of some typical cells and deal with some important layout issues, finally layout of the whole work is presented and simulation result is given. AMS 0.35um technology with quadruple layer metal and double-poly is adopted for this work.

4.7.2. Capacitor layout

Capacitor is one of the common passive components that are frequently used in integrated circuit. It serves as compensation, integrating, etc. Most analog and mixed signal circuit employs some capacitors to implement certain functions. In layout, capacitor is relatively bulky device, even several hundred femto farad will occupy a considerable amount of area. In order to keep the chip cost low enough, the total area of the chip is usually very small, thus we cannot integrate large value capacitors in a chip. Generally, 100pF is the upper limit.

There are several kind of capacitors, to name a few that are practically used, they are oxide capacitors, which employs silicon dioxide as its dielectric, junction capacitors, etc. Oxide capacitors has several subtype, like poly-poly capacitors, MOS capacitors(gate oxide capacitor). Junction capacitor uses the depletion region surrounding a reverse biased junction as dielectric.

In this design, poly-poly capacitors are chosen. The sheet resistance of this sort of capacitors is small and voltage modulation can also be minimized by heavy doping. The temperature coefficient of a poly-poly capacitor is typically less than 250ppm/C. Parasitics of the poly cap

Though ideally the two plates of the poly-poly capacitors are identical, but in layout, the upper plate usually has less parasitic capacitance than the lower plate. The main reason is the lower plate is nearer to the substrate (ground), while the capacitance is inversely proportional to the distance between two plates. Besides, we also have capacitance between poly1/poly2 and metal1/metal2. We should take these effects into account while designing in schematic level. Parasitic resistor also exists in real capacitor, which is formed by the sheet resistance of the cap and contact resistance. Actually, the cap is a distributed RC network.

Common centroid is a very important technique to achieve good matching of concerned components, because during fabrication and packaging, stress gradient is introduced, especially along the edges and corners of the die.

In order to make the matching of capacitance even better, the following practice should be observed [37]:

1. Use identical unit capacitor, otherwise they match poorly.
2. Unit capacitor should have lowest periphery to area ratio, because periphery variation is a major source of random mismatch of capacitors.
3. Larger matched capacitors are preferable to reduce random mismatch.

4. Add an Nwell under the capacitor array to shield the substrate noise.
5. Place dummy capacitors around the outer edge of the cap array to prevent the matched caps from lateral electrostatic fields and variations in etch rates.
6. Adopt cross couple arrayed capacitors to minimize the effects introduced by oxide, stress and thermal gradients.
7. Capacitance of leads connecting the caps should be minimized and matched too.
8. The matched capacitors should be placed well away from power devices because the cap value is temperature dependent.

A sample layout of capacitor in this design is given in Fig. 4.30.

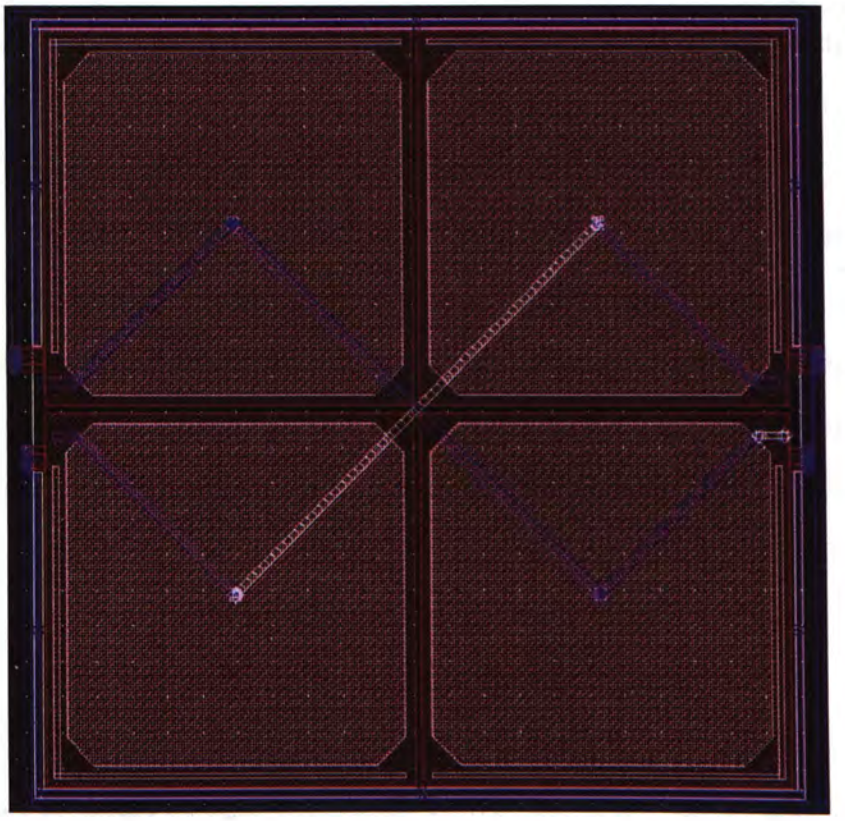


Fig. 4.30 Capacitors Layout Employing Common Centroid Approach

There are two poly caps with the same value in this drawing, each capacitor occupies two unit cap along the diagonal, which makes a common centroid structure. Dummy as well as N well is employed as explained above. Ninety degree angle in unit cap is avoided to better accommodate to fabrication. Symmetry of the layout should be

taken care of, thus parasitic caps could hardly affect the desired cap ratio.

4.7.3. Resistor Layout

Resistor is very useful in analog and mixed signal circuit design. It can acts as voltage divider, voltage to current converter, and set the time constant in filter together with capacitor, etc. Like capacitor, integrated resistors have poor tolerance of absolute value, but precise in ratios of matched resistors.

In standard CMOS technology, several types of resistor are provided, such as poly1 poly2 resistors, N-well resistors, diffused resistors, metal resistors, etc. Metal resistors are usually used for constructing current sense circuits. Poly resistors shows high or low sheet resistance depending on doping, and current flow is uniform because the width of poly is kept constant for a particular resistor. But tiny variation of width also exists due to limited accuracy a certain technology can provide. Besides, temperature coefficient of poly resistor is quite large, normally bigger than +-250ppm/C. But compared with diffused resistors, it has a sharp improvement in terms of temperature sensitivity. So, diffused resistors are replaced by poly ones in most design. N-well resistor can offer high sheet resistance but temperature coefficient is even larger. In general, poly forms the best resistors available on most processes. The layout can be smaller and tank modulation doesn't exist.

For the parasitic issue, contact resistance and parasitic cap between poly and substrate/metal should be dealt with carefully to optimize the performance.
In layout, matching of resistor can be improved through many methods. We should first understand that mismatches comprise of random mismatches and systematic mismatches. Random mismatch stems from fluctuations in dimensions, dopings, oxide thickness and other parameters. Systematic mismatch are caused by contact resistances, process biases, mechanical stresses, temperature gradients, etc. It's

necessary to minimize the systematic errors through various techniques to achieve good matching. Below lists some important practical rules for matched resistor layout [37]:

1. First guarantee the resistors you want to match are the same type, otherwise their characteristics vary much.
2. Resistors should be of same width, because they are dependent on temperature and stress.
3. Width of resistor should be sufficiently large, thus make the width variation relative small.
4. Make the shape of resistors as identical as possible, the different corners, contacts and shapes can easily increase the mismatch.
5. Place the resistors close enough and add dummies, where possible, interdigitate arrayed resistors to prevent the effects of several parameters' gradients. Dummies can make the resistors see the same adjacent structure, thus make the fabricated resistors largely the same.
6. Place the resistors around the middle of the die and away from the power devices. Because in the middle, the stress distribution is minimal. Power devices can heat up the ambient resistor, so it's better to put the resistors far away.

Under the guidance of the above rules, resistors layout are relatively easily done. The width of all resistors in this design is chosen to be 10um, which is 12.5 times the minimum width. Dummy structure is also provided and resistors whose ratios are important are put close to each other.

4.7.4. Power and Ground Routing

Power and ground wires are critical in layout, since noise introduced by different components can couple from each other through power and ground lines. This is a big problem because power and ground have finite internal impedance, the larger it is,

the more severe the coupling problem is. In order to alleviate the coupling problem, we should observe the following practice [37]:

1. Power and ground lines should be wider enough to reduce the wire impedance.
2. Power and ground lines should have large decoupling capacitor, it is also recommended that we route power lines immediately on top of ground lines to obtain large parasitic capacitor.
3. Power and ground lines should use the higher metal layers, because the top layers are thicker and less resistive.
4. Power and ground lines should be put away from the noisy components and wires.

In this mixed signal design, various power supplies are needed, i.e., analog circuit VDD and GND, analog substrate GND, digital circuit VDD and GND, digital substrate GND, isolation N-well VDD and GND, etc. Except for the isolation supplies, each power supply has 8-10um wide metal to conduct the subtotal currents. The metal width is chosen to be around three times wider than required width which can conduct certain amount of current. In general, root metals of supplies go through the whole chip straight and from which narrower branch supply metals outgrow. All VDDs and GNDs are separate in the chip, they GNDs are supposed to be connected together out of the chip. This practice is essential otherwise digital noise will couple through substrate, equivalent metal resistor, parasitic inductance of pad, etc to affect analog circuits.

4.7.5. OTA Layout

A sample OTA layout of a V to I converter in the feedforward path is shown in Fig. 4.31 to illustrate some general considerations of layout. Note that interconnections among main OTA, CMFB, bias are not displayed because these sub building blocks are rearranged in the whole layout.

It can be seen that the main OTA and CMFB is almost exactly symmetric. Since the transistor width is normally much larger than its length, multiple gate fingers are used to get reasonable unit W/L ratio to enhance the accuracy during fabrication. Common centroid layout of presumably symmetric transistors is adopted where possible to achieve precise matching [36], where their gate fingers interdigitate.

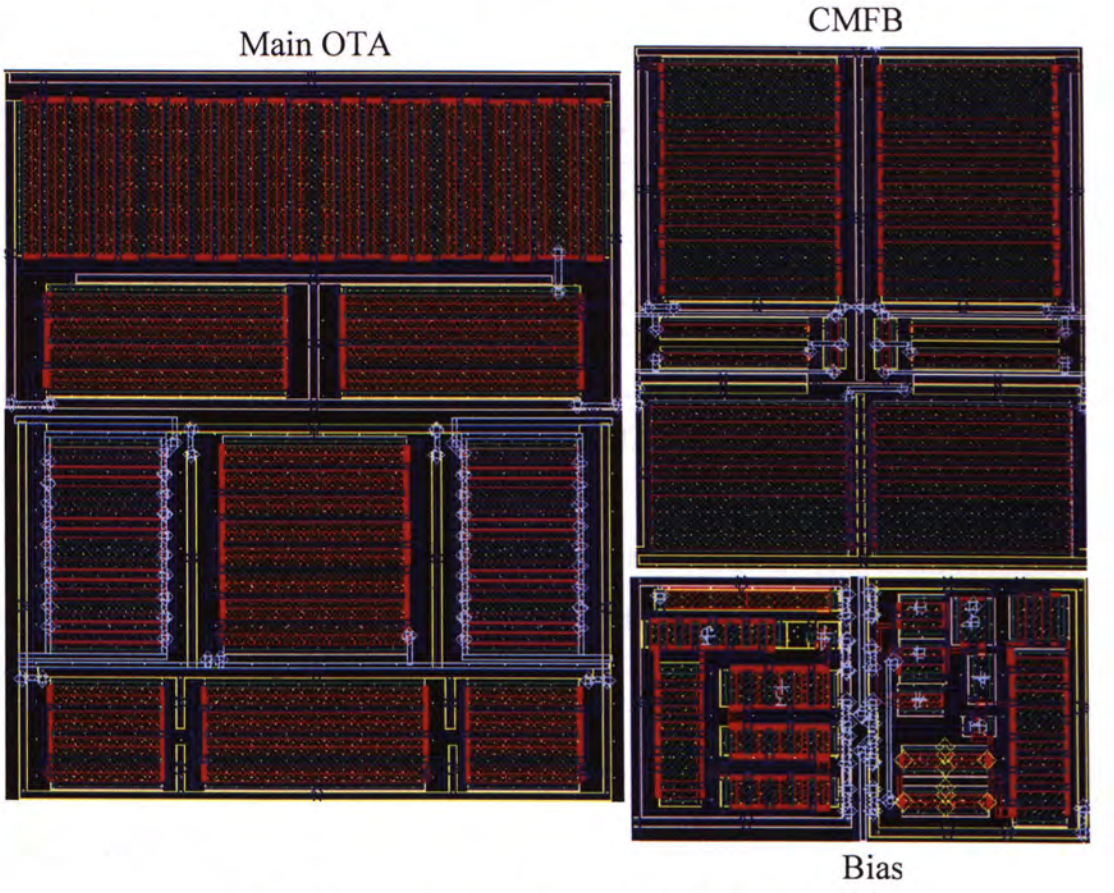


Fig. 4.31 Layout of an OTA in this Design

Post layout simulation and transistor level simulation of this OTA is conducted, their results of AC response are shown in Fig. 4.32.

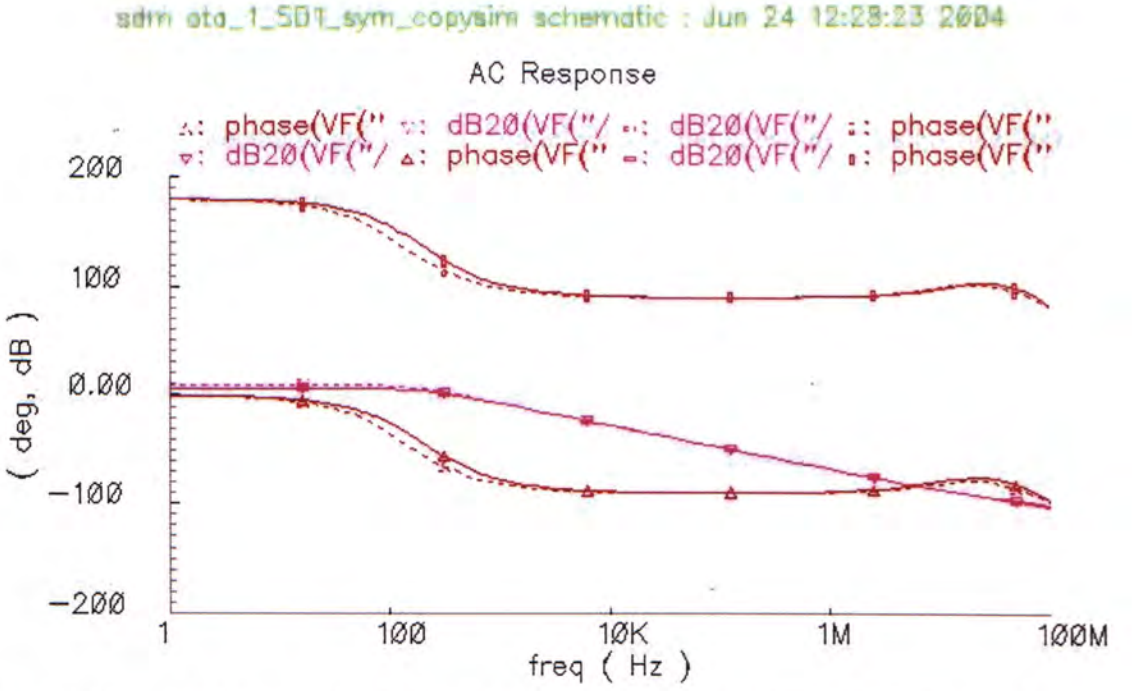


Fig. 4.32 Postlayout Simulation Result in Comparison with Schematic Simulation Result of the OTA

The dashed lines correspond to transistor level simulation results. It is observed that the resistor degenerated OTA gain degrades 3.5dB for postlayout simulation, while the unit gain bandwidth is about the same.

4.7.6. Chip Layout

The whole design is a mixed signal circuit. Digital part and analog parts should be separated to avoid cross coupling. Power supplies of digital circuit and analog circuit are provided independently. In addition, isolation technique is adopted to protect analog circuits from the digital noise. A commonly used shielding method is to employ N-well in between analog and digital part, this approach substantially increases the impedance between these two parts because doping below N-well is at least 10 times less than doping at the surface of substrate, which leads to tenfold increase in substrate resistivity between analog and digital parts. Besides, depletion region between N-well and substrate can also act as bypassing capacitors [36].

High frequency clock signals are arguably the most severe noise sources, they are routed above long narrow N-wells to isolate from other vulnerable circuits. The N-wells are connected to ground via parallel metals and substrate contacts next to the clock metals, noise introduced by the clock signals could find nearest ground and their influence are minimized.

Mixer is another critical part in the design. Not only because it connects to the input stage of the sigma delta modulator directly, any noise introduced here is not shaped, but also due to its mixed signal property, LO signals could easily affect the analog signals flowing through the mixer. Beside the technique that noisy LO signals are separated in N-wells, we also place N-wells around the I path and Q path mixers to protect it from the ambient noises, the N-wells around mixers are connected to an independent power supply which minimize noise injection to the fragile mixers.

For the floor plan of the whole layout, as shown in Fig. 4.33, we put digital part in the upper side, while analog part in the lower side. A relatively wide N-well is placed in between analog and digital parts to provide isolation, in addition, relatively noise insensitive degeneration resistors (N-well protected) in the feedforward path are also placed between these two parts to further widen their distance. The left half of the layout is I path modulator, Q path lies in the right half, they are fully symmetrical except for the shared clock generator, etc. The three stage integrators and feedforward V-I converters are put together to minimize any interruption from other noise sources.

For testing purpose, a total number of 46 pads are used in this design, most of them have ESD protections to prevent the MOS transistors from breaking down, except for the pads connecting IF inputs and feedbacks, otherwise excess delay will be introduced due to large parasitic capacitance associated with ESD protected pad. This is more detrimental to feedback paths. One reference clock for generating LO signals and sampling clock are provided separately. Input resistors and feedback resistors are

external to enable us to freely alter the integrator gain of the first stage, which is illustrated in last chapter. Degeneration resistors in biasing circuits are also not integrated on chip because they should be accurately set to provide precise biasing currents. The loading capacitors of second and third G_m-C are integrated but their values can be enlarged by external parallel caps through bottom pads shown in the figure. With the flexibility of tuning the gains of all three integrator, the sampling frequency of sigma delta modulator can be scaled up or down accordingly while keeping the normalized NTF unchanged. The functions of all pads are briefly described in the above diagram.

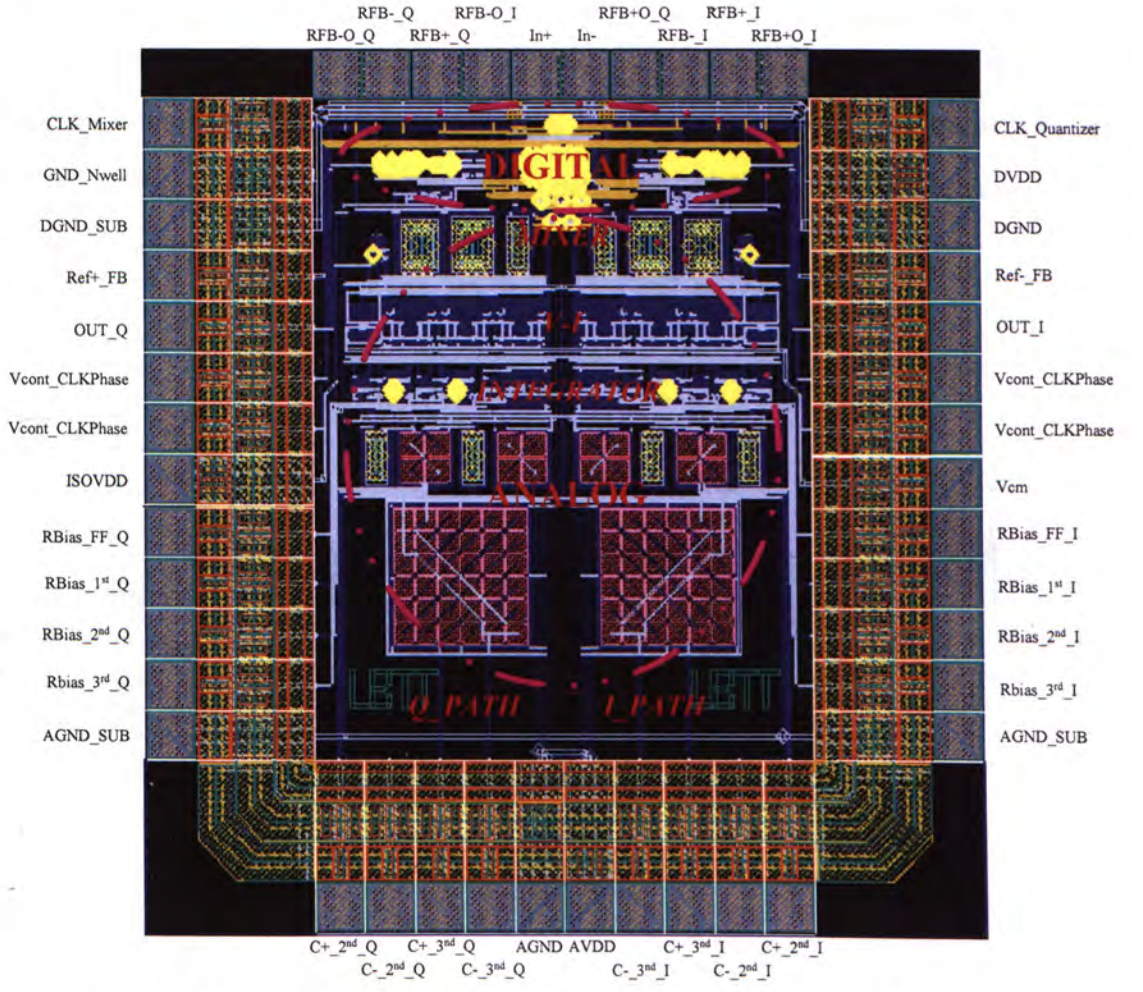


Fig. 4.33 Whole Layout of the IF input I/Q Sigma Delta Modulator

The size of the chip is around1.8mm*1.8mm, active area is smaller than $1mm^2$.

4.8. PostLayout Simulation

For testing, we applied a 25.05MHz sinusoid at the input, with the mixers clocked at 25MHz and sampling frequency of 25.6M. The simulation result, by complex adding the outputs of I/Q channels, shows that no image signal is observable, or, at least 69dB IR ratio. SNDR is calculated to be 61dB. The spectrum is illustrated in Fig. 4.34. Since the simulation time of this mixed signal circuit is formidably long, only 4096 points are taken.

Compared with schematic simulation result with the same setting, the simulated image rejection ratio from postlayout degrades 3dB as limited by the noise floor. The IRR or rather SNR degradation is caused by the extracted parasitic capacitors in postlayout simulation. Since I path and Q path sigma delta modulator are drawn in a highly symmetric way, image signal is well suppressed.

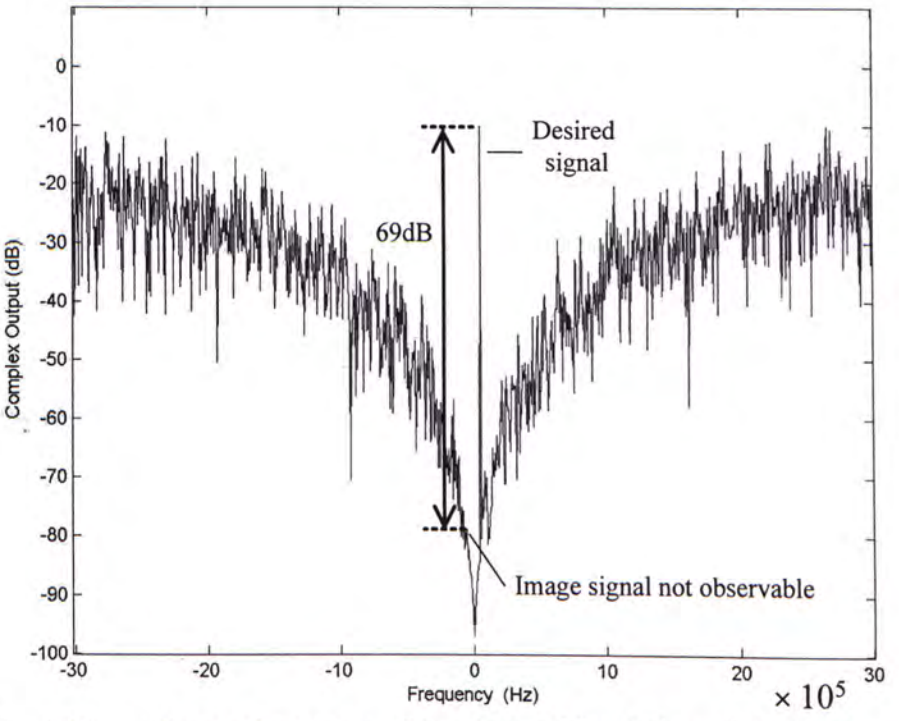


Fig. 4.34 Output Spectrum of Postlayout Simulation of the Design

The chip is fabricated using quadruple layer metal double-poly AMS 0.35um technology, PGA68 is chosen for packaging the chip due to its lower parasitic noise

compared with dual inline package.

5. Chapter 5

Measurement Results and Improvement

5.1. Introduction

Measurement is the last step in our research work. Up to now, high level simulation, transistor level implementation and Layout have been done successfully, final validation from measurement result is important. Postlayout simulation result is only a rough prediction of the chip performance. Process variation and mismatch occurred during fabrication could easily make the chip operate in a somewhat different way. In this chapter testing of the designed chip is presented, whose die image is given in Fig. 5.1. A specific printed circuit board for this chip is designed in order to doing the test. Measurement results are given and the performance is discussed. Finally, improvement of the design is presented especially on the topics of robust biasing and wide swing OTA.

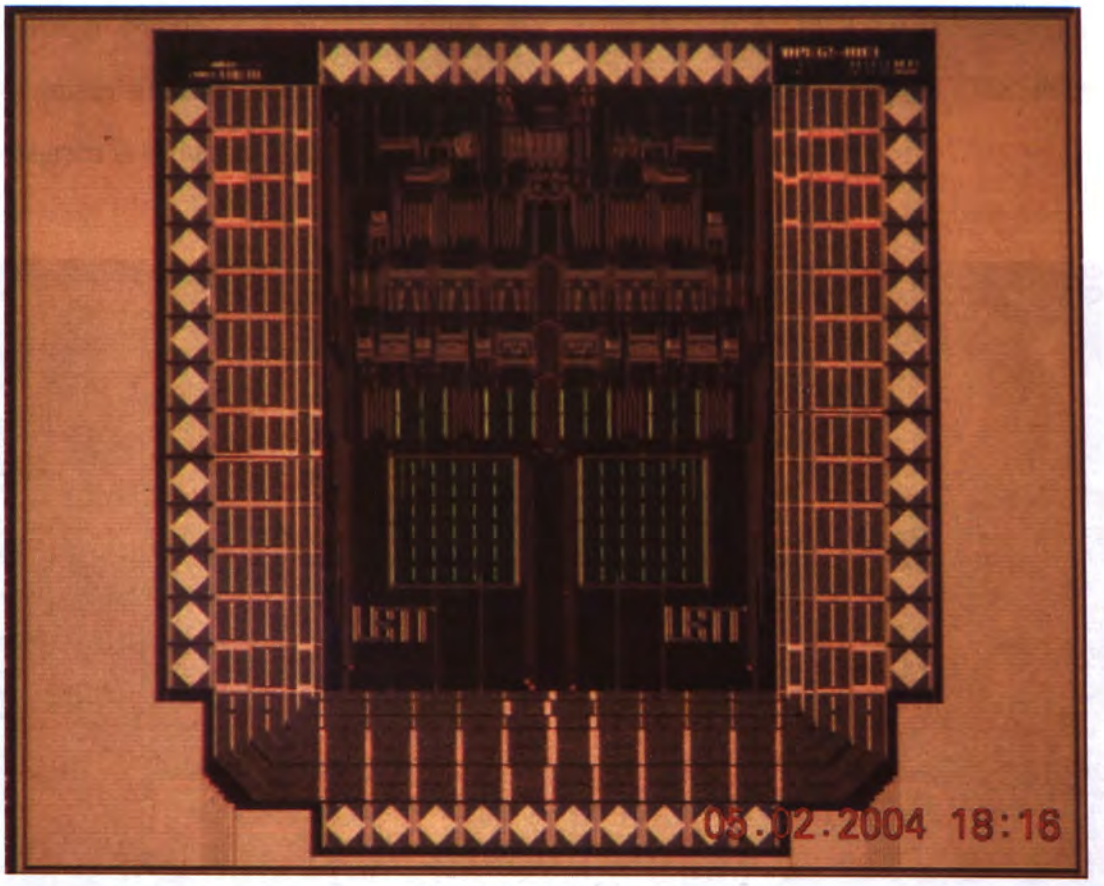


Fig. 5.1 Chip Photo

5.2. PCB Design

Printed circuit board (PCB) is a thin board to which various electronic components are fixed by solder. Component leads or chip pins may pass through holes in the board or they may be surface mounted, in which case no holes are required. Surface mount components usually introduce less parasitic noise mainly due to their compactness. The simplest kind of PCB has components and wires on only one side and interconnections on the other side. None the less, PCBs may have components mounted on both sides and may have many internal layers, allowing more connections to fit in the same board area.

For this work, double layer PCB is designed, i.e., chip and components are placed on both top and bottom layers. Two layers are essential for routing and placing various

external components in this design. Symmetry design of PCB is necessary for optimum matching between external circuitries of I path and Q path. The PCB diagram is shown in Fig. 5.2.

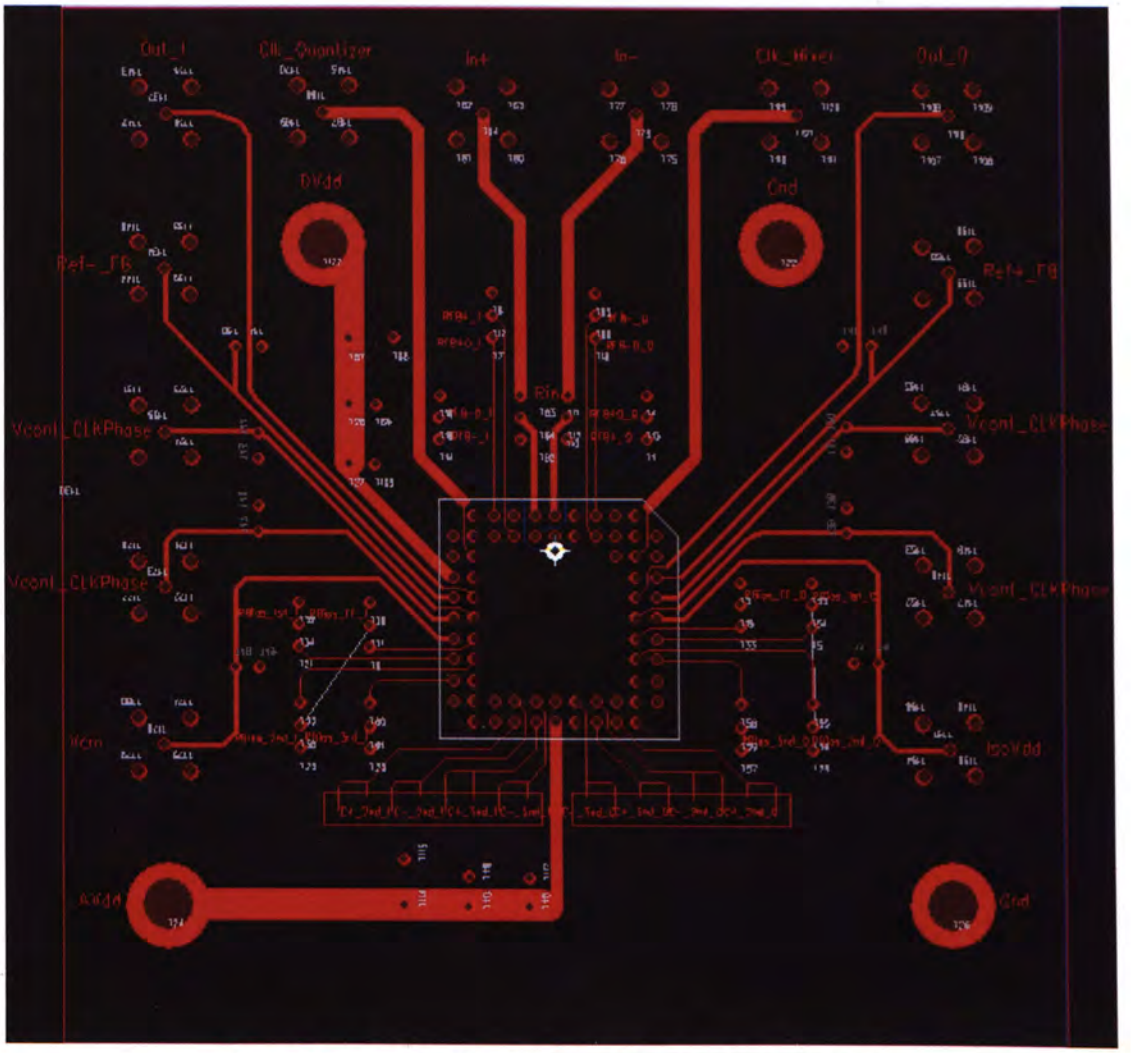


Fig. 5.2 Printed Circuit Board for Testing the Chip

Digital and analog power supplies are separate, while all GND pins of the chip package are connected to large areas of copper flooded over the top and bottom layers (not shown in this diagram otherwise the labels will be covered) BNC connectors are adopted for most input output pins to provide good shielding from noise. One set of three decoupling capacitors with different values of 10uF, 100uF and 1000uF is adopted for each power supply. They are placed near the package to effectively filter supply AC noise before they go into the chip. Three capacitors with

different values are used because single cap is most effective in bypassing noise whose frequency lies in a certain range. Decoupling capacitors are also extensively employed for other DC input signals. Tunable biasing resistors are selected to flexibly adjust the biasing currents. The input and feedback resistors are also tunable as explained before. All the components on the PCB are through hole components except for the optional loading caps, which are surface mounted. The red interconnections are on the top layer while the blue ones are on the bottom. Total size of this PCB is 12.6cm*12.8cm.

5.3. Test Setup

After designing the PCB, the board with specific interconnections and through holes is fabricated. Finalized PCB with various components soldered on it is shown in Fig. 5.3.

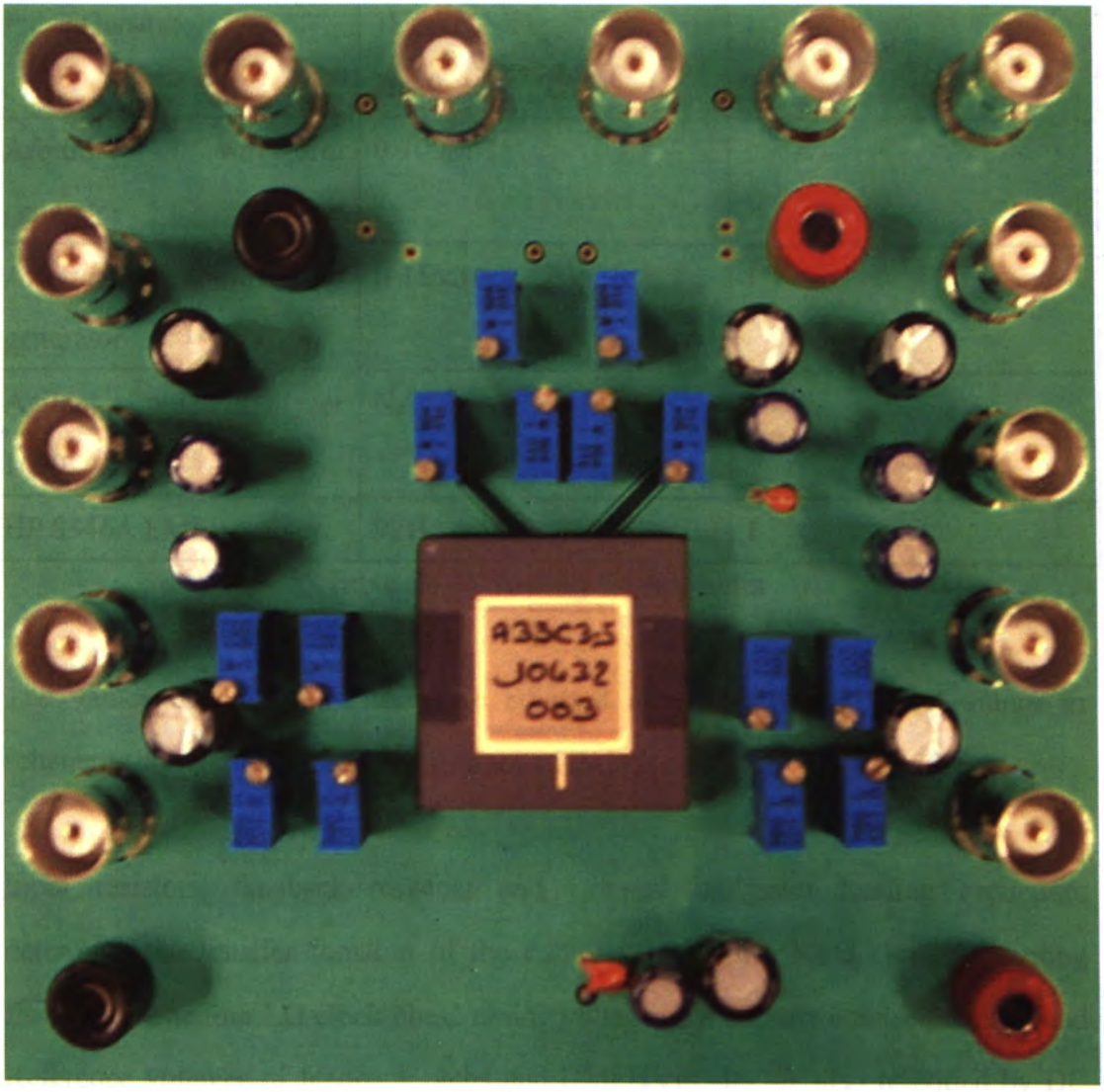


Fig. 5.3 PCB Under Test

In order to test the chip, the following equipments are used

Name	Major Spec	Quantity
HP DC Power Supply	0-20V/0-1.5A 0-35V/0-0.85A	2
Agilent Dual Output DC Power Supply	0-25V/0-1A	2
Agilent Infiniium Oscilloscope	1GHz 4GSa/s	1

Pulse Generator	1Hz-125MHz risetime 2ns-0.1s	1
Arbitrary waveform generator	0-100MHz	1
Arbitrary waveform generator	0-15MHz	1
Agilent Logic Analyzer 1690	NA	1
HP 8546A EMI Receiver	9kHz-6.5GHz	1

Table 3. Testing Equipments

The values of tunable resistors are adjusted according to the preset values in schematic simulation, parasitic resistance of PAD is also taken into consideration.

Input resistors, feedback resistors and external integrator loading capacitors determine the transfer function of the complex modulator for a certain sampling frequency. The four LO clock phase tuning voltages are initially connected to ground. Reference voltages of feedback paths and CMFB circuits are also provided by DC power supply.

The IF input differential signals are generated by an arbitrary waveform generator with two output channels. Two clock inputs are produced by pulse generator and arbitrary waveform generator. Digital output of the chip is connected to a spectrum analyzer which can handle input signal with frequency as low as 9kHz. Agilent logic analyzer is also used to capture the output data which can be processed in a computer.

5.4. Measurement of SNR and IRR

The equipments listed in the table 3 are only sufficient to test the chip with sampling frequency lower than 15MHz. In order to test the chip with sampling frequency of 25.6MHz as initially designed, a single input differential output balun is integrated on PCB to save one channel of a source generator which can then be used to produce high frequency clock signal. Actually this PCB is designed earlier than the one shown in Fig. 5.3, which doesn't use balun.

For testing, 20.05MHz IF input is applied to the balun whose outputs connect to the differential inputs of the chip under test. The frequency of reference clock generating four LO signals is 80MHz, which is four times the input IF frequency. Sampling frequency of the modulator is 25.6M. Transient simulation result shown by the oscilloscope indicates that the modulator under test isn't working well, because long sequence of logic 1 and 0 alternates. The input and feedback resistors are tuned in an effort to scale down the internal signals thus stabilize the modulator, but the transient output hardly changes.

Further testing finds that the biasing circuits oscillate. By probing the voltage at one end of an external biasing resistor, oscillation with frequency of several megahertz is observed. Careful probing validates that the two biasing circuits of first OTA and second/third stage OTAs oscillate. Biasing circuit for the feedforward OTA works properly. We will analyze this phenomenon in the following section.

Though unfortunately the biasing circuits oscillate, the IF input complex sigma delta modulator seems functionally workable, especially at lower sampling frequency. Fig. 5.4 shows the spectrum of one of the modulator's output. The frequency of input signal is 10.05MHz, with magnitude of 400mV. Reference clock frequency and sampling clock frequency are 40M and 10M respectively.

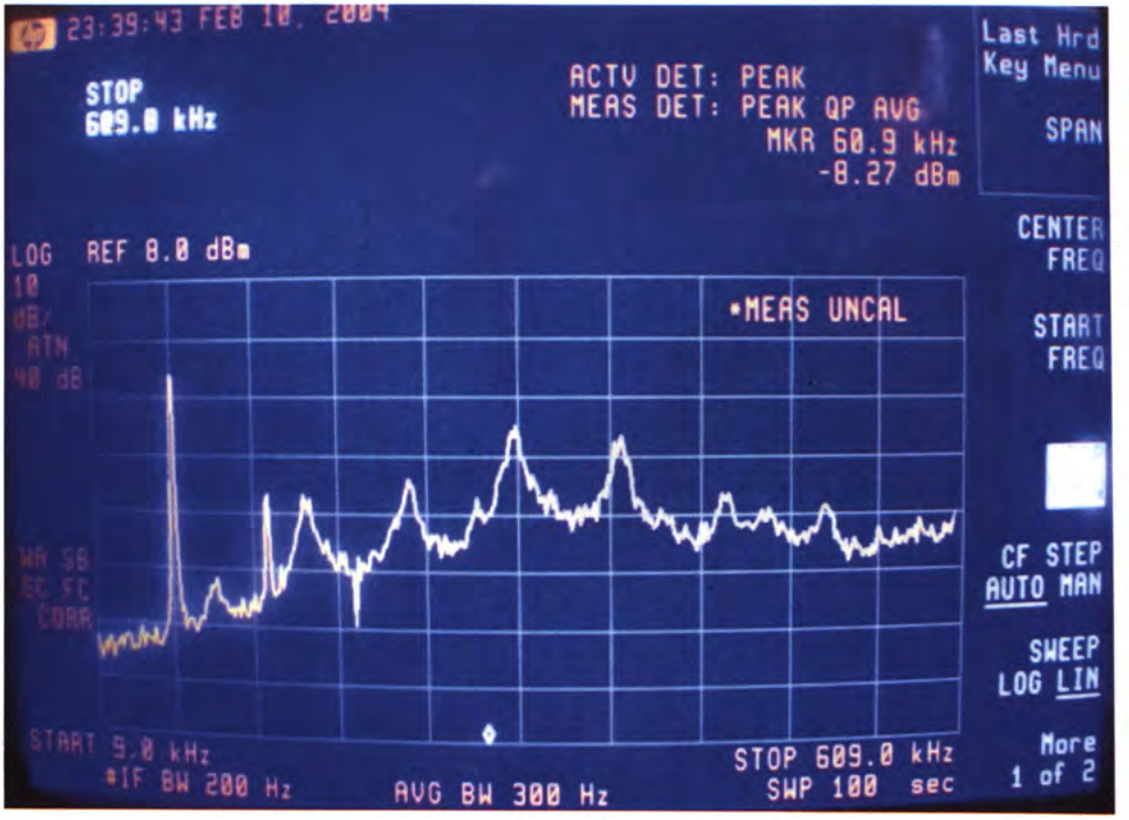


Fig. 5.4 Output Spectrum of Single Channel of Complex Modulator

The diagram shows that a strong signal exists at frequency 60.9kHz, but the frequency of baseband input signal should be 50kHz after the input IF signal being downconverted. This mismatch is resulted from the unstable reference clock, whose frequency varies within a small range over time. The low frequency noise floor is about 45dB below the desired signal observing from the diagram. The noise shaping property of sigma delta modulator is also reflected from the spectrum (if x axis is log scaled, the noise shaping curve is more obvious).

To process the output data using Matlab, logic analyzer is used to sample the output and transfer to a computer. This time IF input frequency is 10.01MHz, other source signals are the same as those in the last measurement. The spectrum of the output of one sigma delta modulator (I path/Q path) is shown in Fig. 5.5, 65536 output data is processed.

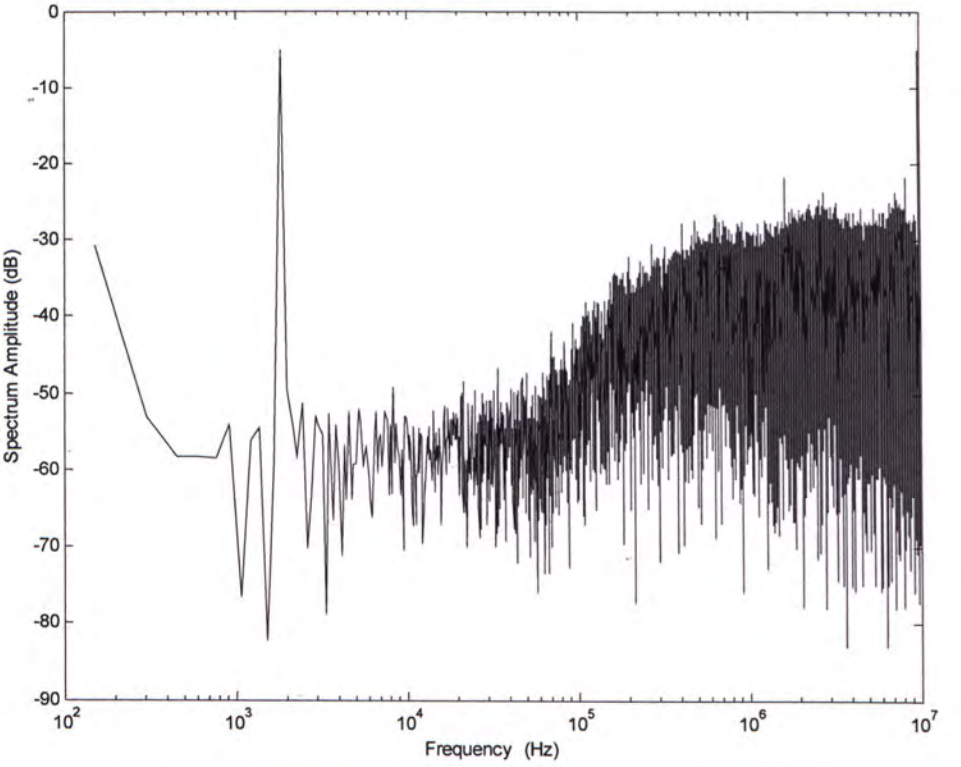


Fig. 5.5 Output Spectrum by Processing Captured Digital Output

A strong DC signal is observed from the spectrum, desired baseband frequency deviates to around 2kHz for the same reason mentioned above. If 100kHz bandwidth is assumed as for the application of GSM receiver, the SNR is only about 15dB. As for the image rejection, output of I path is 90 degree phase shifted and then added with output of Q path. Its spectrum is obtained as shown in Fig. 5.6.

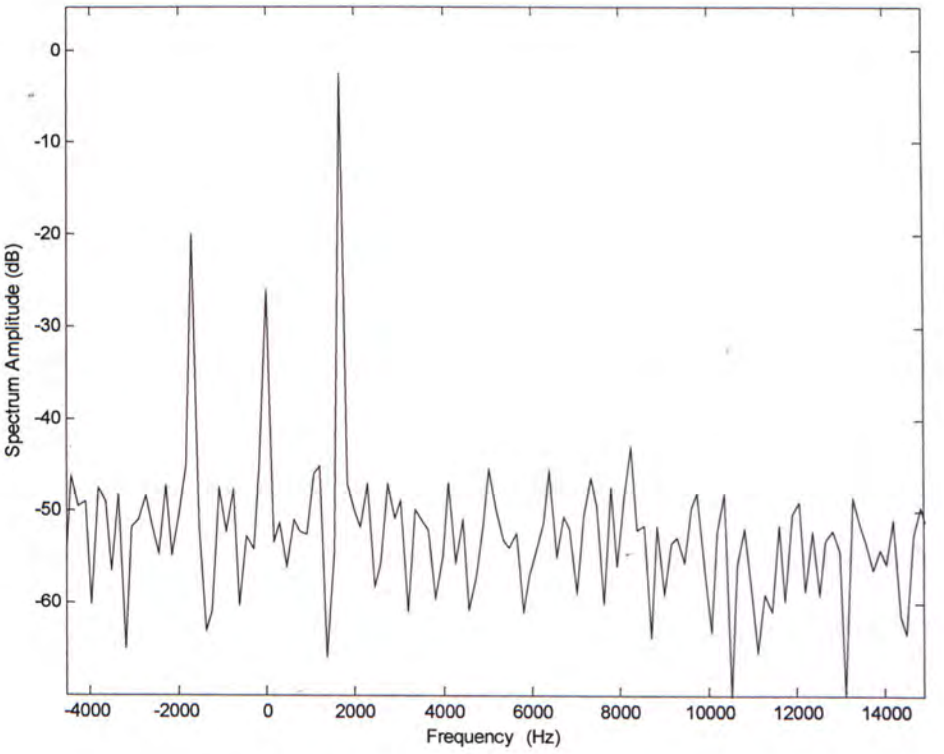


Fig. 5.6 Measurement Result of Image Rejection

The image rejection ratio in this case is about 18dB, noise floor is flat over the frequency range shown in the figure.

The chip under test is functionally workable with power supply as low as 2.6V, which is around 20 percent lower than prescribed 3.3V. Below the critical voltage 2.6V, the desired output signal is quickly inundated by the noise and eventually DFF output sticks to logic 1 or 0.

5.5. Discussion of the Chip Performance

The above measurement results show that the designed IF input complex continuous time baseband sigma delta modulator doesn't work properly. The performance is poor. High image rejection as targeted in this work cannot be consolidated by measurement result. This is mainly due to the oscillation occurred in the biasing

circuits. Other possible reasons include, the process parameter provided by the foundry AMS changes immediately after we submitted this design. When the design is simulated based on the new process parameters, some building blocks do not perform well and the performance of the whole system degrades. Besides, the performance of the whole design wasn't validated through extensive simulation, like corner analysis of whole system, Monte Carlo simulation, etc, which would cost extremely long simulation time. The designed PCB could also introduce substantial noise, but as it is carefully designed with full consideration of supply noise, symmetry, parasitics, etc, it shouldn't be the dominant noise source. The first and somewhat self made PCB has very similar measurement result compared with that of the second, professionally fabricated PCB. The power supply can vary much without considerably affect the output partially indicates that sigma delta modulator is quite immune to various nonidealities.

In short, the unstable biasing circuits are certainly the main contributor to the poor performance. Detailed analysis of the biasing circuit will be given here. Fig. 5.7 shows the adopted biasing circuit again for easy reference.

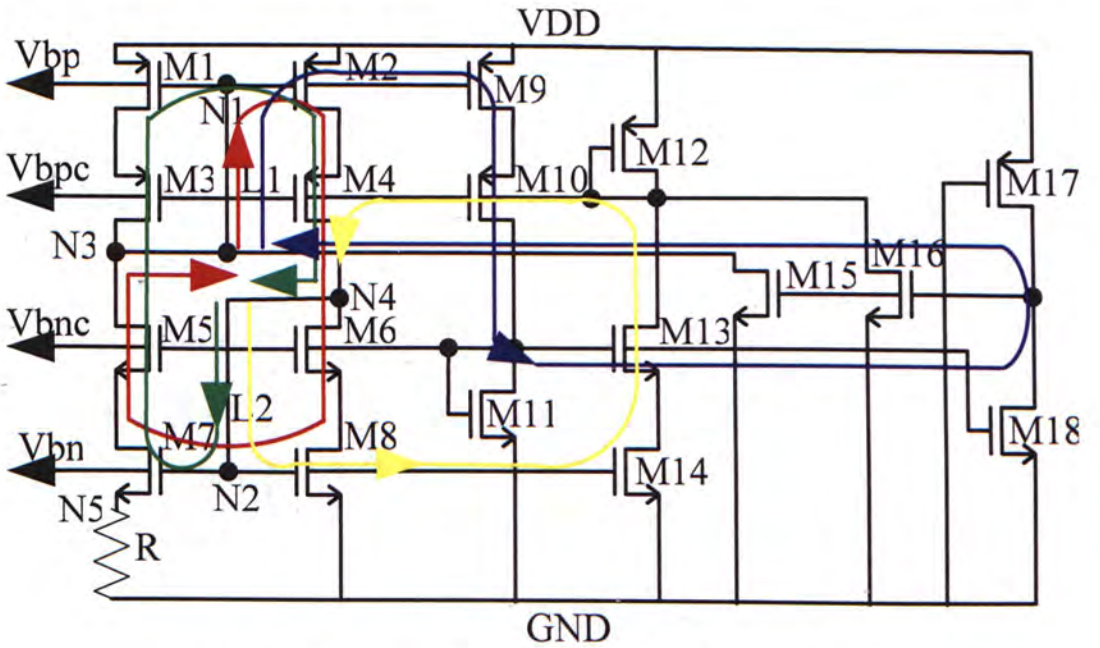


Fig. 5.7 Biasing Circuit with Denoted Internal Loops

The resistor R is external, oscillating waveform is found at node N5 in measurement. This doesn't match with simulation result, where only static currents flow through each branch except for the start up circuitry. Further study finds that in real situation, N5 is at least loaded with a parasitic capacitor mainly from the pad connected to it, furthermore, the subsequent copper wire and resistor could contribute more parasitic capacitance. The pad used in this design has a parasitic capacitance 1.3pF, a 10pF capacitor is added at node N5 to model the real situation. Transient simulation of the biasing circuit of first stage OTA (W/Ls are different for each biasing circuit in this work) is conducted. Node N5 produces a stable DC voltage, whose value is 101.8mV. It seems that the parasitic capacitor will not affect the biasing circuit where no AC source exists. But in reality, noise coupling from substrate or parasitic capacitors can never be avoided, what's worse, the power supply inevitably experiences a startup process, when abundant ac signals rise up. So the performance of ac response for various internal loops should also be taken care of.

First let's see what happens if we replace the ideal power supply VDD with a ramp signal, whose initial and final value is 0 and VDD respectively, rising time is set to 1ps. The transient simulation result at node N5 is given in Fig. 5.8.

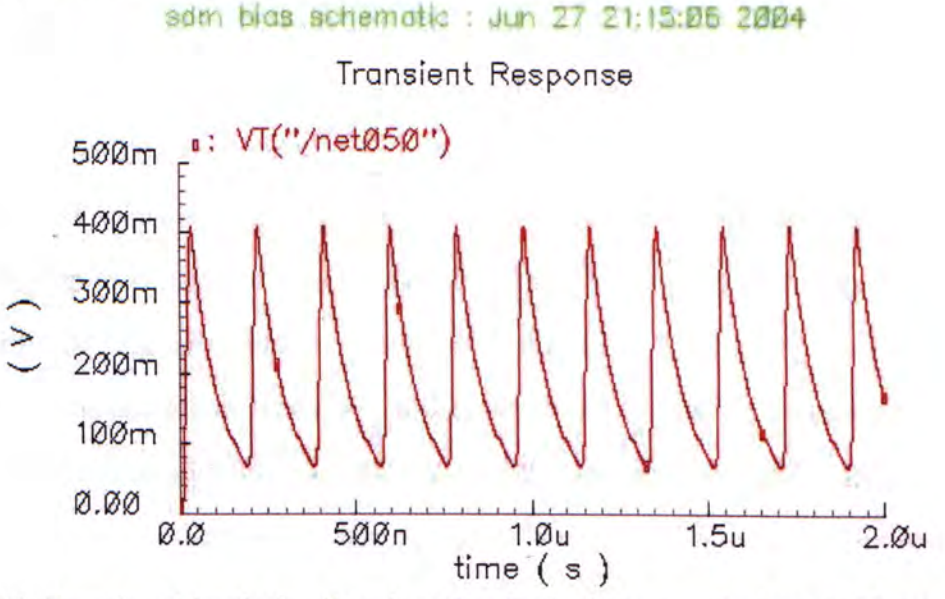


Fig. 5.8 Transient Simulation Result at One End of Biasing Resistor (with parasitic capacitor)

Apparently, the biasing circuit oscillates at a frequency about 5.5MHz. This matches quite well with the oscillation frequency observed in measurement, their amplitudes are also approximately the same. If we take away the loading capacitor at node N5, the corresponding transient response becomes stable, which is shown in Fig. 5.9.

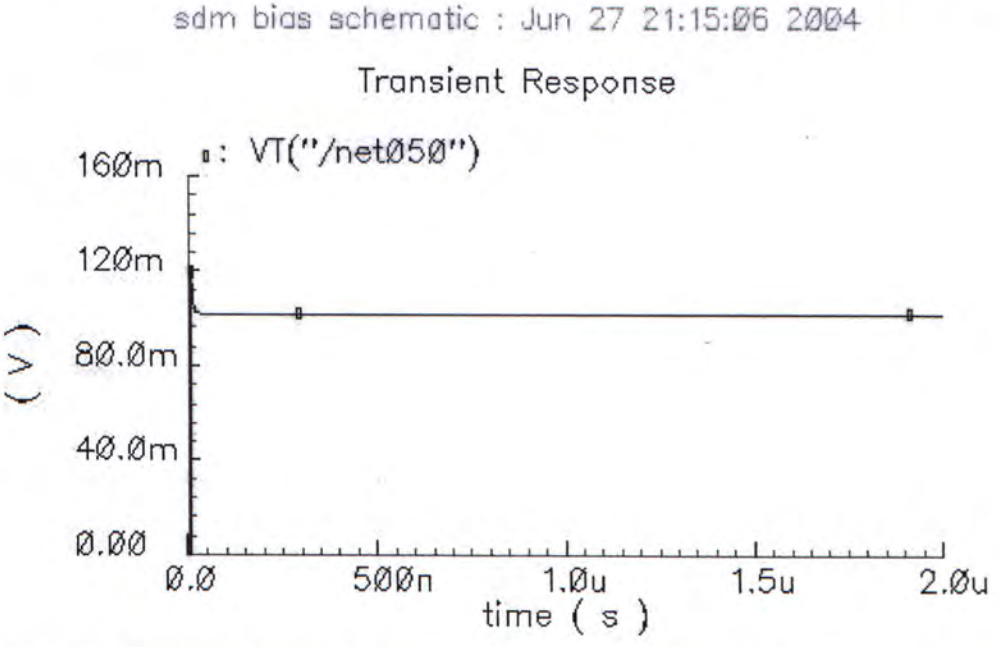


Fig. 5.9 Transient Simulation Result at One End of Biasing Resistor (without parasitic capacitor)

Next, the AC response of the circuit is conducted. This biasing circuit has many closed loops, the colored lines denote the main loops in the circuit. In fact, the loops described by red line and blue line can share the same terminals, start at N1 and end at N3. This is also true for yellow line and green line loops, where N2 and N4 can be start and end points respectively. Green and yellow loops are dealt with first. The line L2 is broken to simulate the AC response of these two open loops (can be taken as one loop). AC signal is applied to node N2 with a DC biasing previously obtained under normal operation. Node N4 is the output and a loading capacitor of 280fF (extracted from simulation) is added to model the parasitic loading cap from M7, M8 and M14 that are otherwise present at node N4 in closed loop form. The results of AC responses without and with 10pF loading cap at N5 are shown in Fig. 5.10.

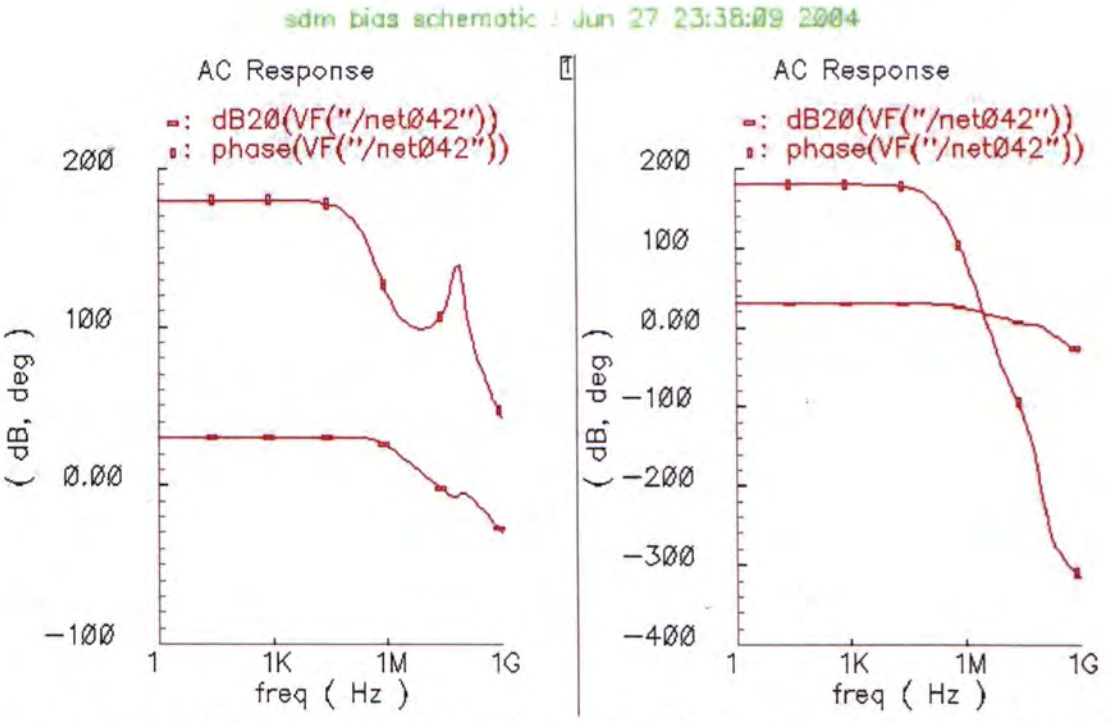


Fig. 5.10 AC Response Simulation Result of the Biasing Circuit Without and With Parasitic Capacitor

As depicted in the diagram, in the case that 10pF loading cap exists at N5 as in real situation, the phase margin becomes zero at around 5MHz, while the gain is still far above unity gain (17dB). Positive feedback is thus formed and any noise at such frequency would result in oscillation. On the other hand, the case that no loading cap is added shows good phase margin (around 90 degree) at unit gain. The same analysis procedure is applied to red and blue loops, the results are similar.

Since we can't eliminate the loading at node N5, how can we make the biasing circuit stable? A quite straightforward way is to decrease the loop gain to a value below 0dB before the phase margin approaches zero. This can be achieved by imposing a capacitor at node N2, which effectively loads the output at node N4. Consequently, the loop gain drops much earlier (due to large output impedance at N4, the dominant pole lies here). Fig. 5.11 shows the simulation result with a 4pF loading added at N2 compared with the original one as shown in the last figure.

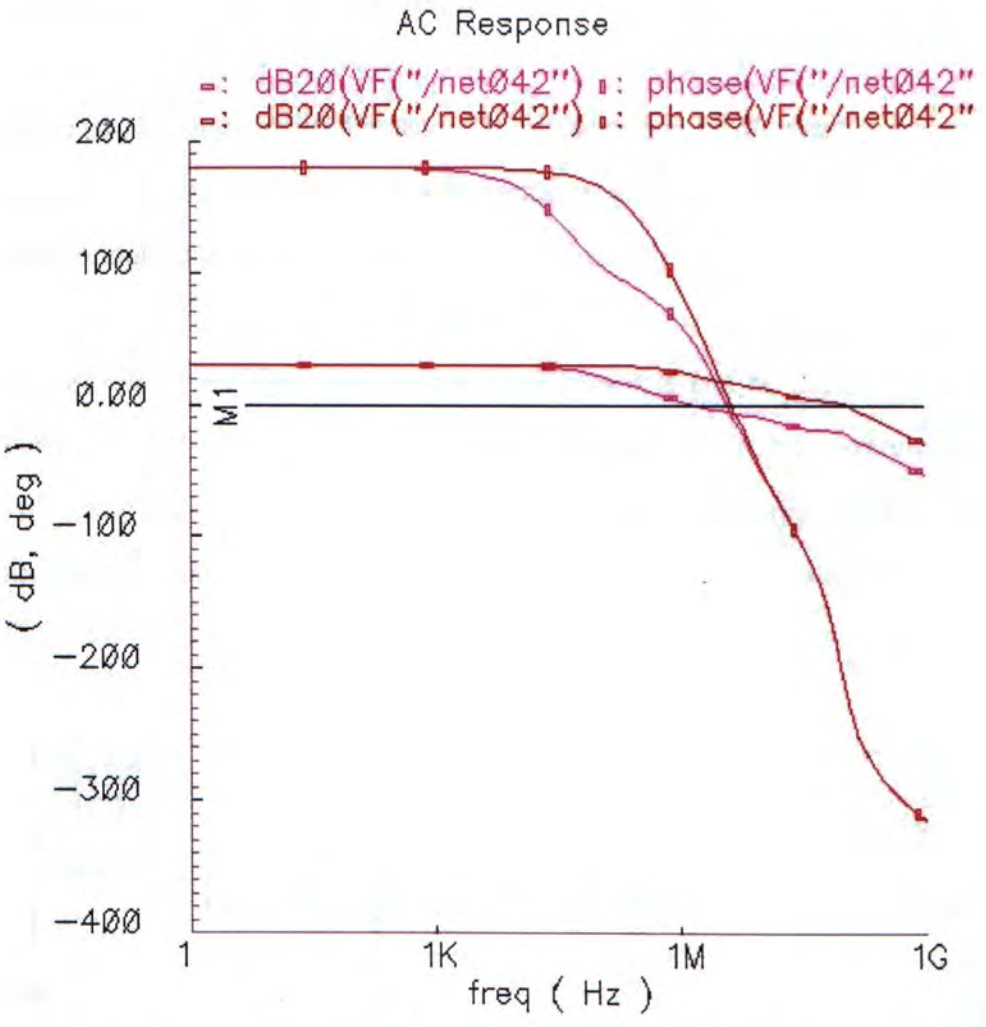


Fig. 5.11 AC Simulation Result with Compensation Capacitor and without

The purple one now has less than unit gain at zero phase margin, or, from the more common perspective, its phase margin is 48 degree in this case. The red one is unstable as described above.

Similarly, the additional compensation capacitor can also be added at node N1, the effect is the same, which is also validated by simulation. If we design the biasing circuits with lower g_m of M1/M2 and M7/M8 or lower output impedance at N3/N4, the compensation capacitor would be unnecessary.

For this kind biasing circuit to operate properly, the start up circuitry should also be carefully designed, W/L ratio of M17 in this circuit should be kept small enough,

otherwise M15/M16 cannot be completely turned off after starting up.

Other two biasing circuits for second/third stages and feedforward transconductances are also analyzed. The former also oscillates after modeling the real situation, the latter remains stable due to its lower loop gain.

In conclusion, we find that though some remedies can be applied to stabilize the biasing circuits, the several intrinsic loops make it difficult to freely adjust biasing voltages while keeping all the loops have enough phase margins. In practice, a much more robust and simpler biasing circuit [36] should be preferable, which is shown in Fig. 5.12.

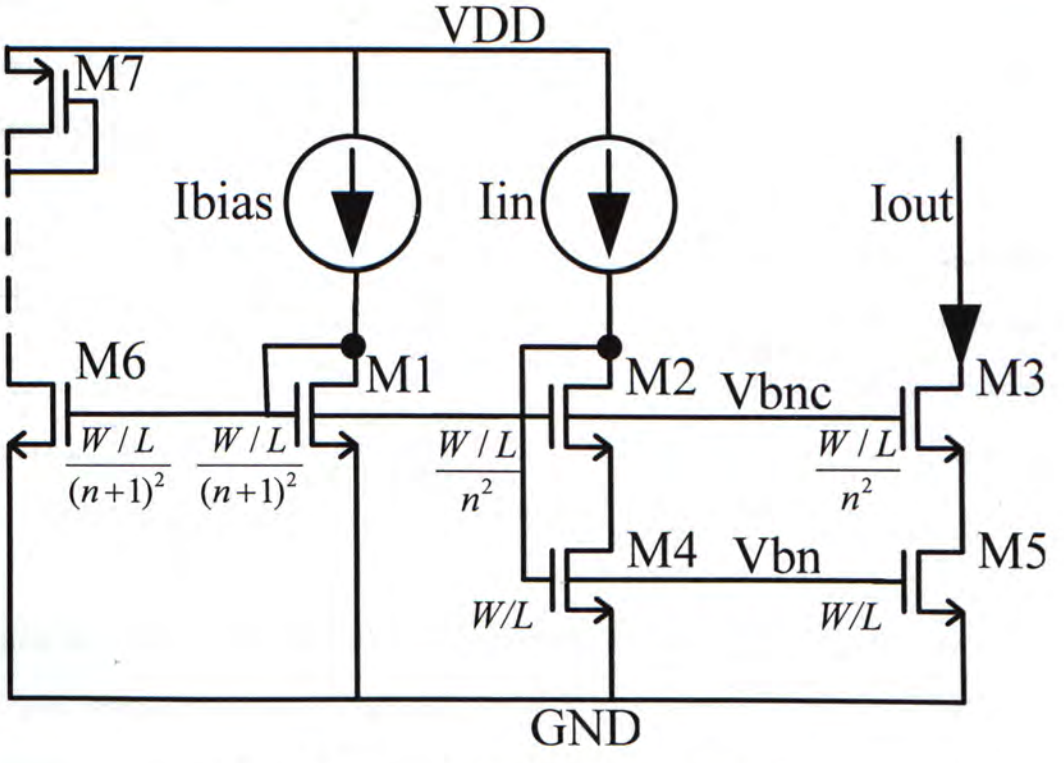


Fig. 5.12 Stable Wide Swing Biasing Circuit

The reference current I_{bias} can be set using an external resistor. By adopting the relationship of W/Ls shown in the diagram, if we assume equal currents in each branch, it can be easily derived that the output voltage (V_{d3}) can be as small as $(n+1)V_{od}$, where V_{od} is the overdrive voltage. Wide output swing can be achieved if

we choose n to be equal to 1. M2 is used here to lower the drain source voltage of M4, thus current flowing through M4 and M5 can match better.

Usually there are quite a few opamps in a design that need biasing. At the layout level, they may distribute everywhere in the whole layout. For opamps close to the current reference branch (in this case, it is comprised of I_{bias} and M1), direct current mirrors (I_{in}, M2, M4 here) near reference branch as well as opamps can be drawn. While for biasing remote opamps, we can't mirror the reference current directly, say, if M1 and M2 in this figure are far away from each other, their matching would be poor due to various gradient effects in a wafer. To circumvent this drawback, the branch composed of M6 and M7 can be adopted, where M6 is close to M1, while M7 is adjacent to the remote opamp, in this way, the reference current can be faithfully copied. One or two diode connected transistors can be cascaded on top of M6 to force its drain voltage to be similar with that of M1.

This sort of biasing circuit presented above is more straightforward and no internal loop exist, accurate biasing can be achieved with good matching between corresponding transistors. None the less, we should be cautious that all the transistors in biasing circuit are operating in saturation region and the output swing is as large as possible provided that matching is guaranteed.

Since the chip do not perform properly mainly due to incautiously designed biasing circuit, new continuous time second order sigma delta modulator with the above biasing circuits is designed and brief simulation results are given in next section. Improvements are made in terms of robustness and wide output swing of building OTA.

5.6. Design of Robust Sigma Delta Modulator

The sigma delta modulator thus far designed uses feedforward compensation for some of its desired feature as described before. The second and third stages adopt G_m_C integrators for its high speed and low power consumption. As a result, several different OTAs and transconductances are required for three main stages and feedforward paths, though an adder is avoided by using V-I converters to implement feedforward coefficients, current comparator is therefore dictated, which increases the loop delay compared with normal voltage comparator. With so many different analog building blocks and mixed voltage current signals, the whole sigma delta modulator is somewhat not robust for manufacturing. Each building block could induce some error due to process variation, etc, and the resulting effects due to the errors of different building blocks are independent with one another, thus the system transfer function could alter much and overall performance degrades considerably. In light of this, simpler and more reliable second order continuous time sigma delta modulator is designed here for testing, RC integrators are employed for all the stages due to their high linearities. Distributed feedback compensation is adopted, which only entails simple DACs and feedback resistors. The simplified diagram is shown in Fig. 5.13.

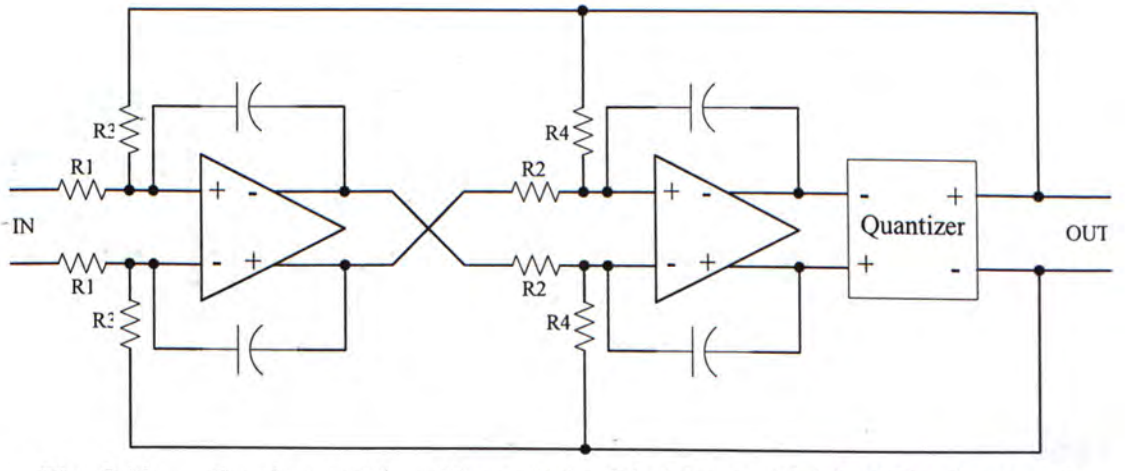


Fig. 5.13 Continuous Time Sigma Delta Modulator with Multi-Feedback and Cascading RC Integrator

The RC constants determine the transfer function of the modulator, near optimal values can be obtained through high level modeling and simulation as well as obeying certain rule of thumb. It is apparent that sigma delta modulator with this kind of structure is much more concise, furthermore, this architecture is also quite tolerant of variations of RC constants [38]. Thus it is suitable for robust design. The only critical building block here is OTA, which is important part of integrators. For robust manufacturing, we should design an OTA not only with sufficient gain, GBW, phase margin, etc, but also stable performance under various extreme situations, i.e., it should pass all corner analysis simulation.

A new fully differential folded cascode OTA is designed toward the objective stated above. Final corner analysis finds that the designed OTA is fairly robust in terms of DC gain, GBW, etc. But the linearity of large transient output signal degrades substantially at corner conditions. Fig. 5.14 compares transient outputs for a small sinusoidal input under normal and extreme simulation conditions.

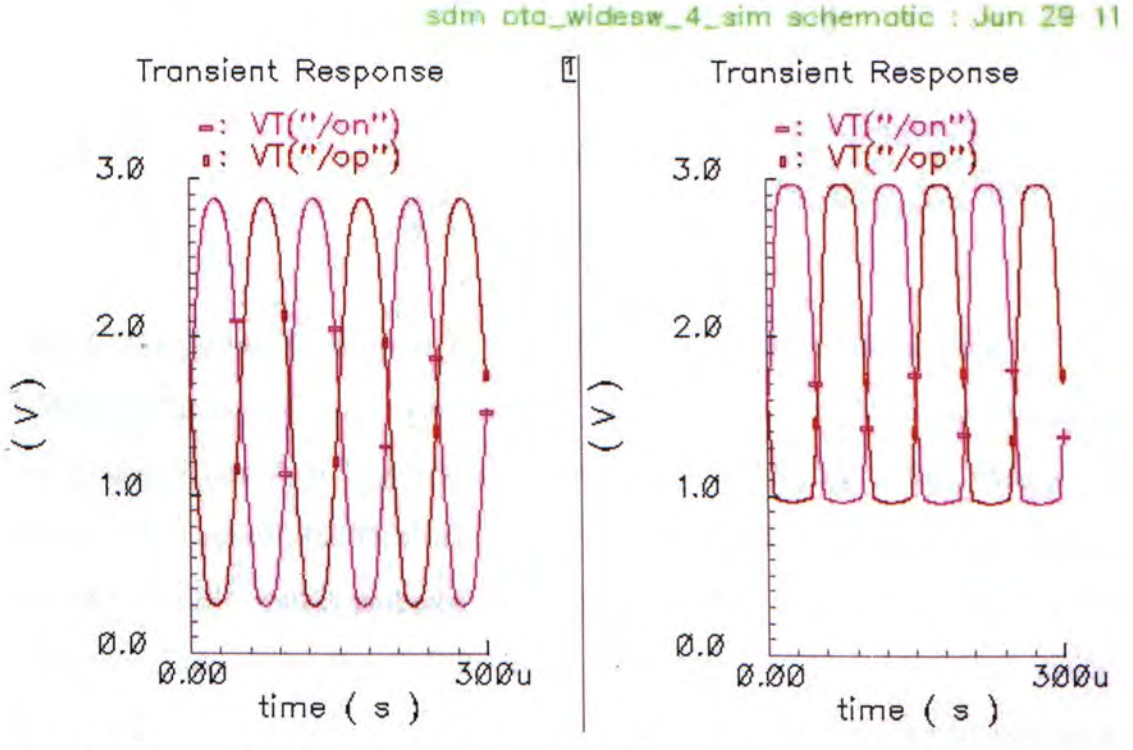


Fig. 5.14 Transient Simulation Result of OTA Under Normal and Extreme Simulation Conditions

By observation, the carefully tuned OTA has good linearity for output swing as large as 300m~2.9V under standard simulation condition. But for a selected corner analysis, the output lower bound is limited to around 1V as shown above. Other corner analysis show similar clipping at lower or upper side. This phenomenon occurred because of the common mode feedback circuitry, which is shown in Fig. 5.15. Brief explanation will be given here.

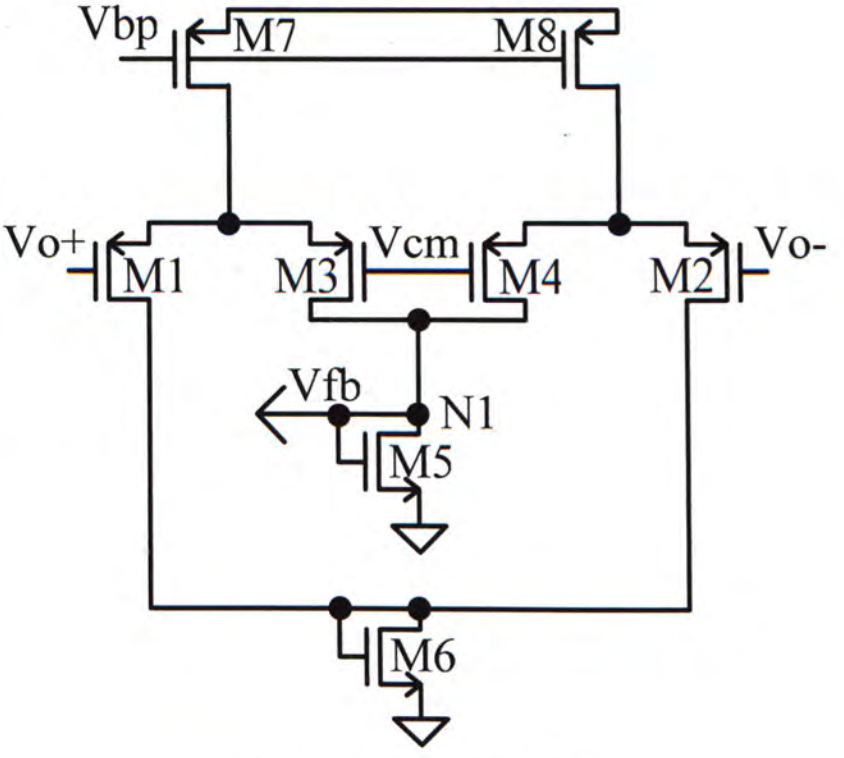


Fig. 5.15 CMFB Circuit

This CMFB is widely adopted in fully differential opamps. Introduction to this CMFB has been given in previous chapter. It seems that the CMFB circuit cannot work when V_{o+} or V_{o-} is large enough to turn off M1 or M2. But in fact, even when M1 or M2 is cut off, the feedback voltage V_{fb} could still be set correctly provided that the CMFB circuit is properly tuned, thus the output swing can circumvent the limitation imposed by the CMFB circuit. Unfortunately, the wide output swing achieved by fine tuning is very fragile, any process variation could easily corrupt it just as the corner analysis result shown in Fig. 5.14. Let's explain this by

qualitatively analyze this circuit.

For symmetry, M1-M4 have the same W/L, current flowing through M7/M8 is identical or at least close to that of M5/M6. Suppose the OTA has a near ideal common mode output voltage, which is very close to V_{cm} (Properly designed CMFB can easily achieve this). As long as the output ac signal of the OTA is small, the CMFB circuit can work properly. When V_{o+} (since the circuit is symmetry, V_{o+}/V_{o-} have same effect) is large enough to turn off M1, all the current from M7 flows into M5, but now Id7' maybe smaller than Id7 as initially designed, because drain voltage of M3/M7 is pushed up for M3 to sink all the current from M7. If now the current flowing through M5 is not large enough to provide a sufficient V_{fb}, M5 will try to draw a little current from M8 to compensate for it. This means the drain voltage of M4 should be at least one V_{th} larger than V_{cm}, otherwise the current cannot flow though M4. As a result, V_{o-} is clipped at a rather high voltage to sink the remaining current from M8, V_{o-} cannot be lower because V_{d4} cannot be pulled down for proper feedback control. If, in another case, M7 provides too much current for M5 if M1 is turned off, the whole OTA cannot operate correctly. Thus in contrast, M1 will not be turned off in order to sink the excessive current from M7. Now the output becomes clipped at upper side. The lower side V_{o-} can be very small since now V_{d4} can be pulled down, M5 need no more current form M8. In summary, we see that the source current of M7/M8 should be exactly the same as the current needed by M5 after M1/M2 is turned off in order to achieve wide output swing. But this is not practical due to process variation and mismatches.

In order to make the OTA have a robust large output swing, the CMFB circuit is studied further. As analyzed above, the main problem is that M7/M8 either provides too much or too little current for M5 after M1 or M2 is turned off. This makes us come up with an idea that a capacitor in parallel with M5 should be helpful, which absorbs abundant current through charging it up or compensates for the current I_{d5} by discharging. Simulation results also confirm this idea. After adding a 1uF capacitor

in parallel with M5, transient simulation is done again under various corner conditions, Fig. 5.16 shows the results.

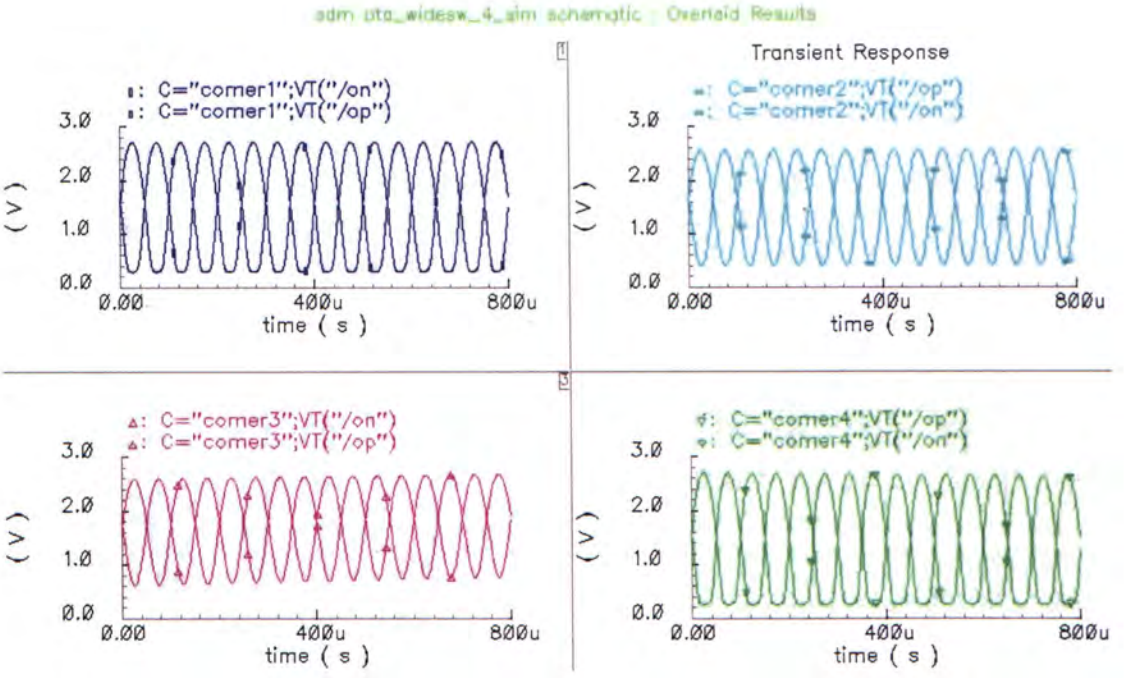
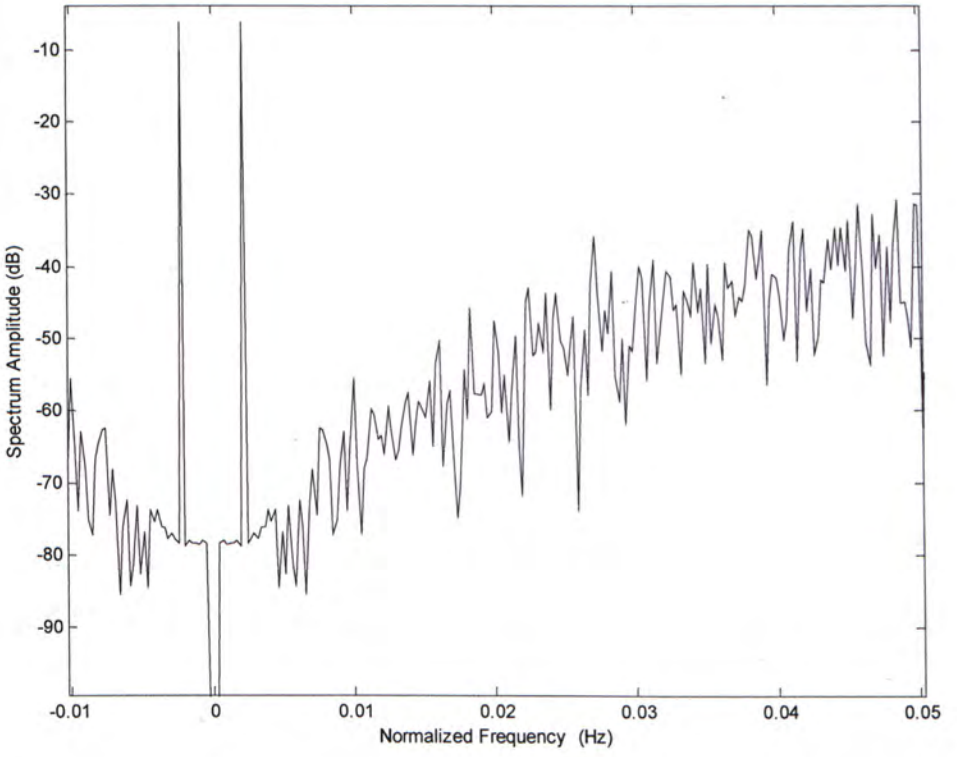


Fig. 5.16 Transient Simulation Results Under four Corner Analysis with Compensating Capacitor in CMFB circuit

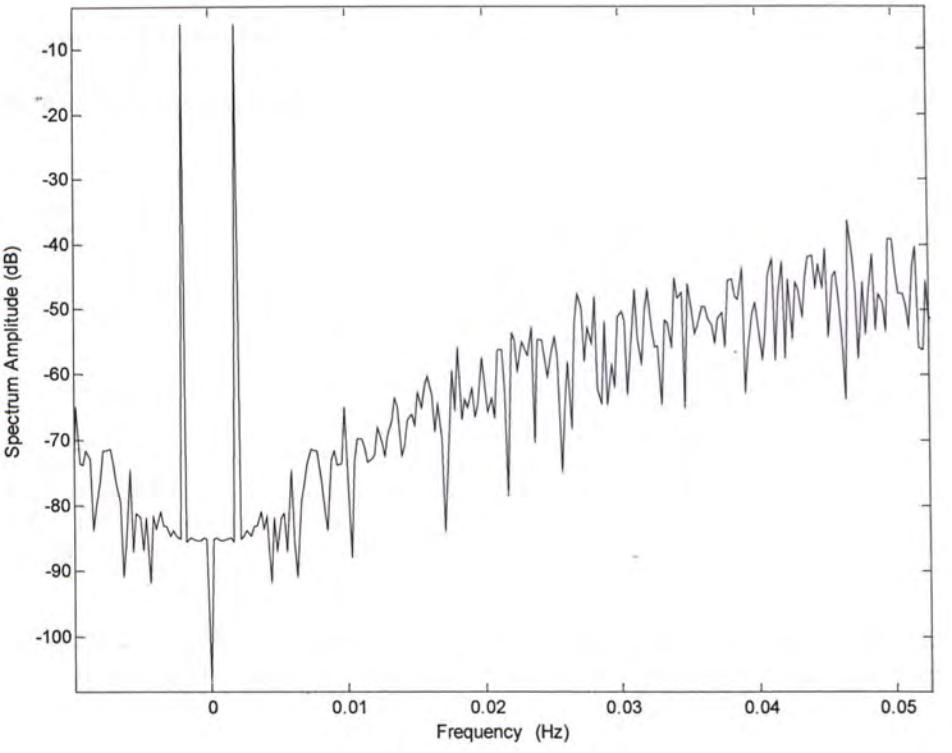
It's apparent that severe clipping disappears for all the four corner analysis. But the drawback is also obvious, the parallel capacitor should be very large otherwise the charging and discharging time would be very short. If the input frequency is relatively low, a small bypass capacitor in parallel with M5 can't sustain long enough to draw or provide current. In other word, the lower input frequency, the larger the capacitor should be to eliminate the clipping problem, so only external capacitor is feasible for this idea. None the less, for critical OTAs in a system, external compact capacitors like surface mount capacitors isn't a big cost compared with the benefit of robust wide output swing. In addition, the extra capacitor has little effect on other performances of OTA, it can simply be treated as a filtering capacitor that stabilizes the CMFB voltage which is initially presumed to be constant.

After designing the OTA with robust performance, a second order sigma delta modulator with the architecture shown in Fig. 5.13 is built up, biasing circuit of OTA

adopts the reliable structure shown in Fig. 5.12. Corner analysis simulation is conducted for both modulators with parallel cap and without of building OTAs. Fig. 5.17 shows the two output spectrums with 4096 points. The input and sampling frequency are 10kHz and 5.12MHz respectively.



(a)



(b)

Fig. 5.17 Output Spectrum of Second Order SDM without (a) or with (b) Compensating capacitors

The calculated SNR for the modulator adopting parallel capacitors in OTAs is 67dB, why the one without capacitor has 60dB SNR. 7dB improvement is achieved in this case. Generally, this approach is more effective to sigma delta modulators with larger internal signal swings, where distortion could easily occur.

Though the above method can help us to achieve robust performance and pass all corner analysis, it is at the cost of some external capacitors. How can we avoid the output swing limitation imposed by the CMFB circuit without using extra component? Another nice way to solve this problem is presented for this special sigma delta modulator employing RC integrators. For general fully differential OTA, its CMFB circuit is controlled by OTA's differential outputs, when the output is large, clipping could easily happen as analyzed before. If we can keep the voltages imposed on CMFB circuit swing in a small range, the CMFB circuit can always operate properly.

In this particular case with cascading RC integrators in a modulator, we can split the input resistors of the second stage and make use of the fractional output voltages to control the CMFB circuit, the idea is illustrated in Fig. 5.18.

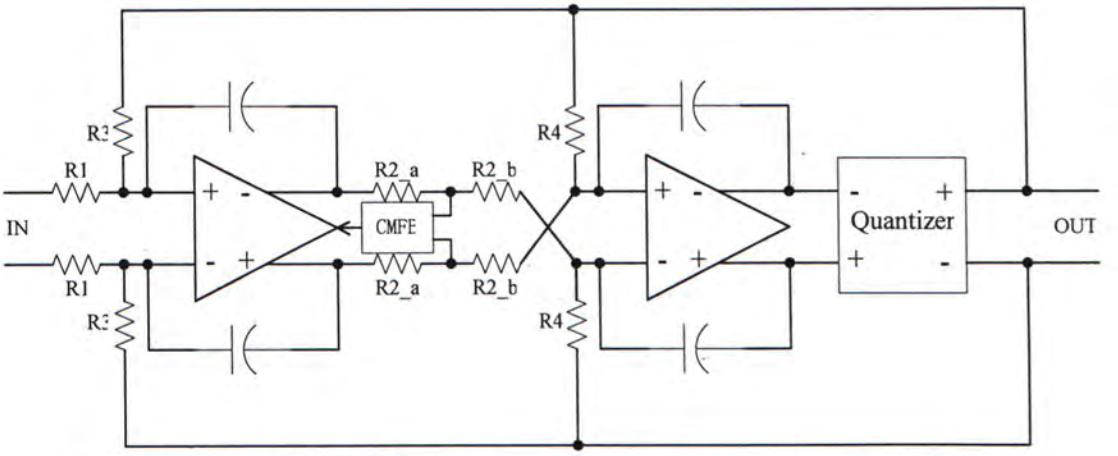


Fig. 5.18 CT SDM with Proposed Resistor Splitting Scheme for CMFB

The input resistor R2 of second stage is split into two parts, since R2 connects to the input of second OTA, which is virtual ac ground but its common mode voltage is presumably the same as the output common mode voltage of first stage, the AC voltage in between R2_a and R2_b is linearly scaled down but common mode is hardly affected. Thus the CMFB circuit can perform properly without seeing large original differential output of the first stage. The drawback is R2_a and the parasitic input capacitor C_{gs} constitute a low pass filter, but the effect is neglectable since its cut off frequency is far beyond the interested signal band. Again corner analysis is carried out for this idea, the ratio of R2_a over R2_b is set to 2, other simulation settings are the same as the previous one. Fig. 5.19 gives the result.

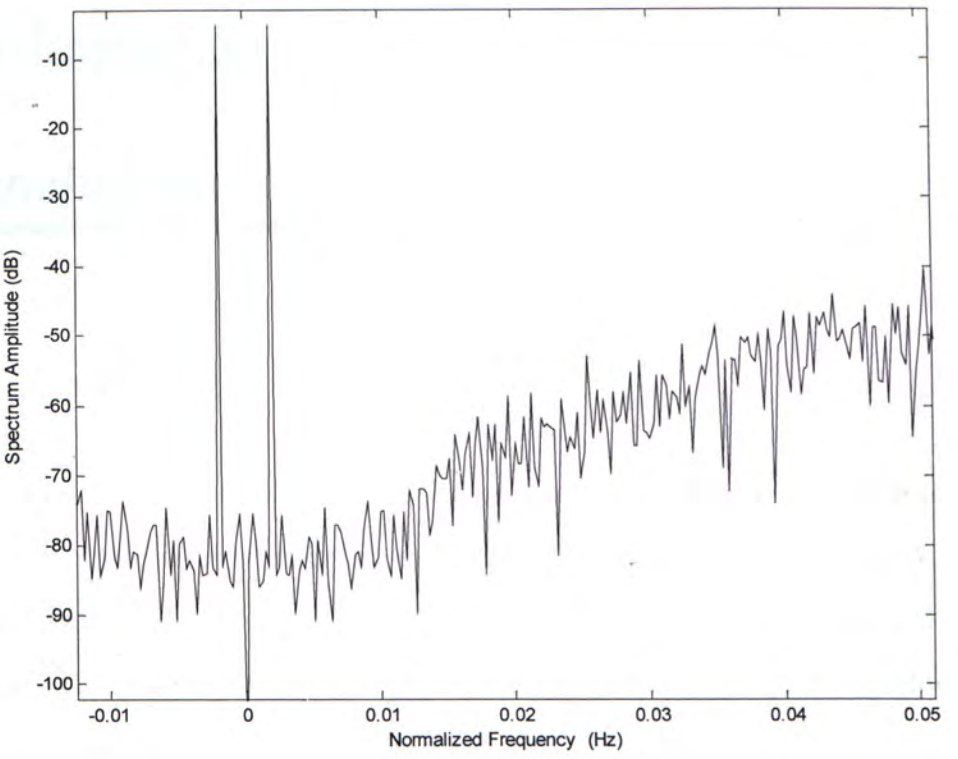


Fig. 5.19 Output Spectrum of Second Order SDM with Resistor Splitting Scheme

The SNR is 65dB, compared with 60dB SNR achieved in conventional implementation as simulated before, 5dB improvement is obtained.

6. Chapter 6

Conclusion

6.1. Conclusion

An intermediate frequency input continuous time baseband complex ΣΔ modulator with integrated mixer is modeled, designed and implemented in this work. Novel resistor time-sharing technique is proposed to solve the matching problem of the input resistors, which act as key components in terms of image rejection performance in the complex modulator. Combining with data-dependent dynamic element matching technique for solving mismatch of feedback resistors, very high IR ratio can be achieved. This improvement greatly relaxes the requirements of channel filter, and also makes future monolithic integration of receiver more realistic. The design parameters are concluded in table 4.

Supply Voltage	3.3V
Signal Bandwidth	200KHz
Intermediate Frequency	25MHz
Input Frequency	25.05MHz
Oversampling Ratio	128
IR Ratio (Layout Level)	69dB
SNDR (Layout Level)	61dB
Power Consumption	14.8mW
Active Chip Area	$1mm^2$
Technology	AMS 0.35um

Table 4. Design Parameters and Performance of this Work

Unfortunately, the fabricated chip cannot work correctly due to oscillating biasing circuits in the design. Nonetheless, the new approach adopted here theoretically improves the matching between I path and Q path significantly, a related design in [2] shows that similar work can achieve over 60dB image rejection even without using the proposed method here. It is reasonable that after solving the remaining dominant mismatch from input resistors, the image rejection can be well improved.

Beside the main contribution of enhancing the image rejection performance of complex modulator in wireless receiver, numerous other ideas are also presented which are related to the design of sigma delta modulator. Firstly, transformation from discrete time prototype of sigma delta modulator to continuous time one usually uses impulse invariant method. In this work a much simpler but effective zero order hold approach is adopted, which also takes into account the effect of input signal in addition to that of the feedback signal. Secondly, the modeling of first stage RC integrator with finite gain and bandwidth OTA is studied extensively, a right model is compared in detail with one often misused model. Thirdly, a new signal scaling method of the sigma delta modulator is presented based on theoretical analysis. The maximum internal signal swing can virtually be controlled to any level without affecting the transfer function of the system. Fourthly, original LO clock generating tree is designed, which have the ability of fine tuning the clock phases, even in sub-pico second range. Fifthly, a straightforward current comparator is designed by adding additional current to voltage conversion stage in front of conventional regenerative voltage comparator. The I-V circuit uses simple diode connected transistor as the loading of previous transconductance, and the cascading current source on top of the diode connected transistor sets the biasing voltage. Sixthly, various internal loops in constant g_m wide swing biasing circuit employed in our design is analyzed and capacitor compensation technique is presented to achieve stable performance. Seventhly, the issue of wide output swing of fully differential OTA is studied and a large capacitor connecting to the CMFB signal is added to make the CMFB circuit operate robustly, i.e., it will not limit the output swing of the

OTA even under extreme simulation condition. Eighthly, in the design of sigma delta modulator where cascading RC integrators are adopted, a nice way to avoid the output swing limitation imposed by CMFB circuit is to split the input resistors of the subsequent stage, and use the obtained fractional output signal to control the CMFB circuit. In this way, input transistors of CMFB circuit will never be turned off but output swing of main OTA is not affected.

6.2. Future Work

Design for manufacturing is a critical issue especially for analog/mixed signal circuit design. Though sigma delta modulator is rather tolerant of analog components' nonidealities, its performance also relies much on the desirable system transfer function, which is sensitive to many obvious and not that obvious design parameters especially those at the input stage. For any future work, robust performance of all the building blocks and whole system should be guaranteed, this means they should pass all the corner analysis and operate well under Monte Carlo analysis.

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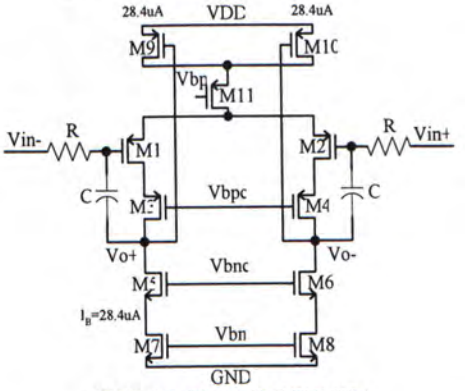
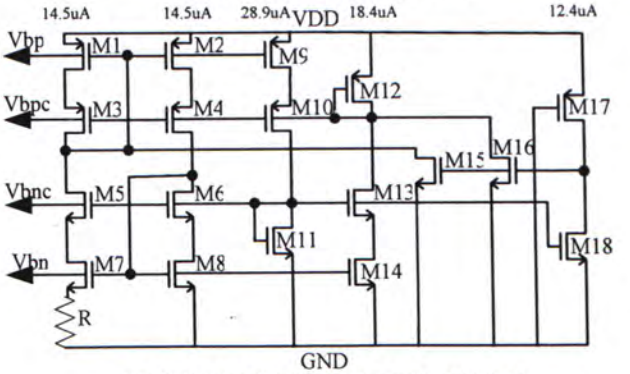
Appendix A Schematics of Building Blocks

First Stage RC Integrator of the Sigma Delta Modulator



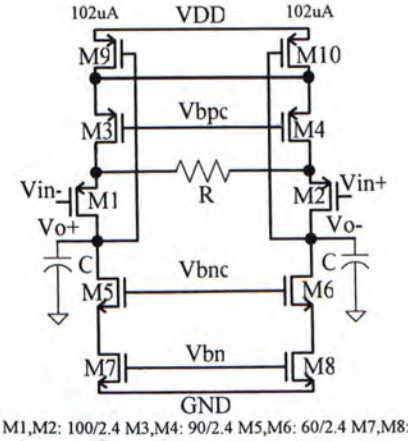
M1,M2: 100/2.4 M3,M4: 70/2.4 M5,M6: 30/2.4
M7,M8:15/2.4 M9,M10: 11/2.4 M11: 300/2.4
R: 40k C: 4p

Biasing Circuit of First Stage OTA



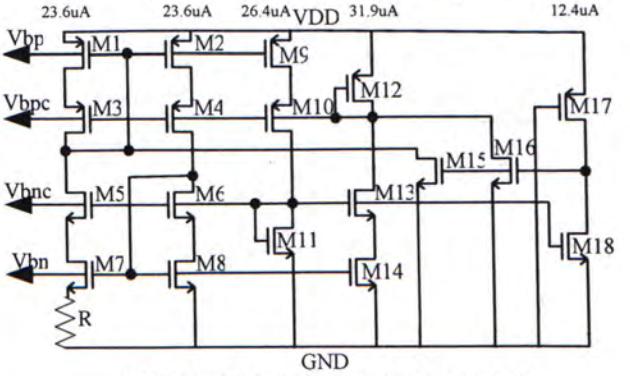
M1,M2: 10/1 M3,M4 15/1.6 M5,M6 3/1.6 M7: 16/1 M8: 4/1
M9: 20/1 M10: 20/1.6 M11: 1.6/1.6 M12: 2/1.6 M13: 5/1.6
M14: 5/1 M15,M16,M18: 10/1 M17: 2/20
Vbn: 765m Vbnc: 1.25 Vbpc: 1.72 Vbp: 2.33 R: 7k

Second and Third Stage OTAs



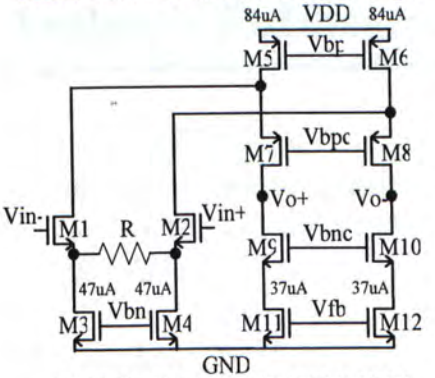
M1,M2: 100/2.4 M3,M4: 90/2.4 M5,M6: 60/2.4 M7,M8:
30/2.4 M9,M10: 15/2.4 R: 18.4k
C(2nd Stage): 3.9p C(3rd Stage): 27.4p

Biasing Circuit of Second and Third Stage OTAs



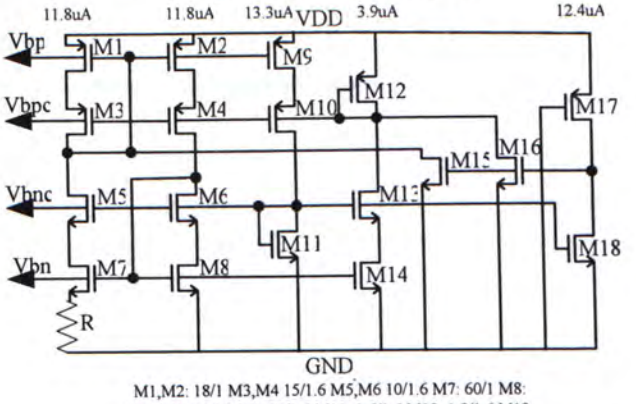
M1,M2: 18/1 M3,M4 15/1.6 M5,M6 3/1.6 M7: 16/1 M8: 4/1
M9: 20/1 M10: 20/1.6 M11: 1.6/1.6 M12: 4/1.6 M13: 5/1.6
M14: 5/1 M15,M16,M18: 10/1 M17: 2/20
Vbn: 860m Vbnc: 1.2 Vbpc: 1.81 Vbp: 2.34 R: 5k

Feedforward V-I Converter for Three Stages



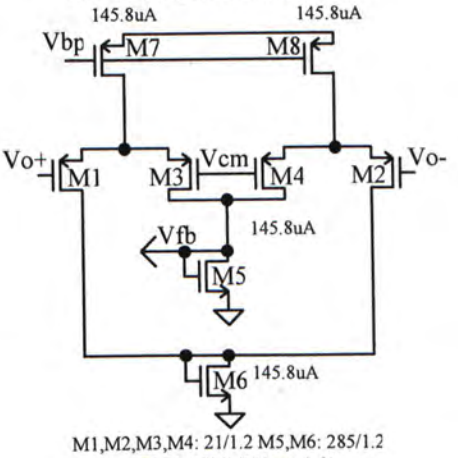
M1,M2: 300/0.35 M3,M4: 100/2.4 M5,M6: 300/2.4
M7,M8: 130/2.4 M9,M10,M11,M12: 60/2.4
R(1st V-I): 20.6k R(2nd V-I): 60k R(3rd V-I): 47.1k

Biasing Circuit of Feedforward V-I



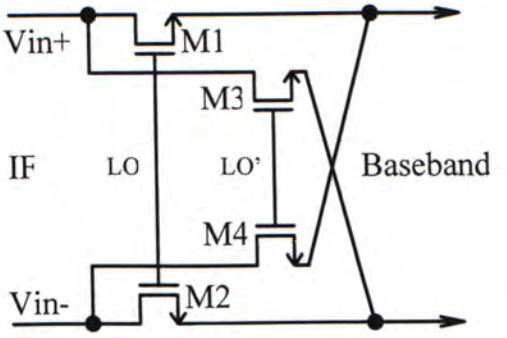
M1,M2: 18/1 M3,M4 15/1.6 M5,M6 10/1.6 M7: 60/1 M8:
15/1 M9: 20/1 M10: 20/1.6 M11: 1.6/1.6 M12: 1.2/1.6 M13
5/1.6 M14: 5/1 M15,M16,M18: 10/1 M17: 2/20
Vbn: 625m Vbnc: 990m Vbpc: 2.05 Vbp: 2.42 R: 5k

CMFB for Feedforward V-I



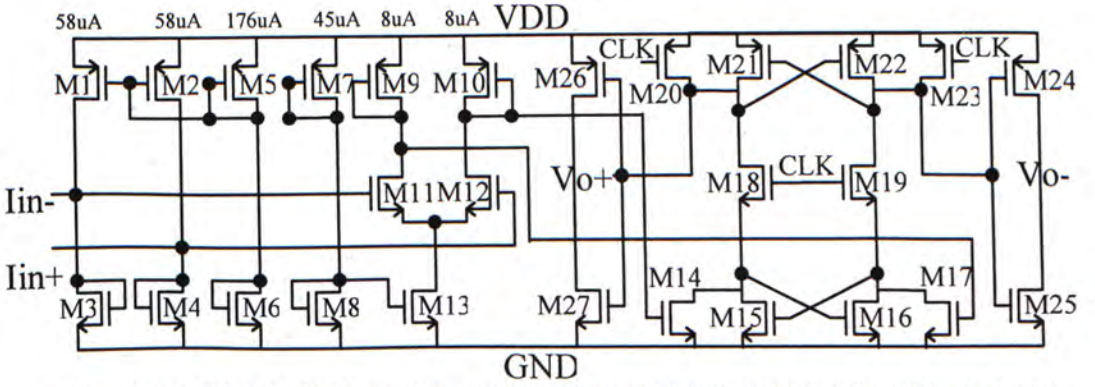
M1,M2,M3,M4: 21/1.2 M5,M6: 285/1.2
M7,M8: 400/1.2 Vcm: 1.65

IF to Baseband Mixer



M1,M2,M3,M4: 3/0.35

Current Input Comparator



M1,M2:6/1.2 M3,M4: 1.2/1.2 M5: 12/0.35 M7: 1.2/1.2 M6,M8: 2/0.35 M9,M10: 0.6/2 M11,M12: 100/0.35 M13: 2/1.2
M14,M15,M16,M17: 3.5/0.35 M18,M19,M21,M22: 8/0.35 M20,M23: 10/0.35 M24,M26: 3.6/0.35 M25,M27: 1.2/0.35

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