Adiabatic Low Power CMOS

A Thesis Submitted

to

The Department of Electronic Engineering

of

The Chinese University of Hong Kong

In

Partial Fulfilment of the Requirements

for the Degree of

Master of Philosophy

by

Kelvin CHEUNG Ka Wai

June 1997

To my parents and Lydia
for their
unconditional love and support

ACKNOWLEDGEMENTS

The author would like to take the opportunity to express the sincere gratitude to my supervisor, Dr. CHAN Cheong Fat, for his encouragement and guidance throughout the research. His professional advice helps me a lot and I believe this knowledge will be helpful to my future.

I would also like to thank all my colleagues in the ASIC/VLSI Laboratory of the Chinese University of Hong Kong, especially the fellow Cadence users, Mr CHENG King Sun, Mr PANG Tin Chak, Mr SIT Wing Yun and Mr TO Chuek Him. Their friendly assistance and discussion helped me to explore the working environment and resolved the problems encountered.

Dr Juraj POVAZANEC has given a lot of valuable advice in the design of the automatic adiabatic clocks generator. I would like to send him a special thank for his suggestion on analogue design.

Finally, I will thank the technical staff of ASIC/VLSI Laboratory, Mr YEUNG Wing Yee. His professional technical supports have created an appropriate working environment.

ABSTRACT

This thesis suggests a new power saving CMOS technology - Adiabatic Quasi-static CMOS (AqsCMOS) logic. AqsCMOS logic makes use of charge recovery technique to achieve a comparatively low power consumption to the CMOS logic. The new technology can be used to drive and be driven by conventional static CMOS logic directly.

As the size of the integrated circuit grows and more devices are fabricated per unit die area with the technology progress, the power dissipation of the integrated circuit becomes a very important concern. The heat produced by the circuit itself can burn the whole integrated circuit. The power dissipation of the conventional static CMOS logic is bounded by the charging and discharging processes of the gate capacitance. In AqsCMOS logic, energy are conserved by selectively charging and discharging the node capacitances to reveal logic levels using harmonic motion of charges. In theory, the power consumption of AqsCMOS logic can be zero.

The basic building block of AqsCMOS logic is an inverter. The AqsCMOS employs "quasi-static logic" to maintain the compatibility of the AqsCMOS logic to the conventional static CMOS logic. Also, the logic levels of the AqsCMOS inverter and CMOS inverter are compatible.

Finally, from the simulation results and the experimental data, the AqsCMOS logic is proved to be feasible. The power dissipation of the AqsCMOS is smaller than the conventional static CMOS logic when the sizes of device are the same. Also, the logic levels of the AqsCMOS are compatible to the static CMOS which can be used to drive the static CMOS devices directly.

TABLE OF CONTENTS

LIST OF FIGURES

LIST OF TABLES

1. INTRODUCTION

1.1 Introduction

In this chapter, the objective of the project will be revealed. The difference between static CMOS, and dynamic CMOS logic and the origin of power dissipation in static and dynamic CMOS integrated circuit will be introduced for the ease to understand the Adiabatic Quasi-static CMOS (Abbreviated as AqsCMOS, pronounced as "æ'kwəz si:məs) technology and its low power property. After a brief description of the Adiabatic CMOS technology, the resources used to complete the research project is listed and the layout of the thesis can be found in the end of this chapter.

1.2 Objective

The objective of the research is to develop a new style of low power CMOS technology, which is compatible to conventional static CMOS logic.

1.3 Static CMOS Logic and Dynamic Logic

In this section, static CMOS logic and dynamic logic will be introduced as the background materials of Adiabatic Quasi-static CMOS logic.

1.3.1 Static CMOS logic circuit

Static CMOS logic gates are constructed using symmetric NMOS and PMOS transistors. Figure 1-1 shows a block diagram view of an general static CMOS logic

gate. The input connect to both the PMOS block (F) as well as the NMOS block ($\overline{F}$). If all the input to the F block is equal to 0, the upper PMOS block conducts and the lower NMOS block is cutoff then the output is a 1 and vice versa for all the inputs to the $\overline{F}$ are equal to ones.

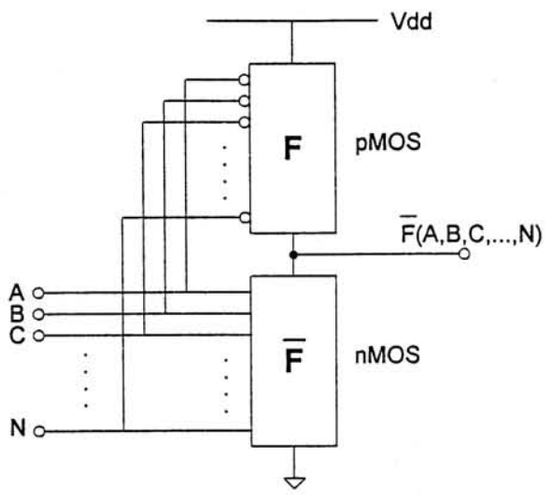


Figure 1-1 General Static CMOS Logic Gate

The static CMOS logic is so far the most commonly used technology for circuit development especially random logic functions.

Clocked static CMOS logic modifies static CMOS logic by inserting a transmission gate between two cascading logic blocks which control the flow of logic levels. When the on and off operations of the transmission gates are controlled by the same clock signal, all the CMOS logic gates will be synchronised.

1.3.2 Dynamic logic

Dynamic logic circuit perform logic operations using the properties of the capacitive charge storage node. In dynamic logic, clock signals of double functions are employed. The first function is providing logic synchronisation. The second function is allowing predefined charge states to be established at a periodic rate. The output is defined only during a portion of the clock cycle, therefore, unlike a

static CMOS discussed in chapter 1.3.1, a dynamic logic gate will only respond to the inputs during a predefined clock cycle.

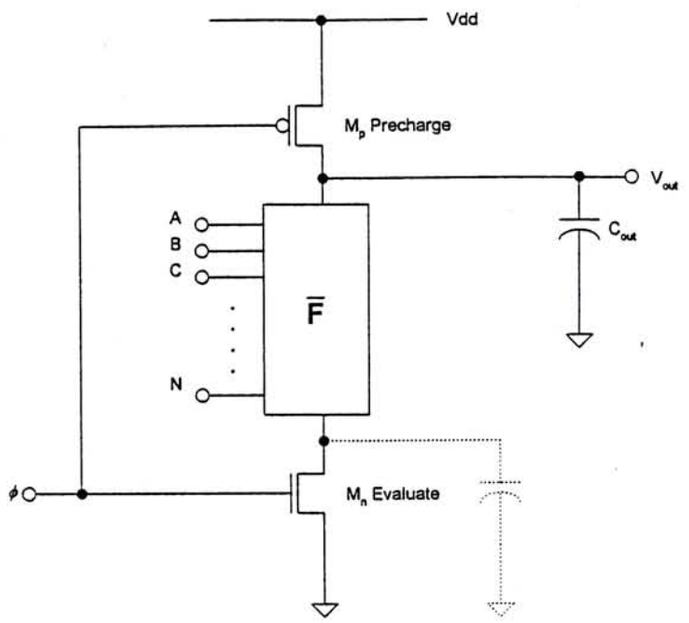


Figure 1-2 General Dynamic Logic Gate

A basic single-clock, two-phase, general dynamic gate is shown in Figure 1-2. In the circuit, the logic is performed by logic block ($\overline{F}$). Transistors M_p and M_n are controlled by the clock ϕ and called precharge and evaluate devices respectively. These two transistors provide dynamic control and synchronisation of the charge.

The operation of the circuit is divided into two phases, the precharge and evaluate phase. When the clock signal is 0, the M_p turns on and the M_n turns off. As a result, the M_p charges up C_{out} to V_{dd} regardless of the inputs. The input signals are accepted at this moment. When the clock switch to 1, the M_p become cutoff and M_n become conducting. If the logic block is also conducting, the C_{out} will be discharge to $V_{out} = V_{ss}$. This is called conditional discharge which is characteristic of dynamic logic.

This logic suffers from unintentional discharge (or unintentional charge up for p-logic) of C_{out} when the gates are cascaded. As discussed before, the input signal

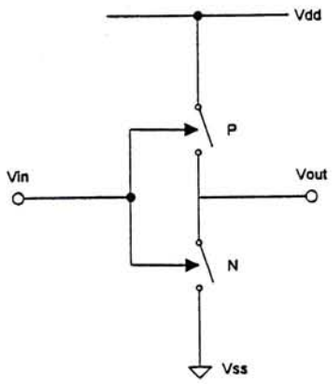


Figure 1-3 CMOS inverter model for static dissipation calculation

must arrive before the evaluate phase starts. Yet the output of the preceding stage cannot pass to the succeeding stage as an input until the evaluate phase start. This contradiction can cause the C_{out} to be discharged incorrectly.

1.4 Power Consumption in Static CMOS Integrated Circuit

There are two main kinds of styles dissipation in CMOS integrated circuit, static dissipation due to the junction leakage current and dynamic dissipation due to the switching transient current and the charging and discharging processes of load capacitances.

1.4.1 Static power dissipation

Consider a CMOS inverter as shown in Figure 1-3 as discussed in chapter 1.3.1, when the input is 0, the NMOS transistor will be turned off and the PMOS transistor will be turned on. The output will be V_{dd} or 1. Similarly, when the input is 1, the NMOS transistor is switched on and the PMOS transistor is switched off. The output will be V_{ss} or 0.

We can find that when one transistor is being switched on, the other must be being switched off. Therefore in an ideal case there will not be any dc current path from the V_{dd} to V_{ss}.

However, there is a small static power dissipation due to reverse bias leakage. In Figure 1-4, we can see the parasitic diode for a CMOS inverter. The source-drain diffusions and the p-well diffusion form parasitic diodes. Also, a parasitic diode is formed between p-well to substrate. Since all of these parasitic diodes are always reverse biased, their leakage current form a current path between V_{dd} and V_{ss} and contribute to the static dissipation.

The reverse biased leakage I_R current is described by the diode equation.

$$I_R = \frac{qAn_i x_d}{2\tau_o} e^{\frac{qV_R}{kT}}, \qquad (1\text{-}1)$$

where

q = electronic charge
A = junction area
n_i = intrinsic concentration of electron
x_d = depletion width
V_R = reverse bias voltage
k = Boltzmann's constant
T = temperature
τ_o = effective carrier lifetime

The static power dissipation per device is the product of the device leakage current and the supply voltage. The total static dissipation P_s should be given by (1-2).

$$P_s = \sum \text{leakage current} \times \text{supply voltage}, \qquad (1\text{-}2)$$

Typical static dissipation due to leakage for an inverter operating at 5V is between 1 to 2nW.

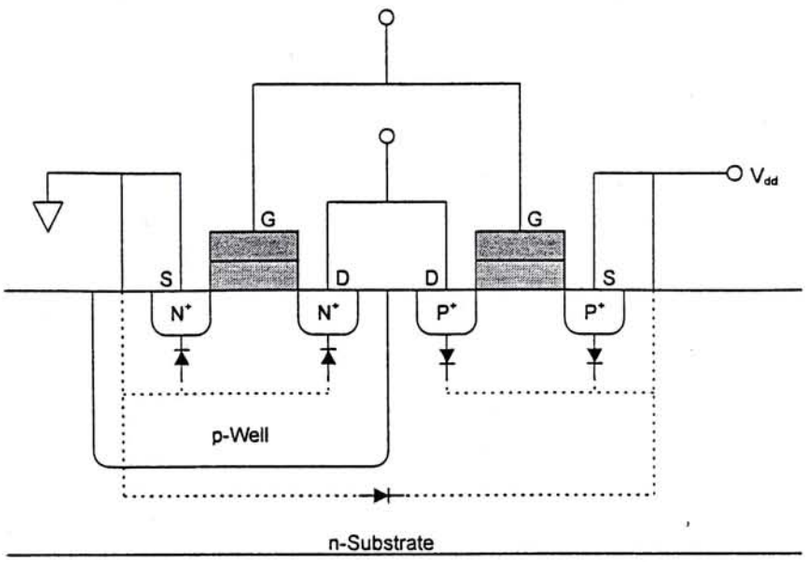


Figure 1-4 Model describing parasitic diodes

1.4.2 Dynamic power dissipation

1.4.2.1 Short circuit current

Referring to chapter 1.4.1, one transistor will be turned off when the other is turned on. If the transistors can be switched from on to off and off to on within zero second as what they should be in the ideal case, there should not be any extra dc current path from V_{dd} to V_{ss}, other than the reverse biased leakage current of the parasitic diodes. However, in reality, the NMOS transistor and the PMOS transistor will be on for a very short period of time during transition because of the non-zero rise and fall time, which will form a short circuit between power supply and ground.

1.4.2.2 Charging and discharging of load capacitances

The main power dissipation of a CMOS circuit is from the charging and discharging of the load capacitances during a transition.

The dynamic power dissipation (charging and discharging load capacitance) can be modelled by assuming the rise and fall time of a square-wave input V_{in} of frequency $f_p = 1/t_p$ is much smaller than its period as

shown in Figure 1-5. The average dynamic power P_d dissipated during switching is given by (1-3).

$$P_d = \frac{1}{t_p}\int_0^{t_p/2} i_n(t)V_o dt + \frac{1}{t_p}\int_{t_p/2}^{t_p} i_p(t)(V_{dd} - V_o)dt, \qquad \textbf{(1-3)}$$

where

i_n = n transistor transient current
i_p = p transistor transient current

For a step input and with $i_n(t) = C_L dV_o / dt$ (C_L = load capacitance)

$$P_d = \frac{C_L}{t_p}\int_0^{Vdd} V_o dV_o + \frac{C_L}{t_p}\int_{Vdd}^{0}(V_{dd} - V_o)d(V_{dd} - V_o)$$
$$= \frac{C_L V_{dd}^2}{t_p}$$

with $f_p = \frac{1}{t_p}$, we have

$$P_d = C_L V_{dd}^2 f_p \qquad \textbf{(1-4)}$$

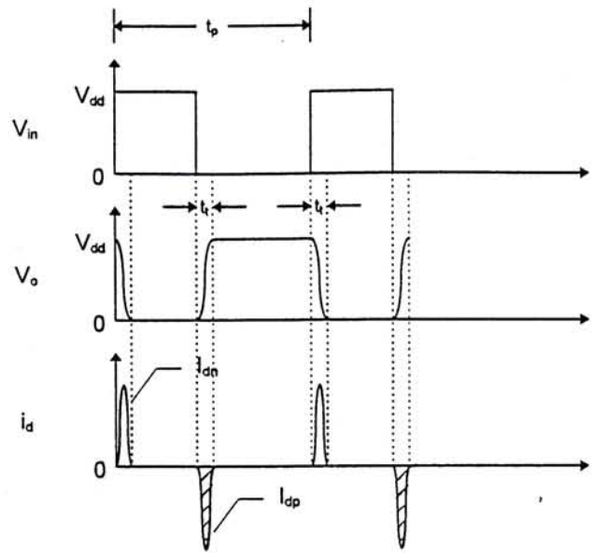


Figure 1-5 Waveforms for explanation of dynamic power dissipation

Equation (1-4) shows an important factor that the dominant dynamic power dissipation is proportional to the operation frequency.

1.4.2.3 Total power consumption

The total power consumption of an integrated circuit is the sum of the static and the dynamic dissipation, i.e.,

$$P_{total} = P_s + P_d + \text{short circuit power dissipation} \qquad (1\text{-}5)$$

1.5 Adiabatic Logic

1.5.1 Low power electronics

Reducing the power consumption of the electronic devices are becoming a very hot research topic. There are two main reasons for the industry demanding low power electronic devices.

1. The power used by the CMOS circuit becomes heat when charges flow from the source to ground. In equation (1-4), we know dynamic power dissipation of

the CMOS circuit is known as $P_d = C_L V_{dd}^2 f_p$. The energy consumption of the circuit increases as the digital circuits are going to operate in higher clock frequencies. The heat produced by an integrated circuit operating in a high frequency can destroy the circuit itself.

2. Portable electronic products such as mobile phone, notebook computer and so on are very popular nowadays. Since most of these products are powered by battery, reducing power consumption means lengthening the operation time before replacing or recharging the battery.

Since the increase in power consumption due to increasing the operation frequency is non-reducible by the conventional static CMOS technology described in chapter 1.3.1, scientists tried different ways to reduce the power consumption of digital circuit such as reducing the operation voltage of static CMOS. However, there seems to be a limit of 0.9V in the operation voltage reduction which will be approached soon. In this moment we have another solution adiabatic logic making use of adiabatic charging and charge recovery technique.

1.5.2 History of adiabatic logic

The biggest breakthrough of adiabatic logic is recovering the charge stored in the node capacitance of a digital circuit revealing logic levels and using adiabatic charging technique to reduce the loss to the on-resistance. Unlike conventional static CMOS, adiabatic logic redistribute the charges in the capacitors instead of discharging them to the ground. Theoretically, adiabatic logic can use zero energy after the circuit is initiated. This is why the technology is called "Adiabatic Logic".

In 1993, Younis and Knight [1] and Merkle [2] first proposed adiabatic logic with almost zero power dissipation. In 1995, Dickinson and Denker [3] introduced adiabatic dynamic logic (ADL) and Wang and Lau [4] introduced Adiabatic pseudo-domino logic (APDL). However, all of the proposed enhancement listed are not compatible to the static CMOS logic design. This means it is difficult to

convert the static CMOS design to adiabatic logic. For instance, adiabatic dynamic logic must utilise precharge, input, evaluate and hold stages controlled by a four-phase clock. Adiabatic pseudo-domino logic use a clock to control the charging and evaluation stages similar to the CMOS domino logic.

To maintain the compatibility with the conventional static CMOS, adiabatic quasi-static CMOS (AqsCMOS), that utilise quasi-static architecture, is proposed in the thesis. The main difference of AqsCMOS from ADL and APDL is the AqsCMOS can drive and be driven by a conventional static CMOS logic device directly. The basic concept of the AqsCMOS is making use of a relatively high frequency adiabatic clock instead of employing multistage operation. This makes converting the design based on conventional static CMOS to AqsCMOS possible. Details about AqsCMOS technology will be introduced and discussed in chapter 3.

1.6 Resources

1.6.1 Computing instrument

Sun Microsystems - SPARCStation 10 with 32MByte RAM
SPARCStation 20 with 64MByte RAM
Ultra 1 with 64MByte RAM

1.6.2 CAD tools

- Schematic capture
  Cadence ASIC Front End version 4.3

- Layout Editor
  Cadence Layout Plus version 4.3
  Cadence ES2 Design Kit 2.1

- Simulation Tool
  HSPICE version h93a by Metawave
  HSPICE version 96 by Metawave

- Circuit Model Library
  ECPD07 HSPICE Lev 6 Rev 4
  ECPD10 HSPICE Lev 6 Rev 5

1.6.3 Fabrication

- ES2 through CMP, France

- Technologies
  Dual Metal, 0.7 micron, p-well CMOS Technology (ECPD07)
  Dual Metal, 1.0 micron, p-well CMOS Technology (ECPD10)

1.7 Organisation of the Thesis

Following this introduction chapter, the background theories of Adiabatic CMOS and Clocked Adiabatic CMOS Technology will be discussed in chapter 2. Based on these theories, Adiabatic Quasi-static CMOS (AqsCMOS) Technology is proposed. In chapter 2, the concept of AqsCMOS will be introduced. AqsCMOS logic will not work with the logic gates alone without Adiabatic Clocks Generator. Chapter 5 and 4 show the designs of Adiabatic Clocks Generators and Adiabatic CMOS Inverters. These chapters will also discuss the considerations in designing the gates and clock generators. To verify the theories and reveal the feasibility of the proposed technology, two test clips are designed and tested. The measuring results of the test clips are shown in chapter 6. The thesis will be concluded in chapter 7. This chapter collates the work that has been performed in the course of the research and makes suggestions for the future work.

2. BACKGROUND THEORIES

2.1 Limit of energy dissipation

In 1988, Bennett [5] proved for every operation of an irreversible device, there must be an energy dissipation not less than $kT\ln 2$ (where k is Boltzmann's constant and T is the temperature).

Consider Merkle's example about the energy dissipation of an irreversible device [2]. When an "AND" gate of power supply 1V allows 100 electrons to flow from ground to the supply during switching operation. The energy dissipation will be 100eV. This value is about $4000kT$, for T is 300K, which is still comparatively very larger than the theoretical limit. However, by observing the trend of modern electronics, we will reach the value $4000kT$ before the year 2000 and the physical limit by the year 2015. To overcome the barrier $kT\ln 2$ which limits the operation frequencies of electronic devices as discussed in chapter 1.5.1, reversible devices must be developed.

2.2 Reversible Electronics

2.2.1 Reversibility

Consider the operation of a CMOS inverter in Figure 2-1.

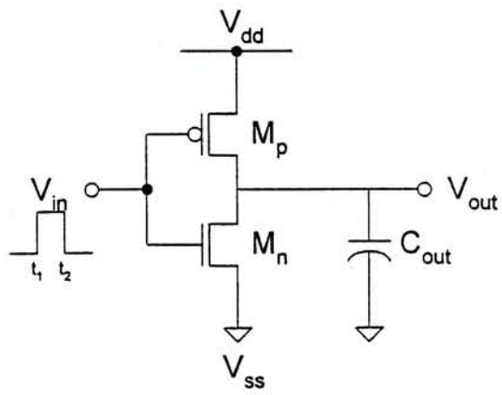


Figure 2-1 Inverter for reversible devices description

At time t_1, the charge stored in C_{out} will be discharged to V_{ss} by M_n. When time = t_2, the C_{out} will be charged up to V_{dd} by M_p. These two operations erase the original statuses of the information storage device completely for the new information. By the historical paradox of Maxwell's demon in thermodynamics of information process [6], each of these erasing operations is equivalent to an increase of entropy in the universe as a whole by at least $k\ln 2$. Therefore, an energy dissipation not less $kT\ln 2$ is unavoidable. In fact, the charging process dissipates $\frac{1}{2}CV^2$ of energy and the discharging process dissipates also $\frac{1}{2}CV^2$ of energy.

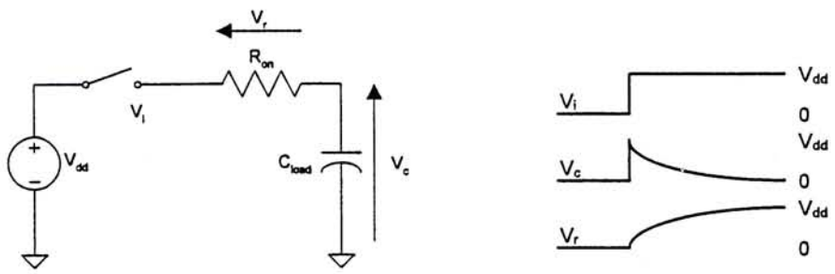
However, if we can, by some means, deposit the charge originally stored in C_{out} (information) instead of discharging (erasing) them to V_{ss} at t_1, and withdraw the charge stored at t_2 and recover it to C_{out}, we can avoid the irreducible thermodynamic cost as the information is never erased. These charge recycling and non-erasing operation are an examples of reversible operations. Also, all the devices performing reversible operations are called reversible devices.

Theoretically, by using reversible devices, we can create circuits consuming zero power.

2.2.2 Adiabatic Switching

2.2.2.1 Conventional Charging

When the input of a CMOS inverter goes from high to low, the circuit can be modelled as shown in Figure 2-2.



(a) (b)

Figure 2-2 Conventional charging model

When the switch is closed, the full potential of the supply appear across the on-resistance R_{on}, causing the load capacitance C_{load} to start charging. The voltage across R_{on} decays as the capacitance is charged to V_{dd}. When the load capacitor is fully charged up, a charge $q = C_{load}V_{dd}$ flows from the supply to the load capacitance. By calculating the energy consumption, $E_T = qV_{dd} = C_{load}V_{dd}^2$ is transferred from the supply.

Only 50% of the energy consumption goes to the capacitance while the energy stored in the capacitance is only $\frac{1}{2}C_{load}V_{dd}^2$. The other $\frac{1}{2}C_{load}V_{dd}^2$ is dissipated as heat primarily in the on-resistance. The energy dissipated as heat can never be recycled by any reversible devices.

The same situation occurs when the load capacitance is discharged. When the input of the inverter goes high, the load capacitor is discharged to V_{ss} and the energy stored will totally dissipated as heat by the on-resistance of the n channel transistor. The charging and discharging processes result in the conclusion about power dissipation described in (1-4).

2.2.2.2 Adiabatic Charging

From chapter 2.2.2.1, the energy dissipated by the on-resistance when there is a high potential difference across the resistance as shown in Figure 2-2b. If we replace the dc supply and the switch shown in Figure 2-2a by a ramp supply, the potential across the on-resistance can be controlled. By increasing the period of the ramp, the V_r can be kept small.

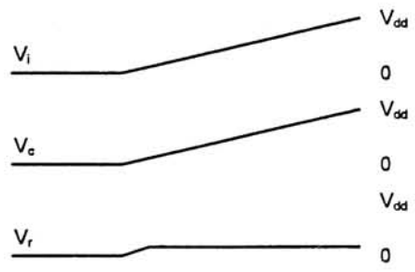


Figure 2-3 Adiabatic charging

If the period of the ramp is much larger than the time constant, i.e., $T >> RC$, the power dissipation, from Athas [8], will be

$$E_T = I^2 R_{on} T = \left(\frac{C_{load} V_{dd}}{T}\right)^2 R_{on} T = \left(\frac{R_{on} C_{load}}{T}\right) C_{load} V_{dd}^2 \qquad (2\text{-}1)$$

Also, the similar discharge can be arranged with a descending ramp.

By this conclusion in (2-1), we can reduce the power consumption by increasing the period of ramp. Athas and Koller called this adiabatic charging process and Merkle called this reversible charging because of its non-dissipative nature. Younis and Knight [1] also achieved adiabatic charging by using an inductor (Figure 2-4) and similar conclusion about energy is drawn in (2-2).

$$E_{loss} = 2C_{load} V_o^2 (1 - e^{\frac{-\pi\alpha}{\omega_d}}) \qquad (2\text{-}2)$$

where

$$\alpha = \frac{R}{2L}$$

$$\omega_d = \sqrt{\omega_o^2 - \alpha^2}$$

$$\omega_o = \frac{1}{\sqrt{LC}}$$

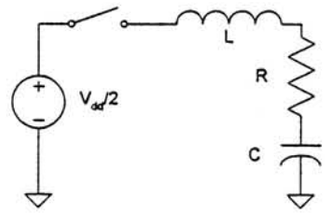


Figure 2-4 Athas and Koller's adiabatic charging model

2.2.3 Reversible devices

A lot of reversible devices have been proposed. Fredkin and Toffoli [7] realised the conservative logic by switches, capacitors and inductors. Younis and Knight [1] introduced charge recovery logic (CRL) of adiabatic family with their reversible charge recovery gate. However, these reversible gates are normally very complicated and large when compared with the conventional CMOS circuits.

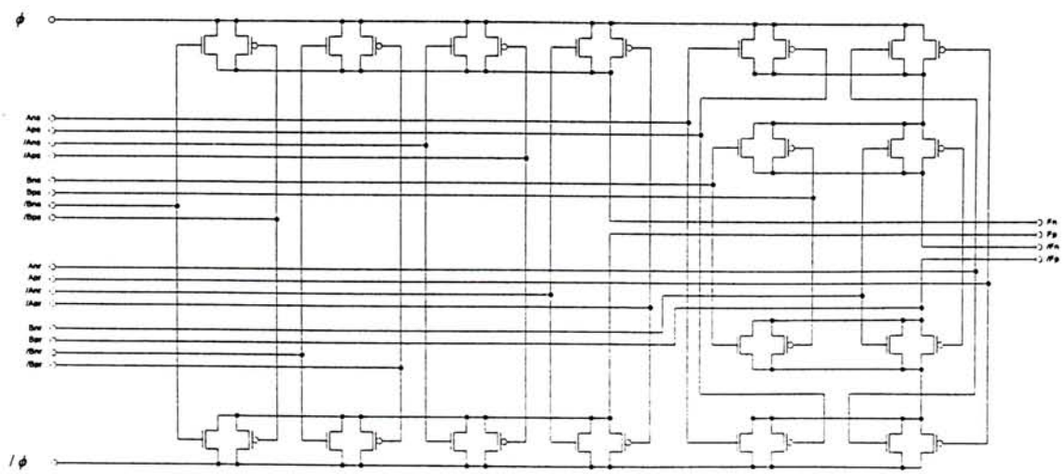


Figure 2-5 Younis and Knight's CRL 2-input AND/NAND gate

For example, the CRL AND/NAND gate as shown in Figure 2-5 required 32 transistors which is 5 times more devices than a conventional CMOS logic.

Dickinson and Denker [3] introduced Adiabatic Dynamic Logic (ADL), that is not completely adiabatic. However, it is simple and readily cascadable as shown in Figure 2-6. The size of ADL gates is small when compared with CRL.

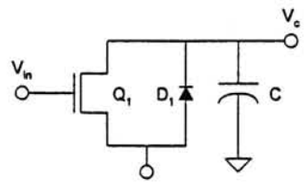


Figure 2-6 Adiabatic Dynamic Logic inverter

ADL requires a pair of complementary adiabatic clocks to further reduce the energy consumption with charge recovery technique. AqsCMOS also use similar clock signals to recycle the charge for information storage. The complementary clock signals are generated by an adiabatic clocks generator which is basically an LC oscillator. The details about the adiabatic clocks generator will be discussed in chapter 5.

2.3 Compatibility to CMOS Logic

Besides the CRL and ADL proposed, there were also adiabatic devices being developed. For example, Wang and Lau's [9] Adiabatic pseudo-domino logic (APDL), Mateo and Rubio's [10] Quasi-adiabatic ternary CMOS logic (QAT), and Moon and Jeong's [11] Efficient charge recovery logic (ECRL). However, most of them are dynamic logic and not compatible to the conventional CMOS logic which is the most commonly used in circuit design.

In the following chapters, we will show simulation results and actual measurements of AqsCMOS to illustrate the compatibility with a conventional CMOS circuit.

3. ADIABATIC QUASI-STATIC CMOS

3.1 Swinging between 0 and 1 by Harmonic Motion

3.1.1 Starting from a simple pendulum

Let us look at a mass m connected to a long string of length l as shown in Figure 3-1. The mass and string can be a simple pendulum swing between position a and b in simple harmonic motion. In the ideal case, the swing will never stop without external interference.

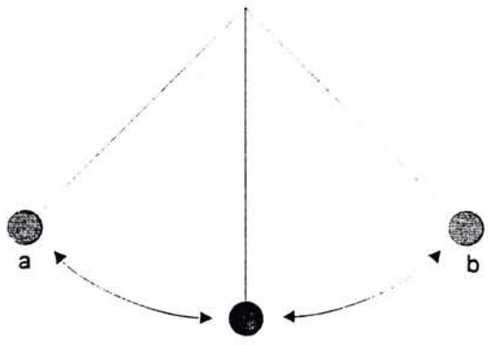


Figure 3-1 A simple pendulum

We can assign logic levels to different position of the swing, for example, position a is assigned to be logic 0 (low) and position b is assigned to be logic 1 (high). We can say when the mass move to position a, the system is revealing logic 0 and when the mass move back to position b, the system is revealing logic 1. Notice that the system switching from 0 to 1 repeatedly without energy loss.

Keeping the output of the system high or low is easy by holding the mass in our

hand at position a or position b respectively. If the mass is stopped at the highest position, the velocity of the mass should be zero. Therefore, no energy is needed for retardation. As a whole, we can switch the output of the system under control without consuming power.

3.1.2 Inductor-capacitor oscillator

Similar oscillator can be implemented by inductors and capacitors. To control the potential swing in the system, switches can be placed between components. Figure 3-2 shows a simple *LC* oscillator switches. When *sw*1 and *sw*2 are closed and sw3 is open, the capacitor *C1* will be fully charged up to V_{dd} and the *C2* will be totally discharged. Then, by opening all the *sw*1's and closing *sw*3, the oscillator start oscillation and periodically charge up and discharge the capacitors[1] with frequency f without consuming any extra energy.

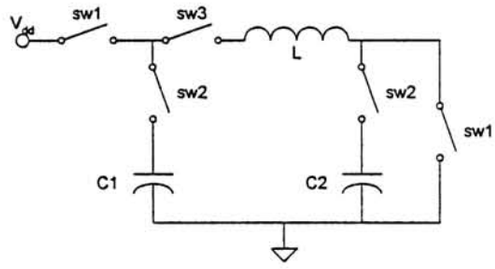


Figure 3-2 A simple LC oscillator

If $C1 = C2 = C$, by conservation of energy in a harmonic motion, the frequency of the oscillation will be

[1] During the oscillation, the potential across *C1* and the potential across C2 will always be the complements of each other, i.e., when *C1* is fully charged up to Vdd, C2 will in the same time be fully discharge and vice versa.

$$f = \frac{1}{\pi\sqrt{2LC}} \qquad (3\text{-}1)$$

By switching *sw2*'s on and off in the proper time, we can control the status of either *C1* or *C2* similar to the hand does to the pendulum in chapter 3.1.1.

If C1 and C2 are the node capacitances of logic gates, the conclusion about the oscillator means it is possible to switch the logic levels with zero energy consumption.

3.2 Redistribution of Charge

Using harmonic motions, we can achieve the reversible operation as discussed in chapter 2.2.1. Consider there are two capacitors (information storage devices) *C1* and *C2*, *C1* is charged up to V_{dd} and *C2* is fully discharged. Let a charged capacitor represents logic 1 and a discharged capacitor represents logic 0. If we want to change the logic levels being stored in the capacitors, by the conventional way the original information stored must be destroyed. For example, to change the logic level of C1 to logic 0 we must connect both terminals of the capacitor to ground. Also, we must connect the *C2* between a power supply if we want to store logic 1 to *C2*. According to chapter 2.2.2.1, each of these two operations wastes $\frac{1}{2}CV^2$ energy. However, we can change the logic levels by redistributing the charge stored in the capacitors instead of destroying it.

In Figure 3-3 a simplified LC oscillator with two pairs of capacitor is shown. Similar to the situation described in the pervious paragraph, initially *C1* is fully charged up to V_{dd} and *C1'* is fully discharged, *C2* is fully discharged and *C2'* is fully charged up to V_{dd}. Consider at time = 0, *sw1* switches to *C1* and *sw2* switches to *C1'*, harmonic oscillation starts and the charge stored in *C1* starts to flow to *C1'*. When all the charge flows from *C1* to *C1'* at $t = t_1$, the switches move to the original position. Then the logic level of *C1* is changed from logic 1 to zero. If we switch *sw1* to *C2* and *sw2* to *C1'*, the charge originally stored in *C1* will now flow into *C2*. Finally, we can exchange the logic level stored in *C1* and *C2* without consuming extra energy by connecting the capacitors together selectively. By the similar

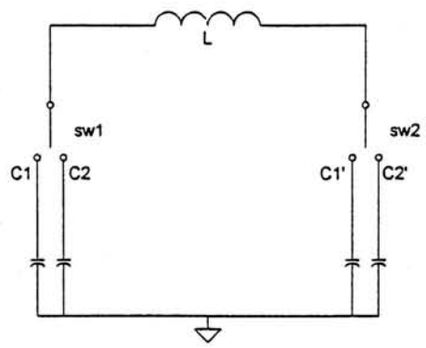


Figure 3-3 LC oscillator of selectable capacitor pairs

switching operations, we can fully control the status of C1 and C2.

3.3 Adiabatic Quasi-static Logic

3.3.1 False reversible inverter

Figure 3-3 shows a selective harmonic charging and discharging by switches. If the capacitors are replaced by the gate capacitances of transistors, it is possible to switch the logic gates by reversible operations through the harmonic motion between inductors and capacitor. As concluded in chapter 2.2.1, we can reduce the power consumption significantly.

In Figure 3-4, a reversible inverter model based on harmonic charging and discharging is constructed. By the "*Control*" signal and its complement, we can control the input to the inverter *INV*. The capacitor $C_{compensate}$ stores the charge for the gate capacitance to switch the inverter when the gate capacitance is required to be discharged for logic low.

This circuit requires no energy to operate when the output loading is zero while the charge is never grounded. However, the output node capacitance is still connected across the V_{dd} and V_{ss}. Energy is dissipated when charge is taken from the V_{dd} to the nonzero node capacitance (non-floating node) and discharged to V_{ss} during switching.

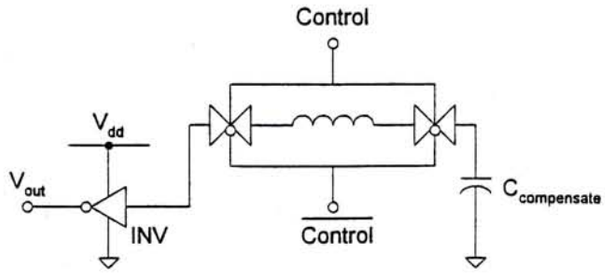


Figure 3-4 False reversible inverter

The other problem of the inverter is that the switching is controlled by the control signals yet there is no direct logic relationship between the control signals and the output, V_{out}, i.e., the circuit is not a inverter. In conclusion, this "inverter" is not cascadable.

3.3.2 Adiabatic inverter

The inverter in Figure 3-4 is modified to a real reversible inverter shown in Figure 3-5. Define that V_{in} is connected to a pair of current direction control devices (Figure 3-6). The device is a switch controlled by V_{in}. When V_{in} is logic 0, the switch selects the 0 size and allow current flow upward only. Similarly, the current will be allowed to flow downward only when V_{in} is logic 1. C_{node} represents the node capacitance of the output pin V_{out}. On the other side of the oscillator, a compensate capacitor $C_{compensate}$ of size equal to the C_{node} is connected to the inductor for the completion of the oscillator in the situation that only one inverter is used. V1 and V2 are a pair of complementary signals which charge and discharge the capacitances.

First of all, assume C_{node} is fully discharged and $C_{compensate}$ is charged to V_{dd}. When Vin of the inverter is logic low, the charge flows from the $C_{compensate}$ to C_{node} only. C_{node} will then be charged by harmonic motion which rises V_{out}. When the C_{node} is fully charged up by the charge originally stored in $C_{compensate}$, the further harmonic motion is block by the current direction control devices. Vout will therefore be rose to V_{dd} and maintained. When the input is logic high, the charge flow back to $C_{compensate}$ and the V_{out} drops to V_{ss} again.

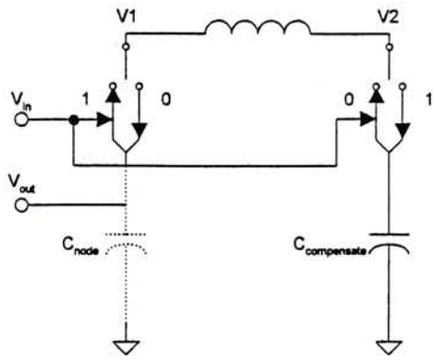


Figure 3-5 Real reversible inverter

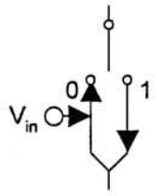


Figure 3-6 Current direction control device

Observing the relationship between V_{in} and V_{out}, we can find $V_{out} = \overline{V_{in}}$. This is a direct inverting relation between V_{in} and V_{out}. Besides, we can find that there is no path between V_{dd} and V_{ss}. All the charge involved in logic operations are recycled. Referring to the logic relation and energy consumption, this real reversible inverter is also cascadable.

According to chapter 2.2.2.2, the power consumption by the on-resistance of the real switching devices can be reduced by adiabatic charging. This real reversible inverter also utilises adiabatic charging. However, it is not fully adiabatic because the charging and discharging processes are done by a sinusoidal signal not a ramp. By equation (3-1), we can increase the period of charging/discharging sinusoidal signal by increasing the size of inductor. Therefore, the inverter is also named "adiabatic inverter".

3.3.3 Effective capacitance

The adiabatic inverter shown in Figure 3-5 allows harmonic motion only when the inverter switch. After the switching is done, the current direction control devices stop the motion. In the inductor's point of view, a switching inverter is a effective capacitance equal to the node capacitances. After the switching process is finished, there will be no charge flow into nor out of the node capacitance, the size of effective capacitance is then greatly reduced to negligible after switching.

Consider $2n$ adiabatic inverters of same size are connected symmetrically, in the both sides of the inductor, i.e., n inverters are connected in each side of the inductor. Assume the inverters are being operated arbitrarily, the probability density function, that each of the inverters is found to be switching within a period of time t, is a constant p. We can expect that the overall capacitance of these n inverters will very likely be a constant when n is large enough. The effective capacitance as seen by the inductor of these n inverter will be

$$C_{effective} = \frac{nC_{node}}{t}\int_0^t pdt = npC_{node} \qquad (3\text{-}2)$$

where

$C_{effective}$ = overall effective capacitance of n inverters, and
C_{node} = node capacitance of each inverter.

In the equation (3-2), the probability density function is governed by the overall switching frequency, $f_{switiching}$, of the inverters and the time of each switching process. The switching time can be calculated by equation (3-1) and equals $\frac{1}{2f} = \pi\sqrt{\frac{LC_{effective}}{2}}$. The probability density function is therefore given by

$$p = \frac{1}{2f} \Big/ \frac{1}{2f_{switching}} = \pi f_{switiching} \sqrt{2LC_{effective}} \qquad (3\text{-}3)$$

Combining the equations (3-2) and (3-3), we have

$$\begin{aligned} C_{effectiv} &= npC_{node} \\ &= n\pi f_{switiching} C_{node} \sqrt{2LC_{effective}} \\ \therefore C_{effectiv} &= 4n^2\pi^2 f_{switiching}^2 C_{node}^2 L \end{aligned} \qquad (3\text{-}4)$$

From equation (3-4), we can model the inverters by simply a pair of capacitors. This result reduce our circuit back to the simple *LC* oscillator as shown in Figure 3-2 A simple LC oscillator. Thus, when the circuit is operating, an oscillation at a frequency equals $\pi\sqrt{2LC_{effective}}$ will be found in each side of the inductor. The operation is different than the single inverter described in chapter 3.2, where the oscillation is stopped when the inverter is not switching. The oscillation signals *V1* and *V2* become the clock signals responsible for all the switching process[2].

3.3.4 Logic alignment

Chapter 3.3.3 shows that the harmonic oscillation will go on across the inductor with a circuit constructed by the logic described in chapter 3.3.2 is operating. Since all the charging and discharging processes are done by the harmonic oscillation of *V1* and *V2*, the node capacitance cannot be fully charged or discharge immediately when the input switches the current control devices. In fact, the node capacitance will be fully charged or discharge when the clock signals source or sink the capacitance.

Consider a harmonic motion of frequency f is oscillating across the inductor.

---

[2] "*V1*" and "*V2*" will be named "adiabatic clocks" in the coming chapters and abbreviated as "*aclk+*" and "*aclk-*".

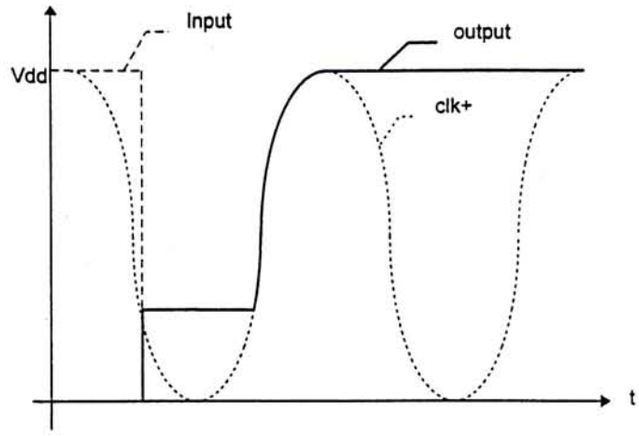


Figure 3-7 Graph describes logic alignment

When the input of a adiabatic inverter goes to a logic 1, the output should be 0, which means discharging the node capacitance. Since the input is not synchronised with the oscillation, the current direction control device may be switched when the *V1* is rising. If *V1* is smaller than V_{dd}, the capacitance C_{node} will be immediately discharged to the same potential as *V1* by the current direction control device. Then, the potential of C_{node} will be held until *V1* rise to the maximum point and fall to the potential of C_{node}. The current direction control device will then allow further discharge of C_{node} to V_{ss} as shown in Figure 3-7.

If the harmonic oscillation is sufficiently faster than the logic, the delay due to logic alignment is negligible. However, if the harmonic oscillation is too fast, according to the principle of adiabatic charging described in chapter 2.2.2.2, there will be a large energy loss to the on-resistance. In general, the author proposes that the oscillation should be about ten times faster than the logic.

We can feed the input signal into the adiabatic logic in anytime without waiting for the precharge period of the system clock. Moreover, the output is available directly from the output terminal shortly after the input is fed without waiting for the evaluation period of the system clock. This property is very similar to static CMOS. Yet, there is still a system clock inside the circuit for the charging and discharging processes. The logic is therefore called "adiabatic quasi-static CMOS logic". The harmonic oscillation signals *V1* and *V2* is called "adiabatic clock

positive (Abbr. *aclk*+)" and "adiabatic clock negative (Abbr. *aclk*-)"[3] respectively.

3.3.5 Cascading the adiabatic inverters

As claimed in the chapter 3.3.2, we can cascade adiabatic inverters and form an inverter chain. The major concern of cascading is the balance of capacitance being connected to both sides of the inductor. There are two methods proposed for the balance of capacitance.

3.3.5.1 Compensated cascading

The first way is using a compensation capacitor $C_{compensate}$ of size equal to the load capacitance C_{load} to balance the loads as shown in Figure 3-8. Connecting in this way guarantees the symmetry of the capacitances. However, this method requires extra capacitances which do not involve in the actual logic operations. The extra capacitances will increase the power consumption in real life because of the non-ideal properties of a capacitor, such as leakage current, parasitic resistance and so on. Also the size of the

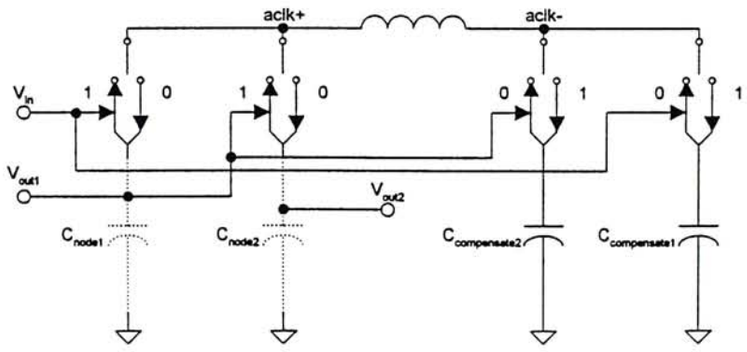


Figure 3-8 Cascading adiabatic inverters by compensate capacitors

[3] Adiabatic clock positive (aclk+) and adiabatic clock negative (aclk-) do not have any physical difference because of the symmetry of the circuit. Circuit designer may arbitrarily choose one of the adiabatic clock signal to be aclk+, then the other will be aclk-.

circuit is increased by the extra capacitors used.

By using matched compensate capacitors the symmetry of the capacitances are guaranteed. However, it is very difficult to make a compensate capacitor perfectly match to a node capacitance. The mismatching of capacitance can make the harmonic motion asymmetric.

Since one compensate capacitor will be switched to store charge when its corresponding node capacitance is switched to discharge and vice versa, compensated cascading virtually redistributes the charge in the compensate capacitor and node capacitances during operations.

3.3.5.2 Balanced cascading

We can replace the compensate capacitor by connecting the actual logic device to the inductor in a balanced way for capacitance balancing. Figure 3-9 shows an example of two inverters in balance cascading.

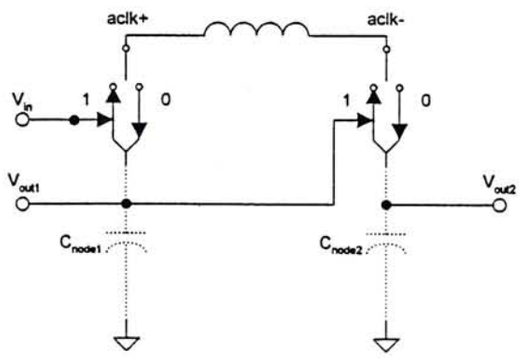


Figure 3-9 Cascading adiabatic inverters by balanced connection

Unlike compensated cascading, balanced cascading do not employ capacitor matched to the logic device. The circuit designer must be very careful about the symmetry of the capacitance connected in the sides of the inductor.

Balanced cascading eliminates all the compensate capacitors which do not participate in logic operation. Normally, compared with compensated cascading, balanced cascading reduce the number of capacitor used by 50%.

Besides the size reduction, eliminating the energy storage capacitors also reduce the energy dissipates to the on resistance of switching devices as discussed in chapter 2.2.2.2. Halving the effective capacitance increase the frequency of the harmonic motion by $\sqrt{2}$. The energy dissipation will increase with the shorter charging period (refer to equation (2-1)). The period of the harmonic motion can be lengthen by increasing the size of inductor.

Omitting the compensate capacitance means charge redistributes amongst the node capacitance during logic operations. Consider the probability of each of the switching devices to be switched on is the same. When the number of switching devices is large, and the randomness of switching is ensured, the charge stored in the whole circuit should be constant at anytime. Then we do not need any extra charge storage devices to buffer the extra charge. Therefore, balance cascading can be used only when the size of circuit is large and the logic devices are switched randomly. Otherwise, compensated cascading should be used. Partly balanced and party compensated cascading is also possible.

3.4 Frequency Control

Chapter 3.1.2 discussed the frequency of adiabatic clocks. When we design a circuit operating in x Hz, the harmonic motion should be oscillating in $10x$ Hz. To control the harmonic oscillation, it is impossible to control the capacitive part of equation (3-1) because the effective capacitance is controlled by the circuit size and its design. Therefore, we should first find the value of effective capacitance, then choose an inductor of proper size.

3.5 Compatibility of AqsCMOS with Static CMOS Logic

As described in chapter 2.3, most of the adiabatic logics proposed are not compatible to static CMOS. First of all, they cannot handle random logic function because the input will not be retrieved by the logic device until the evaluation phase. Also, incompatibility can be caused by different logic representation. For example, the logic representation of TTL and static CMOS are different in terms of the electric potential.

Referring to chapter 3.3, we have proven that AqsCMOS can handle random function. This make a real time information transfer between AqsCMOS logic and conventional static CMOS logic possible. If AqsCMOS and conventional static CMOS can share the same logic representation especially electrical potential, AqsCMOS can be used to drive and can be driven by static CMOS.

In chapter 3.3.2, it is illustrated that current direction control device will fully charge the load capacitance to V_{dd} for logic high and fully discharge it to ground potential for logic low. The output of AqsCMOS is able to drive conventional CMOS directly. Similarly, the current direction control are configured to be controlled by simple electrical potentials. For examples, the current direction control device being shown in Figure 3-6 allows the current to flow downward when the control signal is V_{dd}, and vice versa. The control signal can therefore the output of a static CMOS device.

Therefore, AqsCMOS inverter can be used to drive a static CMOS device as well as can be driven by a static CMOS device theoretically.

4. ADIABATIC QUASI-STATIC CMOS INVERTERS

4.1 Design

4.1.1 Realisation of current direction control device

Figure 3-6 shows the current direction control device which is a main part of an AqsCMOS inverter. In chapter 3, we regard this device as a black box. To realise AqsCMOS logic, we have to implement the current direction control device by semiconductor devices.

The current direction control device has two functions, controlling the direction of current flow, and performing logic functions. To control the direction of current flow, it is obvious that diode must be used. However, a diode allows current flow through in one direction only. We must use two diodes to make current flow in selected direction possible. Selection of current direction can be done by switching

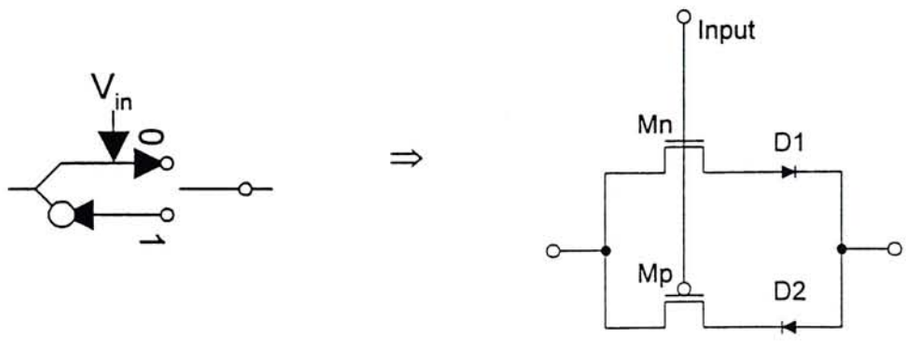


Figure 4-1 Realisation of current direction control device

devices such as PMOS and NMOS.

Therefore, a current direction control device can be constructed as shown in Figure 4-1. When input is high, *Mn* is switched on and *Mp* is switched off and only the diode *D1* is conducting. Similarly, when input is low, Mp will be turned on by input low, which enables D2 to pass the current flows toward left.

4.1.2 Implementation of AqsCMOS inverter by current direction control device

With the current direction control device realised in chapter 4.1.1, AqsCMOS inverter is implemented in Figure 4-2. The AqsCMOS inverter is powered by an adiabatic clock signal ϕ. An n channel transistor is used to pass logic zero to the output node because n channel transistor can pass a true zero. Similarly, an p channel transistor is used to pass logic one to the output node.

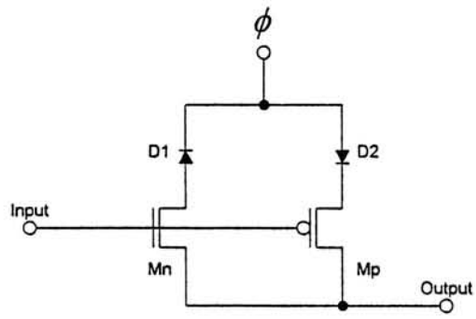


Figure 4-2 Schematic view of an AqsCMOS inverter

When the input is low, the p channel transistor will be turned on during the positive cycle of the adiabatic clock. The diode *D1* will then charge up the output node to one diode drop below the peak voltage of the adiabatic clock signal. When the adiabatic clock signal reach its negative cycle, both transistor will be turned off. Then the potential at the output node will be held at a constant. In the contrary, when the input is high, the output node will be discharged to the diode potential in the negative cycle of the adiabatic clock and the potential will be held in the positive cycle of the adiabatic clock. As stated in chapter 3.3.4, all output transition will be

aligned to the edge the sinusoidal adiabatic clock.

4.1.3 Layout

A layout of 100μ/50μ AqsCMOS inverter based on 1μ technology is shown in Figure 4-3. This inverter is composed of two diodes, 1 p channel transistor of channel width 100μ and 1 n channel transistor of channel width 50μ.

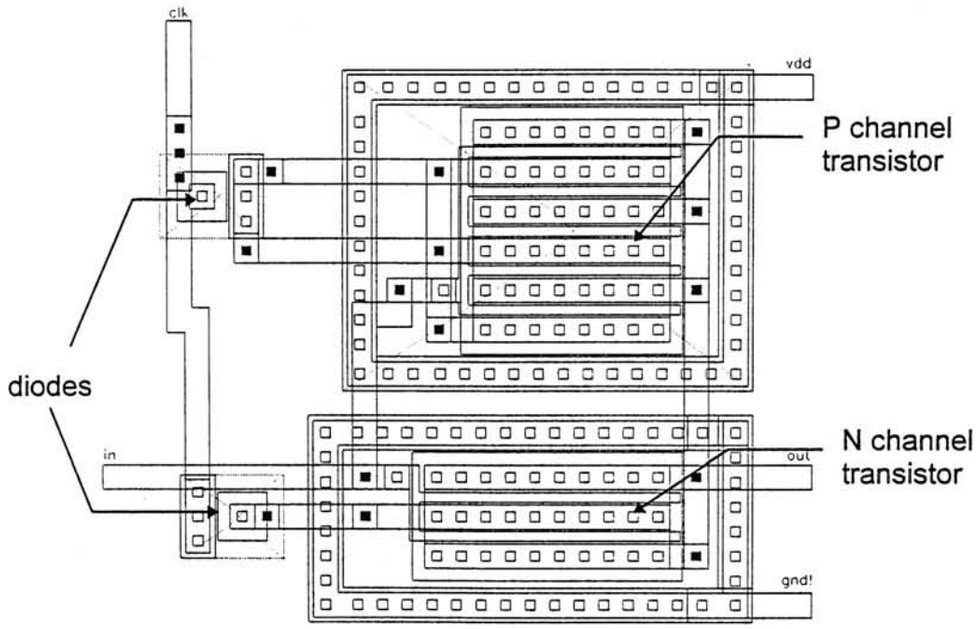


Figure 4-3 Layout view of AqsCMOS inverter

4.1.3.1 Horizontal Transistor Diode

In CMOS industry, a diode is usually constructed by connecting the gate and drain of a n channel transistor together as shown in Figure 4-4. Provided that the V_A is larger than V_B, the transistor will always be biased to saturated region. The drain current I_s pass through the drain-source junction will be governed by equation (4-1).

$$I_{DS} = \frac{\mu_n C_{ox} W}{2L}(V_A - V_B - V_T)^2 \qquad (4\text{-}1)$$

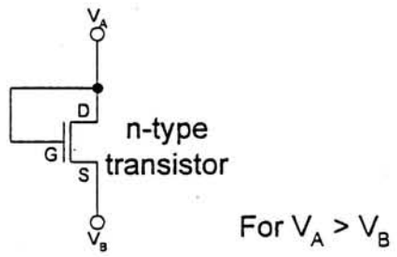


Figure 4-4 A horizontal transistor diode

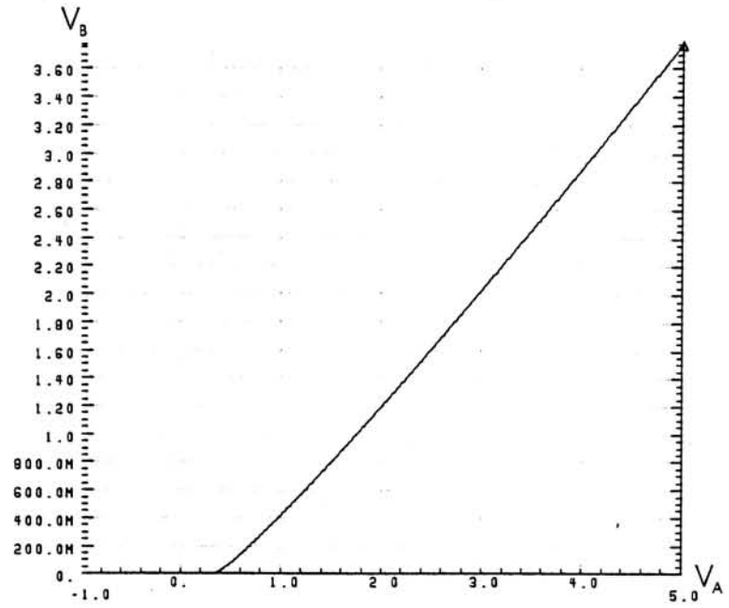
where

μ_n is the mobility of electron
C_{ox} is the oxide capacitance per unit area
W is the channel width of the n - type transistor
L is the chnnel length of the n - type transistor
V_T is the thershold voltage

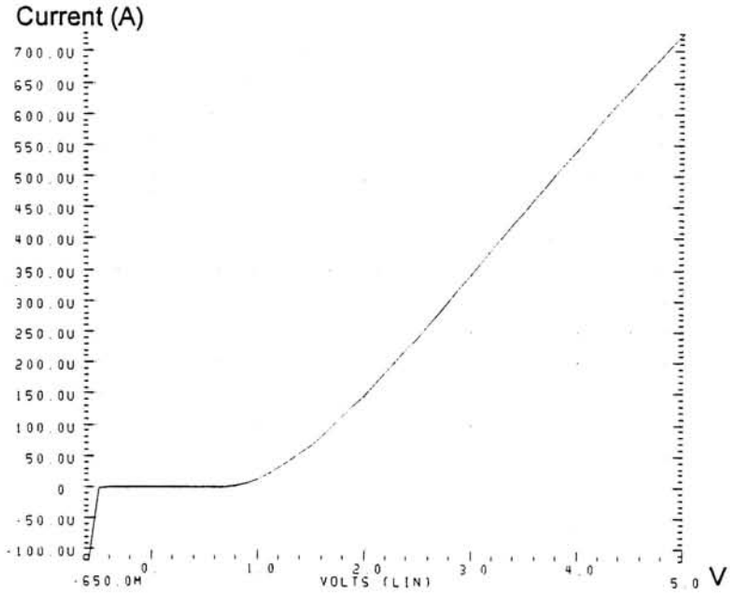
The current of the diode is controlled by the parameters W and L. The diode current can be increased by increasing the channel width. However, increasing the channel width increases the sizes of transistor capacitances, which will reduced the current flow at high frequency.

The biasing behaviour of a CMOS diode is investigated by simulations.

The V_A terminal is first connected to the DC power supply and the V_B terminal is connected to a very large load (1GΩ) to ensure the potential drop to the forward bias resistance of the diode negligible. A DC analysis about the diode voltage V_d in different supply voltage is done by HSpice using ES2 n channel transistor model. The channel width of the n channel transistor is 2.5μ and the channel length is 1μ. A plot on supply voltage against potential at terminal V_B is shown in Figure 4-5a.



(a)



(b)

Figure 4-5 Properties of a horizontal transistor diode

The figure (a) showed that the diode is switched off when the supply is lower than the threshold voltage 0.4V. V_B is risen when the supply voltage V_A increase beyond the threshold voltage. The diode voltage drop can be calculated by the difference between the V_A and V_B. The diode voltage V_D increase from 0.4V when the supply voltage is 0.4V to 1.3V when the supply voltage reach 5V. Comparing to the diode voltage of a simple p-n junction, this relatively high diode voltage results in a large reduction as well as power

consumption.

After finding diode voltage, the terminal V_B of horizontal diode is then connected to a small load (100Ω). With DC power supply of different values being connected to the diode, the properties of forward bias current and the reverse breakdown voltage is investigated.

Figure 4-5b, we can find the forward bias current is small. When the supply voltage is 5.0V, the forward bias current is only 730μA. This means there is a forward bias resistance of about 6.8kΩ. If the forward bias current is small, the time for charging and discharging the succeeding node capacitance will be long and lengthen the rise time and fall time. As a result, the speed of the logic is limited.

The reverse bias breakdown voltage is also illustrated in Figure 4-5b. The breakdown voltage of the diode is very small and about 0.7V. This value is actually diode voltage of a p-n junction. When the supply is -0.7V, the substrate drain junction is forward biased. The reverse bias current then become very large and the diode breakdown. If horizontal diode is used in AqsCMOS logic design, reverse breakdown can occur when the adiabatic clock reach its valley which can be lower than zero potential.

Because of the unsatisfactory properties of a horizontal transistor diode, a vertical diode based on the current n-well technology is fabricated.

The vertical diode, unlike transistors, is a vertical device. This is fabricated by creating a hot n-well on p-substrate. Then a p^+ active area is created on the n-well. The device is actually a p-n junction that allows current flow form p^+ active area to n-well only when V_A is larger than V_B. A comparison between horizontal transistor diode and vertical diode is done.

Similar to the simulations done on horizontal, a vertical diode based on ES2 model is simulated using HSpice. The area of p^+ active area of the simulated diode is 6.25μm². The first simulation finds out the forward bias diode voltage V_D by connecting the vertical diode to a 1GΩ and DC power supply. Figure 4-7a shows the relation between the supply voltage and potential V_B. The diode performs as open circuit when the supply voltage is lower than zero. The diode remains off when the supply voltage is larger zero. After the supply voltage is larger than about 0.8V which is similar to the diode voltage of a p-n junction, the potential of terminal V_B rise with the supply voltage in a constant slope. Finding the difference between the supply voltage and the potential of V_B, the diode voltage of the vertical diode is found to be a constant when the DC supply voltage is from 0.8V to 5V. Therefore, the maximum electrical potential of VB can be $5 - 0.8 = 4.2V$.

The vertical diode is then connected to a 100Ω load for investigation of forward bias current. The forward bias current of a vertical diode can be 95.0mA when the supply voltage is 5.0V as shown in Figure 4-7b. However, the maximum forward bias current of a horizontal transistor diode is only 470μA. As discussed in chapter 4.1.3.1, the small forward bias current means large forward bias resistance. This results slow logic and power

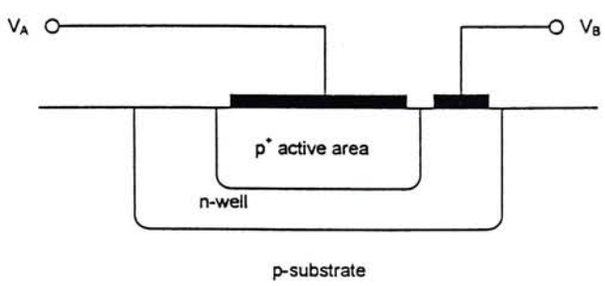


Figure 4-6 Vertical diode

consumption.

Also, the reverse bias breakdown voltage is large. The channel junction is still not breakdown when the supply voltage reach -5.0V. Large reverse breakdown voltage prevents the creation of short circuit from drawing large current.

In conclusions, a vertical diode is used in AqsCMOS inverter ensure of the low power consumption and small diode potential drop.

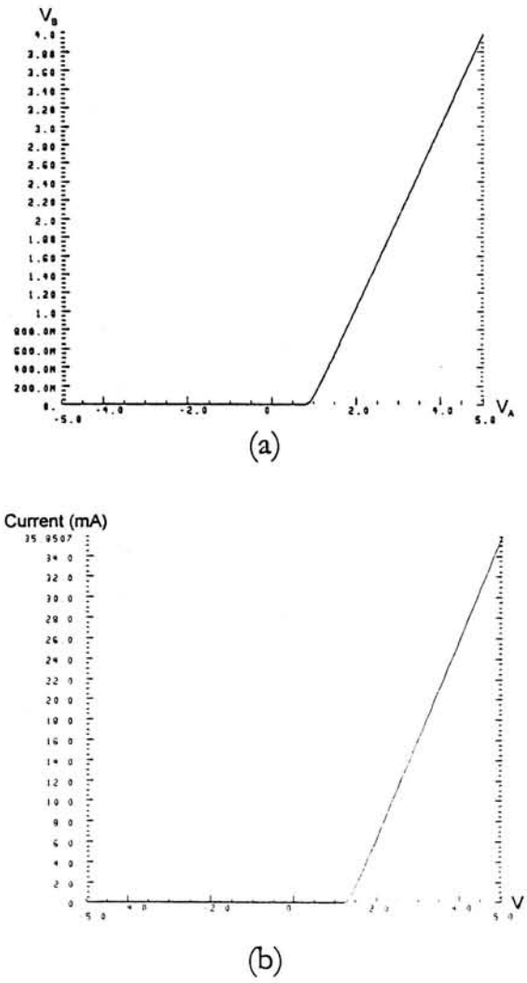


Figure 4-7 Figures showing properties of a real diode

4.1.3.2 Transistor pair

Besides the diodes, one n channel transistor and one p channel transistor are fabricated in the AqsCMOS inverter shown in Figure 4-3.

The sizes of the n-type and the p channel transistors control size of the node capacitance as well as the current sink and source the succeeding node capacitance.

There is a mobility different between electrons and holes. (In ES2 ecpd10 technology, μ_n in n-type is 500cm(Vs)$^{-1}$, μ_p in p-type is 175cm(Vs)$^{-1}$). To keep a symmetric sink and source current to the succeeding node capacitance, the size of the n channel transistor should be twice as large as the p channel transistor as shown in Figure 4-3.

4.2 Capacitance Calculation

Figure 4-8 illustrates all the parasitic capacitances of two cascaded AqsCMOS inverters when looking from the adiabatic clock input terminal *aclk*.

From this model, we can estimate the device capacitance of each AqsCMOS inverter for

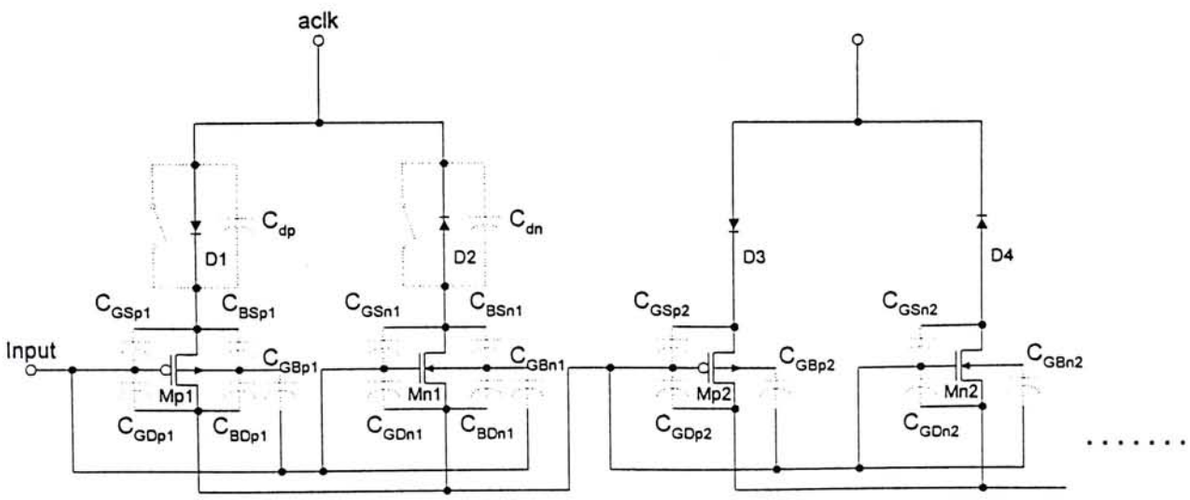


Figure 4-8 All capacitances can be seen by adiabatic clock

the calculation of adiabatic clock frequency as discussed in chapter 3.3.3.

4.2.1 Non-switching device

The capacitance will be very small when the device is not switching (refer to chapter 3.3.3). This can be proven by observing Figure 4-8. When the device is not switching. The potentials at the source of both p channel transistor and n channel transistor are kept constant. The potential at the p-type source will be V_{dd} - (*diode voltage*, V_d) while the n-type source will be kept at V_d. Then both of the diode *D1* and *D2* are not forward biased. What the adiabatic clock see is the diode capacitances. In this case, the diode capacitance is dominated by the junction capacitance C_j because of the transition region. Since the diode is fabricated in a n-p^+ junction, the capacitance is given by equation (4-2).

$$C_j = \frac{A}{2}\left[\frac{2q\varepsilon}{V_0 - V} N_d\right]^{1/2} \qquad (4\text{-}2)$$

where

A is area of the junction contact
q is charge of an electron
ε is the permittivity
V_0 is the contact potential of the p - n junction
N_d is the donor concentration in n - well
V is the applied voltage

Since all the parameters listed in equation is not controllable by designer except the junction contact area A, to keep the diode capacitances small, we should use a diode of area as small as possible.

Usually, the size of the diode capacitance calculated by the equation (4-2) is much smaller than the gate capacitance to be seen by the adiabatic clock when the device is switching. We can regard the diode capacitance as negligible when the device is connected with other AqsCMOS logic devices.

4.2.2 Switching device

Let us look at a switching AqsCMOS inverter as shown in Figure 4-8. First of all, we assume all the node are initially biased to constant potentials which can all be considered as AC grounds. Consider the input switch from 1 to 0, the p channel transistor *Mp1* is turned on and the n channel transistor *Mn1* will be turned off. Therefore, the Mp1 can be replaced by a on-resistance and Mn1 is replaced by a open circuit. Also when the adiabatic clock (*aclk*) rise, the diode *D1* is forward biased and the diode D2 is reverse biased. These are equivalence to closing the switch of associated with *D1* and opening the switch associated with *D2*. Then, current will flow from the terminal aclk to the gates of *Mp2* and *Mn2* through *D1* and *Mp1*. Therefore, the circuit shown in Figure 4-8 is redrawn as shown in Figure 4-9.

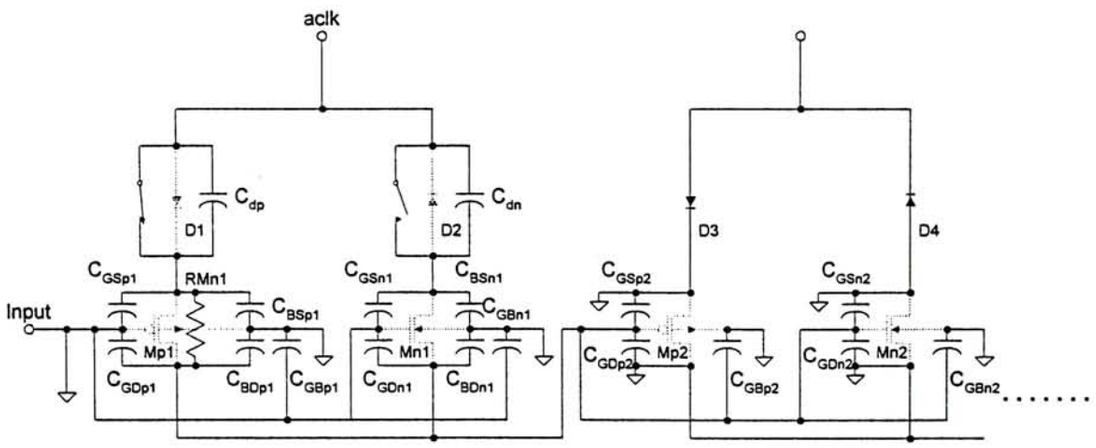


Figure 4-9 Capacitances in a switching AqsCMOS inverter

Following the current path, we can find that *CGBp1* and *CGBn1* can be omitted since they are connect between two grounds. With replacing the semiconductor devices such as diodes and transistors by open circuit, short circuit and on-resistance, we can model the AqsCMOS inverter by a equivalence circuit as shown in Figure 4-10.

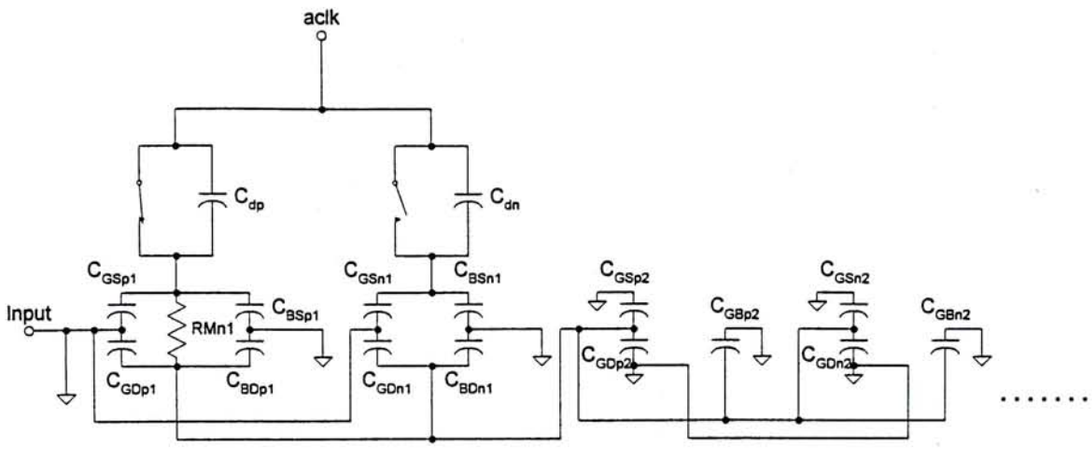


Figure 4-10 An model of an AqsCMOS inverter

We can redraw the model clearly as shown in Figure 4-11 Redrawn model of an AqsCMOS inverter. Since the energy loss to the on-resistance *RMn1* is small, we can replace it by a short current.

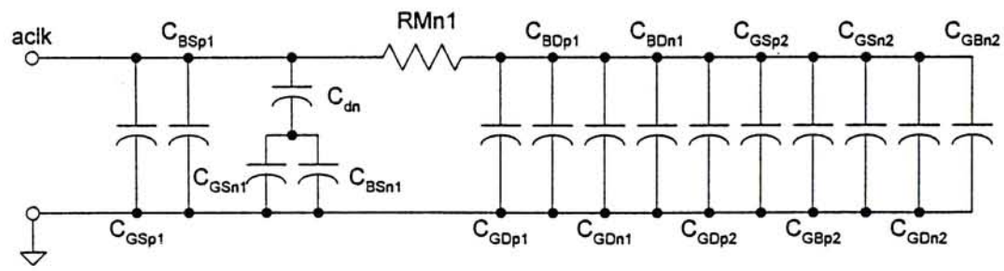


Figure 4-11 Redrawn model of an AqsCMOS inverter

With removing the on-resistance *RMn1*, the model become a pure capacitive network. The capacitance of a switching AqsCMOS inverter as seen by the adiabatic clock input should be given by

$$C_{sw} = C_{GSp1} + C_{BSp1} + [C_{dn} \| (C_{GSn1} + C_{BSn1})] + C_{GDp1} + C_{BDp1} + C_{GDn1} + C_{BDn1} + C_{GDp2} + C_{GSp2} + C_{GBp2} + C_{GDn2} + C_{GSn2} + C_{GBn2} \quad (4\text{-}3)$$

Consider the all the n channel transistors are of the same sizes as well as all p channel transistors. We can simplify the equation (4-3) by letting

$$C_{GSn1} = C_{GSn2} = C_{GSn};$$
$$C_{GDn1} = C_{GDn2} = C_{GDn};$$
$$C_{GSp1} = C_{GSp2} = C_{GSp};$$
$$C_{GDp1} = C_{GDp2} = C_{GDp};$$
$$C_{BSp1} = C_{BSp};$$
$$C_{BDp1} = C_{BDp};$$
$$C_{BSn1} = C_{BSn};$$
$$C_{BDn1} = C_{BDn};$$
$$C_{GBp2} = C_{GBp};$$
$$C_{GBn2} = C_{GBn};$$

The simplified equation is as shown in equation (4-4).

$$C_{sw} = 2C_{GSp} + C_{BSp} + [C_{dn} \| (C_{GSn} + C_{BSn})] + 2C_{GDp} + C_{BDp} + 2C_{GDn} + C_{BDn} + C_{GBp} + C_{GSn} + C_{GBn} \quad (4\text{-}4)$$

4.3 Clocking Scheme

Being illustrated in chapter 3.3.4, the logic aligns to the adiabatic clock edges. If two cascading inverters are connected to the same adiabatic clock, delay will be introduced to the output of the second stage inverter when logic switches. The reason is that the second stage inverter has to wait for the rising or falling edge of the adiabatic clock which is opposite to edge that toggles the output of the first stage inverter (the input of the second stage inverter). For example, if the input of the first stage changes from 0 to 1, the output of the first stage inverter will be toggle to 0 by the falling edge of the adiabatic clock. In the same time the output of second stage inverter should be switched to 0 immediately. However, it is impossible for the second inverter to switch the output logic until the rise edge of the adiabatic clock arrived. This delay will introduce delay or power consumption to the second stage.

The delay can be avoided by introducing the balanced cascading described in chapter 3.3.5.2. Consider an inverter chain with all the odd stages are connected to a positive

adiabatic clock output and the even stages are connected to a negative adiabatic clock output. The positive and negative adiabatic clock output are 180° out of phase. Thus, the outputs of the even stages can be toggled immediately after the odd stages are toggled without waiting for the opposite edge.

This clocking scheme eliminates the raise problem discussed in the pervious section.

If an AqsCMOS circuit is not merely composed of inverters, the clocking scheme is not as simple as we discussed. The circuit designer has to investigate the relations between the input and the output. Theoretically, the circuit designer should keep all the related logic being switched in the same adiabatic clock cycle if possible for speed optimisation.

4.4 Energy Loss of AqsCMOS inverter

Referring to the AqsCMOS inverter built in Figure 4-2, since there is no direct path from the power source to the ground, the short current dissipation (chapter 1.4.2) during switching is zero. This is the same as the original idea of AqsCMOS logic described in chapter 3. The power is still dissipated in the adiabatic inverter by leakage dissipation (chapter 1.4.1), on-resistance of the charging and discharging paths, and the standard voltage drop of diodes.

The on-resistance dissipation in adiabatic logic has been discussed in chapter 2.2.2.2. On-resistance dissipation is not avoidable in all semiconductor switches. In an AqsCMOS inverter, on-resistance will be the on-resistance of the transistors in enabled the charging or discharging paths. Employing adiabatic charging reduces the on-resistance dissipation greatly when compared with conventional charging by equation (2-1). The degree of reduction is controlled by the period of the adiabatic clock signals. Normally the time constant of the semiconductor devices are very small. The period of the adiabatic clock signals will be much larger than the time constant of the devices through the clock is suggested to be ten times faster than the logic.

Since diodes are used in AqsCMOS inverter, there must be a constant voltage drop

equal to diode voltage, V_d, across the diode. If the current pass through the diode is I, the power dissipation by the diodes will be $V_d I$. Note that the power consumption by the diode is not related to the architecture of the diodes but the transistors because the current flowing through the diode is much larger than the transistor as shown in Figure 4-7b. Since the transistors in AqsCMOS, is assumed to be operating in saturation region when switched on. Adjusting the channel widths of the transistors, the charging and discharging currents can be controlled by equation (4-5).

$$I_{DS} = \frac{\mu_n C_{ox} W}{2L}[V_{GS} - V_T]^2 \qquad (4\text{-}5)$$

Normally, about 90% of power dissipation in CMOS circuits goes to load capacitance charging and discharging and direct paths between power supply and ground. AqsCMOS eliminates the direct paths and recycles the charge.

5. ADIABATIC CLOCKS GENERATOR

5.1 Introduction

By the basic principles described in chapter 3, adiabatic quasi-static CMOS logic recover the charge by harmonic motion (adiabatic clocks) across an inductor. In the ideal case, we can use a simple inductor to generator the adiabatic clocks. However, in reality, there is power loss in the inductor, which will cause the harmonic oscillation to stop. In order to keep the oscillation in a stable amplitude, we have to use an active an adiabatic clocks generator.

In the project, three adiabatic clocks generator are proposed.

5.2 Full Adiabatic Clocks Generator

Full adiabatic clock generator or simply adiabatic clock generator[4] is originally introduced by Dickinson and Denker [3]. It is composed of two inverter and one inductor. The design of the generator is shown in Figure 5-1.

The operating principle of full adiabatic clock generator is simple. When the *clk-* signal goes low, inverter composed by *Mn1* and *Mp1* outputs logic 1 when *clk-* goes below the threshold voltage of the inverter. The output of the inverter is connected directly to the *clk+* signal output. The logic 1 pull the *clk-* signal further down to V_{ss}. As a continuous

[4] The adiabatic clock generator is called full adiabatic clock generator for distinguishing it from the half adiabatic clock generator and the automatic adiabatic clock generator which will be discussed in the following sections.

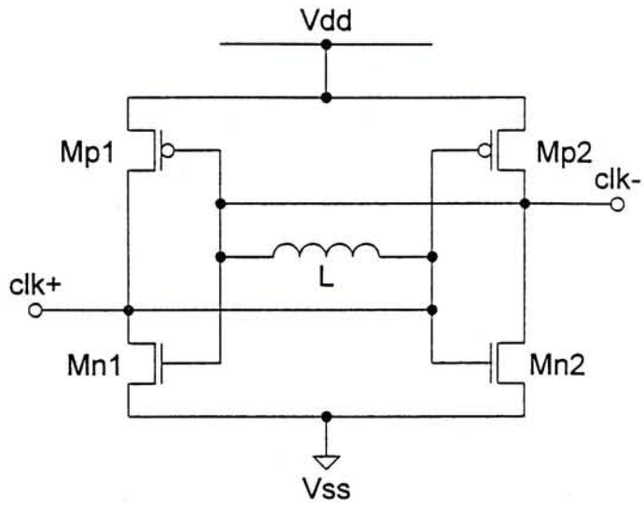


Figure 5-1 Full adiabatic clock generator

operation, the oscillation of clk+ and clk- will be kept to be 180° out of phase and swing between V_{ss} and V_{dd}. This design employed symmetric structure which ensures the symmetry of the adiabatic clock signals.

5.2.1 Sizes of the transistors used

To ensure oscillations between V_{dd} and V_{ss}, the clock generator must be able to give the LC oscillator sufficient energy to be stored in the inductor and the capacitances.

The energy supply to the oscillator is controlled by the channel width to length ratio of the transistors. When the sizes of p channel transistor is large, the current flow from the power source V_{dd} to the oscillator which charge up the selected capacitances is large. Similarly, the n channel transistors are responsible for discharging the selected capacitances. Therefore, the energy passable from the generator to the oscillator every time the inverters switch should not be smaller than the energy loss in the LC oscillator.

If the transistors are not large enough, the oscillator cannot be initialised. The oscillation will then be fail to start. However, if the transistors are too large, the capacitance will be charged up or discharged immediately after the inverters are switched. The fast charging and discharging processes can make the LC oscillation

no longer sinusoidal. The sizes of the transistors should therefore kept small so that the time constant of the charging path or the discharging path should be smaller than the period of the natural frequency of the LC oscillator.

Keeping the sizes of transistors between the first and second criterion is not easy because it is very difficult to calculate the actual energy loss in each LC oscillation and the time constant of charging and discharging paths.

5.2.2 Energy consumption of full adiabatic clocks generator

Since the full adiabatic clocks generator is designed on the basis of inverters energy loss is created when the inverters are switching.

When each of the inverters switches, there will be a direct path created which direct the current from the power source V_{dd} to ground V_{ss} by the adiabatic clock generator. Since the frequencies of adiabatic clock signals is ten times faster than the logic, the direct paths occurs ten times more than a usual CMOS inverter.

Besides, the inverter switches after the clocks go beyond the threshold voltage. The p channel transistor will be kept on when the clock signal is already going down after pass the maximum point. The extra charge acquired from the source will pass through the inductor to the capacitance in the other side of generator. Obviously, in the same time, the n channel transistor in the other side is turned on when the clock signal in the other side is already going up after passing the lowest point. Some of the extra charge will then discharged by the n channel transistor. While the extra charge is acquired from the power source and finally flow into the ground. A energy consumption equal VQ is created.

Energy will be poured into the oscillator though the swing amplitude is large enough. The capacitances will sometimes be connected to V_{dd} or V_{ss} unnecessarily. The extra energy poured will virtually lose by heat through getting extra charge form V_{dd} and discharging them to ground.

The energy being poured into the oscillating system should be the same as the energy loss every time the inverters switch. As discussed in chapter 3.3.3, the energy consumption of each adiabatic clock cycle should be the same if the circuit is large and random enough. The energy acquired from the power source by the adiabatic clock generator should be controlled by the sizes of transistors used. However, from simulations, the energy consumption is found to be varied with the amplitude of the oscillation. In another word, the energy consumption is larger when the oscillation is about to be initialised while it is smaller when the oscillation become steady. The circuit designer simply cannot find the suitable sizes for the transistor used in the clock generator. What the designer can do is finding optimal sizes for the transistor by simulation.

5.3 Half Adiabatic Clocks Generator

Half adiabatic clock generator is shown in Figure 5-2. This circuit compared of one n channel transistor and one p channel transistor and one inductor.

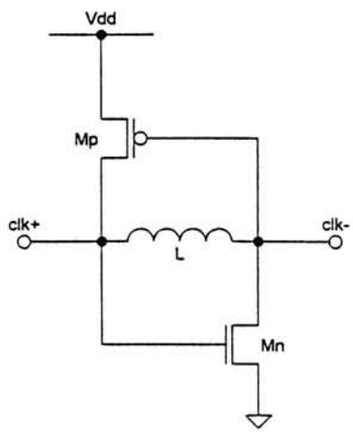


Figure 5-2 Half adiabatic clock generator

Half adiabatic clock generator is an asymmetric circuit. Because of the asymmetric design, the symmetry of the clock signals generated cannot not be guaranteed. Energy will enter the oscillator only when *clk*- goes low and *clk*+ goes high. Compared to full adiabatic

clock generator, frequency of pouring energy into the oscillator is halved.

5.3.1 Transistor sizing

Since the frequency of pouring energy into the system is halved, transistors of larger size must be utilised to give sufficient energy to initialise the oscillation. Similar to the full adiabatic clock generator, the transistor should be large enough to pour an amount of energy into the LC oscillator which is not less than the energy loss between two successive switches. Half adiabatic clock generator also suffers from the same problem as full adiabatic clock generator. It is very difficult to find out the right sizes for the transistors. The easiest way to design is making use of a circuit simulator.

The undesirable high frequency is fifty per cent solved. The high frequency is stopped by the oscillation half cycle that both of the transistors are turned off.

5.3.2 Energy consumption of the half adiabatic clock generator

The main difference between full adiabatic clock generator and half adiabatic clock generator is the elimination of direct path from the power source to the ground. All the energy drawn from the source when the p channel transistor is switched on will be pour into the LC oscillator since there is only one path for the current to flow when the p channel is turned on. Also, half adiabatic clock generator ensures all the charge charged by the n channel transistor comes from the oscillator. Combining the AqsCMOS inverter introduced in chapter 4, all direct paths are eliminated from the logic system.

The energy loss due to turning on the transistors in improper time is not eliminated but reduced. Since the frequency of switching is halved, the frequency of creating energy loss by the improperly turned on transistor is halved.

Simulation results indicate there can be up to 30% of energy save by replacing a full adiabatic clocks generator with a half adiabatic clocks generator.

clock generator, frequency of pouring energy into the oscillator is halved.

5.3.1 Transistor sizing

Since the frequency of pouring energy into the system is halved, transistors of larger size must be utilised to give sufficient energy to initialise the oscillation. Similar to the full adiabatic clock generator, the transistor should be large enough to pour an amount of energy into the LC oscillator which is not less than the energy loss between two successive switches. Half adiabatic clock generator also suffers from the same problem as full adiabatic clock generator. It is very difficult to find out the right sizes for the transistors. The easiest way to design is making use of a circuit simulator.

The undesirable high frequency is fifty per cent solved. The high frequency is stopped by the oscillation half cycle that both of the transistors are turned off.

5.3.2 Energy consumption of the half adiabatic clock generator

The main difference between full adiabatic clock generator and half adiabatic clock generator is the elimination of direct path from the power source to the ground. All the energy drawn from the source when the p channel transistor is switched on will be pour into the LC oscillator since there is only one path for the current to flow when the p channel is turned on. Also, half adiabatic clock generator ensures all the charge charged by the n channel transistor comes from the oscillator. Combining the AqsCMOS inverter introduced in chapter 4, all direct paths are eliminated from the logic system.

The energy loss due to turning on the transistors in improper time is not eliminated but reduced. Since the frequency of switching is halved, the frequency of creating energy loss by the improperly turned on transistor is halved.

Simulation results indicate there can be up to 30% of energy save by replacing a full adiabatic clocks generator with a half adiabatic clocks generator.

5.3.3 Weakness of the half adiabatic clocks generator

The half adiabatic clocks generator eliminates direct path by removing two transistors. But removing these transistor make the design of the generator asymmetric. For example, there is only a p channel transistor connects the *clk*+ pin to V_{dd} and a n channel transistor connects the *clk*- pin to the ground in Figure 5-2. The maximum swing of the *clk*+ is maintained at V_{dd} by the p channel transistor but the minimum swing is not ensured by the switching devices. On the contrary, the *clk*- signal is kept to swing down to the V_{ss} but the maximum swing is unknown. The only way to keep the symmetry is the inductor present between the adiabatic clock output.

The other weakness of the half adiabatic clocks generator is the slow swing recovery when there are some unbalanced switchings occur in two sides of the generator. Since there is only one transistor in each side of the generator, the recovery speed will be slow if the unbalance switchings cause a reduction of clock swing cannot be recovered by the transistor immediately. For example, recovery from the unbalanced switchings which make the adiabatic clock minima rise from V_d is slow because it is done by the n channel transistor in the *clk*- side.

5.4 Automatic Adiabatic Clocks Generator

The direct path problem in a full adiabatic clocks generator is solved by a half adiabatic clocks generator. Yet the asymmetric structure of a half adiabatic clocks generator cannot ensure the generation of symmetric adiabatic clock signals. Reviewing the a full adiabatic clocks generator, the main problems of full adiabatic clocks generator are direct path and energy loss due to oversize transistors. As claimed in chapter 5.2.1, it is possible to find the suitable sizes for the transistors used in all time of operation. One of the cures is introducing feed back system which control the sizes (or effective size) of transistors used based on the status of operation. This is similar to the automobile which adjust the gear ratios in different situations automatically. The generator designed is therefore called automatic adiabatic clocks generator.

5.4.1 Operation of automatic adiabatic clocks generator

The automatic adiabatic clocks generator shown in Figure 5-3 is basically an enhanced full adiabatic clocks generator. *Mp*1, *Mp*2, *Mn*1 and *Mn*2 are transistors of small sizes which form a weak full adiabatic clock generator. Since the sizes of these four transistors are small, the driving ability is limited. Another swing controlling circuit is formed by *Mp*3, *Mp*4, *Mp*5, *Mp*6, *Mn*3, *Mn*4, *Mn*5, and *Mn*6 which are comparatively large in sizes. The p channel transistors *Mp*4 and *Mn*5 and the n channel transistors *Mn*4 and *Mn*5 are switched by the adiabatic clocks as full adiabatic clock generator. The p channel transistor *Mp*3 and *Mp*5 and the n channel transistor *Mn*3 and *Mn*5 are the feed back transistors that control the current flow into the oscillator.

The idea feedback system is simple, consider the peaks and valleys of the adiabatic clock signals can be monitored by four AqsCMOS inverters. For example, the maximum swing of *clk*+ can be monitored by an AqsCMOS inverter of constant

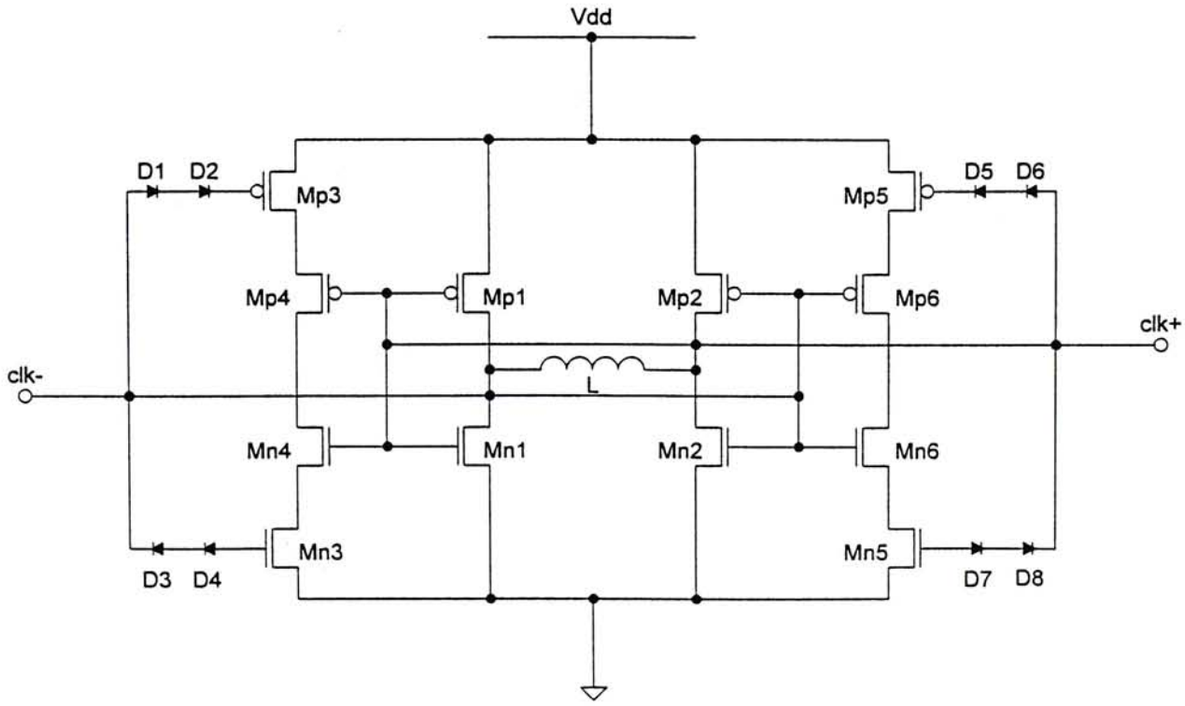


Figure 5-3 Automatic adiabatic clocks generator

input low and powered by *clk+*. The output of the inverter will then be the maximum adiabatic clock peak voltage minus the diode voltage. By feeding the output of the inverter to *Mp*3, *Mp*3 will be turned on if the peak of oscillation is lower than $V_{dd} - V_T$. The drain-source current is inversely related to the output of the inverter since $I_{DS} = \frac{\beta}{2}(V_{GS} - V_T)$. Controlling the current allowance by using different bias current is very similar to adjusting the size of transistor. Similar dynamic effective size adjustment can be done to the rest of three monitors.

Consider the AqsCMOS inverter of constant input acting as monitor. From Figure 4-2, we can simplify the inverter by eliminating the path of the transistor that will not turned on by the constant input. Then we can also replace the transistor that will always be turned on by the input with short circuit. Then we can see the constantly biased inverter can be fully replaced by a diode. Therefore, the diodes *D*1, *D*3, *D*6 and *D*8 are used in Figure 5-3 instead of AqsCMOS inverter for monitoring the oscillation.

If the maximum voltage of the adiabatic clock signal reach $V_{dd} - V_T + V_d$, the p channel transistor controlling P2 or P3 will be fully turned off. Then the peak of selected adiabatic clock will be controlled by the small transistors. The value $V_{dd} - V_T + V_d$ is called threshold peak voltage.

The threshold peak voltage can be adjusted by inserting additional devices into the automatic adiabatic clocks generator. For example, by introducing extra diodes *D*2, *D*4, *D*5 and *D*7 the threshold peak voltage is adjusted to be $V_{dd} - V_T + 2V_d$.

Similarly, threshold valley voltage is the minimum adiabatic clock voltage that turns off *Mn*4 and *Mn*6. When the selected n channel transistor is turned off, the minimum point of adiabatic clock signal will be fully controlled by the small transistors.

By adjusting the threshold peak and trough voltage and the sizes of transistors, we can achieve an automatic adiabatic clock generator of different maximum and minimum energy consumption and symmetric adiabatic clocks swing.

5.4.2 Energy consumption of automatic adiabatic clocks generator

As automatic adiabatic clocks generator is a symmetric design, the problem of direct path illustrated in chapter 5.2.2 is still a problem. This problem is not solved in the design of automatic adiabatic clock generator but suppressed. Since the effective transistor sizes of the current paths are not constants but change as the circuit operate dynamically. When the circuit is operating steadily, the energy required is small and the adiabatic clock swing is large and stable. The effective transistor sizes will be reduced so that the current acquired form the source will therefore reduced also. When the transistors switch, the direct path current will be kept low with the reduced effective transistor sizes.

Reducing the effective transistor sizes also reduce the energy loss due to improperly turned on transistors.

6. EVALUATION

6.1 Introduction

In order to evaluate the functions as well as the performances of the Adiabatic CMOS logic, a lot of simulation are done. Furthermore, two test circuits named "Pendulum" and "Auto-pendulum" were fabricated.

6.2 Simulation Results

6.2.1 Adiabatic clocks generators

In chapter 5, full, half and automatic adiabatic clocks generators are introduced and compared on a theoretical point of view. To obtain more engineering data, such as the strength of the oscillators and the power consumption, they are also simulated.

The three adiabatic clocks generators simulated are similarly configured. The channel width of the p type transistors used in full and half adiabatic clocks generators are both 70μ and that of the n type transistors used are 35μ. Since automatic adiabatic clocks generator connects two transistors in series to perform as a transistor of controllable channel width, the main p type and n type transistors used are 140μ and 70μ respectively. The small transistors used are 10μ (p type) and 5μ (n type). All the generator are used to power a pair of 50pF balanced load and the inductor connected between the load is of inductance 100nH.

By observing Figure 6-1, we can notice that a half adiabatic clock generator need

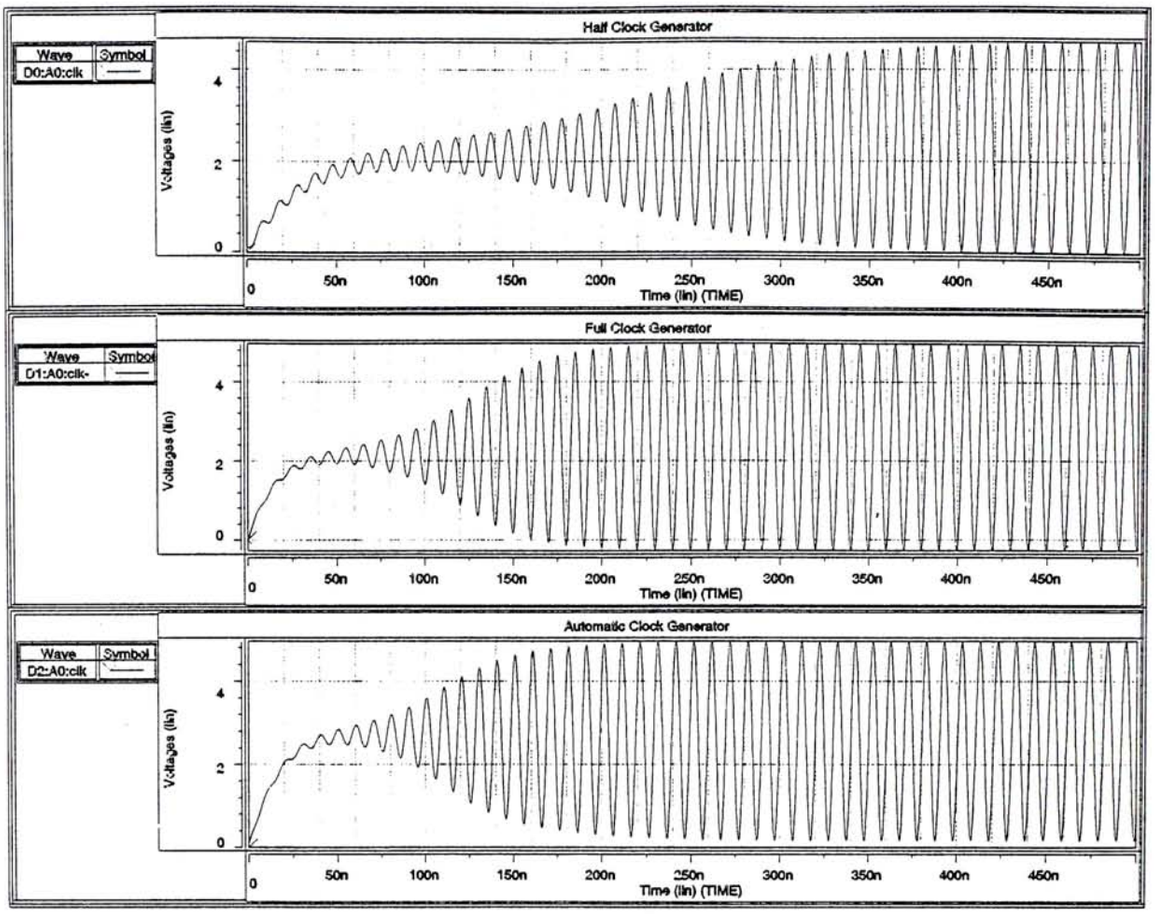


Figure 6-1 Adiabatic clock signals generated by different clocks generators

the longest time to bring the oscillation from its starting state to steady state. The full adiabatic clocks generator reach a steady state significantly faster while the automatic adiabatic clocks generator is the fastest.

This comparison shows that the ability to start an oscillation of different clocks generators. The half adiabatic clocks generator is weakest because it has only one charging and discharging path for the LC oscillator which enhance the oscillation once a period. The full adiabatic clocks and automatic clocks generators both employ two charging and discharging paths in the both sides of the inductor. Also, the amplitude of the sinusoidal waves generated by different clocks generators are different. The weakest half adiabatic clocks generator produce the smallest swing. The peak to peak swing is about 4.5V. The full adiabatic clocks generator produces the largest swing which is higher than V_{dd} and lower than ground. The automatic adiabatic clocks generator keep the swing between V_{dd} and ground of about 4.8V

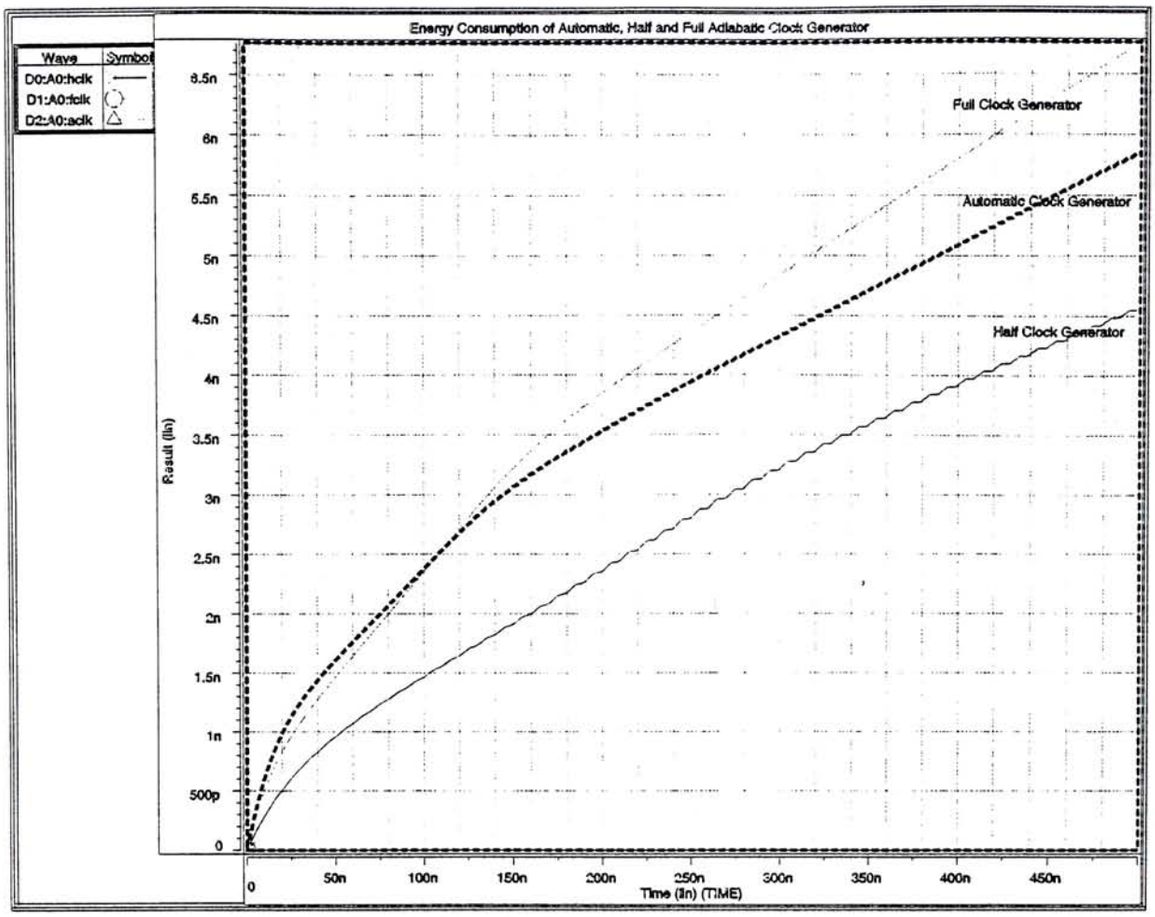


Figure 6-2 Power consumption of different adiabatic clocks generators

peak to peak.

A strong adiabatic clocks generator usually means a large energy loss. When the swing can be started or recovered in a very short time, the adiabatic clocks generator must be able to introduce a lot of extra charge into the oscillation. However, when the oscillation is started in a steady state, the extra charge needed is not as much as a starting or a recovering oscillation. The large amount of extra charge introduced by a strong adiabatic clocks generator become energy loss. Comparing the power consumption of different adiabatic clocks generators, the strongest full adiabatic clocks generator consume the largest amount of power while the weakest half adiabatic clocks generator consume the smallest. The automatic clock generator can significantly reduce the power consumption after the oscillation is started. This is because a feedback system is introduced which reduce the power consumption when the oscillation become steady.

6.2.2 Adiabatic quasi-static CMOS inverters

A 18 stages AqsCMOS inverter chain are simulated in order to evaluated the function and performance of an AqsCMOS logic. The inverter chain is powered by a full adiabatic clocks generator and balanced cascading with the clocking scheme described in chapter 4.3. The size of inductor used is 100nH. The frequency of adiabatic clock is 100MHz. The simulations are done based on the assumption listed below.

1. Assuming that the probabilities of an inverter being turned on and off are equal and equals 0.5. The charges store by the transistors in an inverter chain consists of inverters of equal size should be a constant in the static state.

2. If the number of inverters in the chains are large, the transistors will be in different status at every moment. If a large logic function block is built instead of a inverter chain, the occurrence of switching inside the block can be considered as a random function. In these cases, we can assume the effective load capacitance of the inverter or function block as a constant.

6.2.2.1 Functional evaluation

The input to the AqsCMOS inverter chain is a 1 MHz 1V to 4V square waveform.

From the simulated results, we can see the adiabatic clock output become stable at about 2.0 μs.

The AqsCMOS inverter perform inverting operations properly with logic swing up to 5V. The reason for the logic level beyond V_d and V_{dd} - V_d is that in the reality, the adiabatic clock swing will go beyond V_{dd} and V_{ss} with the switching energy storage devices such as inductors and capacitors. The output maximum voltage will then becomes V_{clk_max} - V_d and the minimum voltage is V_{clk_min} - V_d. The maximum swing of the logic devices can be 0 to

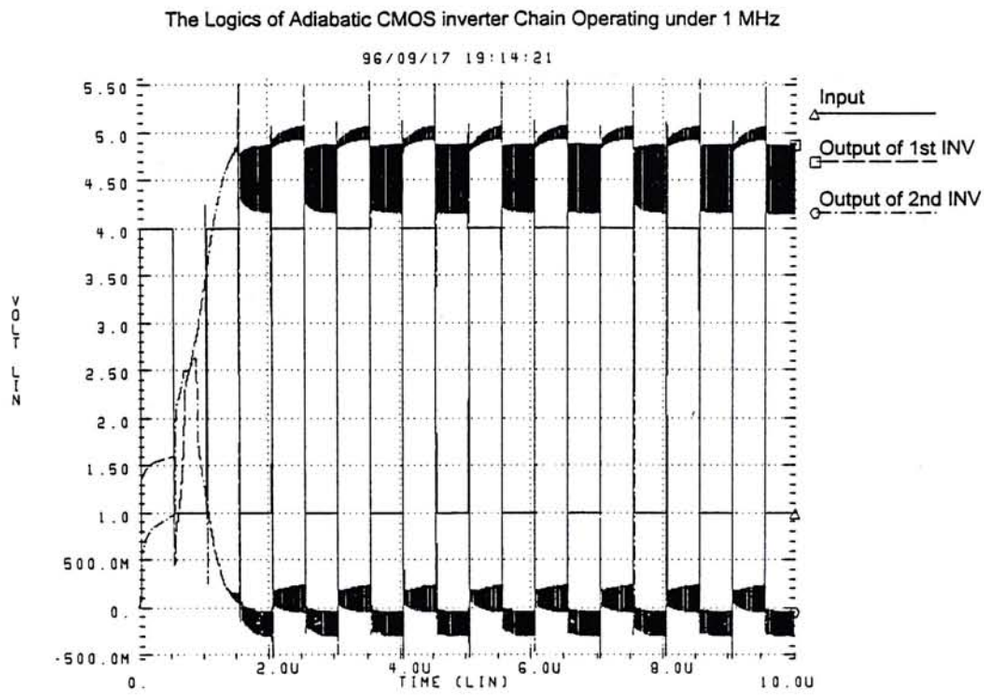


Figure 6-3 Simulation results of AqsCMOS inverter chain operating under 1MHz for functional evaluation

5V.

By using an input waveform swing from 1V to 4V, we can see the AqsCMOS can restore the logic level to 0 to 5V. This shows that the logic levels can be maintained throughout the inverter chain. However, when the logic levels of the input of an AqsCMOS inverter is small, the high frequency noise at the peak and valley of the inverter output will be significant.

When the input frequency in increase to 10MHz, the output waveform is again plotted in Figure 6-4.

When the logic frequency is increased to 10MHz which is about tenth of the frequency of the adiabatic clocks, the logic function is still working properly. Also, the high frequency located in the peak and valley are

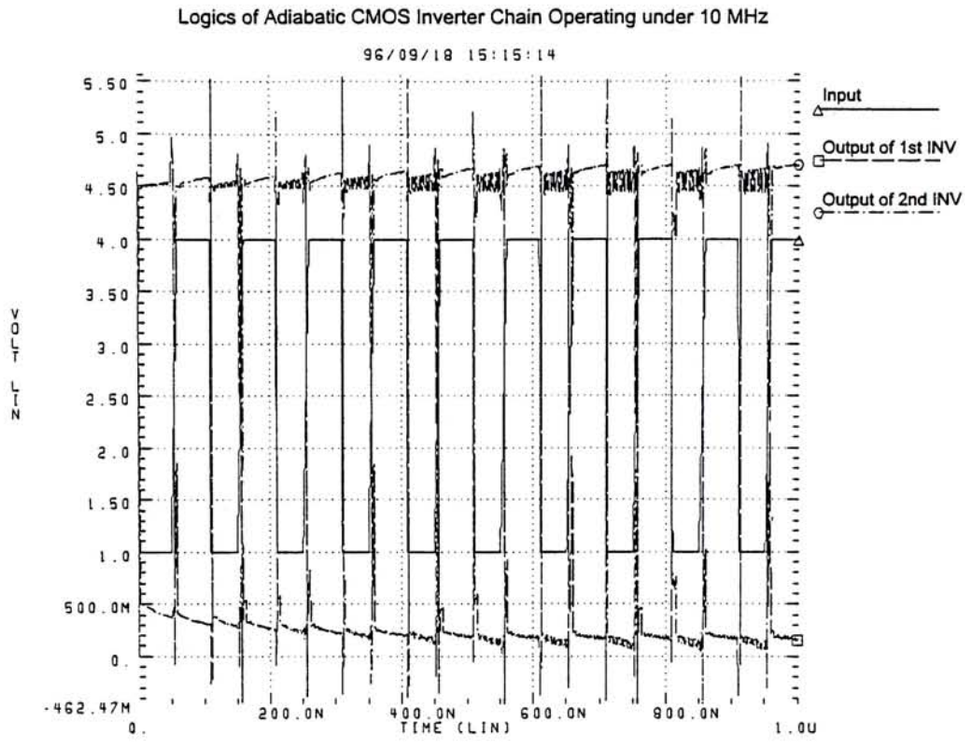


Figure 6-4 Simulation results of AqsCMOS inverter chain operating under 10MHz for functional evaluation

suppressed. Since the logic period decreases, the time for charging and discharging the node is also decreased. The peak and the valley of the output is therefore reduced.

6.2.2.2 Performance evaluation

The power consumption of the AqsCMOS logic devices are measured by plotting the energy consumption as a function of time with the calculation listed below.

The power consumption of the inverter chain simulation by taking the power difference of an adiabatic clocks generator with a fixed capacitive load and the same adiabatic clocks generator with a fixed capacitive load plus a 18-stage AqsCMOS inverter chain.

Energy consumption is plotted by integrating the product of the current flow from the only power supply V_{dd} and the V_{dd}.

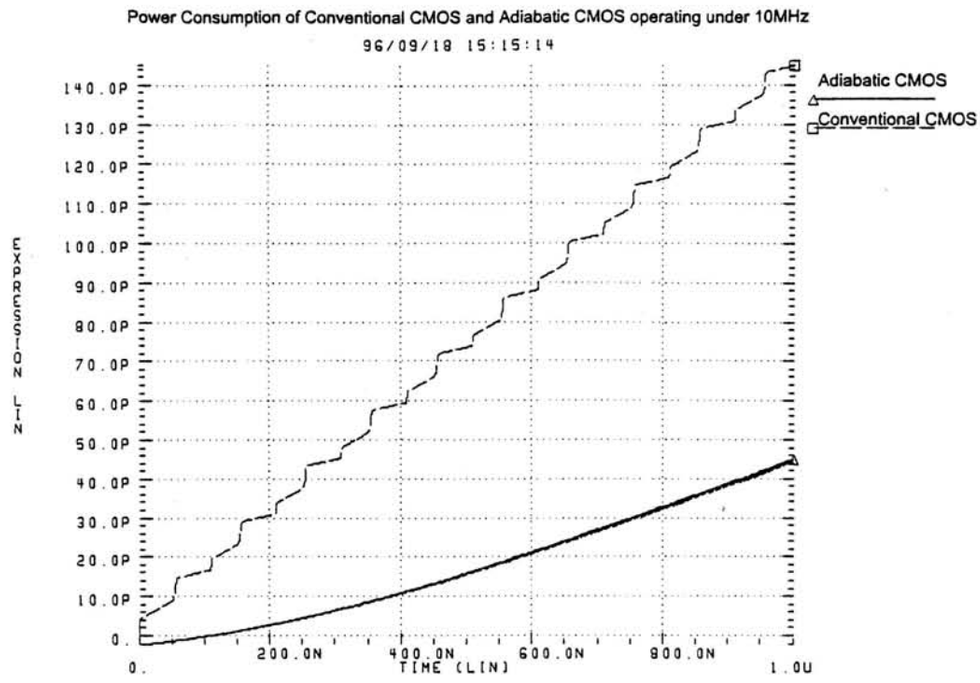


Figure 6-5 Comparison between the power dissipation of AqsCMOS and conventional CMOS inverter chain operating under 10MHz

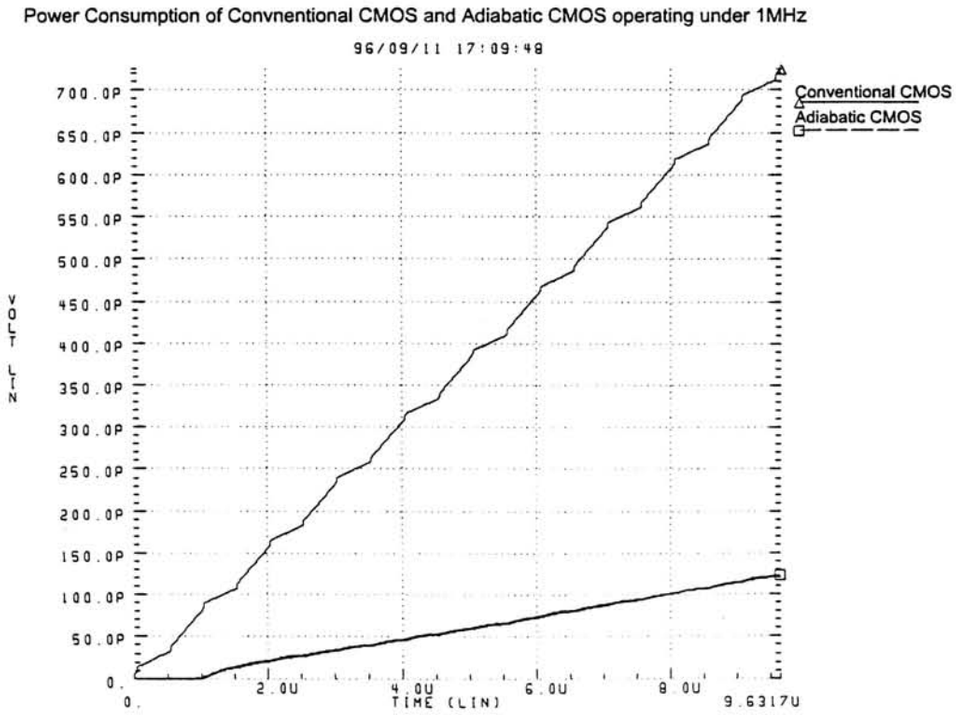


Figure 6-6 Comparison between the power dissipation of AqsCMOS and conventional CMOS inverter chain operating under 1MHz

The comparison between the energy dissipation of an AqsCMOS and a conventional CMOS inverter chains of the same length and same size is shown in Figure 6-6 and Figure 6-5.

By the simulation results, the AqsCMOS can save up to 80% of power when compared with the conventional CMOS.

6.3 Test Circuit - Pendulum

6.3.1 Layout

Pendulum is a 40-pin DIP integrated circuit based on dual layer metal, 1.0 micron, N-well CMOS technology[5].

The test circuit consists of five independent modules sharing the same ground pin (*gnd*).

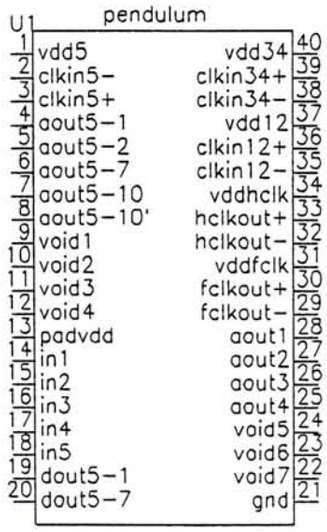


Figure 6-7 Pendulum

[5] The table of pin layout of pendulum can be found in Appendix I.

Pin #	Name	Description
1	vdd5	The power input for the fifth inverter chain (module 5)
2	clkin5-	Negative adiabatic clock input for the fifth inverter chain (module 5)
3	clkin5+	Positive adiabatic clock input for the fifth inverter chain (module 5)
4	aout5-1	Analogue output of the first inverter in the fifth inverter chain (module 5)
5	aout5-2	Analogue output of the second inverter in the fifth inverter chain (module 5)
6	aout5-7	Analogue output of the seventh inverter in the fifth inverter chain (module 5)
7	aout5-10	Analogue output of the tenth inverter in the fifth inverter chain (module 5)
8	aout5-10'	Analogue output of the first repeater in the fifth inverter chain (module 5)
9	void1	Void
10	void2	Void
11	void3	Void
12	void4	Void
13	padvdd	The power input for all pads
14	in1	Input of the first inverter chain (module 3)
15	in2	Input of the second inverter chain (module 3)
16	in3	Input of the third inverter chain (module 4)
17	in4	Input of the fourth inverter chain (module 4)
18	in5	Input of the fifth inverter chain (module 5)
19	dout5-1	Digital output of the first inverter in the fifth inverter chain (module 5)
20	dout5-7	Digital output of the seventh inverter in the fifth inverter chain (module 5)
21	gnd	Ground
22	void7	Void
23	void6	Void
24	void5	Void
25	aout1	Analogue output of the first inverter chain (module 3)
26	aout2	Analogue output of the second inverter chain (module 3)
27	aout3	Analogue output of the third inverter chain (module 4)
28	aout4	Analogue output of the fourth inverter chain (module 4)
29	fclkout-	Negative adiabatic clock output of full adiabatic clock generator (module 1)
30	fclkout+	Positive adiabatic clock output of full adiabatic clock generator (module 1)
31	vddfclk	Power input for full adiabatic clock generator
32	hclkout-	Negative adiabatic clock output of half adiabatic clock generator (module 2)
33	hclkout+	Positive adiabatic clock output of half adiabatic clock generator (module 2)
34	vddhclk	Power input for half adiabatic clock generator (module 2)
35	clkin12-	Negative adiabatic clock input for the first and second inverter chain (module 1)
36	clkin12+	Positive adiabatic clock input for the first and second inverter chain (module 1)
37	vdd12	The power input for the first and second inverter chain (module 1)
38	clkin34-	Negative adiabatic clock input for the third and fourth inverter chain (module 2)
39	clkin34+	Positive adiabatic clock input for the third and fourth inverter chain (module 2)
40	vdd34	The power input for the third and fourth inverter chain (module 2)

Table 1 Table of Pin Layout Pendulum

The module 1 is a full adiabatic clocks generator (fclk) of size 1000/500.

The module 2 is a half adiabatic clocks generator (hclk) of size 1000/500.

The module 3 consists of two inverter chains of size 100/50 (inverter chain 1

and inverter 2) sharing the V_{dd} (*vdd12*), aclk+ (*clkin12+*) and aclk- (*clkin12-*).

The module 4 consists of two inverter chains of size 100/50 (inverter chain 3 and inverter 4) sharing the V_{dd} (*vdd34*), aclk+ (*clkin34+*) and aclk- (*clkin34-*).

The module 5 is one inverter chain of independent V_{dd} (*vdd5*), aclk+ (*clkin5+*) and aclk- (*clkin5-*). Some analogue output pins are placed to examine the analogue output signals of the intermediate adiabatic inverters (*aout5-1*, *aout5-2*, *aout5-7*, *aout5-10 and aout5-10'*).

A pair of conventional inverter of size 10/5 are placed between the 10th and 11th, 20th and 21st, 30th and 31st, 40th and 41st adiabatic inverters in all adiabatic CMOS inverter chains for logic levels enhancement.

6.3.2 Test circuit of pendulum

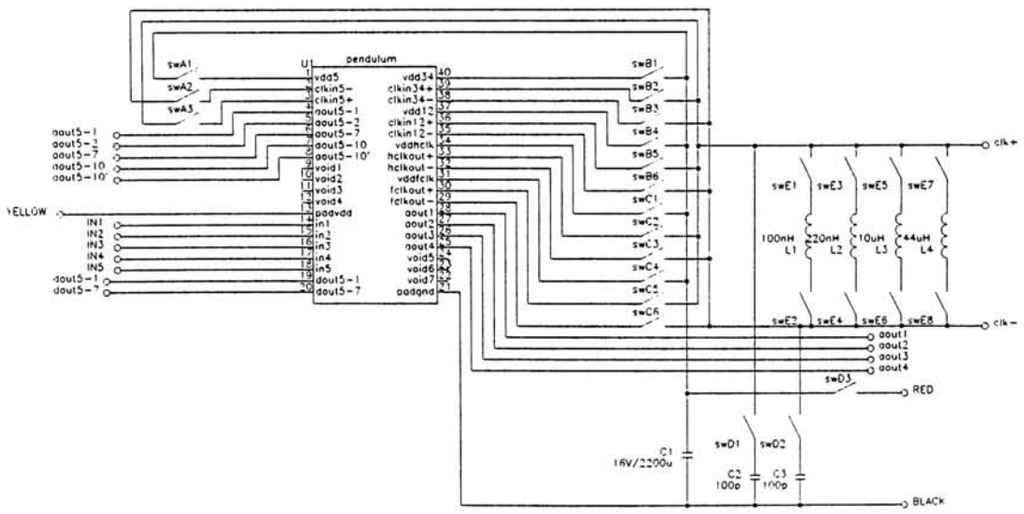


Figure 6-8 The test circuit of pendulum

A test circuit is designed for connection between modules and external capacitors and inductors as shown in Figure 6-8. By opening and closing the different switches, modules and external loads can be enabled or disabled independently. Also the switches allow a variety of inductor to be used.

SwD1 is the ON/OFF switch of the whole circuit. When *swD1* is open, the whole circuit will be separated from the power source. *SwD2* and *swD3* are used to enable and disable the external capacitive loads which simulate the load capacitances of large circuits. The switches *swC1* to *swC6* are responsible to the selection of adiabatic clocks generator. When *swC1* to *swC3* are switched on, the fclk will be connected to the inductor which allows the further connection to the AqsCMOS inverters chains (module 3 to 5). *SwA1* to *swA3*, swB1 to *swB3*, and *swB4* to *swB6* control the connections to the AqsCMOS Inverter chains, the module 5, module 3 and module 4 to the inductor respectively. When either the fclk or the hclk are selected by the switches *swC1* to *swC6*, connecting the enabled Inverter chain to the inductor will also connect the selected clocks generator to those inverter chains.

6.3.3 Module 1 - Full adiabatic clocks generator (fclk)

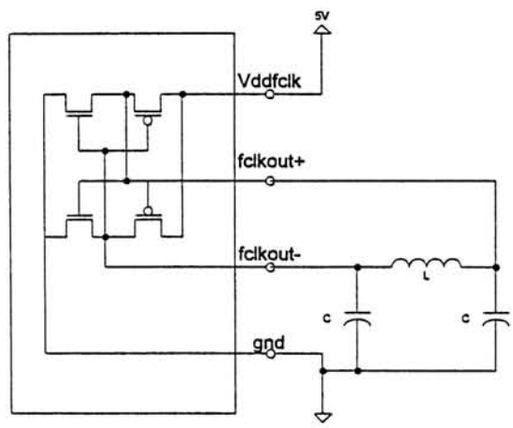


Figure 6-9 Test circuit for full adiabatic clocks generator

By closing the switches *swC4*, *swC5*, *swC6*, *swD1* and *swD2*, a test circuit is setup as shown in Figure 6-9. The output wave from is shown in Figure 6-10.

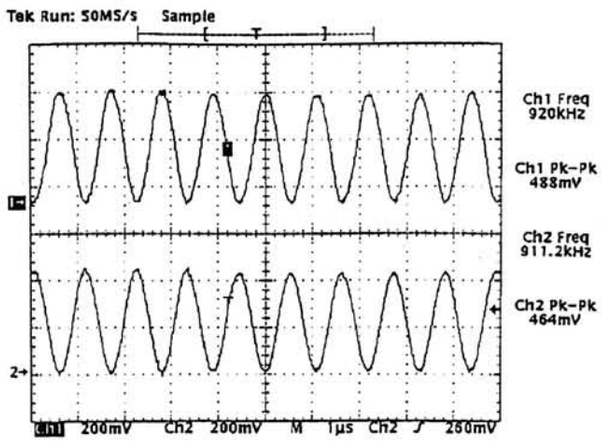


Figure 6-10 Full adiabatic clocks output

As Figure 6-11 shown, there are undesirable high frequencies found whenever the clock signal pass through 2.5V. The reason is when the time constant of the time constant of the charging and discharging paths of the capacitor through the transistors is comparatively smaller than the period of the natural frequency of the LC oscillator. As a result, the charging and discharging processes are not governed by the natural frequency but the time constant.

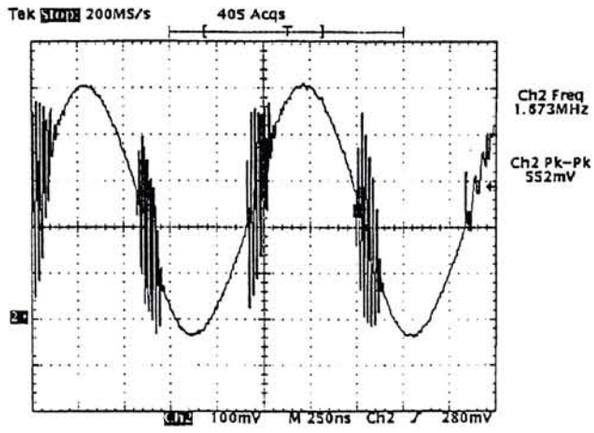


Figure 6-11 Undesirable high frequency

6.3.4 Module 2 - Half adiabatic clocks generator (hclk)

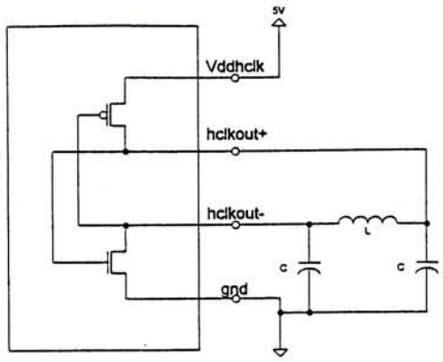


Figure 6-12 Test circuit for half adiabatic clocks generator

The external connection of the test circuit of half adiabatic clocks generator is the same as that of full adiabatic clocks generator as shown in Figure 6-12. The output waveform is shown in Figure 6-13.

Since there are no direct current path between the *Vddhclk* and *gnd*, no undesirable high frequencies are found in the clock outputs. However, the oscillation will not start in hclk without a sufficiently large inductor.

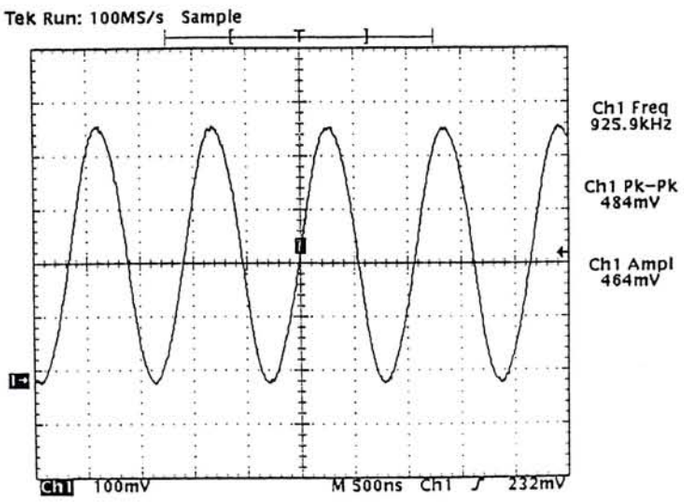


Figure 6-13 Half adiabatic clock output

6.3.5 Module 3 to 5 - Adiabatic inverter chains

6.3.5.1 DC characteristics

The evaluation is divided into four parts.

a. Feeding 0 to *in5*, 5V to *clkin5+*, 0 to *clkin5-* (Table 2)

b. Feeding 5V to *in5*, 0 to *clkin5+*, 5V to *clkin5-* (Table 3)

In all the evaluation listed above, signals from *aout5-1*, *aout5-2*, *aout5-7*, *aout5-10*, *aout5-10'*, *dout5-1* and *dout5-7* are recorded.

	Aout5-1		aout5-2		aout5-7		aout5-10		aout5-10'		dout5-1		dout5-7	
Clip #	max.	min.	max.	min.	Max.	min.	max.	min.	max.	min.	max.	min.	max.	min.
1	4.27V	4.15V	65mV	-95mV	4.19V	4.03V	65mV	-95mV	105mV	-55mV	65mV	-55mV	65mV	-55mV
2	4.27	4.15	65m	-55m	4.15	4.03	65m	-55m	65m	-55m	65m	-55m	65m	-55m
3	4.31	4.19	65m	-55m	4.19	4.07	65m	-55m	105m	-55m	65m	-55m	65m	-55m
4	4.31	4.15	65m	-95m	4.19	4.03	65m	-95m	65m	-55m	65m	-55m	65m	-95m
5	4.27	4.15	65m	-95m	4.19	4.03	65m	-95m	65m	-55m	65m	-95m	65m	-95m
6	4.27	4.11	65m	-95m	4.19	4.03	65m	-95m	65m	-55m	65m	-95m	65m	-95m
7	4.27	4.15	65m	-95m	4.19	4.03	65m	-95m	65m	-55m	65m	-95m	65m	-95m
8	4.27	4.11	65m	-95m	4.15	4.03	65m	-95m	65m	-55m	65m	-95m	65m	-95m
9	4.27	4.11	65m	-95m	4.19	4.03	65m	-95m	65m	-55m	65m	-95m	65m	-95m
10	4.27	4.15	65m	-95m	4.19	4.03	65m	-95m	65m	-55m	65m	-95m	65m	-95m

Table 2 Test on passing 0 to an adiabatic inverter chain with DC aclk

	aout5-1		aout5-2		aout5-7		aout5-10		aout5-10'		dout5-1		dout5-7	
Clip #	max.	min.	max.	min.	Max.	min.	max.	min.	max.	min.	max.	min.	max.	min.
1	65mV	-95mV	4.31V	4.15V	65mV	-95mV	4.15V	4.03V	5.07V	4.95V	5.07V	4.95V	5.07V	4.95V
2	65m	-95m	4.31	4.15	65m	-95m	4.15	4.03	5.07	4.95	5.07	4.95	5.07	4.95
3	65m	-95m	4.31	4.15	65m	-95m	4.15	4.03	5.07	4.95	5.07	4.95	5.07	4.95
4	65m	-55m	4.31	4.11	65m	-55m	4.15	4.03	5.07	4.95	5.07	4.95	5.07	4.95
5	65m	-95m	4.31	4.15	65m	-95m	4.15	4.03	5.07	4.95	5.07	4.95	5.07	4.95
6	65m	-95m	4.31	4.15	65m	-95m	4.15	4.03	5.07	4.95	5.07	4.95	5.07	4.95
7	65m	-95m	4.31	4.11	65m	-55m	4.15	4.03	5.07	4.95	5.07	4.95	5.07	4.95
8	65m	-55m	4.31	4.15	65m	-55m	4.15	4.03	5.07	4.95	5.07	4.95	5.07	4.95
9	65m	-95m	4.31	4.15	65m	-95m	4.15	4.03	5.07	4.95	5.07	4.95	5.07	4.95
10	65m	-95m	4.31	4.15	65m	-95m	4.15	4.03	5.07	4.91	5.07	4.91	5.07	4.95

Table 3 Test on passing 5V to an adiabatic inverter chain with DC aclk

6.3.5.2 AC characteristics

By the assumption stated in Chapter 3.3.3, we can simulate a very large logic circuit by using simply a pair of capacitor connected to aclk+ and aclk- of the adiabatic clocks generator. Therefore, in order to evaluate the operation of adiabatic inverters inside a large circuit system, the module 2 (hclk), module 5 (inverter chain 5) and the external loads (2 10nF capacitors) are enabled by *swA1*, *swA2*, *swA3*, *swC1*, *swC2*, *swC3*, *swD1*, *swD2*.

By selecting L = 5.6μH, the output frequency of the adiabatic clocks generator is about 900kHz.

As proposed in Chapter 4.3, the logic frequency should be about 1/10 of that of the adiabatic clock. Thus the input frequency is selected to be 101kHz. Figure 6-14 to Figure 6-18 reveal the output of *aout5-1* to *aout5-10'* and Figure 6-19 and Figure 6-20 reveal the output of *dout5-1* and *dount5-7*.

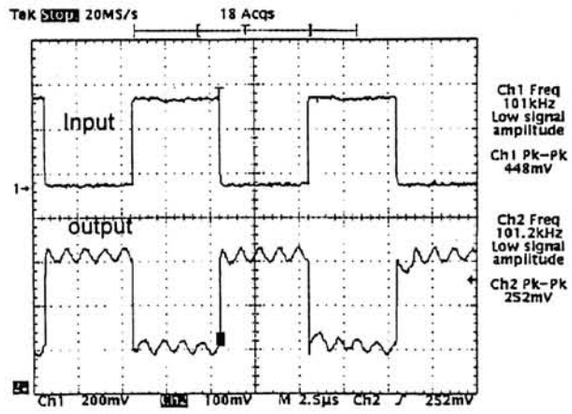


Figure 6-14 Input and analogue output of the first inverter

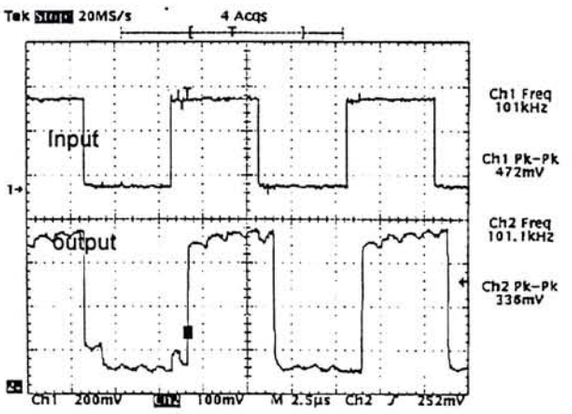


Figure 6-15 Input and analogue output of the second inverter

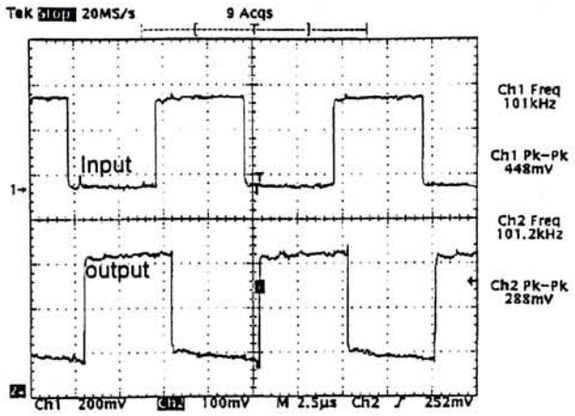


Figure 6-16 Input and analogue output of the seventh inverter

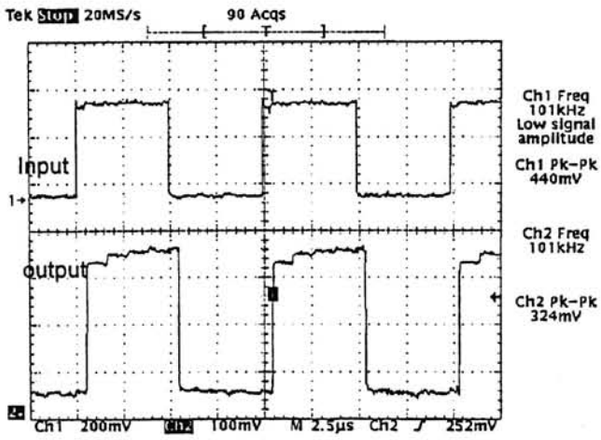


Figure 6-17 Input and analogue output of the tenth inverter

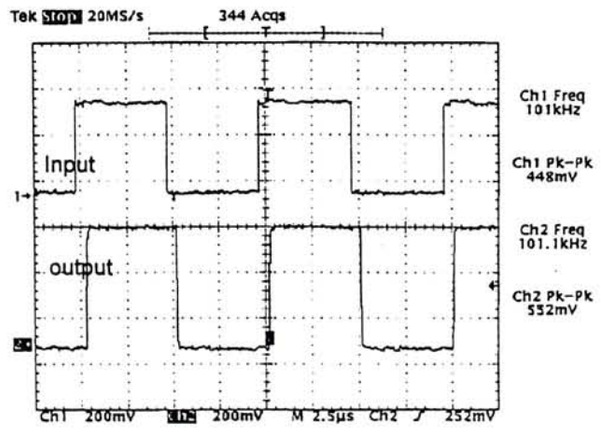


Figure 6-18 Input and analogue output of the repeater after the tenth inverter

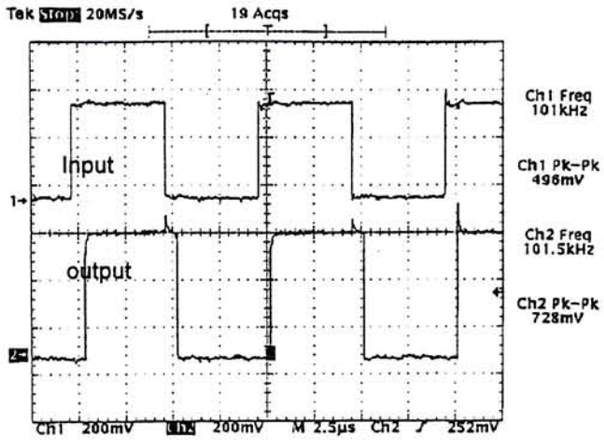


Figure 6-19 Input and digital output of the first inverter

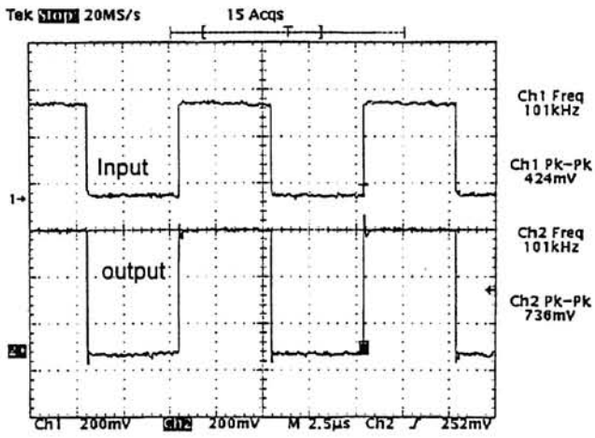


Figure 6-20 Input and digital output of the seventh inverter

6.3.6 Power dissipation

Measuring power of a CMOS circuit is difficult as the power consumption is too small. The easiest way to measure the power dissipation is using a small resistor to connected between the power source output and the Vdd input of the circuit to be measure to extract the current flow from the source. As the power consumption of CMOS circuit is small, the resistance of the Vdd terminal can be several megaohms. The potential different between the terminals of the resistor will be the product of voltage supply and size of resistor. By measuring the potential difference, we can find out the current flow from the source and then the power consumption can calculated.

Since the size of inverter chain is not large, we cannot measure the power dissipation of the AqsCMOS inverter chain directly because of the assumption stated in chapter 3.3.3. A possible method to find out the power consumption of the relatively small circuit is measuring the power consumption difference between a system that connects adiabatic clock generator, inverters and a pair of large constant capacitive loads, and a same system without adiabatic chain. However, since power consumption of the adiabatic inverter chain is very small, the difference between the two systems are not distinguishable by the measuring instrument. An indirect measurement is done to find out the possible energy save of employing AqsCMOS system instead of the energy consumption of the inverter chain.

Consider a pair of large capacitive load of equal sizes are connected to the positive and negative adiabatic clock respectively. When an AqsCMOS inverter chain of balanced cascading with clocking scheme described in chapter 4.3 is also connected to the adiabatic clocks and running under a selected logic frequency, we can say the power dissipation of the inverter chain is negligible. By comparing the power dissipation of the conventional CMOS logic of loading equal to the size of the large capacitive load used and the power dissipation of the AqsCMOS system, we can compare the power consumption of an AqsCMOS inverter chain and conventional logic system.

The sizes of capacitors used are both 10nF and the resistance used to measure the current is 10Ω to compensate the ×10 probe reading. If the logic running is 101kHz, the current drawn from the power source by the conventional CMOS should be $CVf = 20n \times 5 \times 101k = 10.1mA$.

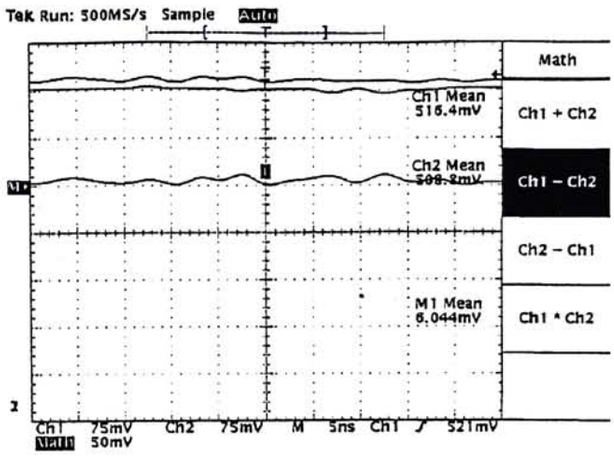


Figure 6-21 Current measure of AqsCMOS logic

By the reading of channel 1 - channel 2, we find the current flow from the source is 6.044mA. Thus, we can prove the power consumption of AqsCMOS is less than conventional CMOS. However, this method is a rough comparison of the two circuits. At this stay, we can only quantitatively prove that the power consumption of AqsCMOS is better.

7. CONCLUSIONS

7.1 Introduction

This chapter conclude the thesis in terms of design, function, and power dissipation. By the end of the chapter, discussion and future possible development can be found.

7.2 Design

In the thesis, a new type of quasi-static logic, Adiabatic Quasi-static CMOS (AqsCMOS) logic, is proposed.

7.2.1 Adiabatic quasi-static CMOS logic

The AqsCMOS logic is designed based on a simple electric pendulum. When a LC oscillator start oscillation, the capacitor will be periodically charge up and discharged without using energy. In electronics, charging and discharging can be used to represent logic level 0 and 1.

Using switches to control the charging and discharging processes, we can control the charging and discharging processes. However, the control signals of the switches do not have any logic relation with the status of the capacitors. This can be solved by introduction the current direction control device. By the current direction control device, logic block can be built.

By introducing the concept of effective capacitance, adiabatic clocks and so on,

a large AqsCMOS system can be built. When the adiabatic clock is sufficiently faster than the logic, the logic can be switched almost randomly. It is therefore compatible to the conventional CMOS logic, which means AqsCMOS logic can drive and can be driven by conventional logic device directly.

7.2.2 Adiabatic quasi-static CMOS inverters

The basic building block of AqsCMOS logic is an inverter (Figure 4-2). The inverter is basically the realisation of the current direction control device which consist of a n channel, a p channel transistor and two diodes. The mean function of the diodes is to keep the load from being charged or discharged.

Assume that the AqsCMOS inverter is powered by a sinusoidal signal. If a logic 0 is applied to the input, the p channel transistor turns on during the negative cycle of the adiabatic clock and charge the load capacitance to one diode drop below the peak of adiabatic clocks. The diode clamp the load voltage at the previously charged state until the input switch and the n channel turns on. Conversely, the of input switch to 1 and the p channel transistor turns off. The load capacitance is discharged by the n channel transistor and the potential is kept by another diode.

AqsCMOS is readily cascadable. Cascading AqsCMOS need no circuit modification. To optimise the speed, it is suggested to power the inverter by two adiabatic clocks alternatively.

7.2.3 Adiabatic clocks generator

Three adiabatic clocks generator are introduced. They are full, half, and automatic adiabatic clocks generator. The full adiabatic clock generator and automatic employ symmetric circuit design which guarantee the symmetry of adiabatic clock generated. However, they both suffer form the direct path problem which consumption power. The automatic clocks generator make use of negative feedback system that control the effective transistor size to suppress the unnecessary power loss. Half adiabatic clocks generator cannot guarantee the symmetry of generated signal while the circuit

is asymmetric. Yet direct path problem is totally eliminated.

7.3 Function

By simulations results and the test results of the test clip - Pendulum, the AqsCMOS is proven to be functional. In the simulation, the system can run up to 15MHz

7.4 Power Dissipation

By simulation results and the actual test result, the AqsCMOS system can save up to 40% of power.

7.5 Discussion

The main reason for developing AqsCMOS is to save energy consumption by adiabatic charging and charge recovery technique. It is interesting to point out that, the power consumption in AqsCMOS is not dissipated to the actual logic devices but the adiabatic clock. The efficiency of the adiabatic clock is important because adiabatic clock will operate in the speed ten times faster than the logic. So far, only the automatic clock generator is designed to improve the efficiency adiabatic clock generator. The author believe that design of adiabatic clock generator will be a important topic if AqsCMOS is going to be further developed.

7.6 Further Development

In the thesis only inverter is developed. There are a lot of problem to solve when jumping from inverter to other logic building blocks. For example, clocking scheme and load balancing in two sides of adiabatic clock generator.

The adiabatic clock generator is another part of the project to be further developed. As state in chapter 7.5, the adiabatic clock generator control the degree of power saving. The

efficiency of all the clock generator designed is still losing energy in different ways. Using feedback system seem to be able to suppress the unnecessary power loss. It is worth to investigate the feedback system and maybe a better adiabatic clock generator can be developed.

The energy loss and a lot of physical properties of AqsCMOS logic is not yet studied because it is not the main point of the thesis. However, the author believe that studying the logic thoroughly is necessary before the logic can be mature.

7.7 Conclusion

Adiabatic quasi-static CMOS logic is developed and tested. It is compatible to the conventional CMOS and readily cascadable. The test results show the AqsCMOS can save power up to 40% when compared with conventional CMOS.

8. REFERENCES

[1] S. G. Younis and T. F. Knight, "Practical implementation of charge recovering asymptotically zero power CMOS," in Research on Integrated Systems: Proc. 1993 Symp. Cambridge, pp. 234-250, MA: M.I.T. Press, 1993.

[2] R. C. Merkle, "Reversible electronic logic using switches," in Nanotechnolgy, VOL. 4, pp. 21-40, 1993

[3] Alex G. Dickinson and John S. Denker, "Adiabatic Dynamic Logic," in IEEE Journal of Solid State Circuit, VOL. 30, No. 3, pp. 311-315, March 1995.

[4] W. Y. Wang and K. T. Lau, "Adiabatic Pseudo-domino Logic," in Electronic Letters, VOL. 31, No. 23, pp. 1982-1983, November 1995.

[5] Charkes H. Bennett, "Notes on the history of reversible computation," in IBM Journal of Research and Development, VOL. 32, No. 1, pp. 16-23, January 1988.

[6] J. C. Maxwell, "Theory of Heat," 4th Edition, Longmans, Green and Co., London, 1875 (1st Edition, 1871), pp. 328-329.

[7] Fredkin, E. and Toffoli, T., "Design principles for achieving high performance submicron digital technologies," in Proposal to DARPA, MIT Laboratory of Computer Science.

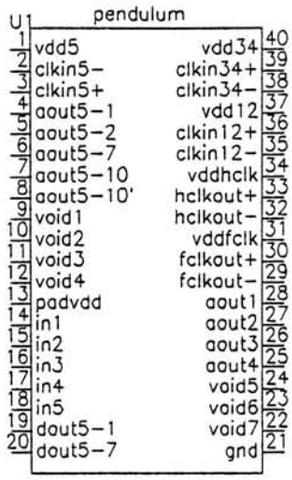
[8] W. C. Athas, J. C. Koller, L. J. Svensson, "An energy-efficient CMOS line driver using adiabatic switching," Inform. Sci. Inst., CA, Tech. Rep. ACMOS-TR-2, July 1993.

[9] W. Y. Wang and K. T. Lau, "Adiabatic pseudo-domino logic," in Electronics Letters, VOL. 31, No. 23, pp. 1982-1983, November 1995.

[10] D. Meteo and A. Rubio, "Quasi-adiabatic ternary CMOS logic," in Electronics Letters, VOL. 32, No.2, pp 99-101, January 1996.

[11] Yong Moon, Deog-Kyoon Jeong, "An efficient charge recovery logic circuit," in IEICE Transactions in Electronics, VOL. E79-C, No. 7, July 1996.

APPENDIX I TABLE OF PIN LAYOUT PENDULUM



Pin #	Name	Description
1	vdd5	The power input for the fifth inverter chain (module 5)
2	clkin5-	Negative adiabatic clock input for the fifth inverter chain (module 5)
3	clkin5+	Positive adiabatic clock input for the fifth inverter chain (module 5)
4	aout5-1	Analogue output of the first inverter in the fifth inverter chain (module 5)
5	aout5-2	Analogue output of the second inverter in the fifth inverter chain (module 5)
6	aout5-7	Analogue output of the seventh inverter in the fifth inverter chain (module 5)
7	aout5-10	Analogue output of the tenth inverter in the fifth inverter chain (module 5)
8	aout5-10'	Analogue output of the first repeater in the fifth inverter chain (module 5)
9	void1	Void
10	void2	Void
11	void3	Void
12	void4	Void
13	padvdd	The power input for all pads
14	in1	Input of the first inverter chain (module 3)
15	in2	Input of the second inverter chain (module 3)
16	in3	Input of the third inverter chain (module 4)
17	in4	Input of the fourth inverter chain (module 4)
18	in5	Input of the fifth inverter chain (module 5)
19	dout5-1	Digital output of the first inverter in the fifth inverter chain (module 5)
20	dout5-7	Digital output of the seventh inverter in the fifth inverter chain (module 5)
21	gnd	Ground
22	void7	Void
23	void6	Void
24	void5	Void
25	aout1	Analogue output of the first inverter chain (module 3)
26	aout2	Analogue output of the second inverter chain (module 3)
27	aout3	Analogue output of the third inverter chain (module 4)
28	aout4	Analogue output of the fourth inverter chain (module 4)
29	fclkout-	Negative adiabatic clock output of full adiabatic clock generator (module 1)
30	fclkout+	Positive adiabatic clock output of full adiabatic clock generator (module 1)
31	vddfclk	Power input for full adiabatic clock generator
32	hclkout-	Negative adiabatic clock output of half adiabatic clock generator (module 2)

33	hclkout+	Positive adiabatic clock output of half adiabatic clock generator (module 2)
34	vddhclk	Power input for half adiabatic clock generator (module 2)
35	clkin12-	Negative adiabatic clock input for the first and second inverter chain (module 1)
36	clkin12+	Positive adiabatic clock input for the first and second inverter chain (module 1)
37	vdd12	The power input for the first and second inverter chain (module 1)
38	clkin34-	Negative adiabatic clock input for the third and fourth inverter chain (module 2)
39	clkin34+	Positive adiabatic clock input for the third and fourth inverter chain (module 2)
40	vdd34	The power input for the third and fourth inverter chain (module 2)

Table 4 Table of Pin Layout Pendulum

APPENDIX II PHOTOGRAPHS OF PENDULUM

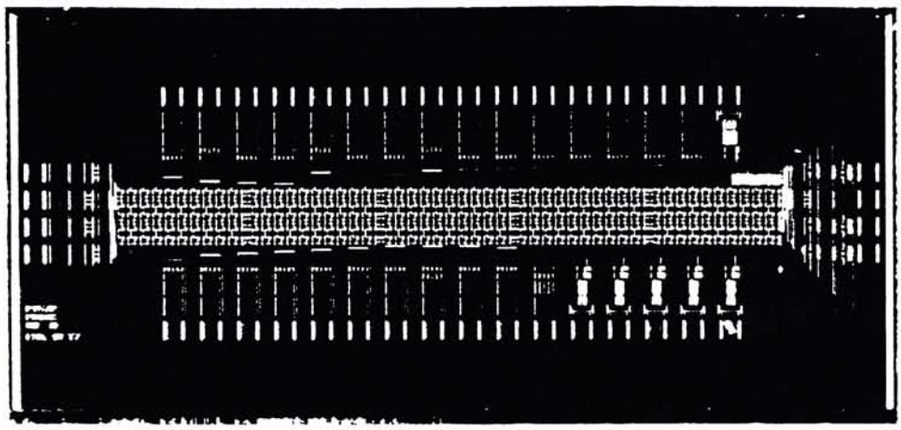


Figure II-1 Overview of Pendulum

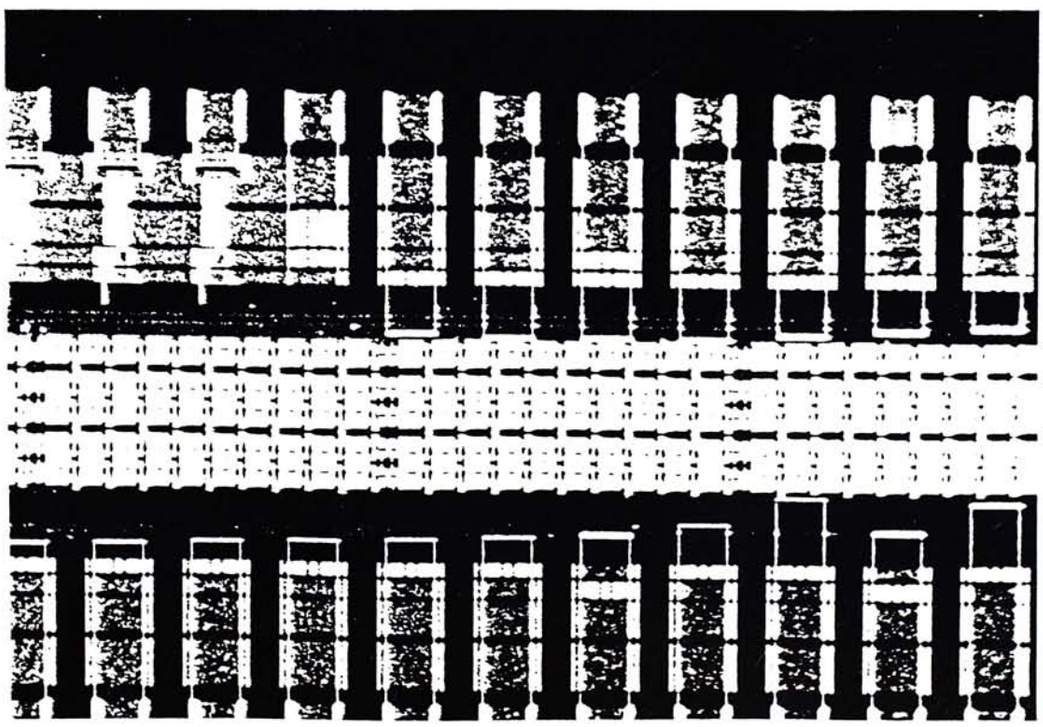


Figure II-2 AqsCMOS inverters