

CMOS Dual-modulus Prescaler Design for RF Frequency Synthesizer Applications

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in
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In the design of phase-locked loop (PLL) frequency synthesizer, a dual-modulus prescaler (DMP) is required to provide two consecutive dividing ratios. The prescaler is known to be one of the most challenging sub-circuits in PLL because it operates at the highest frequency and can consume much power. Moreover, PLL is basically a mixed-signal system and great care has to be taken to reduce the coupling of switching noise from the digital circuitry to the sensitive analog devices, such as voltage-control oscillator (VCO) and charge pump (CP), via the supply lines and substrate. One major concern is the switching noise introduced by the DMP. In this thesis, the design and implementation of three different DMP topologies are presented.

For the first DMP, a new approach based on the source coupling logic (SCL) and pre-processing clock technique in a differential mode is proposed. Besides of high speed performance, this structure also exhibits relatively constant supply current with reduced switching noise, which is beneficial to PLL operation. The design was fabricated using AMS 0.35 μ m double-poly three-metal standard CMOS process. The chip occupies an active area of approximately $220\mu\text{m} \times 130\mu\text{m}$. At a supply voltage of 3V, current consumption was found to be roughly 4mA at an input frequency of 960MHz. Its maximum operating frequency was about 1.1GHz.

In the second design, a DMP based on the phase-switching technique was

implemented for low power applications. Ultra low power consumption is achieved by using a single delay flip-flop (DFF) in the front-end divide-by-4 and to eliminate the power-hungry synchronizing circuits in solving the glitch problem. The design was fabricated using AMS 0.35 μm double-poly four-metal standard CMOS process with an active size of approximately 200 μm \times 80 μm and is measured to operate from 2.08 to 2.66GHz at 1.5V supply voltage. The experimental circuit was found to have a power consumption of less than 1mW.

In the final design, a DMP with wider frequency range is proposed to accommodate process variations. In this configuration, two divide-by-2 stages are combined to realize a broadband front-end divide-by-4 circuit. For further speed enhancement, proper circuit technique is also applied to reduce the load capacitance at critical output nodes. The design was fabricated using AMS 0.35 μm double-poly four-metal standard CMOS process with an active size of approximately 186 μm \times 65 μm . It was measured to operate from 1.98 to 2.88GHz at 1.5V supply voltage. The experimental circuit was found to have a power consumption of 1.02mW.

摘要

在鎖相迴路頻率合成器中，雙模數預置分頻器用作提供兩個連續的分頻模數。由於雙模數預置分頻器工作於整個鎖相迴路頻率合成器中最高的頻率，而它的功率消耗亦很高，使它成為整個鎖相迴路設計中最具挑戰的子電路之一。此外，鎖相迴路頻率合成器基本上是一個混模訊號系統。故須要特別注意數位電路所產生的開關雜訊透過電源線耦合到較敏感的類比電路，例如壓控振盪器和電荷充電泵。而雙模數預置所產生開關雜訊亦是值得關注的問題。在這篇論文裏，介紹了三個雙模數預置分頻器的設計和實現。

第一個雙模數預置分頻器的設計，是運用了源極耦合邏輯與差模架構的優先處理脈波技術。除了高速度的表現外，這種電路的結構展示出較穩定的電源電流和較少開關雜訊。這個電路以 AMS 0.35 μm 標準 CMOS 製程製造。晶片的佈局面積約 220 μm \times 130 μm 。在 3V 的供應電壓下，工作於 960MHz 輸入頻率的電流消耗為 4mA。而最高的工作頻率約 1.1GHz。

第二個電路則運用了相位轉移技術。由於建議電路中四分頻器只利用了一個延遲正反器實現，而脈衝的問題亦不需運用高功率消耗的同步電路去解決，故達到低功率消耗的表現。這個建議電路同樣以 AMS 0.35 μm 標準 CMOS 製程製造。晶片核心的佈局面積約 200 μm \times 80 μm 。在 1.5V 的供應電壓下，電路的工作頻率範圍為 2.08 至 2.66GHz。實驗結果顯示，電路的功率消耗少於 1mW。

第三個建議設計為一個工作頻率範圍較闊的雙模數預置分頻器。這個電路利用了兩個二分頻器來取代第二個建議電路中的四分頻器。為達到更高工作頻率，這電路亦應用了新的技巧來減少全速二分頻器的輸出電容。這個電路以 AMS 0.35 μm 標準 CMOS 製程製造。晶片的佈局面積約 186 μm \times 65 μm 。在 1.5V 的供應電壓下，電路的工作頻率範圍為 1.98 至 2.88GHz。實驗結果顯示，電路的功率消耗為 1.02mW。

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Chapter 1

Introduction

1.1 Motivation

Wireless applications are gaining popularity. Frequency synthesizer is one of the major components in transceiver design. High frequency synthesizer is usually implemented by using PLL to compensate for the frequency drift versus time and temperature in VCO.

The integer-N architecture (Figure 1.1) is the simplest form of PLL-based synthesizer. It consists of a voltage-controlled oscillator (VCO), a phase frequency detector (PFD), a charge pump (CP), a low-pass loop filter (LPF) and an integer-N divider. The feedback loop ensures that once the system is locked, the output frequency of PLL is set to be a multiple of the reference frequency in most PLL systems crystals are commonly used to generate the reference, due to their excellent purity and stability.

The output frequency, therefore, can be varied by simply modifying the value of N . Since N is an integer, it is necessary that the reference frequency equals to the channel spacing.

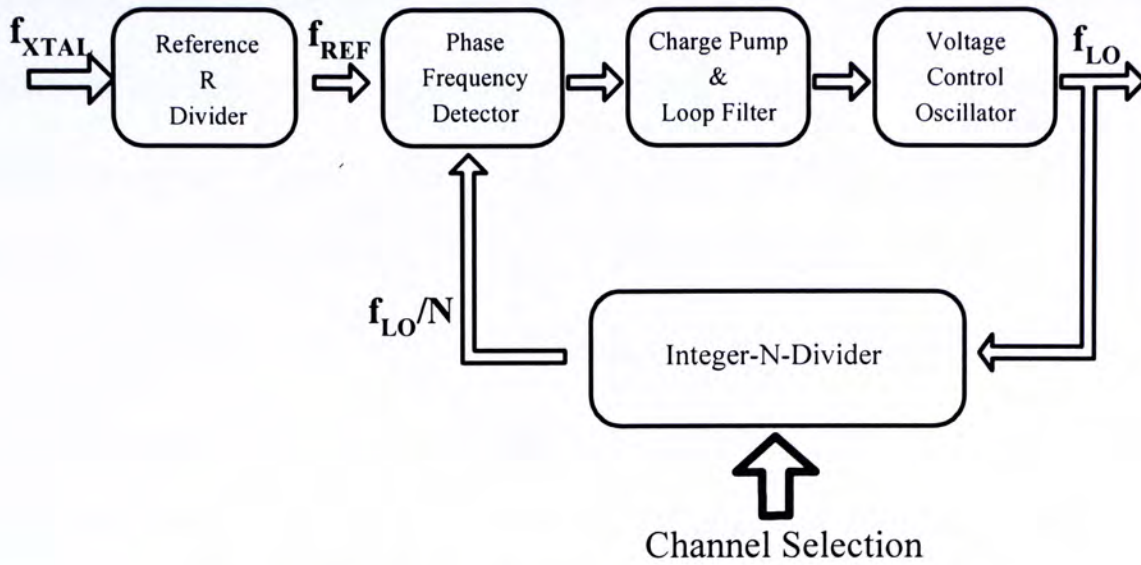


Figure 1.1: Block diagram of an integer-N PLL

The intuitive realization of a programmable counter is consisted of a NAND gate and programmable flip-flop (P-FF) counter, as shown in Figure 1.2 [1]. However, this topology suffers from some drawbacks. Firstly, the counter contains huge amount of logic when the division ratio is large that leads to high circuit complexity. The synchronous implementation also implies that all P-FFs are operated at the highest frequency. As a result, it consumes a lot of power and it is not suitable for low power applications. Besides, operation at giga-hertz range using this CMOS technology is difficult due to the low transconductance of transistor.

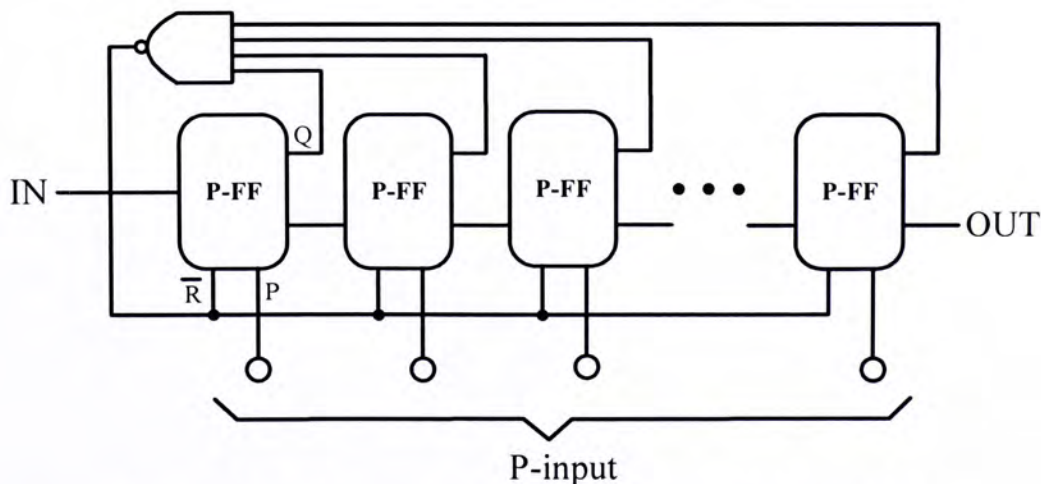


Figure 1.2: Block diagram of a programmable divider

A better implementation of the integer-N-divider is shown in Figure 1.3. It consists of a DMP, a programmable counter and a swallow counter. The DMP is used to pre-divide the input frequency with two possible division ratios (N and N+1). The DMP begins with a division ratio of N+1 and the output of DMP is then divided by both the pulse counter and swallow counter. After the swallow counter counts S pulses, the Modulus Control changes its logic value. The DMP then divides the input by N until the pulse counts P pulses. It then resets both counters and the whole cycle is repeated. Since the program counter already counted S pulses before the division ratio changes, only P-S pulses are required before the program counter is overflow. Consequently, the effective division ratio N_{total} which equals to the total number of pulse at the input counted for one cycle becomes:

$$(N + 1)S + (P - S)N = NP + S \quad \dots(1.1)$$

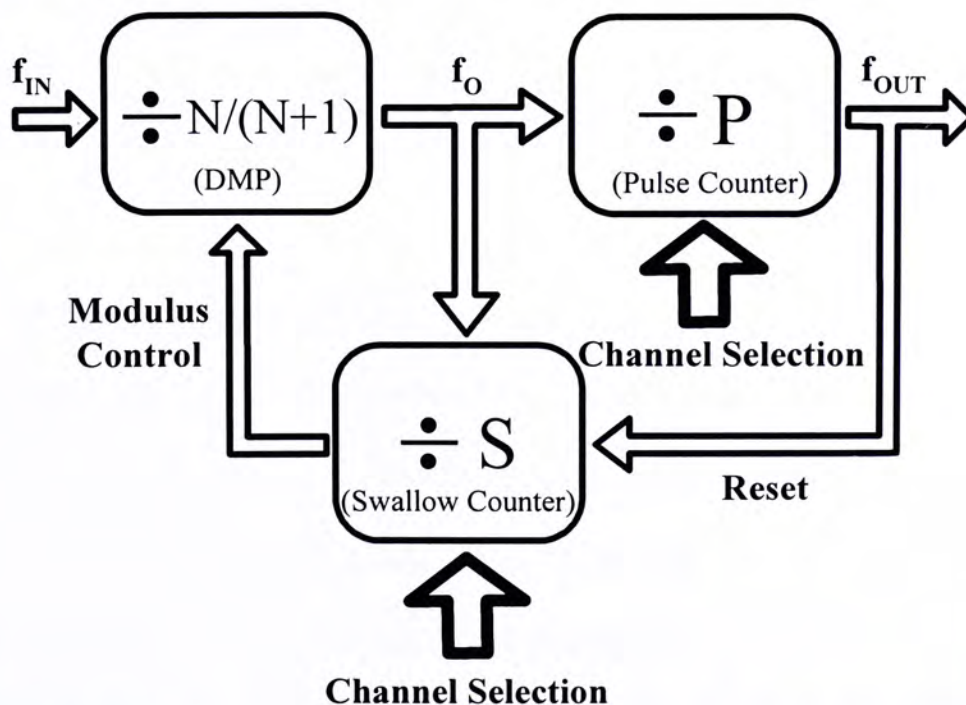


Figure 1.3: Block diagram of a pulse-swallow integer-N-divider

If S is variable between 0 and $N-1$, the complete range of division numbers can be realized. For proper reset by the pulse counter, P must be larger than the largest value of S , i.e. $P \geq N$. For a given minimum synthesizer frequency, the prescaler division number is limited since the smallest obtainable division number is N^2 .

This implementation only requires the DMP to work at the highest frequency and it looses the requirements of the other two counters in terms of both the speed and power dissipation.

In PLL, DMP is one of the most challenging sub-circuits because it operates at the highest frequency. Since it is not a problem to design a very high frequency VCO in current CMOS technology, DMP becomes the major bottleneck on operating frequency of PLL. Low power dissipation is always desirable for PLL design in order to stretch the battery life of portable products and to prevent circuit failures due to overheat. However, DMP is also known to be one of the most power consumption building blocks in PLL. Simultaneous switching noise in prescaler coupling to the VCO will also affect the phase noise performance of the PLL. Hence, the design of high-speed, low power and low switching noise DMP is a key hurdle for high performance PLL and is the subject of this work.

1.2 Thesis Organization

This thesis contains eight chapters. Chapter 2 investigates the various topologies of DMP. The basic operating principles, the advantages and disadvantages for each of them will be mentioned. Chapter 3 gives an in-depth discussion of the full-speed divide-by-2 design. A brief review of different divider designs is also provided. Chapters 4, 5 and 6 will present successful implementation of three DMPs: namely a 3V 900MHz low switching noise DMP, a 1.5V 2.4GHz low power DMP and a

1.5V 2.4GHz wideband DMP using 0.35 μ m CMOS processes. In Chapter 7, the measurement results are reported. Finally, conclusions and future works are covered in Chapter 8.

Chapter 2

DMP Architecture

This chapter introduces three different architectures of DMP. Operating principle as well as advantages and disadvantages of them will be presented.

2.1 Conventional DMP

The traditional DMP [2-4] generally consists of a synchronous divide-by-4/5 stage, an asynchronous divide-by-16 stage and some control logic as shown in Figure 2.1.

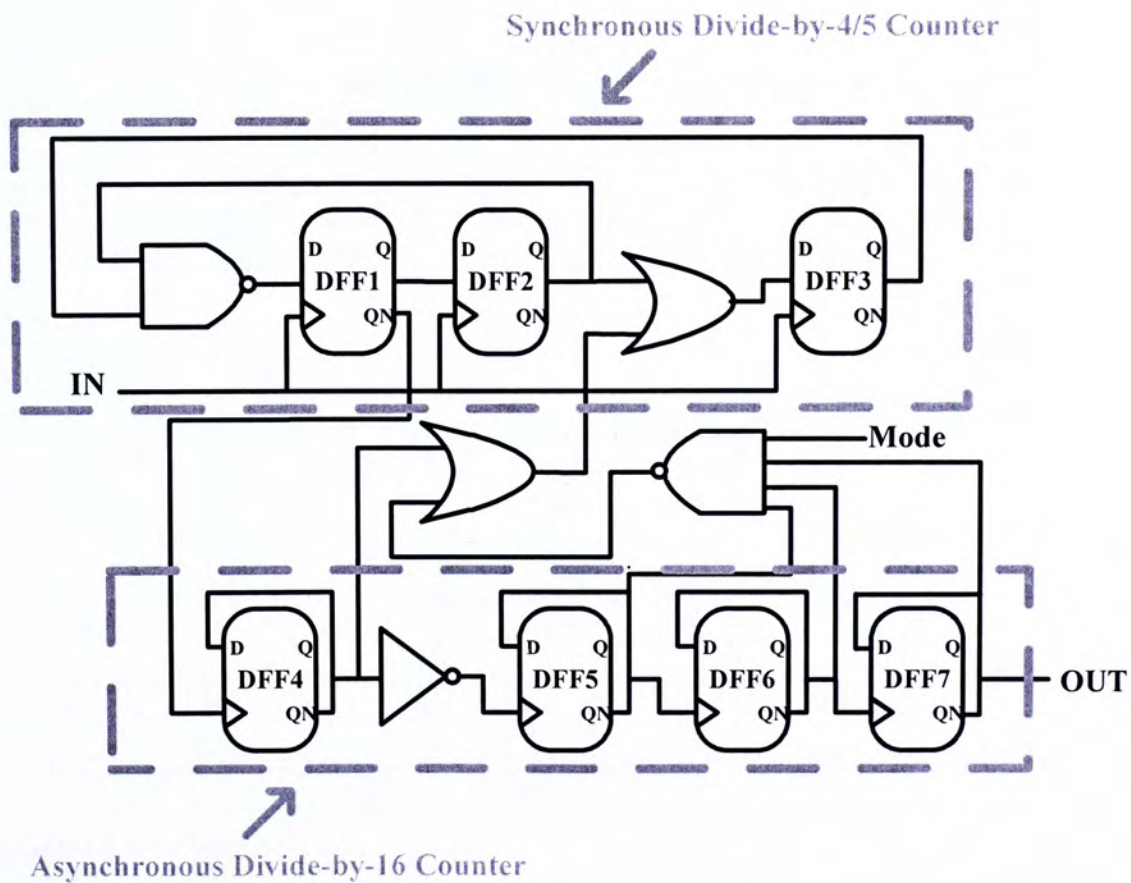


Figure 2.1: Block diagram of a conventional 64/65 DMP

2.1.1 Operating Principle

In Figure 2.1, QN of DFF1 is picked as the output of the fast 4/5 divider and connected to the clock of the first divide-by-2 stage, DFF4, of the asynchronous counter. Moreover, an inverter is added after the output of DFF4 to act as a buffer. The output of the circuit is either the clock input divided by 64 or 65 controlled by the 4 input Mode. When Mode equals to 0, the output is the clock divided by 64. When Mode = 1, the output is the clock divided by 65.

In order to introduce how the DMP can perform two modes of division, the working principle of synchronous divide-by-4/5 counter is firstly discussed.

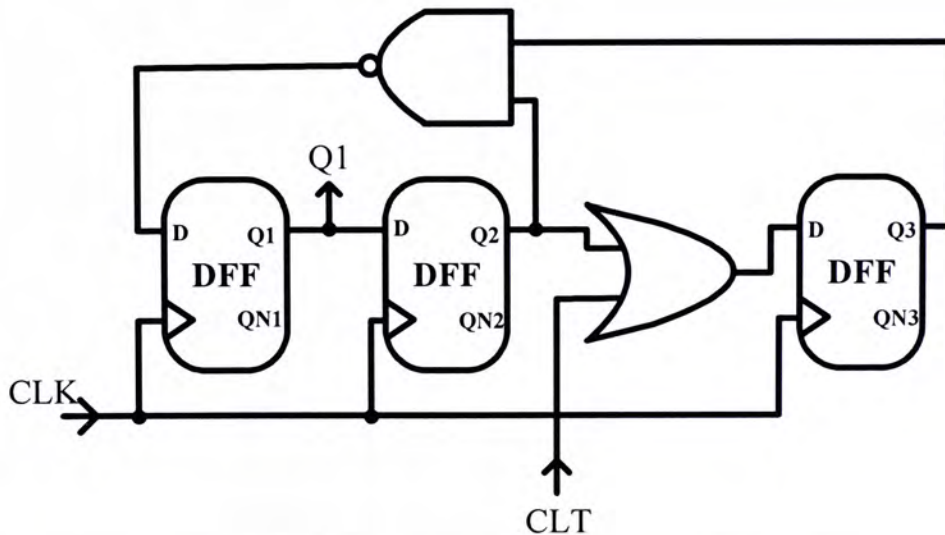


Figure 2.2: Synchronous divide-by-4/5 divider

Figure 2.2 shows the divide-by-4/5 counter extracted from the whole DMP. The three DFFs, the OR and the NAND gate constitute a state machine that is clocked by the CLK signal. The value of the CLT control signal determines which sequence of states it will go through.

When $CLT = 1$, $Q3$ is always equal to 1. As a result, the NAND gate operates as inverter and the circuit can be simplified as that in Figure 2.3. The state of $Q1$ is determined by the complement of $Q2$'s previous state, and the state of $Q2$ equals to the previous state of $Q1$. As a result, the state sequence of the divide-by-4/5 circuit when $CLT = 1$ is shown in Figure 2.4. Since the state sequence of $Q1$ repeats for every four states, it acts as a divide-by-4 circuit.

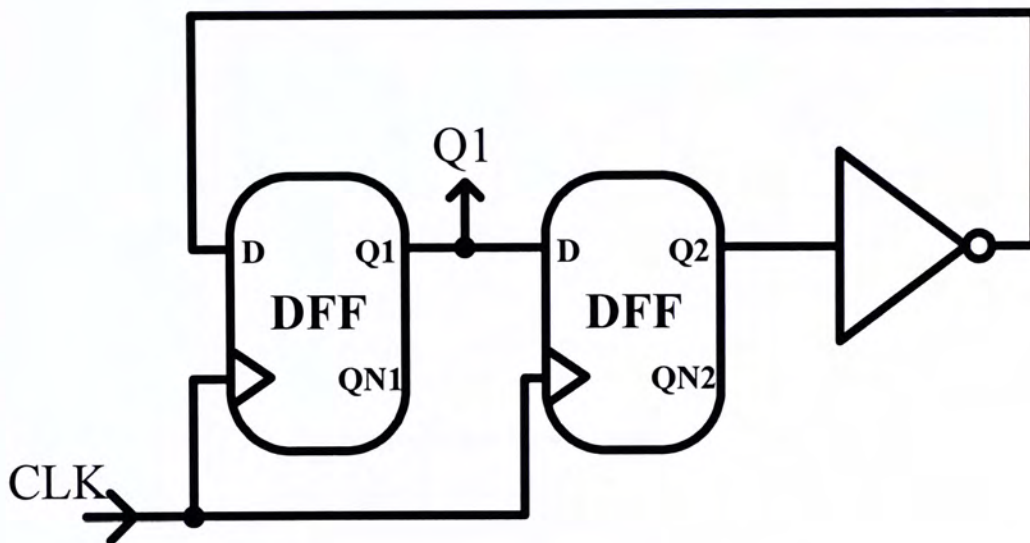


Figure 2.3: Equivalent circuit of divide-by-4/5 circuit for $CLT = 1$

Q1	Q2	Q3
0	0	1
1	0	1
1	1	1
0	1	1

Figure 2.4: State Sequence of the Simplified Circuit

When $CLT = 0$, the OR gate is bypassed. The circuit is simplified as Figure 2.5 and Figure 2.6 shows the state sequence of it. Since the state sequence of Q1 repeats for every five states, it becomes a divide-by-5 circuit.

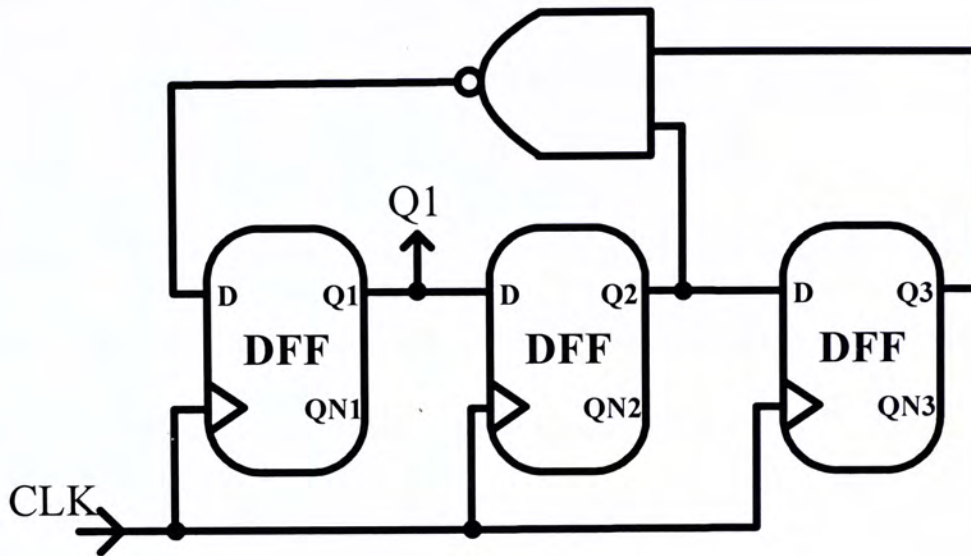


Figure 2.5: Equivalent divide-by-4/5 circuit for $CLT = 0$

Q1	Q2	Q3
0	0	0
1	0	0
1	1	0
1	1	1
0	1	1
0	0	1

Figure 2.6: State sequence of the simplified circuit

When $Mode = 0$ ($CLT = 1$), the control logic ensures the divide-by-4/5 circuit divided by 5 once for every output cycle. Division of 65 is then accomplished by dividing 15 times by 4 and one time by 5.

2.1.2 Disadvantages

The main drawback of the conventional DMP is situated in the synchronous divider. All three fully functional DFFs in the synchronous divider operate at the highest speed, seriously increases the load of VCO and power consumption. Besides, DFF3 in the input stage which is used to synchronize the two inputs of NAND gate. However, this DFF can only operate properly with a large swing input. This limits the performance of the input sensitivity. Moreover, the maximum operating speed of the divider-by-4/5 counter is much less than the basic divide-by-4 topology since the additional gating logics and DFF add extra propagation delay in the feedback path. Although clever design can reduce this effect by embedding the NAND-gate into the first stage of flip-flop, this delay can never be eliminated completely. Therefore, a DMP with this architecture will always have a smaller operating speed than a standalone divide-by-4 circuit. Finally, this architecture requires the control logic circuitry to generate a pulse with very short duration (1 clock period) when Mode = 0. It is difficult to generate such pulse at high frequency operation.

2.2 Pre-processing Clock Architecture

The pre-processing clock technique [5] provides us another choice for designing DMP (Figure 2.7). This approach avoids the use of gating method in conventional design and results a higher operating speed compared to conventional DMP architecture.

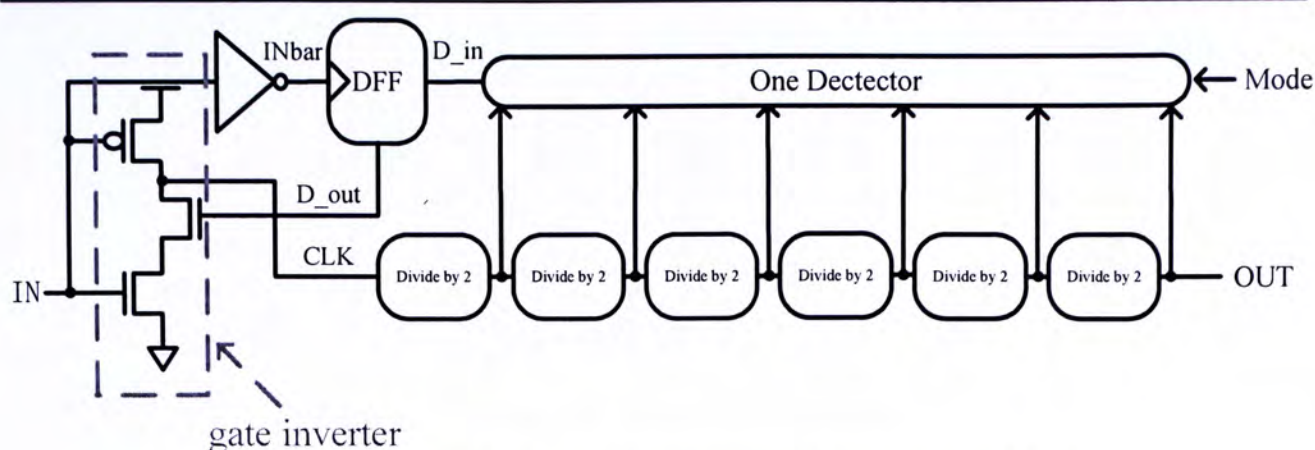


Figure 2.7: 64/65 DMP using pre-processing clock technique

2.2.1 Operating Principle

Two division ratios can be achieved by changing the Mode signal. When Mode = 0, CLK is an inverted version of the input clock, IN and the division ratio equals to 64.

When Mode = 1, the gate inverter posited in front of the first divider generates a signal (CLK) with one pulse removed (pulse swallowing). If the one detector generates a pulse (lasted for one clock period) for every output cycle, a division ratio of 65 can be obtained. The DFF is used to synchronize the rising-edge of D_in and that of INbar to perform correct logic operation of gate inverter. The detail of operation is depicted in Figure 2.8.

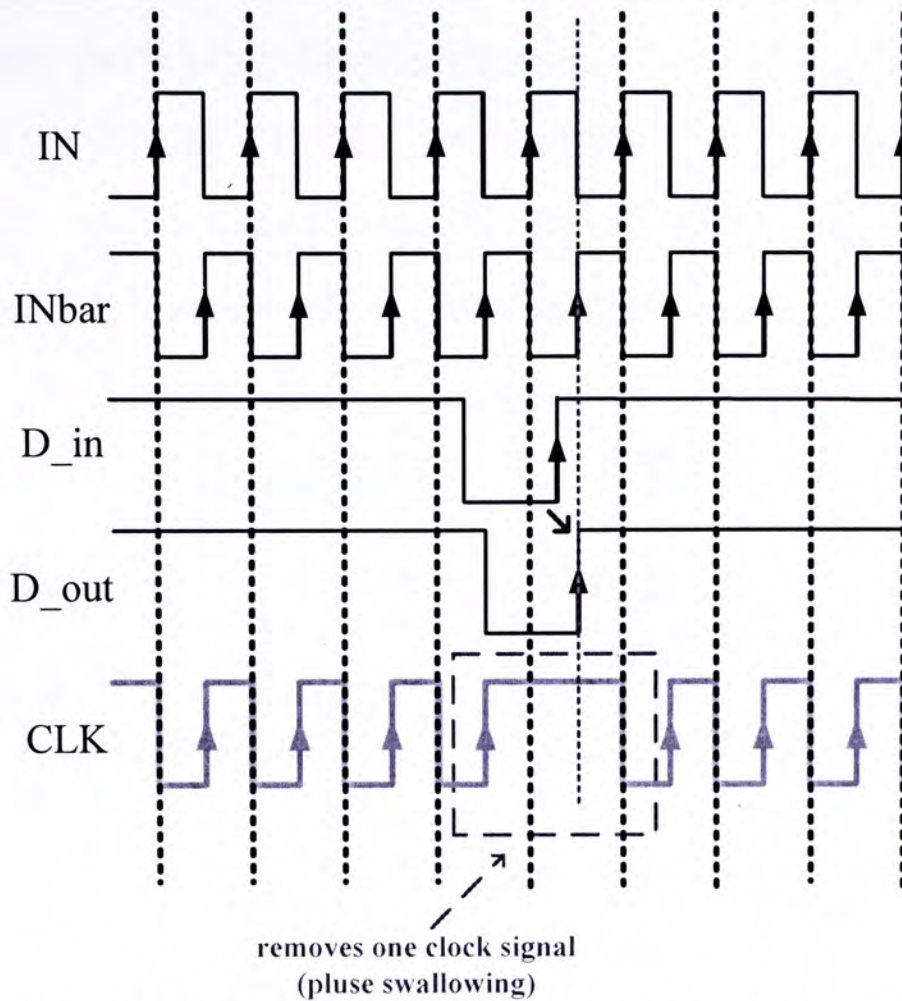


Figure 2.8: Principle of Pre-processing Clock Technique

2.2.2 Advantages and Disadvantages

The pre-processing clock architecture only requires the VCO output to drive one DFF. Besides, this kind of architecture makes use of asynchronous divider. Only two blocks (i.e. full-speed divider and DFF) are needed to operate at the highest frequency and thus lower the power consumption.

However, this architecture still suffers from some drawbacks. Since it makes use of DFF and some logic gates as the input stage and they can only function properly with a large swing input, this circuit is expected to have a lower input sensitivity. Moreover, the operating frequency of this architecture is limited by the logic circuits because it employs some logic gates to operate at the highest frequency.

2.3 Phase-switching Architecture

The phase-switching DMP topology was first proposed [6] to overcome the speed limitation associated with the conventional divider circuits using gating method. Figure 2.9 shows the functional block diagram of phase-switching DMP that consists of a divide-by-2 circuit, a divide-by-32 circuit and some phase control logic.

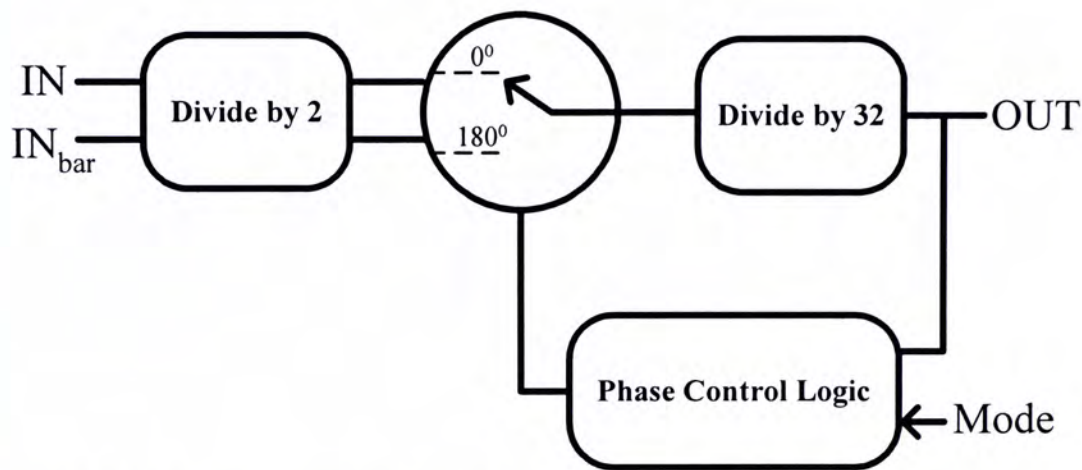


Figure 2.9: Block Diagram of 64/65 DMP using phase-switching technique

2.3.1 Operating Principle

The principle of phase-switching is demonstrated in Figure 2.10. Pulse-swallowing is achieved by making use of the differential output, $DIV_1(0^\circ)$ and $DIV_1(180^\circ)$ of full speed divider. When $Mode = 1$, the phase-selection network is disabled and the DMP simply acts like an asynchronous divide-by-64 ripple counter. However, when $Mode = 0$, an additional delay of one clock period will be introduced for every output cycle by the switching network and thus a dividing ratio of 65 is resulted.

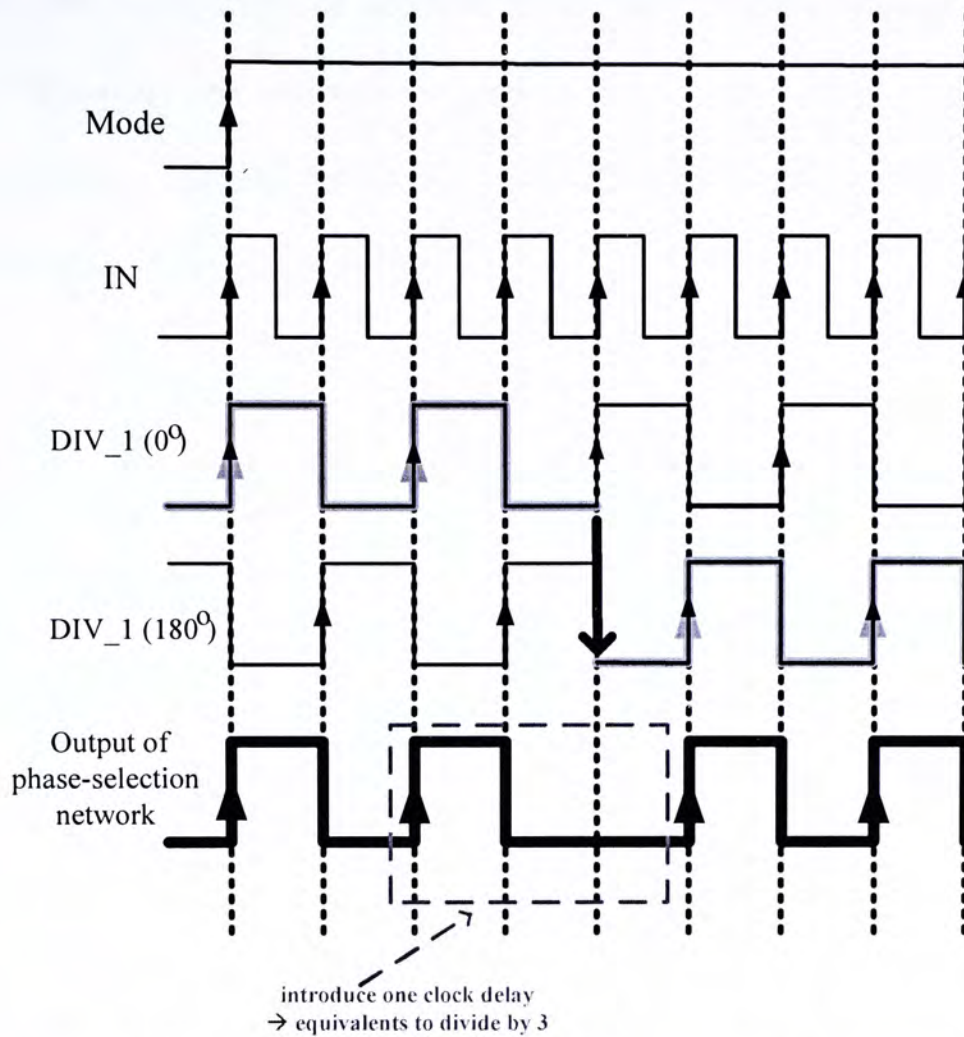


Figure 2.10: Working principle of phase-switching technique

2.3.2 Advantages and Disadvantages

This architecture only requires the VCO output to drive one DFF (full-speed divider) and therefore reduces the loading of VCO. Since only one DFF is needed to operate at the highest frequency, low power consumption can be achieved. Moreover, the input stage is the full-speed divide-by-2 circuit. Due to the injection-locking phenomenon, it achieves very high input sensitivity. Unlike the conventional DMP using synchronous divide-by-4/5 counter, no extra propagation delay is contributed to the loop in full-speed divider and thus a higher operating speed can be resulted. Since there is no logic gates operate at the highest speed, the operating speed of the prescaler is only limited by the first divide-by-2 stage.

However, the requirement of accurate multi-phase output increases the design difficulty. Moreover, this architecture need to tackle with glitch problem (Figure 2.11) during phase switching instant. Re-timing circuitry maybe needed to solve this problem and thus resulting high power consumption.

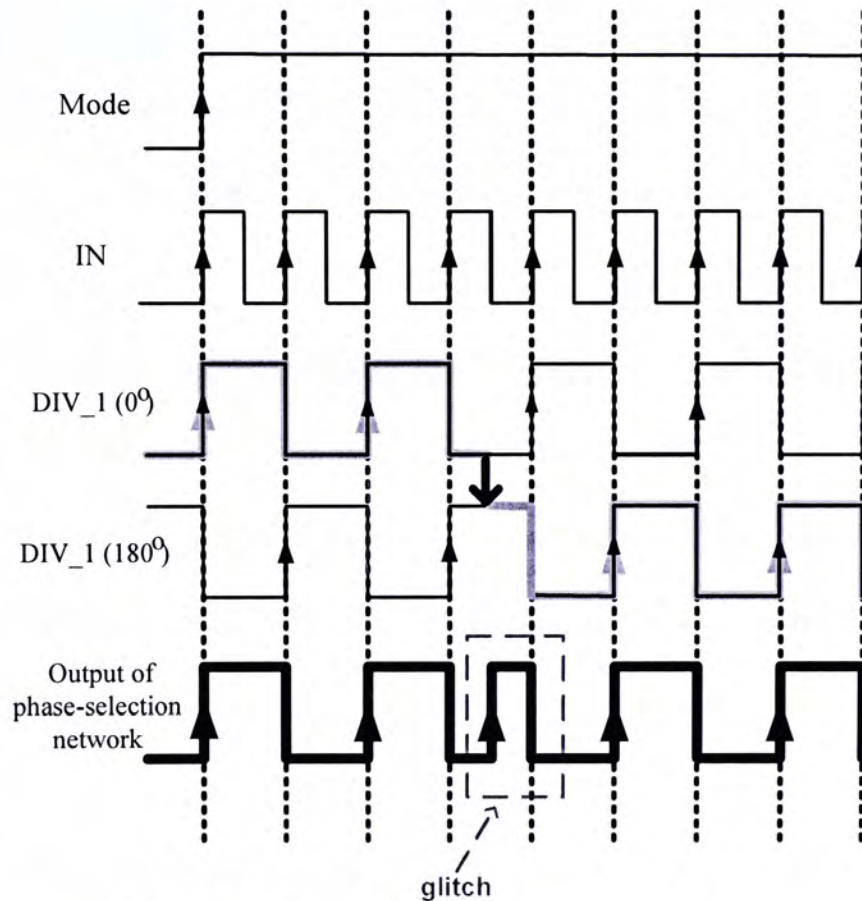


Figure 2.11: Glitch problem in phase-switching prescaler

2.4 Summary

This chapter provides an architecture overview of DMP design. The basic operating principles of three architectures are explained. Besides, the advantages and disadvantages of them are also mentioned. A thoroughly understanding of them and applying a suitable architecture to meet the design specifications are particularly important.

Chapter 3

Full-Speed Divider Design

3.1 Introduction

Full-speed divider is also the most challenging block in DMP design because it operates at the highest frequency and consumes a lot of power. It also needs to have a wide operating bandwidth. The input frequency range should be wide enough to cover the whole frequency band in the presence of process and temperature variations. The full-speed divider is usually implemented by using source-coupled logic (SCL) divider due to its superior speed performance compare to the dynamic true single-phase clock (TSPC) divider. This chapter gives an in-depth discussion of SCL divider design. Working principle, circuit analysis and implementation issues such as transistor sizing and layout considerations of it will be covered. Furthermore, a brief review of different divider topologies is also given.

3.2 Working Principle

The SCL divide-by-2 circuit incorporates a single master-slave flip-flop in a negative feedback loop. The flip-flop basically consists of two latches connected in cascade and is clocked by differential input clock, as shown in Figure 3.1. It has a fully differential structure. This circuit topology forces the state of each latch to toggle once (between one and zero) for two consecutive clock cycles and provides a divided by 2 function.

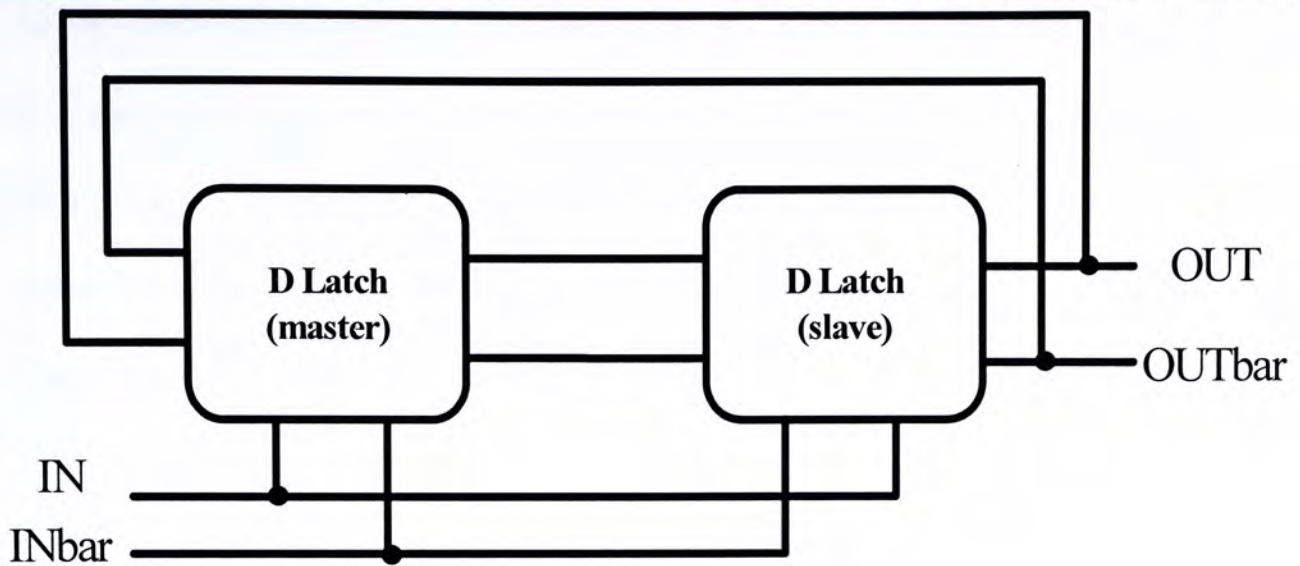


Figure 3.1: Block diagram of SCL divide-by-2 circuit

The schematic diagram of a SCL latch is shown in Figure 3.2. It consists of a current source, a sampling pair, a latching pair, two current-switches and active loads. In CMOS technology, passive poly-silicon resistors suffer from a process variation as large as 20% and also occupy large area. As a result, PMOSs serve as active loads with relatively constant resistance.

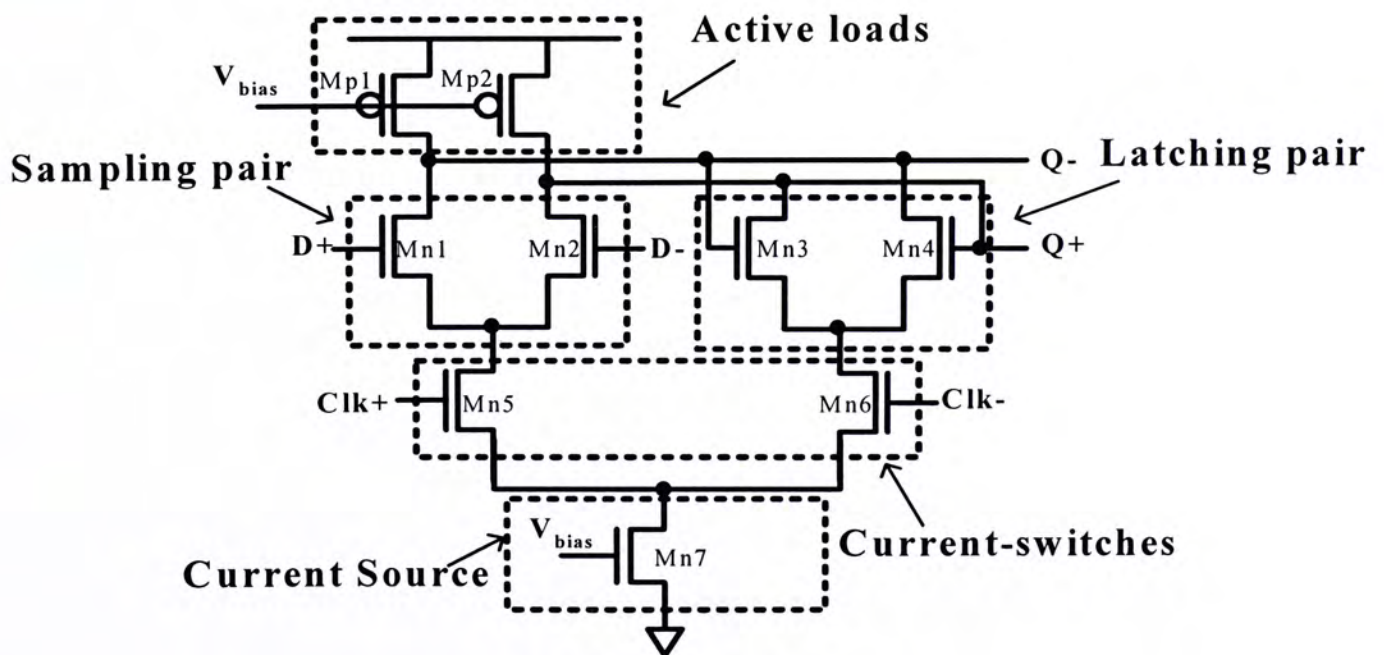


Figure 3.2: Schematic of a SCL latch

In the sensing mode ($CLK+ = 1$ and $CLK- = 0$), most current is flowing through the sensing pair and the D-latch is acting as a differential amplifier. In the latching mode ($CLK+ = 0$ and $CLK- = 1$), current is switched to the latching pair. The D-latch becomes a latch and the output is hold by the positive feedback of latching pair. Due to its current steering characteristic, it is also called a current-mode logic (CML) latch.

3.3 Design Issues

The key of high speed operating of the SCL divider is the limited output swing. The smaller the output swing, the faster the latch can change states. However, too small swing will affect the divider's driving ability and lowers the current switching ability of the following divider. The operating bandwidth and the operating frequency of the half-speed divider will therefore be reduced. Although increasing the size of current-switches in the half-speed divider can maintain the current switching ability, it increases the capacitive loading to the full-speed divider and slows down the operation of full-speed divider again. As a result, the output swing of the full-speed divider should be carefully determined.

Due to the number of stacked transistors in SCL latch, the NMOS tend to suffer from the body effect and that degrades the speed of divider. If the current source is removed, the structure has a potential to work faster.

The operating speed of the divider can be improved by increasing the transconductance of transistors, which is achieved by either increasing the aspect ratio (W/L) or by increasing the input dc bias level. However, both of them lead to increased power consumption. The increased drain capacitance at the output node

due to the increased transistor sizes also slows down the operation again. Besides, increasing the input dc bias requires a higher supply voltage. As a result, there exist complex tradeoffs between the speed, power consumption and minimum supply voltage.

Another way to increase the operating speed of divider as well as maintaining sufficient output swing is to apply a buffer after the full-speed divider. However, such high speed buffer consumes a lot of power. This time, it forms tradeoffs between speed, power consumption and driving ability.

3.4 Device Sizing

In a SCL latch, the loop gain provided by the cross-coupled pair must far exceed unity to ensure the state is store indefinitely. However, the regenerative pairs need not exhibit a loop gain much greater than unity for divider design. [7] This is because the latching mode is so short that even a weak regeneration can hold the stage by the parasitic capacitance at the output nodes at high frequencies. Too strong latching effect however resists the change of stage in sampling mode and thus lowers the speed of divider. Therefore, to optimize the full-speed divider, proper transistor sizing of the sampling part (Mn1, Mn2 & Mn5) and the latching part (Mn3, Mn4 & Mn6) is extremely important [8]. Besides, the aspect ratio of transistor should be kept as small as possible where minimum gate length is adopted in order to minimize the parasitic capacitance.

Besides, the ratio between the NMOS and the PMOS devices has to be found to set the output dc level appropriately. It is important since it determines the input dc level of the following divider.

One difficulty in sizing is that you can only roughly optimize the full-speed divider since you can never get the exact output capacitive loading until the next stage has been optimized (i.e. the half-speed divider). The effect of scaling in the half-speed divider propagates back to the full-speed divider and this scaling scenario extends to every stage in DMP also. Due to the feedback topology of DMP, each stage will affect each others. For this reason, the overall DMP must be treated as one entity, requiring iterations in the design of each building block.

3.5 Layout Considerations

As we all know, minimizing the output capacitance is the prime important for high speed and low power divider design. Also, the routing of the divide-by-2 stage is complicated due to the differential and feedback structure which requires special attention during layout.

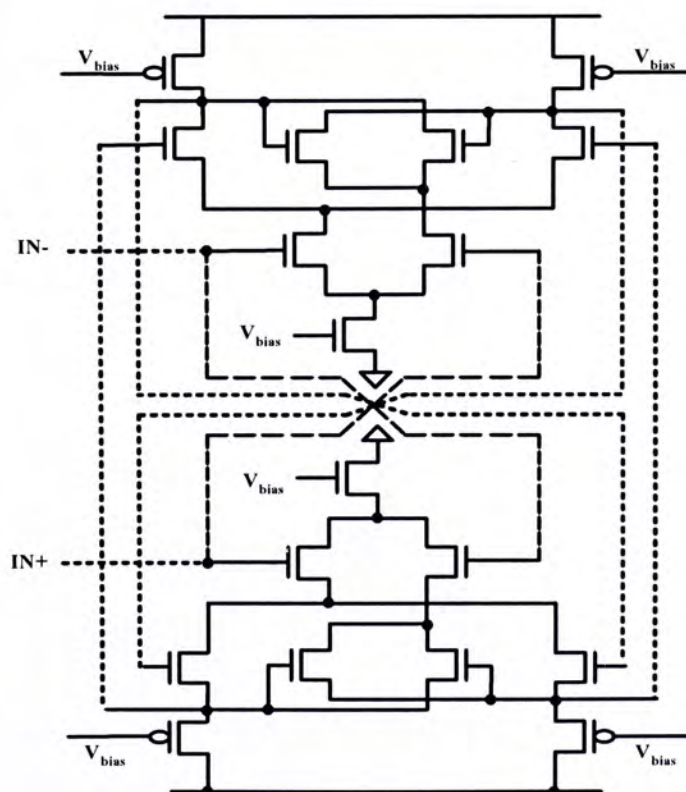


Figure 3.3: Back-to-back configuration of divider

Firstly, long signal routing should be avoided by using circular layout, as depicted in Figure 3.3. To reduce coupling effect, most of the supplies are suggested to run horizontally near the edge of the cell. Since the master and slave latches are laid out in back-to-back fashion around the power supply lines, it ensures all differential connections have the same length. For differential circuitries, symmetry layouts are required for noise immunity reason.

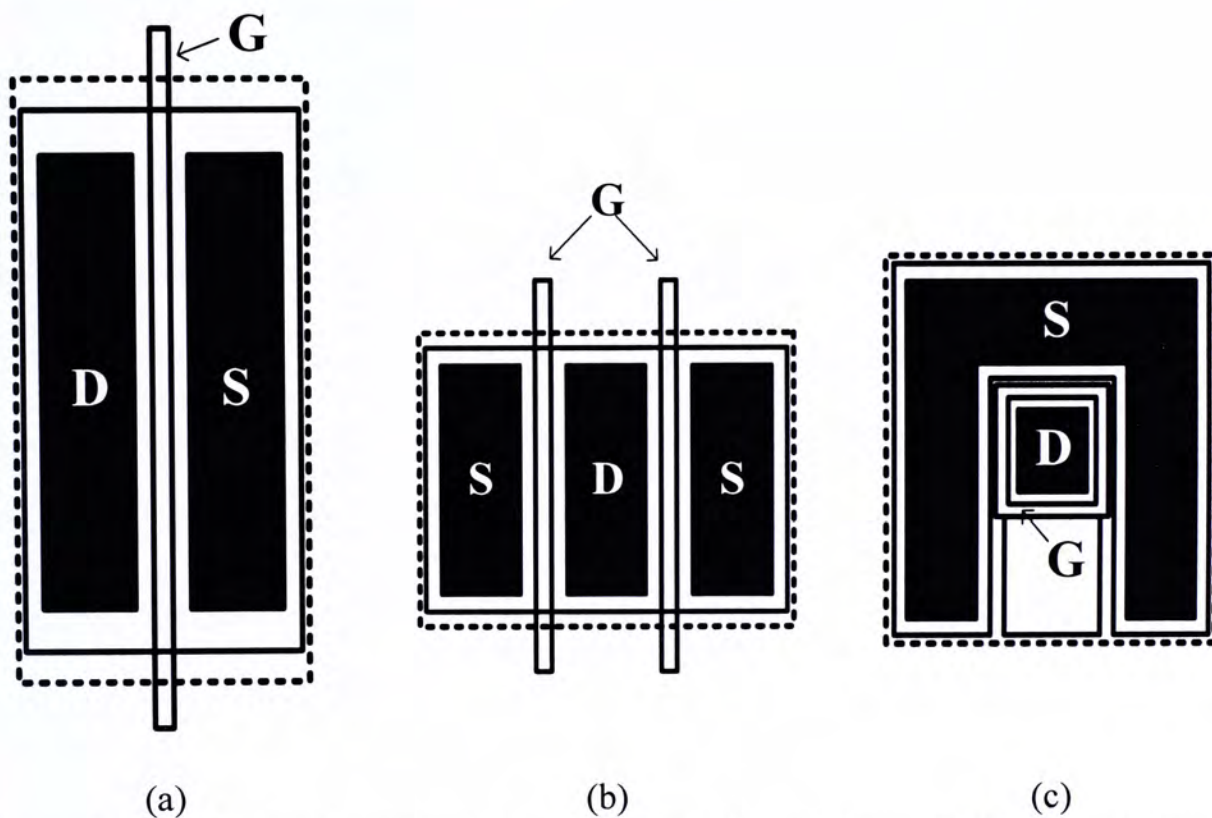


Figure 3.4: Transistor layout techniques (a) Straight-gate layout (b) Two-gate layout (c) Ring-shape layout

Another way to minimize the parasitic capacitance at the output node is to use ring-shaped transistor layout technique. [9] It may help at certain nodes to reduce the drain capacitance. The drawback of this layout technique is the increased source capacitance which might be a problem with the stacked structure. Moreover, models are not available from the fabrication foundry for transistors using ring-shaped layout. Extra modeling efforts are necessary which could be quite time consuming.

To reduce the development cycle, pseudo-ring-shaped layout is proposed. The pseudo ring-shaped layout technique is essentially the 2-gate finger technique, see Figure 3.4. It is worth to point out that the 2-gate finger technique gives the smallest drain capacitance among all multi-finger techniques. Most importantly, no extra modeling is required. Compared to other multi-finger techniques, the simplicity of 2-gate finger layout also minimizes metal crossings due to complicated routing. Besides, the source capacitance by using this layout method is relatively smaller compared to the ring-shaped layout technique which makes it more suitable for circuits with stacked structure.

Furthermore, layout should be kept as compact as possible to minimize interconnection parasitics. Due to the high resistance of poly-silicon and high capacitance between poly and substrate, interconnections are made with metal and the use of gate is limited to gates. Wide metals tracks should be used for power lines to minimize voltage drop due to parasitic resistance and to sustain the high current flows. Besides, enough via should be added to connect different metal layers in order to reduce parasitic resistance.

3.6 Input Sensitivity

Besides of speed and power, input sensitivity (Figure 3.5) is another key performance of divider. It illustrates the minimum input swing (or input power) for proper operation versus operating frequencies. Note that the input sensitivity curve is not symmetric, minimum clock swing for proper division at relatively low frequencies is smaller compared to that at relatively high frequencies. It is because even if the current is not fully switched between the sampling parts and latching parts,

the circuit still has enough time to restore the levels at low frequency operation. However, the divider requires greater clock slew rates so as to steer the tail current rapidly at high frequency operation. For a sinusoidal clock waveform, this translates to larger swing [7].

An interesting observation is that there exists a frequency continuous to provide a divide-by-2 operation with extremely small input swing. It is because the divider is in fact a two-stage oscillator oscillating at half of the input frequency under the condition that there is no ac input.

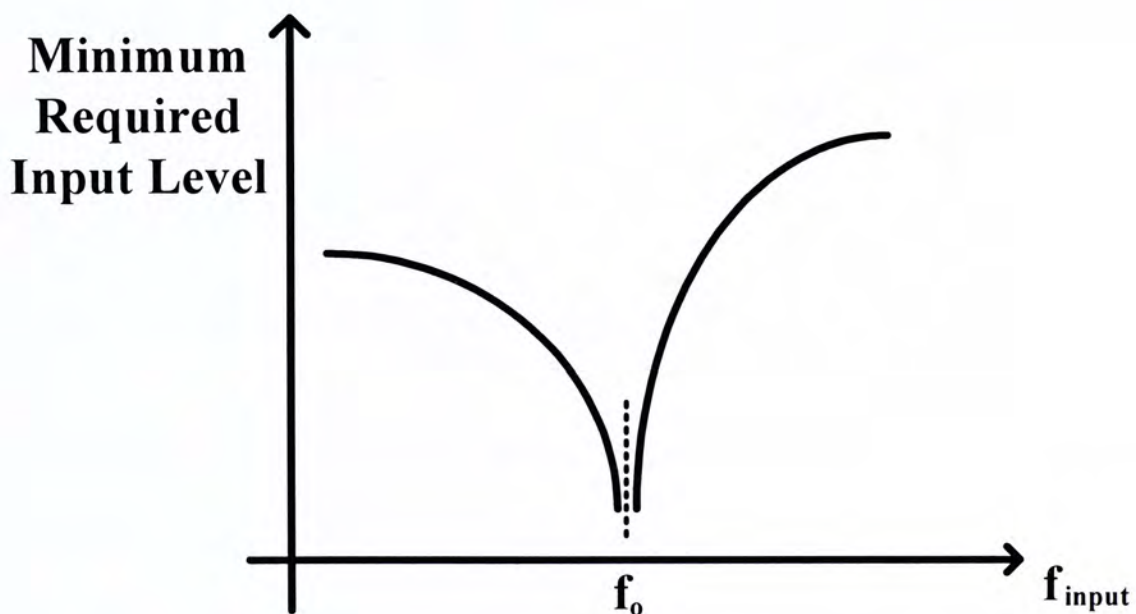


Figure 3.5: Minimum input swing as a function of input frequency

The bandwidth of the divider is defined as the frequency range for proper operation at a particular input swing (usually take the VCO output swing as a reference). The divider needs to have an input frequency range at least as wide as the whole tuning range of oscillator to cover the whole channels in the presence of process and temperature variation. Some design margin should be considered to guarantee the divider is able to work under process variations of the VCO as well as the divider itself.

3.7 Modeling

As mentioned before, the divider without ac input is essentially a ring oscillator (Figure 3.6) where the latch without clock signal acts like a delay cell. As a result, a high speed divider can be obtained if a high speed ring oscillator is designed. The task now becomes simply designing a high speed oscillator.

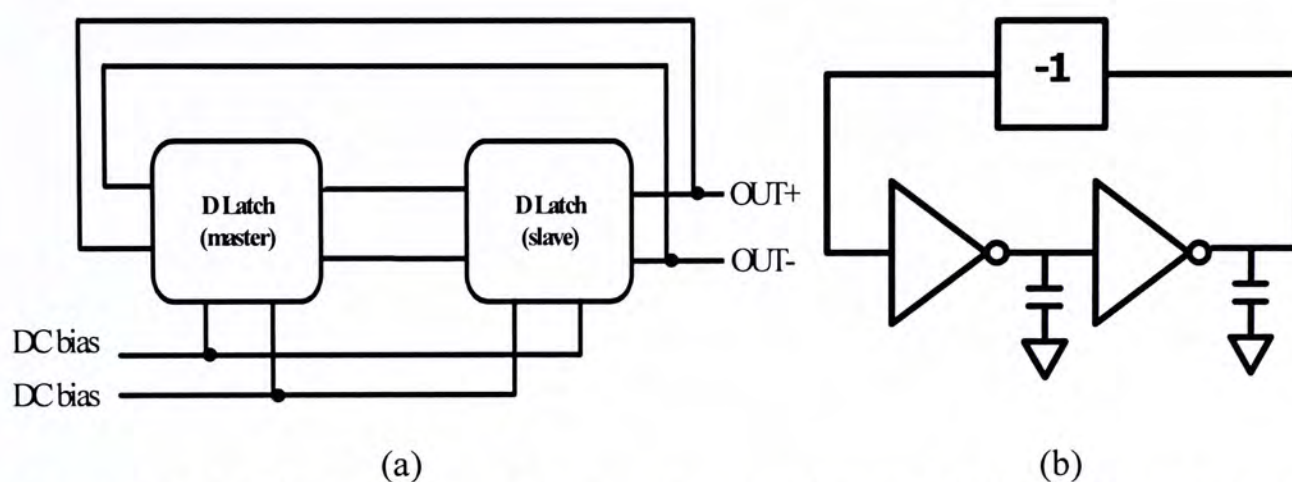


Figure 3.6: (a) Block diagram of the two-stage oscillator (b) Half-circuit equivalent

Since the requirement of loop gain for oscillation is just larger than one, we biased the active loads in deep-triode region rather than saturation region to maximize the bandwidth of the delay stage and thus achieve a high oscillating frequency.

The operating frequency of the divider can be roughly predicted by obtaining the self-oscillating frequency of the divider. As suggested in [10], the delay cell can be modeled as a single-pole, single-zero system. The pole formed by the small signal resistance and the output capacitive load becomes the main constraint of high speed operation. Besides, the gate-drain capacitance can provide a feed-forward path that for the input signal to the output of the latch at very high frequencies which results a dominant right-half plane zero. The pole could be located positioned at right-half plane or left-half plane depending on your design. As shown in Figure 3.7(a), the

delay stage can be model as a differential amplifier with negative resistance loads with values of $-2/g_{m3}$. From the half-circuit in Figure 3.7(b), the equivalent resistance $R_p // (-1/g_{m3,4}) = R_p / (1 - g_{m3,4} R_p)$. [7] If the gain of regenerative pair (i.e. $g_{m3,4} R_p$) drops below unity, the dominant pole will be located at the left-half plane. Figure 3.8 shows the frequency response of delay cell for the two possible cases.

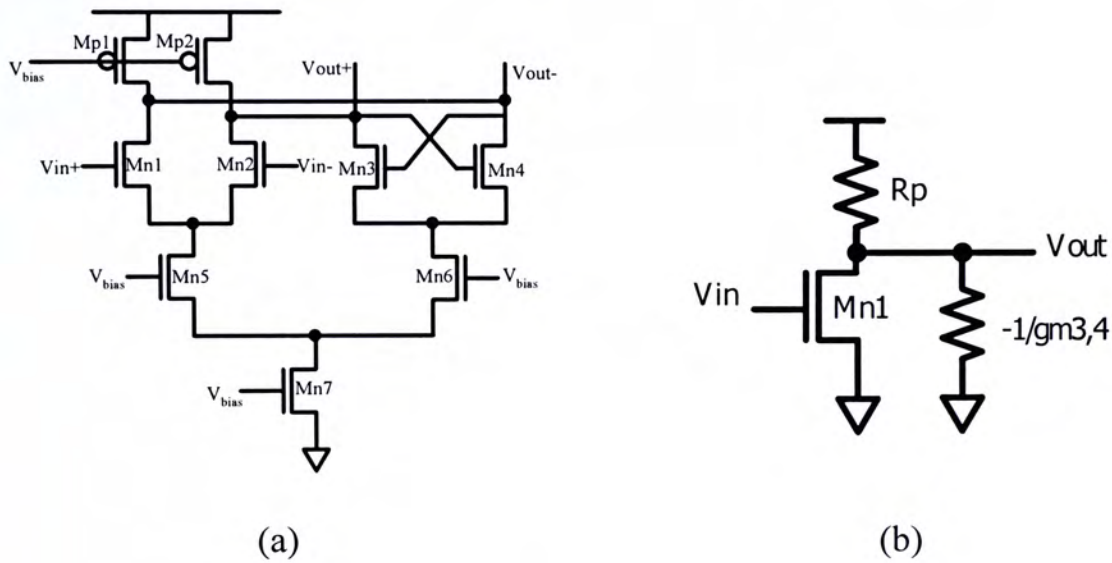
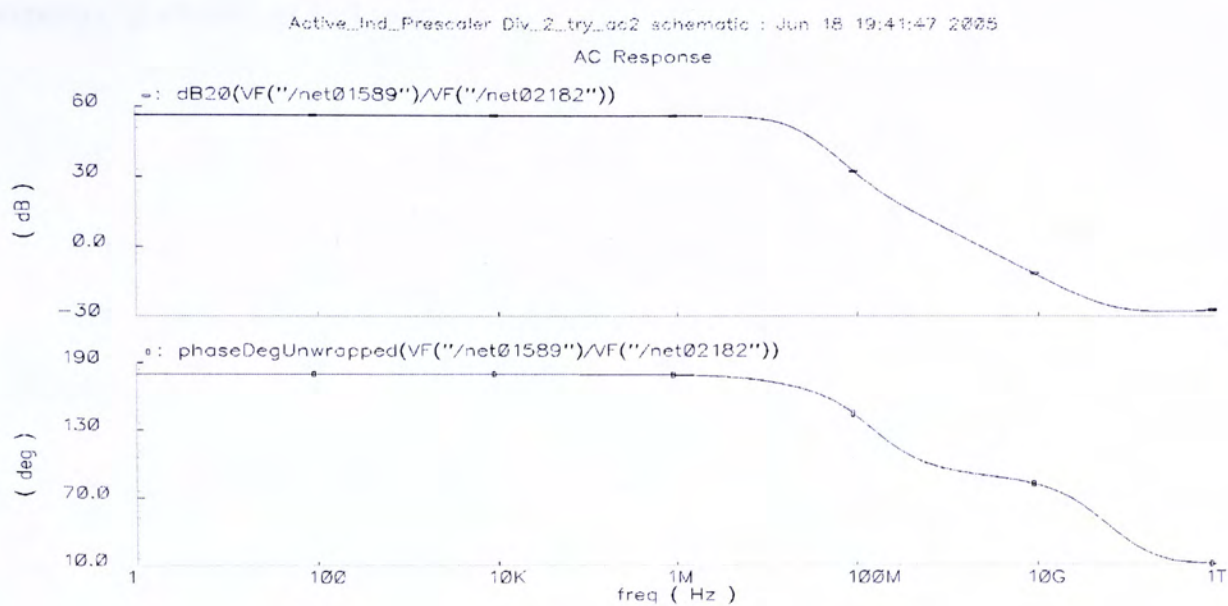
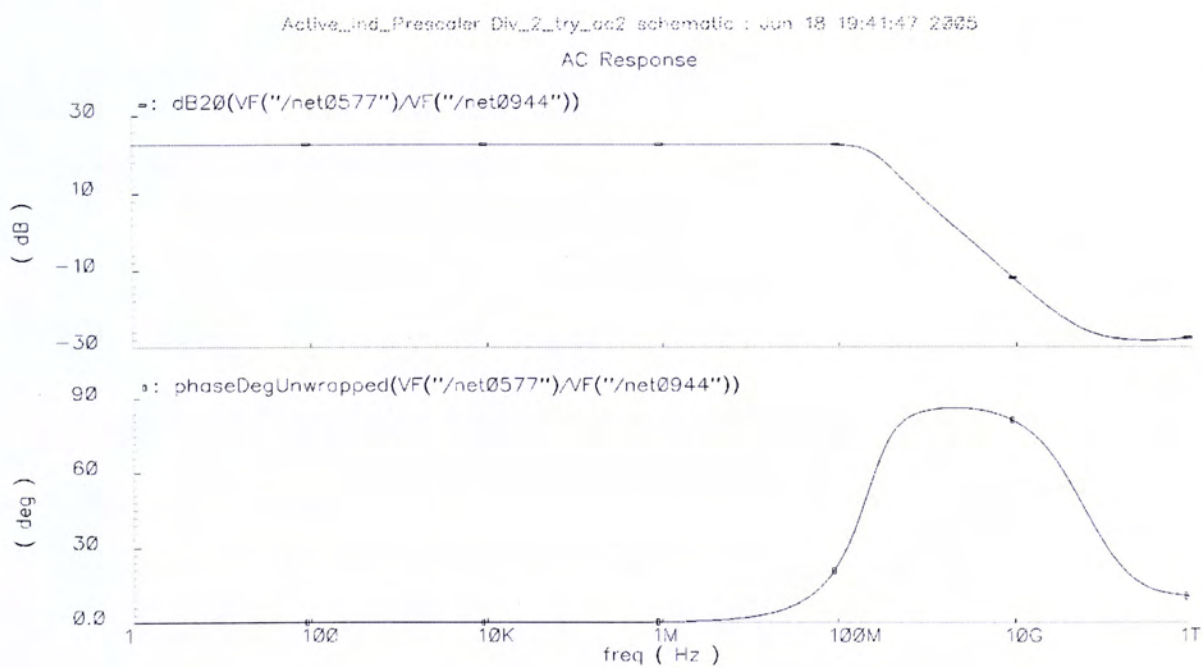


Figure 3.7: Delay cell (a) Schematic diagram (b) Half-circuit equivalent



(a)



(b)

Figure 3.8: Frequency response of delay cell (a) with LHP pole and RHP zero
(b) with RHP pole and RHP zero

The delay stage can be considered as a first order system and its frequency response is shown as follows:

$$H(j\omega) = A_0 \frac{1 - j\omega/\omega_z}{1 \pm j\omega/\omega_p} \quad \dots(3.1)$$

where

A_0 : small signal dc gain of the delay stage

ω_p : frequency of dominant pole

ω_z : frequency of dominant zero

Barkhausen criteria indicate that the necessary but not sufficient conditions for oscillation are:

1. Total phase shift around a loop equals to 360°
2. Loop gain is greater or equal to 1

Taking account with the -180 degree shift through the negative feedback, each delay stage should contribute -90 degree phase shift for oscillation. At the oscillating frequency, the following phase relationship should be satisfied:

$$\begin{aligned} \angle H(j\omega_0) &= -\tan^{-1}\left(\frac{\omega_0}{\omega_z}\right) \mp \tan^{-1}\left(\frac{\omega_0}{\omega_p}\right) = -\frac{\pi}{2} \\ \tan\left[-\tan^{-1}\left(\frac{\omega_0}{\omega_z}\right) \mp \tan^{-1}\left(\frac{\omega_0}{\omega_p}\right)\right] &= \tan\left(-\frac{\pi}{2}\right) \\ \frac{\left(\frac{\omega_0}{\omega_z}\right) \times \left(\frac{\omega_0}{\omega_p}\right)}{1 \pm \left(\frac{\omega_0}{\omega_z}\right) \times \left(\frac{\omega_0}{\omega_p}\right)} &= \infty \end{aligned}$$

$$1 \pm \left(\frac{\omega_0}{\omega_z}\right) \times \left(\frac{\omega_0}{\omega_p}\right) = 0$$

$$\omega_0 = \sqrt{\pm \omega_z \omega_p} \quad \dots(3.2)$$

In addition to the phase condition, the gain at ω_0 must be greater than unity to initiate the oscillation. Apply condition (3.2) to (3.1), yields other criteria for oscillation:

$$|H(j\omega_0)| \geq 1$$

$$\left| A_0 \frac{1 - j\sqrt{\pm \omega_z \omega_p} / \omega_z}{1 \pm j\sqrt{\pm \omega_z \omega_p} / \omega_p} \right| \geq 1$$

$$|A_0| \times \frac{|1 - j\sqrt{\pm \omega_p} / \omega_z|}{|1 \pm j\sqrt{\pm \omega_z} / \omega_p|} \geq 1$$

$$|A_0| \times \frac{\sqrt{1 \pm \omega_p} / \omega_z}{\sqrt{1 + \omega_z} / \omega_p} \geq 1 \quad \dots(3.3)$$

3.8 Review on Different Divider Designs

3.8.1 Divider with Dynamic-Loading Technique

A key problem limiting the speed of the conventional SCL divider is the dilemma of load resistance. On the one hand, a smaller load resistance is needed to keep the RC time constant small during the sampling period; while on the other hand, a large load resistance is needed to make the signal difference large during the latching period so that it can drive the other flip-flop. In [11], a dynamic loading technique is proposed to solve this problem, as shown in Figure 3.9. In each of the latch, the PMOS loads are clocked by the complement of the switching clock. This dynamic

loading technique increases the operating frequency and the operating frequency range of the divider.

However, this circuit suffers from a few problems. Firstly, this technique increases the loading of VCO since the VCO is required to drive four more PMOS load transistors. Also, the dc bias of the PMOS loads and the NMOS current switches are forced to be the same. In order to turn on both the PMOS and NMOS devices, there exists a minimum supply voltage which makes it not suitable for low voltage supply. A new divider is therefore proposed [12] aimed to solve this problem. The schematic of this low voltage divider is shown in Figure 3.10 which makes use of common gate input. This topology can work well at a relative low supply voltage. However, the low input impedance of the divider limits the VCO output swing (loading effect). To drive the mixer, extra buffers are needed which leads to high power consumption.

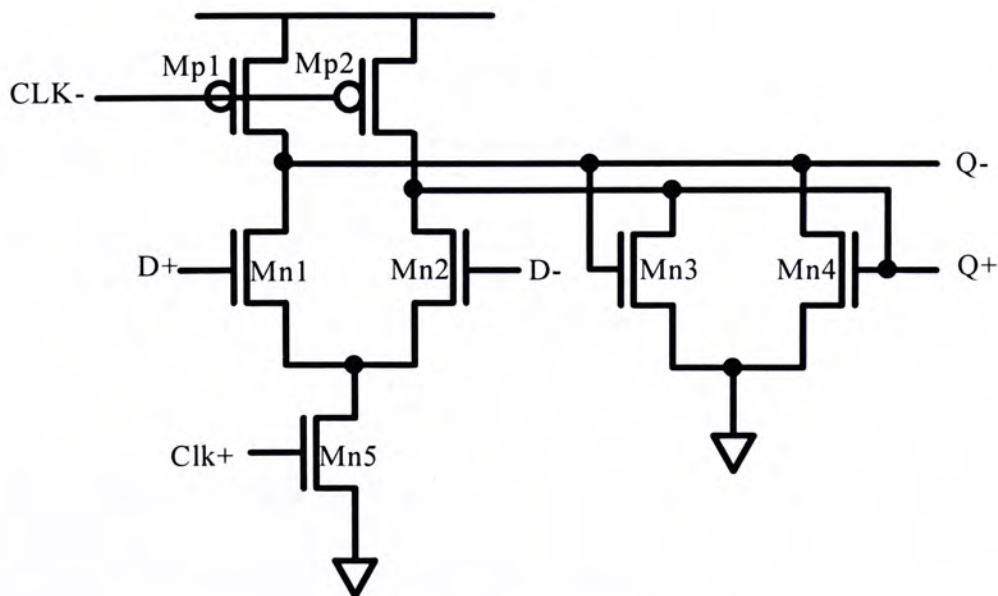


Figure 3.9: Schematic of dynamic loading latch

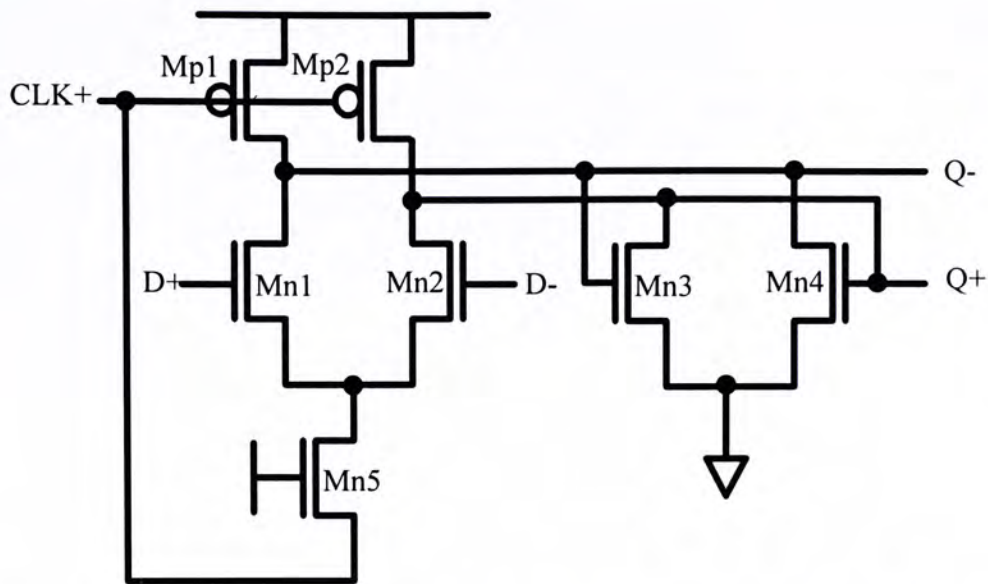


Figure 3.10: Schematic of low voltage dynamic loading latch

3.8.2 Divider with Negative-Slew Technique

As mentioned in the pervious section, divider is a ring oscillator with the absent of ac input. This implies some of the speed enhancement techniques for ring oscillator design can also be applied for divider design. One well-known speed enhancement technique for multi-phase ring oscillator is the negative-slew technique [13-15]. As shown in Figure 3.11 and Figure 3.12, the PMOSs of each inverter are turned on before the high-to-low transition and are turned off prematurely before the low-to-high transition. This mechanism speeds up the transition and results a higher oscillation frequency. In the slewed delay cell, the improved performance comes at the expense of the greater power consumption due to the time overlap when both PMOS and NMOS transistors are turned on.

In [16], the similar multi-feedback scheme is applied to the synchronous 4/5 divider in the DMP. The additional feedbacks (in the form of dotted lines) turn on the additional NMOS transistors prematurely and thus reduce the signal growth. The

operating frequency increases due to the reducing of time to change logic states. However, the complex routing and extra parasitic capacitance contributed by the additional NMOS transistors make the speed enhancement very limit. Most importantly, this technique can only apply to multi-stage (at least three stages) synchronous divider.

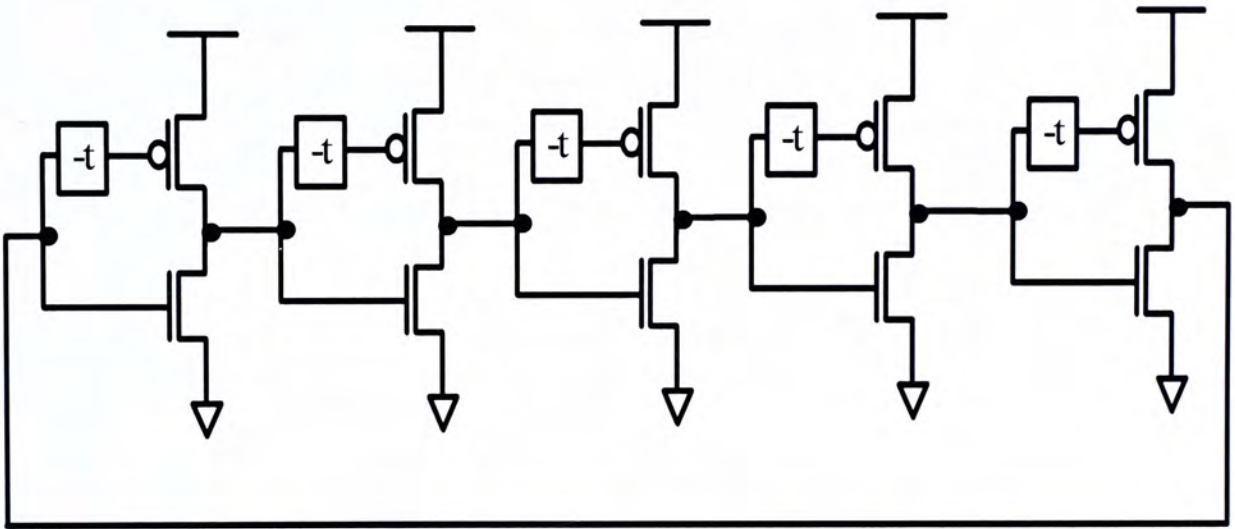


Figure 3.11: Conceptual ring oscillator with negative slew technique

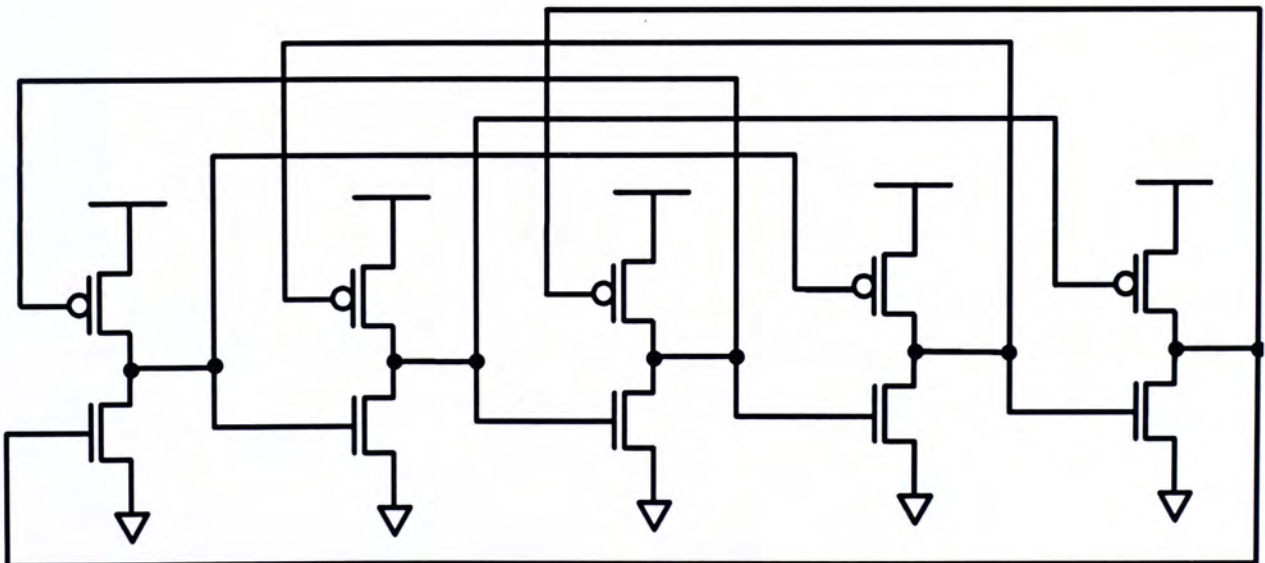


Figure 3.12: Real implementation of ring oscillator with negative slew technique

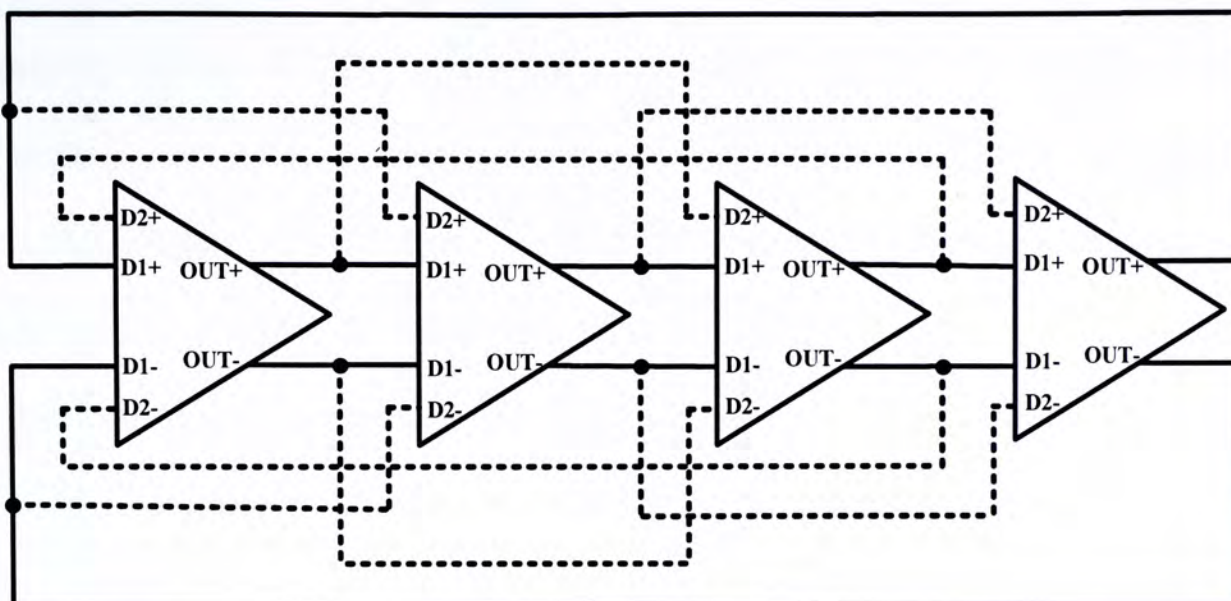


Figure 3.13: Block diagram of differential ring oscillator with negative slew technique

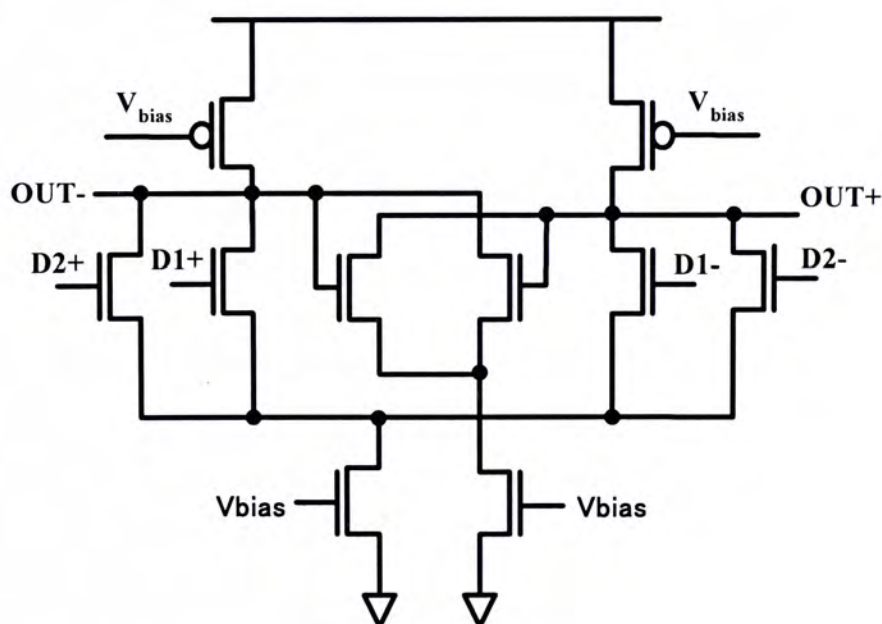


Figure 3.14: Schematic diagram of delay cell for differential ring oscillator with negative slew technique

3.8.3 LC Injection-Locked Frequency Divider

The dividers mentioned in previous sections are all static dividers. Such dividers can operate at very wide frequency range, from near DC to a high frequency. However, the power consumption increases drastically along with the increments of

operating frequency. Another type of high frequency divider is injection-locked frequency divider (ILFD), it can operate at relatively higher frequencies at the expense of narrow locking range. The division capability of ILFD with ratios higher than two brings an important power consumption and speed advantages to ILFD over static dividers. Figure 3.15 shows an example of ILFD.

The injection-locking phenomenon has been known for decades and Miller proposed a regenerative frequency divider based on this phenomenon in 1939 [17]. The main idea of his concept of frequency division was to create an oscillation at the sub-harmonic of the input signal. The ILFD can be described in Figure 3.16 based on the mixer-based model similar to Miller's since the locking mechanisms of regenerative frequency divider and ILFD are identical [18]. The model consists of an injector (mixer), a frequency multiplication element and a band pass filter. The frequency multiplication element in the feedback loop represents the non-linearity of the mixer. The band pass filter comes from the load impedance of the LC tank with finite quality factor. An input frequency ω_{in} and a postulated signal of frequency $(N-1)\omega_{out}$ are applied to the RF and LO ports of the mixer respectively. The mixer output contains different sideband frequencies among which only the sideband $\omega_{in} - (N-1)\omega_{out}$ survives at the output while injection-locked. As a result, the output frequency ω_{out} will be synchronized with the sub-harmonics of the input signal ω_{in}/N . The ILFD maintains locked as long as the injected signal is sufficient large. A large input amplitude is also required to excite the LO port of mixer.

The ILFD can achieve division ratios greater than two. However, due to the load selectivity, the output signal is locked only within a band around the LC resonant frequency. Besides, the large area occupied by the inductors also increases the cost of the chip.

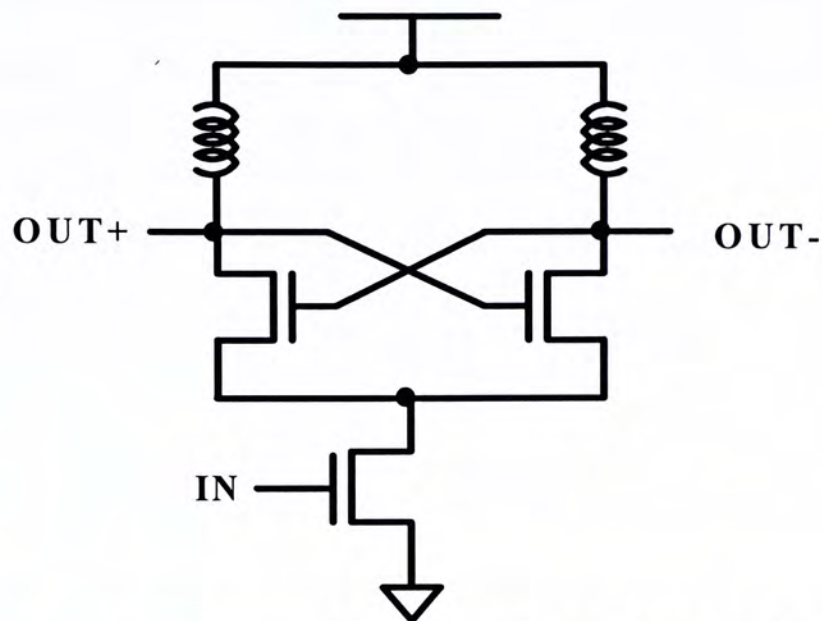


Figure 3.15: Schematic of LC injection-locked divider

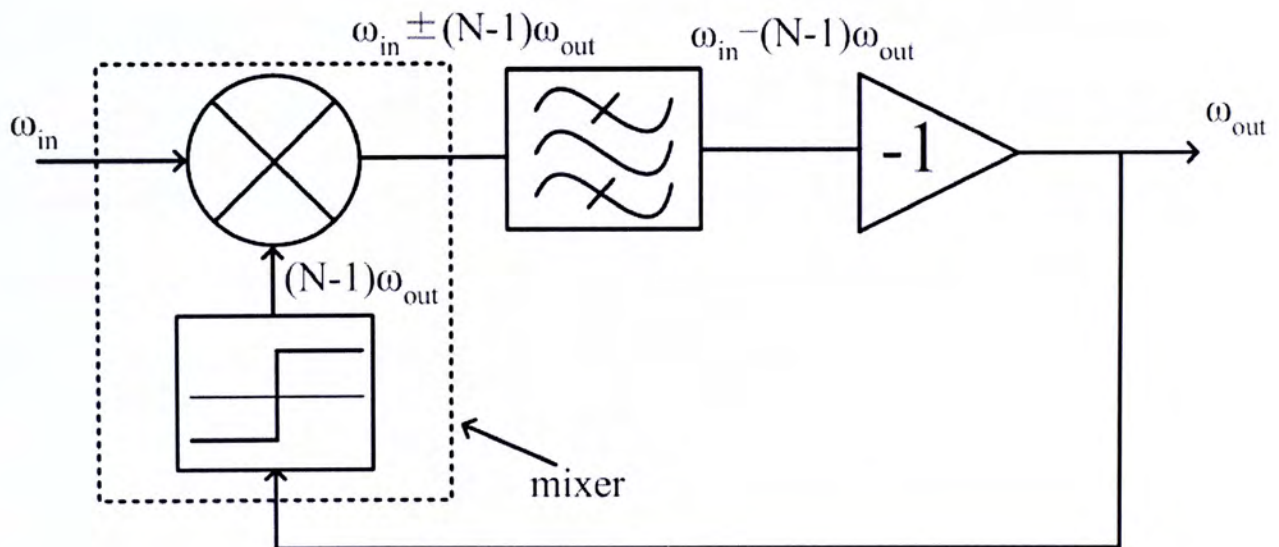


Figure 3.16: Equivalent model of LC injection-locked divider

3.8.4 Dynamic True Single Phase Clock Frequency Divider

Other than the static SCL divider, dynamic TSPC divider is another popular frequency divider in high frequency applications.

A TSPC frequency divider is shown in Figure 3.17 [19]. The circuit can be separated into three parts. The first part is a gated inverter that consists of M_{p1} , M_{p1} and M_{n1} . It passes the complement of node $n3$ when CLK goes low. The second part

is a latch stage that consists of M_{n2} , M_{n3} , M_{n4} , M_{n5} , M_{p3} and M_{p4} . This part will be activated and stores the output of the gated inverter when CLK is high. The final part is an inverter formed by transistors M_{p5} and M_{n6} to serve as an output buffer. It can also filter out the spikes at the output. For high speed operation, it can be implemented by pseudo-NMOS logic to reduce parasitic capacitance. The output of the TSPC flip-flop (Q_n) is directly connected back to the input (D) to obtain the divide-by-2 function.

The operation of the TSPC divider is divided into two phases: pre-charge phase and evaluation phase. In the pre-charge mode ($CLK = 0$), node $n1$ is pre-charged to a stage opposite to node $n3$ and node $n2$ is pre-charge to V_{DD} . As transistors M_{p4} and M_{n4} are turned off, node $n3$ is floating. In the evaluation mode, if node $n1$ is pre-charge to “1”, node $n2$ is discharged and voltage of node $n3$ is pulled up by transistor M_{p4} . on the other hand, if node $n1$ is pre-charge to “0”, node $n2$ is not discharged and voltage of node $n3$ is pulled down by transistors M_{n4} and M_{n5} . Since the logic stage changes at every input rising transition, it performs as a divide-by-2 circuit.

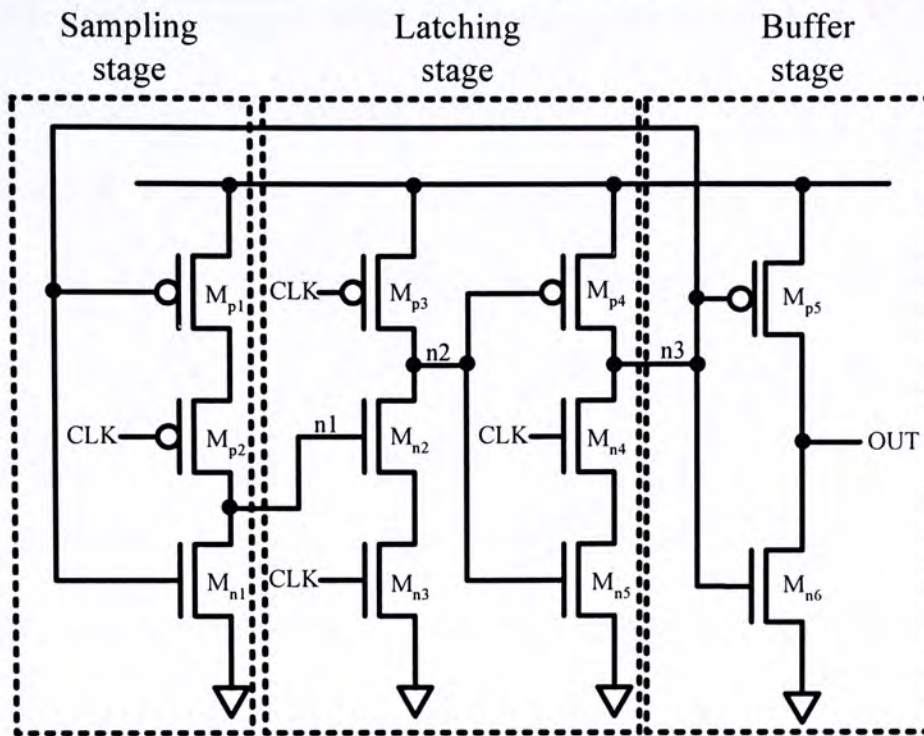


Figure 3.17: Schematic of the TSPC rising-edge-triggered divider proposed by Yuan and Svensson

This kind of divider is much simpler compared to the SCL design. And there is no static power consumption since there is no direct path from the voltage supply to the ground. Since some nodes have been already charged to high through the PMOSs during the pre-charge phase, those nodes need only to be selectively discharged during the evaluation phase while discharging through the NMOS devices is significantly faster than the time needed to charge up the nodes through the PMOS devices due to the higher mobility of NMOS devices. Furthermore, the output of this divider is rail-to-rail and this makes it easier to drive other digital logic circuits without any amplification of output signal. However, the circuit requires large amplitude of the input signal and the operating speed is very sensitive to the slope of the input signal. Therefore, a high speed buffer may need to insert in front of the TSPC. As a result, TSPC is not commonly used in the full speed divider design, in the contrast, TSPC dividers are usually adopted for the later divide-by-2 stages due

to its low power performance at relatively low frequency operation. Moreover, TSPC suffers from charge sharing problem at low frequency operation which results a minimum operating frequency of the circuit. Devices sizing plays an important role in increasing the operating frequency of the TSPC divider. Transistors should be carefully optimized for high speed in a series of post-layout simulation and layout-modification trials.

Figure 3.18 illustrates a falling-edge-triggered version of the divider in Figure 3.17. Since the discharging time is shorter than the charging time in CMOS technology, falling-edge-triggered divider is preferred for better jitter performance. Although the pull-up capability can be increased by increasing the size of PMOS devices, we don't usually do so for high frequency circuit designs because of the increased parasitic capacitance.

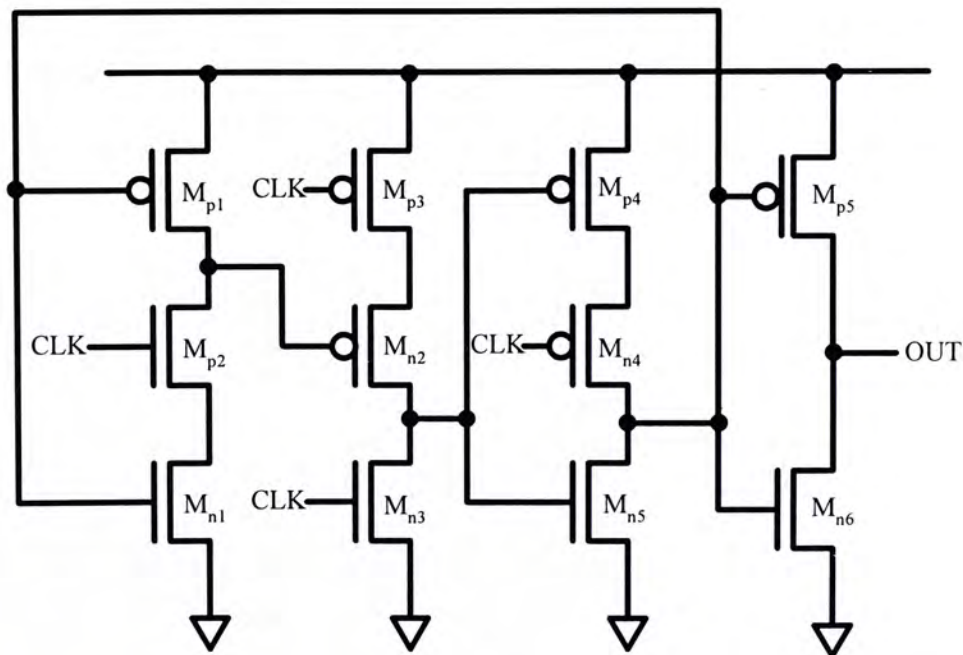


Figure 3.18: Schematic of the falling-edge-triggered TSPC divider Yuan and Svensson

Figure 3.19 shows another TSPC D-FF for high speed operation [20]. It can operate faster than the Yuan and Svensson's divider as the clock transistors are all tied to supplies. Since pseudo ring-shaped layout technique can be applied to the clock transistors which are usually large in size for high speed operation, less parasitics will be appeared in the internal nodes. However, it suffers much from charge sharing problem. When CLK keeps high and D changes from high to low instantly, M_{N1} turns off and M_{P1} turns on. Then $n1$ and $n2$ are sharing their charges through M_{P1} . At low frequencies operation, $n2$ has enough time to rise above the threshold voltage of M_{N2} . As CLK is high and M_{P1} is on, $n3$ discharges slowly which leads M_{P4} to turn on and Q_n (D) will rise up to high. As a result, the edge-triggering operation of the flip-flop is prevented and glitch will appear at the output which fails the divide-by-2 operation. This implies, however, there is a minimum clock speed of the dynamic divider.

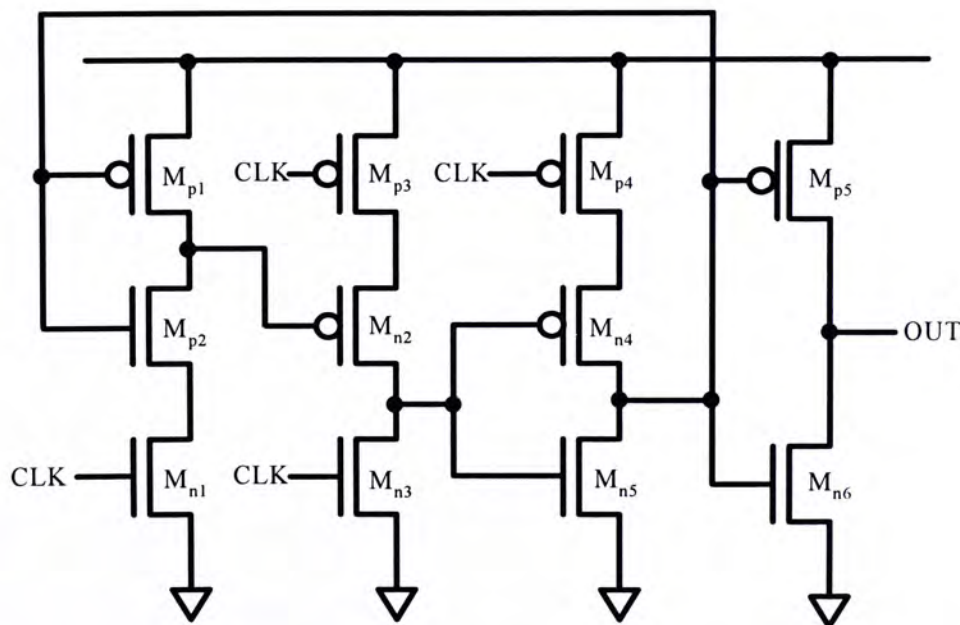


Figure 3.19: Schematic of the falling-edge-triggered TSPC divider proposed by Qguey and Vittoz

The operating speed of the TSPC dividers mentioned before is severely affected by the large RC delay due to the stacked structures. The effect of transistor sizing is not so evident because most transistors are drivers and loads at the same time. Although the propagation delay can be reduced by increasing the size of clocked transistors, it increases the load capacitance of VCO. As a result, a new TSPC divider is proposed applying ratioed logic so that the stacked structure in the latch can be removed [21]. At high frequency operation, the concept of static power consumption has little meaning because the transaction time of a signal takes a considerable portion of a clock period. Therefore, the ratio logic can replace the ratioless logic without paying much penalty on the power consumption.

In order to maintain the function as a latch, the devices sizing of ratio latch (Figure 3.20) is important. When CLK is high, the latch is in latching mode. The size of M_{n1} and M_{p1} are determined so that the voltage of the node n1 remains below the threshold voltage of M_{n2} , regardless of input D' which can be achieved by setting the size of M_{n1} much larger than that of M_{p1} . Thus pull-up or pull-down of the output Q' does not happen because M_{n2} and M_{p2} remain cut-off when the clock is high. As a result, the signal path from input D' to output Q' is not transparent.

When CLK is low, the latch enters sampling mode. If D' is low, node n1 is pulled up to V_{DD} by M_{p1} . Also, the pull-down strength of M_{n2} must be sufficiently larger than the pull-up strength M_{p2} , so that the output low voltage is lower than the input low voltage of the following gates (i.e. Q' is low). If D' is high, both M_{n1} and M_{p1} are turned off. Node n1 thus remains at the ground level which is its pre-charged state. Then the output Q is pulled up to V_{DD} by M_{p2} (i.e. Q' is high).

Figure 3.21 shows the schematic of the ratioed TSPC divider. In contrast to the conventional TSPC divider, only seven transistors are necessary. Since the number of

clock transistors is reduced and remove of stacked structure, the clock loading is reduced and the output driving ability is increased. It is worth to notice that the size of devices in each stage is progressively increasing since the output Q_n has to drive four transistors.

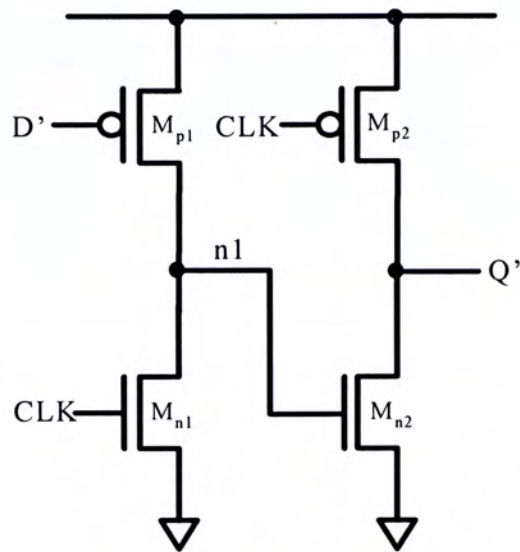


Figure 3.20: Schematic of a-ratioed latch

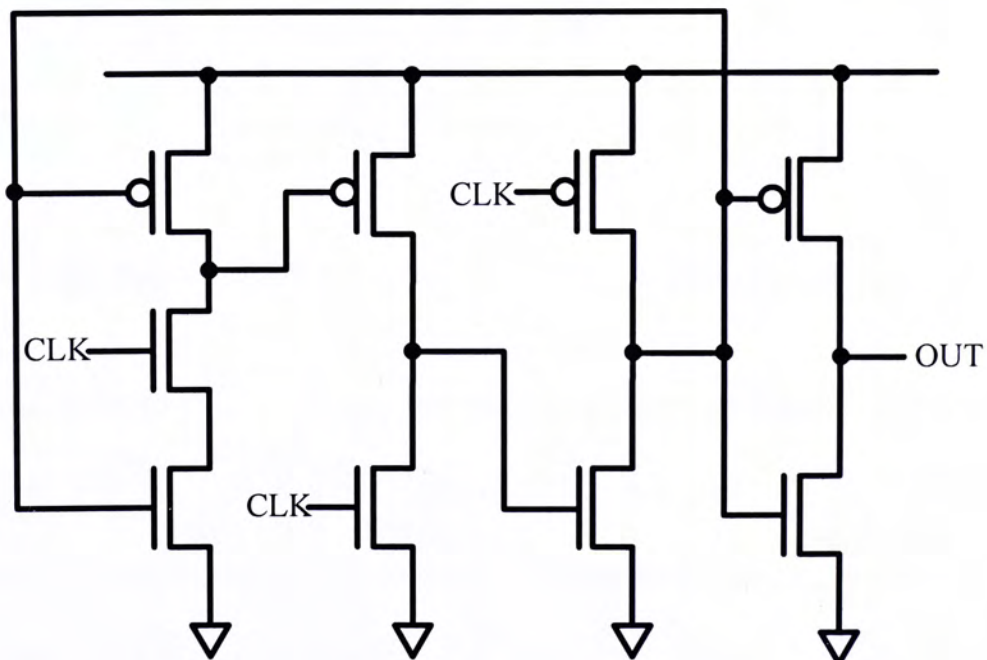


Figure 3.21: Schematic of a 7-transistor falling-edge-triggered TSPC divider

Further, a six-transistor TSPC divider (Figure 3.22) is proposed by replacing the N-C²MOS sampling part with a pseudo-NMOS inverter [22]. Since there are no stacked structures in the divider, the circuit can work faster and is more suitable for low voltage operation. However, in order to make the ratioed divider to operate correctly, careful design must be done to ensure that the NMOS transistors have larger pull-down capability than the pull-up capability of PMOS transistors. Besides, the high level of the input CLK must be larger than $V_{DD} - |V_{tp}|$ and the low level of it must be smaller than V_{tn} . Therefore, the minimum supply voltage is $|V_{tp}| + V_{tn}$.

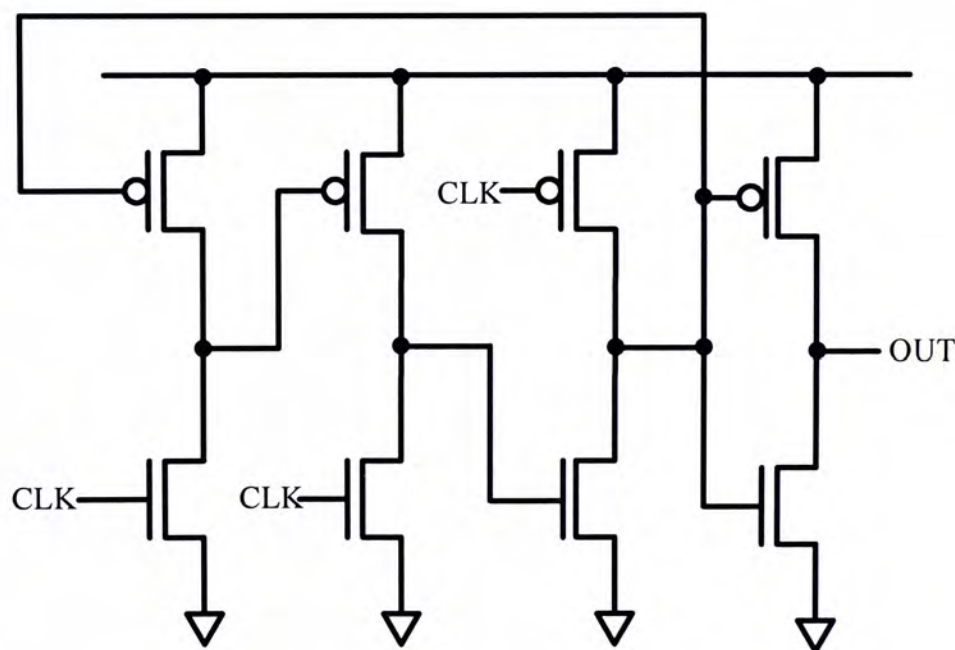


Figure 3.22: Schematic of a 6-transistor falling-edge-triggered TSPC divider

Compared with the SCL divider, the TSPC divider consumes less static power than SCL divider which makes it more power efficient for relative low speed applications. However, the TSPC require a larger amplitude input signals. Besides, TSPC divider cannot generate differential or multiple-phase outputs which make it not suitable for phase-switching implementation of DMP.

3.9 Summary

This chapter introduces the working principle, circuit analysis and implementation issues such as transistor sizing and layout considerations for SCL divide-by-2 circuit design. Besides, a brief review of different divider topologies, such as dynamic load SCL divider, multi-feedback SCL divider, injection-locked divider and dynamic TSPC divider is given.

Chapter 4

3V 900MHz Low Noise DMP

4.1 Introduction

PLL is a common block in mixed-signal designs and one of the major requirements of it is the low phase noise performance.

In mixed-signal design, the switching noise generated in the digital section affects the performance of the analog section. Great care has to be taken to reduce the coupling of switching noise from the digital circuitry to the analog counterpart through the supply lines and substrate. Several techniques were proposed to suppress supply noise by using filtering, guard-rings and separated on-chip power distribution networks for the analog and digital circuits. However, noise coupling cannot be eliminated completely in low-resistive substrate CMOS process.

Since the fundamental source for substrate noise is the supply current spikes during logic transitions, especially for high speed digital circuits. A more efficient way to minimize supply noise injection is using low-noise logic families based on their current steering method that has relatively constant power supply current and the reduced internal swings. One possible low noise digital circuit technique is the SCL. Besides of generating less supply noise, SCL also has better noise immunity.

Figure 4.1 gives the linear time-invariance (LTI) continuous time model of the PLL with individual output-referred noise sources. For the PLL, there are several possibilities of noise injection into the loop. Table 4.1 lists various noise sources in the loop of PLL and their corresponding transfer functions.

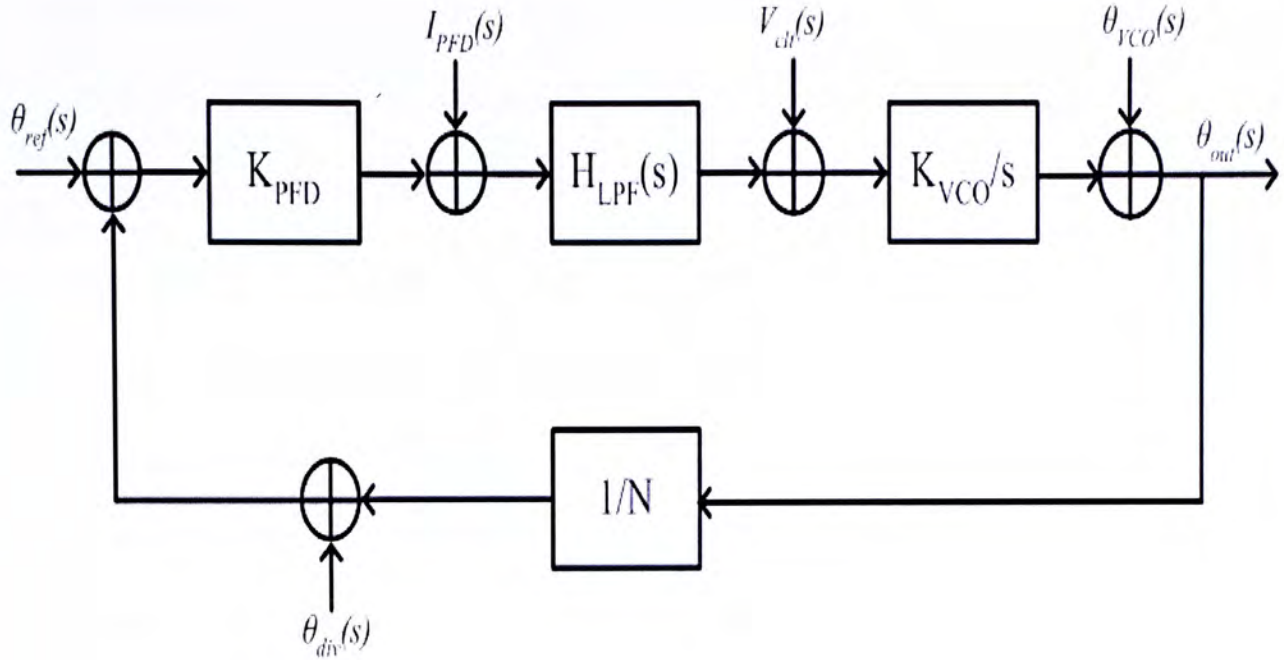


Figure 4.1: LTI model of PLL

	Phase transfer function		
Reference noise	$\theta_{out}(s) / \theta_{ref}(s)$	$\frac{NK_{PFD}K_{VCO}H_{LPF}(s)}{Ns + K_{PFD}K_{VCO}H_{LPF}(s)}$... (4.1)
PFD/CP noise	$\theta_{out}(s) / I_{PFD}(s)$	$\frac{NK_{VCO}H_{LPF}(s)}{Ns + K_{PFD}K_{VCO}H_{LPF}(s)}$... (4.2)
LF noise	$\theta_{out}(s) / V_{LPF}(s)$	$\frac{N \cdot K_{VCO}}{Ns + K_{PFD}K_{VCO}H_{LPF}(s)}$... (4.3)
VCO noise	$\theta_{out}(s) / \theta_{VCO}(s)$	$\frac{N}{Ns + K_{PFD}K_{VCO}H_{LPF}(s)}$... (4.4)
Divider noise	$\theta_{out}(s) / \theta_{div}(s)$	$\frac{NK_{PFD}K_{VCO}H_{LPF}(s)}{Ns + K_{PFD}K_{VCO}H_{LPF}(s)}$... (4.5)

Table 4.1: PLL phase noise transfer function

where

θ_{ref} : reference noise

θ_{out} : PLL output phase noise

θ_{VCO} : VCO output phase noise

θ_{div} : phase noise generated by the integer-N-divider

I_{PFD} : current noise associated with PFD/CP

V_{cft} : voltage noise generated by loop filter

K_{PFD} : gain of the PFD and CP, with the unit of A/rad

K_{VCO} : gain of the VCO, with the unit of Hz/V

$H_{\text{LPF}}(s)$: transimpedance of the loop filter

Equations 4.1 and 4.5 show the magnitude response of reference noise is the same as the noise from integer-N-divider. Also, from equation 4.2, the noise at the output of PFD and CP can simply be input-referred and combined with the reference and divider noise divided by the PFD gain.

It is found that both of the noise transfer functions of reference, PFD and CP have low-pass characteristics (see equation 4.1, 4.4 and 4.5) while that of VCO has a high-pass characteristic (equation 4.4). Therefore, phase noise close to the carrier is dominated by the noise from the reference, PFD and divider, while the phase noise far from the carrier is the mainly dominated by the VCO.

To achieve an optimal noise performance, the loop bandwidth should be optimized to mitigate the total output noise. However, the loop bandwidth is limited by typically one-tenth of the reference frequency in order to obtain a stable loop response. The loop bandwidth is also limited to obtain significant attenuation of the reference spurs. A higher order loop filter is usually used for the design of PLL in order to reduce more noise and spurs with more degrees of design freedom.

As long as the PLL maintains stable, a large bandwidth is always preferred to obtain faster settling response. However, the loop bandwidth can only be extended if

the divider, PD and reference noise multiplied by the division ratio N does not exceed the noise of VCO. As a result, it is preferable to reduce the prescaler noise, especially for wideband PLL designs. Besides, it is also important to minimize the noise coupling to itself and other sensitivity analog blocks, such as CP and VCO. One solution is implementing the prescaler by using differential SCL divider. Indeed, many fully differential PLL designs have been published aimed to reduce its sensitivity to noise and to generate less jitter [23-27].

In this chapter, a new approach based on the SCL divider and pre-processing clock technique in a differential configuration is proposed for DMP implementation. The constant-current characteristic of the SCL divider exhibits relatively constant supply current with reduced switching noise, which is beneficial to PLL operation.

4.2 Proposed DMP Topology

As mentioned in Chapter 2, there are three different DMP architectures: conventional architecture, pre-processing clock architecture and phase-switching architecture. Since pre-processing clock DMP operates faster than the conventional DMP and does not have to deal with the glitch problem in phase-switching architecture, it is picked as the architecture in this design.

There are two options in implementing the divider, namely: SCL divider and TSPC divider. In principle, the TSPC design offers lower power consumption due to the absence of a direct path between the power supply and ground rails. However, the output voltage swing of the SCL circuit is much less than the rail-to-rail logic level which allows the flip-flop to operate at even higher frequency. Both SCL and TSPC divider circuits were simulated (Fig. 4.2 - 4.3) to study the supply noise issue.

They are both operating at the same conditions (3V supply voltage and 900MHz) for fair comparison. Table 4.2 indicates that the current ripples (peak-to-peak value) associated with the TSPC circuit is at least four times larger than that of the equivalent SCL design.

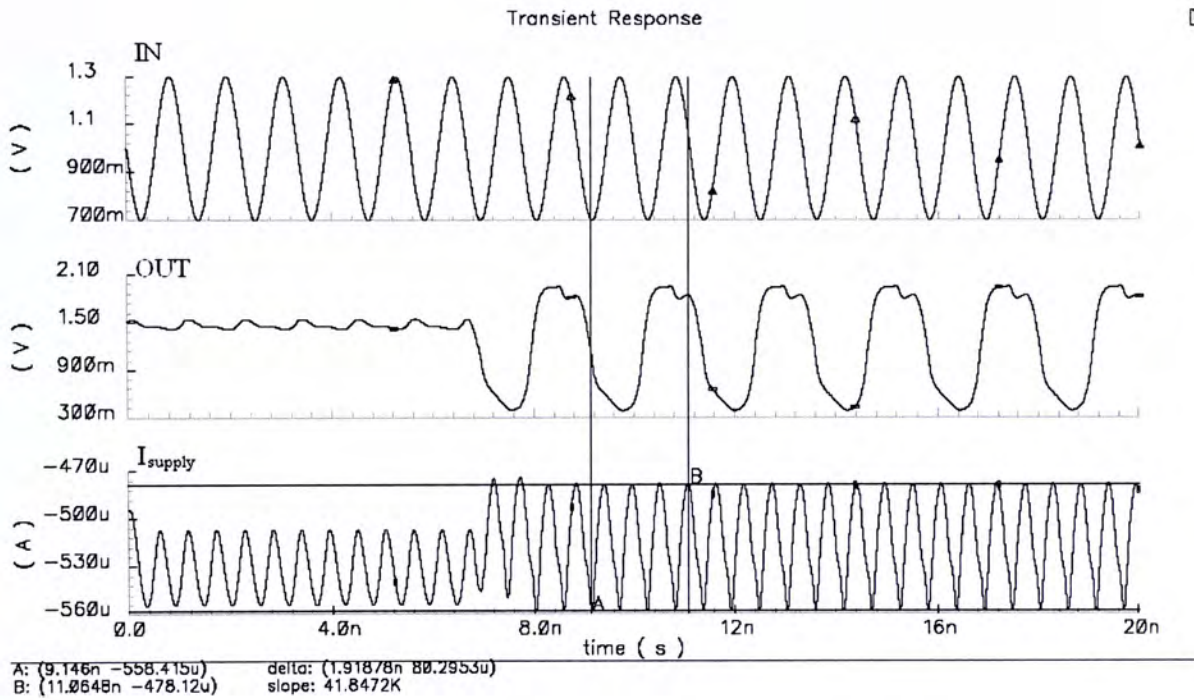


Figure 4.2: Simulation results: SCL divider

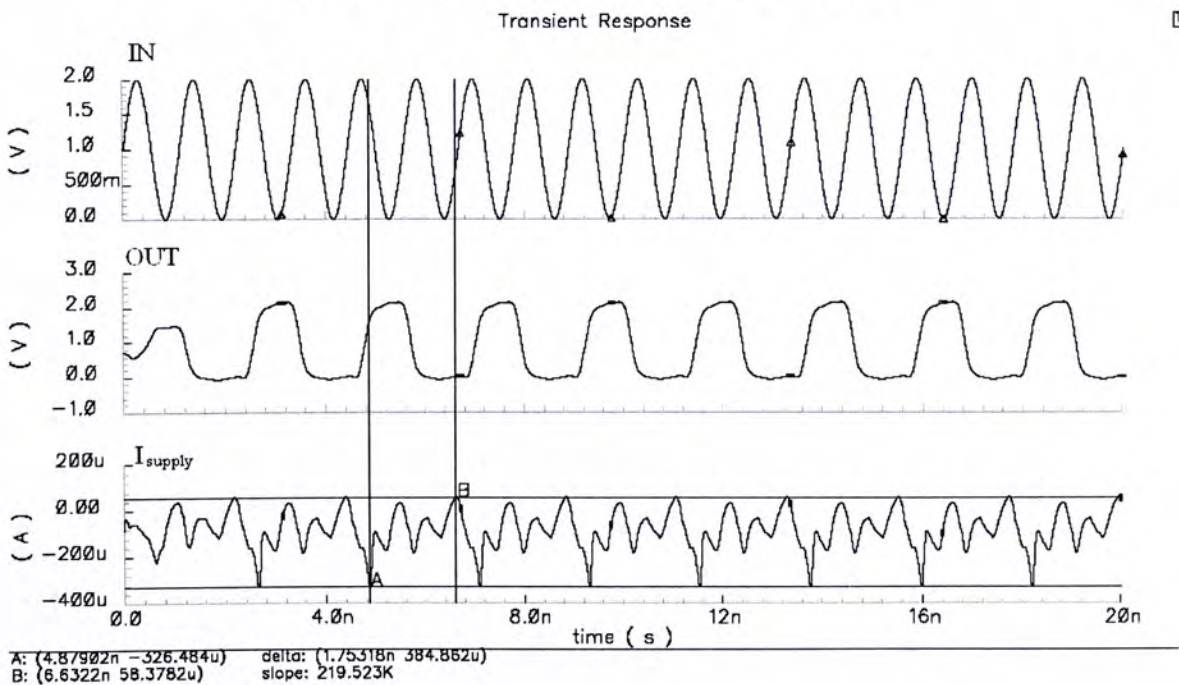


Figure 4.3: Simulation results of TSPC and SCL divider

	TSPC divider	SCL divider
Current Variation /μA	384.85	80.30

Table 4.2: comparison on current variation of TSPC and SCL divider

Since the pre-processing clock architecture in [5] is single-ended, differential pre-processing clock architecture is therefore proposed to reduce the noise generated and achieve a better noise immunity.

An intuitive differential implementation of pre-processing clock DMP is illustrated in Figure 4.4 where the upper feedback logic is exactly the complement of the lower feedback logic.

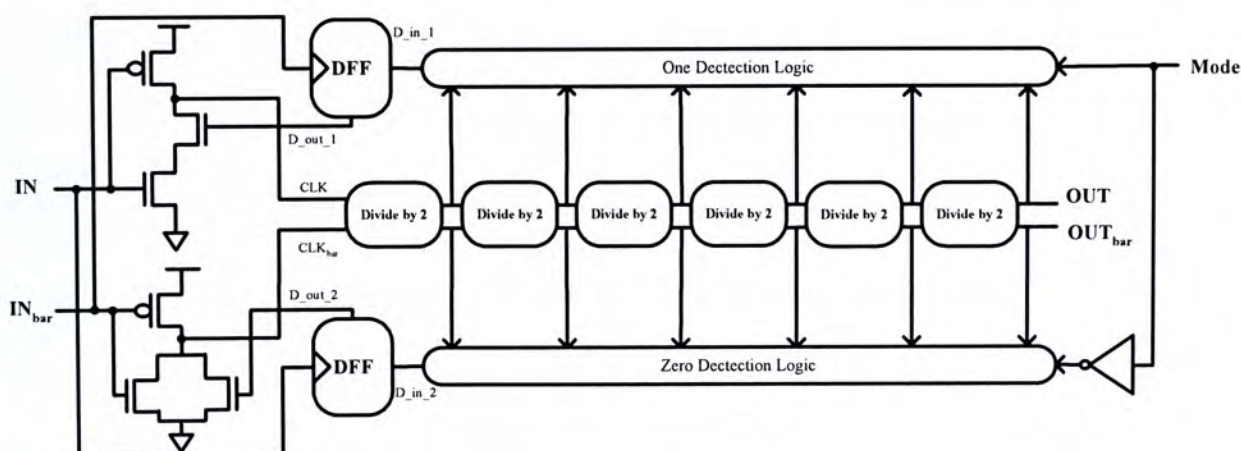


Figure 4.4: Differential implementation of the pre-processing clock DMP

In the proposed DMP architecture, all the D flip-flops are chosen to be differential types. Note that the speed limitation of divider circuits is, in general, governed by the operating speed of the logic gates in the feedback path rather than the divide-by-2 stage since the feedback logics are needed to generate short-duration pulses for certain period. As a result, a feedback path design with smaller number of logic gates will offer a speed advantage. This is achieved by sharing part of logic using one feedback instead of two as shown in Figure 4.5. It also offers better noise

performance with less switching action, less circuit complexity, smaller die size and lower power consumption.

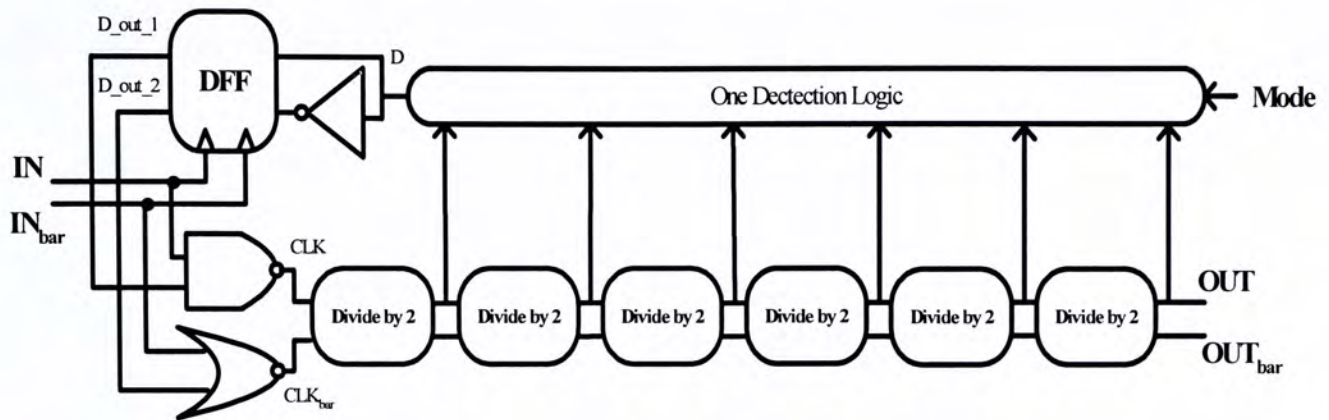


Figure 4.5: Differential implementation of the pro-processing clock DMP with shared feedback logic

4.3 Circuit Design and Implementation

Figure 4.6 shows you the SCL latch used in this design. The conventional SCL latch is applied because it exhibits relatively constant total current level and better noise rejection performance due to its differential and stacked structure. Minimum gate length is applied to all transistors to minimize parasitic capacitance except for the current sources. By using long channel devices for current source, higher impedance at the common-source node of M_{n5} and M_{n6} can be obtained due to the minimized effect of channel-length modulation. A better common-mode noise and power supply noise rejection is therefore achieved. Furthermore, the circuit can be viewed as a ring oscillator if there is no input signal. The free-running frequency given as:

$$f = \frac{1}{4 \times \tau_D}$$

where τ_D is the propagation delay of the D-Latch. Note that optimal operation (highest input sensitivity) occurs when the individual divide-by-2 stage is self-oscillating at half of the input frequency.

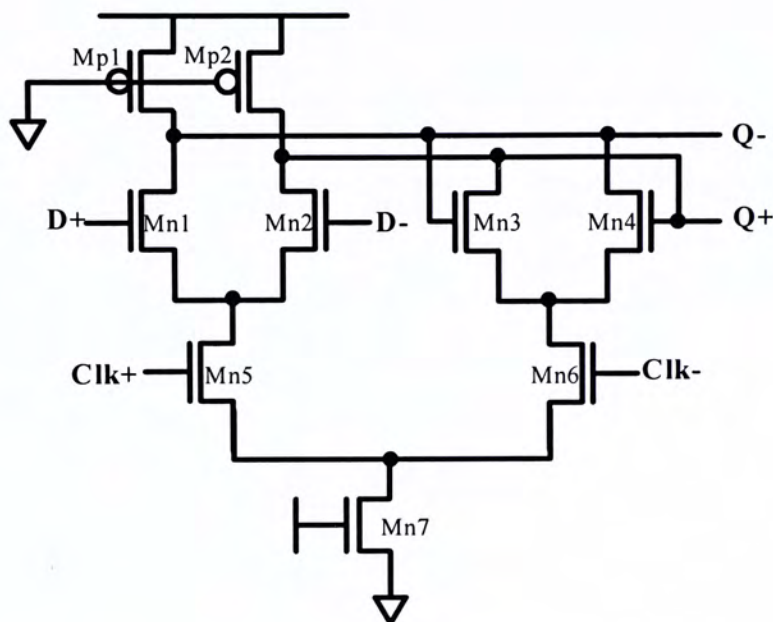


Figure 4.6: Schematic of the SCL latch

Since an inverter is inserted to convert the single-phase output from the “One Detector” into a differential signal, a time delay difference (τ_1) will appear at the input of the DFF which synchronize the input with the clock for proper logic operation. The condition for its proper operation is given below:

$$\tau_1 \ll T_m$$

where T_m is the period of the input clock. The operation of the differential DFF is demonstrated by simulation as shown in Figure 4.7. Note that the devices in the “One Detector” should be kept as small as possible so that loads appeared at the

differential outputs of divide-by-2 stages are the same. Note that dummy gates are added to maintain the balanced condition if necessary.

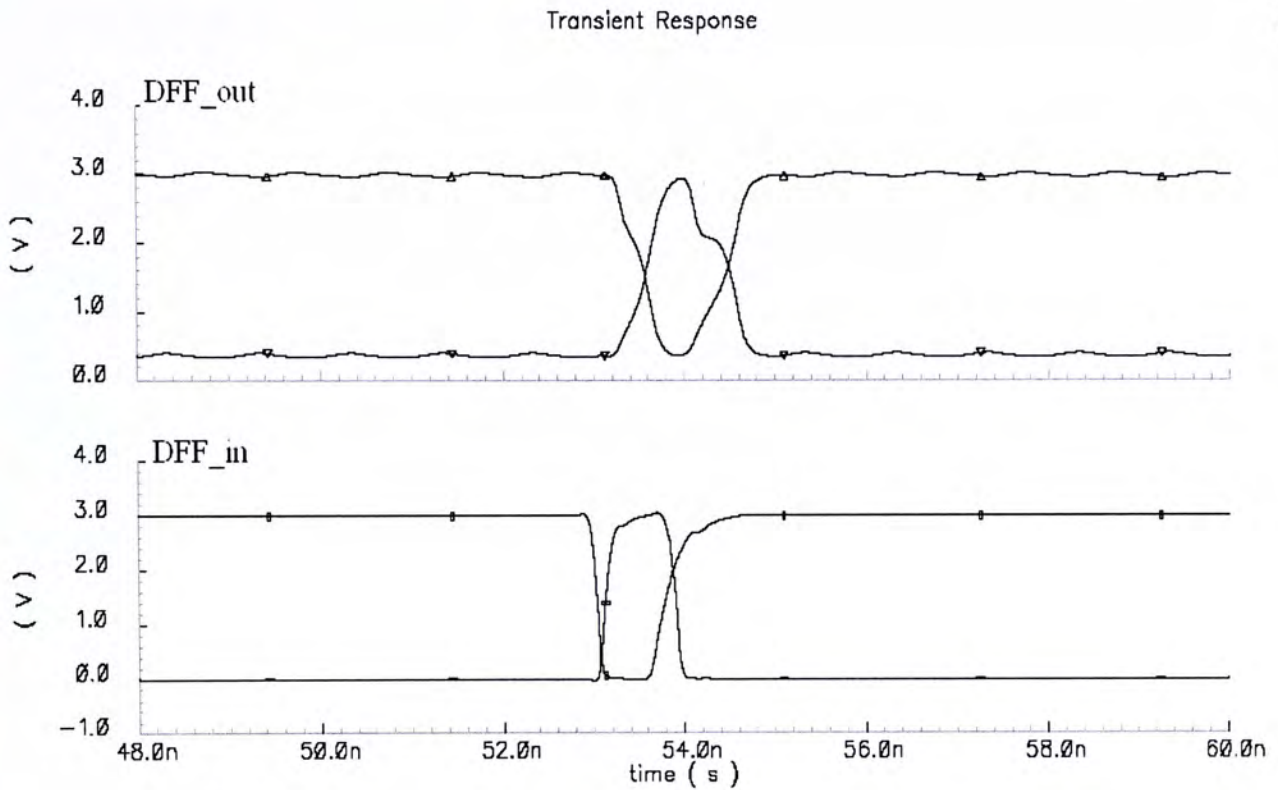


Figure 4.7: Operation of the DFF

4.4 Simulation Results

The DMP is finally integrated with a LC VCO to verify its operation. Figure 4.8 shows the relationship between the differential VCO output and the pre-processed clock signal. It can be shown that there is one pulse removed for the pre-processed clock signal when the DMP is operating at the mode of divide-by-65. Figure 4.9 shows you the simulation results of the DMP output, which is a divide-by-65 version of the input (VCO output).

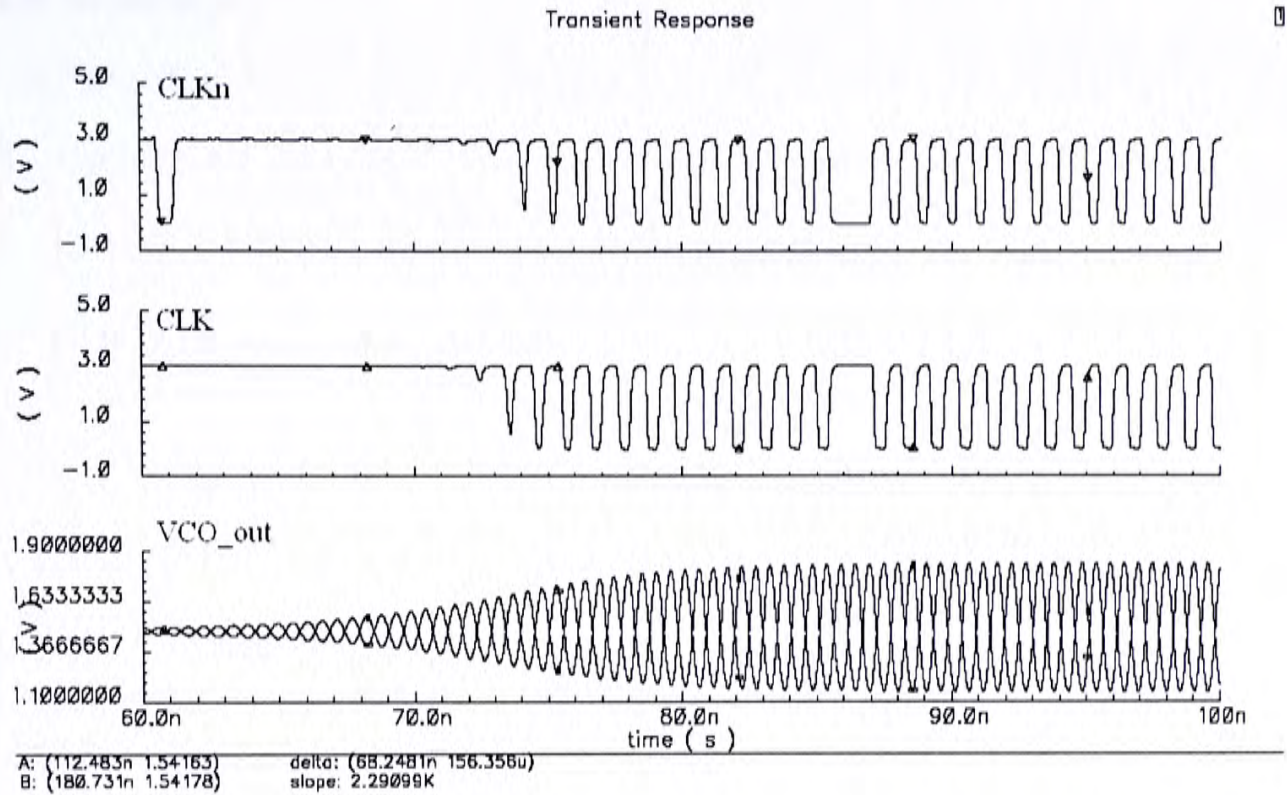


Figure 4.8: Relationship between the VCO output and the pre-processed clock

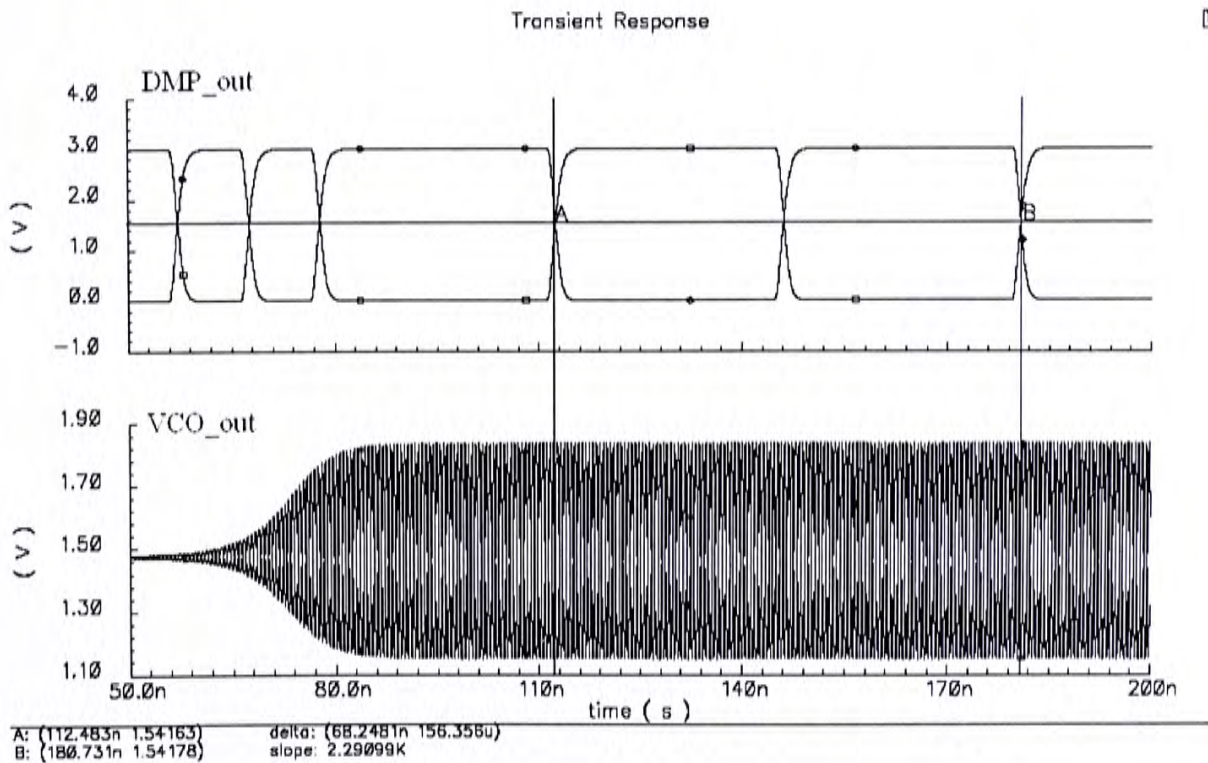


Figure 4.9: Waveforms of VCO output and DMP output for divide-by-65 operation

4.5 Summary

A high-speed 64/65 dual-modulus prescaler for PLL application has been designed. The flexibility of using differential architecture with pre-processing clock technique for attaining low supply noise performance is demonstrated. The circuit operates well at 900MHz with a 3V supply voltage.

Chapter 5

1.5V 2.4GHz Low Power DMP

5.1 Introduction

The increasing prominence of portable systems has led to rapid developments in low power design during the recent years. The reason is obvious because it helps to stretch the battery life of portable products and to increase the circuit reliability. Since lower heat is generated in low power design, it ensures the device performance and prevents it from failure.

The total power consumption of conventional CMOS digital circuits can be expressed as sum of three main components, namely: the dynamic power consumption, the leakage power consumption and the short-circuit power consumption, as shown in the following equation:

$$P_{\text{total}} = \alpha f C V_{\text{DD}}^2 + I_{\text{leak}} V_{\text{DD}} + I_{\text{short}} V_{\text{DD}} \quad \dots(5.1)$$

where

f: operating frequency

C: output capacitance

V_{DD} : supply voltage

I_{leak} : leakage current

I_{short} : short circuit current

α : effective number of power-consuming transitions per clock cycle

Equation 5.1 suggests that the power consumption can be reduced by decreasing the supply voltage. For high speed digital circuit, dynamic power consumption is dominant among the three terms. (i.e. $P_{\text{total}} \approx \alpha f C V_{\text{DD}}^2$). As a result, the effect of power reduction due to decreased supply voltage becomes more significant. Intuitively, the supply voltage of the digital circuitry in a mixed-signal system should be as low as possible because low voltage means low power for digital circuit. Another motivation for low voltage design is the low drain-source voltage requirement due to the trend of device scaling. It avoids transistors from irreversible breakdown.

In PLL, prescaler is indeed an ultra-high speed digital circuit. Higher performance (high frequency operation with less power consumption) is possible to be achieved by decreasing the supply voltage. However, the design of low voltage prescaler is a challenging task since the threshold voltage of transistor does not scale down much compared to the scaling on supply voltage. Besides, an inevitable trade-off of reducing supply voltage is the increasing of delay.

Another challenge for low power DMP design is the lack of accurate transistor RF-models. The RF-models provided by AMS have the limitation that the width of transistors should be multiple of $5 \mu\text{m}$ which is not very useful for DMP design since small size transistors are usually used. As a result, circuit performance cannot be predicted precisely at high frequencies. To have a reliable design, designer need s over-design to overcome this limitation and over-design requires extra power consumption.

In this chapter, a 2.4GHz DMP is proposed with low supply voltage (1.5V) based on the phase-switching architecture. New design techniques are adopted to maintain high-speed operation with ultra low power consumption.

5.2 Proposed DMP Topology

Fig. 5.1 shows the functional block diagram of proposed phase-switching DMP that consists of a divide-by-4 circuit, a divide-by-16 circuit, a phase-selection network and control logic. When Mode=1, the phase-selection network is disabled and the DMP simply acts like an asynchronous divide-by-64 ripple counter. However, when Mode=0, an additional delay of one clock period will be introduced by the switching network for every output cycle and a dividing ratio of 65 is resulted.

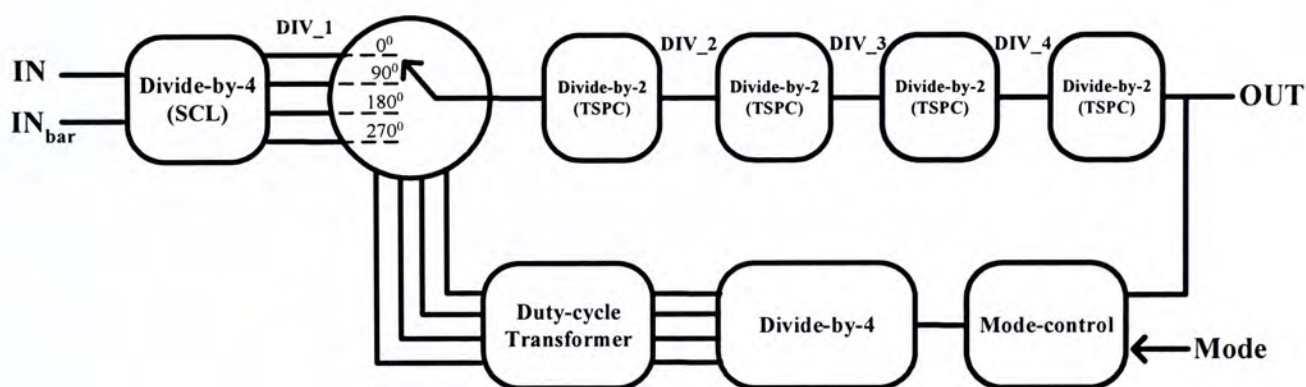


Figure 5.1: Block Diagram of Phase-switching DMP

The phase switching is applied after the divide-by-4 outputs instead of after the divide-by-2 output. It reduces the operating frequency of the phase-selection network and the feedback logics and thus reduces the power consumption. The divide-by-4 circuit is conventionally performed by a pair of SCL divide-by-2 circuits. The operating speed of it depends on the speed of the first divider. Such digital divider is wideband but is very power hungry at high operating speed. Analog injection-locking dividers and regenerative dynamic dividers provide solutions to overcome the speed limitation with the drawback of large size due to the use of passive inductors and reduced bandwidth.

In this design, a sub-harmonic injection-locking inductor-less ring oscillator

divider is applied to the full-speed divider. This divider is exactly the half-speed SCL divide-by-2 stage operating at the mode of divide-by-4. The inherent quadrature phase output of this divider makes it fits the design of phase-switching DMP. Another advantage of this architecture is that no pre-amp stage is used as the input sensitivity of SCL divider is very high leads to low power consumption. For further power reduction, the divide-by-16 circuit is implemented by using single-ended TSPC logic.

Traditionally, a 2-bit finite-state machine (FSM) (Figure 5.2) is used to generate the switching control signals with a 4-to-1 multiplexer (MUX) (Figure 5.3) which consists of three 2-to-1 MUX. Figure 5.4 and Figure 5.5 shows the two common implementations of 2-to-1 MUX, however, both of them require differential input, S and \bar{S} . Although the differential phase control input can be obtained by adding an inverter, signal race problem may occur for high frequency operation. Similarly, the delay between S_0 and S_1 in FSM also causes signal race problem.

In this design, a divide-by-4 stage is used to replace the 2-bit FSM. There is no signal race problem for the phase-control signals since it generates four 90° -spaced phases simultaneously. The output of the divide-by-4 stage then is fed to a duty-cycle transformer to generate four non-overlapping clocks for the MUX. A 4-to-1 MUX is used to provide the phase switching function.

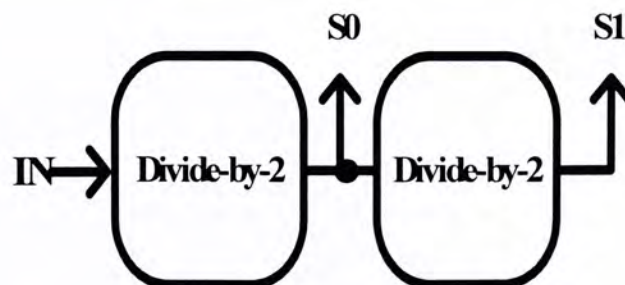


Figure 5.2: Block diagram 2-bit FSM

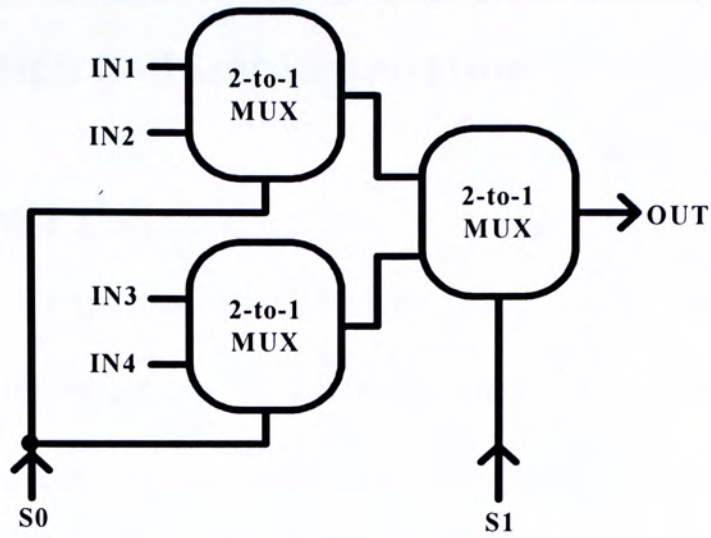


Figure 5.3: Block diagram 4-to-1 MUX

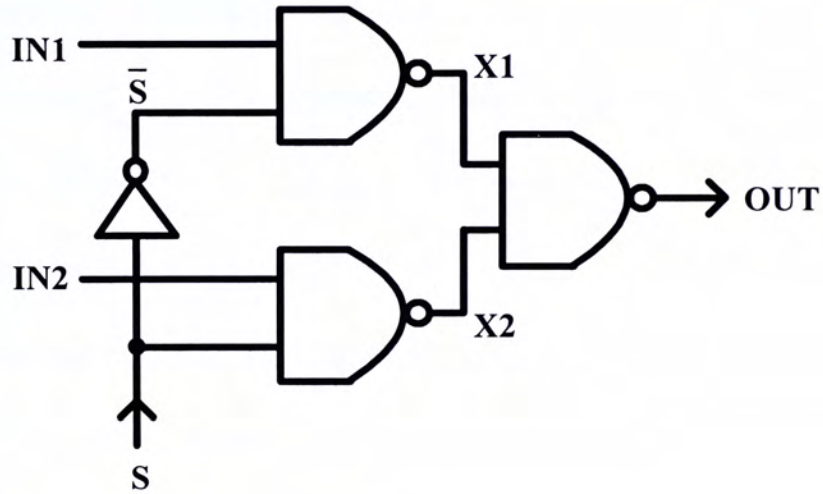


Figure 5.4: NAND gate implementation of 2-to-1 MUX

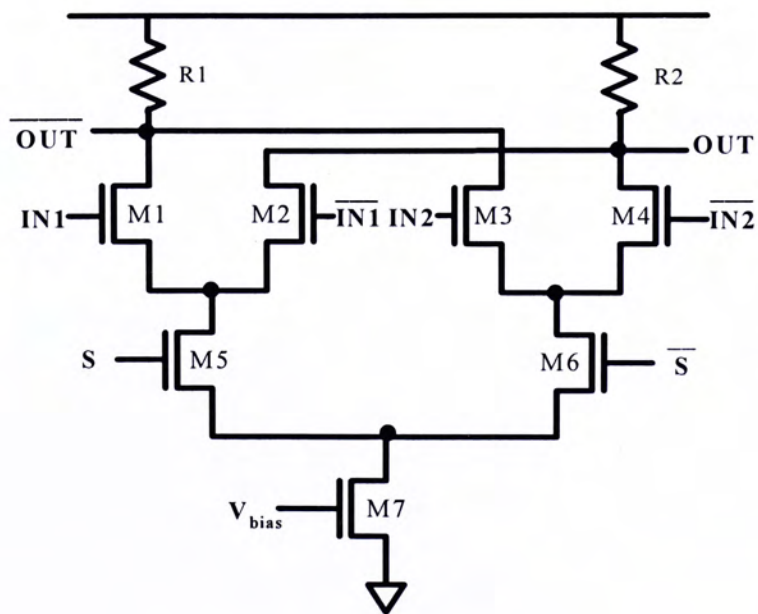


Figure 5.5: SCL 2-to-1 MUX

5.3 Circuit Design and Implementation

5.3.1 Divide-by-4 stage

The divide-by-2 circuit basically consists of two SCL latches (Figure 5.6) connected in a master-slave configuration with negative feedback. Note that the current source in conventional SCL latch is removed for low voltage operation. One advantage of the SCL divider is its limited output swing which leads to low power consumption for high frequency operation ($P_{\text{total}} \approx \alpha f C V_{\text{swing}} V_{\text{DD}}$). If these two flip-flops are clocked in-phase rather than opposite-phase, the dividing ratio is doubled [28]. Similar to injection locked divider, the output can be synchronized by the input and the circuit can be operated as a divide-by-4 stage if the input clock frequency falls to the stable regions. However, the synchronous phenomenon of it is due to both the analog injection-locking characteristic and the digital synchronization property of flip-flop which enable it to operate properly for very wide bandwidth. Note that the number of transistors required and power are reduced at the expense of the operating bandwidth. Fortunately, for most RF systems, narrowband operation (a few hundred MHz or less) is usually sufficient to fulfill the requirement and to accommodate process variations. Figure 5.7 shows the simulated waveforms of the full-speed divider.

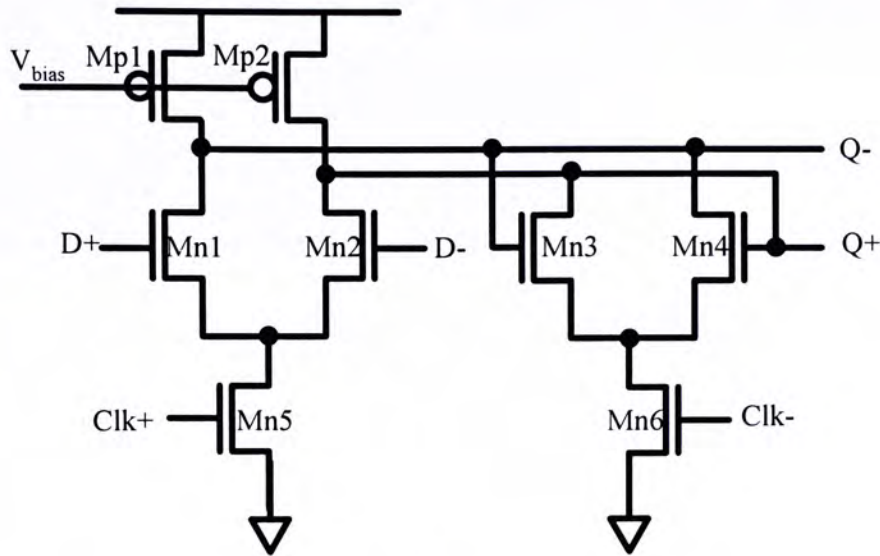


Figure 5.6: Schematic of low voltage SCL latch

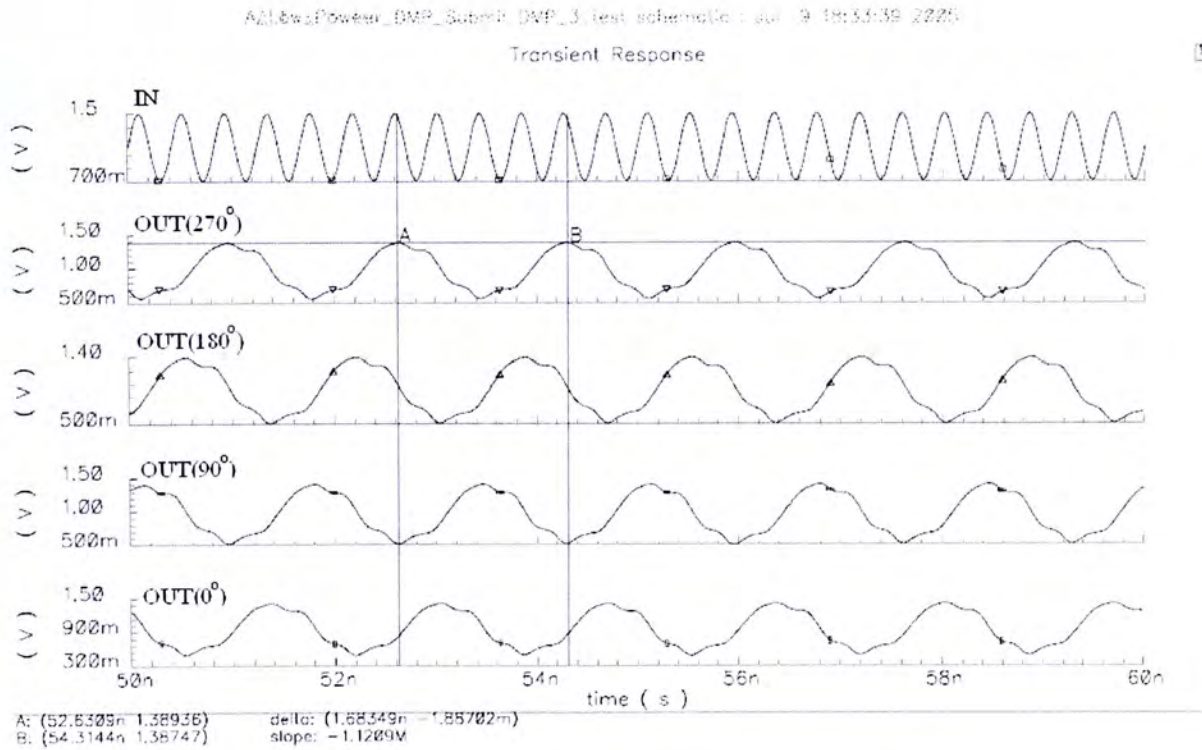


Figure 5.7: Simulation results of the full-speed divide-by-4 stage

Furthermore, a divide-by-4 stage is adopted to provide the required quadrature output with single-ended input in the feedback logic. Due to the lack of differential input, the above divider is not suitable for the feedback divider. Since current can either flow through the sensing pair or the latching pair, current switching can be implemented by using a single switch to make the circuit operate well with

single-ended input. Although either Mn5 or Mn6 can be removed, removal of Mn6 is preferred for low voltage operation. It is found that the circuit functions properly even though Mn6 is removed, provided that the input swing is sufficiently large to maintain proper current-switching level. The schematic of the feedback divider is shown in Figure 5.8. Figure 5.9 shows the simulated waveforms of the feedback divider.

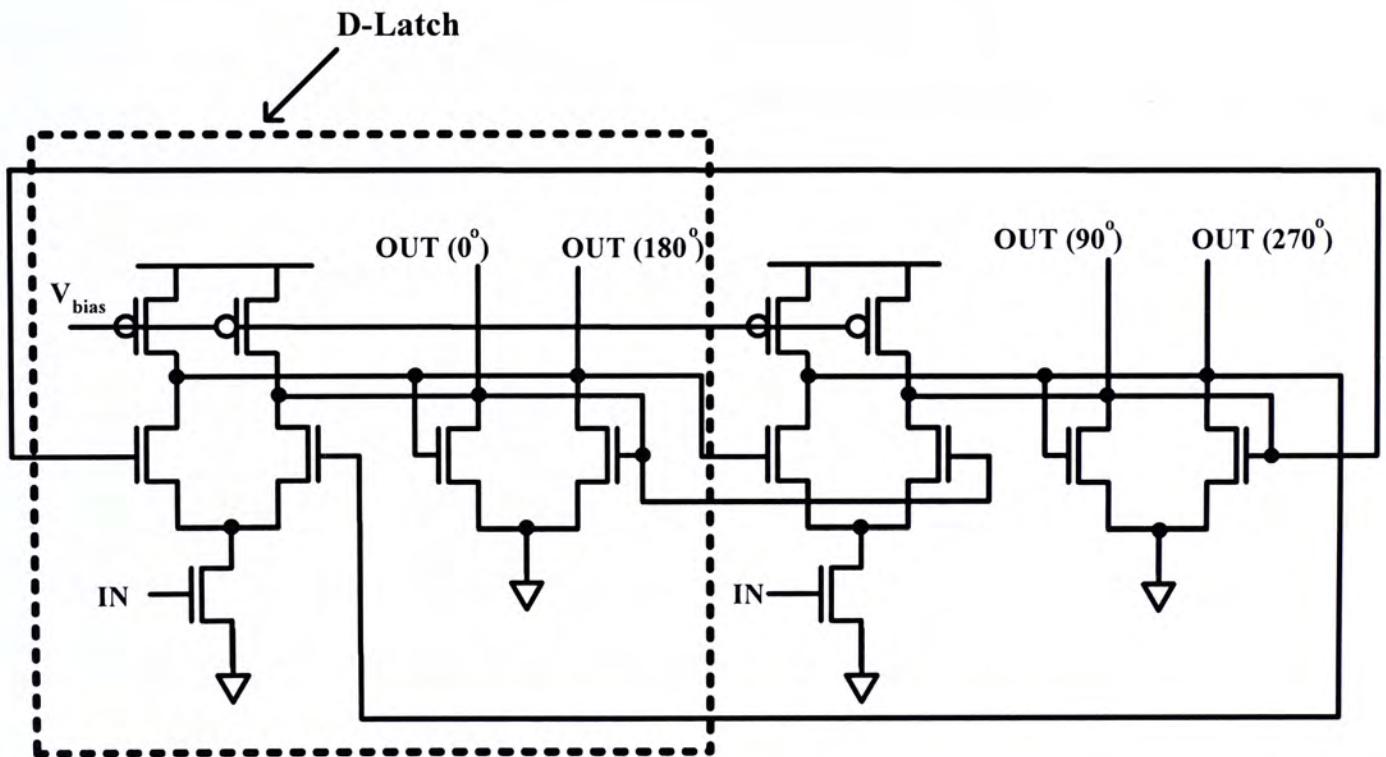


Figure 5.8: Schematic of the feedback divide-by-4 stage

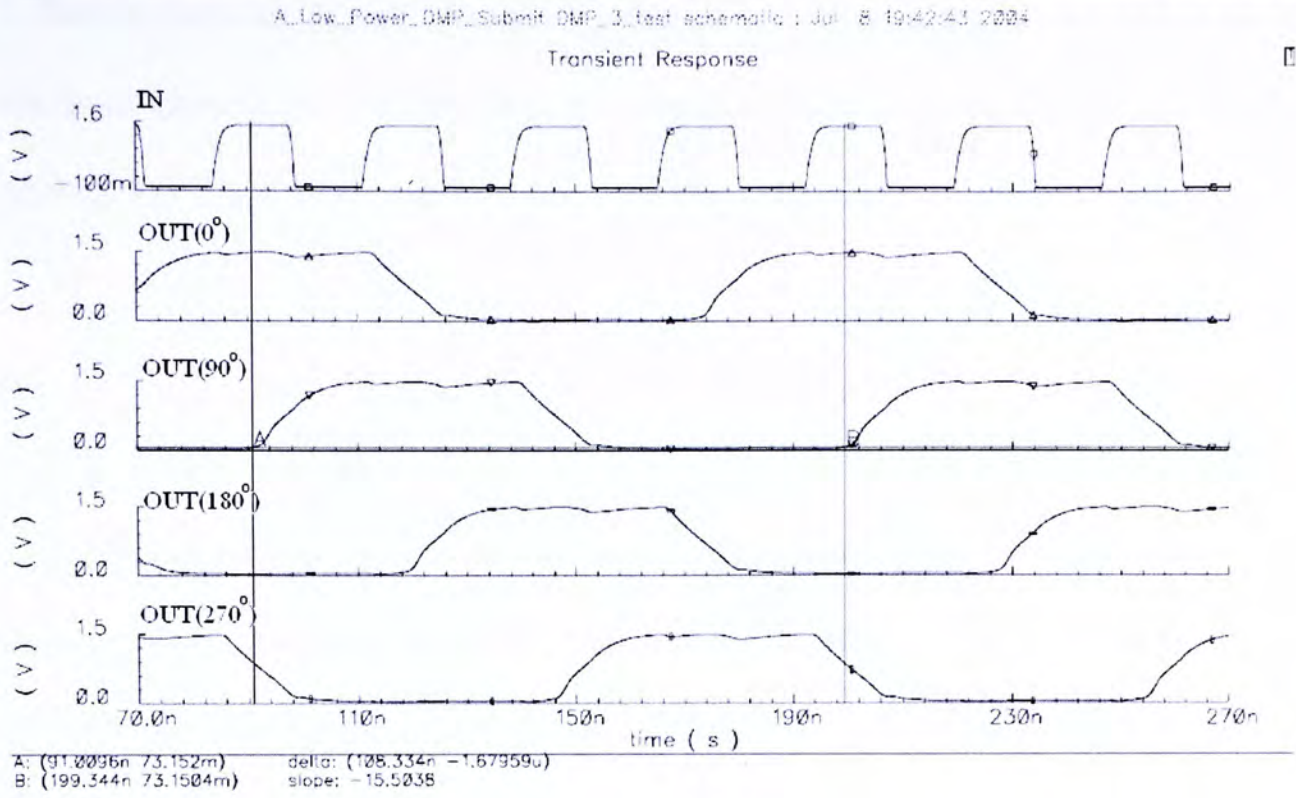


Figure 5.9: Simulation results of the feedback divide-by-4 stage

It is always difficult tasks to design a very high speed SCL divider (i.e.: the full-speed divider) and a very low speed SCL divider (i.e.: the feedback divider), but it can be done by proper transistor sizing of the sampling part (Mn1, Mn2 & Mn5) and the latching part (Mn3, Mn4 & Mn6). For the low speed divide-by-4 stage, long channel devices are used to achieve a low speed operation by increasing the output capacitance. Table 5.1 summarizes the design parameters of the two dividers.

	Mp1/Mp2	Mn1/Mn2	Mn3/Mn4	Mn5	Mn6
Full-speed	3 μ /0.35 μ	4 μ /0.35 μ	2 μ /0.35 μ	3 μ /0.35 μ	1.5 μ /0.35 μ
Divide-by-4					
Feedback Divide-by-4	1 μ /3 μ	1 μ /1.5 μ	1 μ /0.35 μ	1 μ /1.5 μ	--

Table 5.1: Device sizing of the full-speed divider and feedback divider

For the transistor layout, pseudo ring-shaped layout technique is used to minimize the drain capacitance contributed to the output nodes for high speed and low power operation ($P_{\text{total}} \approx \alpha f C V_{\text{DD}}^2$).

5.3.2 TSPC dividers

To further reduce the power dissipation, the remaining divide-by-16 circuit is implemented by using single-ended TSPC logic. It consists of four TSPC divide-by-2 stages in cascade configuration. Since the first TSPC divide-by-2 works at around 600MHz which frequency is still high, the seven-transistor ratioed divider is applied. More importantly, the input loading of this divider is smaller since there are only three clock transistors instead of four in conventional nine-transistor divider implementations. As the following divide-by-2 stages have much relaxed speed requirements, the Yuan and Svensson's dividers are applied to reduce the static power consumption.

5.3.3 Phase-selection Network

An active low switching-amplifier 4-to-1 MUX is used to provide the phase switching function. The schematic of the 4-to-1 MUX is shown in Figure 5.11 which consists of 4 switching amplifier stages connected in parallel.

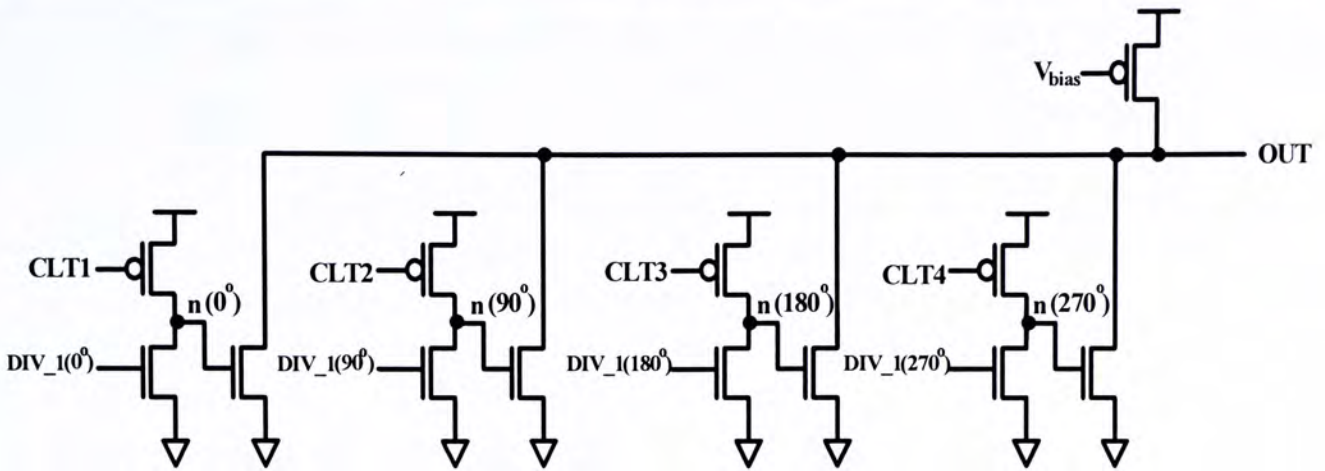


Figure 5.10: Schematic of the phase-selection network

5.3.4 Mode-control Logic

There are two possible ways to implement the mode control logic, as shown in Figure 5.12 and Figure 5.13 respectively. One uses a NAND gate cascaded with an inverter and another applies an inverter cascaded with a NOR gate. Although they have exactly the same function, the later seems is preferred because the loop delay of the DMP contributed by the inverter is outside the feedback loop which results a faster settling time of DMP.

When Mode = '1', the output of the mode-control logic is an inverted version of the input (i.e. OUT in DMP). When Mode = 0, the output of the mode-control logic equals to 0 which turns off all the current sources in the feedback divider. As a result, the feedback path is disabled and the output of the feedback divider is hold as that in pervious stage.

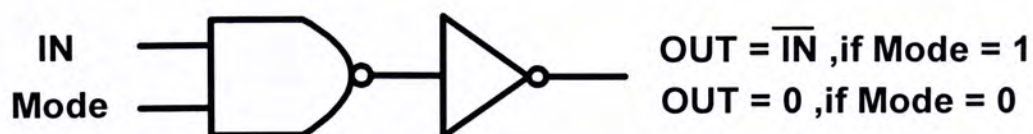


Figure 5.11: One possible implementation of the mode-control logic

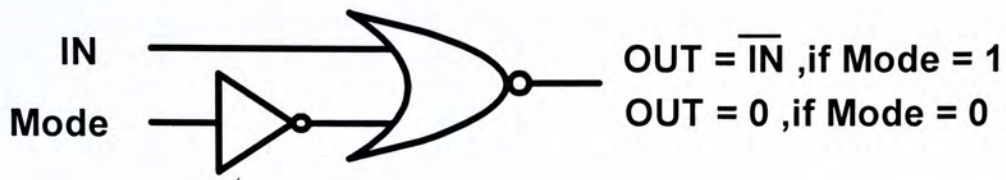


Figure 5.12: Another possible implementation of the mode-control logic

5.3.5 Duty-cycle Transformer

Moreover, a duty-cycle transformer is added to convert the divider output from 50% duty-cycle to the required 25% duty-cycle. It generates four non-overlapping clocks for the MUX. Figure 5.14 shows the logic design of the transformer and Figure 5.15 shows the corresponding output waveforms.

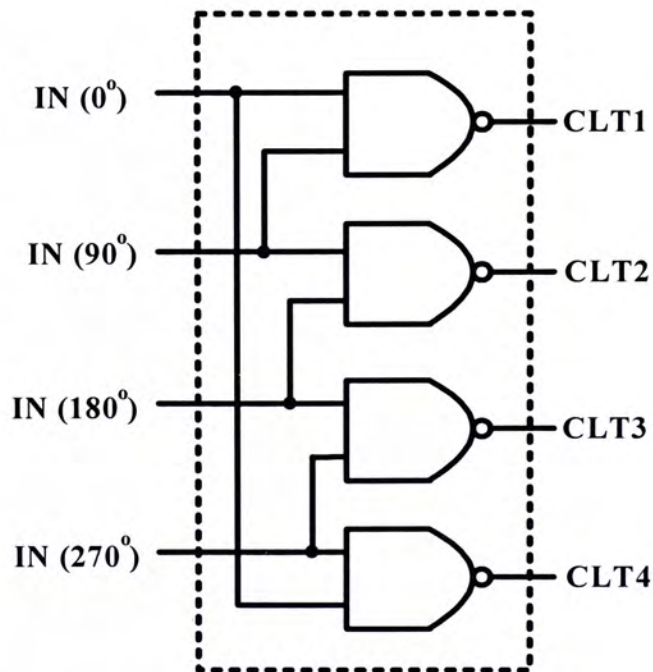


Figure 5.13: Logic implementation of duty-cycle transformer

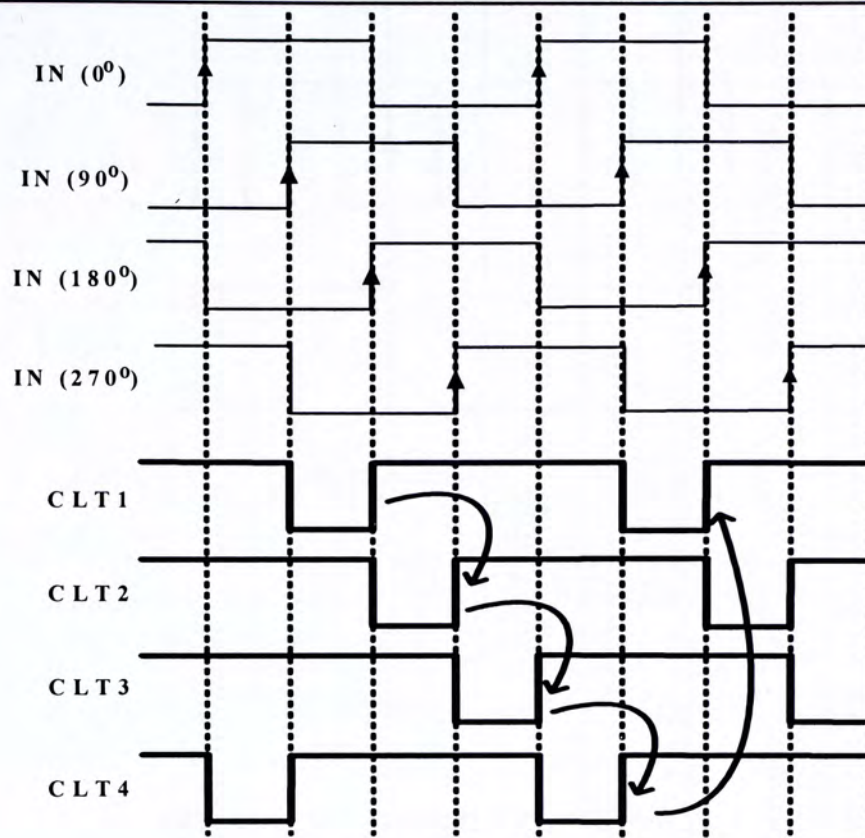


Figure 5.14: Waveform diagram of the duty-cycle transformer

5.3.6 Glitch Problem

Although the phase-switching technique seems to be an attractive solution for DMP design, it usually suffers from the glitch problem as illustrated in Figure 5.15. Improper switching can introduce undesirable transition and counting error. Much effort has been devoted in the past to tackle this problem. To tackle this problem, re-timing circuitry [29] and synchronization flip-flop [30] are usually added which leads to increased power consumption. Besides, additional feedbacks are added to the MUX in [31] to solve the glitch problem with reduced operating speed.

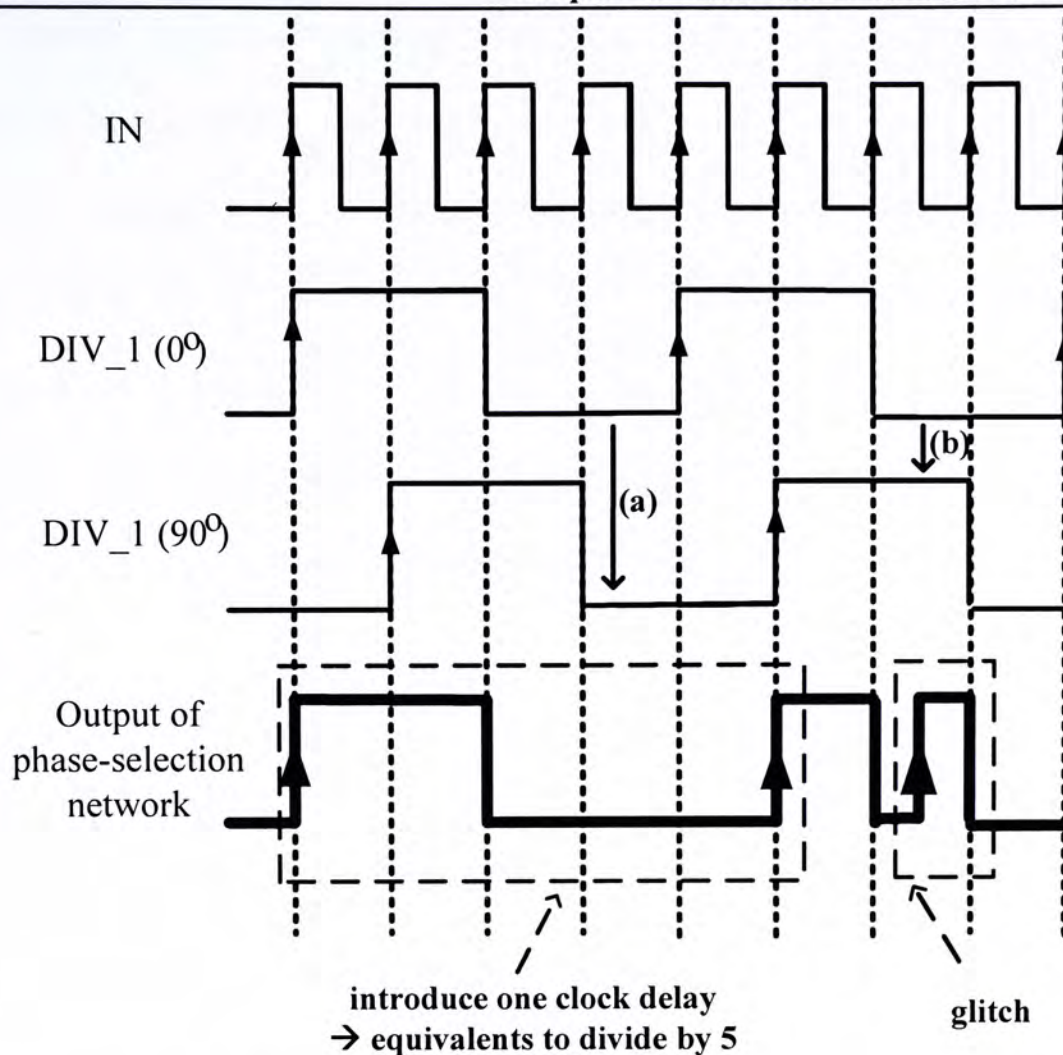


Figure 5.15: Waveforms for (a) proper switching and (b) improper switching

In [32], a glitch-free DMP was proposed by reversing the switching sequence (Figure 5.16) to avoid the use of power hungry re-timing circuitry. This technique ensures the switching only happens within the timing windows. However, the reverse switching scheme decreases one clock cycle at switching instants rather than increases one cycle in forward switching scheme. It is interesting that this idea assumes signals are perfect square waves, which is usually not available for high frequency operation. The waveforms at each divide-by-2 stage are shown in fig. One potential problem is that the phase-selection network output at the switching instant may not be able to fully charge to VDD or discharge to GND due to the time allowed for generating a pulse is shorter, especially when an input waveform with finite rise- and fall-time is employed (Figure 5.17). The missing of pulse at the phase-selection

network output causes miscounting issue which results in an erroneous output frequency in the synthesizer. One way to solve this problem is to reduce the rise- and fall-time by re-shaping the waveform (amplification), which again would lead to increased power consumption. Since there are no rail-to-rail glitches appear at the MUX output if sinusoidal waveform inputs are applied, such small glitches is removed by using low power buffers with small unity-gain bandwidth (low-pass) to eliminate the high frequency components (Figure 5.18).

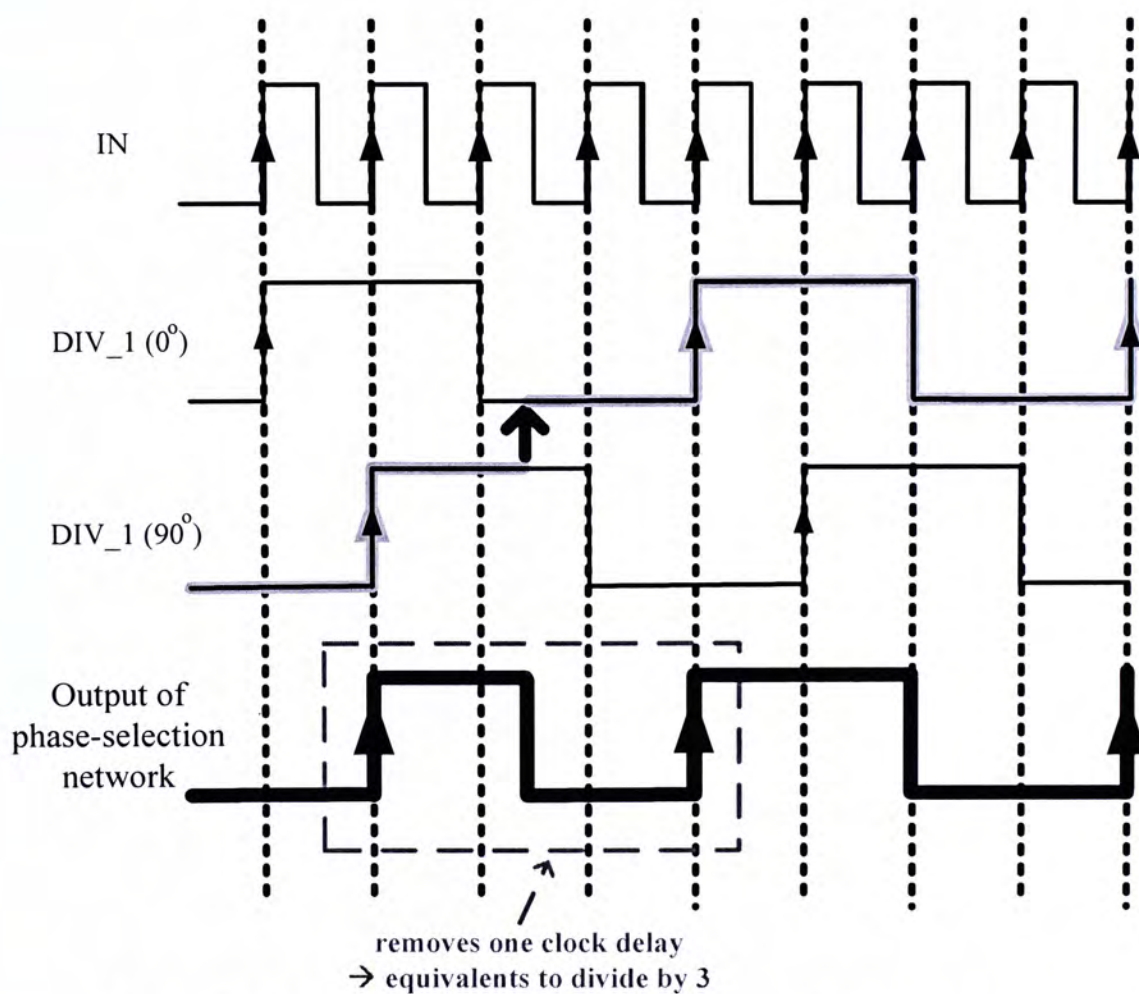


Figure 5.16: Waveform diagram for reverse-switching scheme

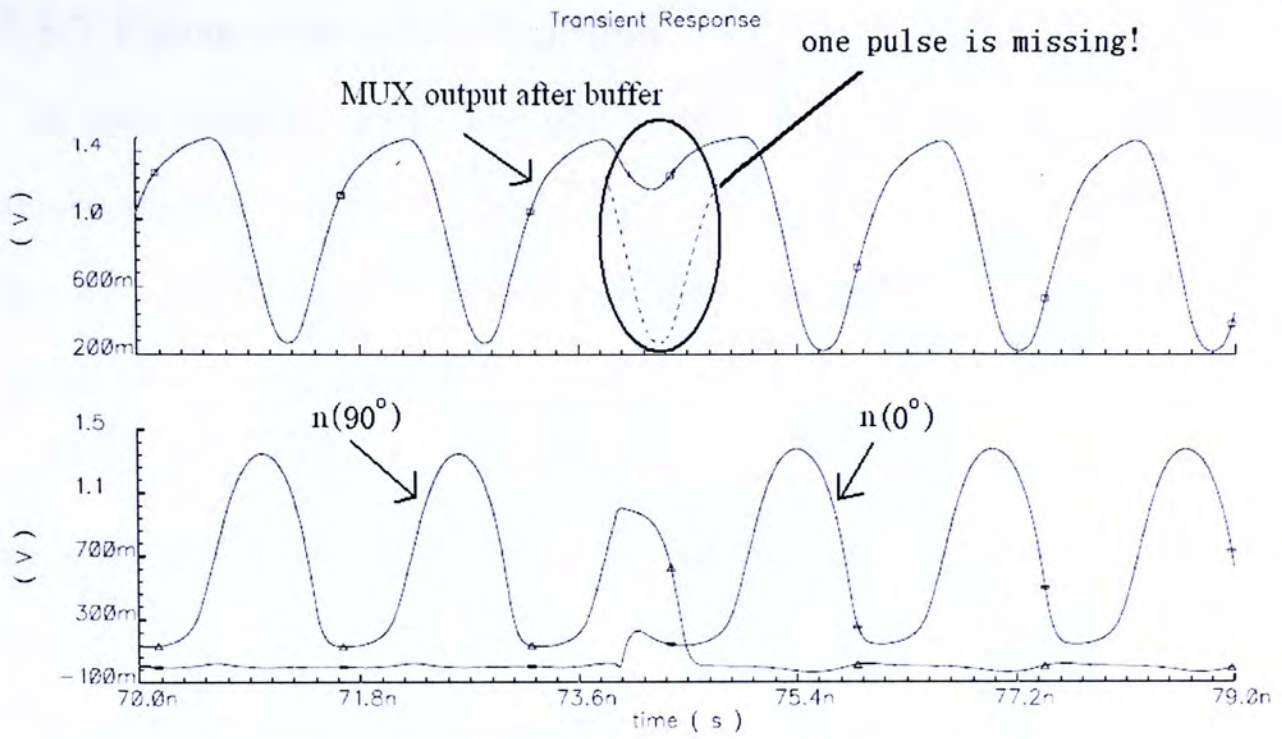


Figure 5.17: Simulated waveforms of MUX output after buffer and intermediate nodes (in Figure 5.10) with reverse-switching scheme

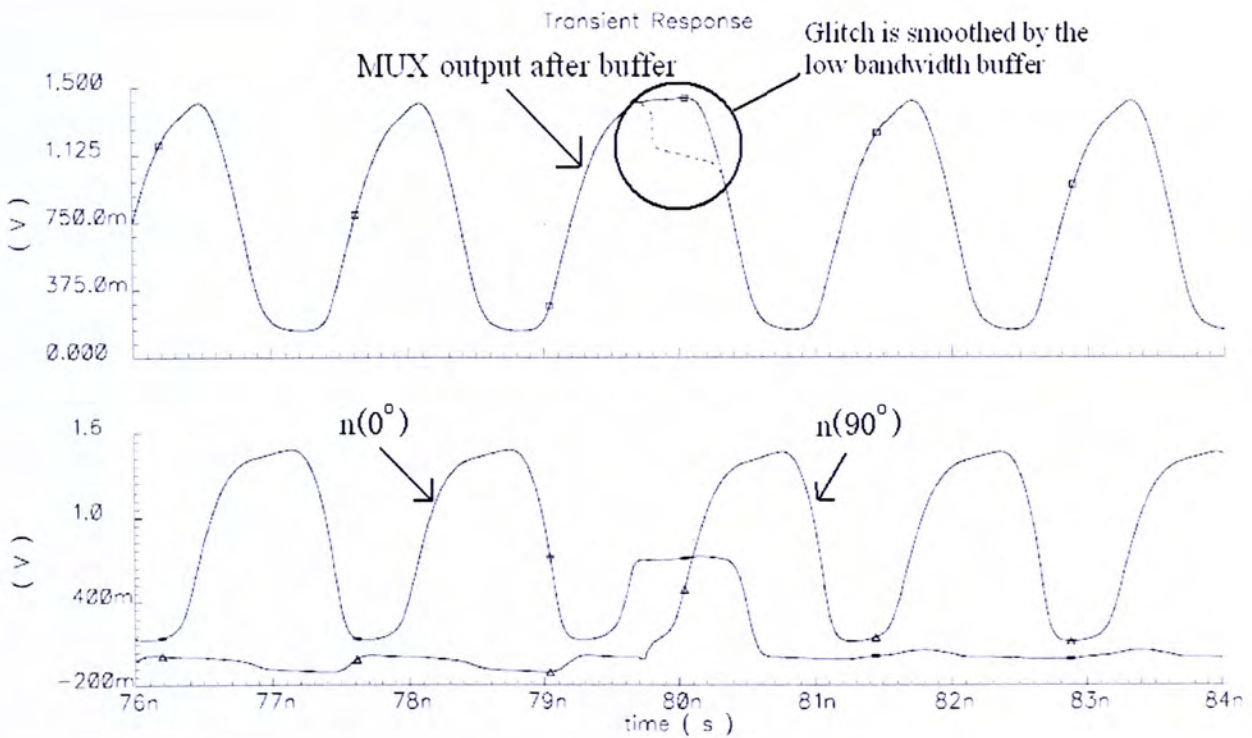


Figure 5.18: Simulated waveforms of MUX output after buffer and intermediate nodes (in Figure 5.10) with forward-switching scheme

5.3.7 Phase-mismatch Problem

In phase-switching DMP, any phase mismatch due to process variations and asymmetric layout of the full-speed divider leads to finite accuracy of the output. For the case of dividing 65, same phase error appears periodically for every four output period. As a results, there exists spurs at the output spectrum located at $1/4f_0$, $2/4 f_0$, $3/4 f_0$ from the fundamental output frequency f_0 [33]. Similarly, this non-ideality causes unwanted spurs at the PLL output spectrum and it affects the performance (noise and stability) of synthesizer. Extra attention is paid on the layout of differential full-speed divide-by-4 circuitries to lower the magnitudes of spur to negligible levels.

5.4 Simulation Results

Figure 5.19 shows the simulated waveforms of the four phase-control signals. When Mode = 1, one of the phase-control signals remains low while the other three equal to high so that there is no phase-switching activities occur. When Mode = 0, the four phase-control signals serve as non-overlapped clocks for the switch amplifier 4-to-1 MUX.

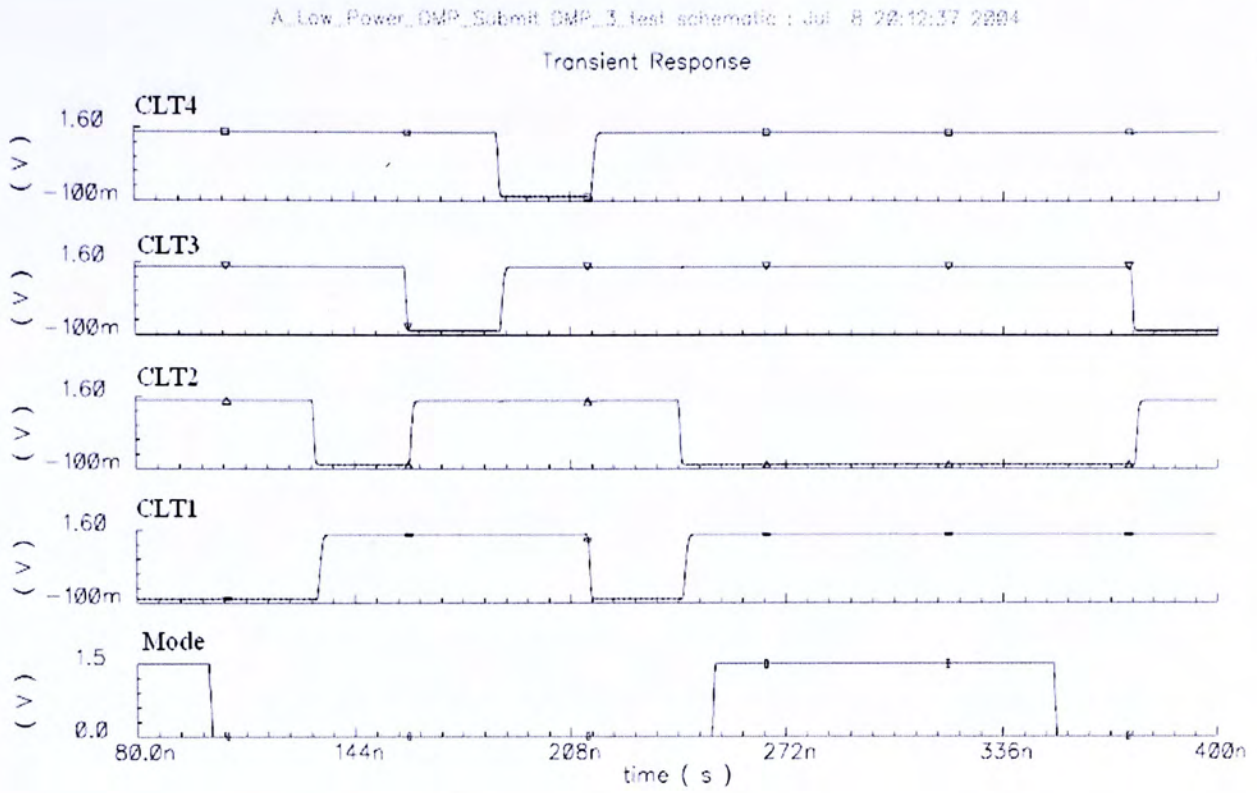


Figure 5.19: Simulated waveforms of the phase-control signals

The MUX output for different logic value of Mode is simulated, as shown in Figure 5.20. When Mode = 1, the MUX output is a divide-by-4 version of the input. When Mode = 0, it introduces one clock delay for every output period because of the phase-switching effect of the quadrature divide-by-4 output.

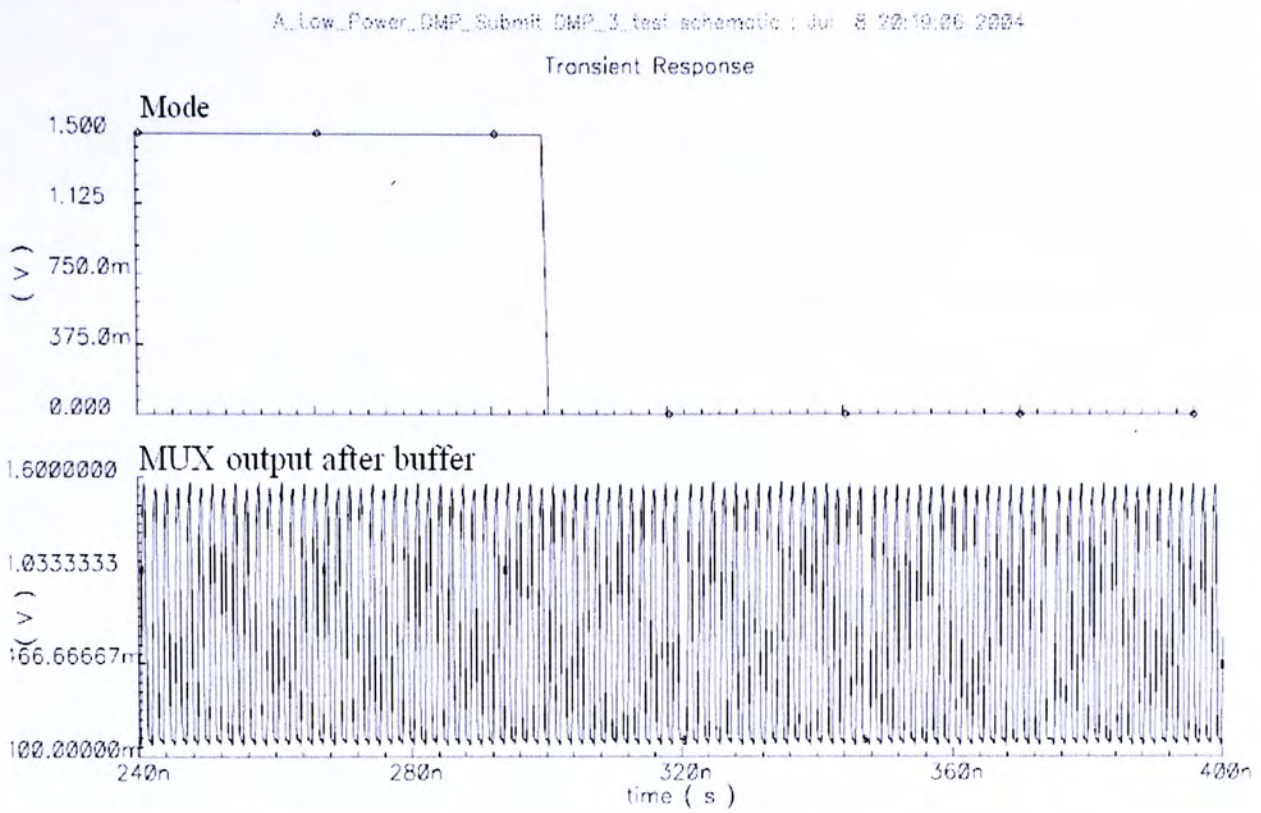


Figure 5.20: Simulated waveforms of the MUX output

Figure 5.21 and Figure 5.22 show the simulated waveforms of each divide-by-2 stage's output for different logic value of Mode with 2.4GHz input. When Mode = 1, the output divides the input by 64. When Mode = 1, the output divides the input by 65.



Figure 5.21: Simulation results of divide-by-64 operation



Figure 5.22: Simulation results of divide-by-65 operation

5.5 Summary

This chapter presents the design and implementation of a 2.4GHz dual-modulus 64/65 DMP using phase-switching technique. The simulated power consumptions of each block in DMP are summarized in Table 5.2. A total power dissipation of less than 1mW is achieved at a supply voltage of 1.5V. The divide-by-4 stages are realized by one flip-flop instead of two which makes it possible to reduce the circuit complexity and power dissipation and a new low power scheme is proposed to handle the glitch problem. From simulation, an operating frequency range of 2.2GHz – 2.7GHz GHz (with 0dbm input) is obtained.

Block	Power Consumption (μ W)
Full-speed Divide-by-4	380
TSPC dividers	280
Low-speed Divide-by-4	95
Phase-select Network	70
Others (e.g. buffers, logic gates)	80
Overall DMP	905

Table 5.2: Simulated power consumption of each block in DMP

Chapter 6

1.5V 2.4GHz Wideband DMP

6.1 Introduction

In pervious design, power dissipation is reduced at the expense of the operating bandwidth. The limited bandwidth decreases the circuit's flexibility and robustness. In this chapter, a new wideband DMP is proposed based on the architecture in pervious design. This chapter also introduces some new circuit techniques to increase the operating frequency.

6.2 Proposed DMP Architecture

Recall that a narrowband circuit is applied to perform a divide-by-4 operation to lower the power consumption of DMP. This DMP design replaces the narrowband divide-by-4 circuit by a pair of divide-by-2 circuits to increase the operating bandwidth.

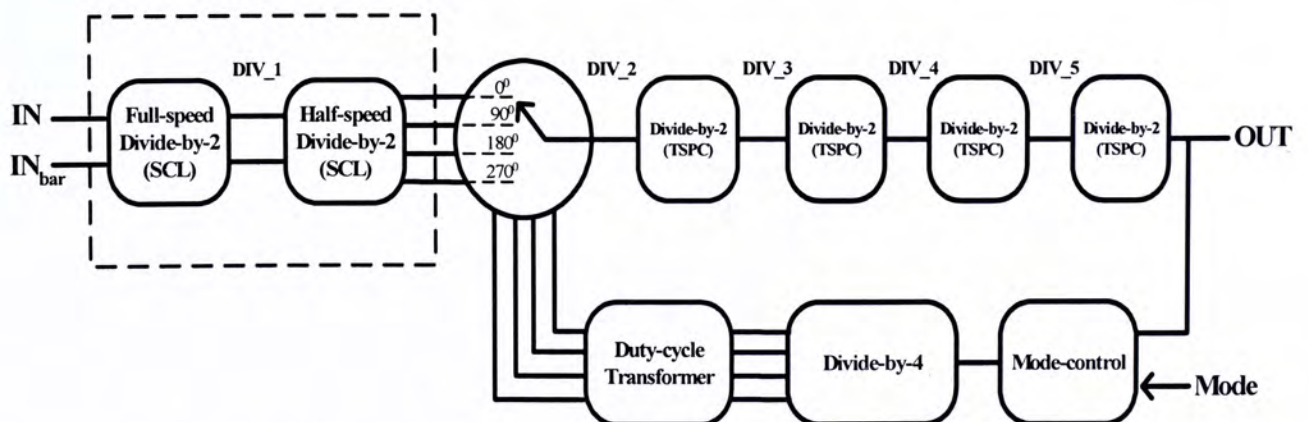


Figure 6.1: Block Diagram of wideband phase-switching DMP

6.3 Divide-by-4 Stage

Two circuit design techniques, namely current-switch combining and capacitive load reduction, are applied to the front-end divider-by-4 stage in order to increase the operating speed enhancement with low power consumption.

6.3.1 Current-switch Combining

In the conventional SCL divider (Figure 6.2), four current-switches are required. The four current-switches, however, can be combined in pairs according to the phase of input. By doing this, number of transistors in each divide-by-2 circuit is decreased from 16 to 14. It simplifies the layout and thus reduces the parasitics due to routing. As a result, a high operating speed is achieved. In this DMP design, current-switch combining technique is applied to both the full-speed divider and the half-speed divider.

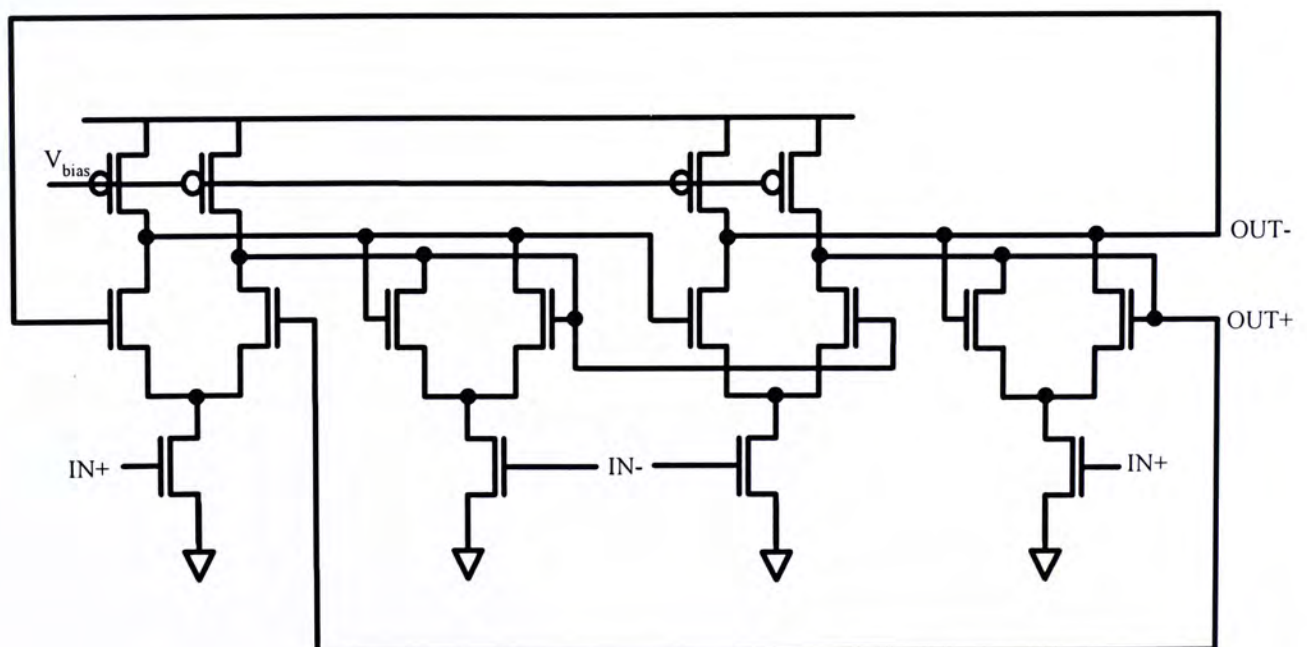


Figure 6.2: Schematic of the conventional divide-by-2 circuit

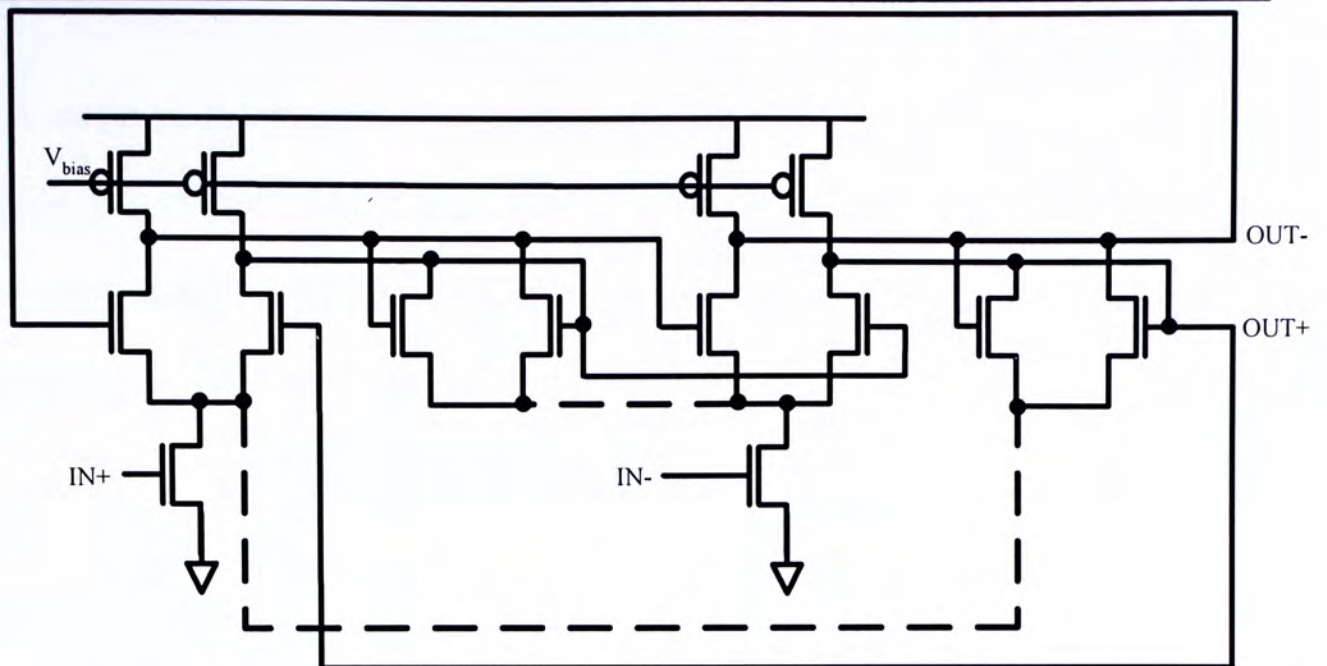


Figure 6.3: Schematic of the divide-by-2 circuit with combined current-switches

6.3.2 Capacitive Load Reduction

Intuitively, the operating frequency of full-speed divider increases as the self-oscillating frequency increases. As illustrated in Figure 6.4, the input sensitivity curve is expected to shift towards to the high frequency end for an increased self-oscillating frequency.

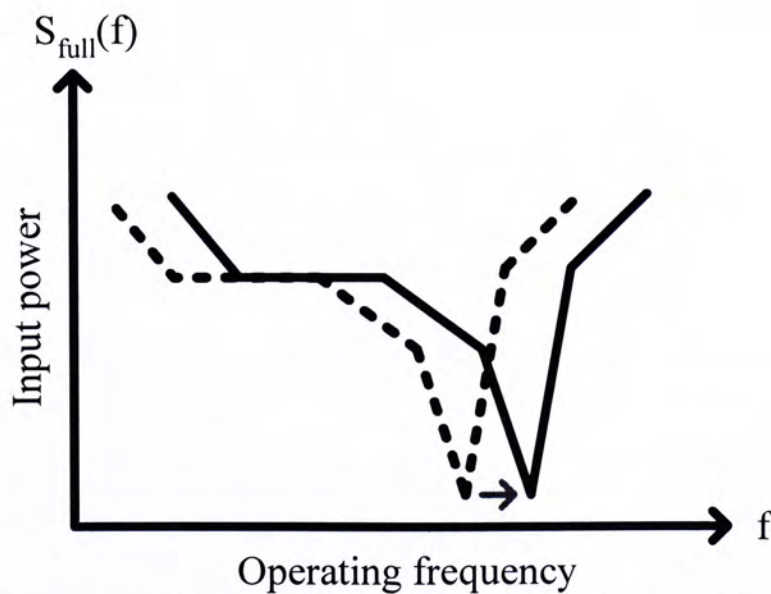


Figure 6.4: Input sensitivity curve with increased self-oscillating frequency

A model is developed to predict the self-oscillating frequency of the divide-by-2 circuit [12]. Since node X and node Y in the SCL latch (Figure 6.5(a)) are ac grounded, a half-circuit small-signal equivalent in Figure 6.5(b) can be obtained (assuming the latch is a single-pole system,).

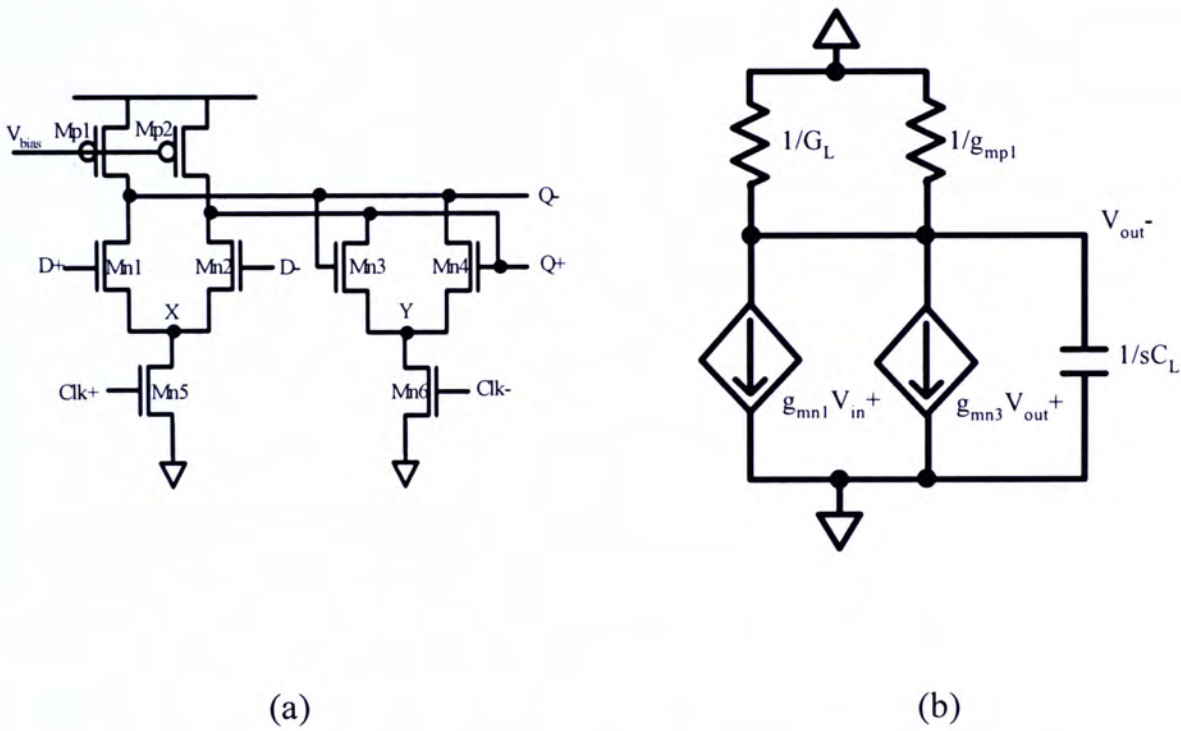


Figure 6.5: SCL latch model (a) schematic (b) equivalent small-signal model

By KCL,

$$-V_0 G_L - V_0 g_{mp1} - V_0 s C_L + g_{mn1} V_0 + g_{mn3} V_i = 0$$

$$V_0 [G_L + g_{mp1} + s C_L + g_{mn1}] = g_{mn3} V_i$$

$$\frac{V_0}{V_i} = \frac{(g_{mn3} / G_L + g_{mp1} + g_{mn1})}{1 + s(C_L / G_L + g_{mp1} + g_{mn1})} \quad \dots(6.1)$$

At steady-state of oscillation, the loop gain becomes unity (i.e. $V_0 = V_i$). By substituting this condition into Equation 6.1., the self-oscillating frequency of the divide-by-2 circuit can be estimated by the following equation:

$$f_{out} = \frac{\sqrt{g_{mn1}^2 - (-g_{mn3} + g_{mp1} + G_L)^2}}{2\pi C_L} \quad \dots(6.2)$$

where $G_L = g_{dsp1} + g_{dsn1} + g_{dsn3}$

In practice, this model is not very accurate since the output signals are large signal rather than small signal during oscillation and parasitic capacitors become non-linear. However, this model can still give us a rough idea for designing high speed divider. One observation from Equation (6.2) is that high self-oscillating frequency can be obtained by reducing the loading capacitance C_L , which is mainly depends on the size of its loading transistors (i.e. current-switches in the half-speed divider). One design dilemma is that the size of current-switch cannot be too small in order to provide enough current for high frequency operation. In addition, the operating speed of the half-speed divider decreases significantly if the size of current-switches in the half-speed divider is reduced (Figure 6.6).

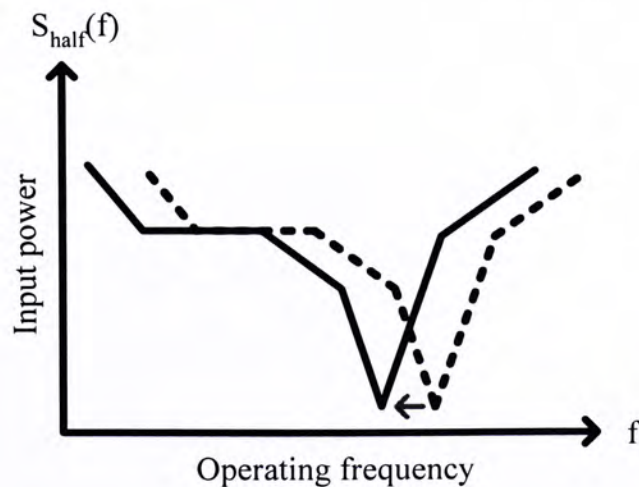


Figure 6.7: Input sensitivity of half-speed divider with smaller current-switches

A solution to break this design barrier is adding an extra current-source in parallel with the current switch. The schematic of the proposed SCL latch is shown in Figure 6.6. The original current-switch Mn5 is divided into two transistors, Mn5a and Mn5b. Note that the sum of the current provided by both Mn5a and Mn5b should be equal to that provided by Mn5. In this latch, transistor Mn5a functions as a current-switch with reduced size while Mn5b is biased to V_{DD} to provide more current for high speed operation. In order to optimize the input sensitivity of the whole DMP, the self-oscillating frequency of the half-speed divider should be equal to half of that of the full-speed divider.

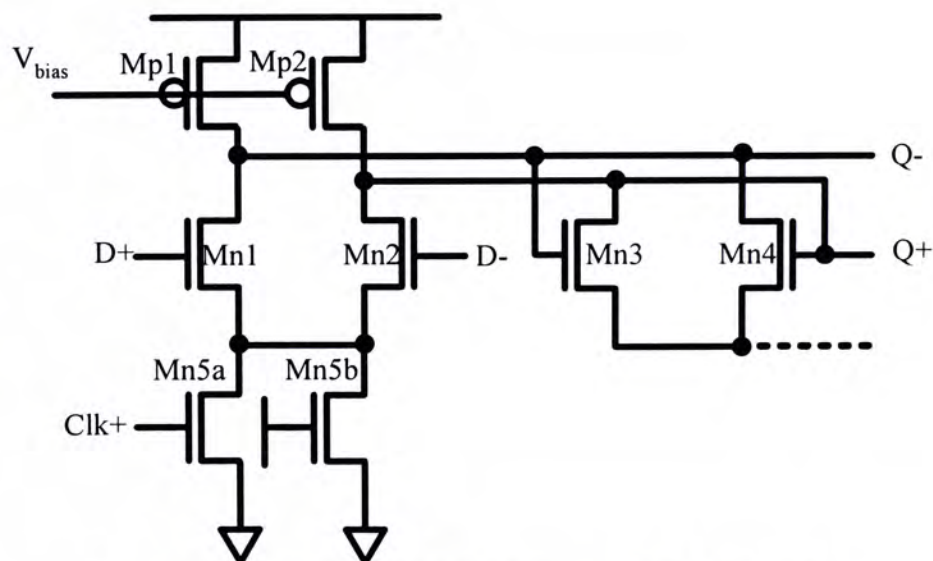


Figure 6.8: Schematic of the proposed SCL latch

The drawback of this technique is the reduced operating bandwidth in half-speed divider. However, the bandwidth requirement of the half-speed divider is only half compared to that of the full-speed divider which is not tough. It is important to point out that the self-oscillating frequency using this technique does not decrease (Figure 6.7).

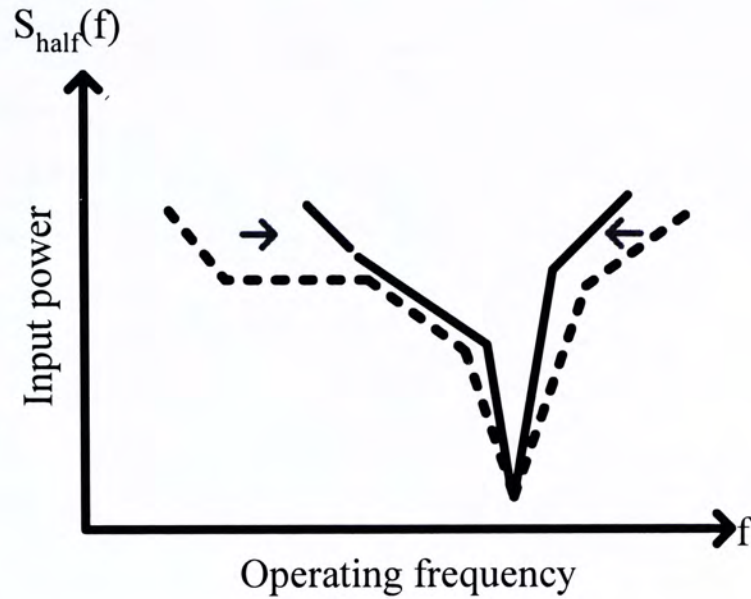


Figure 6.7: Input sensitivity of half-speed divider with proposed technique

Since the capacitive load reduction technique does not require any modifications on the full-speed divider, any other speed-enhancement circuit techniques can also be applied to the full-speed divider. Note that this technique is also applicable for the full-speed divider to minimize the load of the VCO.

6.4 Simulation Results

To study the effect on input sensitivity for different sizes of Mn5a and Mn5b, three dividers are simulated and their input sensitivity curves are plotted in Figure 6.9. The sizes of transistor in three cases are summarized in Table 6.2.

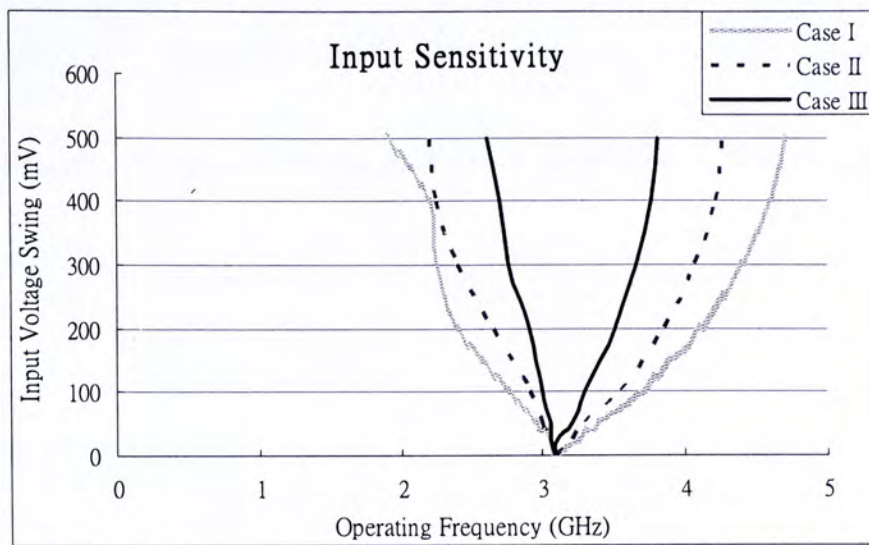


Figure 6.9: Simulated input sensitivity with different sizes of loading transistor

Case	Size (W/L) of Mn5a	Size (W/L) of Mn5b
I	10 μ m/ 0.35 μ m	--
II	7.5 μ m/ 0.35 μ m	2.5 μ m/ 0.35 μ m
III	5 μ m/ 0.35 μ m	5 μ m/ 0.35 μ m

Table 6.1: Sizes of transistor in different cases

Simulation shows that over 13% speed improvement is achieved for the full-speed divider by reducing the size of the current-switch from 5 μ m to 3 μ m. Besides, it also shows that a higher output voltage swing (better driving capability) can be achieved by using the proposed technique.

Size (W/L) of loading transistor	Size (W/L) of parallel-connected current Source	Maximum operating frequency	Output swing @ 2.9GHz input
5 μ m/ 0.35 μ m	--	2.9GHz	607mVpp
3 μ / 0.35 μ m	2 μ / 0.35 μ m	3.3GHz	690mVpp

Table 6.2: Simulation results of full-speed divider with 300mV input swing

6.5 Summary

A wideband DMP is designed based on the phase-switching architecture. Current-switches are combined in both the full-speed divider and half-speed divider to simplify the layout. Besides, higher operating speed is achieved by reducing the output capacitance of the full-speed divider. Simulations show that the proposed DMP work well from 2GHz to 3GHz. At 1.5V supply, the simulated power consumption is 1.2mW.

Chapter 7

Experimental Results

7.1 Introduction

In this chapter, the measurement results of three DMP prototypes are presented. They were all fabricated by using AMS 0.35 μ m standard CMOS process.

7.2 Equipment Setup

Figure 7.1 shows you the complete measurement setup. The bare dies are attached to evaluation PCBs using silver epoxy for measurement purpose. All connections between the PCB traces and die are done by gold bondwires. A signal generator (Agilent E4433B) is employed to provide the input signal. Besides, a spectrum analyzer (HP 8546A) is used to obtain the frequency spectrum at the output of DMP. For time domain analysis, an oscilloscope (Agilent 54622D) is used to capture the output waveform. The DC power supplies (HP E3620A) in the setup provide the supply voltage and biasing voltage for the device under test (DUT).

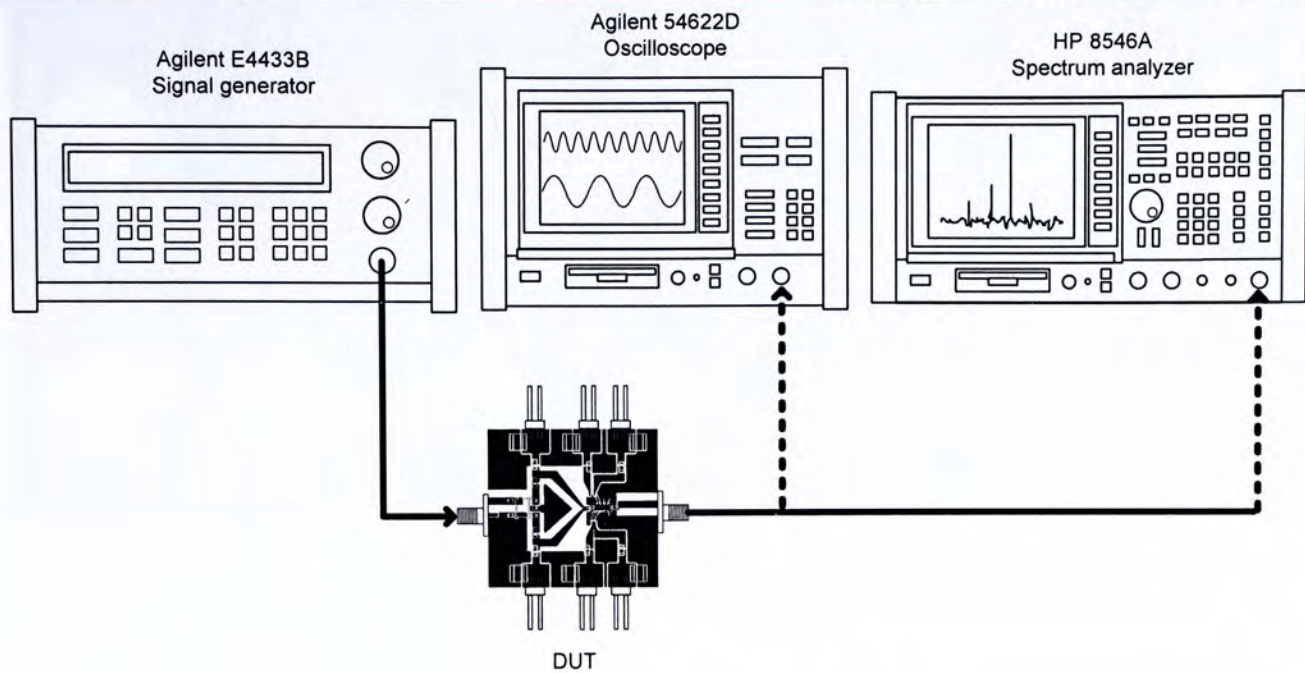


Figure 7.1: Equipment setup

7.3 Measurement Results

7.3.1 3V 900GHz Low Noise DMP

Figure 7.2 shows the microphotograph of the fabricated circuit. The chip occupies an active area of approximately $220\mu\text{m} \times 130\mu\text{m}$. The DMP works well at 900MHz with 3V supply. For measurement purposes, on-chip output buffers were added for driving the $50\text{-}\Omega$ external load. In addition, off-chip 3-dB hybrid was employed to provide a differential input for the DMP. Figure 7.3 and Figure 7.4 show the captured signal waveforms for an input frequency of 128MHz and 960MHz. For an input of 960MHz, the output frequencies were 14.99MHz and 14.77MHz when dividing ratios are 64 and 65 respectively. Excluding the output buffer, current consumption was found to be about 4mA at an input frequency of 960MHz. For sensitivity study, Figure 7.5 gives the measured input power variation as a function of operating frequency. The maximum operating frequency was around 1.07GHz.

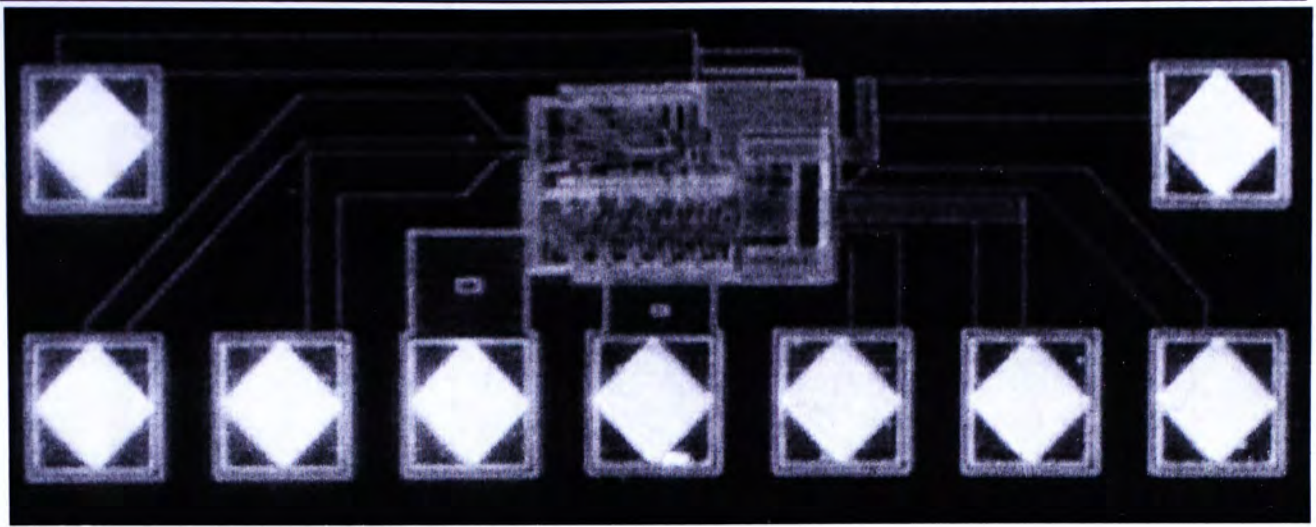


Figure 7.2: Microphotograph of fabricated low noise DMP

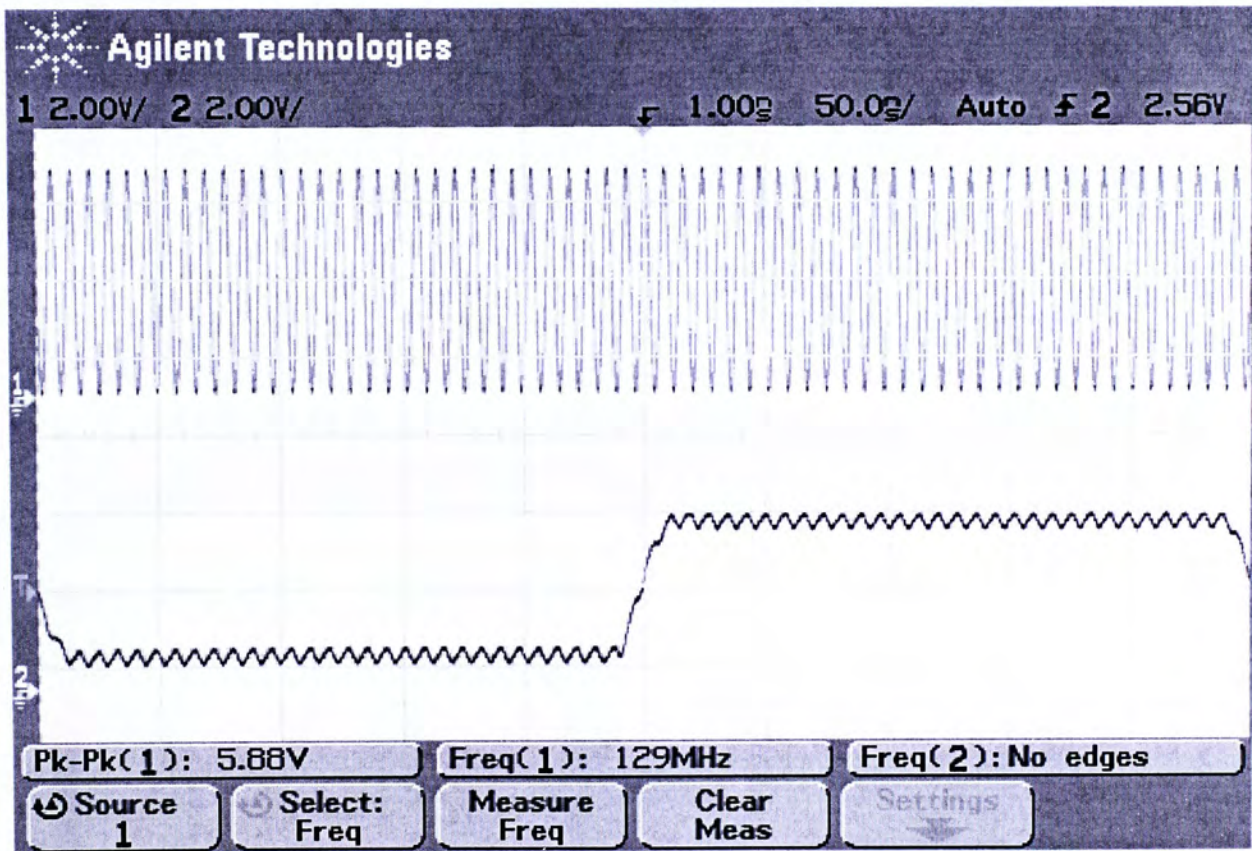
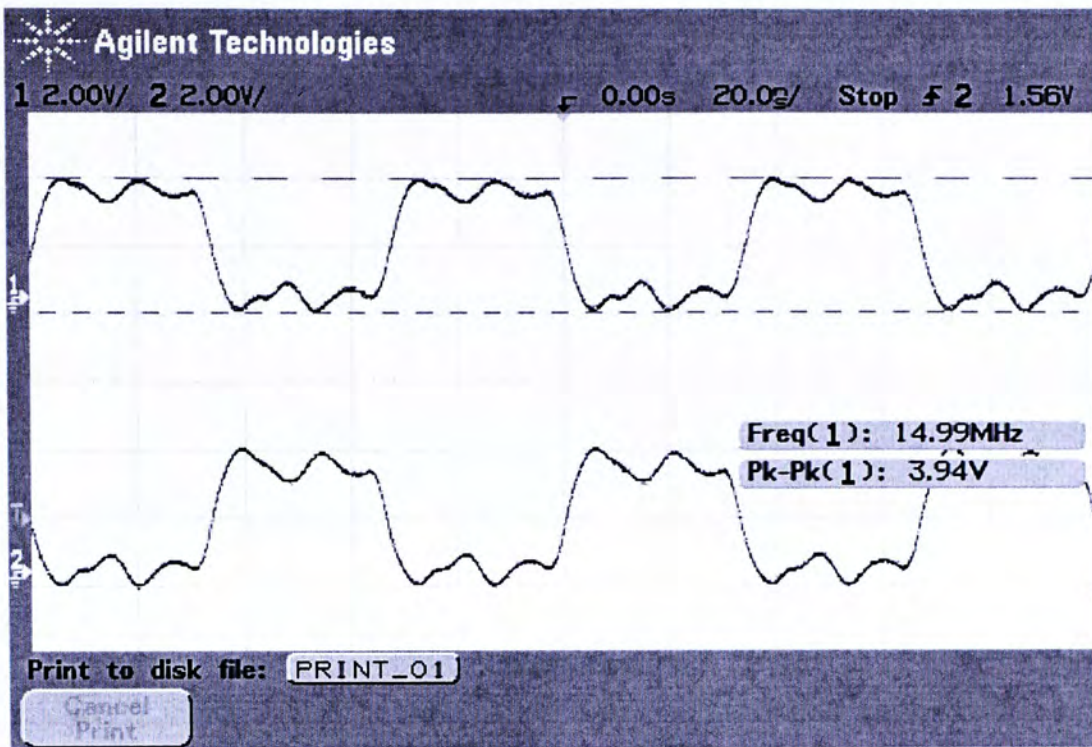
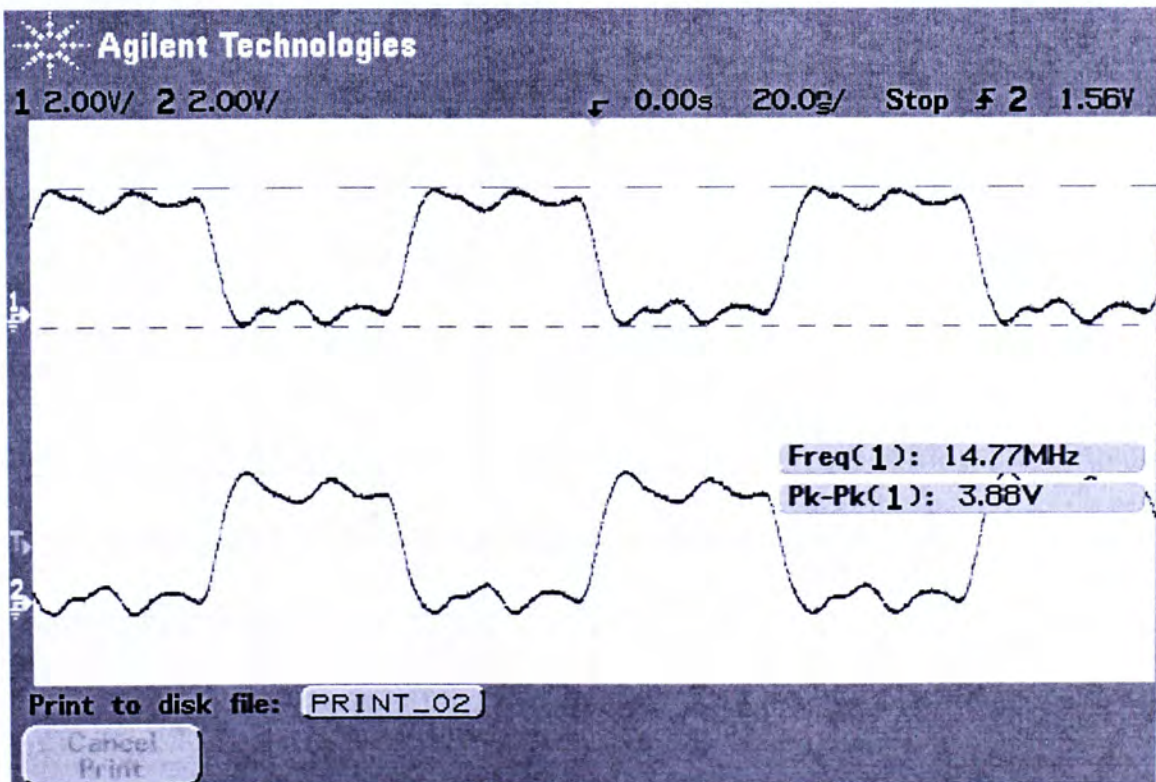


Figure 7.3: Divider-by-64 input and output waveforms ($f_{in}=128\text{MHz}$)



(a)



(b)

Figure 7.4: Output Waveforms @ 960MHz inputs (3dBm) (a) Divide-by-64 (b) Divide-by-65

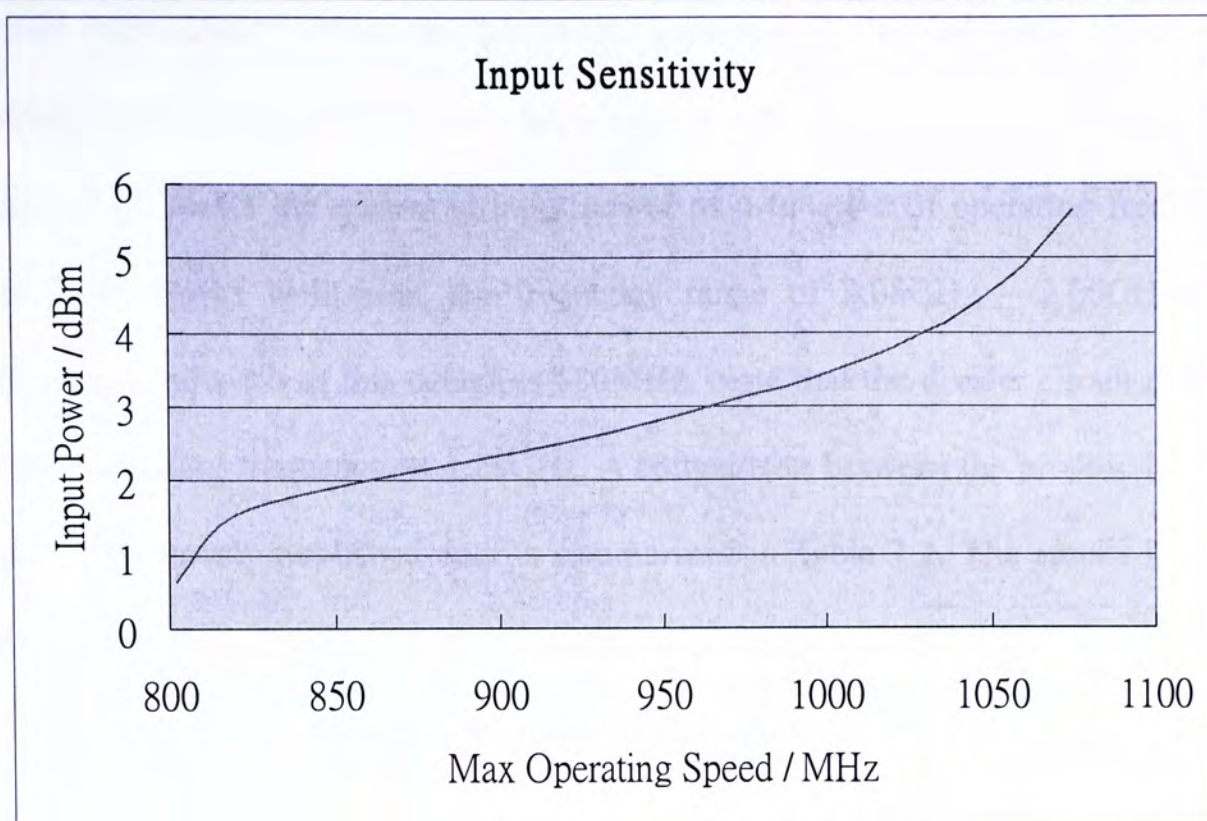


Figure 7.5: Input signal level versus operating speed

7.3.2 1.5V 2.4GHz Low Power DMP

The microphotograph of the fabricated circuit is shown in Figure 7.6. The active area is approximately $220\mu\text{m} \times 130\mu\text{m}$. Similarly to the previous circuit, on-chip output buffers were added for driving the $50\text{-}\Omega$ external load and off-chip 3-dB hybrid was employed to provide a differential input for the DMP. At 1.5V supply voltage, power consumption was found to be about 0.87mW with input frequency of 2.4GHz. Figure 7.7 and Figure 7.8 show the frequency spectrum of the output for different modes of operation. In practice, spurs will appear at an offset frequency of $f_0/4$ from carrier for divide-by-65 operation. One source of the spurs is the phase-mismatch introduced by the manufacturing tolerances and routing problem. Another major source phase-mismatch is due to the amplitude and phase mismatch of the hybrid. Since only one divide-by-4 circuit is employed, any mismatch in the

hybrid will directly affect the quadrature accuracy of the full-speed divide-by-4 output. Besides, output waveforms are also captured in Figure 7.9 and Figure 7.10. Figure 7.11 shows the measured input power as a function of operating frequency. The DMP works well from the frequency range of 2.08GHz – 2.66GHz. The operating bandwidth of this design is 580MHz. Note that the divider circuit exhibits a self-oscillating frequency of 2.28GHz. A comparison between the proposed design and the previously published data is summarized in Table 7.2. The results indicate that the new design offers the highest figure of merit (GHz/mW) which is defined as the ratio of operating frequency to power dissipation at that frequency.

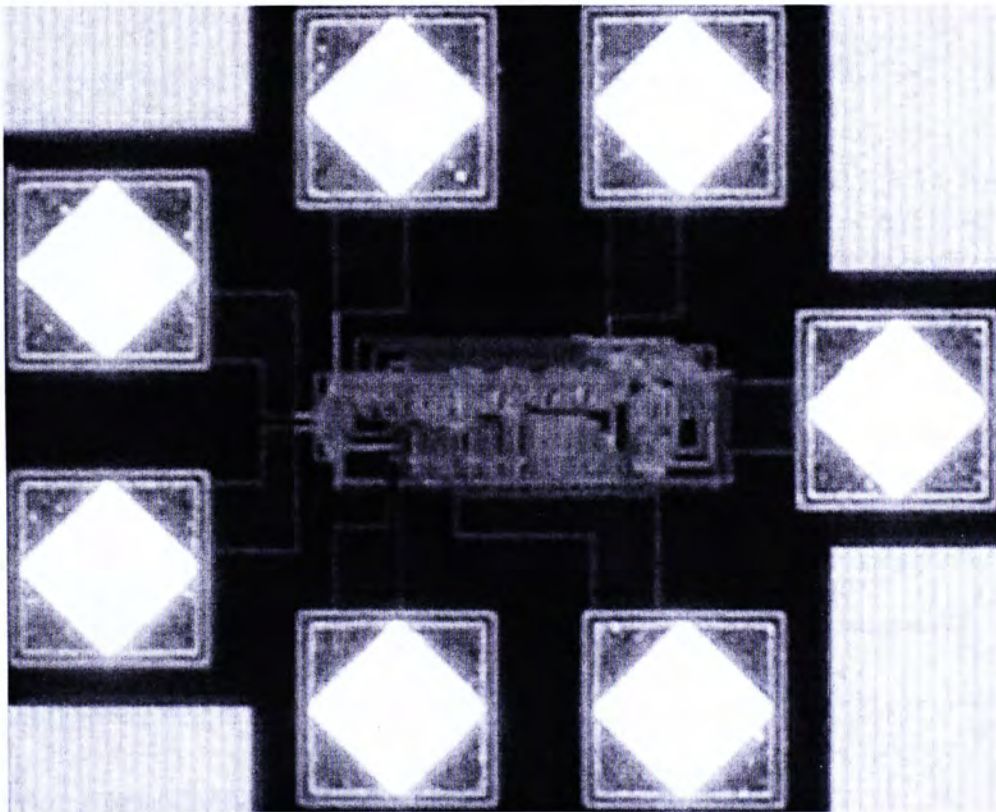


Figure 7.6: Microphotograph of fabricated low power DMP

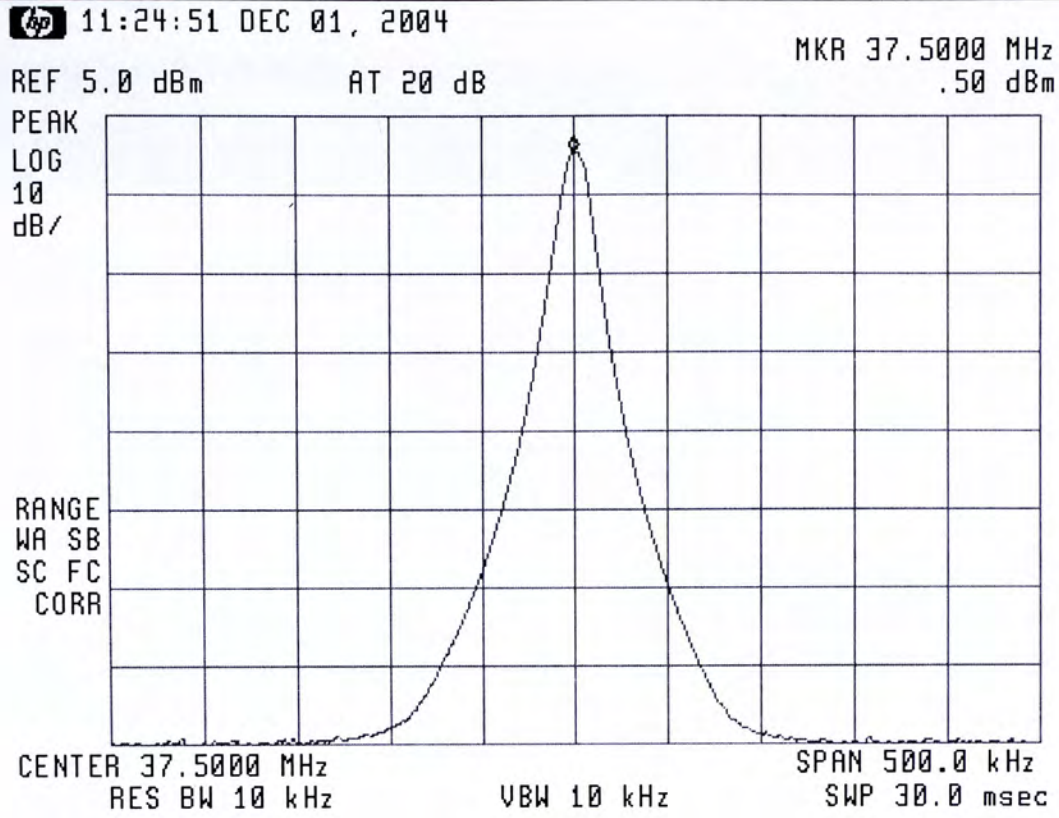


Figure 7.7: Output spectrum of divide-by-64 operation ($f_{IN} = 2.4\text{GHz}$)

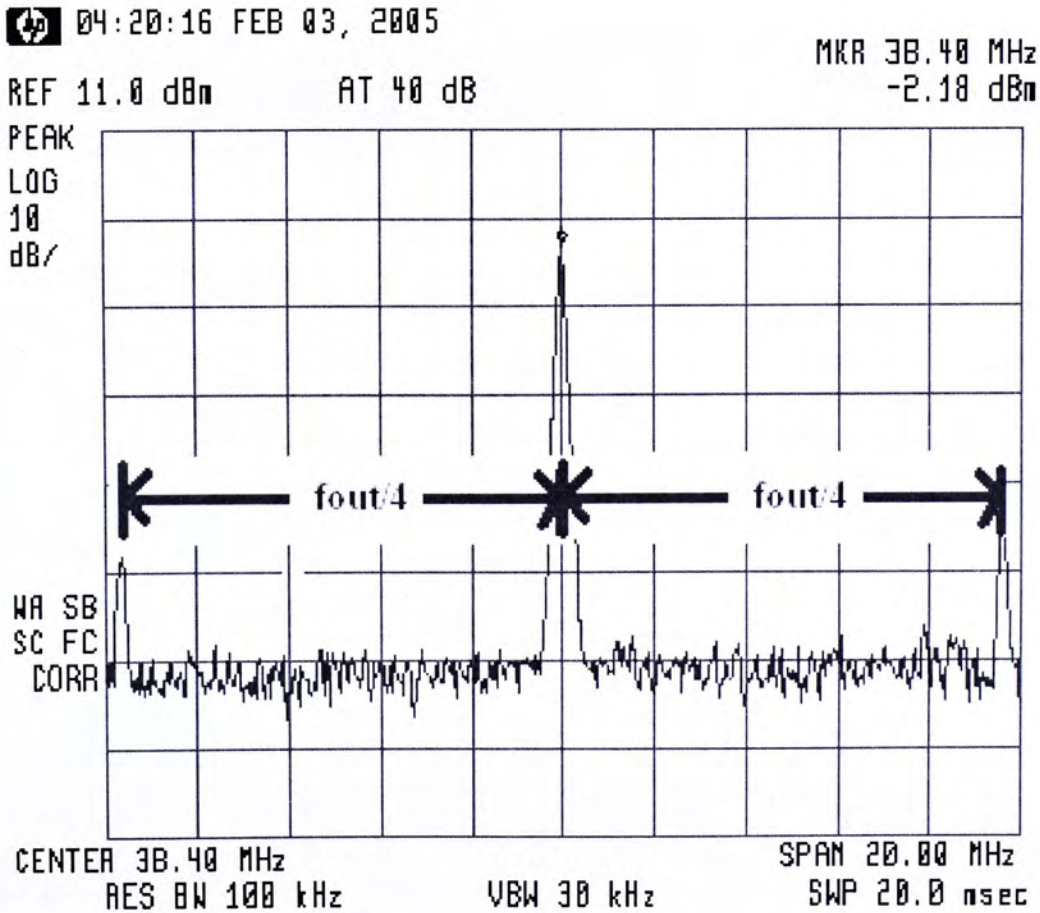


Figure 7.8: Output spectrum of divide-by-65 operation ($f_{IN} = 2.5\text{GHz}$)

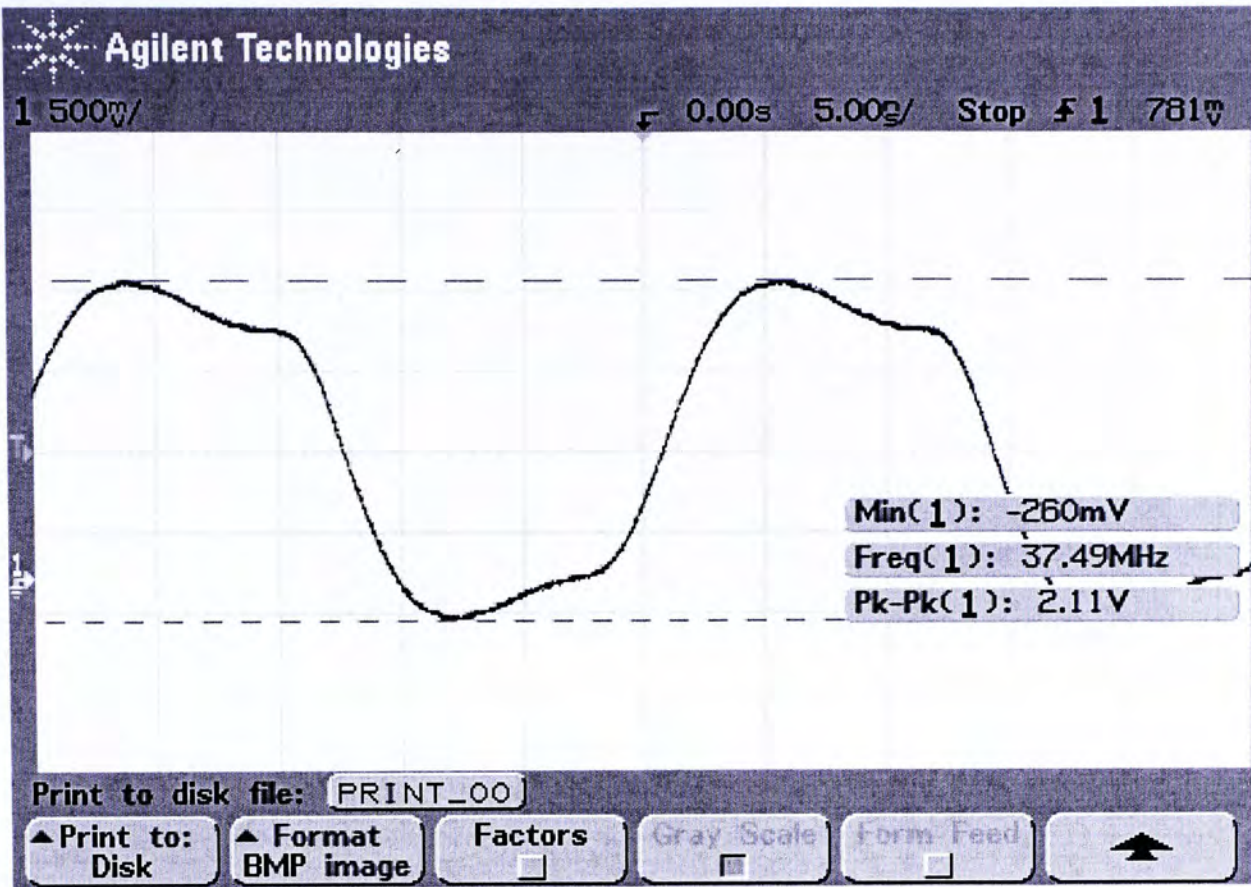


Figure 7.9: Output waveform of divide-by-64 operation ($f_{IN} = 2.4\text{GHz}$)

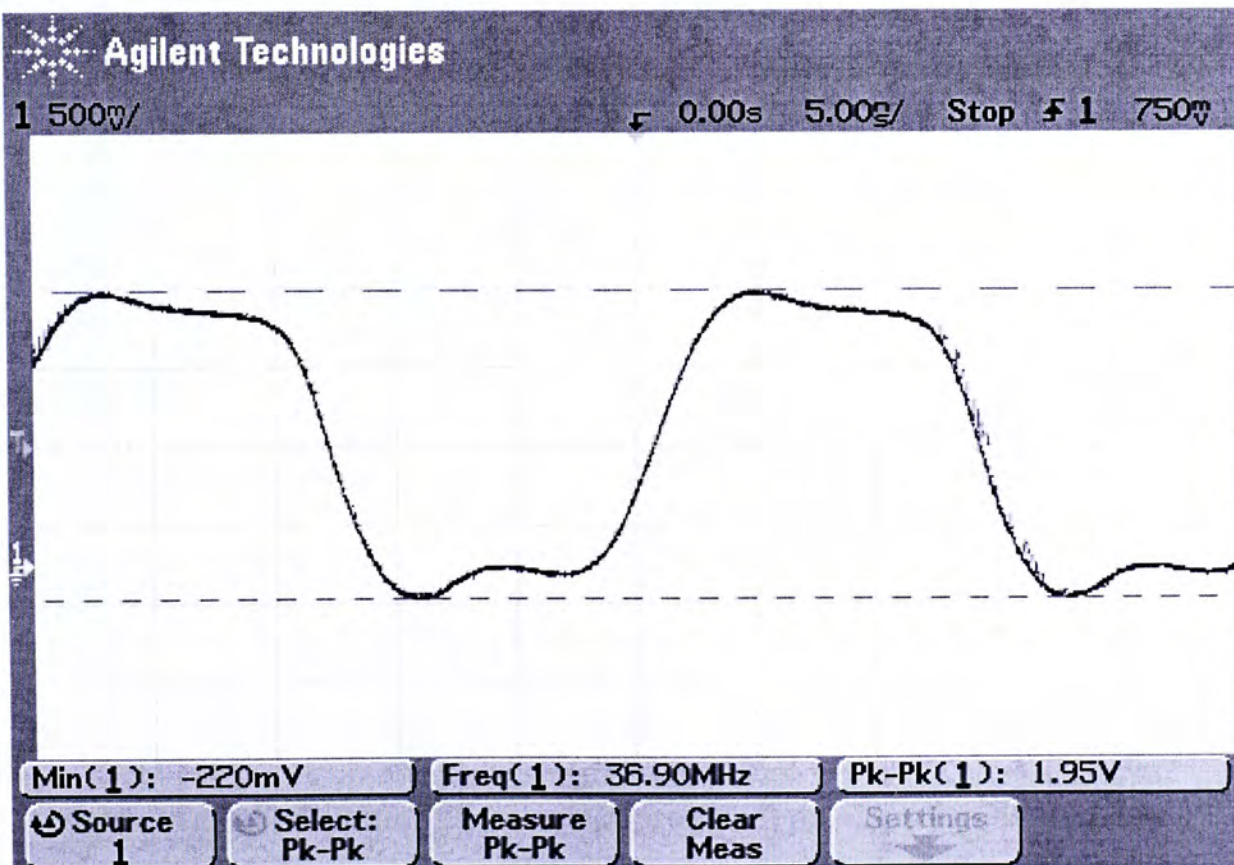


Figure 7.10: Output waveform of divide-by-65 operation ($f_{IN} = 2.4\text{GHz}$)

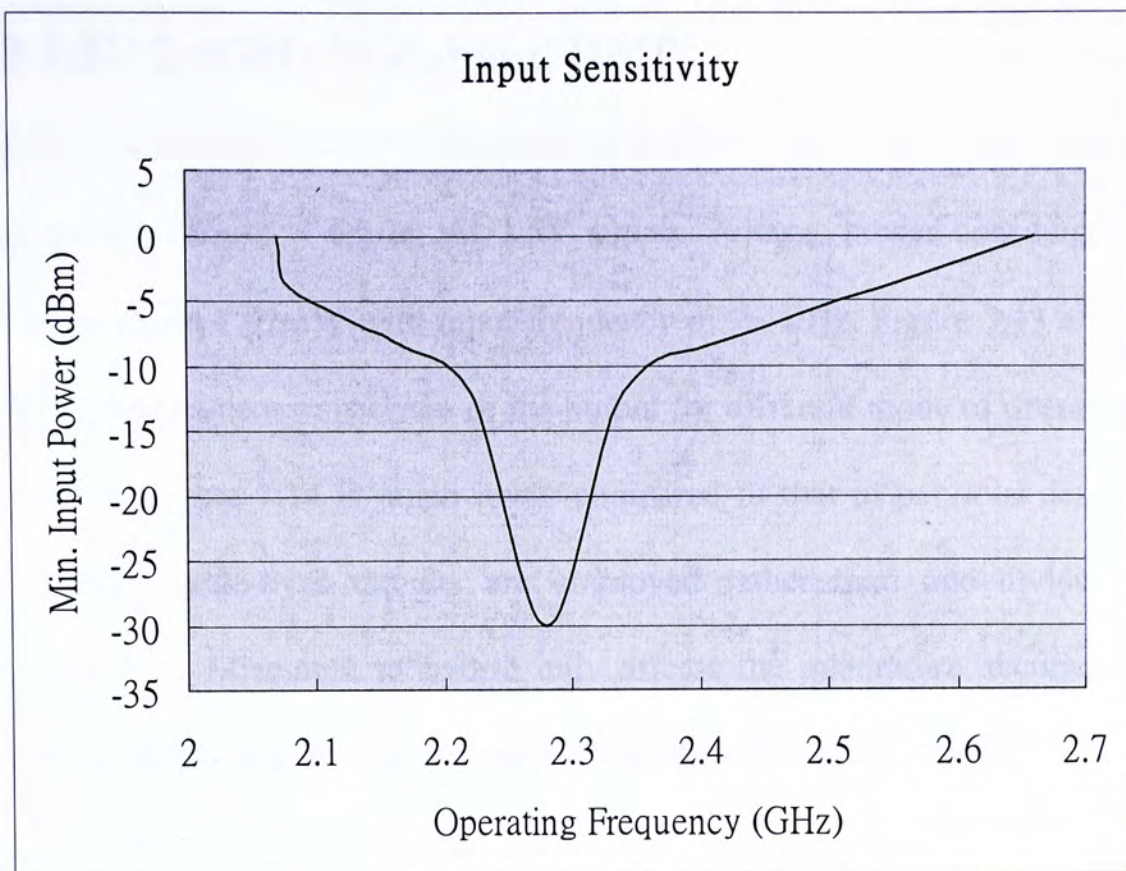


Figure 7.11: Measured minimum input power versus frequency

Reference	Process Technology	Dividing Ratio	V_{DD} (V)	Active Area (mm^2)	FOM* (GHz/mW)
[28]	0.25 μm SiGe BiCMOS	64/72	1.5	0.030	2/1.95 = 1.03
[29]	0.25 μm Std. CMOS	200-204	2.2	0.090	5.3/26.8 = 0.20
[32]	0.35 μm Std. CMOS	15/16	1.5	0.040	2.4/3 = 0.80
[35]	0.5 μm SOI CMOS	2	3	--	5/24 = 0.21
[36]	0.25 μm Std. CMOS	128/129	2.5	0.221	2.3/12 = 0.19
[37]	0.18 μm Std. CMOS	16/17	1.8	--	10/19.8 = 0.51
<i>This work</i>	0.35 μm Std. CMOS	64/65	1.5	0.016	2.4/0.87 = 2.76

Table 7.1: Performance comparison with previously published data

7.3.3 1.5V 2.4GHz Wideband DMP

Figure 7.12 shows the microphotograph of the fabricated circuit with a die size of approximately $186\mu\text{m} \times 65\mu\text{m}$. At 1.5V supply voltage, power consumption was found to be about 1.02mW with input frequency of 2.4GHz. Figure 7.13 and Figure 7.14 show the frequency spectrum of the output for different mode of operation. The spur level in Figure 7.14 is much lower compared to that in pervious design. It is because two divide-by-2 circuits are employed rather than one divide-by-4 in pervious design. Mismatch in hybrid only affects the quadrature accuracy of the output of the full-speed divider, but not the output of half-speed divider.

Figure 7.15 and Figure 7.16 show the captured output waveforms for different mode of operation. Figure 7.17 shows the measured input sensitivity of the DMP. The DMP works well from the frequency range of 1.98GHz – 2.88GHz. The operating bandwidth of this design is 900MHz. Note that the divider circuit exhibits a self-oscillating frequency of 2.26GHz.

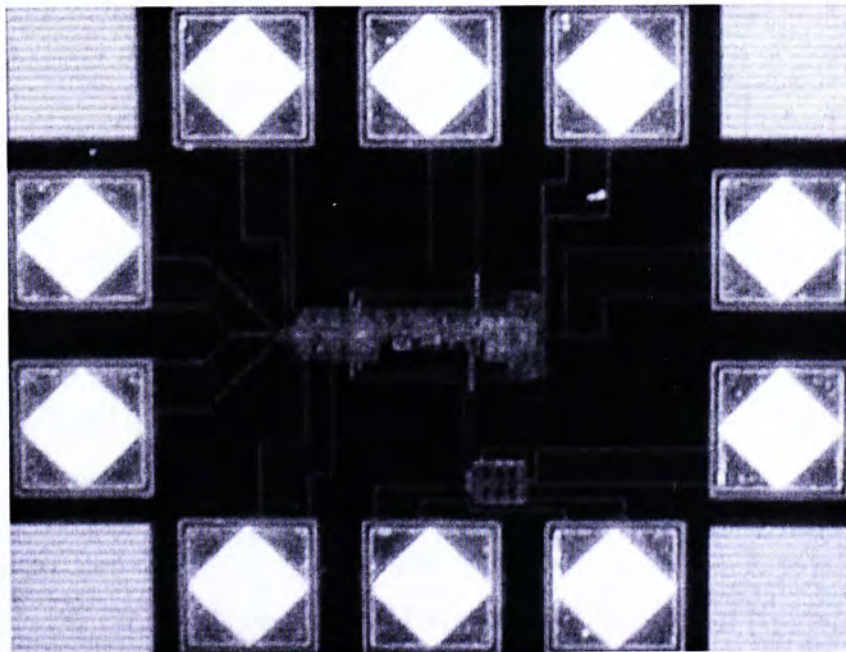


Figure 7.12: Microphotograph of the fabricated wideband DMP

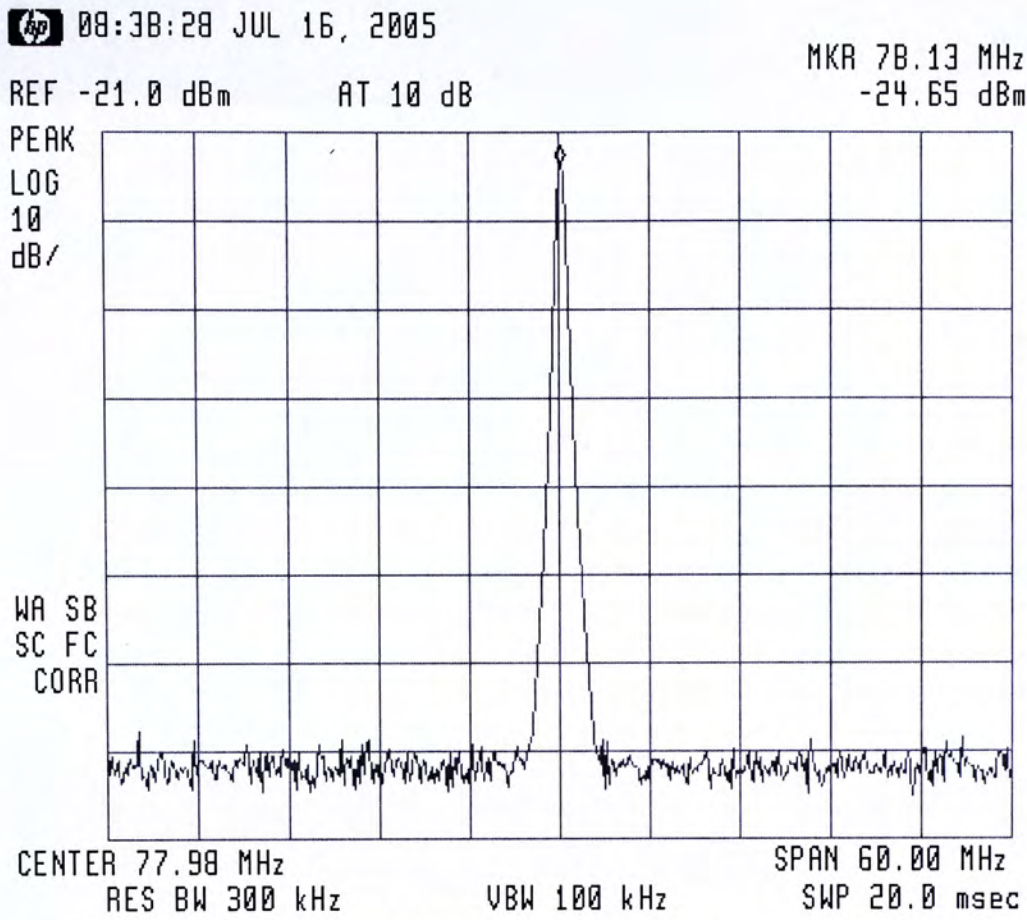


Figure 7.13: Output spectrum of divide-by-32 operation ($f_{IN} = 2.5\text{GHz}$)

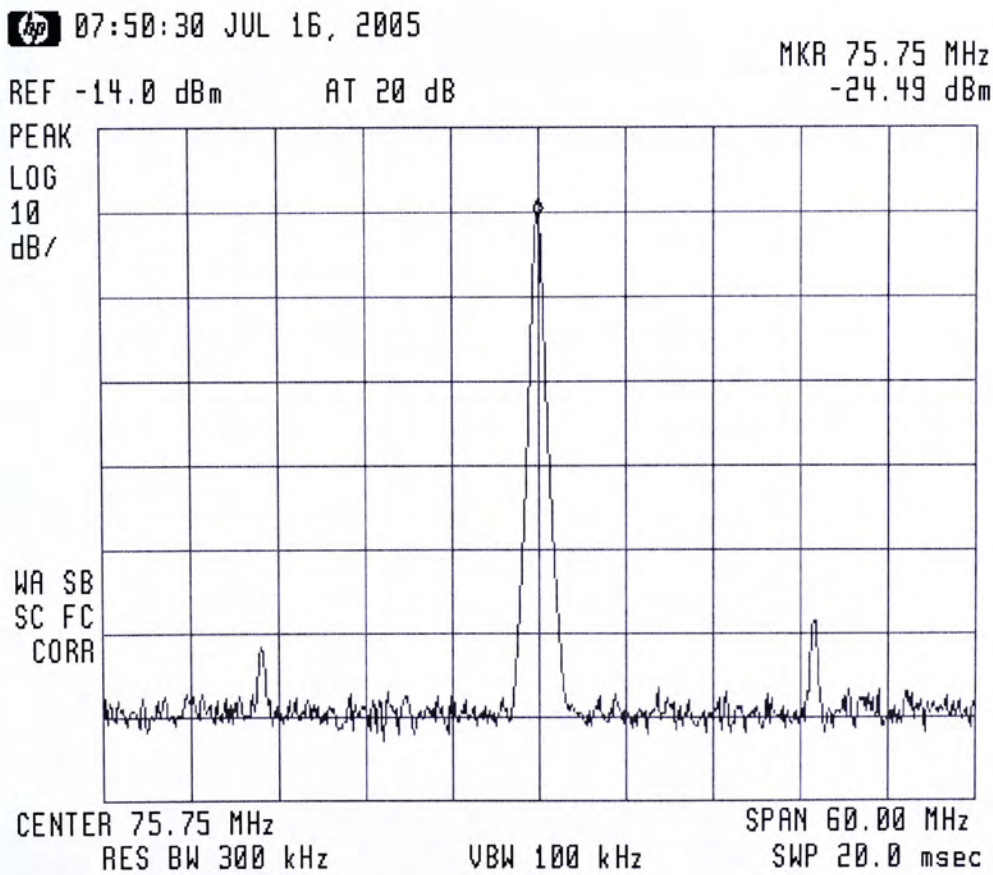


Figure 7.14: Output spectrum of divide-by-33 operation ($f_{IN} = 2.5\text{GHz}$)

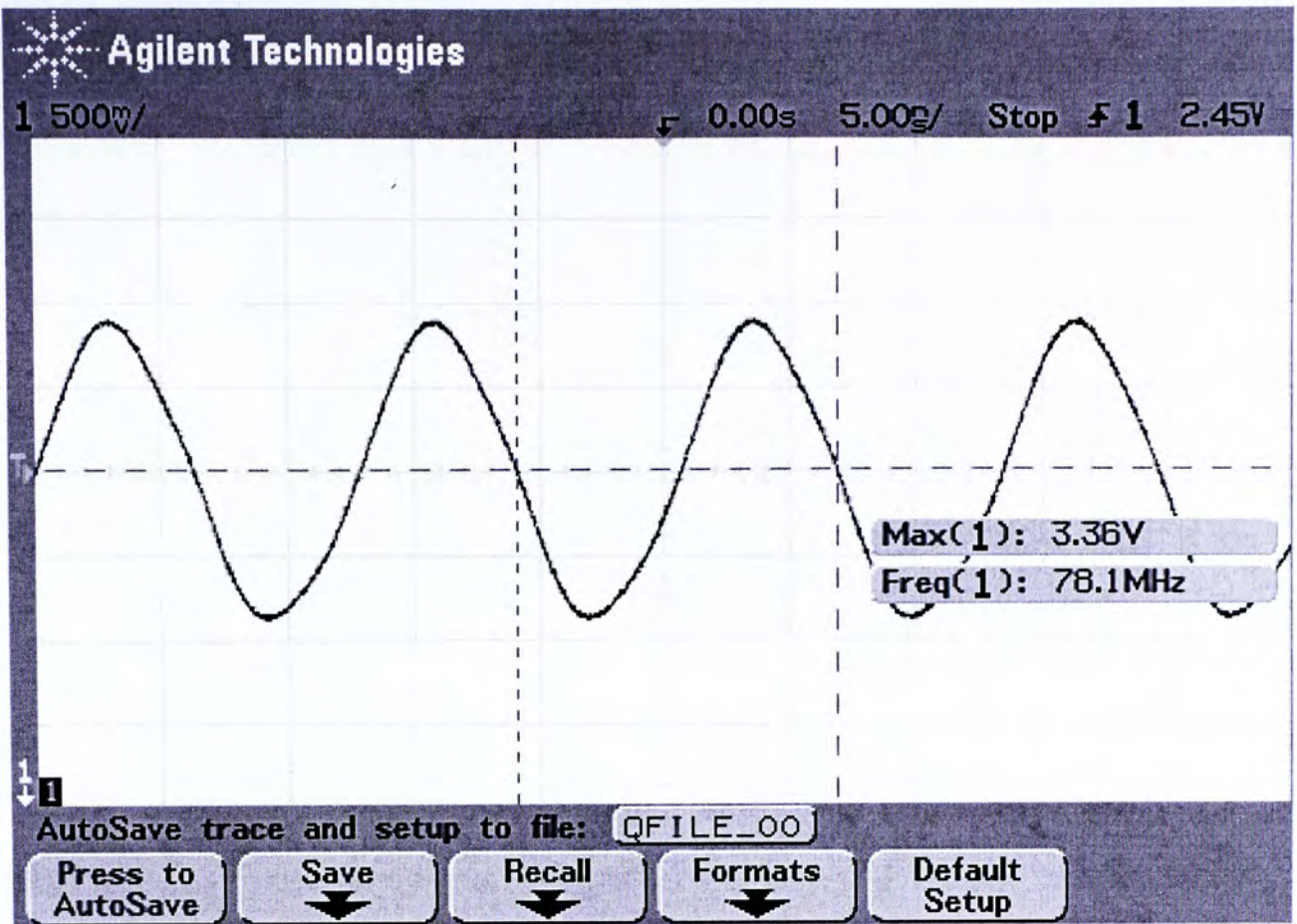


Figure 7.15: Output waveform of divide-by-32 operation ($f_{IN} = 2.5\text{GHz}$)

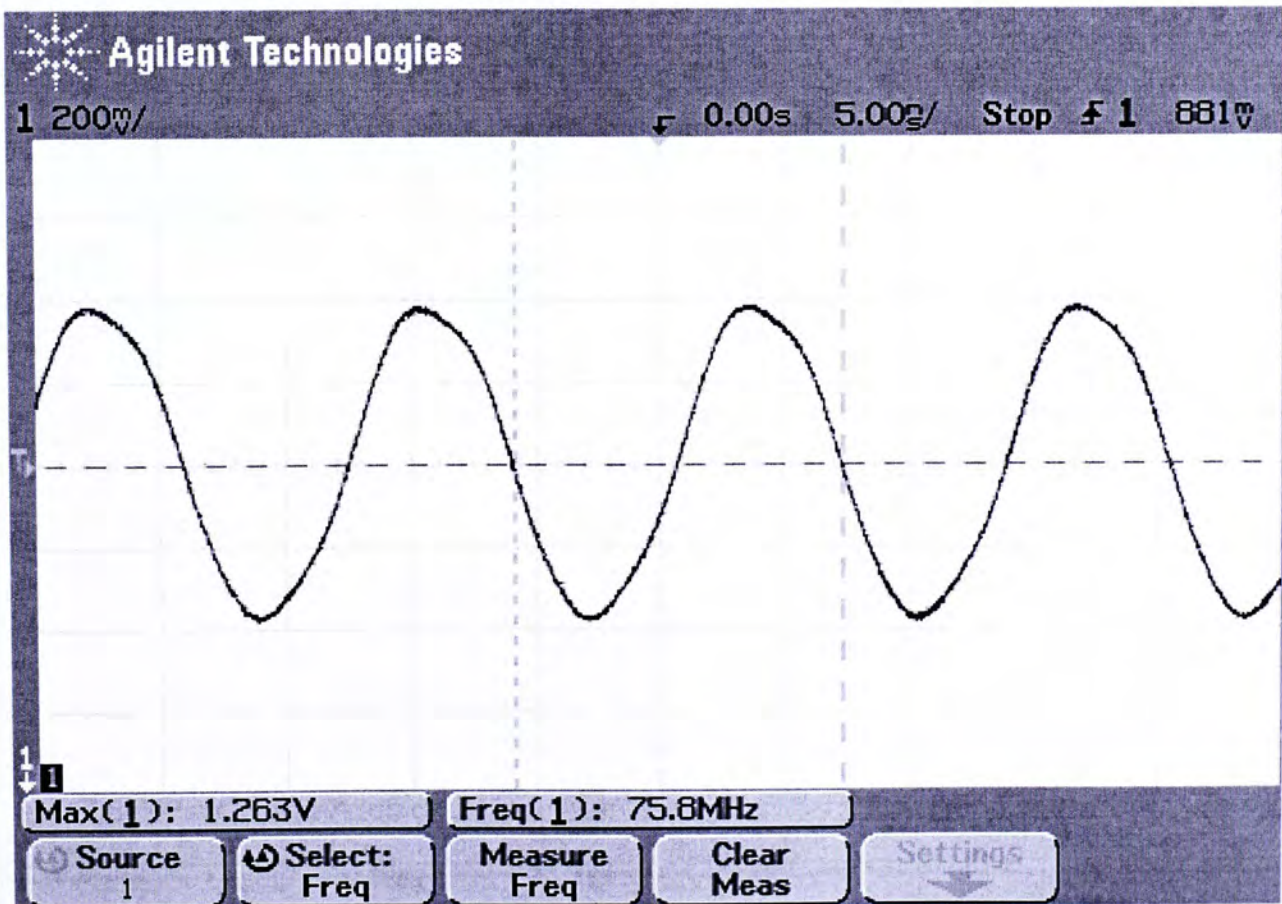


Figure 7.16: Output waveform of divide-by-33 operation ($f_{IN} = 2.5\text{GHz}$)

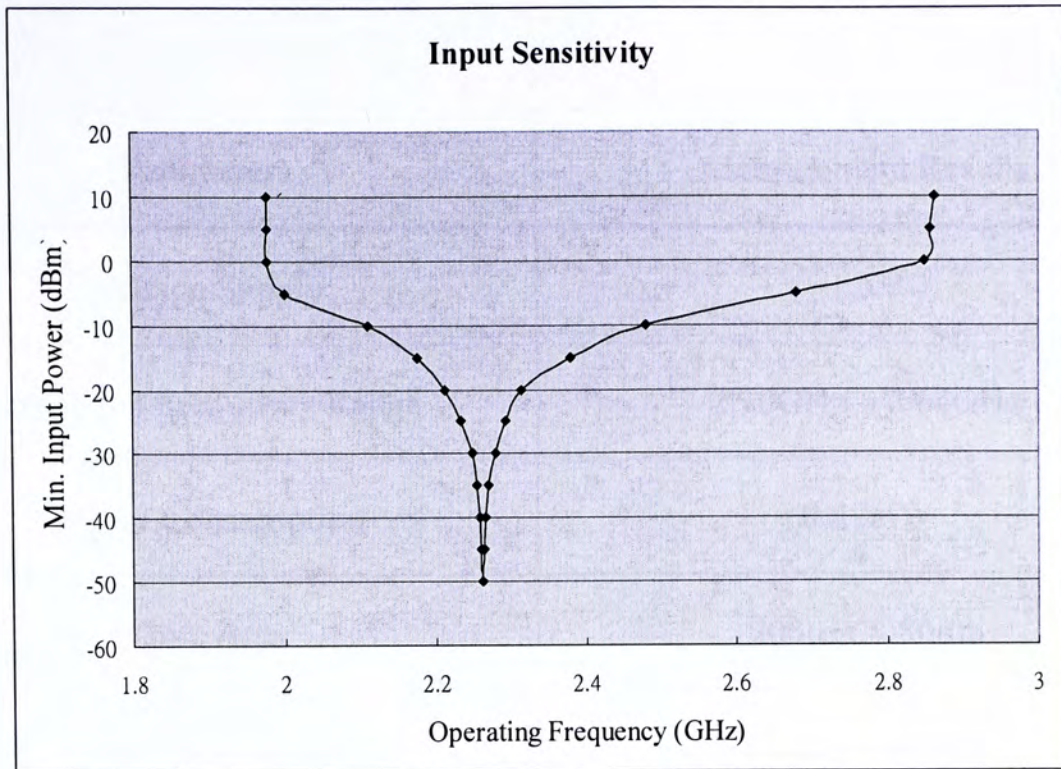


Figure 7.17: Measured minimum input power versus frequency

7.3 Summary

The performance of the three DMP designs, namely the 3V 900MHz low noise DMP, the 1.5V 2.4GHz low power DMP and the 1.5V 2.4GHz wideband DMP, are summarized in Table 7.2, Table 7.3 and Table 7.4 respectively.

Parameters	Measurement Results
Voltage Supply	3V
Operating Frequency Range	50MHz - 1.1GHz
Power Consumption	12mW
Core Area	220 μ m \times 130 μ m
DMP Architecture	Pre-processing clock

Table 7.2: Performance of the low noise DMP

Parameters	Measurement Results
Voltage Supply	1.5V
Operating Frequency Range	2.10GHz – 2.64GHz
Power Consumption	0.87mW
Core Area	200 μ m \times 80 μ m
DMP Architecture	Phase-switching

Table 7.3: Performance of the low power DMP

Parameters	Measurement Results
Voltage Supply	1.5V
Operating Frequency Range	1.98GHz – 2.88GHz
Power Consumption	1.02mW
Core Area	186 μ m \times 65 μ m
DMP Architecture	Phase-switching

Table 7.4: Performance of the wideband DMP

Chapter 8

Conclusions and Future Works

8.1 Conclusions

In PLL frequency synthesizer, DMP is one of the most challenging sub-circuits. It is known to be the major bottleneck on operating frequency of PLL and it is also one of the most power consuming building blocks in PLL. Simultaneous switching noise in prescaler coupling to analog blocks and the noise generated itself will also affect the phase noise performance of the PLL. The main objective of this research is to implement high performance DMP for RF frequency synthesizer applications.

In this thesis, different architecture of DMP and different divider design techniques are reviewed. Three prototypes namely a 3V 900MHz low switching noise DMP, a 1.5V 2.4GHz ultra low power DMP and a 1.5V 2.4GHz wideband DMP have been designed, laid out, fabricated and characterized using AMS 0.35 μ m standard CMOS process.

The first DMP design makes use of source coupling logic (SCL) and pre-processing clock technique in differential mode for implementation. This DMP generates less switching noise and has better noise immunity. The occupies approximately 220 μ m \times 130 μ m active area. At a supply voltage of 3V, current consumption was found to be about 4mA at an input frequency of 960MHz. The maximum operating frequency is about 1.1GHz.

The second prototype demonstrates a low power consumption design of DMP. Ultra low power consumption is achieved by using only one DFF in the divide-by-4

design and no power-hungry synchronizing circuits to solve the glitch problem. The core size of the chip is approximately $200\mu\text{m} \times 80\mu\text{m}$ and it is measured to operate from 2.08 to 2.66GHz at 1.5V supply voltage. The experimental circuit was found to have a consumption of less than 1mW.

The third design is aimed to extend the bandwidth of the second design as well as maintaining low power consumption. The proposed DMP is based on the architecture in the second design, except two divide-by-2 circuits are used to realize the full-speed divide-by-4 circuit. For further speed enhancement, proper circuit technique is also applied to reduce the load capacitance at critical output nodes. The active area of the chip is approximately $186\mu\text{m} \times 65\mu\text{m}$. It was measured to operate from 1.98GHz to 2.88GHz at 1.5V supply voltage. The experimental circuit was found to have a power consumption of 1.02mW.

8.2 Future Works

As the maximum operating speed among the three designs is 2.4GHz, it is not applicable to other applications operating at higher frequency bands, such as WLAN 802.11a at 5GHz. Since there are very few DMPs can achieve the 5GHz range using the low cost standard $0.35\mu\text{m}$ process, designing a 5GHz DMP can be one of the research works in the future.

Recently, there are many low voltage synthesizers operating at 1V supply [38-40]. Although we have tried 1.5V supply voltage in the designs, there still have room to lower the supply voltage. Therefore, another possible future development is to design a high speed DMP under the 1V supply voltage. .

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