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# Reduced 1/$f$ noise in $p$-Si$_{0.3}$Ge$_{0.7}$ metamorphic metal–oxide–semiconductor field-effect transistor

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We have demonstrated reduced 1/$f$ low-frequency noise in sub-$\mu$m metamorphic high Ge content $p$-Si$_{0.3}$Ge$_{0.7}$ metal–oxide–semiconductor field-effect transistors (MOSFETs) at 293 K. Three times lower normalized power spectral density (NPSD) $S_{I_D}/I_D^2$ of drain current fluctuations over the 1–100 Hz range at $V_{DS} = -50$ mV and $V_G - V_{th} = -1.5$ V was measured for a 0.55 $\mu$m effective gate length $p$-Si$_{0.3}$Ge$_{0.7}$ MOSFET compared with a $p$-Si MOSFET. Performed quantitative analysis clearly demonstrates the importance of carrier number fluctuations and correlated mobility fluctuations (CMFs) components of 1/$f$ noise for $p$-Si surface channel MOSFETs, and the absence of CMFs for $p$-Si$_{0.3}$Ge$_{0.7}$ buried channel MOSFETs. This explains the reduced NPSD for $p$-Si$_{0.3}$Ge$_{0.7}$ MOSFETs in strong inversion. © *2004 American Institute of Physics.*
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Low-frequency (LF) noise is becoming a major concern for continuously scaled down Si metal–oxide–semiconductor field-effect transistor (MOSFET) devices, since the 1/$f$ noise increases as the reciprocal of the device area. Excessive LF noise and fluctuations could lead to serious limitations on the functionality of analog and digital circuits. Replacing bulk Si MOSFETs with a buried channel SiGe hetero-MOSFET could significantly reduce 1/$f$ noise and increase drive current. We have demonstrated a reduced normalized power spectral density (NPSD) $S_{I_D}/I_D^2$ of drain current fluctuations in a metamorphic high Ge content $p$-Si$_{0.3}$Ge$_{0.7}$ MOSFET compared to a bulk $p$-Si one. Previously, reduced LF noise was reported in pseudomorphic $p$-SiGe MOSFETs in comparison with $p$-Si.[1–5] Opposite results were published as well.[4–6]

The multilayer SiGe heterostructure was grown by solid-source molecular-beam epitaxy (SS-MBE) on a $n$-type ($1 \times 10^{15}$ cm$^{-3}$) Si(001) wafer. It consists of a 2.5 $\mu$m relaxed Si$_{1-y}$Ge$_y$, linearly graded, virtual substrate with a final Ge composition $y = 0.4$, a 500 nm Si$_{0.6}$Ge$_{0.4}$:Sb ($5 \times 10^{17}$ cm$^{-3}$) doped layer acting as a "punch-through stopper" to avoid short channel effects, a 5 nm Si$_{0.6}$Ge$_{0.4}$ spacer layer, a 9 nm compressive-strained Si$_{0.3}$Ge$_{0.7}$ channel, and a 4 nm tensile-strained Si cap layer. The $p$-Si$_{0.3}$Ge$_{0.7}$ MOSFET devices were fabricated using a reduced thermal budget process at 650 °C to minimize Ge outdiffusion from the strained Si$_{0.3}$Ge$_{0.7}$ channel[7] and to avoid Sb penetration into the channel. The 200 nm of SiO$_2$ was deposited by plasma enhanced chemical vapor deposition (PECVD) as a field oxide. In the active transistor area, the field oxide was removed by wet chemical etching. After a cleaning step, the gate oxide was fabricated by depositing a 7 nm remote PECVD (RPECVD) SiO$_2$ layer at 330 °C, followed by an anneal in N$_2$O ambient at 650 °C for 1 min. The source and drain contacts were fabricated by BF$_2^+$ implantation at an energy 40 keV, dose of $4 \times 10^{15}$ cm$^{-2}$, and activated at 650 °C for 30 s. Finally, Al gate and Ti/Pt/Au contacts metallization were evaporated. The $p$-Si MOSFET devices were fabricated on SS-MBE grown 100 nm Si epilayers on $n$-type ($1 \times 10^{17}$ cm$^{-3}$) Si(001) wafers using a self-aligned gate process with 9 nm of dry thermally grown SiO$_2$ at 800 °C for 120 min and had a 300 nm $p$-type ($5 \times 10^{19}$ cm$^{-3}$) polycrystalline silicon gate.

The LF noise was measured using an HP 35670A dynamic signal analyzer and custom-made preamplifier containing OPA637 (Texas Instruments) and LT1028 (Linear Technology) operational amplifiers in the first stage. All measurements were done on MOSFETs with an effective gate length of 0.55 $\mu$m and gate width 50 $\mu$m in an electrically shielded room at 293 K.

The LF noise measurements were performed at $V_{DS} = -50$ mV, from subthreshold to the strong inversion region ($V_G - V_{TH}$ from 0.5 to $-3$ V) of MOSFET operation. A typical NPSD $S_{I_D}/I_D^2$ of drain current fluctuations versus frequency in the range of $1-10^5$ Hz is presented in Fig. 1. The spectra are dominated by a flicker, 1/$f$ component, at LF and thermal noise in the high-frequency range. Over three times lower 1/$f$ noise for $p$-Si$_{0.3}$Ge$_{0.7}$ MOSFET is clearly visible from Fig. 1. We have not observed a generation–recombination (GR) noise component at any gate overdrive voltage. This is usually manifested as bumps in the spectra. GR noise could appear in the spectra due to Sb diffusion into the Si$_{0.3}$Ge$_{0.7}$ channel from the Sb-doped "punch-through" stopper or the existence of deep levels in the heterostructure. Thus, we can confirm the absence of these defects and contaminations after the full MOSFET fabrication process.

The NPSD $S_{I_D}/I_D^2$ in the 1/$f$ region is described in terms of carrier number fluctuations (CNFs), correlated mobility fluctuations (CMFs), and source–drain series resistance fluctuations (SDRFs):[8]

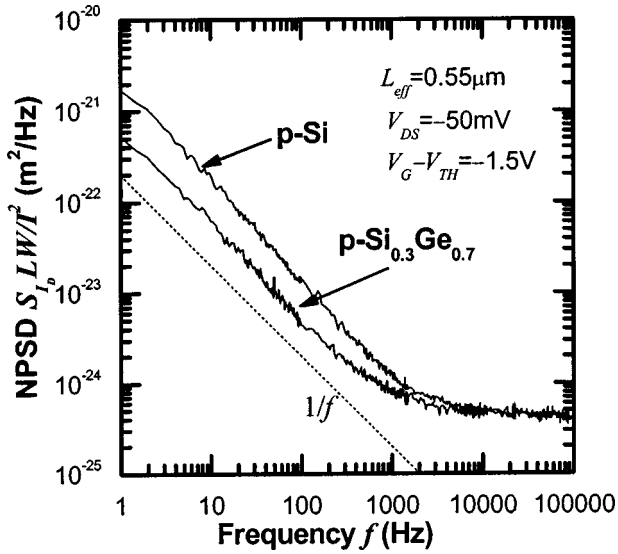[a]Electronic mail: m.myronov@warwick.ac.uk

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FIG. 1. NPSD of drain current fluctuations as a function of frequency for $p$-$\mathrm{Si}_{0.3}\mathrm{Ge}_{0.7}$ and $p$-Si MOSFETs.



FIG. 2. NPSD of drain current fluctuations as a function of overdrive gate voltage for $p$-$\mathrm{Si}_{0.3}\mathrm{Ge}_{0.7}$ and $p$-Si MOSFETs at $f=1$ Hz.

$$S_{I_D}/I_D^2 = (1+\alpha\mu_{\mathrm{eff}}CI_D/g_m)^2\left(\frac{g_m}{I_D}\right)^2 S_{V_{\mathrm{fb}}} + \left(\frac{I_D}{V_{DS}}\right)^2 S_{R_{SD}}, \tag{1}$$

where $\alpha$ is the Coulomb scattering coefficient, $\mu_{\mathrm{eff}}$ is the effective mobility, $S_{V_{\mathrm{fb}}} = S_{Q_{it}}/(WLC^2)$ is the flat-band voltage spectral density with $S_{Q_{it}}$ being the interface charge spectral density per unit area. $C$ is the gate oxide capacitance $C_{\mathrm{ox}}$, in the case of the Si MOSFET or $C_{\mathrm{ox}}C_{\mathrm{cap}}/(C_{\mathrm{ox}}+C_{\mathrm{cap}})$ in the case of the MOSFET with a SiGe buried channel separated from $\mathrm{SiO}_2$ by the Si cap layer with capacitance $C_{\mathrm{cap}}$. The maximum of effective mobility in $p$-Si and $p$-$\mathrm{Si}_{0.3}\mathrm{Ge}_{0.7}$ MOSFETs are 110 $\mathrm{cm}^2\,\mathrm{V}^{-1}\,\mathrm{s}^{-1}$ and 490 $\mathrm{cm}^2\,\mathrm{V}^{-1}\,\mathrm{s}^{-1}$, respectively. The flat-band voltage spectral density is defined by:[8,9]

$$S_{V_{\mathrm{fb}}} = \frac{q^2 k_B T N_{st}}{WLC_{\mathrm{ox}}^2 f^\gamma} = \frac{q^2 k_B T \lambda N_t}{WLC_{\mathrm{ox}}^2 f^\gamma}, \tag{2}$$

where $f$ is the frequency, $\gamma$ is the characteristic exponent close to unity, $k_B T$ is the thermal energy, $N_{st}$ is a density of traps near the $\mathrm{Si}/\mathrm{SiO}_2$ and/or $\mathrm{Si}/\mathrm{Si}_{0.3}\mathrm{Ge}_{0.7}$ interface, $\lambda$ is the tunnel attenuation distance to the Si cap and/or $\mathrm{SiO}_2$, and $N_t$ is the volumetric trap density in the Si cap and/or $\mathrm{SiO}_2$. The values of extracted fitting parameter $N_{st}$ in $p$-Si and $p$-$\mathrm{Si}_{0.3}\mathrm{Ge}_{0.7}$ MOSFETs are $5\times10^9$ $\mathrm{eV}^{-1}\,\mathrm{cm}^{-2}$ and $4\times10^8$ $\mathrm{eV}^{-1}\,\mathrm{cm}^{-2}$, respectively. The spectral density of SDRF is defined by:[10]

$$S_{R_{SD}} = \alpha_{H\_SD}\frac{R_{SD}^2}{fN_{SD}} \sim \frac{R_{SD}^2}{f}, \tag{3}$$

where $\alpha_{H\_SD}$ is the Hooge parameter for $1/f$ noise in the series resistance, $N_{SD}$ is the total number of free carriers, and $R_{SD}$ is the source–drain series access resistance. The extracted values of $S_{R_{SD}}$ for $p$-Si and $p$-$\mathrm{Si}_{0.3}\mathrm{Ge}_{0.7}$ MOSFETs are $7.0\times10^{-6}$ $\mathrm{ohm}^2\,\mathrm{Hz}^{-1}$ and $1.2\times10^{-7}$ $\mathrm{ohm}^2\,\mathrm{Hz}^{-1}$, respectively.

CMF can be important from the onset of strong inversion mode ($V_G \geq V_{\mathrm{TH}}$) of MOSFET operation. Typically,
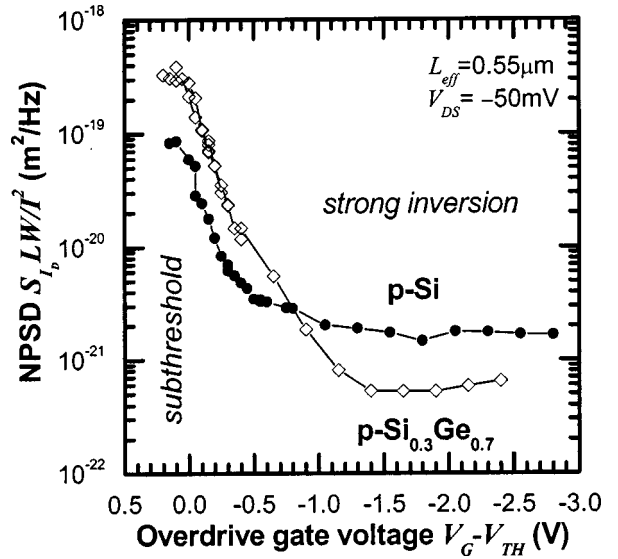
SDRF can appear at high gate voltages, when the channel resistance reduces to the value of source–drain series access resistance.

Figure 2 shows the NPSD of drain current fluctuations at $f=1$ Hz as a function of gate overdrive voltage. In the subthreshold region, the $1/f$ noise depends only on the number of traps near the $\mathrm{SiO}_2/\mathrm{Si}$ interface for the surface channel $p$-Si MOSFET and near both the $\mathrm{SiO}_2/\mathrm{Si}$ and $\mathrm{Si}/\mathrm{Si}_{0.3}\mathrm{Ge}_{0.7}$ interfaces for the buried channel $p$-$\mathrm{Si}_{0.3}\mathrm{Ge}_{0.7}$ MOSFET, and is described by CNF. In this region, the NPSD of the $p$-Si MOSFET is three times lower than in the $p$-$\mathrm{Si}_{0.3}\mathrm{Ge}_{0.7}$ (Fig. 2). This is explained by a better quality of thermally grown $\mathrm{SiO}_2$ at 800 °C in the $p$-Si MOSFET compared to the RPECVD deposited $\mathrm{SiO}_2$ at 330 °C in the $p$-$\mathrm{Si}_{0.3}\mathrm{Ge}_{0.7}$ device. In the strong inversion region, at $V_G - V_{\mathrm{Th}} = -1.5$ V, the NPSD of the $p$-$\mathrm{Si}_{0.3}\mathrm{Ge}_{0.7}$ MOSFET is more than three times lower than in $p$ Si. At high gate overdrive voltages, the NPSD of the $p$-$\mathrm{Si}_{0.3}\mathrm{Ge}_{0.7}$ MOSFET slightly increases. This indicates the stronger contribution of SDRF because of source–drain series access resistance becomes comparable to the channel region resistance at high gate overdrive voltages.

Figure 3 shows how measured and calculated power spectral density (PSD) vary with device conductance for the $p$-Si MOSFET. This curve fit very well with CNF, CMF, and SDRF using Eq. (1). The Coulomb scattering coefficient $\alpha = 8\times10^4$ V s/C extracted from the fitting of experimental data for a $p$-Si MOSFET is close to the predicted value of $10^5$ V s/C for holes.[8]

Figure 4 shows the variation of PSD with device conductance for the $p$-$\mathrm{Si}_{0.3}\mathrm{Ge}_{0.7}$ MOSFET. It is completely explained with CNF and SDRF, which reduces Eq. (1) for the NPSD to

$$S_{I_D}/I_D^2 = \left(\frac{g_m}{I_D}\right)^2 S_{V_{\mathrm{fb}}} + \left(\frac{I_D}{V_{DS}}\right)^2 S_{R_{SD}}. \tag{4}$$

This behavior is caused by the difference in the distance from traps near the $\mathrm{Si}/\mathrm{SiO}_2$ interface to carriers in the surface Si channel, and the $\mathrm{Si}_{0.3}\mathrm{Ge}_{0.7}$ buried channel separated by a 4 nm Si cap layer from the $\mathrm{SiO}_2$. This was confirmed by the
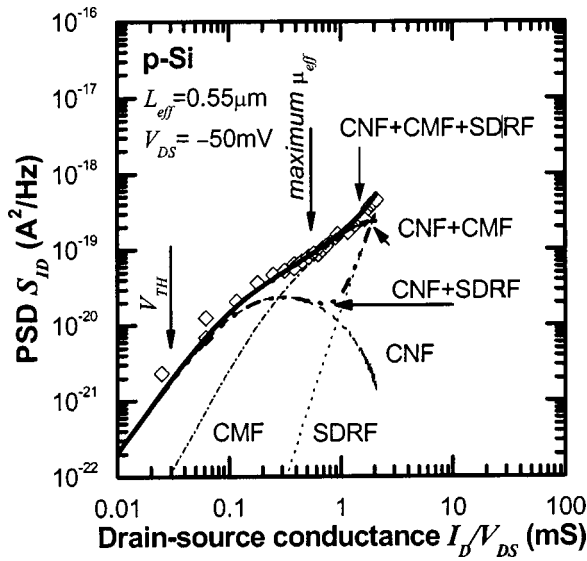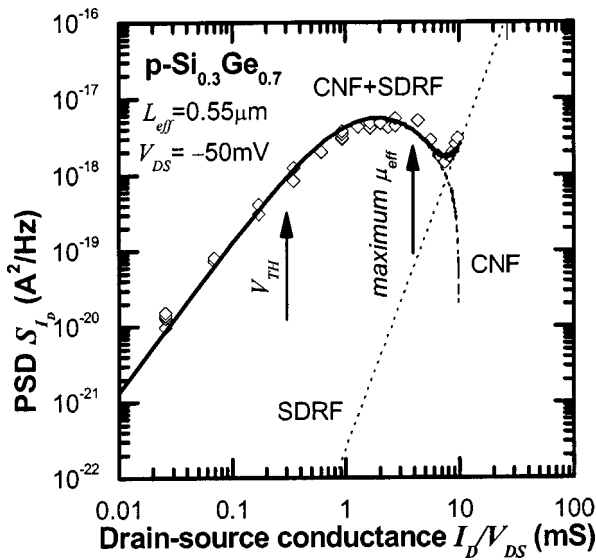
FIG. 3. PSD dependence on device conductance for *p*-Si MOSFET at *f* = 1 Hz. Open diamonds correspond to measured PSD.
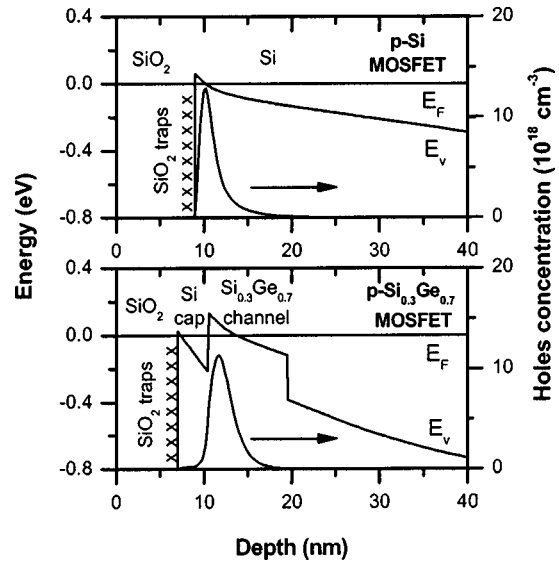


FIG. 5. Valence-band energy diagrams and holes concentration profiles for *p*-Si and *p*-Si$_{0.3}$Ge$_{0.7}$ MOSFETs at applied $V_G - V_{TH} = -1.5$ V.

self-consistent solution of Schrodinger–Poisson equations for both devices (Fig. 5). In the strong inversion region of MOSFET operation, these traps act as powerful fluctuating scattering centers for holes in the channel.

In conclusion, a significant reduction in LF noise in a high Ge content metamorphic *p*-Si$_{0.3}$Ge$_{0.7}$ MOSFET com-

pared to a bulk *p*-Si MOSFET designed for deep sub-$\mu$m technology was reported. This advantage was realized in devices with $L_{eff}$=0.55 $\mu$m, which is pertinent to current Si technology. In the linear region of MOSFET operation, the reduction in $1/f$ noise of NPSD is greater than a factor of 3. PSD in the *p*-Si MOSFET was well described with the help of CNF, CMF, and SDRF components of $1/f$ noise. Analysis of the *p*-Si$_{0.3}$Ge$_{0.7}$ MOSFET PSD showed the absence of CMF component due to the existence of the Si cap layer in the *p*-Si$_{0.3}$Ge$_{0.7}$ MOSFET, which further separates the holes in the buried Si$_{0.3}$Ge$_{0.7}$ channel from traps near the Si/SiO$_2$ interface.



FIG. 4. PSD dependence on device conductance for *p*-Si$_{0.3}$Ge$_{0.7}$ MOSFET at *f* = 1 Hz. Open diamonds correspond to measured PSD.

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