A Study of the Device Characteristics of a Novel Body-Contact SOI Structure

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Content

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Abstract

Silicon-On-Insulator (SOI) technology is known to have improved device performance over bulk silicon counterpart for the same design geometry in terms of switching speed, packing density, process simplicity and other overall characteristics. In view that bulk silicon devices technology is reaching its geometry physical limits as well as the substantial investment cost for moving into deep sub-micron region, SOI technology has received increasing attentions and are becoming an attractive alternative or even replacement of bulk silicon devices particularly in the low voltage and Ultra Large Scale Integration (ULSI) applications.

In this work, we have performed a detailed study of the device characteristics of a particular Body-Contact SOI (BCSOI) structure. The BCSOI structure is constructed in such a way that when using implantation method for substrate preparation, the silicon overlayer quality underneath the entire gate region is persevered to be as good as in bulk silicon structure.

Buried insulator layers, either using oxide or nitride, with or without body contact opening are directly put underneath the source and drain junctions of a bulk silicon nMOS structure for computer simulation comparisons. Key performance characteristics including back body effect, current-voltage (I-V) curves, transconductance and subthreshold swing of an nMOS transistor built on different substrate structure are extracted and studied in details. Dependence on fundamental SOI structure parameters such as buried insulator thickness, silicon overlayer thickness and body contact size are also explored.

It was revealed that an nMOS transistor built on BCSOI structure is free of

floating body effects, the undesirable phenomenon that associated with conventional SOI devices. Although the overall device performance of the device on BCSOI structure does not have significant improvements over those on bulk silicon structure, the existence of an insulator underneath the junctions enable it to have similar switching speed as if of conventional SOI devices.

Due to having an opening in the buried insulator, an inverter built on BCSOI structure are prone to latch-up. By constructing an equivalent pMOS transistor, the latch-up susceptibility characteristics of such a CMOS inverter are examined. The dependence on buried insulator thickness, n-well depth, transistor separation and body contact size are also characterized.

Despite of using one additional mask, the overall processing cycling time and cost of BCSOI structure are estimated to be not exceeding those of conventional SOI structure. Above all, the BCSOI structure enables ease of oxidation after nitrogen implantation when constructing devices on nitride insulating structure using implantation method. All in all suggest that the BCSOI structure shall be an viable alterative for consideration especially when silicon on nitride applications are in concern.

Chapter 1 Introduction

Devices fabrication in the Very Large Scale Integration (VLSI) scale is a costly and time-consuming process nowadays. As device simulation software are capable of predicting device characteristics in a more and more accurate manner, new design will undergo comprehensive simulation prior to actual device fabrication, thereby rendering it as an verification step. In view that more and more attention are paid to silicon-on-insulator (SOI) technology and in particular to the performance improvement of devices built on modified SOI structures, such studies are made possible and easier with the help of accurate two-dimensional simulation software.

1.1 Perspective

SOI technology is now considered an alternative choice when considering moving further into deep sub-micron geometry technology. SOI CMOS technology is known to have improved device performance over bulk silicon counterpart for the same design geometry. Cost is the primary reason that retained SOI technology from wide proliferation in the past. However, in view of the heavy investment for deep sub-micron bulk silicon technology, the recent breakthrough in SOI technology researches and the lowering of SOI substrate cost have make people to have second thought on SOI technology.

Two dimensional numerical simulation software usually focus on the studying of one single, or at most a few, devices on a pre-defined structure. Not only the

electrical behaviour of the devices at many bias conditions can be simulated, various features such as Fermi level, potential distribution contour, current flow direction within the entire device structure can also be visualized. These provide device designers additional important information of the device under design which cannot be obtained by measuring the electrical behaviour of actual devices. Simulation software therefore always has their place in the realm of device design.

1.2 MEDICI - The Simulation Package

MEDICI is an upgraded simulation package of the previously known PISCES-2B simulation software. Both of them were developed and marketed by Technology Modelling Association, Inc.

PISCES-2B is a numerical simulation package that models two-dimensional distributions of potential and carrier concentration in devices to predict electrical characteristics for many bias conditions. It solves Poisson's equation and both the electron and hole current-continuity equations to analyze devices and effects even if the current flow involves both types of carriers. In addition to the functions provided by PISCES-2B, MEDICI is also capable of performing simple SPICE-type circuit analysis to devices, thereby making MEDICI a more self-sufficient tool for device and circuit simulations.

Simulations are performed according to a pre-defined source file which describes how a structure is built. By manipulating the source file, structures of various combinations can be constructed. Performance of device built on them can therefore be extracted without the need to actually fabricating the devices - a significant savings of time and money.

Throughout this thesis, MEDICI is the simulation tool. A detailed illustration of the simulation source file is provided in Appendix A.

1.3 Overview

The objective of this work is to use computer simulation to characterize a transistor that is built on a Body-Contact Silicon-On-Insulator (BCSOI) structure and compare its performance to those on bulk silicon structure and conventional SOI structure, either using oxide or nitride as the insulating layer.

In Chapter 2, the emergence of SOI devices is presented. Aspects such as the advantages, categories, drawbacks, manufacturing methods and future trend of conventional SOI devices are illustrated. Special notes on the quest for silicon-on-nitride structure is also made.

A description of the BCSOI structure is presented in Chapter 3. Apart from the construction of the BCSOI structure, its impact on the substrate manufacturing and device fabrication sequence is also discussed and compared to bulk silicon and conventional SOI technique.

The basic methodology of computer simulation of device is explained in Chapter 4. The construction of a source file for simulation and the simulation software, MEDICI, are presented. Structures to be simulated are also built up and described in details.

The simulation results of a nMOS transistor built on different structures are reported in Chapter 5. Performance of the transistors on various structures are characterized and compared in terms of body effect, current-voltage characteristics, transconductance and subthreshold region properties. Dependence of the

characteristics of the BCSOI structure on parameters including buried insulator thickness, silicon overlayer thickness and body-contact size are also studied.

The main purpose of Chapter 6 is to investigate the latch-up susceptibility of a CMOS inverter on the BCSOI structure. In the consideration of manufacturing latitude, dependence of the latch-up susceptibility on the structure parameters such as buried insulator thickness, well junction depth, separation of the transistors and body contact size are also explored.

Finally, a summary of this thesis and recommendations for future work are given in Chapter 7 as the concluding chapter.

Chapter 2 The Emergence of SOI Devices

2.1 Introduction

Silicon-on-insulator (SOI) devices, because of their radiation hardness feature, was firstly introduced over 30 years ago, primarily for special niche applications such as space and military electronics. Due to the high cost in substrate preparation, commercial applications were, however, rare.

Nevertheless, SOI devices excel conventional bulk silicon devices in switching speed, packing density, process simplicity and other overall performance. In view that bulk silicon device technology is reaching its geometry physical limits, given the improvement in substrate manufacturing methods, which means more cost-effectiveness, SOI technology now receives extensive researches and studies. Regardless of their few drawbacks, SOI devices are becoming an attractive alternative or even replacement of bulk silicon devices particularly in the low voltage and deep sub-micron Ultra Large Scale Integration (ULSI) applications.

In this chapter, apart from highlighting the SOI technology development, classification of them as well as the various substrate preparation methods are also reviewed. The trend in future development and the quest for silicon-on-nitride structure are also presented.

2.2 Advantages of SOI Devices

Shown in Figure 2.1 is a schematic configuration of CMOS transistors in bulk silicon and SOI wafers. One can see that devices that are built on SOI wafers

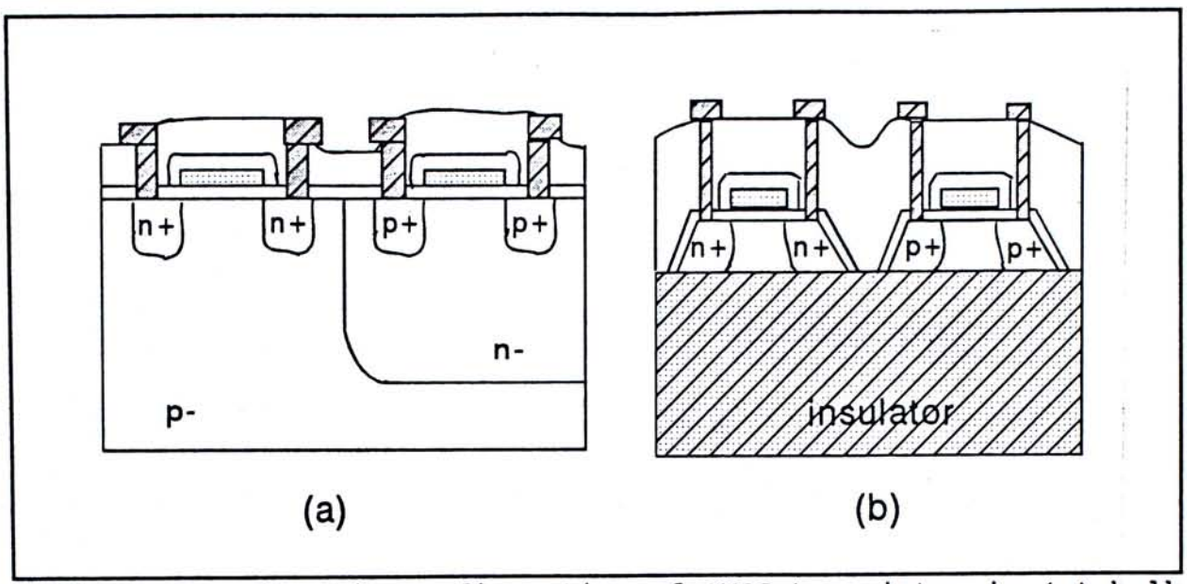


Figure 2.1 Schematic configuration of CMOS transistor in (a) bulk silicon and (b) SOI wafers.

are isolated form each other. As a result of the isolation, SOI devices, in many aspects, have advantages over bulk silicon devices. Invariant to different types of SOI substrate configuration, the advantages of SOI devices may be classified into four areas:

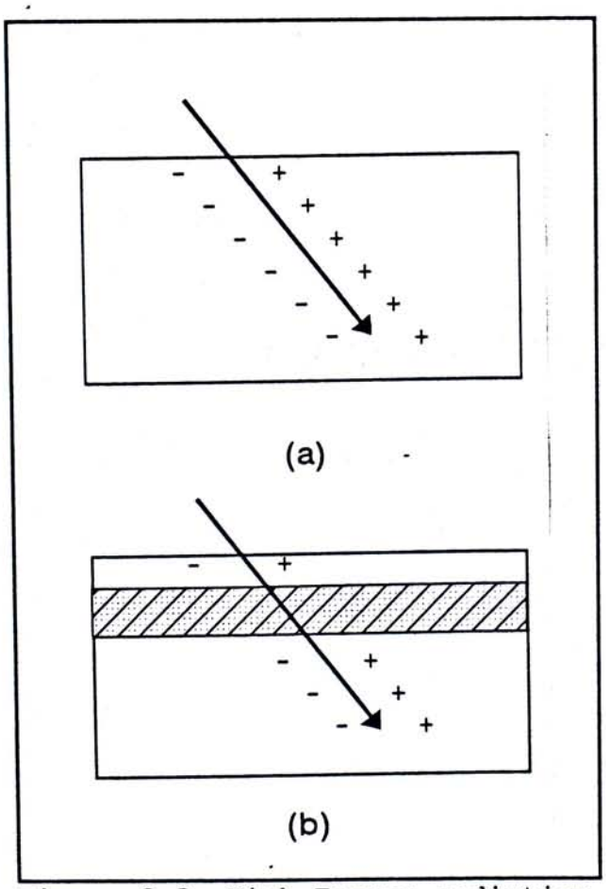


Figure 2.2 High Energy radiation causes ionization in a (a) bulk silicon and (b) SOI wafer.

2.2.1 Reliability Improvement

SOI devices have long been used primarily in military and space electronics where harsh environment is always encountered. When a radiation strikes a semiconductor device, electron-hole pairs are generated along the path of radiation (Figure 2.2a). The

number of electron-hole pairs that are generated is proportional to the radiation intensity. The generated electrons are then attracted by V_{dd} while holes migrate to V_{ss}. When such a current flow become significant as compared to the storage charge as in state-of-the-art DRAM cell, for instance, it will upset the logic state in cell, leading to what is termed "soft error", or Single Event Upset (SEU).

Due to the isolation feature, most of the generated electron-hole pairs are confined in the substrate region of a SOI wafer and do not interact with the surface active region (Figure 2.2b). With such a structure, improvement of radiation resistance of a circuit that is subject to 5MeV alpha particle doses was found to be over two orders of magnitude (Guerra, 1990; Guerra et. al., 1990).

2.2.2 Total Isolation

The isolation feature offered by SOI substrate makes them far more shrinkable than their bulk counterpart (Figure 2.3). Researchers found that integrated circuits on SOI substrate can be designed to occupy 30 to 40% less space than bulk silicon circuits (Peter 1993). The isolation, which does not call for the formation of well. Nor the need for digging high aspect ratio trench, can be easily realized by simpler

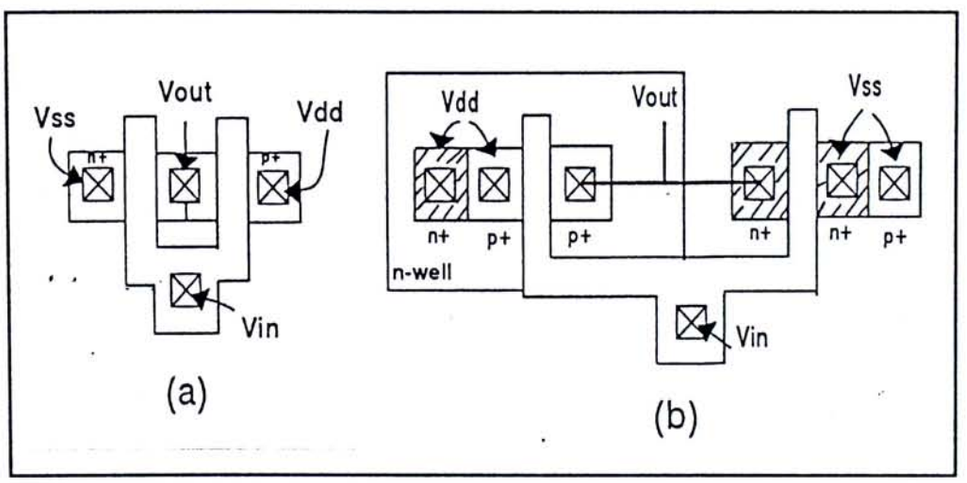


Figure 2.3 A SOI CMOS invertor (a) occupies less space than a bulk CMOS invertor (b).

processing, a saving of over 20% has been estimated (Peter, 1993). The absence of well in SOI substrate is conducive to much lower junction leakage current. SOI devices have thus been designed to work in high temperature (>350°C) with no degraded performance. Latch-up susceptibility is a major problem for ULSI bulk device technology in which devices are closely placed. In SOI devices, since N-transistors and P-transistors are completely isolated so that there is no path connecting them together. SOI devices are indeed latch-up free.

2.2.3 Improved Junction Structure

The special junction structure of SOI devices substantially lower parasitic junction capacitance and hence reduces propagation delay and dynamic power dissipation in circuits (Hosack et. al., 1990; Guerra, 1990). SOI devices can have undegraded performance even at reduced supply voltage which is the key prerequisite for low voltage LSIs applications (Auberton-Herve et. al., 1995; Nishimura, 1994).

In bulk CMOS devices, the parasitic drain-to-substrate (or source-to-substrate) capacitance consists of two components: the capacitance between the junction and the substrate itself, and the capacitance between the junction and the channel stop implant under the field oxide (Figure 2.4a). The parasitic junction capacitance become more significant as the increase of substrate doping concentration which is needed as device geometry is shrunk.

In SOI devices, junctions reach the isolation layer (Figure 2.4b). Hence, the junction capacitance only has one component: the capacitance between the junction and the substrate. Such a capacitance can only be smaller than those in a typical

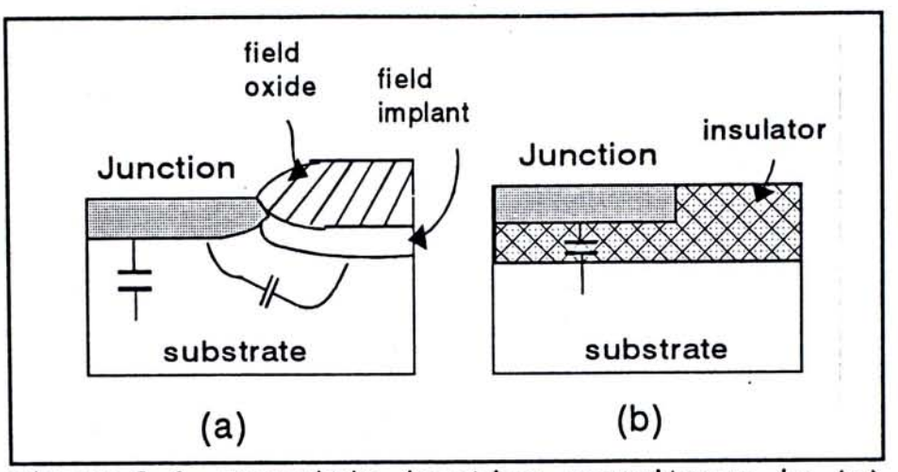


Figure 2.4 Parasitic junction capacitance in (a) bulk silicon and (b) SOI wafers

bulk silicon MOS structure. Note that the thickness of the buried insulator does not need to be scaled down as devices shrink. This reinforces the junction capacitance advantage of SOI over bulk even in sub-micron dimensions.

The existence of a buried insulator underneath the devices not only reduces the junction capacitance, but also all the capacitance between the silicon substrate and other terminals. Table 2.1 presents typical capacitance of a bulk and a SOI 1μm processes (Colinge, 1991). The reduction of capacitance is most noticeable in junction capacitance, but one can observe that even metal 1-to-substrate capacitance can be reduced by 40% by using SOI substrate than bulk silicon wafers.

Table 2.1 : Parasitic capacitance (pF/μm^2) found in typical bulk and SOI 1μm CMOS processes (Colinge, 1991).

Capacitor Type	SOI (SIMOX)	Bulk	Gain (SOI over bulk)
Gate	1.3	1.3	1
Junction-to-substrate	0.05	0.2 to 0.35	4 to 7
Polysilicon-to-substrate	0.04	0.1	2.5
Metal 1-to-substrate	0.027	0.05	1.85
Metal 2-to-substrate	0.018	0.021	1.16

2.2.4 Integrated Device Structure

Apart form being used to produce mainstream, ULSI and power devices, the SOI structure also has extensive applications in optoelectronics, microwave, bipolar, smart sensors and smart power applications (Auberton-Herve and Nishimura, 1994).

With the dielectric isolation existing under the monocrystalline silicon layer, a large variety of devices, such as DMOS, CMOS, high-voltage PMOS, bipolar, Schottky diodes etc., can be integrated on the same SOI wafer. An intelligent power LSI has been demonstrated (Vogt et. al., 1991). In the structure as shown in Figure 2.5, it is consisted of high voltage DMOS and low voltage controlling CMOS on one single chip. Appropriate shielding allows switching of 10A at 500V without influencing the low voltage circuitry. Switching inductive loads is also easy.

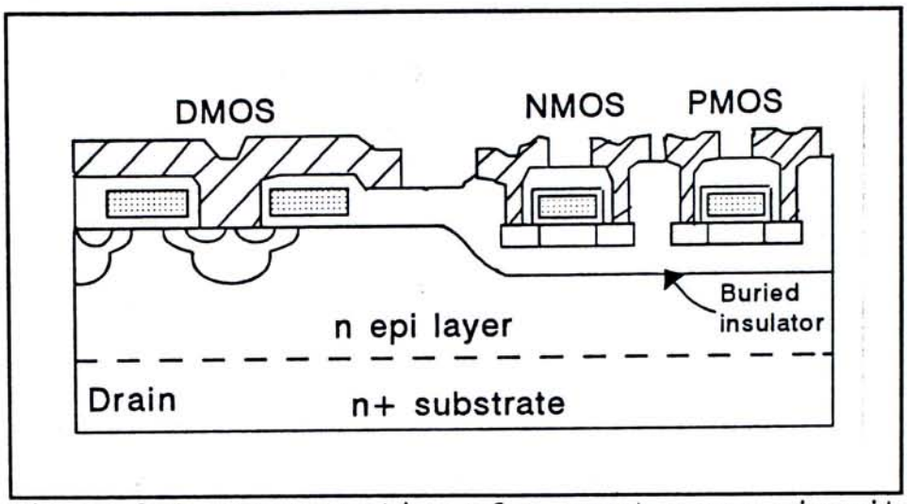


Figure 2.5 Cross-section of a smart power circuit showing cells of the DMOS transistor and the CMOS n- and p-channel devices on the buried oxide (Vogt et. al., 1991).

Another application of SOI technology is 3-Dimensional (3-D) circuits. A lot of efforts especially in Japan have been placed into this direction with a goal of integrating more than 10 device layers on top of each other (Ryssel et. al. 1993).

2.3 Categories of SOI Devices

Despite that SOI MOSFETs can be made on SOI substrate that are prepared by various methods, their physics performance depends primarily on the thickness of the silicon overlayer of the substrate and the channel doping concentration. Three categories of SOI device can be distinguished as a result.

Consider a typical SOI NMOS transistor as shown in Figure 2.6. Apart from the conventional bulk silicon MOS parameters, two additional thickness are important. They are

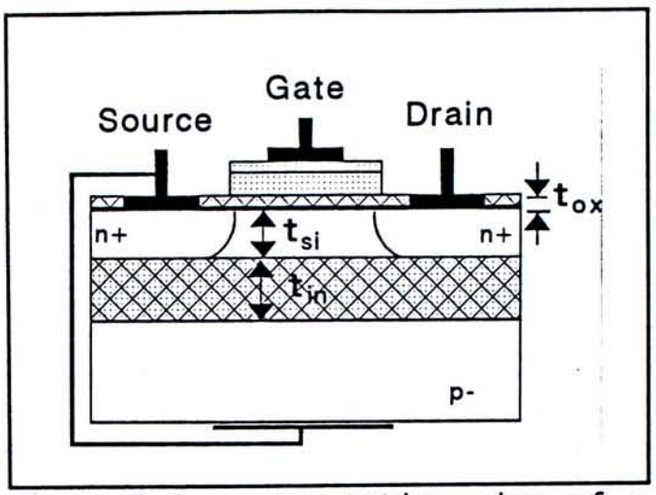


Figure 2.6 Cross-section view of a SOI NMOS transistor.

i) t_{si} : the thickness of top silicon overlayer; and

ii) t_{in} : the thickness of the insulator layer.

The choice of t_{si} determines the category of SOI devices while the choice of t_{in} is a trade-off between cost and device properties advantages.

In a bulk silicon MOS device, the depletion zone under the Si-SiO_2 interface extends into the bulk up to a maximum depth of X_{dmax}, which is classically given by:

$$X_{dmax} = \sqrt{\frac{4\ \epsilon_{si}\ \Phi_B}{q\ Na}}$$

Φ_B is the Fermi potential which is also expressed as $\frac{kT}{q} \ln \frac{Na}{n_i}$;

ϵ_{si} is the permissivity of silicon which is 1.05E-12 F/cm;
Na is the substrate dopant concentration; and
q is the charge equivalent of an electron, i.e. 1.6E-19C.

In SOI MOSFET, such a depth not only extends from the front gate down into the channel but also from the back side up into the channel as well. Both of the extension have to be considered upon classification.

2.3.1 Thick Film SOI Devices

SOI devices with $t_{si} > 2\ X_{dmax}$ are classified as Thick Film SOI devices.

In this type of device, the depletion zones extend from the front gate and back gate do not interact with each other. There exists a "neutral" silicon region, called body, in between the depletion zones. A thick film SOI device behaves exactly like a bulk silicon device if the body region is grounded. However, if it is left floating, although the SOI device will behave basically like a bulk silicon device, undesirable parasitic bipolar effects will be noticeable (refer to section 2.4.2 for details).

2.3.2 Thin Film SOI Devices

SOI devices with $t_{si} < X_{dmax}$ are classified as Thin Film SOI devices. Under this circumstance, the channel region is always at full depletion (unless a very large reverse bias is applied at back gate such that strong carrier accumulation exist there). Because of this feature, thin film SOI devices are also known as Fully Depleted SOI (FDSOI) devices. In addition to the advantages mentioned in section 2.2, FDSOI devices have been reported to have many additional merits which have included reduced electric field at channel, higher transconductance, excellent resistance to short channel effect and a quasi-ideal subthreshold slope etc (Cullen and Duffy, 1990; Colinge, 1989; Vasudev, 1990). FDSOI devices have received great attention for they are the only candidate that can be employed for ULSI and low voltage applications (Auberton-Herve et. al., 1995).

2.3.3 Medium Film SOI Devices

SOI devices with $X_{dmax} \leq t_{si} \leq 2\, X_{dmax}$ are classified as Medium Film SOI devices.

Depending on the bias conditions of the front gate and back gate, the channel region of these devices may be just fully depleted or just neutral. In other words, almost all the time the channel region is partially depleted and so devices of this kind are also termed Partially Depleted SOI (PDSOI) devices.

Since the front and back gate depletion zones always modulate each other, the performance of PDSOI devices is unstable and is strongly dependent on the biasing conditions.

2.4 Drawbacks of SOI Devices

Impact ionization, i.e. the generation of electron-hole pairs under a high electric field intensity, is a well known physical phenomenon that exists whenever high electric field regions presents. The existence of floating body and parasitic bipolar transistor in SOI structure amplifies the effect of impact ionization and transforms it to undesirable effects such as kink effect, single transistor latch and early breakdown voltage.

2.4.1 Floating Body Effects

The undesirable floating body effects of conventional SOI devices are generally categorized as Kink Effect and Parasitic Bipolar Effects.

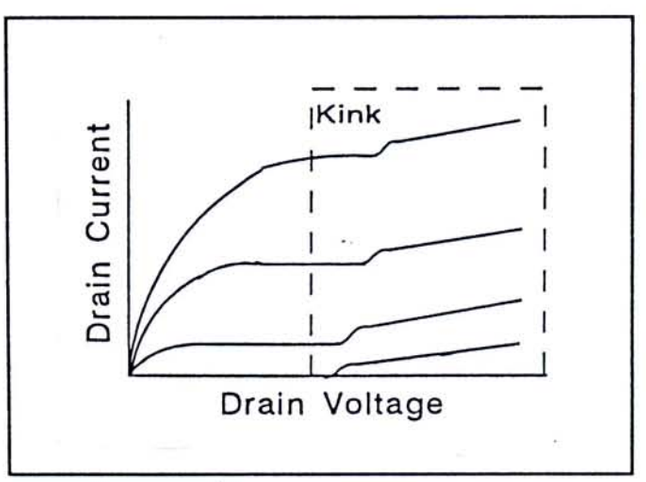


Figure 2.7 Kink effect is symbolized with the "kink" appearance in the current-voltage curve.

2.4.1.1 Kink Effect

The kink effect is symbolized

by an appearance of a "kink" in the current-voltage characteristic curve of a SOI device (Figure 2.7), particularly on thick film SOI devices. The kink may appear above a certain drain voltage and can be very severe in n-channel transistors but not on p-channel transistors.

The existence of kink effect can be explained as follows. In n-channel transistor, at high drain voltage, the electric field at the drain region is so high that impact ionization become significant. In thick film or PDSOI structures, the generated electrons will move towards V_{dd} while holes migrate and accumulate at the neutral, floating body region, which most likely exist near or under the source region of the transistor where the potential is the lowest. The accumulation of holes will raise the body potential and transforms itself as if the application of back bias. As a result, threshold voltage of the transistor will be reduced and a sudden jump in the channel current is resulted and appeared as kinks.

Kink effect is not observed in bulk silicon devices because the body of them is grounded. Generated holes can be absorbed by the substrate by means of an elevated substrate current. Kink effect is also not observed in p-channel transistors since the rate of impact ionization is much lower than in n-channel transistors (Sze, 1981).

Kink effect is also rarely observed in FDSOI devices since the depletion zone in FDSOI extends well beyond the thickness of the silicon overlayer. The overall electric field is reduced and hence reduces the rate of impact ionization. Moreover, in FDSOI devices, source-to-substrate diode is already forward biased, the generated holes can be recombined readily in the source and will not accumulate there (Colinge, 1991; Jaczynski et. al., 1992).

2.4.2 Parasitic Bipolar Effects

Within any MOS structure, such as a n-channel one, a parasitic bipolar transistor exists if we consider its n^+ source, the p^- body and n^+ drain as the emitter, base and the collector of an NPN bipolar transistor (Figure 2.8). Unlike in bulk device in which the body region is grounded by means of substrate contact, in SOI devices the body is usually left floating. The existence of such a floating body parasitic bipolar transistor give rise to undesirable effects : a) Single Transistor Latch; and b) Early Breakdown voltage.

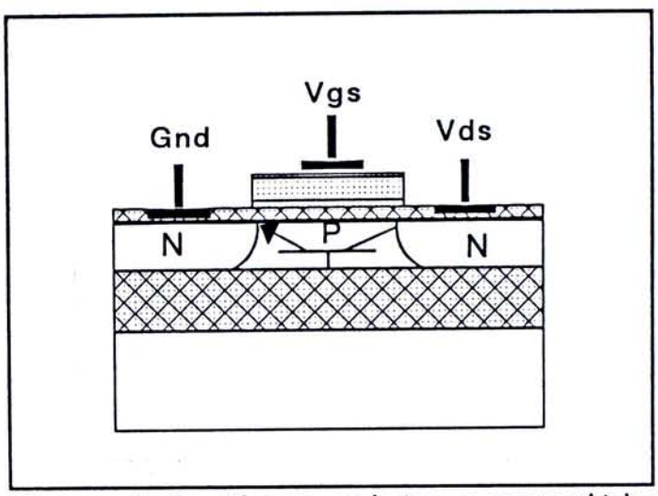


Figure 2.8 There exists a parasitic NPN bipolar transistor in a typical n-channel MOS structure.

2.4.2.1 Single Transistor Latch

For devices with floating body, the subthreshold slope can change drastically when the drain bias is increased. Figure 2.9 shows the typical I_{ds}-V_{gs} characteristics of such a kind of devices.

At low drain bias, a normal subthreshold I_{ds}-V_{gs} characteristics is exhibited no matter what sweep direction of

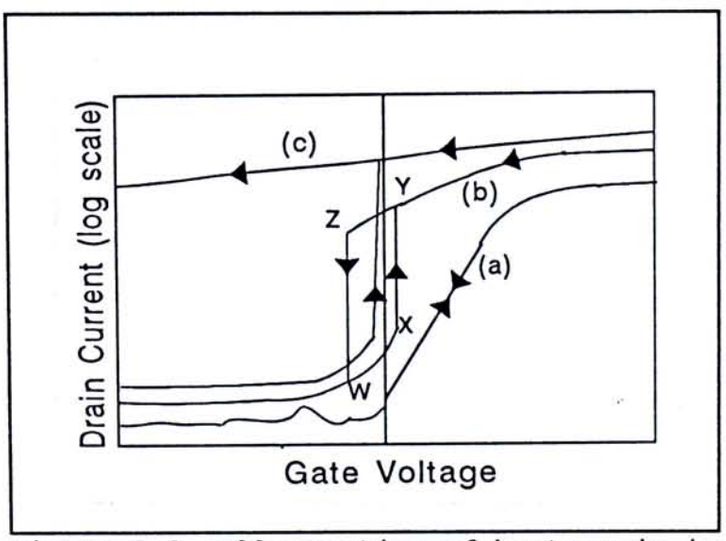


Figure 2.9 Illustration of hysteresis in I_{ds}-V_{gs} chara-cteristics of devices with floating body.

V_{gs} bias is (curve a). At intermediate drain bias, a hysteresis developed and there are break points, X, Y, W and Z, in the I_{ds} and V_{gs} curves where the drain current change abruptly and the subthreshold slope approach 0 mV/decade (curve b). At high drain bias, the hysteresis is such severe that, in the descending V_{gs} sweep, I_{ds} will remain high even the gate voltage is well below threshold voltage, and the transistor is regarded "latched" (curve c). Once the transistor is latched, it remains latched as long as the drain voltage is maintained, which indicates that the latch phenomena is not a transient effect (Colinge, 1991; Chen et. al., 1988).

The single transistor latch phenomena can be explained as follows. The application of drain bias give rise to impact ionization with proportional magnitude at the drain region, regardless of the gate voltage bias. The generated majority carriers in the base region can give rise to body potential and thereby reducing threshold voltage. At the same time, the generated minority carriers become the body current, I_{body}. Due to existence of a floating base parasitic NPN bipolar transistor, the generated body current are amplified by a factor β, i.e. the bipolar transistor gain. This forms a positive feedback loop on the current flowing through the devices.

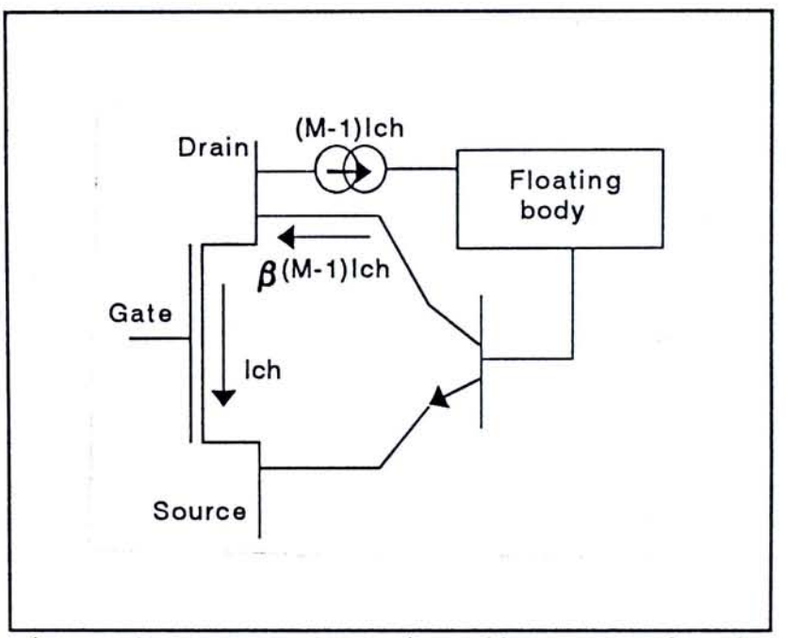


Figure 2.10 A schematic diagram of the positive feedback loop.

Mathematically, the body current may be quantified as

$$I_{body} = (M-1)(I_{ch} + \beta I_{body}) \quad \text{(Eqn. 2.1)}$$

where M is the multiplication factor due to impact ionization; and

I_{ch} is the current that flows across the channel.

Rearranging,

$$I_{body} = \frac{(M-1) I_{ch}}{1-\beta(M-1)} \quad \text{(Eqn. 2.2)}$$

Also, the drain-to-source current I_{ds} can be written as

$$I_{ds} = M(I_{ch} + \beta I_{body}) \quad \text{(Eqn. 2.3)}$$

Or,

$$I_{ds} = \frac{M I_{ch}}{1 - \beta(M-1)} \quad \text{(Eqn. 2.4)}$$

Hence, it is clear that the positive feedback behaves like this: the raised body potential due to impact ionization reduces the threshold voltage which in terms elevates I_{ds} and aggravates the body current. When the gain of the positive feedback loop, β(M-1), reaches unity, I_{ds} increases suddenly. Yet, the positive feedback is self-limiting: increasing body bias also increases the drain saturation voltage which results in lower channel electric field and smaller impact ionization.

During a descending V_{gs} sweep, the high impact ionization rate under the drain region keeps the body potential high, and therefore keeps the threshold voltage low, a high I_{ds} is observed until the feedback loop no longer be maintained. The drain current drops suddenly when β(M-1) becomes less than unity. Notice that the separation of break points of Y to Z and X to W indicates that it takes a higher gate voltage to initiate the current jump and turn on the feedback loop. However, if the drain bias is so high that, once the feedback loop is triggered, it can not be turned

off. At this stage, β(M-1) remains ≈ 1 and the transistor is at "latched" state.

Nevertheless, latch is practically eliminated if the body region is grounded.

2.4.2.2 Early Breakdown Voltage

Despite that the peak electric field at the junction of SOI device is lower than bulk, SOI devices are found to have apparently lower breakdown voltage than the bulk counterparts (Figure 2.11). From bipolar transistor theory (Sze, 1981), the collector breakdown voltage with open base, BV_{CEO}, is smaller than when the base is grounded (BV_{CBO}). The two breakdown voltages relate as

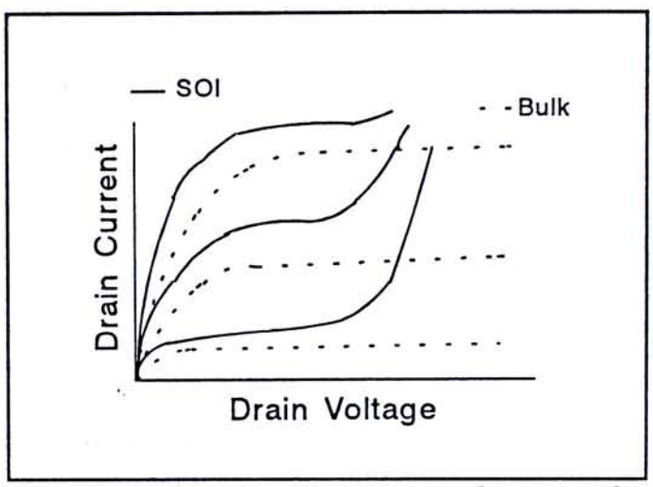


Figure 2.11 Phenomena of early breakdown in floating body SOI devices.

$$BV_{ds} = BV_{CEO} = \frac{BV_{CBO}}{\sqrt[n]{\beta}} \qquad \text{(Eqn. 2.5)}$$

where n ranges between 3 and 6. It is of course quite a simplification in accounting for the breakdown mechanism occurring in SOI devices, since both β and (M-1) depend on the drain voltage in an non-linear manner (Young and Burns, 1988; Yoshimi et. al., 1990). In fact, the degree of the breakdown voltage degradation is also affected by the carrier lifetime and channel length (Figure 2.12) (Colinge, 1989).

In essence, the drain-to-source breakdown voltage decreases with increasing carrier lifetime, τ_n, and decreasing effective channel length. It is controlled by the common-emitter bipolar breakdown voltage BV_{CEO} which occurs when β(M-1)=1.

Note that M increases strongly with V_{ds} due to the increasing drain electric field, while β decreases strongly with V_{ds} due to the high injection in the base.

Possible solution of the problem include the use of Litghtly Doped Sources and Drains (LDS and LDD) to alleviate impact ionization, lifetime killers, controlled introduction of defects in silicon film and the use of body contact (Colinge, 1989).

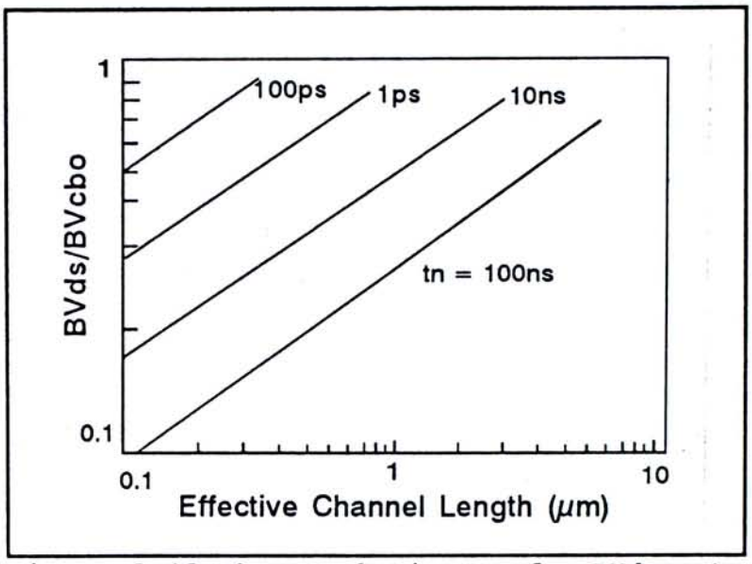


Figure 2.12 The relation of BVds to carrier lifetime and effective channel length.

Such a drawback had limited the proliferation of PDSOI and FDSOI devices in commercial market where supply voltage of 5V was prevalent. The popularity of mobile phones and portable computer arouse the concern for lower power consumption. Supply voltages of 3.3V or even 2.5V will become the mainstream, thereby making the early breakdown drawback of SOI devices not a big concern.

2.4.3 Cost

Cost has long been the decisive factor that limits the wide-spread of SOI applications. At present, a SOI wafer may be 2 to 3 times more expensive than a bulk silicon wafer. The paradox is how a more expensive substrate can be used to reduce the final cost of chips. Obviously, the merits and the reduced processing steps of SOI wafers have to offset the high substrate cost so as to complete with bulk silicon substrate. In fact, it has been envisaged that a 40 to 50% less cost will

be needed to produce 256Mbit and 1Gbit DRAM on SOI substrate than on conventional silicon substrate (Auberton-Herve et. al., 1995).

For high performance circuits, a recent study has demonstrated potential cost reduction of using SOI substrate for producing 0.25μm 64Mbit SRAM in view that SOI technology requires 20% fewer processing steps, enables 30% higher packing density, improves performance by 30% and maintains the same yield. Also, it has been claimed that SOI technology delays the need for a new wafer size and equipment capable for finer geometry for the sake of substantial development saving. All in all leading to a conclusion that, with the wide-spread in the field of SOI technology application, further lowering in SOI wafers cost is plausible and the commercial availability of SOI wafers is foreseeable.

2.5 Manufacturing Methods

Early SOI technologies such as Silicon-On-Sapphire (SOS) was developed to meet the requirement of military and space electronics for radiation hardness of MOS devices. Since then, SOI technologies have been extending to a wide variety of application fields such as bipolar devices, smart power devices, ULSI and low voltage application etc. Depending on the field of applications, different SOI substrate configuration are needed, thereby inducing the invention of many different substrate preparation methods (Ryssel et. al., 1993). Of all the available methods, five groups of preparation methods can be distinguished:

2.5.1 Epitaxy-Based Method

The most successful application of this method is the Silicon-On-Sapphire

(Al_2O_3) substrate. Apart from this, devices that are built on substrate material such as Spinel ($MgAl_2O_4$), CaF_2, SrF_2, and BaF_2 or Epitaxial Lateral Overgrowth (ELO) have also been reported. Sapphire substrate is commercially manufactured both by Edge-defined Film-fed Growth (EFG) which results in large area wafer and the conventional Czochralski (CZ) method.

Sapphire substrate are known to have a very low thermal conductivity and the interface quality between silicon and sapphire is not as good as the interface between silicon and oxide. Hence, thermal expansion and lattice mis-match between silicon and sapphire exists. Moreover, aluminum diffusion from Al_2O_3 into the silicon takes places during epitaxy will result in high p-type conductivity. Poorer carriers mobilities are usually resulted. Recently, new method, Double Solid Phase Regrowth (DSPR) were developed to improve the silicon quality.

As shown in Figure 2.13, after the implantation, an amorphous region is formed near the SOS interface. A subsequent recrystallization from the undamaged top layer leads to an almost perfect silicon layer with much fewer defects. The final overlayer thickness can be of 0.1 to 0.5μm. Despite of the

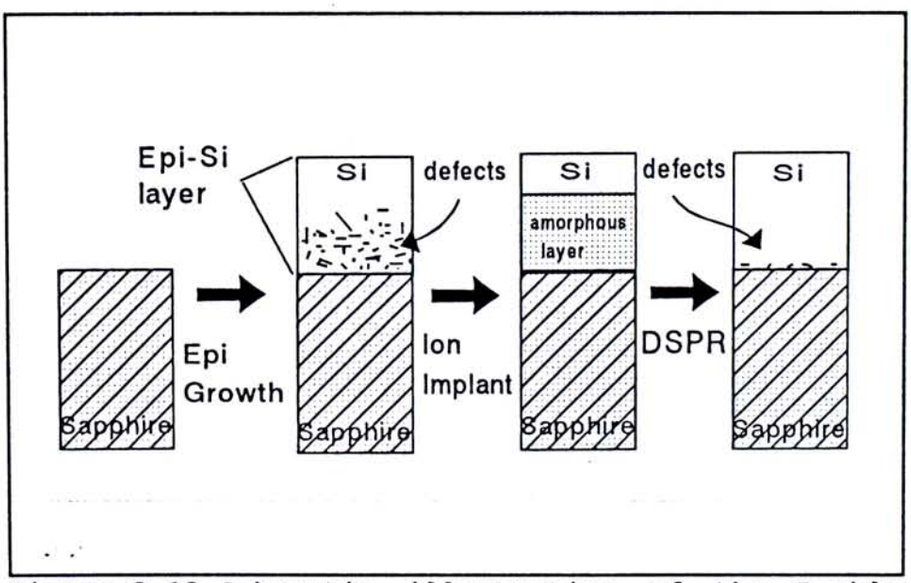


Figure 2.13 Schematic illustration of the Double Solid Phase Regrowth (DSPR) method.

improvement in film quality, the carrier mobility is constantly smaller than bulk device by 10 to 40% (Cristoloveanu and Li, 1991). The poorer carrier lifetime in SOS inhibits the realization of bipolar device on it. Nevertheless, SOS is dedicated for radiation hard market rather than competing in ultra-fast microelectronics.

2.5.2 Recrystallization-Based Method

The basic steps in this method are thermal oxidation of wafers, the deposition of polysilicon, the deposition of capping layer such as SiO_2, Si_3N_4 and the local melting and then recrystallization of polysilicon by means of lamp, laser, heated strip or e-beam. In Zone Melting Recrystallization (ZMR) method as shown in Figure 2.14, polysilicon is recrystallized by a linear heat source, either a heated graphite strip or a bank of lamps. Starting from the seeding opening, similar crystalline structure can be formed over the entire wafer with nearly no grain subboundaries in one single scan if the film is thick enough ($\geq 1\mu m$). However, threading dislocation density of 10^4 to 10^5 cm^{-2} still exists in ZMR films. Nevertheless, a wide variety of electronic devices and VLSI circuits have been fabricated on ZMR films.

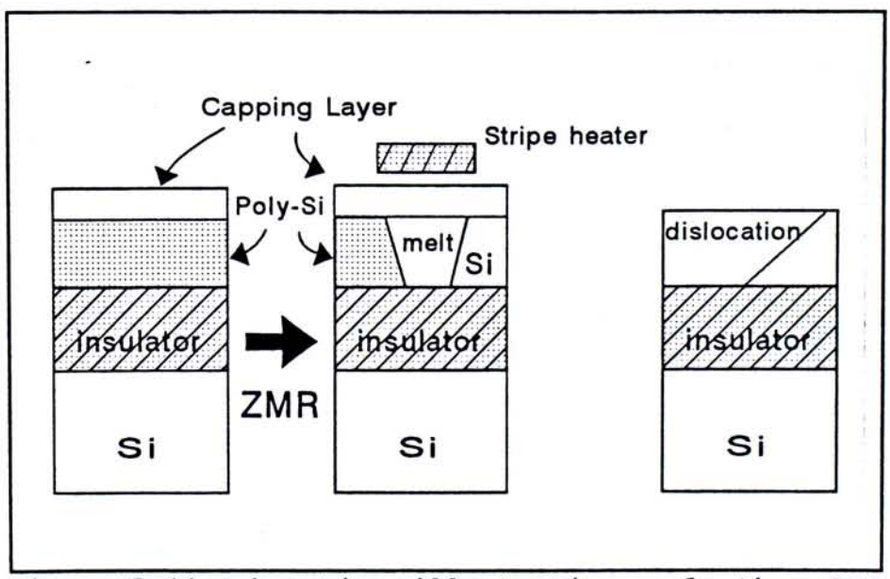


Figure 2.14 Schematic illustration of the ZMR method.

The outstanding merits

of ZMR method is that simultaneous recrystallization of several layers on top of each other for 3-dimensional device application is made possible by this method. A straightforward application is to integrate a controlling CMOS circuit on the same SOI substrate with a high voltage power device (Zavrachy et. al., 1991).

2.5.3 Wafer Bonding Based Method

This method is most easily understood conceptually (Figure 2.15). In the original process, two clean oxidized wafers are brought together. Upon annealing the wafer sandwich at an elevated temperature, even without the need of applying any external force, strong binding force between the two wafers will be established. One side of the sandwich is then lapped down to the desired layer thickness.

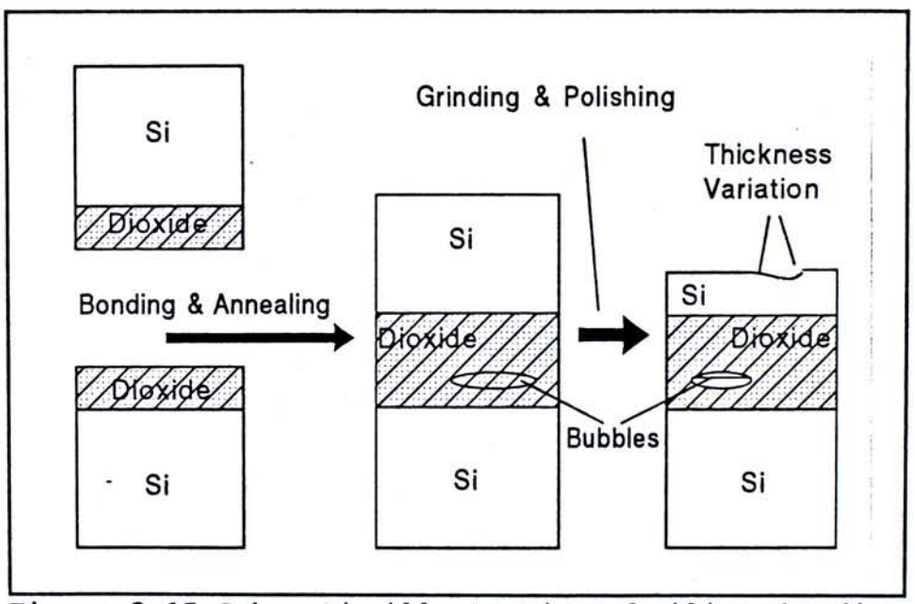


Figure 2.15 Schematic illustration of silicon bonding method.

Substrate prepared by this method offer the silicon film with high quality and enable good interface quality, thereby assuring low interface trap density and comparable carrier mobilities as in bulk devices. Yet, the lower oxide layer breakdown voltage of bonded substrate indicates a weaker interface integrity. Moreover, it is difficult to achieve thin silicon layer with good uniformity by this method. The existence of voids due to incomplete bonding at the Si-SiO_2 interface,

for example, the introduction of minute particles during bonding process, limits the usable area on a bonded wafer. Alternate to the original bonding method, a "Smart Cut Technology" was recently proposed (Auberton-Herve et. al., 1995). By making use of ion implantation method, it is reported that SOI wafers can be prepared with implantation-controllably good uniformity and comparable oxide bonding integrity and with even more competitive cost. Large volume production of this method is awaited to be seen.

2.5.4 Oxidation-Based Method

Representative methods under this category are Dielectric Isolation (DI) method and Full Isolation by Porous Oxidized Silicon (FIPOS) method.

2.5.4.1 Dielectric Isolation (DI) method

This is the first technique developed for fully isolating the collector of bipolar transistors with a layer of SiO_2 rather than p-n junctions. The fabrication of DI wafers are shown in Figure 2.16. An n-type wafer is used as the starting material. After oxidation, selected windows are opened on the oxide layer. V-grooves are then formed at the backside of wafers. Wafers are then subjected to thermal oxidation. Next to it is the deposition of thick ($\geq 200\mu m$) polysilicon layer so as to

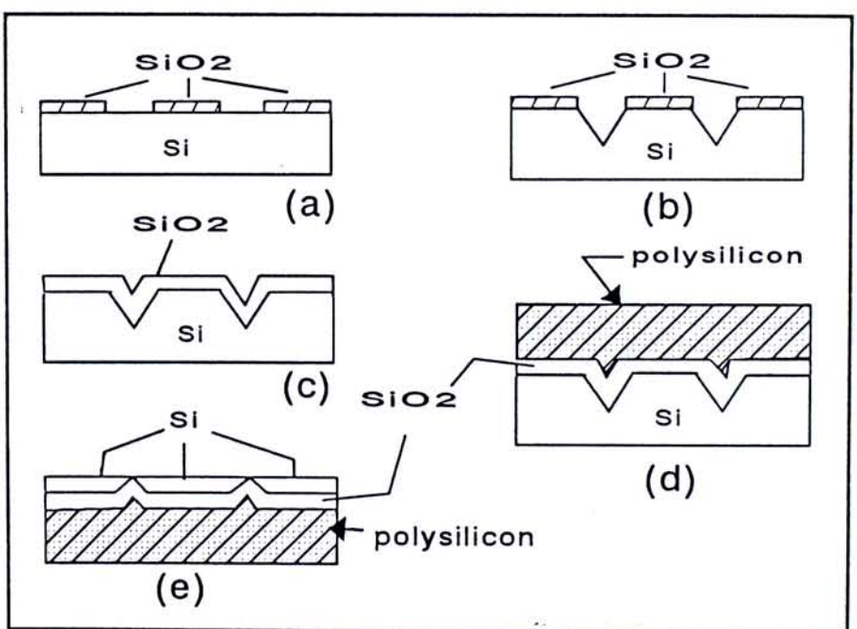


Figure 2.16 Illustration of Dielectric Isolation (DI) method.

form the mechanical support to the final wafer structure. Wafers are then flipped over. The wafer surface is then lapped until the oxide regions are exposed. Good control to ensure uniform oxide region exposure is conducive to proper device isolation.

The major limitation of this method is the incapability of shrinkage, due to the existence of V-grooves. Also, the process is not compatible to standard CMOS flow. And, above all, the preparation cost is expensive.

2.5.4.2 Full Isolation by Porous Oxidized Silicon (FIPOS) method.

This preparation method offers the potential for essentially defect-free active layer. As shown in Figure 2.17, the substrate preparation starts from an epi wafers with selec-tively etched silicon islands. Then, the heavily doped p^+ regions are converted to porous silicon under anodization process in HF solution. The thickness of the porous silicon layer can be easily and uniformly controlled. Due to the existence of large surface area, porous silicon oxidizes much faster than single-crystalline silicon. By exploiting this property, silicon islands are

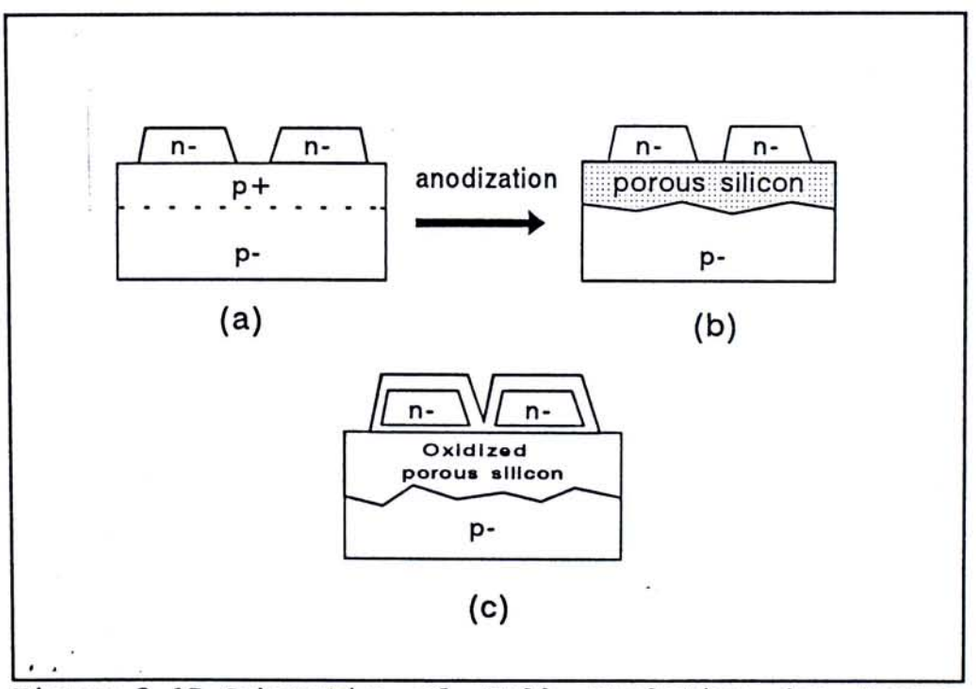


Figure 2.17 Schematic of Full Isolation by Porous Silicon (FIPOS) preparation method.

completely surrounded after oxidation. The major problem of FIPOS is that the preparation is incompatible to standard CMOS flow, thereby creating difficulty in actual implementation.

2.5.5 Implantation-Based Method

Silicon isolation by IMplantation of OXygen (SIMOX) and Silicon isolation by IMplantation of NItrogen (SIMNI) are the two most successful applications of this substrate preparation method. The synthesis of insulator layer by these methods employ the high energy (150-200keV) and high dose ($>$ 1E18/cm^2) implantation at elevated substrate temperature ($>$500°C). Next to implantation, high temperature ($\geq$1300°C) and long time (4 - 6 hours) annealing is needed to restore the damaged surface layer as well as forming the insulator layer. Because of the ability of forming ultra-thin surface layer (80nm or less), the interest on using this methods is increasing. Dislocation density and metal contamination in the top silicon overlayer formed by these two methods are typically below 10^4/cm^2 and 10^{17}/cm^3 respectively which is close to those in bulk silicon wafers. Yet, the high implantation dose, about three order of magnitude higher than conventional source and drain region implantation dose, and the long annealing time elevate the cost of substrate preparation and thereby limiting the wide-spread of the implantation based SOI wafers.

2.6 Future Trends

Each substrate preparation method produces SOI devices for their particular field of applications. Each method has its own advantages and disadvantages. Yet,

the key is to see what advantages can be obtained in switching to SOI structure over bulk structure in the respective application fields.

Apart from the advantages of SOI devices as mentioned in Chapter 2.2, ultra-thin SOI MOS transistors with fully depleted structure have been reported to have the additional advantages such as increased carriers mobilities, lower subthreshold swing, reduced short channel effect and suppressed kink effect. With regard to the shrinkage limitation and the process issues with sub-micron and low voltage applications, such a kind of SOI devices have drawn huge attention and is about to proliferate in the market.

Only implantation based methods such as SIMOX and SIMNI can be used to prepare very thin silicon overlayer. In fact, SIMOX is a rather mature process and SIMOX wafers are commercially available. Also, process is compatible to CMOS line, no addition of equipment is needed.

2.7 The Quest for Silicon-On-Nitride Structure

Despite that technology on SIMOX is rather mature, the quest for SIMNI technology is always on-going. Implantation is the only means to produce silicon on nitride structure.

The stoichiometric structure of nitride is Si_3N_4. Compared to SiO_2, it is clear that less nitrogen dose is needed. In fact, at 200keV implantation energy, the critical dose for nitride formation is 1.1E18/cm^2; whereas it is 1.4E18/cm^2 for oxide formation (Hemment, 1986). Hence, a saving of 27% implantation time is expected when switching to nitride formation. Furthermore, nitrogen ions can be set up to a higher beam current. Also, unlike oxygen ions, nitrogen ions are not corrosive.

Thus, nitrogen implantation does not require specially designed anti-corrosion implanter. The apparent savings of implantation cost thereby contributes to significant lowering of the overall substrate preparation cost.

On the other hand, nitrogen is of smaller size than oxygen. Less implantation damage will be introduced to substrate. Hence, shorter annealing time can be used - a saving of cost as well.

Nevertheless, nitrogen is an n-type dopant and it retards oxidation. Although devices have been successfully built from SIMNI substrate (Zimmer et. al., 1982; Zimmer and Vogt, 1983), none of them was able to built up FDSOI structure. In FDSOI structure, the surface is easily converted to n-type after implantation (Poon, 1988) and thereby making subsequent oxidation difficult. New structure is needed to be proposed to make this technology to be realized easier.

Chapter 3 Descriptions of Body-Contact SOI Structure

3.1 Introduction

To harness the full potential of SOI devices, the floating body effects must be suppressed. The use of thin film SOI structure already effectively eliminates the kink effect. However, the susceptibility of single transistor latch and early breakdown still exist. Regarding the implantation based substrate preparation methods, although the dislocation density on the top silicon overlayer is acceptably low, it is still of one to two orders of magnitude higher than those in bulk silicon substrate. A Body-Contact SOI (BCSOI) substrate configuration capable of maintaining the top silicon overlayer quality to be as good as in bulk silicon substrate shall be suggested. The BCSOI structure is estimated to be prepared with lower cost than conventional SOI structure and will make the fabrication of devices on silicon-on-nitride structure formed by SIMNI method easier.

3.2 Current Status of Body-Contact SOI Substrate

Many efforts have been devoted for creating SOI structures that can free SOI MOSFETs from floating body effects.

Floating body effects can indeed be effectively suppressed if contacts are made to the body region (such a kind of contact is called body contact). However, where and how to place the contact require profound and careful considerations.

Previously proposed structures such as the "smart" body contact substrate (Matloubian, 1989) and the Omura-Izumi structure (Omura and Izmui, 1988) are

mainly structures with body-contact made from the top. The packing density advantages of SOI circuits is therefore offsetted.

To maintain the packing density advantage while finding means to connect the body region from the top, a Dual Source SOI (DSSOI) MOSFET structure was proposed (Ploeg et. al., 1992). As referred to Figure 3.1, the resulted device is asymmetric, however. Due to the addition of a p^+ region underneath the n^+ region in the single source region, thermal budget is tight and the source resistance is elevated, thereby limiting the maximum operating current. Also, the use of aluminum spike to connect the p^+ region underneath the n^+ region is not reliable and prone to have problems in view of process repeatability.

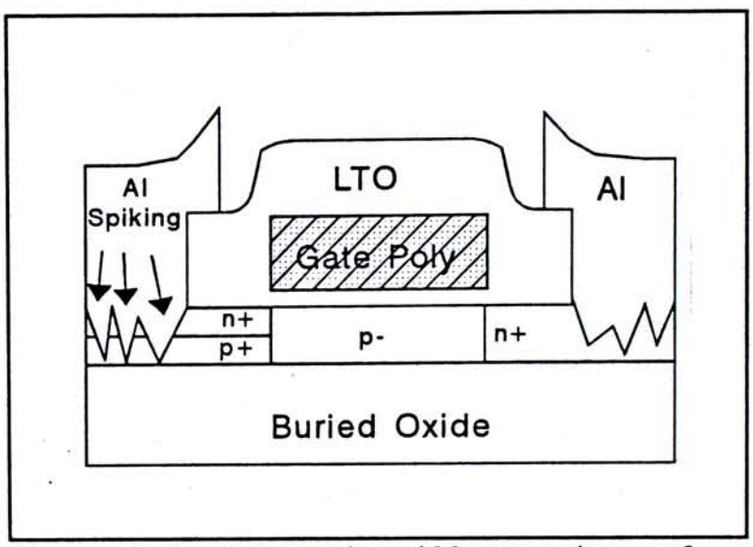


Figure 3.1 Schematic illustration of a Dual Source SOI(DSSOI) MOSFET.

For those proposed to have body contact on the buried insulator, a seeded channel approach (Ting et. al., 1986), a Quasi-SOI MOSFET structure (Nguyen et. al., 1992), a Patel structure (Patel et. al., 1990, 1991) and a Kamins structure (Kamins et. al., 1986) were reported. The first two approaches employed lamp recrystallization Selective Epitaxy Growth (SEG) process to form the silicon overlayer. The seeded window is designed to be directly under the gate channel region to realize good after-growth silicon quality (Figure 3.2). The process is,

however, inconvenient and is not compatible to standard CMOS processing sequence. Also, it is difficult to form thin silicon overlayer for enhanced transistor performance.

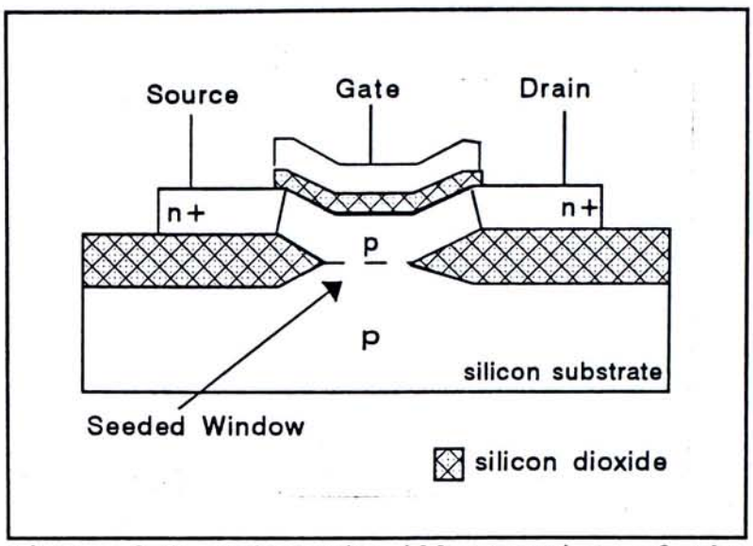


Figure 3.2 Schematic illustration of the seeded channel approach and Quasi-SOI MOSFET structure (see text).

For the Patel structure, the body contact is made from the bottom and is located beside the gate region (Figure 3.3). Masked ion implantation approach is used for substrate preparation. However, since the channel region is also implanted, the silicon quality there is poorer than those in bulk silicon device. The long time and high temperature post-implant anneal not only cannot fully reduce the damage, but just add cost on to substrate preparation. Moreover, since nitride retards oxidation, building devices on buried nitride layer with thin top silicon overlayer via this method is quite difficult.

On the other hand, the advantage of the Kamins structure (Figure 3.4) is that it allows the body-contact "self-align" to the gate region. Both oxide or nitride buried layer can be formed

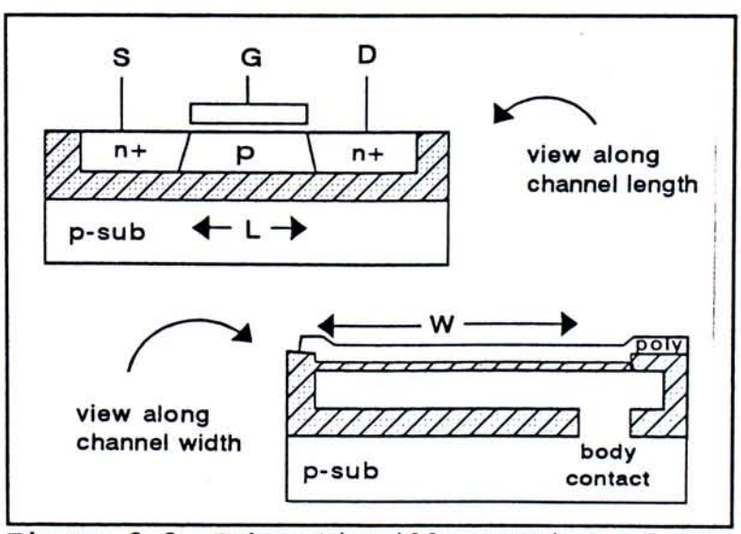


Figure 3.3 Schematic illustration of the Patel structure (see text).

with no additional mask. However, the choice of tungsten for masking buried insulator implantation elevates the metal contamination level on the substrate, because of the sputtering nature associated with implantation, and limits the post-implant annealing temperature to about 1125°C. The resulting transistor performance showed apparent leakage at junctions and a four-fifth reduction in device transconductance. These indicate that the implantation damage was unable to be removed at the limited anneal temperature. Moreover, having the insulator formed after gate electrode definition imposes severe penalty on packing density, thereby limiting its application in small geometry CMOS regime.

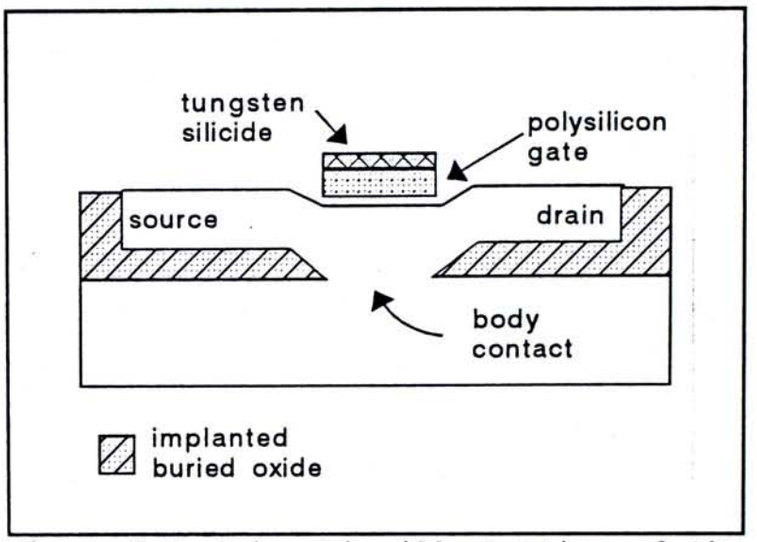


Figure 3.4 Schematic illustration of the Kamins structure (see text).

3.3 The Body-Contact SOI Structure to be Studied

More and more researchers have envisaged that SOI technology is emerging as a workable alternative to bulk silicon technology especially in the low voltage and ULSI applications. By far, FDSOI structure is the only competent candidate for such an application. As discussed in Chapter 2.3, FDSOI substrate can be readily prepared by implantation method among which SIMOX method is already a rather mature method.

By employing the SIMOX method, BCSOI structures can be built easily. As

shown in Figure 3.5(a), the body contact is provided from the bottom, i.e., an opening is made in the buried insulator layer. The entire region under the gate is made as the body contact (Figure 3.5(b) and (c)).

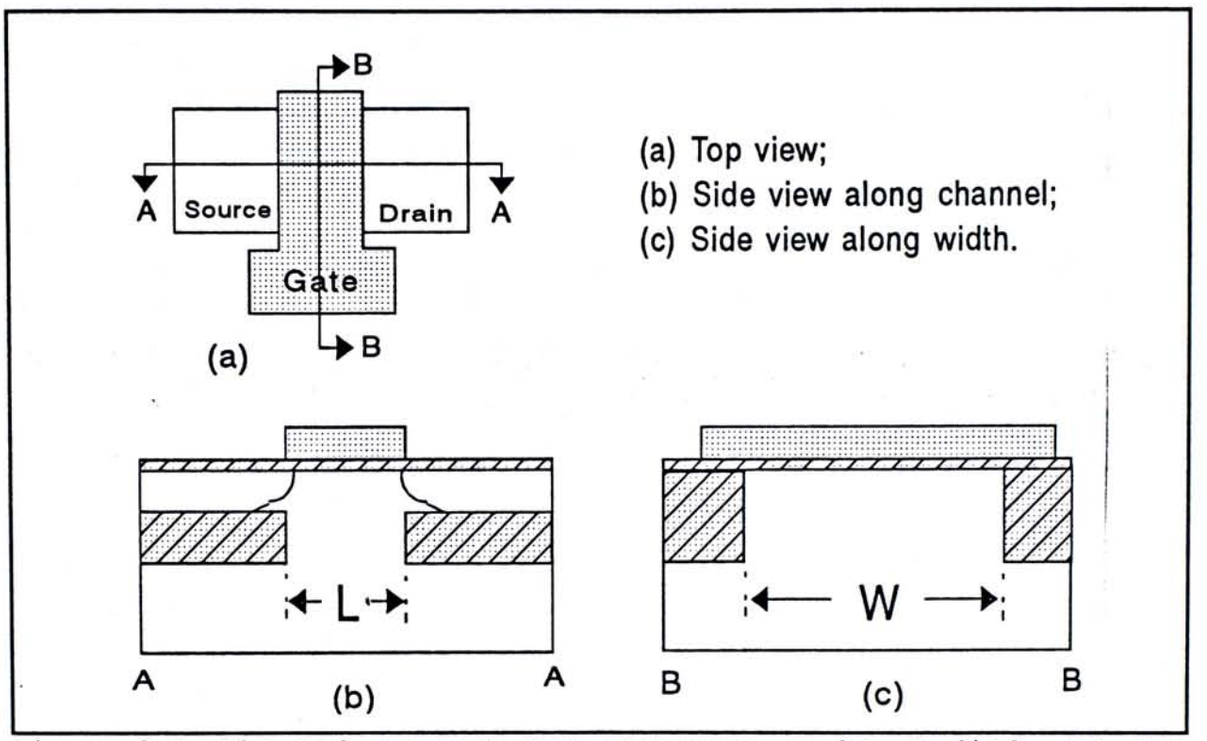


Figure 3.5 The Body-Contact SOI structure to be studied: (a) Top view; (b) cross-sectional view along channel length (L); and (c) cross-sectional view along channel width (W).

Masked implantation method is used to form the body contact. Instead of using tungsten as the masking material as in the Kamins structure, dielectric materials such as SiO_2 or Si_3N_4 are employed. A very low metallic contamination level in the channel region is therefore ensured. For such a BCSOI structure, provided it is proved to be workable later on in this thesis, devices built on it shall have the following advantages:

(a) Elimination of Floating Body Effects

The physical existence of a body contact frees a SOI device from potential build-up in the body region, thereby eliminating all floating body effects. SOI devices built on the novel structure can have comparable

breakdown voltage as bulk devices, extending their possible use in the wide supply voltage range.

(b) Preservation of Good Quality Silicon Overlayer

The novel structure is designed in such a way that during insulator ions implantation, the entire channel region is masked out. Implantation damages such as dislocation, metallic contamination etc. will not be introduced into the channel region. As a result, the quality of the silicon overlayer can be made to be identical to those in bulk silicon structure. In other words, improved channel silicon quality are ensured using the BCSOI structure compared to conventional SOI structure.

(c) Reduced Junction Capacitance Advantage Maintained

As shown in Figure 3.5(a), similar to conventional SOI structures, the source and drain junctions reach to the insulator layer that is formed underneath. Hence, the reduced junction capacitance advantage over bulk silicon structure is maintained. Higher switching frequency and shorter commutation delay merits that have been realized in conventional SOI structure can also be realized in the BCSOI structure.

(d) ULSI application possible:

Since body-contact is made form bottom, the packing density advantage as if those of conventional SOI devices over bulk devices is preserved in BCSOI structure. This is particularly attractive for ULSI applications.

(e) Lower Substrate Cost

In conventional implantation-based SOI substrate preparation, since

the channel region is also implanted with heavy dose, substantial damage is made there. High temperature (>1350°C) and long (4 to 6 hours) post-implant anneal cycle is carried out to reduce the damage or re-store the silicon quality. With the new structure, since the channel region is of excellent quality, it is expected the annealing time can be reduced. A shorter cycle time means substrate can be prepared at lower cost.

(f) SIMNI applications possible:

Nitrogen is known to be an n-type dopant. Implantation of nitrogen into bulk devices have been manipulated to be used as a means to retard oxidation. Although devices have been successfully built on silicon-on-nitride substrate (Munzel et. al., 1984; Zimmer et. al., 1982; Zimmer and Vogt, 1983), none of them was built on silicon overlayer with thickness $t_{si} \leq$ 150nm, thereby limiting their applications in FDSOI devices regime. With the BCSOI structure, the channel region will not be doped n-type and gate oxidation with good gate oxide integrity is also made easier.

3.4 Impact on Device Fabrication

A breakdown of the device fabrication of bulk CMOS, conventional SOI CMOS and BCSOI CMOS is shown in Table 3.1.

3.4.1 Fabrication of Conventional Bulk CMOS

As referred to Table 3.1, the fabrication of bulk CMOS structure is a standard process flow. Steps marked with "x" mean that those steps are required in the CMOS device processing. Such a bulk CMOS process flow is put here as the

basis of comparison when discussions on the processing of SOI CMOS are presented. Detailed processing descriptions can be referred elsewhere (Ruska, W. S., 1988; Yang, E. S., 1988; Chen, J. Y., 1990) and is therefore not to be discussed here.

3.4.2 Fabrication of Conventional SOI CMOS

Referring to Table 3.1, extra steps are required, as compared to bulk CMOS processing, for the formation of insulator layer in conventional SOI CMOS structure. Nevertheless, those steps are only dielectric, such as silicon dioxide (SiO_2) or silicon nitride (Si_3N_4), deposition, implantation and annealing. They can all be done in the same fabrication line without the need of extra equipment. This affirms that implantation SIMOX process is compatible to standard CMOS line. In fact, SIMOX wafers are also commercially available.

The gains in the processing of SOI substrate are from the omission of well formation, the skip of steps that are optional (steps that are marked "#" in the Table) and the reduced time for field oxidation (steps that are marked "+" in the Table means steps with advantage over bulk CMOS processing).

Without the need for forming well, the long well drive-in time can be waived. Depending on the circuit design, inter-device isolation formed by LOCOS process can be extended and merged with the buried insulator layer, thereby putting the field implant lithography and field implantation steps become optional. Lightly Doped Drain (LDD) structures may not be needed in genuine FDSOI structure since they only add up as series resistance and suppress carrier recombination in source and drain regions. For a fair comparison with bulk devices, they are kept

Table 3.1: A Breakdown of Process Steps for Bulk CMOS, Conventional SOI CMOS and BCSOI CMOS

Process Steps	Bulk CMOS	Conventional SOI CMOS	BCSOI CMOS
Starting Material	x	x	x
Masking Dielectric Deposition			x
Body Contact Definition			x
Oxygen / Nitrogen Implantation		x	x
Capping Dielectric Deposition		x	x
Annealing		x	x+
Capping Dielectric Removal		x	x
Well Definition	x		
Well Doping and Drive-in	x		x
Nitride Deposition	x	x	x
Active Definition	x	x	x
Field Implant Lithography	x	x #	x #
Field Implantation	x	x+	x+
Field Oxidation	x	x	x
Nitride Removal	x	x	x
Vt Implant Lithography	x	x	x
Vt Implant	x	x	x
Gate Oxidation	x	x	x
Poly Deposition and Doping	x	x	x
Poly Definition	x	x	x
N LDD Lithography	x	x#	x#
N LDD Implantation	x	x#	x#
Spacer Formation	x	x	x
N^+ S & D Lithography	x	x	x
N^+ S & D Implantation	x	x	x
N^+ Re-oxidation	x	x	x
P^+ S & D Lithography	x	x	x
P^+ S & D Implantation	x	x	x
Dielectric Deposition	x	x	x
Contact Definition	x	x	x
Metallization	x	x	x
Metal Definition	x	x	x
Sintering	x	x	x

Remarks: x process steps that are required.
process steps that are optional.
+ process steps that are with advantages.

unchanged there. Also, since the top silicon layer is very thin, in most cases

$\leq$100nm for FDSOI devices, the field oxidation time is about 50% shorter than in bulk silicon case. In essence, the processing of conventional SOI CMOS is less complicated than bulk CMOS processing.

3.4.3 Fabrication of BCSOI CMOS

The fabrication of BCSOI CMOS is very similar to the fabrication of conventional SOI CMOS. On comparison, extra steps for masking dielectric deposition and body contact definition are needed for BCSOI CMOS processing (Table 3.1). The processes involved in the body contact definition step are only lithography and etching. Those processes, once again are fully compatible to CMOS line. The advantage of BCSOI structure over conventional SOI structure is the freedom of choice between oxygen or nitrogen for implantation. Also, as stated previously, due to the non-damaging feature in the channel region, shorter post-implant anneal time can be used, thereby keeping the overall process cycle time of the BCSOI structure to be more or less the same as conventional CMOS SOI structure.

Chapter 4 Device Simulations

4.1 Introduction

The collaborative efforts that researchers over the world contributed have made models that govern device physics and mechanisms become more and more accurate. Given the great improvement in computation speed and compared to the high cost and long time for actual device fabrication, detailed computer simulation of processes have become a cost-effective and indispensable mean on process or structure development.

It is rare nowadays that new circuit design are not simulated in computer prior to actual device fabrication. There are many kind of simulation software which can be used for a vast variety of applications. Down to device structure studying, MEDICI, a more self-sufficient software upgraded from formerly known PISCES-2B, is undoubtedly a popular device simulation tool. This chapter provides a description of the MEDICI program for the analysis of electrical behaviour of different devices. Then, description of grid allocation, initial solution and content of source file are highlighted. Structures to be simulated are also discussed in details, finally.

4.2 MEDICI

MEDICI, in essence, is a simulation software that can model the two-dimensional distributions of potential and carriers concentrations in both MOS and bipolar devices so as to predict their electrical characteristics for any bias

conditions. It solves Poisson's equation and both the electron and hole current continuity equations for analysing devices in which current flow is dominated by either single carrier, such as MOSFETs and JEFTs etc, or both carriers, such as bipolar, diodes and CMOS latch-up etc. Both steady-state and transient state operation conditions can also be predicted.

To enable for more accurate results, a number of well-acclaimed physical models for carrier mobility, recombination rate and lifetime etc have been incorporated in MEDICI. Since detailed discussions on the models can be referred elsewhere, only how a solution is derived will be briefly presented here.

4.2.1 Basic Equations

The electrical behaviour of semiconductor devices is governed by Poisson's equation,

$$\nabla\cdot(\nabla\psi) = -\frac{q}{\epsilon}(p - n + N_D^+ - N_A^-) \qquad \text{(Eqn. 4.1)}$$

and the continuity equations for electrons

$$\frac{\partial n}{\partial t} = \frac{1}{q}\nabla\cdot\vec{J}_n - (R - G) \qquad \text{(Eqn. 4.2)}$$

and holes

$$\frac{\partial p}{\partial t} = -\frac{1}{q}\nabla\cdot\vec{J}_p - (R - G) \qquad \text{(Eqn. 4.3)}$$

The mission of MEDICI is to solve the above partial differential equations for the electrostatic potential ψ, and the electron and hole concentration, n and p respectively. Note that ψ is always defined as the intrinsic Fermi potential, i.e. $\psi_{intrinsic}$; R is the rate of recombination and G is the rate of generation; N_D^+ and N_A^-

are the ionized impurity concentrations. Of course, both R and G are functions of ψ, n and p!

From the concept of drift and diffusion components, $\vec{J}_n$ and $\vec{J}_p$ can be written as functions of E, n and p, i.e.

$$\vec{J}_n = q n \mu_n \vec{E}_n + q D_n \nabla n \qquad \text{(Eqn. 4.4)}$$

$$\vec{J}_p = q p \mu_p \vec{E}_p - q D_p \nabla p \qquad \text{(Eqn. 4.5)}$$

where μ_n and μ_p are the electron and hole mobilities; D_n and D_p are the diffusivities of electron and hole and is related by Einstein relations as

$$\frac{D_n}{\mu_n} = \frac{D_p}{\mu_p} = \frac{kT}{q} = \phi_T \qquad \text{(Eqn. 4.6)}$$

Obviously, $\vec{E}_n$ and $\vec{E}_p$ are related as $\vec{E}_n = \vec{E}_p = -\nabla\psi$ provided that the effects of band-gap narrowing is neglected and Boltzman carrier statistics is assumed.

It is hence apparent that the Poisson's equation, which governs the electrostatic potential, and the two continuity equations, which govern the carriers concentration, are coupled and non-linear. Consequently, there is no method to solve the equations in one direct step. Instead, solution must be obtained by a non-linear iteration method, starting from some initial guess.

4.2.2 Solution Methods

To solve the partial differential equations of a device structure on computer, it must be discretized on a simulation grid. This is to say, the continuous functions of the three partial differential equations are represented by vectors of function values at the nodes, and the differential operators are then replaced by suitable

difference operators.

Suppose there are N nodes in a simulation grid, then approximate values of electrostatic potential and carrier concentration to certain pre-defined confidence level is to be made based on the partial differential equations at each node. As a consequence, total 3N nonlinear algebraic equations for the unknown potential and concentration are resulted.

In principle, 3N algebraic equations can be solved to obtain the solution by using various numerical methods such as Boundary Element Method, Finite Difference Method and/or Finite Element Method. However, in practice, this is virtually impossible since the equations involve divergence term and product with dependent variable n, p and ψ.

Nonlinear iteration methods such as Gummel's method and Newton's method must be employed. Either approach involves solving several large linear system of equation. The number of equations in each method is on the order of 1 to 3 times the number of grid points, depending on the number of carrier being solved for.

4.2.2.1 Gummel's Method

In this method, the partial differential equations are solved sequentially. The Poisson equation is solved by assuming fixed quasi-Fermi potential. The new potential is substituted into the continuity equations, which are linear and can be solved directly. The new carrier concentration are substituted back into the charge term of Poisson's equation and another cycle begins. Solution is achieved in a linear rate.

Mathematically, the iteration sequence can be represented as

$$\nabla\cdot(\mu_n^{(i)} n^{(i)} \nabla\psi^{(i)} + D_n^{(i)} \nabla n^{(i)}) = G(n^{(i)}, p^{(i)}) - R(n^{(i)}, p^{(i)}) \quad \text{(Eqn.4.7)}$$

$$\nabla\cdot(\mu_p^{(i)} p^{(i)} \nabla\psi^{(i)} + D_p^{(i)} \nabla p^{(i)}) = G(n^{(i)}, p^{(i)}) - R(n^{(i)}, p^{(i)}) \quad \text{(Eqn 4.8)}$$

$$\nabla\cdot(\epsilon \nabla\psi^{(i+1)}) = q(n^{(i)} - p^{(i)} - N_D + N_A) \quad \text{(Eqn 4.9)}$$

The iteration process repeats until an insignificant difference between the (i+1)-th and (i)-th solution is accomplished. The solution is then said to be converged to a pre-defined tolerance.

The success of this method depends therefore on the degree of coupling between the equations. The most important coupling is the drift term of carrier current, which is directly related to the Poisson solution. Whenever drift terms are unimportant, such as in isolated structure, Gummel's method is suitable. When the current is drift-dominated, for instance, in a pure resistance structure, convergence is slow.

4.2.2.2 Newton's Method

In this method, all of the variables in the problem are allowed to change during each iteration, and all of the coupling between variables is taken into account. As a result, the Newton algorithm is very stable and the solution time is nearly independent of bias conditions, even into high-level injection. Solution is achieved in a quadratic rate leading to rapid convergence.

Rewriting the governing equations (Eqn. 4.1), (Eqn. 4.2) and (Eqn. 4.3) into the form

$$\begin{aligned} F_\psi(\psi, n, p) &= 0 \\ F_n(\psi, n, p) &= 0 \\ F_p(\psi, n, p) &= 0 \end{aligned} \quad \text{(Eqn.4.10)}$$

Given an initial guess for the unknowns at each node (ψ_o,n_o,p_o), a new update ($\Delta\psi$,Δn,Δp) can be derived by solving he linear system

$$\begin{bmatrix} \frac{\partial F_\psi}{\partial \psi} & \frac{\partial F_\psi}{\partial n} & \frac{\partial F_\psi}{\partial p} \\ \frac{\partial F_n}{\partial \psi} & \frac{\partial F_n}{\partial n} & \frac{\partial F_n}{\partial p} \\ \frac{\partial F_p}{\partial \psi} & \frac{\partial F_p}{\partial n} & \frac{\partial F_p}{\partial p} \end{bmatrix} \begin{bmatrix} \Delta\psi \\ \Delta n \\ \Delta p \end{bmatrix} = - \begin{bmatrix} F_\psi \\ F_n \\ F_p \end{bmatrix} \qquad \text{(Eqn. 4.11)}$$

Again, by successive iteration of the matrix system, the solution of nodal variables are to be solved to a pre-defined confidence level.

The disadvantage of Newton's method is that, for large grids, the memory and time necessary to invert the matrix may be excessive. The memory space is three time larger than Gummel's method and the computational effort spent in inversion may become intolerable.

The single biggest acceleration of a Newton iteration is the Newton-Richardson method, which only re-factors the matrix when necessary. The decision to re-factor is made on the basis of the decrease per step of the error norm. Frequently, the matrix only need be factorized twice per basis point under the method, as opposed to 40 or 50 factorization in a decoupled method.

With such a refinement, full Newton is the method for solving one-carrier problems and even two-carrier simulations for device structures of moderate complexity.

4.2.3 Initial Guess

The onset of any iteration required the availability of an initial guess. Five types of initial guesses are used in MEDICI.

The first one is simply assuming charge neutrality so as to obtain the first equilibrium bias point. This is the starting point of any device simulation.

By modifying one or two previous solution, a second initial solution with applied bias can be obtained by setting the applied bias at contacts.

In some cases, a better guess can be obtained with a local guess. This takes the solution memory, sets the applied bias, and changes the majority carrier Fermi potentials throughout heavily doped regions to be equal to the bias applied to that region.

Projection is another type of initial guess. It uses an extrapolation of two previous solution to the new bias assuming that equivalent bias steps are taken. This is particularly economical in generating I-V data.

Finally, a special initial guess is presented immediately after performing a re-grid. This guess is an interpolation of the solution on a coarse grid to the new grid.

Based on the initial guess by any of the initial guess methods, solution are then solved accordingly.

4.2.4 Grid Allocations

In device simulation, simulated results may change along with any change in grid allocations. A finer grid density, in general, gives out more accurate simulation results. However, it imposes heavy burden in terms of execution time and memory storage. The number of equations to be solved is generally linearly related to the number of nodes, N, while the number of arithmetic equations required for the solution is proportional to N^{α} where α is in between 1.5 and 2. The goal is to get a trade-off so that minimum node points is used for simulation without sacrificing accuracy.

Flexibility in grid allocation is required. MEDICI supports a general irregularly shaped triangular grid allocation that is able to match arbitrarily shaped device structure and allows refinement of particular regions with minimum impact on others. The capability of re-allocating grid according to dopant concentration or potential as desired via "REGRID" command ensure higher accuracy. Examples of the regrid can be seen in Appendix A.

For performance comparison, consistency in grid allocation is important. The key is to maintain the same initial grid allocation in different structures. Then use regrid to fit the minute change in the configuration. In such a way, errors due to different grid allocation are minimized.

4.2.5 Source File

MEDICI simulates the electrical behaviours of devices according to the source file that commands.

Users of MEDICI may direct the program through source file that consists of the input statements for structure configuration, solution method specification and display favourite.

The basic source file that is used for performance comparison simulation of different structures in this thesis is shown in Appendix A for reference. More detailed description of the source file statement are also available there.

To maintain consistency in simulations, for all the different device structures, similar source files are used. The only minor change is in the "REGION" statement which is inevitable to account for different physical configuration change.

4.3 Structures for Simulations

It is known that, compared to p-channel MOSFET, n-channel MOSFET are more susceptible to impact ionization. In fact, impact ionization originates several undesirable effects such as hot electrons effect and latch-up etc in bulk silicon devices. As a result, examination on n-channel MOSFET structure is inevitable and, as a matter of fact, the primarily focus of the present study. Five basic structures are considered and studied in details by simulation in this thesis to compare the device performance on these different structures. Further simulations with variations on the geometrical parameters of these basic structures will also be performed to study the dependence of the performance on these device parameters. A brief description on the five basic structures is as follows:

4.3.1 1.2μm NMOS Bulk (LDD)

An n-channel MOS transistor of 1.2μm channel length with Lightly Doped Drain (LDD) configuration built on bulk silicon structure is chosen as the basis of simulation. For simplicity, such a structure is called Structure A in the rest of this thesis.

As shown in Figure 4.1, the structure is a conventional four-terminal n-channel MOS transistor. The selection of transistor

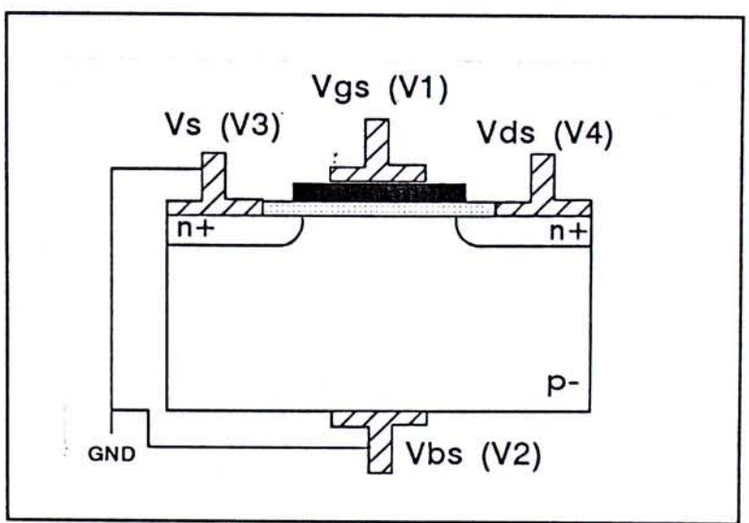


Figure 4.1 Schematic of an n-channel MOS transistor built on bulk silicon (Structure A).

parameters not only need to take care of proper transistor properties, but also take other structures performance into consideration so that a fair comparison can be assured. Hence, slight modification to key structure parameters from the basic 1.2μm process flow is needed.

Substrate concentration (N_a) -- In bulk silicon device technology, it is well known that the choice of N_a affects a series of device performance such as back body effect, short channel effect, carriers mobilities, latch-up susceptibility, threshold voltage etc. Note that N_a also affects the depth of channel depletion layer, thereby determining the type of SOI device. In the original process flow, N_a is specified as 2E16/cm^3. Yet, to adjust the threshold voltage to the usable range, channel implantation is needed to elevate the channel surface concentration to about 5.5E16/cm^3. To skip the implantation step during processing, N_a is chosen to be 5.5E16/cm^3 without affecting overall device performance.

Gate oxide thickness (t_{ox}) -- The selection of t_{ox} has ample effect on device performance. However, t_{ox} is rather invariant to whatever the substrate configuration is built on. Hence, t_{ox} is kept as 250Å as if in the original process specification.

Junction Depth (X_j) and Source/Drain concentration ($N_{s/d}$) -- The combinations of these two factors changes the series resistance of the source and drain regions, thereby modulating overall transistor current output level. Since thin film SOI device structure is to be simulated later on, the X_j can only be as deep as the silicon overlayer. Hence, X_j is chosen to be 0.1μm instead of 0.4μm in the original process flow but $N_{s/d}$ = 9E20/cm^3 is remained intact.

Given the parameters, substitute them into the empirical formula (Sze, 1981)

$$L_{\min} = 0.4 \sqrt[3]{X_j t_{ox} (W_S + W_D)^2}$$

where $$W_S = \sqrt{\frac{2\epsilon_{si}\ \psi_{bi}}{q\ N_a}}$$

$$W_D = \sqrt{\frac{2\epsilon_{si}\ (\psi_{bi} + V_{dd})}{q\ N_a}}$$

and $$\psi_{bi} = \frac{kT}{q} \ln\left(\frac{N_{S/D}\ N_a}{n_i^2}\right)$$

Upon calculation, a L_{min} of 0.77μm is resulted, indicating that the n-channel MOS transistor of Structure A is expected to exhibit long channel behaviour.

4.3.2 1.2μm SOI(O) NMOS 1000/3500 NBC

This is a conventional Silicon-On-Insulator n-channel MOS transistor structure using oxide as the insulator layer; the top silicon overlayer is chosen as 1000Å thick whereas those of the insulator layer is 3500Å; No Body-Contact (NBC) is used in this structure. For simplicity, this structure is called Structure B in the rest of this thesis.

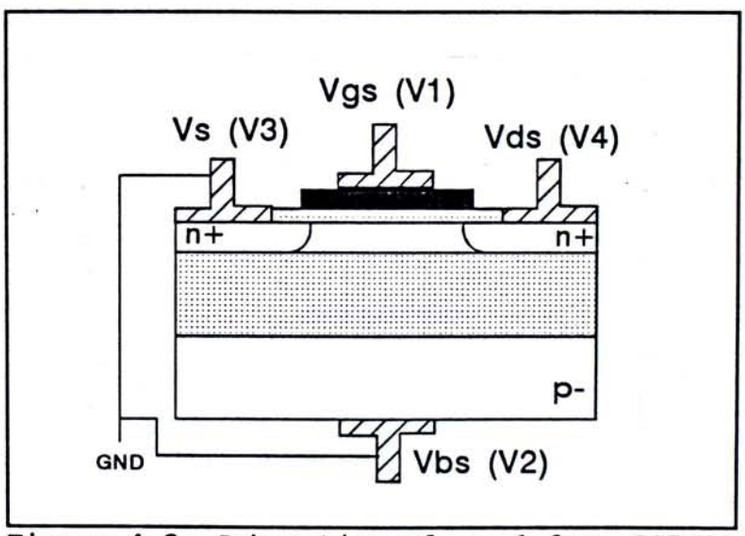


Figure 4.2 Schematic of a 1.2μm SOI(O) NMOS 1000/3500 NBC structure (Structure B).

As shown in Figure 4.2, an oxide insulator layer is added into the basic Structure A. Recalling from chapter 2.3, both t_{si} and t_{in} are important. In Structure B, t_{si} is chosen to be 0.1μm. A calculation from Eqn. 2.1 result in a value of X_{dmax} = 0.152μm. Since $t_{si} < X_{dmax}$, performance of a

FDSOI device is ensured. On the other hand, t_{in} is chosen to be 0.35μm. Too thick the t_{in} means longer substrate implantation and anneal time which adds cost to it; whereas too thin of it will degrade the superiority of SOI devices over bulk devices. In view that SOI substrate with 350nm thick insulator layer is frequently reported and also commercially available, it is adopted as the thickness for Structure B. An additional statement "REGION NUM=2 OXIDE Y.MIN=0.1 Y.MAX=0.45" is needed to be added into the basic source file to account for the configuration change.

4.3.3 1.2μm SOI(N) NMOS 1000/3500 NBC

This is a conventional Silicon-On-Insulator n-channel MOS transistor structure using nitride as the insulator layer; the top silicon overlayer is chosen as 1000Å thick whereas those of the insulator layer is 3500Å; No Body-Contact (NBC) is used in this structure. For simplicity, this structure is called Structure C in the rest of this thesis.

As shown in Figure 4.3, Structure C is basically identical to Structure B. The only difference is the use of nitride layer as the insulator layer, instead of oxide in Structure B. Consequently, similar to Structure B, FDSOI device performance is

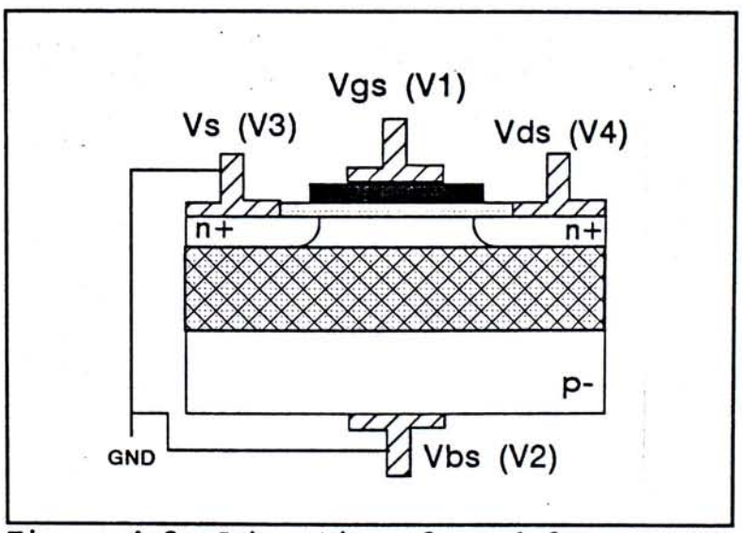


Figure 4.3 Schematic of a 1.2μm SOI(N) NMOS 1000/3500 NBC structure (Structure C).

also ensured in Structure C. Alternation to the region statement to "REGION NUM=2 NITRIDE Y.MIN=0.1 Y.MAX=0.45" in the source file is needed to account for the difference in the use of nitride insulator material.

4.3.4 1.2μm SOI(O) NMOS 1000/3500 WBC

This is a novel Silicon-On-Insulator n-channel MOS transistor structure using oxide as the insulator layer; the top silicon overlayer is chosen as 1000Å thick whereas those of the insulator layer is 3500Å; As described in Chapter 3, this novel structure contains a body contact, hence called With Body-Contact (WBC) structure, with size equal to the channel region. For simplicity, this structure is called Structure D in the rest of this thesis.

As shown in Figure 4.4, an opening in the insulator layer underneath the gate region is seen in this structure. Apart from this difference, this structure is basically identical to Structure B. Since the entire gate region is open, depletion width extend fully down into the substrate region reaching a depth of X_{dmax}.

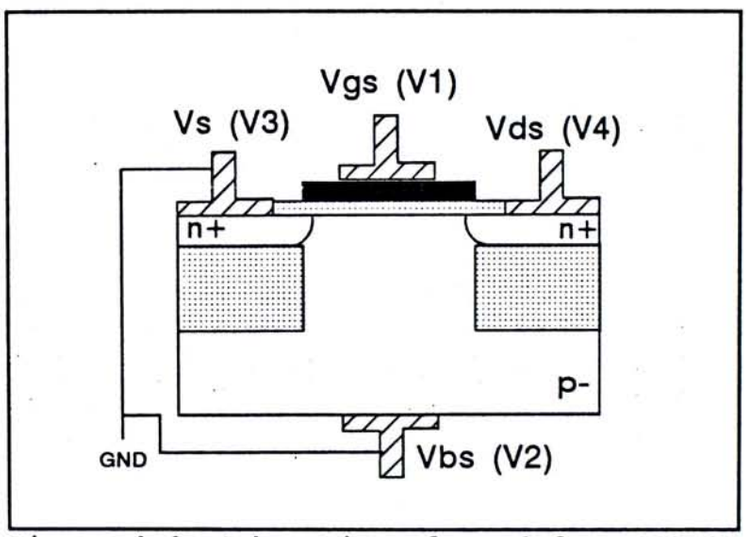


Figure 4.4 Schematic of a 1.2μm SOI(O) NMOS 1000/3500 WBC structure (Structure D).

To account for this special configuration, two REGION statements, "REGION NUM=2 OXIDE Y.MIN=0.1 Y.MAX=0.45 X.MAX=0.5" and "REGION NUM=3 OXIDE Y.MIN=0.1 Y.MAX=0.45 X.MIN=1.7" are

needed to add into the basic source file.

4.3.5 1.2μm SOI(N) NMOS 1000/3500 WBC

This is a novel Silicon-On-Insulator n-channel MOS transistor structure using nitride as the insulator layer; the top silicon overlayer is chosen as 1000Å thick whereas those of the insulator layer is 3500Å; Again, this is a With Body-Contact (WBC) structure. The size of it is equal to the channel region. For simplicity, this structure is called Structure E in the rest of this thesis.

As shown in Figure 4.5, this structure is basically identical to Structure D; the only difference is the use of nitride as the material for insulator layer.

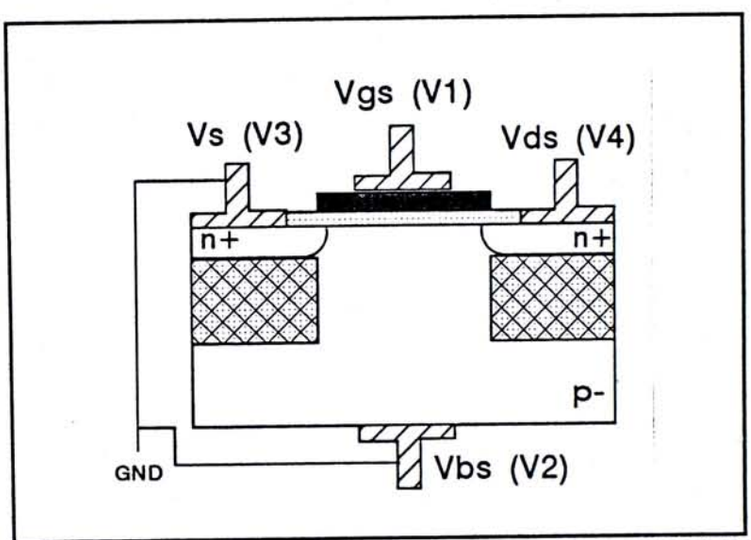


Figure 4.5 Schematic of a 1.2μm SOI(N) NMOS 1000/3500 WBC structure (Structure E).

Again, to account for this special configuration, two REGION statements, "REGION NUM=2 NITRIDE Y.MIN=0.1 Y.MAX=0.45 X.MAX=0.5" and "REGION NUM=3 NITRIDE Y.MIN=0.1 Y.MAX=0.45 X.MIN=1.7" are needed to add into the basic source file.

4.4 Summary

By far, identical nMOS transistor built on five different configurations have been constructed. The goal is to characterize the performance of the BCSOI

structures, i.e. Structure D and Structure E, and compare them with those in conventional SOI structures, i.e. Structure B and C respectively, and with bulk silicon structure, i.e. Structure A, so that justification on the BCSOI structures can be drawn thereafter.

Chapter 5 Simulation Results

5.1 Introduction

Apart form the advantages of the BCSOI structures as discussed in chapter 2.2, it is of equal importance to characterize the BCSOI structures electrically so as to verify their effectiveness. In this chapter, insulator layers, either using oxide or nitride, with or without body contact opening are directly placed under the junctions of a bulk silicon structure for MEDICI simulation comparisons. Key performance characteristics including back body effect, current-voltage (I-V) curves, transconductance and subthreshold swing of single n-channel MOS transistor on different structures are extracted and studied in details. Dependence on fundamental SOI structure parameters such as body contact window size, insulator thickness and silicon overlayer thickness are also explored.

5.2 Comparisons of Different Structures

Structures under simulation are already described in details in Chapter 4. To safeguard simulation consistency, identical initial grid allocation and similar source files are used for the five structures. There are only slight changes in the region statement in the source file to account for the change in configuration in different structures.

Comparisons of the device performance of the transistors built on different structures are made by investigating the impurity distributions, back body effect, breakdown voltage, current output capability, transconductance and subthreshold

swing. The goal is to characterize the performance of transistor that is built on BCSOI structures and to compare them with those in bulk silicon structure and on conventional SOI structures.

Table 5.1 reminds the readers the definitions of the five different structures that are under study:

Table 5.1 Definitions of the five structures under study by simulations.

Structures	Descriptions	Remarks
St. A	1.2μm NMOS Bulk (LDD)	Bulk silicon structure
St. B	1.2μm SOI(O) NMOS 1000/3500 NBC	Conventional SOI
St. C	1.2μm SOI(N) NMOS 1000/3500 NBC	Conventional SOI
St. D	1.2μm SOI(O) NMOS 1000/3500 WBC	BCSOI structure
St. E	1.2μm SOI(N) NMOS 1000/3500 WBC	BCSOI structure

5.2.1 Impurity Profiles of Structures

The impurity profiles of interest are those at the source (or drain, since symmetric junction structure is assumed) region and channel region of the transistor of different structures.

Source (or Drain) Region Impurity Profile

Since all the structures are constructed with similar source file, the peak concentration in the source (or drain) region are essentially identical. However, due to the existence of an insulator layer underneath the junctions, the impurity profiles of the structures that have or do not have insulator layer appears differently, which can be best represented by a plot of impurity concentration versus depth from the silicon surface.

Consider the source (or drain) impurity profile of Structure A as shown in

Figure 5.1, the distinct dip in the concentration profile indicates the existence of a p-n junction, i.e. the transition from the heavily doped n-type source (or drain) to the p-type substrate.

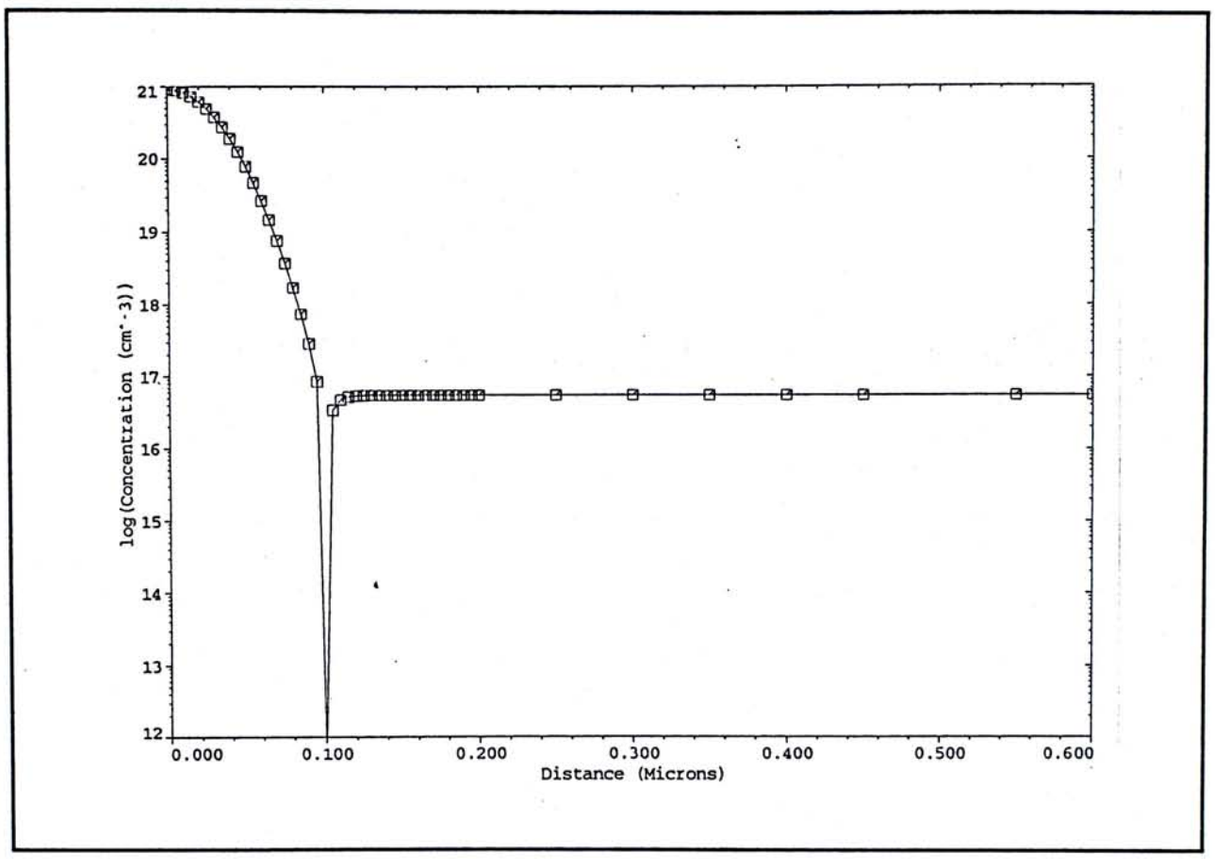


Figure 5.1 The doping concentration profile at junction region of Structure A

A parasitic capacitance, called junction capacitance is associated with such a p-n junction structure. According to SPICE model (Antognetti and Massobrio, 1988), the parasitic junction capacitance of a p-n junction with Area, A, and periphery perimeter, P, is modelled as:

$$C = \frac{(CJ)(A)}{(1 - V_R / PB)^{MJ}} + \frac{(CJSW)(P)}{(1 - V_R / PB)^{MJSW}} \qquad \text{[Eqn. 5.1]}$$

In SPICE terminology,

CJ zero-bias bulk capacitance per square meter;

CJSW zero-bias perimeter capacitance per meter;

MJ bulk-junction grading coefficient, usually taken as 0.5 for step-junction approximation;

MJSW perimeter capacitance grading coefficient, usually taken as 0.33 for linear gradient approximation;

PB bulk junction potential, and is related as $[E_g/2 + (kT/q)\ln (Na/n_i)]$, where n_i is the intrinsic doping concentration; and

V_R reverse bias at the junction;

Note that separate capacitance models are defined for the area and periphery of a junction. This is because the capacitance per unit area and its dependence on the reverse-bias voltage in the boundary regions of the diffusion are different from those associated with the flat junction. Moreover, below the thick oxide region, the doping is usually elevated as a result of channel stop implantation.

In classical p-n junction theory, CJ and CJSW are respectively related as:

$$CJ = \left[\frac{q\ \epsilon_{si}\ \epsilon_o}{2\left(\frac{1}{N_j}+\frac{1}{N_B}\right)(\phi_o+V_R)} \right]^{1/2} \qquad \text{[Eqn. 5.2]}$$

$$CJSW = \left[\frac{q\ \epsilon_{si}\ \epsilon_o}{2\left(\frac{1}{N_j}+\frac{1}{N_{sw}}\right)(\phi_o+V_R)} \right]^{1/2} \qquad \text{[Eqn. 5.3]}$$

where N_j is the doping concentration of the junction;

N_B is the doping concentration of the substrate beneath the junction;

N_{sw} is the doping concentration at the sides of the junction;

ϕ_o = $(kT/q)\ln(N_jN_B/n_i^2)$; and

ϕ_o' = $(kT/q)\ln(N_jN_{sw}/n_i^2)$ are the built-in potential of a p-n junction.

With reference to the above models, it is clear that, in bulk structure, parasitic junction capacitance arise from two parts, the modulation between the junction and the substrate underneath it; and the modulation between the junction and the region surrounding it. Furthermore, junction capacitance is proportional to the square root of the dielectric constant of the material where the junction exist. Since the dopant concentration that surrounds the junction is usually of several orders of magnitude lower than the junction itself, the square root of such a concentration also dominates the magnitude of junction capacitance.

Visualizing the metal wire connecting the source (or drain) region as a source of inductance with a finite inductance L, then the switching frequency at the junction is proportional to $(LC)^{-1/2}$. In other words, for the same circuit layout design, where L is fairly not changeable, higher switching frequency can be realized if the junction capacitance C is reduced.

In conventional SOI structures, i.e. Structure B and C, since an insulator layer exists under the source and drain junctions, junction dopant impurity can only extend to the insulator surface. As shown in Figure 5.2, the continuity of the impurity profile is "truncated" by the insulator layer. No distinct p-n junction is observed and the source (or drain) junction edge is abruptly cut off.

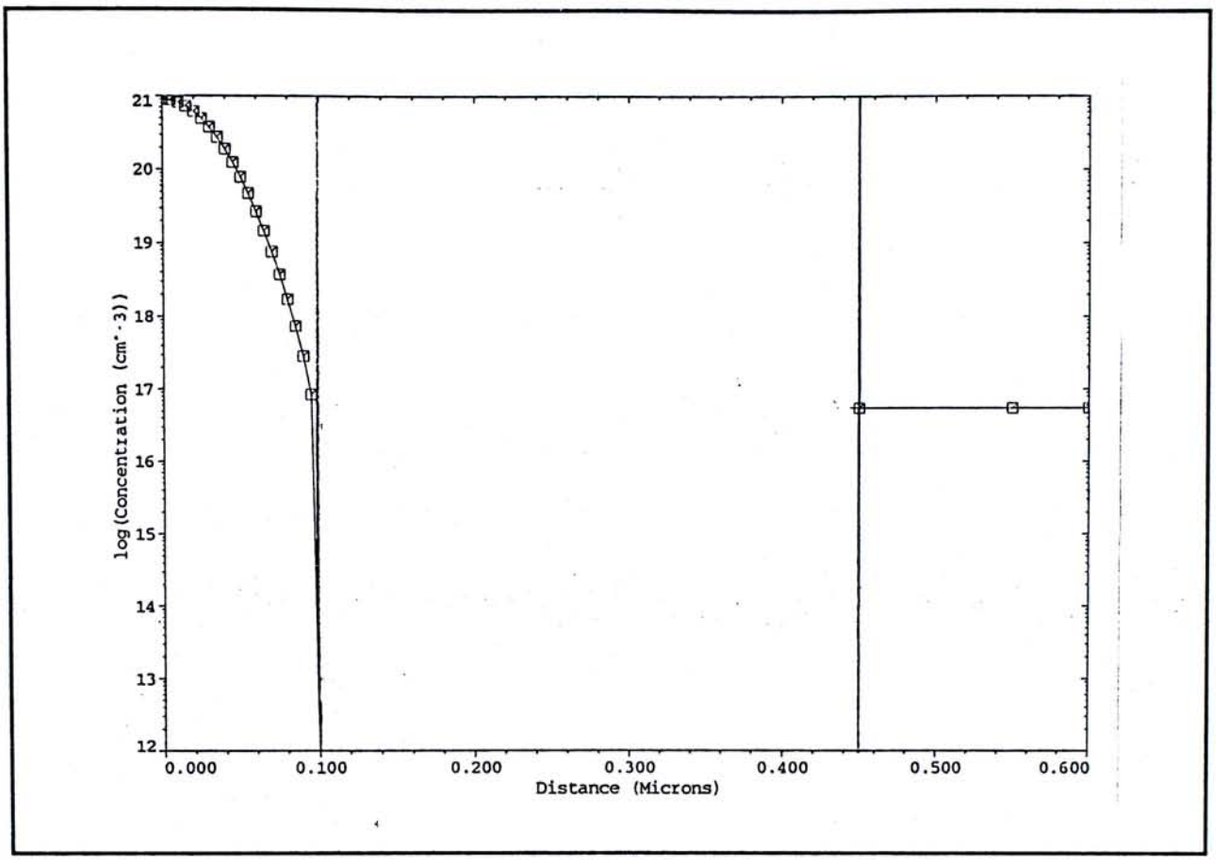


Figure 5.2 "Truncated" concentration profile exists in both conventional and BCSOI Structure.

Instead of being surrounded by silicon material, three sides of a junction in conventional SOI structure are surrounded by insulator material. May it be nitride or oxide, the dielectric constants of both the materials are lower than silicon ($\epsilon_{silicon}$ = 11.9; ϵ_{oxide} = 3.9; $\epsilon_{nitride}$ = 7). A reduced dielectric constant means a reduced junction capacitance, according to classical p-n junction model.

On the other hand, there shall have almost no active dopant exist in the insulator. Although the classical junction model may not be appropriate to accurately model the junction behaviour in conventional SOI structure, a further reduction in junction capacitance is envisaged, which in turns explains why circuits built on SOI structures can be operated with higher frequency.

In the BCSOI structures, i.e. Structure D and E, since the insulator layer

underneath the junctions are preserved. The impurity profile at junctions are in fact identical to those in conventional SOI structures and will appear exactly as the one in Figure 5.2.

As a consequence, in view of the very similar junction configuration, the switching speed advantage over bulk silicon substrate in conventional SOI structure can therefore also be maintained in BCSOI structure.

Channel Region Impurity Profile

As described in Chapter 4, the uniform substrate impurity doping is chosen in such a concentration that no additional surface threshold voltage adjustment implant or deep anti-punchthrough implant is required while ensuring the threshold voltage of the transistor in the proper range. Given that, if one considers a plot of impurity concentration versus depth from silicon surface at the gate region, a uniform doping profile is expected.

Shown in Figure 5.3 is the impurity profile plot of Structure A, D and E. A flat line is observed. The concentration of it is in fact the substrate doping concentration. Due to having an opening in the insulator layer under the entire channel region, the doping profile is a continuous downward one even in the BCSOI structures.

On the contrary, the doping profile continuity is disrupted at the insulator layer in conventional SOI structures as shown in Figure 5.4. Nevertheless, the doping concentration is uniform on both sides of the insulator layer.

The best visualization of the impurity doping distribution of an entire transistor can be observed from the 3-dimensional plots. The plots for Structure A, B and C, and D and E are shown in Figure 5.5, 5.6 and 5.7 respectively.

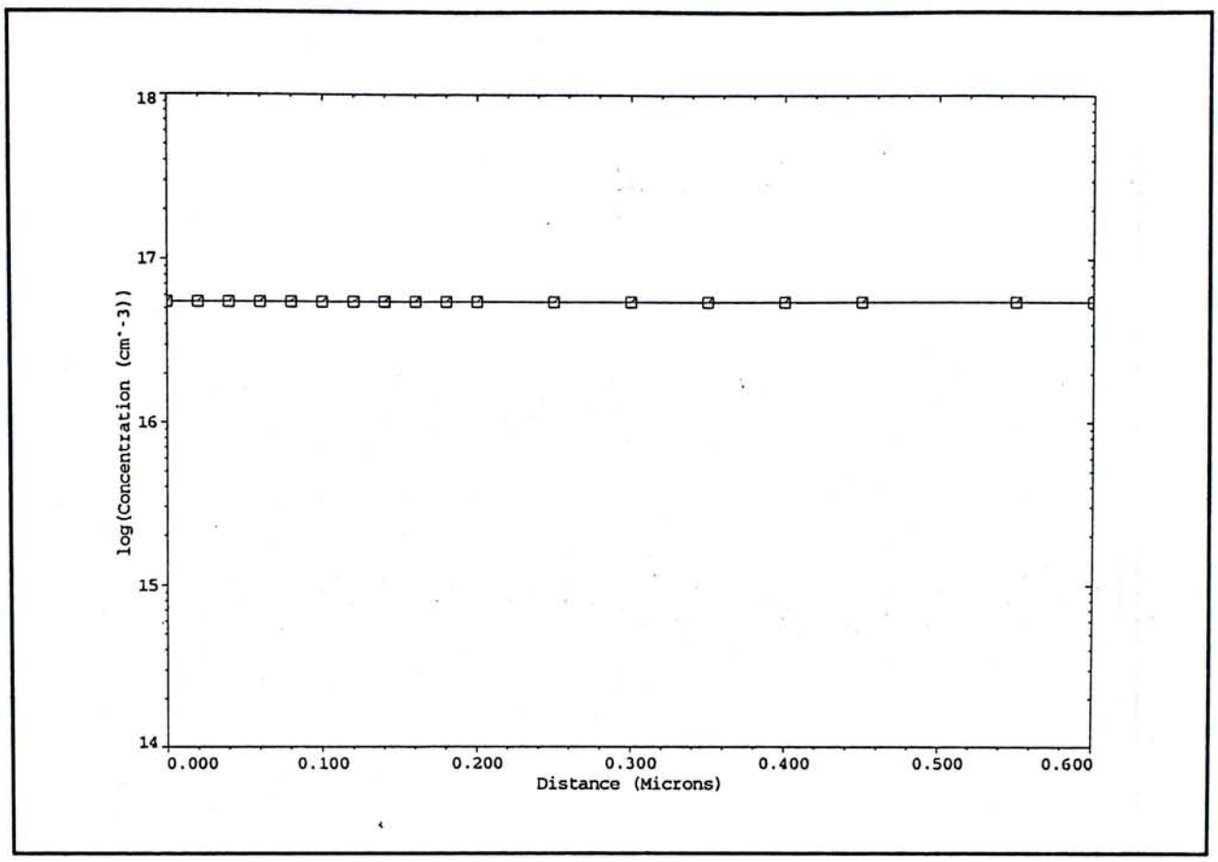


Figure 5.3 The channel impurity profile of Structure A, D and E.

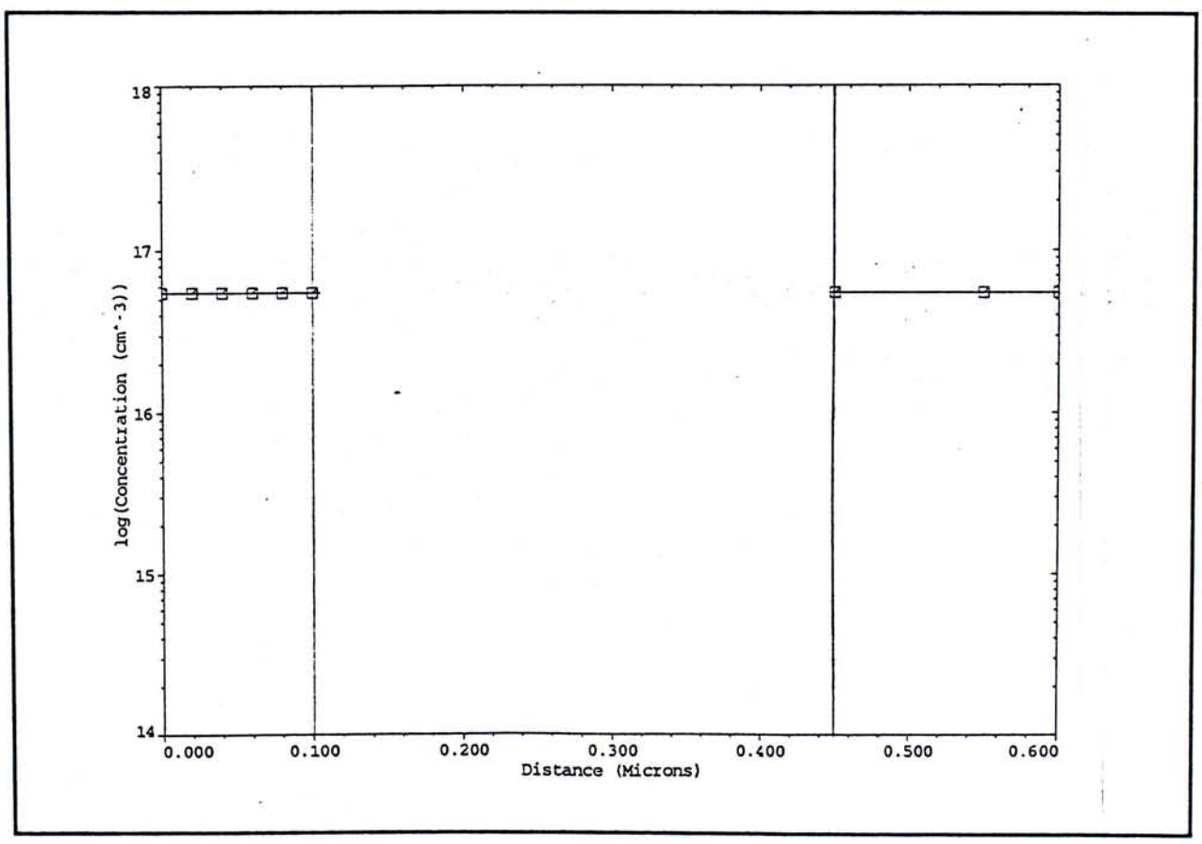


Figure 5.4 The channel impurity profile plot of Structure B and C.

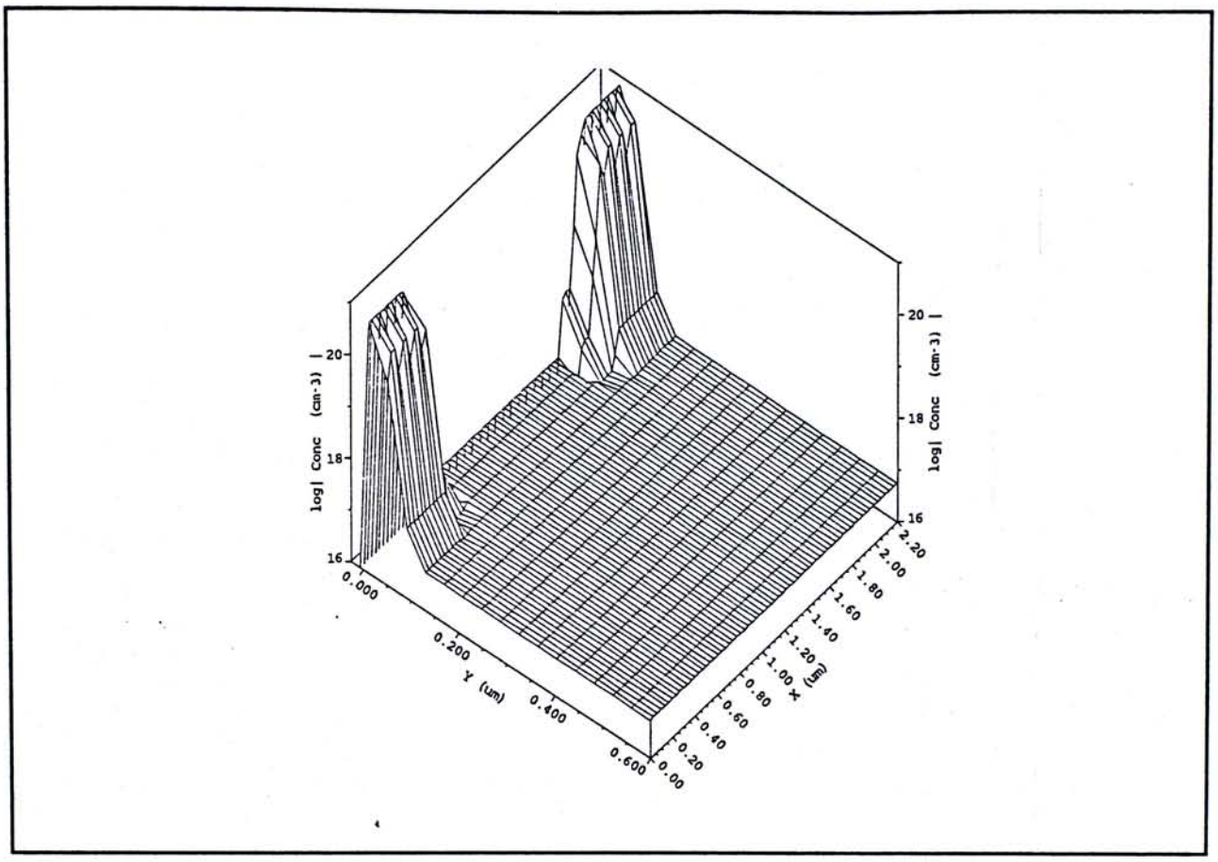


Figure 5.5 The 3-Dimensional impurity plot of Structure A.

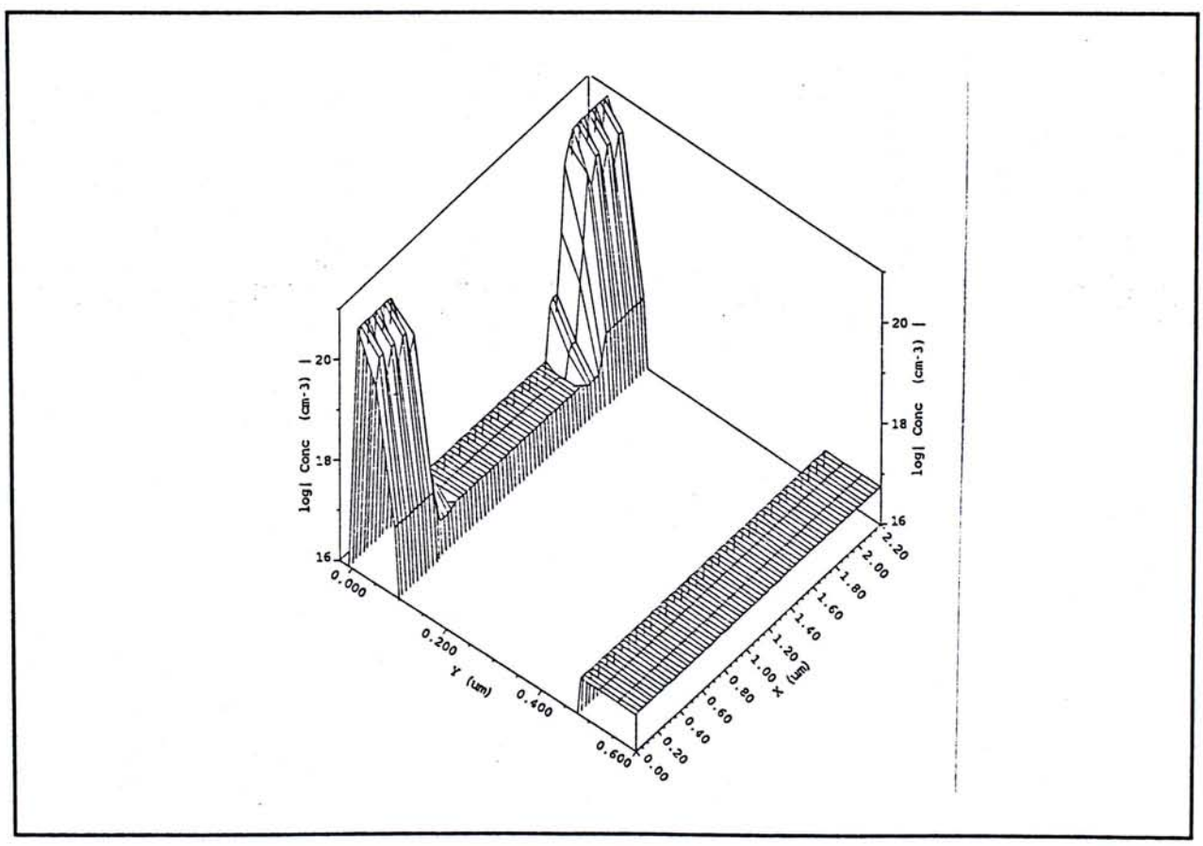


Figure 5.6 The 3-Dimensional impurity plot of Structure B and C.

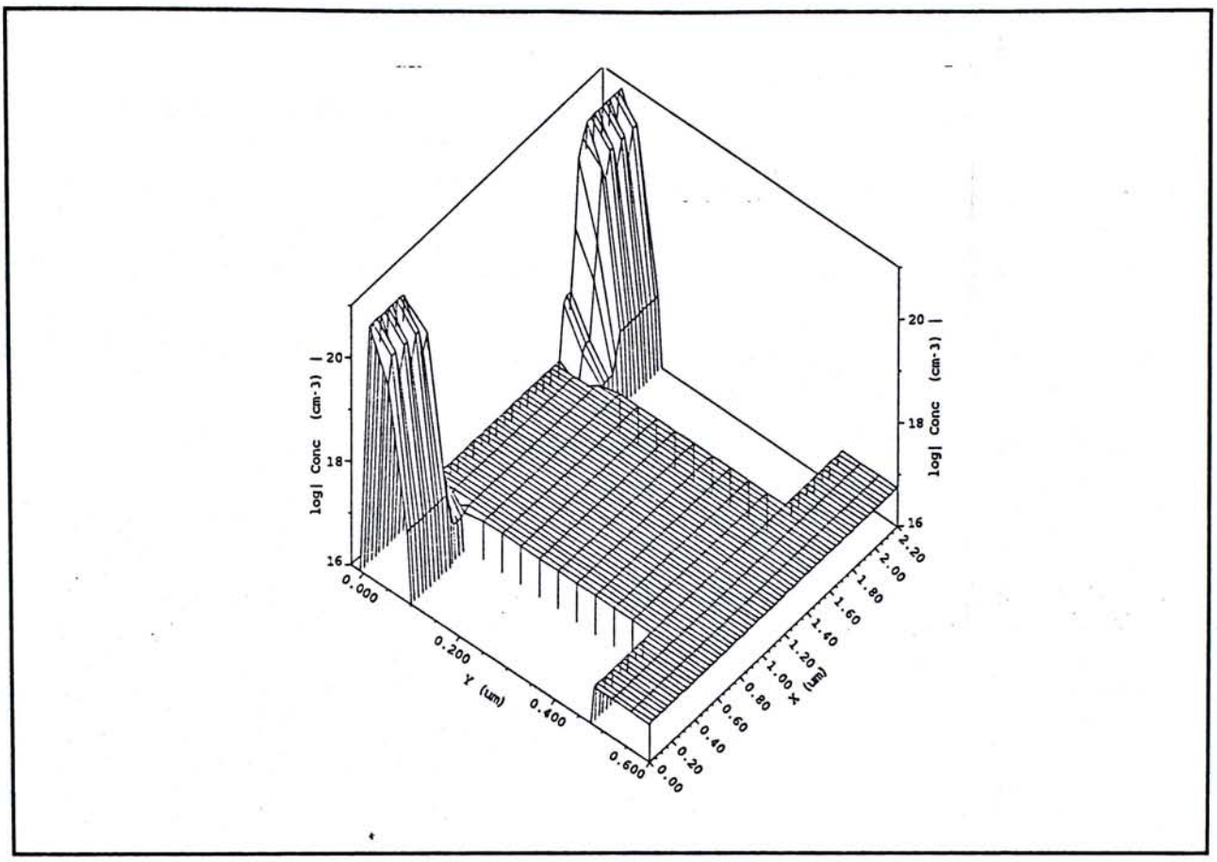


Figure 5.7 The 3-Dimensional impurity plot of Structure D and E.

It is clear that, although the overall doping impurity distribution may be similar, continuity of them in different structure is blocked by the different insulator layer configuration. Device performance are apparently affected as a result.

5.2.2 Body Effect

In bulk devices, it is known that transistor threshold voltage (Vt) can be modulated by applying voltage at the substrate. In fact, the body effect can be defined as the dependence of the Vt on the substrate bias (bulk-to-source voltage V_{bs}), which can be represented by a "body effect" figure, i.e. a graph of drain-to-source current I_{ds} versus gate to source voltage V_{gs} at low drain-to-source voltage V_{ds} with various V_{bs}.

Although the application of V_{bs} is the only mean for circuit designer to modulate transistor threshold voltage, it is generally regarded as undesirable in circuit applications. Despite CMOS invertor is practically free of body effect, circuits such as CMOS NAND gate and CMOS OR gate which consist of transistors in series on the same substrate, may prone to be affected by body effect especially when the substrate potential are not properly kept from variation, and hence incur temporary logic malfunction.

Classically, the threshold voltage of a bulk nMOS transistor is given by

$$V_t = \phi_{ms} + 2\phi_f - \frac{Q_{ss}}{C_{ox}} + \frac{\sqrt{2\epsilon_{si}\ q\ N_a(2\phi_f - V_{bs})}}{C_{ox}} \qquad \text{[Eqn. 5.4]}$$

Defining Vto as the threshold voltage of the transistor at zero back bias, i.e. $V_{bs} = 0$, Eqn. 5.4 can then be re-written as

$$Vt = Vto + \gamma\,[(2\phi_f - V_{bs})^{1/2} - (2\phi_f)^{1/2}] \qquad \text{[Eqn. 5.5]}$$

where $\gamma = (2q\epsilon_{si}N_a)^{1/2}/C_{ox}$

γ is called body factor and has a unit of $V^{1/2}$ for bulk silicon devices. From Eqn. 5.5, it is clear that, for bulk silicon devices, the dependence of the threshold voltage on substrate bias is non-linear and is also modulated by structure parameters such as N_a and C_{ox}.

Figure 5.8 represents the simulated body effect figure of Structure A. It is apparent that threshold voltage (Vt) increase with more negative substrate bias V_{bs}. Because of the increase in Vt, the I_{ds} values at the same V_{gs} is lowered with increasing back bias.

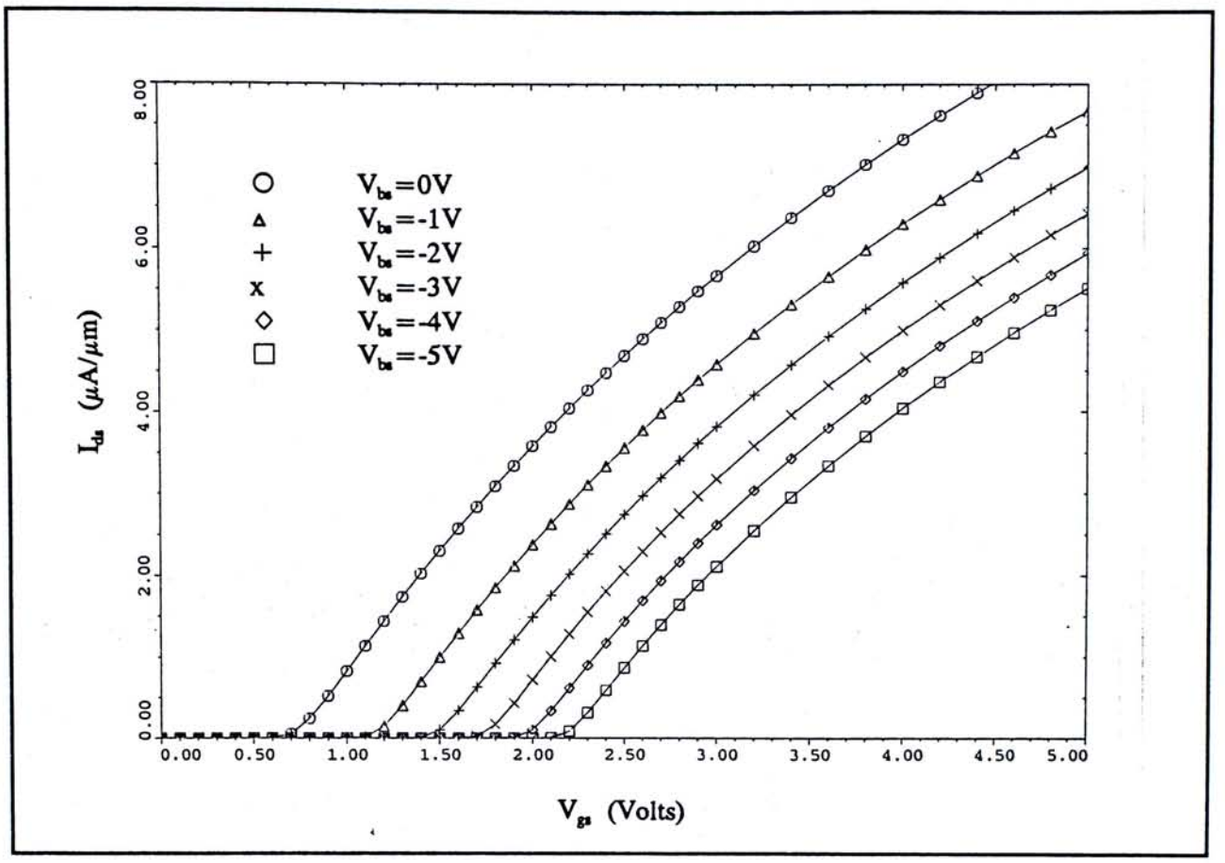


Figure 5.8 The simulated body effect figure for Structure A.

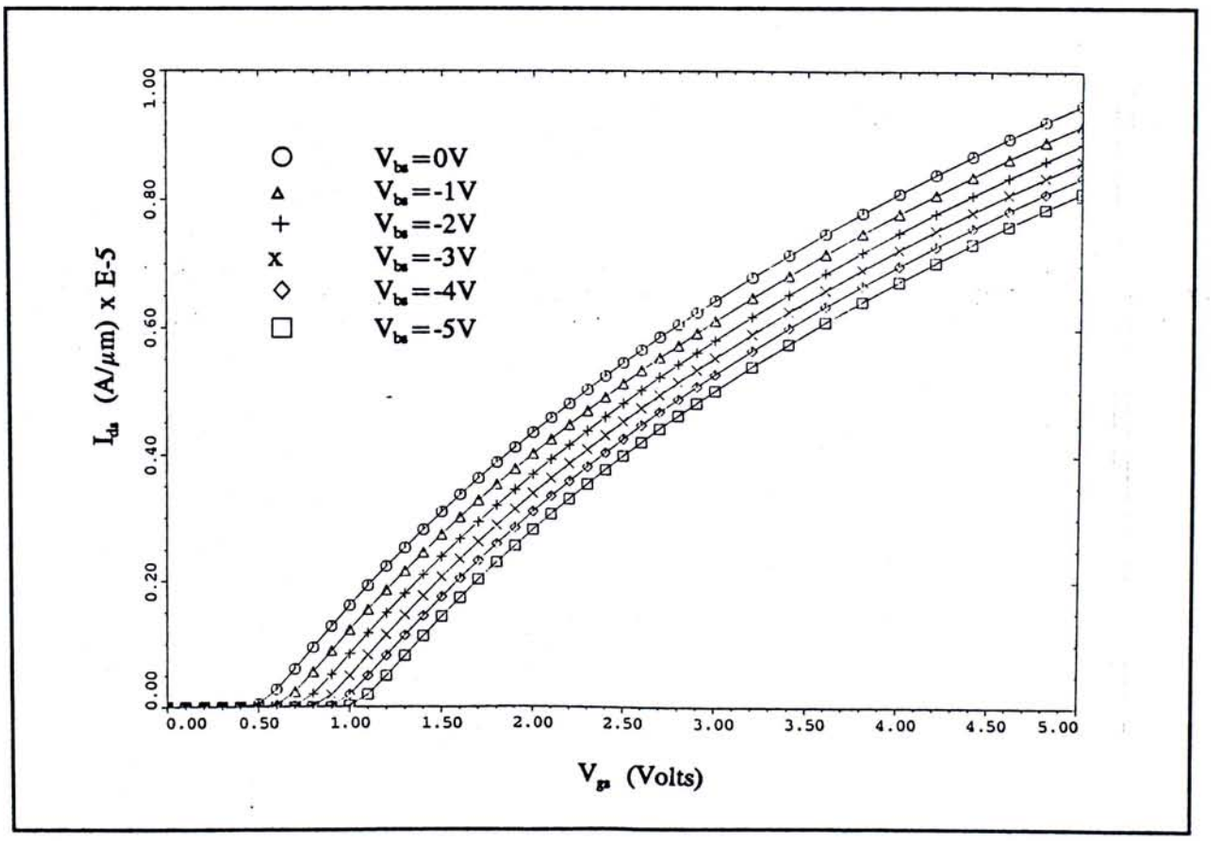


Figure 5.9 The body effect figure of Structure B.

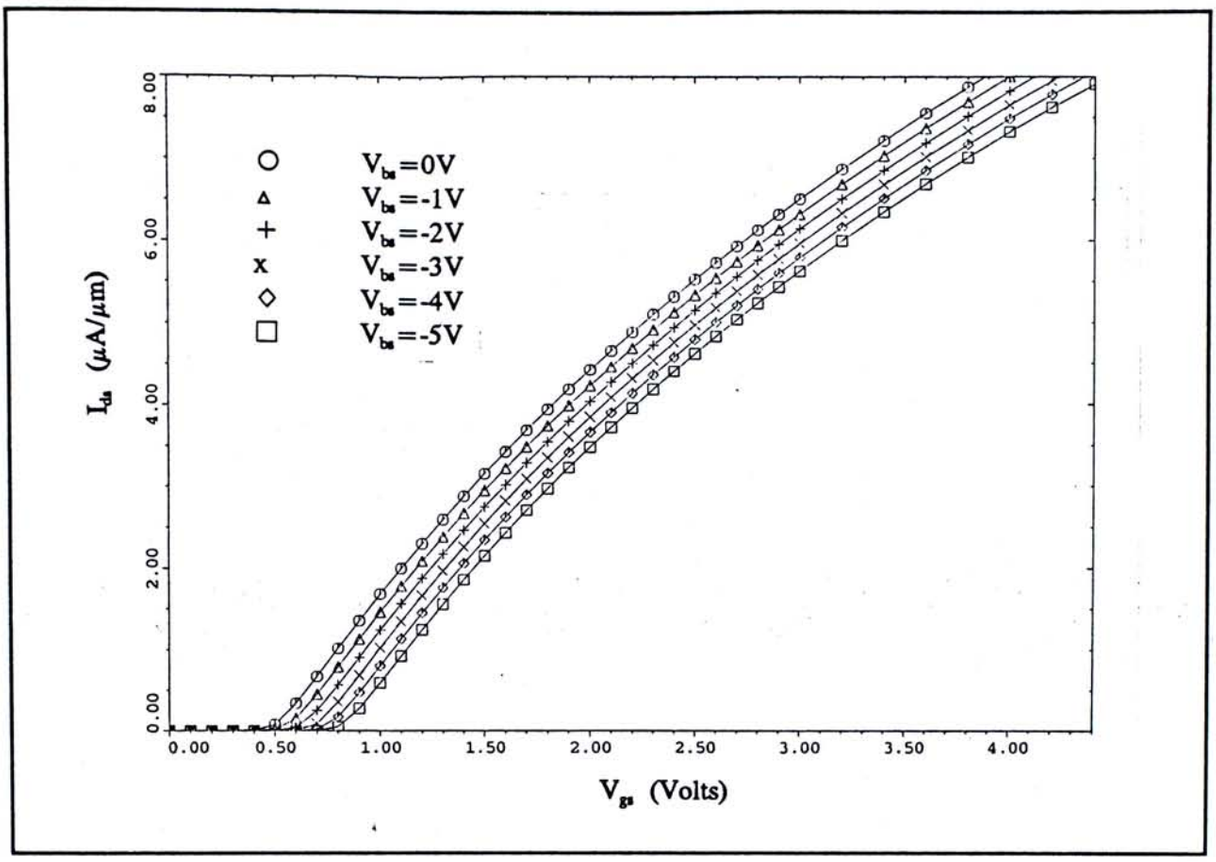


Figure 5.10 The body effect figure of Structure C.

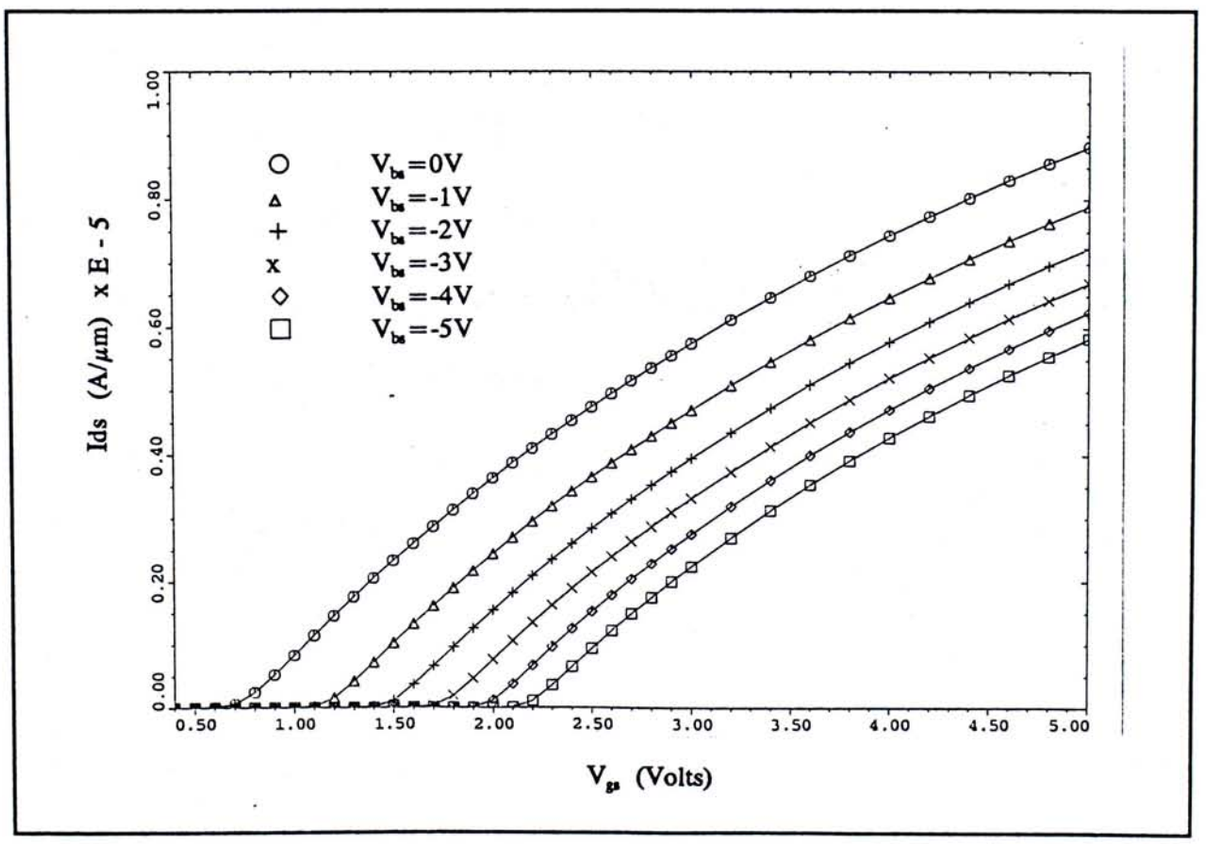


Figure 5.11 The body effect figure of Structure D.

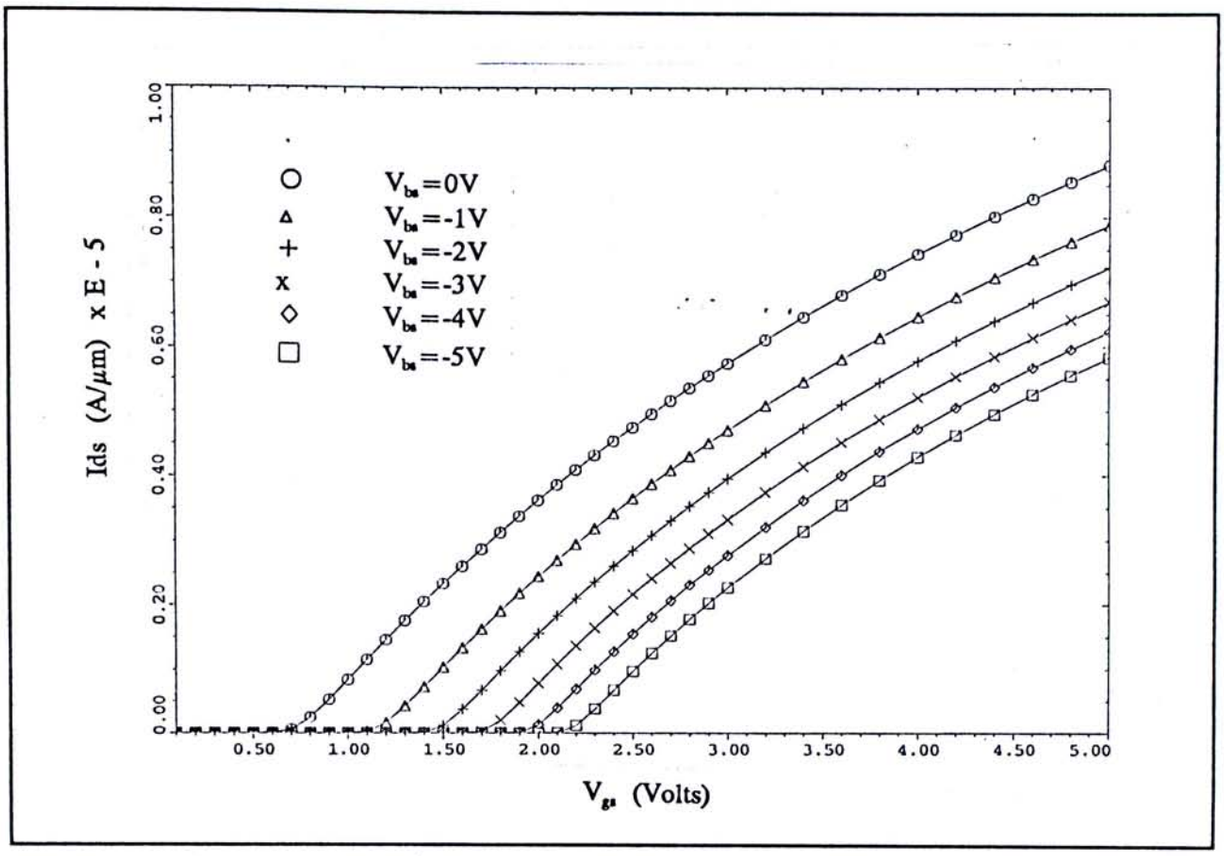


Figure 5.12 The body effect figure of Structure E.

Similarly, the body effect figures of Structure B, C, D and E are shown in Figure 5.9, 5.10, 5.11 and 5.12 respectively. One can observe that devices built on Structure B and C have very similar body effect characteristics. The same is true for devices built on Structure A, D and E.

Comparisons of the body effect of the five structures can best be viewed in a composite graph as shown in Figure 5.13 and 5.14 on which the data points have been normalized to the corresponding Vt and I_{ds} values at zero back bias. Apparently, the Vt of conventional SOI devices are the least susceptible to the application of back bias. The I_{ds} degradation is therefore the least severe.

According to Colinge 1991, the Vt of conventional SOI devices have a linear dependence on V_{bs}. Such a concept are indeed verified as one can observe the straight line characteristics for both Structure B and C.

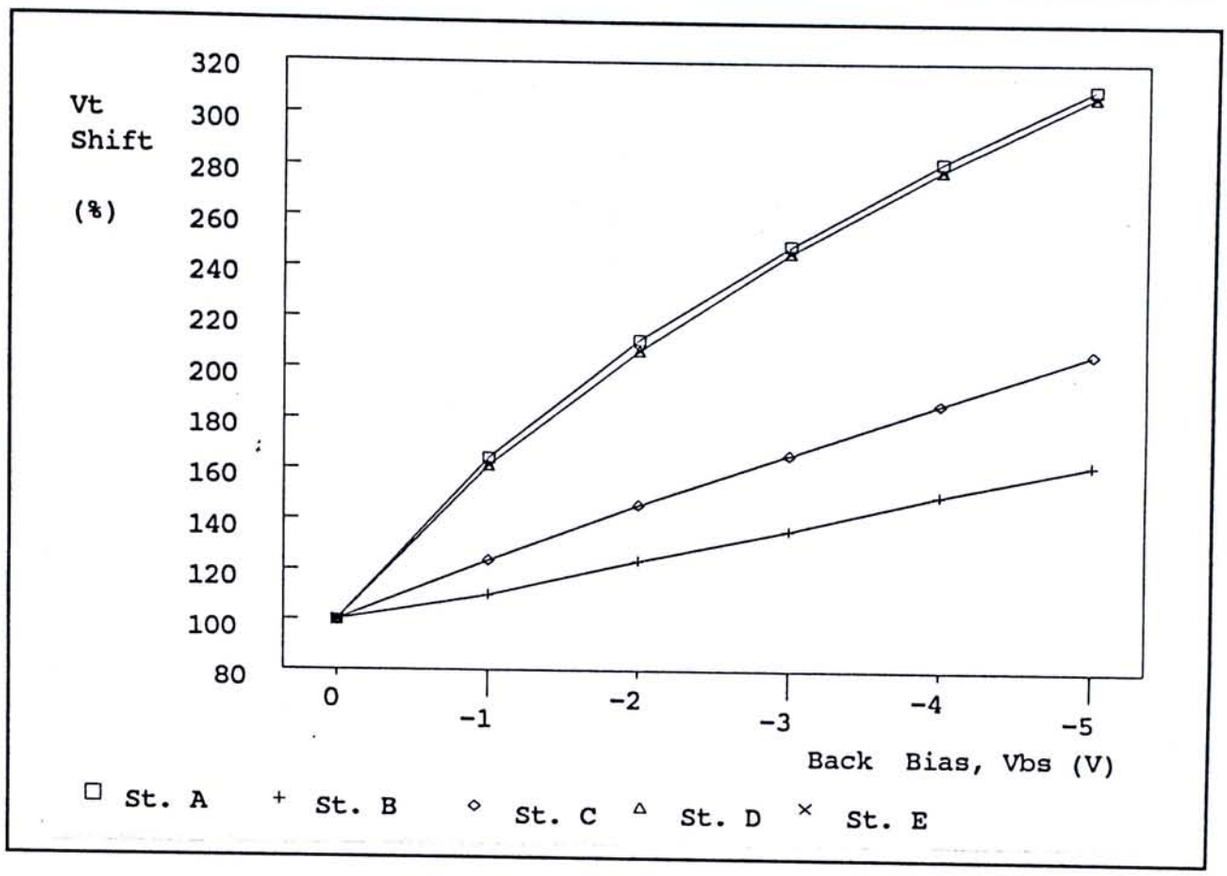


Figure 5.13 Comparisons of the increase of "normalised" threshold voltage due to back bias.

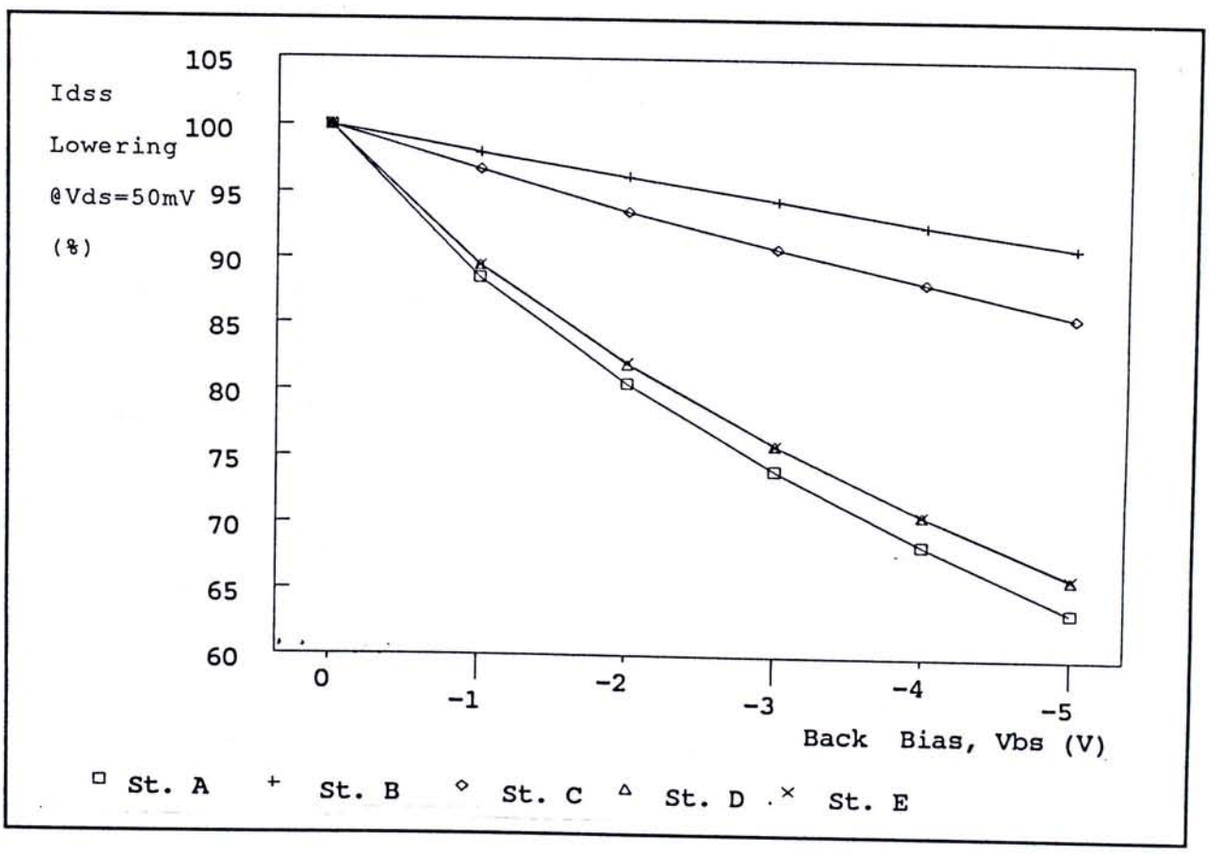


Figure 5.14 Comparisons of "normalized" Ids degradation due to back bias.

On the contrary, due to having an opening in the insulator layer, device on Structure D and E behave alike those on Structure A in terms of Vt increment against V_{bs}. Nevertheless, the I_{ds} degradation is slightly less severe than bulk device, and device on Structure D behaves slightly better than those on Structure E.

It is concluded that the body effect of nMOS transistor on BCSOI structures is not as ideal as in conventional SOI structures, but shows very similar behaviour in terms of Vt shift and has slight improvement in terms of I_{ds} degradation as compared to those on bulk silicon substrates.

5.2.3 Breakdown Voltage and Transistor Current Driving

The breakdown voltage and transistor driving can best be examined from a plot of I_{ds} versus V_{ds} of various V_{gs}.

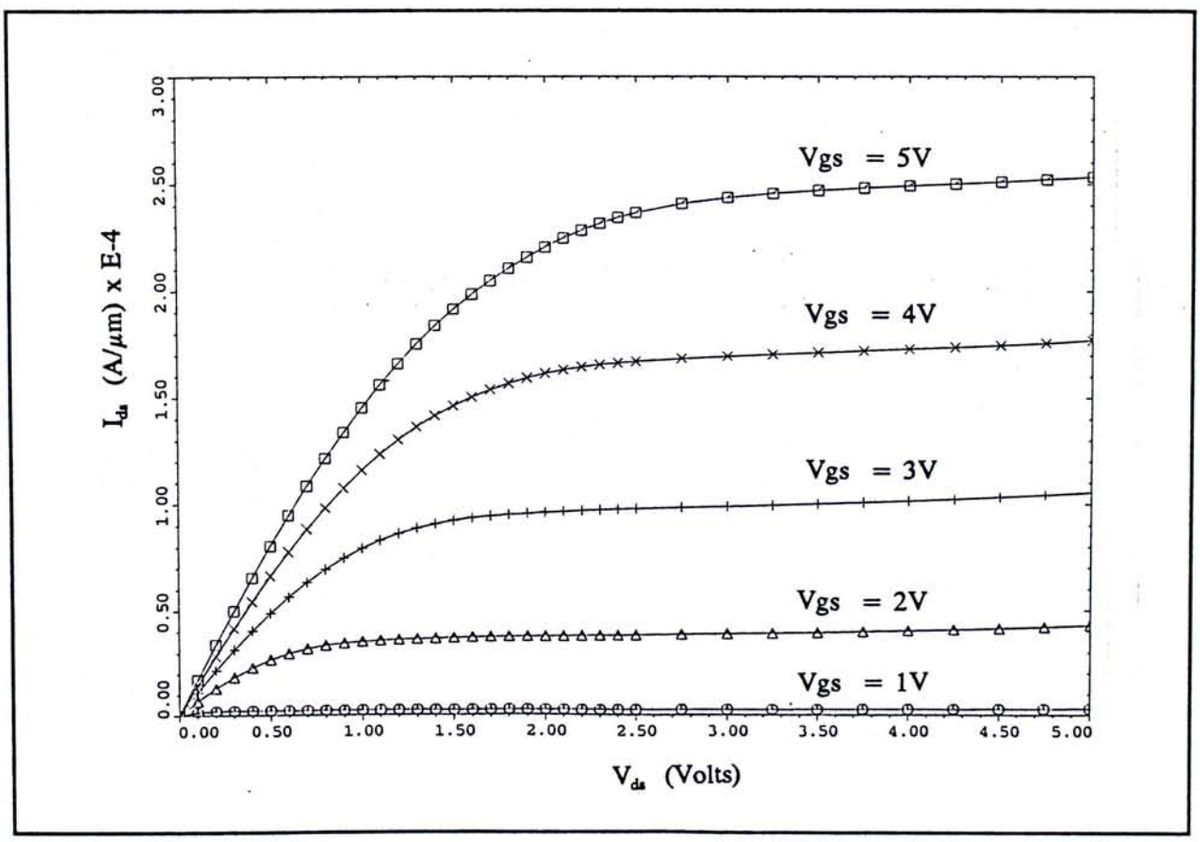


Figure 5.15 The simulated I-V characteristics of Structure A.

The simulated I-V (I_{ds} versus V_{ds}) characteristics of Structure A is shown in Figure 5.15. Long channel transistor behaviour is observed and the transistor is well-behaved at V_{ds}=5.0V. By the same token, the I-V characteristics of Structure B, C, D and E can be seen in the subsequent Figure 5.16, 5.17, 5.18 and 5.19 respectively.

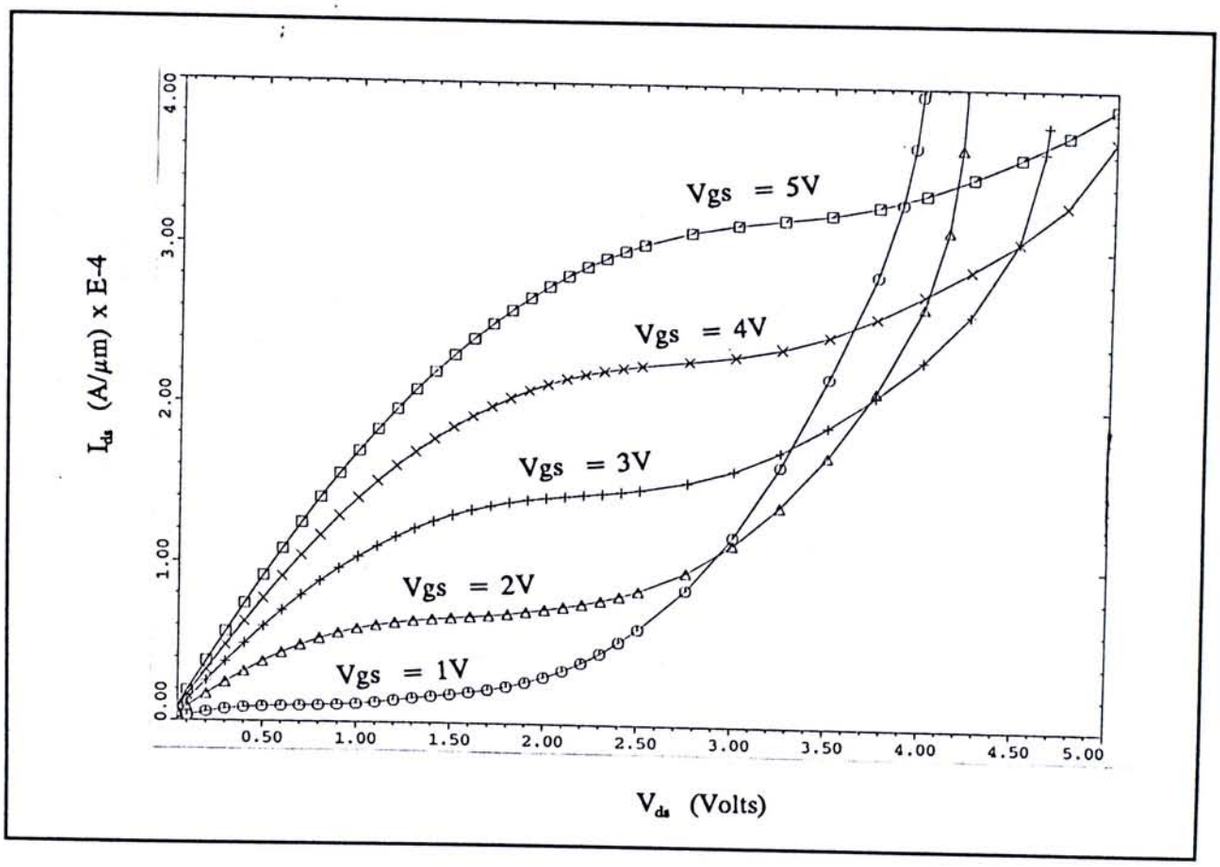


Figure 5.16 The simulated I-V characteristics of Structure B.

Referring to Figure 5.16 or 5.17, for those conventional SOI structures, it is observed that I_{ds} increase very rapidly at high V_{ds} especially when the V_{gs} values are low. Such a rapid I_{ds} increment at high V_{ds} cause non-convergence in computer simulation before V_{ds} reaches 5.0V and hence excludes such a transistor from the possibility of working at 5.0V in reality. This phenomena is in fact the undesirable floating body effect in conventional SOI structure that described in Chapter 2, and

is also the major drawbacks that have limited them from wide-spreading.

It is also noted from Figure 5.16 or 5.17 that convergence of simulation resumes up to at least V_{ds}=5.0V when V_{gs} equals to 4.0V and 5.0V. This can be explained as follows: At sufficiently high gate voltage, the induced gate potential is so strong that it starts to lower the potential barrier at the junction regions. In such a condition, the entire body becomes a conduction path connecting the drain and source directly. The transistor becomes really fully depleted and, there is no body region exists when the transistor is in conduction.

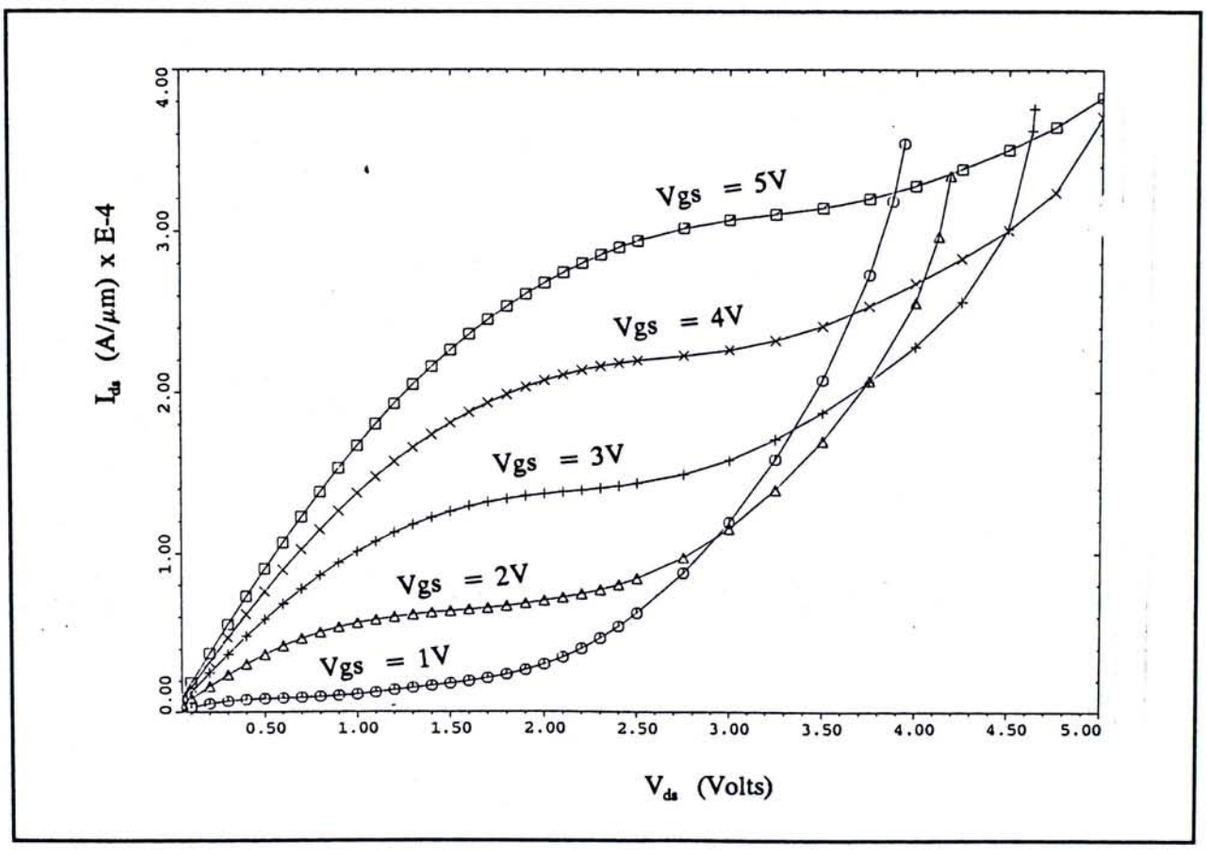


Figure 5.17 The simulated I-V characteristics of Structure C.

Contrarily, as evidenced in Figure 5.18 and 5.19, no floating body effect is observed in the BCSOI Structures D and E. Good long channel I-V characteristics are resulted. Breakdown voltage value is similar to those in bulk structure.

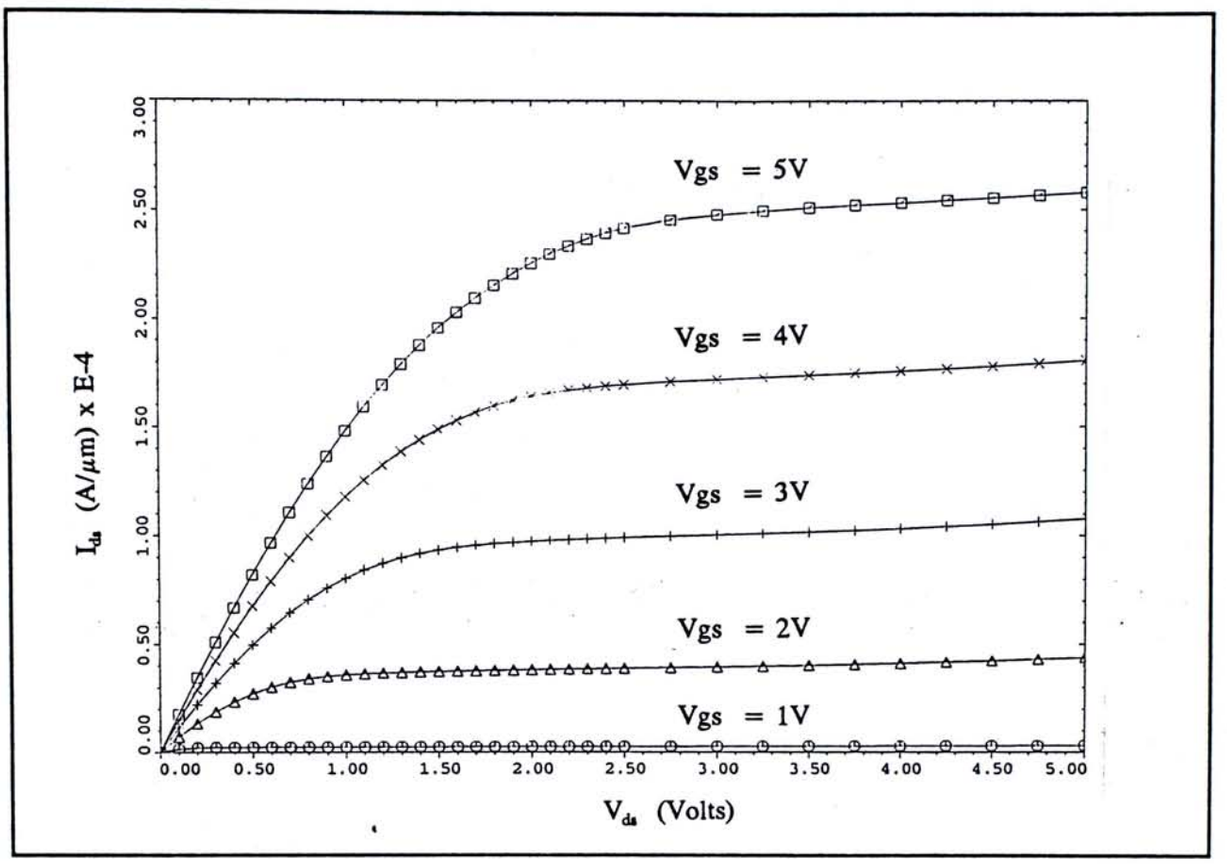


Figure 5.18 The simulated I-V characteristics of Structure D.

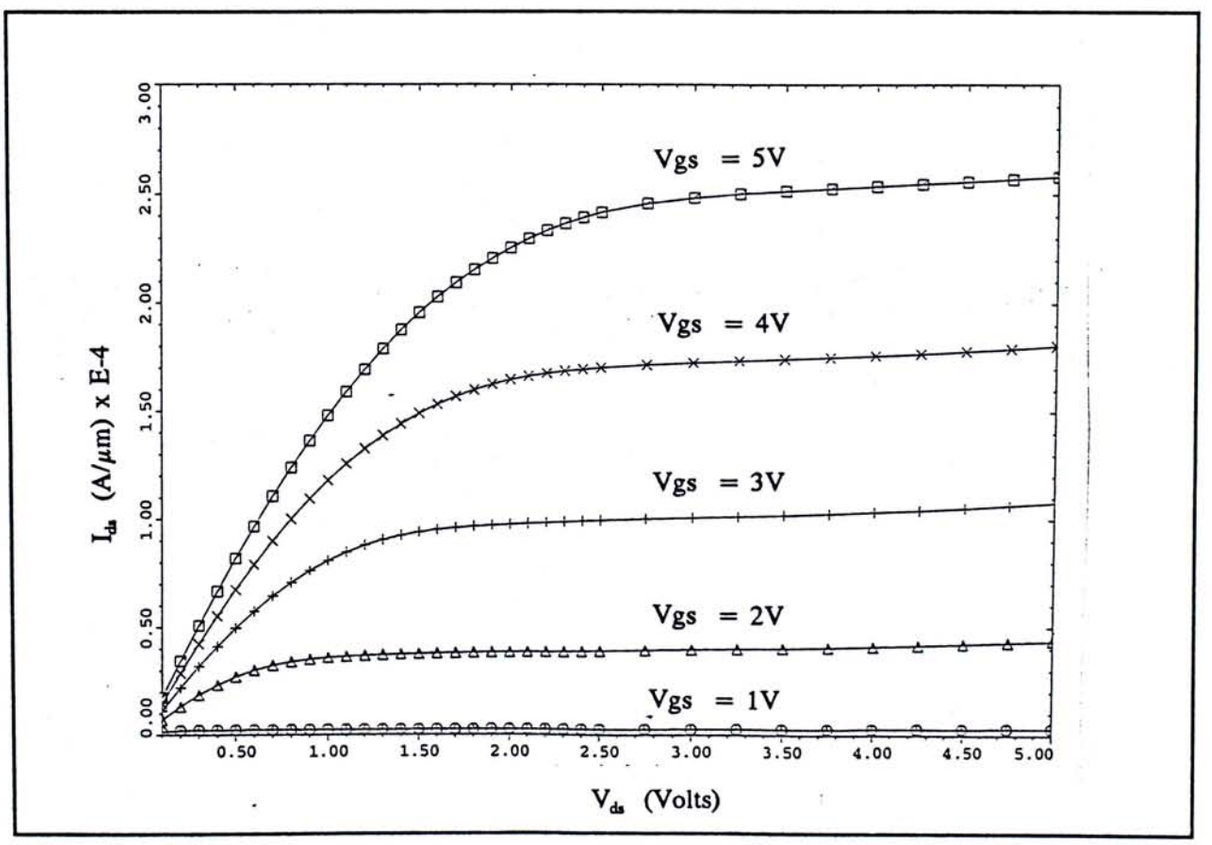


Figure 5.19 The simulated I-V characteristics of Structure E.

It is concluded is that the opening in the insulator layer in BCSOI structures can, as expected, effectively eliminate the floating body effect that exist in conventional SOI structure and the breakdown voltage performance is comparable to those of bulk silicon structure.

5.2.4 Transconductance and Mobility

Transconductance in linear region, g_m, can be used as a measure of current conduction capability of a transistor. It is defined by the derivative of I_{ds} against V_{gs} at a selected V_{ds} value. The magnitude of g_m of a transistor also determines the cut-off frequency, i.e. the maximum frequency that a transistor can handle. On the graph of Ids versus Vgs, g_m is in fact the slope of the lines as extracted on a selected V_{gs} and V_{ds} values.

Usually, the values of g_m of a transistor is considered at two regions, namely, the linear region and the saturation region. To ensure the transistor in linear region, a low V_{ds} value is needed. In this thesis, a value of 0.1V is selected when deriving linear region g_m; Contrarily, a high V_{ds} value is required to ensure the transistor in saturation region. Given that, a value of 5.0V is chosen for saturation region g_m derivation. The extracted values are shown in Table 5.1 for reference.

Table 5.1 Table of linear and saturation region transconductance of the Structures.

g_m (μA/Vμm)	St. A	St. B	St. C	St. D	St. E
Linear Region	3.409	3.434	3.428	3.482	3.472
Saturation Region	70.337	------	------	71.603	71.491

It is seen in Table 5.1 that no saturation region g_m values can be obtained for

Structure B and C since the floating body effects exist in the structures exclude them from having a convergent simulation result. The comparison is hence made only among Structure A, D and E for saturation region g_m.

No matter it is the linear region or saturation region g_m, the nMOS transistor on Structure A is consistently lowest among those on other structures. It shall be noted that when comparing the linear region g_m between Structure B and C as well as between Structure D and E, advantage of using oxide, rather than nitride, as buried insulator is apparent, though the improvement is not significant. It is more interesting to point out that the linear region g_m for BCSOI structures are of slight, about 1.3%, advantage over conventional SOI Structures.

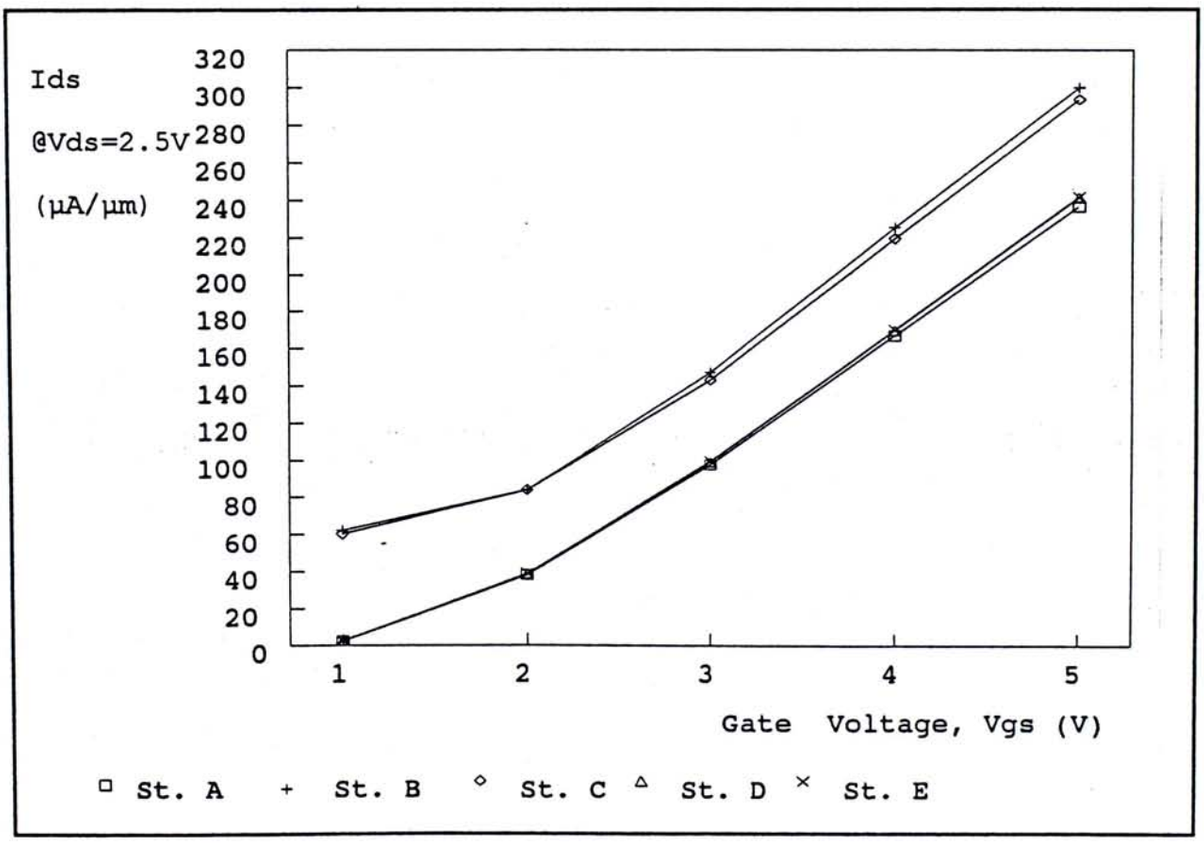


Figure 5.20 The graph of I_{ds} versus V_{gs} at V_{ds} = 2.5V of the Structures.

The current output I_{ds} against gate bias V_{gs} is compared in Figure 5.20 and

5.21 in which the V_{ds} value is taken at 2.5V and 5.0V respectively. Due to the floating body effects, for Structure B and C, no I_{ds} information can be resulted for V_{ds}=5.0V at low gate bias. Nevertheless, the current output for Structure B and C are always the highest, the improvement over other structures are 25 to 40%. On the other hand, almost identical behaviour are recorded for Structure D and E. The behaviour also have about 5% performance advantage over those in Structure A.

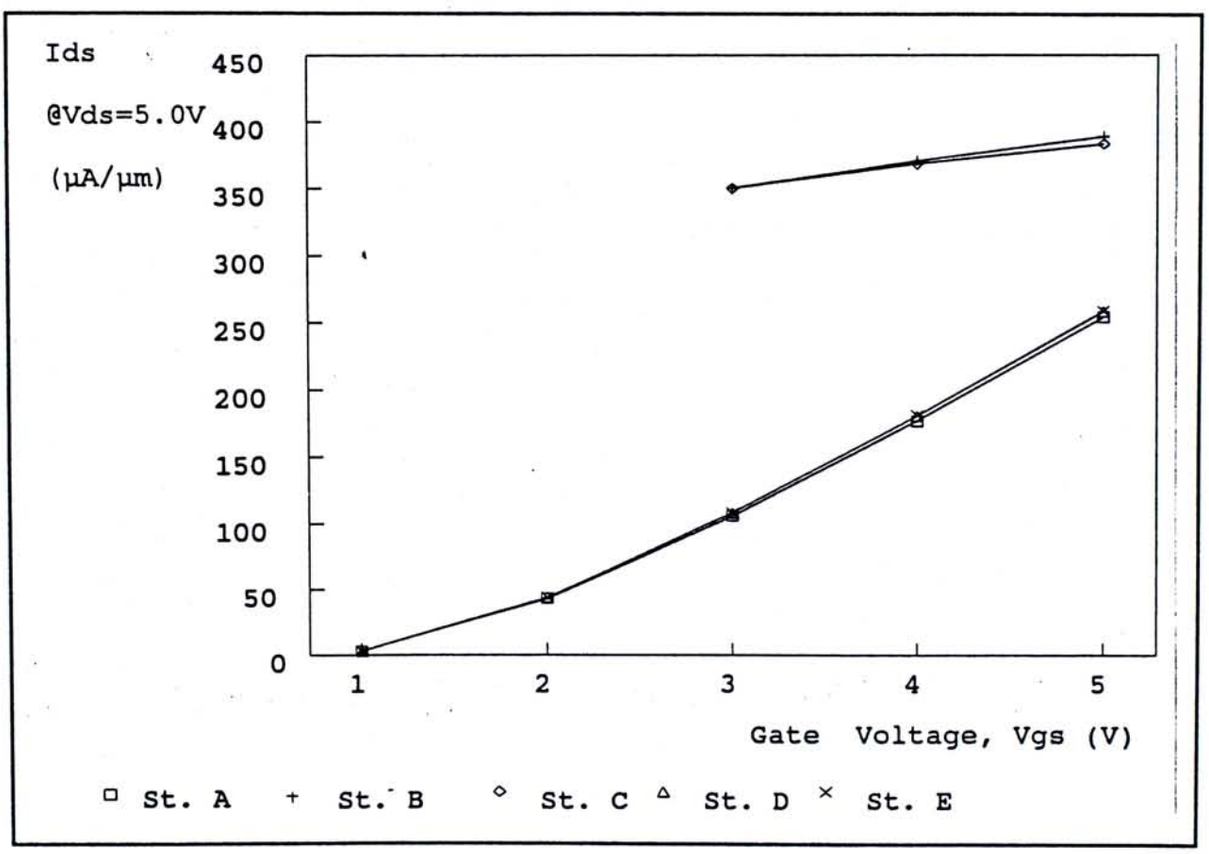


Figure 5.21 The graph of Ids versus Vgs at Vds=5.0V for the Structures.

Carrier mobility, μ_n, is related to transconductance, g_m, classically as $g_m = (W/L)\mu_n C_{ox} V_{ds}$ in linear region (C_{ox}: the gate capacitance). The relation indicates that calculation of carrier mobility requires the knowledge of g_m at a particular V_{ds} value. Nevertheless, the rule of thumb is that μ_n increases with increasing g_m,

though not necessarily in a linear way. As a result, the explanation of g_m improvement made above are also applied on the improvement of μ_n.

It is concluded that g_m , μ_n and hence current driving of nMOS transistor built on BCSOI structure are not as good as on conventional SOI structure but it has slight improvement over those on bulk silicon structure.

5.2.5 Subthreshold Swing

A plot of the I_{ds} (in logarimetic scale) versus V_{gs}, from negative to positive values, at both low (such as 0.05V) and high (such as 5.0V) V_{ds} values can reveal the on and off characteristics of a transistor as well as its leakage current level at subthreshold region both in the linear and saturation drain bias. Such a figure for Structure A is shown in Figure 5.22.

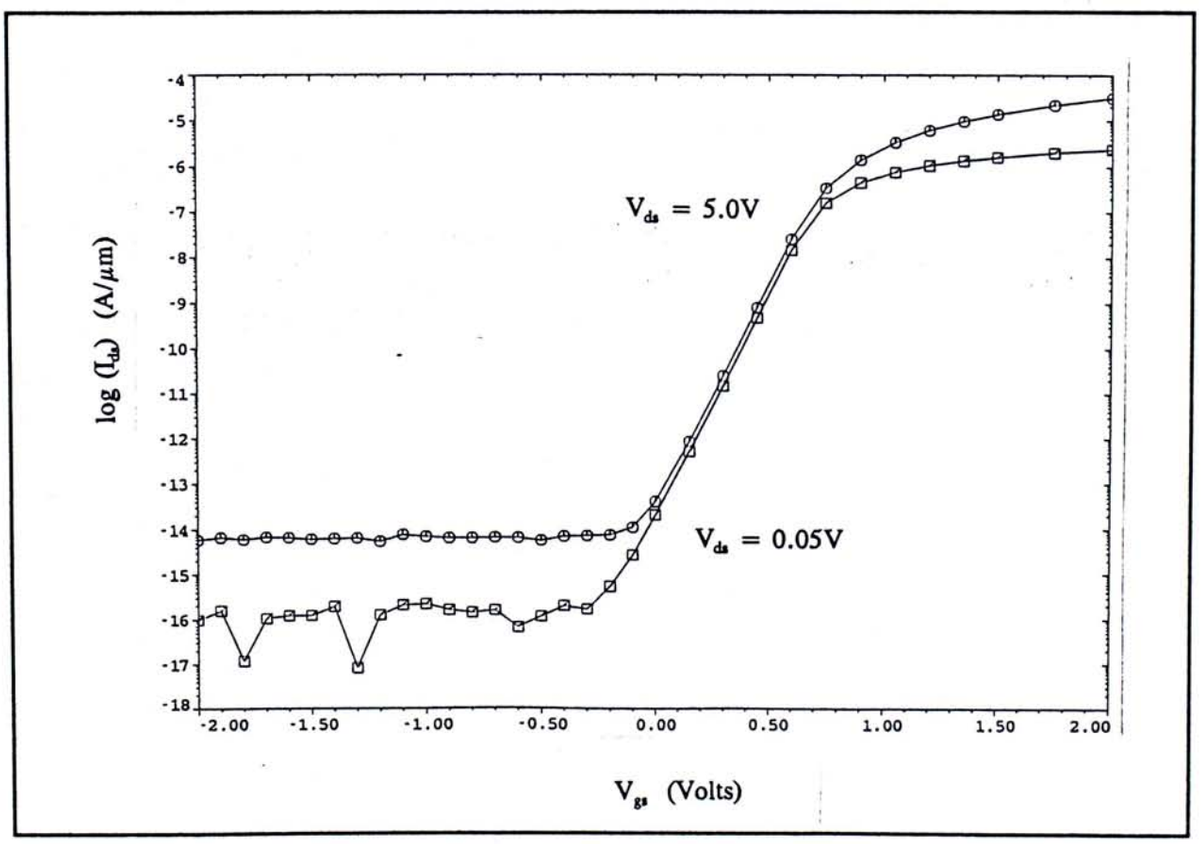


Figure 5.22 The simulated subthreshold swing characteristics for Structure A.

According to Figure 5.22, when V_{gs} is negative, leakage current exists in the transistor. The leakage current at high V_{ds} is about an order of magnitude higher than those at low V_{ds} bias. When V_{gs} is approaching the threshold voltage of the transistor, significant increase in I_{ds} is observed and can be seen as the almost "straight" line region. Upon further increase in V_{gs}, I_{ds} becomes saturated and starts to level off. The slope of the straight line, i.e. when current conduction increases significantly, represents how sensitive I_{ds} responds to V_{gs} increment. Subthreshold swing, S_t is defined as the reciprocal of such a slope. Mathematically, $S_t = [\partial(\log I_{ds})/\partial V_{gs}]^{-1}$, in unit of mV/decade.

With analogy to bipolar transistor theory (Chen, 1990), the subthreshold swing of bulk transistor can be related as

$$S_t = 2.3 \left(\frac{kT}{q}\right)\left(1 + \frac{C_d}{C_{ox}}\right) \qquad \text{[Eqn.5.6]}$$

where C_d is the capacitance due to the depletion width under the gate.

Depending on the structure configuration, S_t shall be different. A small value of S_t means the turn on or off is sharp, response is fast and channel current is effectively controlled by gate bias. From Figure 5.22, the S_t for Structure A is derived to be 102mV/decade, which is typical for a 1.2μm nMOS transistor.

Simulated subthreshold swing characteristics of Structure B, C, D and E are shown in Figure 5.24, 5.25, 5.26 and 5.27 respectively for comparisons.

As referred to Figure 5.24, a hysteresis is observed in the subthreshold swing curve of Structure B. At V_{ds}=0.05V, the curve is well-behaved. Contrarily, at V_{ds}=5.0V, during the forward V_{gs} sweeping, a disruption is observed. The disruption represents the point where a convergent solution is unable to be derived

by simulation. During a reverse V_{gs} sweeping, although no disruption is seen, the I_{ds} curve does not matched with the one during the forward V_{gs} sweeping.

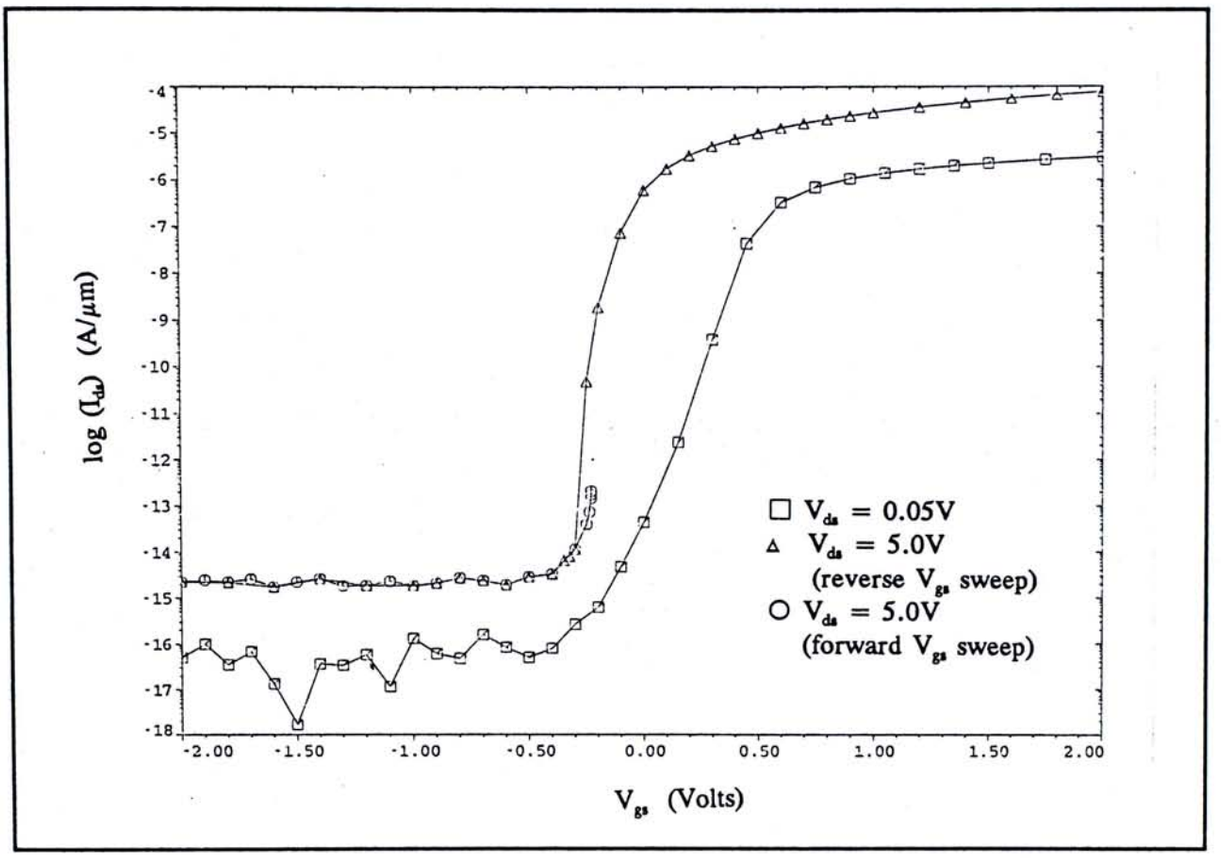


Figure 5.24 The simulated subthreshold swing characteristics for Structure B.

In other words, a loop shall exist in the subthreshold swing curve. Also, there is an apparent separation in the two subthreshold swing curves of different V_{ds} values. All these indicate that the hysteresis effect that associated with conventional SOI structure as described in section 2.4.2.1 is also reaffirmed by computer simulation.

Similarly, as referred to Figure 5.25, there are disruptions in the subthreshold swing curves for both V_{ds} bias for Structure C. During the reverse V_{gs} sweeping, no convergent solution can be obtained. Nevertheless, the existence of a loop is apparent, indicating the existence hysteresis effect.

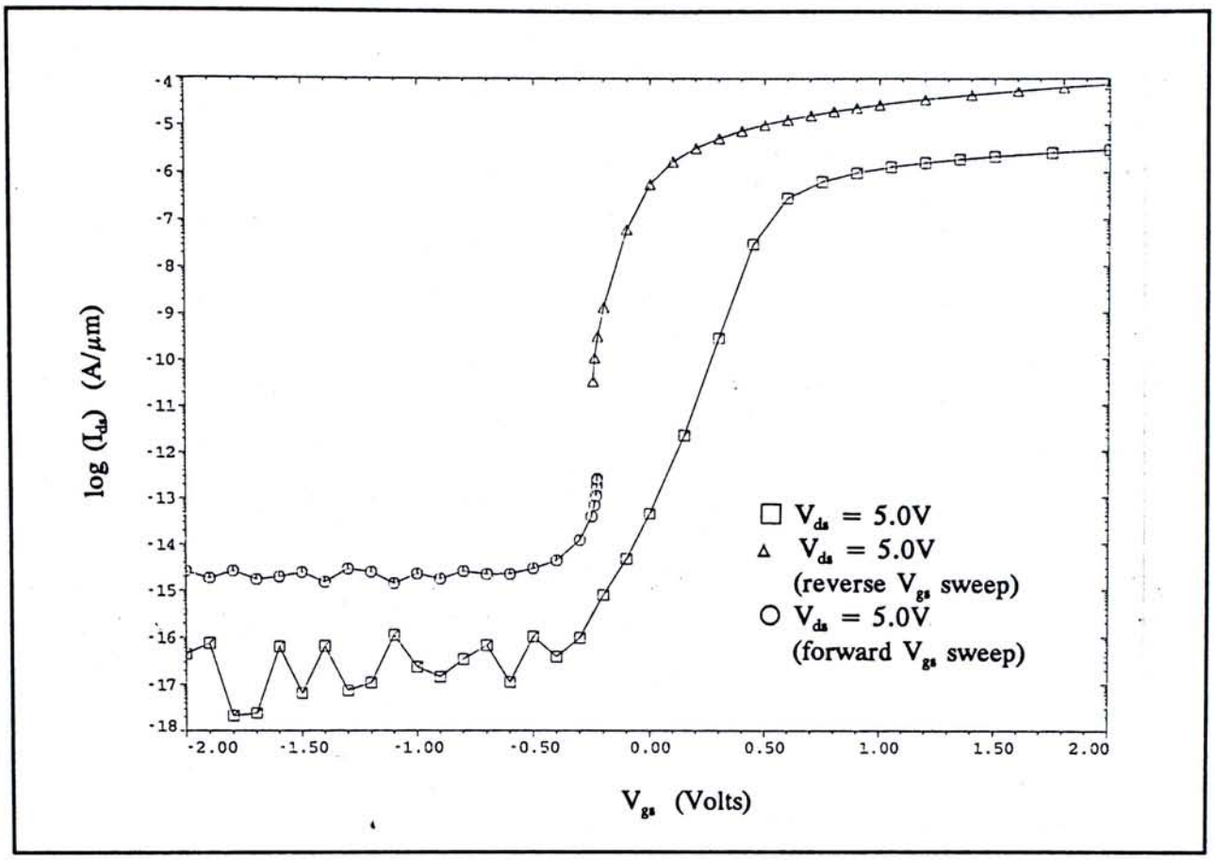


Figure 5.25 The simulated subthreshold swing characteristics for Structure C.

Despite of the disruption in subthreshold swing, in order to have a comparison among the structures, the current and voltage values at the break points are employed for the calculation of St. For subthreshold characteristics comparisons, the values of S_t and leakage current at subthreshold region of all the structures are derived and tabulated in Table 5.2 for comparison.

It is observed from Figures 5.26 and 5.27 that, the subthreshold swing characteristic for Structure D and E are very similar to Structure A. Nevertheless, there are some improvement in subthreshold leakage current as referred to Table 5.2(b). The reduction in subthreshold leakage current is attributed to the existence of insulator underneath the junctions, thereby effectively blocking most of the minority carriers migration.

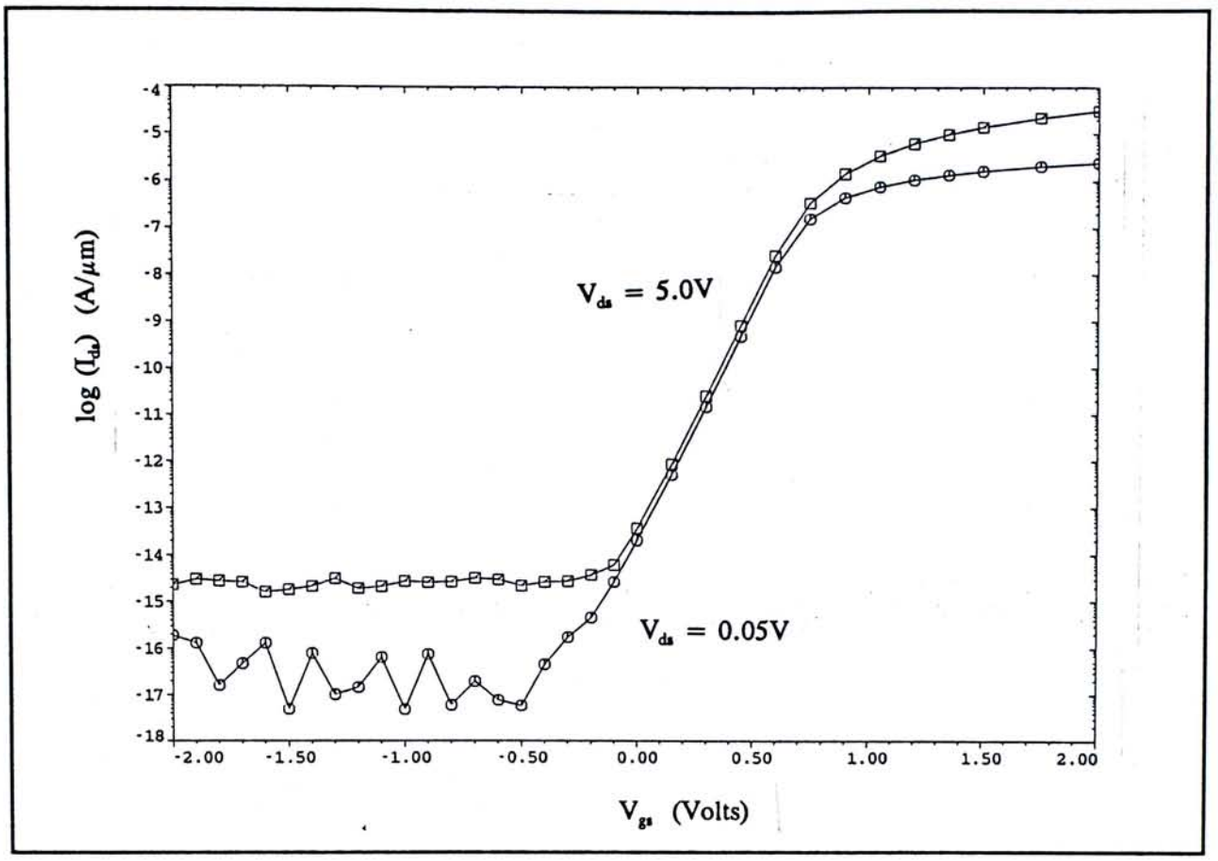


Figure 5.26 The simulated subthreshold swing characteristics for Structure D.

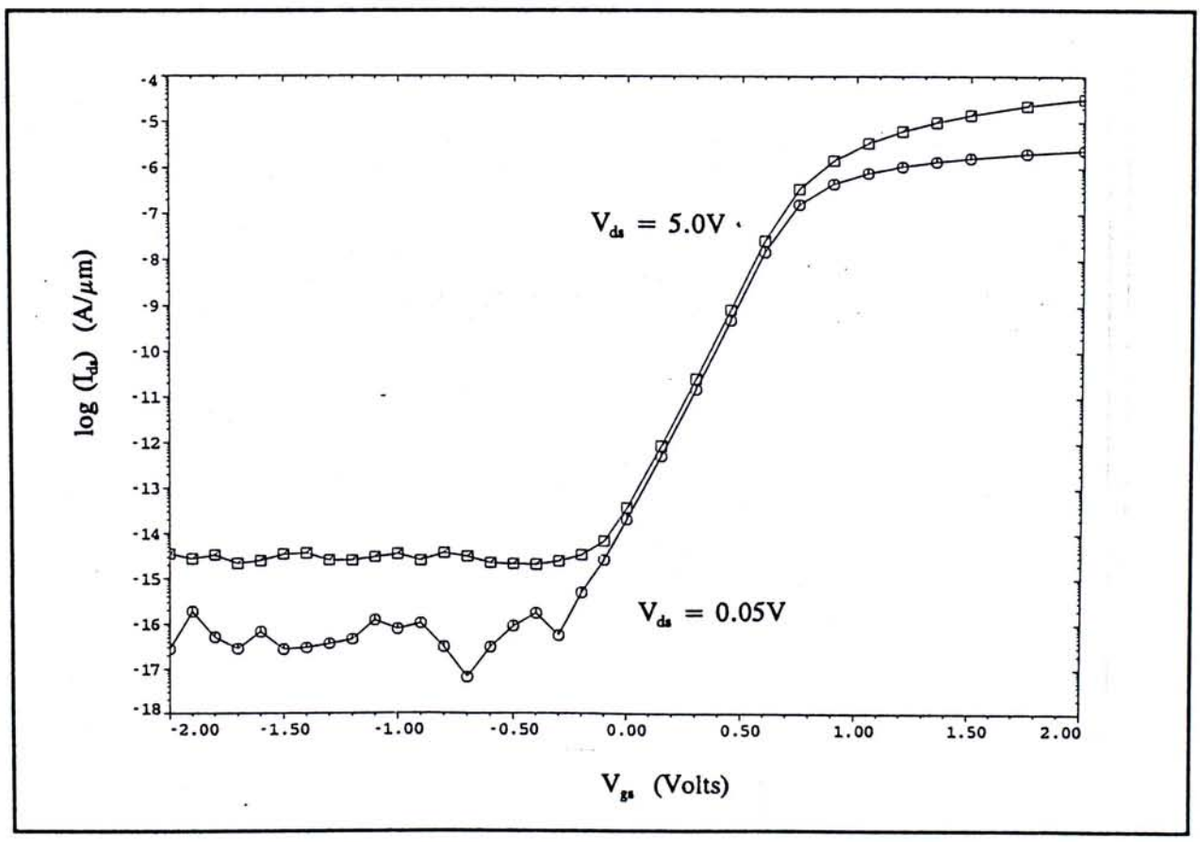


Figure 5.27 The simulated subthreshold swing characteristics for Structure E.

Due to the front gate and back gate depletion region coupling, the expression of S_t for conventional FDSOI structure is a three-capacitor network, which is more complicated then the two-capacitor based expression as in bulk structure (Figure 5.28). If one considers $C_{ox} << C_{ox1}$ and $C_{ox2} << C_{si}$, then the complicated expression can be simplified to become $S_t \approx (kT/q)(\ln 10)$. This indicates that the theoretical minimum of 60mV/decade at room temperature.

Table 5.2 (a) : Derived S_t values in unit of mV/decade of the Structures.

	Structure A	Structure B	Structure C	Structure D	Structure E
@V_{ds} = 0.05V	102.6	67.9	71.2	102.6	102.7
@V_{ds}= 5.0V	102.7	13.7	16.3	102.4	102.4

Table 5.2 (b) : Derived subthreshold leakage current in unit of A/μm of the Structures.

	Structure A	Structure B	Structure C	Structure D	Structure E
@V_{ds} = 0.05V	1.2E-16	4.9E-17	3.6E-17	6.3E-17	6.4E-17
@V_{ds}= 5.0V	6.4E-15	2.1E-15	2.2E-15	2.4E-15	3.0E-15

Referring to Figure 5.24 and 5.25, at low V_{ds} value (0.05V), a sharper slope are observed for both Structure B and C as compared to Structure A. According to Table 5.2(a), the S_t values derived are 67.9mV/decade and 71.2mV/decade for Structure B and C respectively. The values are larger than the theoretical limit because of the finite value of C_{ox2}. In practice, the presence of traps at the Si-SiO_2 interface will further limit the S_t value. This excellent S_t value allows transistors to use lower threshold voltage value while maintaining low leakage current either. As a result, better speed performance can be obtained, even at low supply voltage.

On the other hand, due to the floating body effect, hysteresis in subthreshold swing is observed in Structure B and C when V_{ds} bias is high. At high V_{ds} (5.0V),

a disruption in the curve is observed. Sometimes, the simulation just cannot converge at such a hysteresis point. The slope appears rather vertical. In fact, referring to Table 5.2(a), the resulted S_t vales are only 13.7 mV/decade and 16.7mV/decade for Structure B and C respectively, which is significantly lower than the theoretical limit. Such a hysteresis effect is undesirable and may lead to single transistor latch phenomenon as described in Chapter 2 which may disrupt the operation of the transistor in conventional SOI devices.

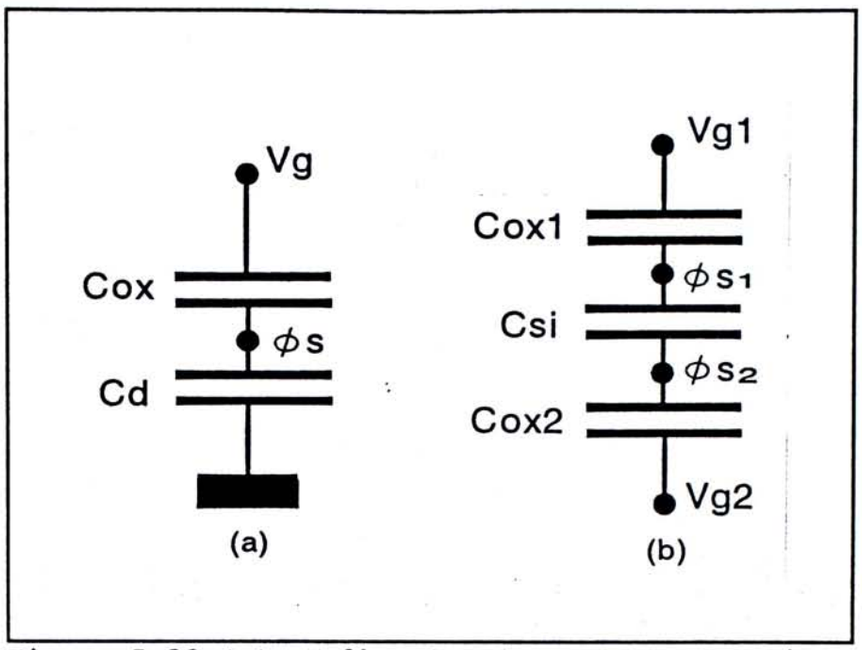


Figure 5.28 (a) Bulk structure: two-capacitor network; and (b) Conventional SOI structure : three-capacitor network.

As referred to Figure 5.26 and 5.27, the subthreshold swing characteristics for Structure D and E are well behaved for both the V_{ds} bias. Similar S_t values as if for Structure A are recorded. This confirms that the structures have similar performance as if in bulk silicon structure and the undesirable floating body effect exist in conventional FDSOI structures are effectively eliminated. It is interesting to note that the leakage current at subthreshold region is lower than those in bulk structure, though it is not as good as those in conventional SOI structure.

In short, the hysteresis effect is effectively avoided in the BCSOI structure and the S_t values are essentially identical to bulk devices. Nevertheless, due to the

existence of insulator layer underneath the junction, there is some improvement in subthreshold leakage current in the BCSOI structure over the bulk substrate structure.

5.3 Dependence on Key Structure Parameters

By far, nMOS transistor built on BCSOI structures have been found to be free of undesirable floating body effect while preserving the performance equivalent to those on bulk silicon structure with slight improvement. At this stage, it is straightforward to evaluate the manufacturability of such a kind of BCSOI structure by studying the configuration margins, i.e. to study the possible performance changes against the change of key structure parameters including insulator layer thickness, body contact size variation and silicon over layer thickness. Examination of transistor performance is also made by extracting the simulation results of I-V characteristics, back body effect, subthreshold swing and transconductance of the transistors subject to different configuration parameters changes. In view that both of the BCSOI structures, i.e. Structure D and E, have very similar overall performance and that silicon-on-nitride structure is of more interest, studying on transistor performance against key parameters changes will be primarily devoted to Structure E in the subsequent sections.

5.3.1 Dependence on Insulator Thickness

The choice of insulator thickness, t_{in}, calls for a careful trade-off between substrate preparation cost and device performance in both conventional and BCSOI structures.

In conventional SOI structures, variation in t_{in} affects body effect of transistors that built on them. In general, the thicker t_{in}, the higher immunity of the transistors to back body effect. Two extreme cases shall be noted:

(a) When t_{in} equals to zero, the structure is essentially a bulk structure; and

(b) When t_{in} is very large, it becomes similar to SOS structure.

Treating t_{in} as a variable and using MEDICI, performance of a nMOS transistor on Structure E in terms of body effect, current driving, transconductance and subthreshold swing were simulated.

With reference to Figure 5.29, there is no change at threshold voltage at all

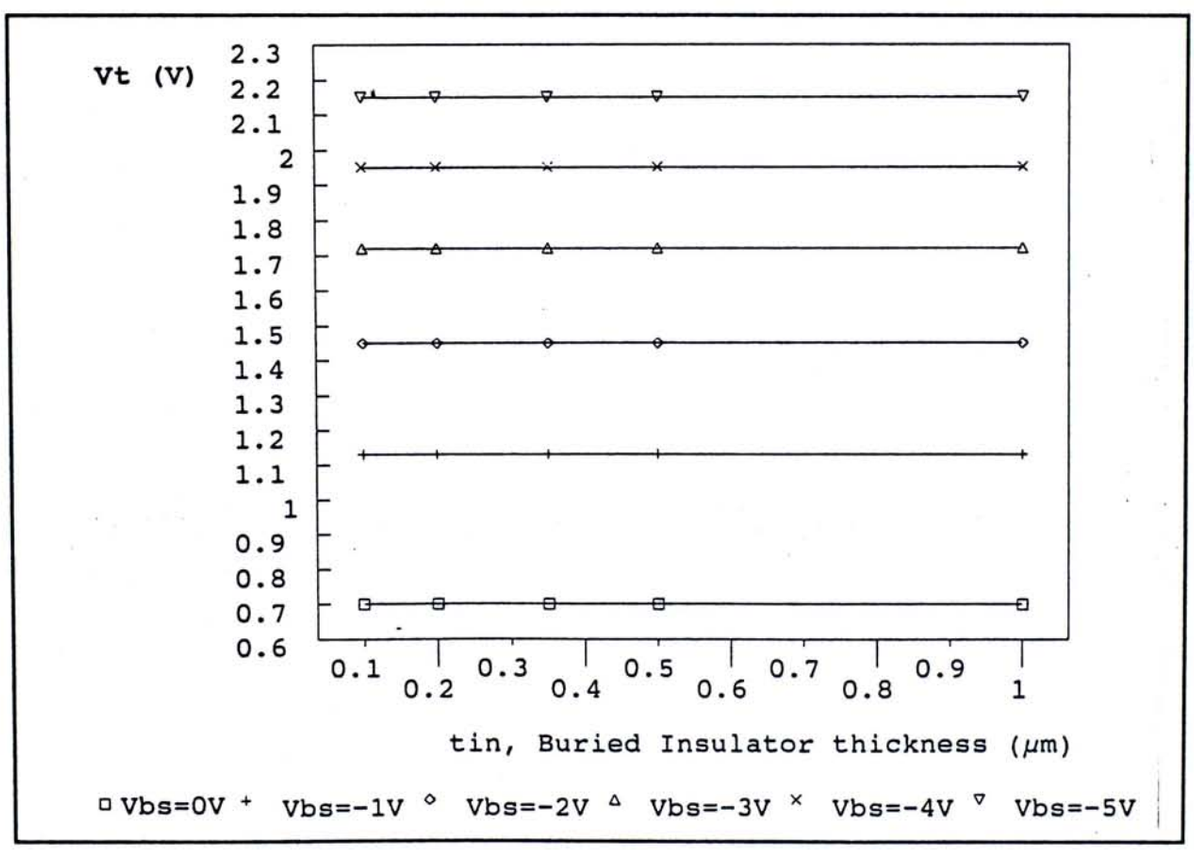


Figure 5.29 The graph of threshold voltage change against t_{in}.

substrate bias on changing t_{in}. This implies a wide process latitude as long as BCSOI structure is in concern. The I_{ds} degradation, according to Figure 5.30, is also

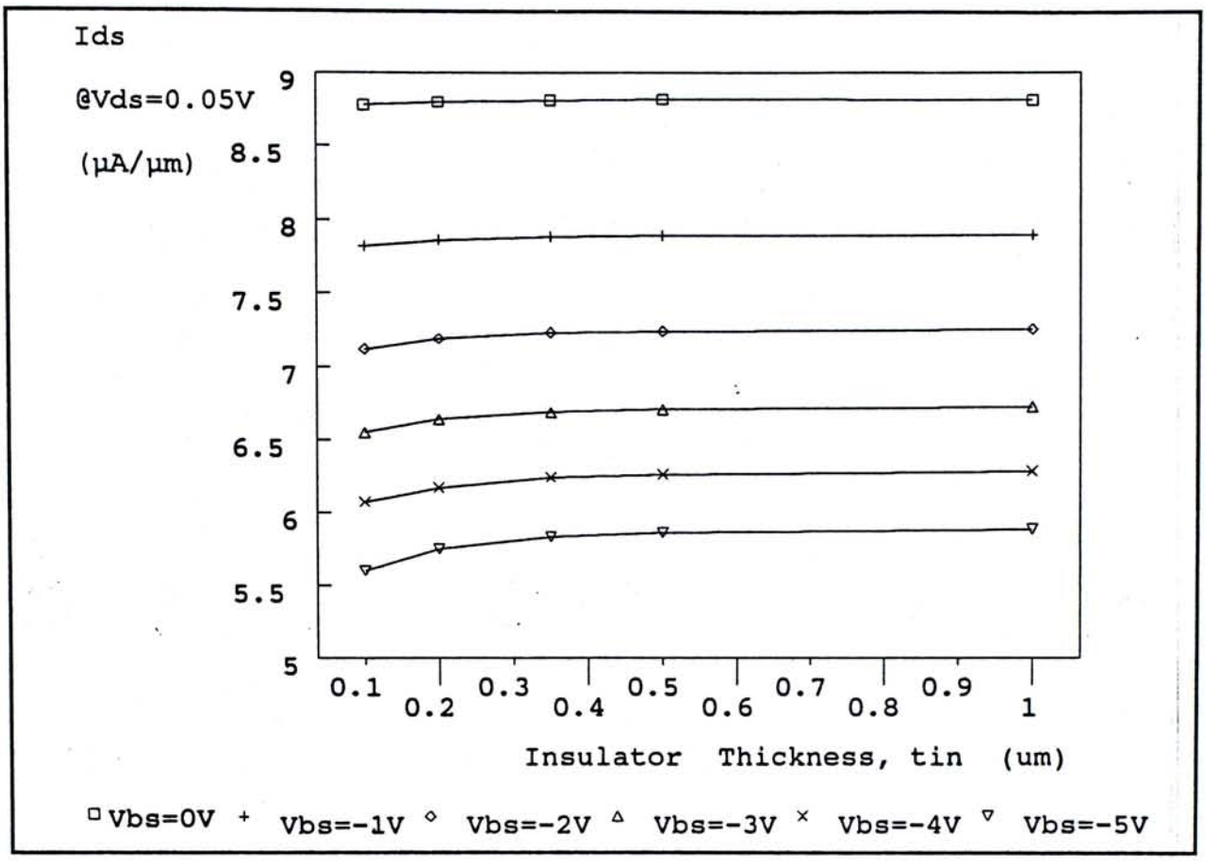


Figure 5.30 The graph of I_{ds} degradation against t_{in}.

not discernable when t_{in} is thick enough. A more severe I_{ds} degradation is recorded when t_{in} is 0.1μm. A thickness of 0.3μm or above seems to be a good choice.

Saturation current output is also found to be stable as referred to Figure 5.31. The effect of t_{in} change on g_m is also insignificant (Figure 5.32). With reference to Table 5.3, the dependence of subthreshold swing on t_{in} is also weak.

Table 5.3 (a) : Derived St values in unit of mV/decade of the Structures with varying t_{in}.

t_{in}	0.1 μm	0.2 μm	0.35 μm	0.5 μm	1.0 μm
@V_{ds} = 0.05V	102.65	102.63	102.67	102.63	102.47
@V_{ds}= 5.0V	102.55	102.49	102.39	102.41	102.40

Table 5.3 (b) : Derived subthreshold leakage current in unit of A/μm of the Structures with varying t_{in}.

t_{in}	0.1 μm	0.2 μm	0.35 μm	0.5 μm	1.0 μm
@V_{ds} = 0.05V	8.3E-17	6.4E-17	6.4E-17	5.9E-17	5.4E-17
@V_{ds}= 5.0V	3.4E-15	3.1E-15	3.0E-15	2.7E-15	2.7E-15

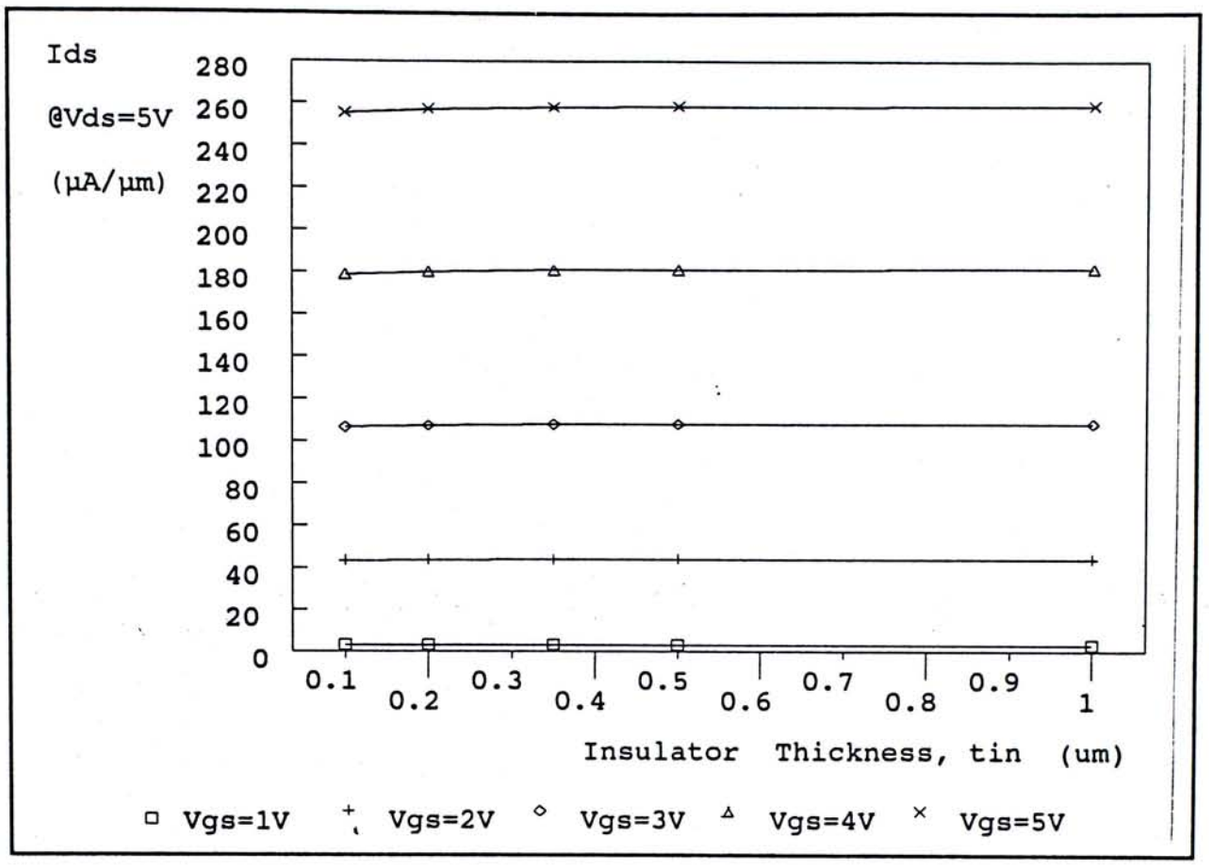


Figure 5.31 The graph of saturation I_{ds} against substrates with varying t_{in}.

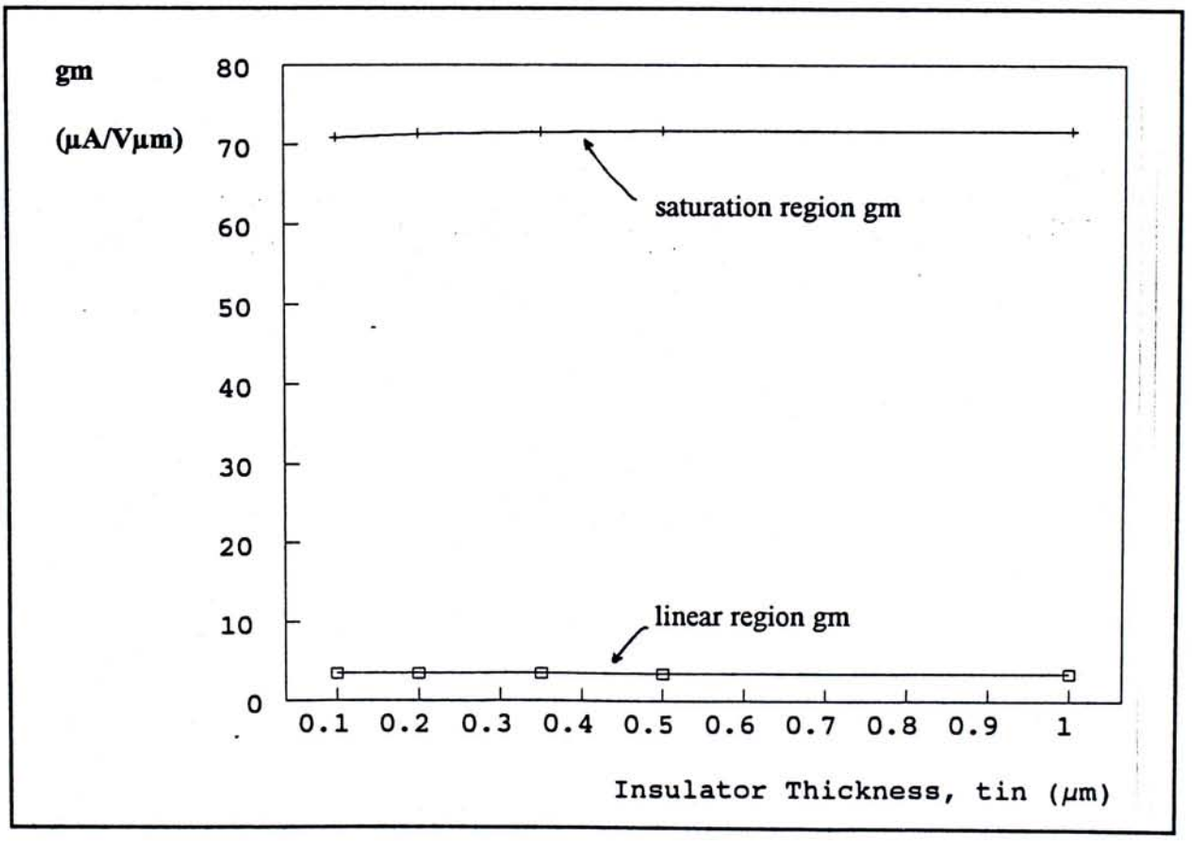


Figure 5.32 The graph of g_m against substrates of varying t_{in}.

An almost 30% increase in subthreshold leakage current is recorded when t_{in} changes from 0.2μm to 0.1μm, indicating substrate with thin t_{in} is not desirable.

In brief, if $t_{in} \geq 0.3\mu m$, transistor performance is stable and it provides wide latitude on processing and performance.

5.3.2 Dependence on Silicon Overlayer Thickness

For FDSOI devices built on conventional SOI structure, variation in silicon overlayer thickness, t_{si}, causes fluctuation on transistor threshold voltage. This is a potential yield limiting factor if t_{si} variation become out of control.

Referring to Figure 5.33, it is seen that the threshold voltage of nMOS transistor does not changes with change to silicon overlayer thickness. This implies

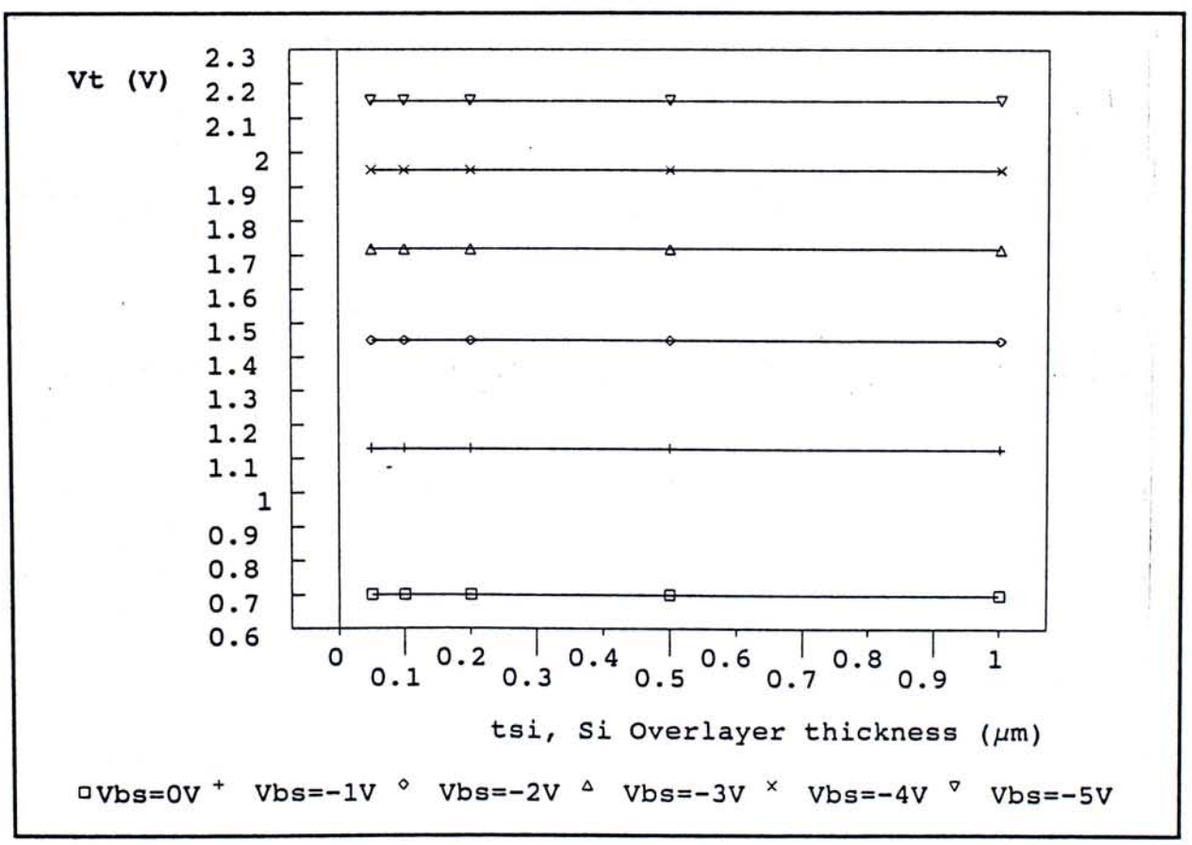


Figure 5.33 The graph of Vt changes on back bias of substrate with varying t_{si}.

that the threshold voltage of transistor on BCSOI structure have wide latitude against

t_{si} changes. On the other hand, at low V_{ds} (0.05V), the current output at V_{gs}=5.0V appears to become elevated with a thinner t_{si} overlayer as shown in Figure 5.34. In terms of transconductance and current output level, it can be

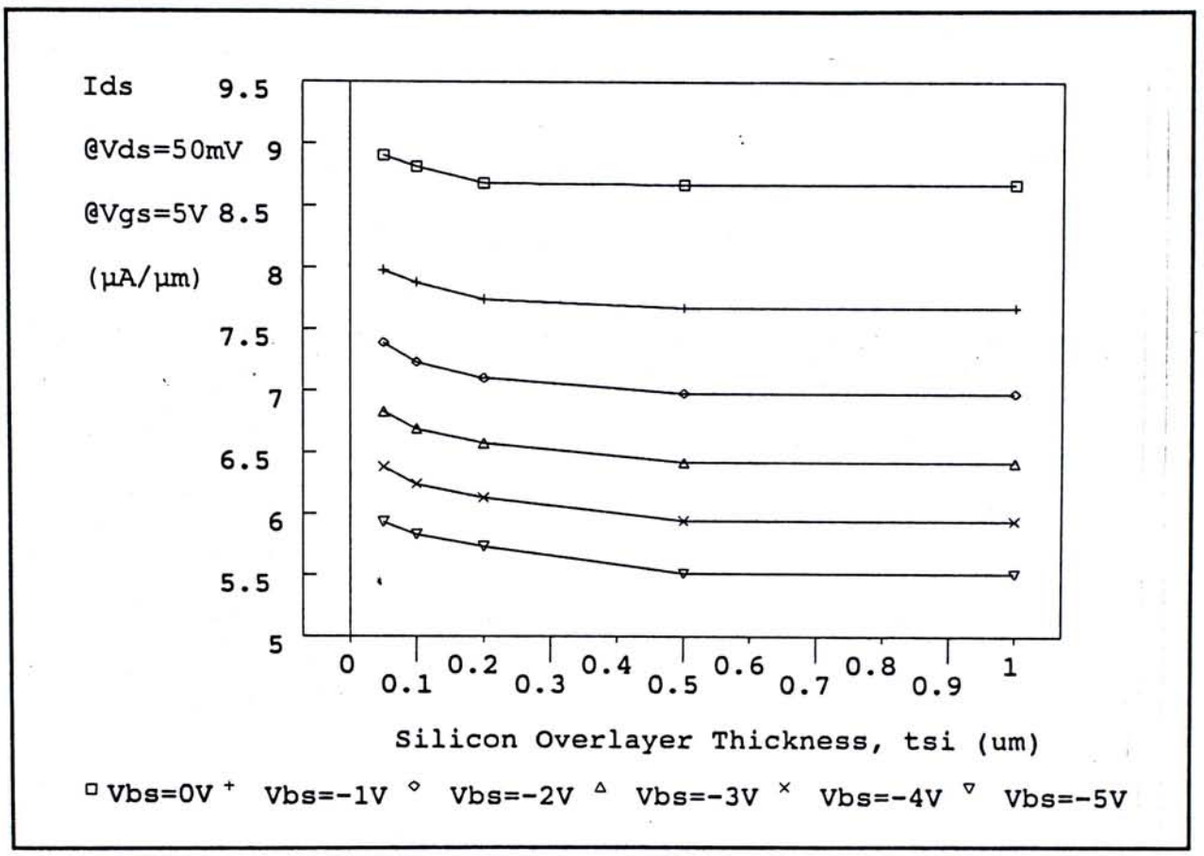


Figure 5.34 The graph of I_{ds} degradation against substrate of varying t_{si}.

observed in Figure 5.35 and 5.36 that there are hardly any discernable difference despite of a very small increment in t_{si}=0.05μm.

Table 5.4 (a) : Derived St values in unit of mV/decade of the Structures with varying t_{si}.

t_{si}	0.05 μm	0.1 μm	0.2 μm	0.5 μm	1.0 μm
@V_{ds} = 0.05V	102.65	102.67	102.69	102.61	102.69
@V_{ds}= 5.0V	102.55	102.39	102.57	102.69	102.72

Table 5.4 (b) : Derived subthreshold leakage current in unit of A/μm of the Structures with varying t_{si}.

t_{si}	0.05 μm	0.1 μm	0.2 μm	0.5 μm	1.0 μm
@V_{ds} = 0.05V	3.5E-17	6.4E-17	1.2E-16	1.2E-16	1.4E-16
@V_{ds}= 5.0V	2.5E-15	3.0E-15	4.5E-15	6.6E-15	6.4E-15

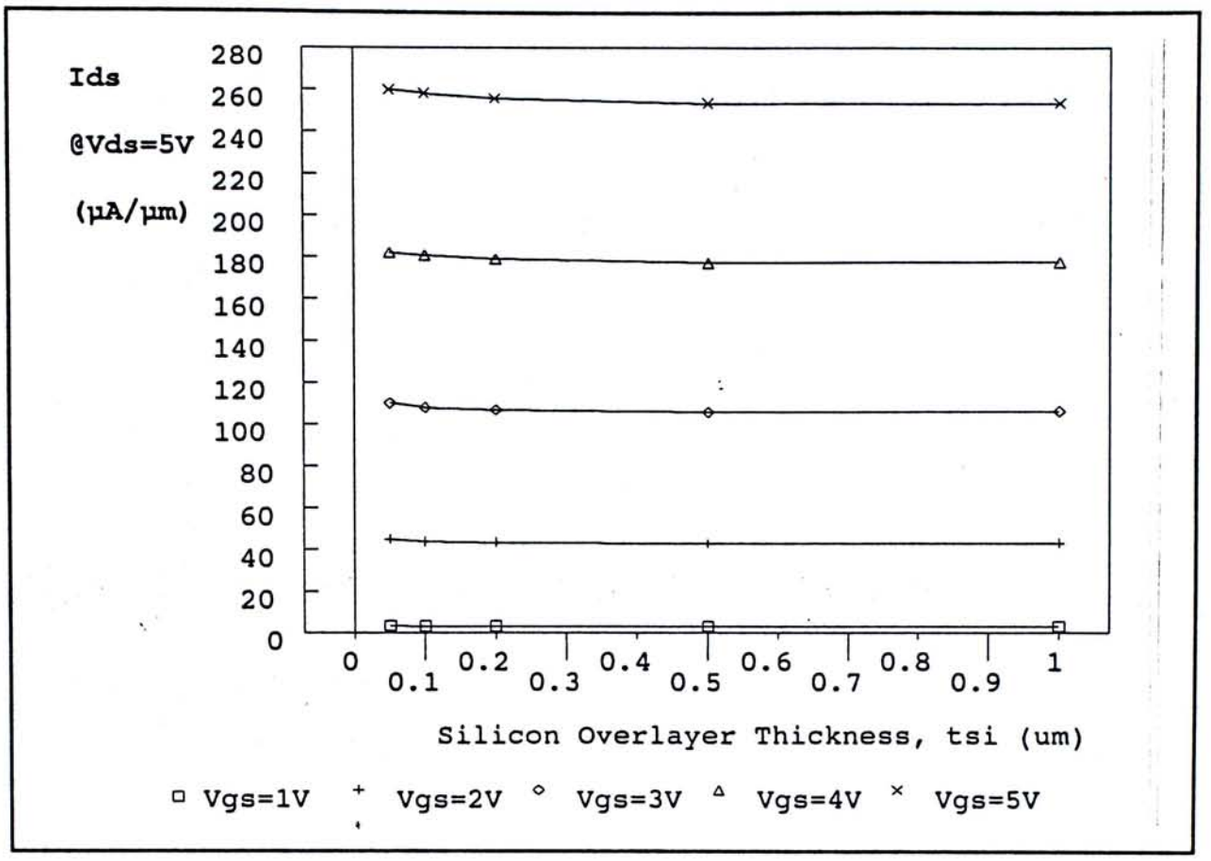


Figure 5.35 Saturation current I_{ds} against substrate with varying t_{si}.

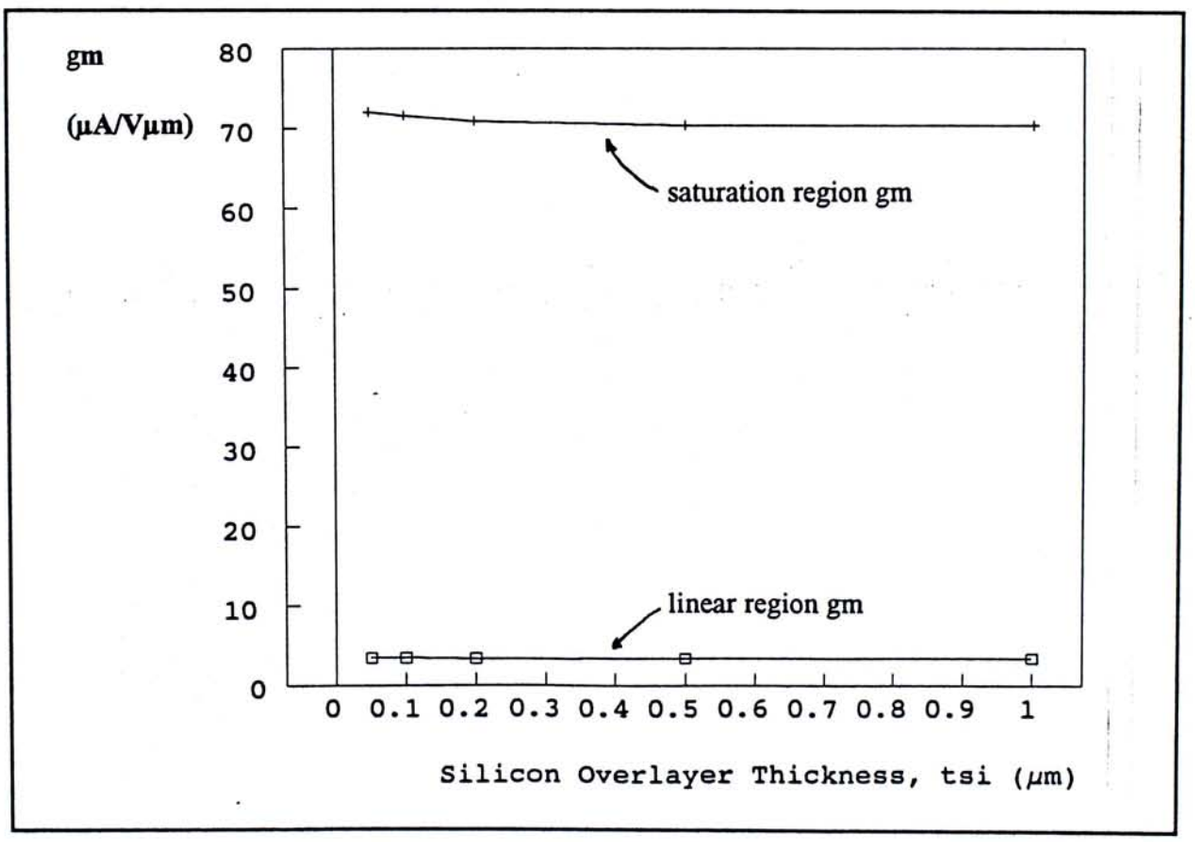


Figure 5.36 The graph of g_m against substrate with varying t_{si}.

According to Table 5.4, variation in t_{si} has no effect on transistor swing. However, the simulated subthreshold leakage current are found to be improved when t_{si} is smaller. A smaller p-n junction surface as t_{si} become smaller is believed to be contributing to the improvement.

5.3.3 Dependence on Size of Body-Contact

The size of buried contact t_{bc} of a BCSOI structure has ample effects on the performance of devices built on it. If we consider $t_{bc}=0$, then the structure is equivalent to a conventional SOI structure. Devices built on it behave essentially those of conventional SOI devices. On the contrary, if t_{bc} is large, devices basically transform back to those on bulk silicon substrate.

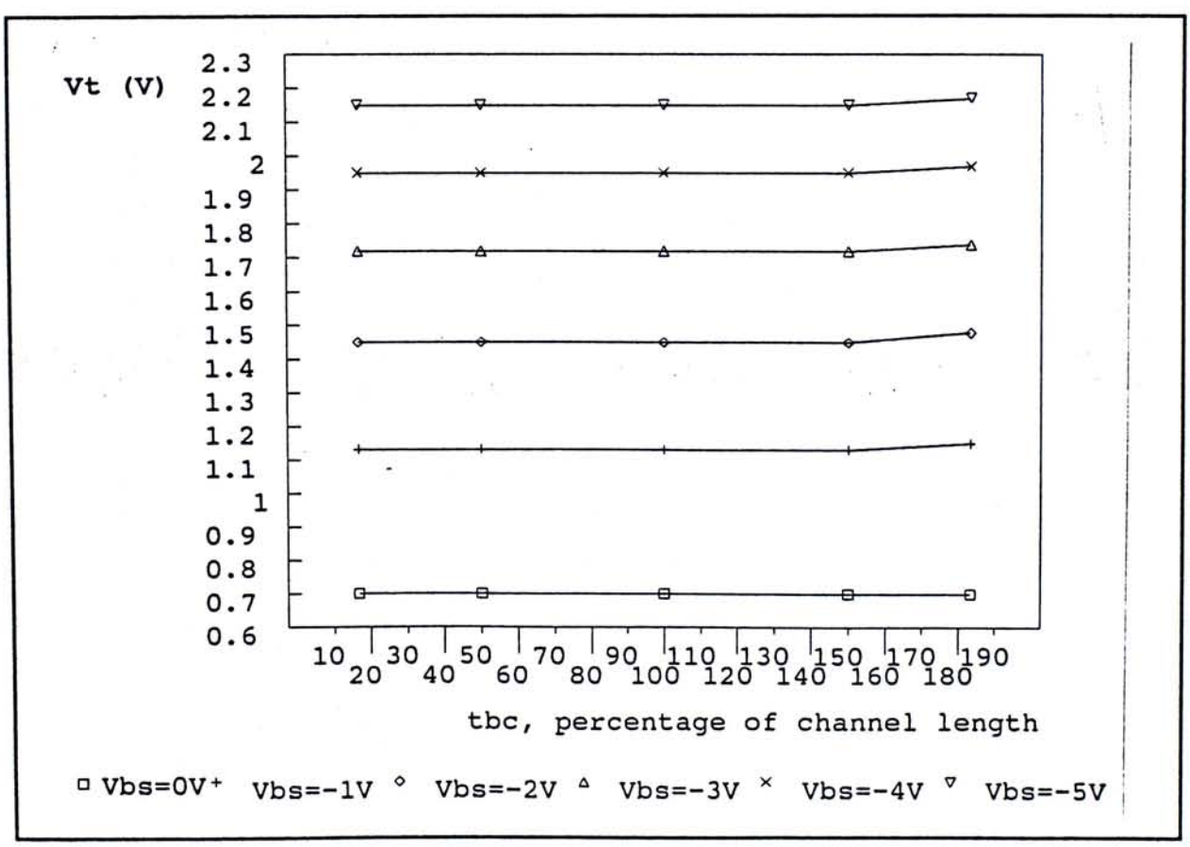


Figure 5.37 The graph of threshold voltage changes against substrate of varying t_{bc}.

From the manufacturing point of view, variation in t_{bc} is indispensable. It is therefore important to investigate such an effect made on device performance.

According to Figure 5.37, threshold voltage fluctuation is small when t_{bc} is large; however, it drops as t_{bc} become small. As a result of threshold voltage decreases at small t_{bc}, the saturation current I_{ds} output at lower Vds (50mV) and at Vgs=5.0V is elevated as shown in Figure 5.38.

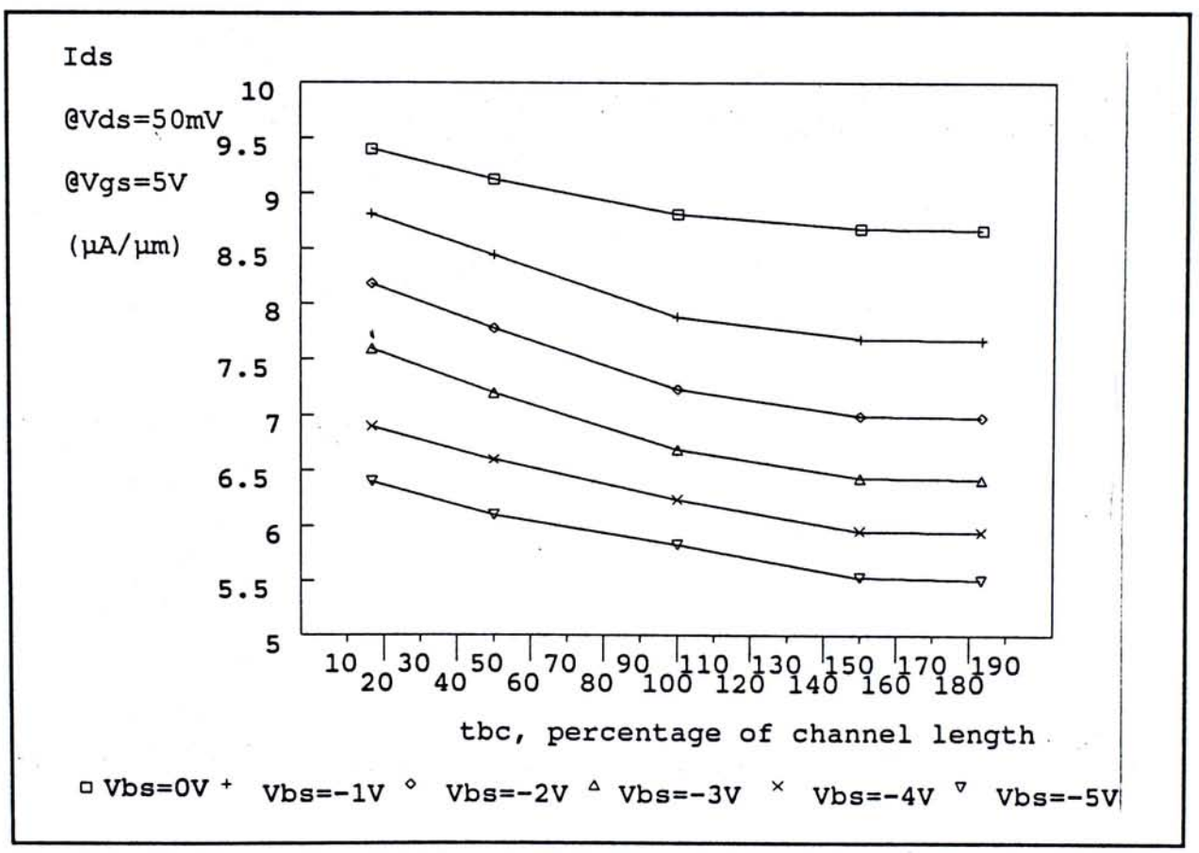


Figure 5.38 I_{ds} degradation at low Vds (50mV) against substrate of varying t_{bc}.

Such a phenomena is also confirmed by the increase of Ids at Vds=5V as well as g_m for all gate voltage bias, as referred to Figure 5.39 and 5.40.

Moveover, referring to Table 5.5, swing and leakage current are reduced with reduced t_{bc}. Although a reduced t_{bc} appears to be attractive in the overall device performance, it is repeatedly stressed that too small t_{bc} will prone to floating body

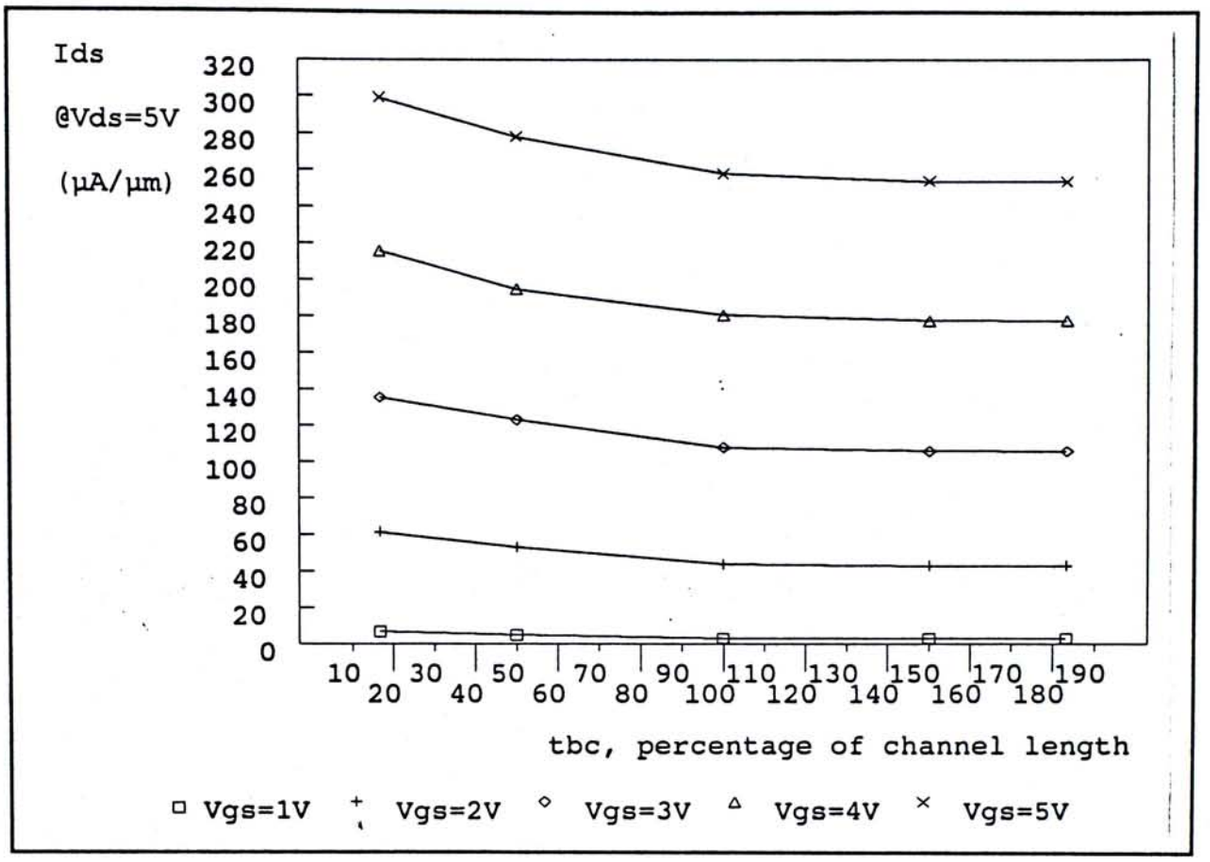


Figure 5.39 Saturation current I_{ds} output against substrate of varying t_{bc}.

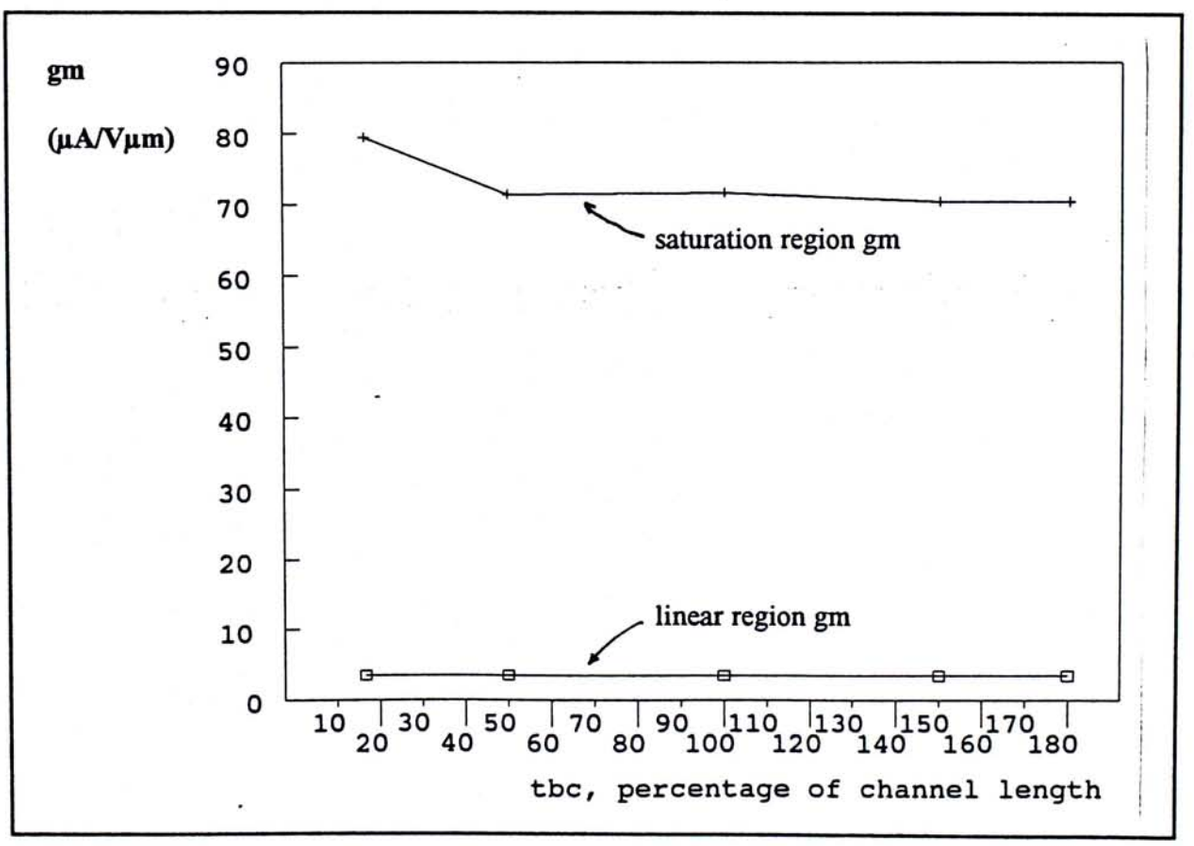


Figure 5.40 The graph of g_m against substrate of varying t_{bc}.

effect. For stable device performance while compromising ease of manufacturing, t_{bc} shall be chosen as the same size of gate length.

Table 5.5 (a) : Derived St values in unit of mV/decade of the Structures with varying t_{bc}.

t_{bc}(% of gate length)	16.7	50	100	150	183
@V_{ds} = 0.05V	89.92	100.62	102.67	102.69	102.61
@V_{ds}= 5.0V	90.13	100.35	102.39	102.69	102.72

Table 5.5 (b) : Derived subthreshold leakage current in unit of A/μm of the Structures with varying t_{bc}.

t_{bc}(% of gate length)	0.05 μm	0.1 μm	0.2 μm	0.5 μm	1.0 μm
@V_{ds} = 0.05V	5.7E-17	4.1E-17	6.4E-16	1.2E-16	1.2E-16
@V_{ds}= 5.0V	2.2E-15	2.3E-15	3.0E-15	6.6E-15	6.4E-15

5.4 Summary

The BCSOI SOI structure is verified to be capable of immune to undesirable floating body effect which exists in conventional SOI structures. Performance of nMOS transistor built on BCSOI structure, although not as good as in conventional SOI structure, is found to have advantages over those in bulk silicon structure. The improved performance of devices on BCSOI structure is also found to have wide latitude against structure parameters variation of t_{si}, t_{bc} and t_{in} upon structure manufacturing. Those advantages allow the fabrication of FDSOI devices built on silicon-on-nitride BCSOI structure by implantation based method easier.

Chapter 6 Latch-up Susceptibility Study of BCSOI Structure

6.1 Introduction

Although the significantly lower power consumption and the ease of scaling features have enabled CMOS circuits become the overwhelming majority in VLSI and even ULSI applications, susceptibility to latch-up is still a major problem of them especially when they are closely placed on bulk silicon substrate. On the contrary, because there is no path connecting the n- and p-MOS transistors, devices built on conventional SOI structure are inherently immune to latch-up.

The simulation results in Chapter 5 clearly indicate that undesirable floating body effects are effectively suppressed by employing the Body-Contact SOI (BCSOI) structure in an nMOS transistor. The lower impact ionization rate in pMOS transistors excludes their need to employ the BCSOI structure. Without any opening under the channel region of p-channel transistors, there are still no path connecting both types of transistors in CMOS circuits, thereby preserving the latch-up immunity advantages as if in conventional SOI structure. Such an idea has been demonstrated successfully already (Patel et. al., 1990 and 1991).

Nevertheless, to realize FDSOI circuits on SIMNI wafers, the channel regions of both n-channel and p-channel transistors are needed to be protected from nitride implantation so that direct gate oxidation is easier. The straight-forward way is to employ the BCSOI structure in both type of the transistors. By opening up a contact in the buried nitride layer, not only a well is needed to be formed, CMOS

circuits will also become susceptible to latch-up.

In this chapter, the latch-up susceptibility of an CMOS inverter built on SIMNI substrate with BCSOI structure in both types of transistors is studied. By using MEDICI, latch-up susceptibility dependence on structure configuration such as buried insulator thickness, well depth, separation of the transistors, body contact sizes are simulated.

6.2 Construction of a p-channel MOS Transistor

To realize CMOS operation on BCSOI silicon-on-nitride structure, in addition to the nMOS transistor structure built on Structure E as constructed in previous chapter, a pMOS transistor is also required.

When utilizing computer simulation, such a pMOS transistor construction is basically straight-forward. Based on the source file for Structure E, to construct an equivalent pMOS transistor, several changes on command lines are needed:

a) change the p-type substrate to n-type substrate;

b) change the source and drain dopant type from n-type to p-type;

c) change the "SOLVE" content to find solution of HOLES, instead of ELECTRONS in nMOS transistor simulation;

d) adjust the substrate and channel concentration so that the threshold voltage can be trimmed to usable range; and

e) change the bias conditions to account for pMOS transistor simulation.

Apart from the above changes, the source file of a BCSOI silicon-on-nitride pMOS transistor is basically identical to the nMOS transistor on Structure E as used previously. In other words, structure parameters such as gate oxide thickness,

channel length, buried nitride thickness, silicon overlayer thickness etc of the pMOS transistor are the same as those for nMOS transistor.

The altered source file for pMOS transistor is then fed into the computer to obtain the transistor performance of a pMOS transistor. Alike the case with nMOS transistor, performance of the pMOS transistor is evaluated by means of studying its body effect, I-V characteristics, transconductance and subthreshold swing.

6.2.1 Threshold Voltage and Body Effect

Shown in Figure 6.1 is the graph of I_{ds} versus V_{gs} at low V_{ds} (-0.05V) at various V_{bs} values. The threshold voltage at zero back bias, Vtp0, of the pMOS transistor is extracted to be -0.7V. Such a threshold voltage is of similar magnitude to that of nMOS transistor on Structure E. According to Figure 6.1, it is observed that threshold voltage of the transistor increases with increasing back bias. As a result of the threshold voltage increment, degradation of I_{ds} value at V_{gs}=5V of various Vbs is explicitly seen. Similar to the calculation of the body factor for nMOS transistor as presented in Chapter 5, the body factor of the pMOS transistor is estimated to be $0.4V^{½}$.

6.2.2 I-V Characteristics

As shown in Figure 6.2, long channel behaviour is observed in the pMOS transistor. No sight of floating body effect, which may exist in conventional SOI structure, is perceived from the well-behaved I-V curves. The current driving capability is about half of those of nMOS transistor at the respective V_{gs}, indicating the pMOS is of equivalent performance and can be operated at 5V supply voltage.

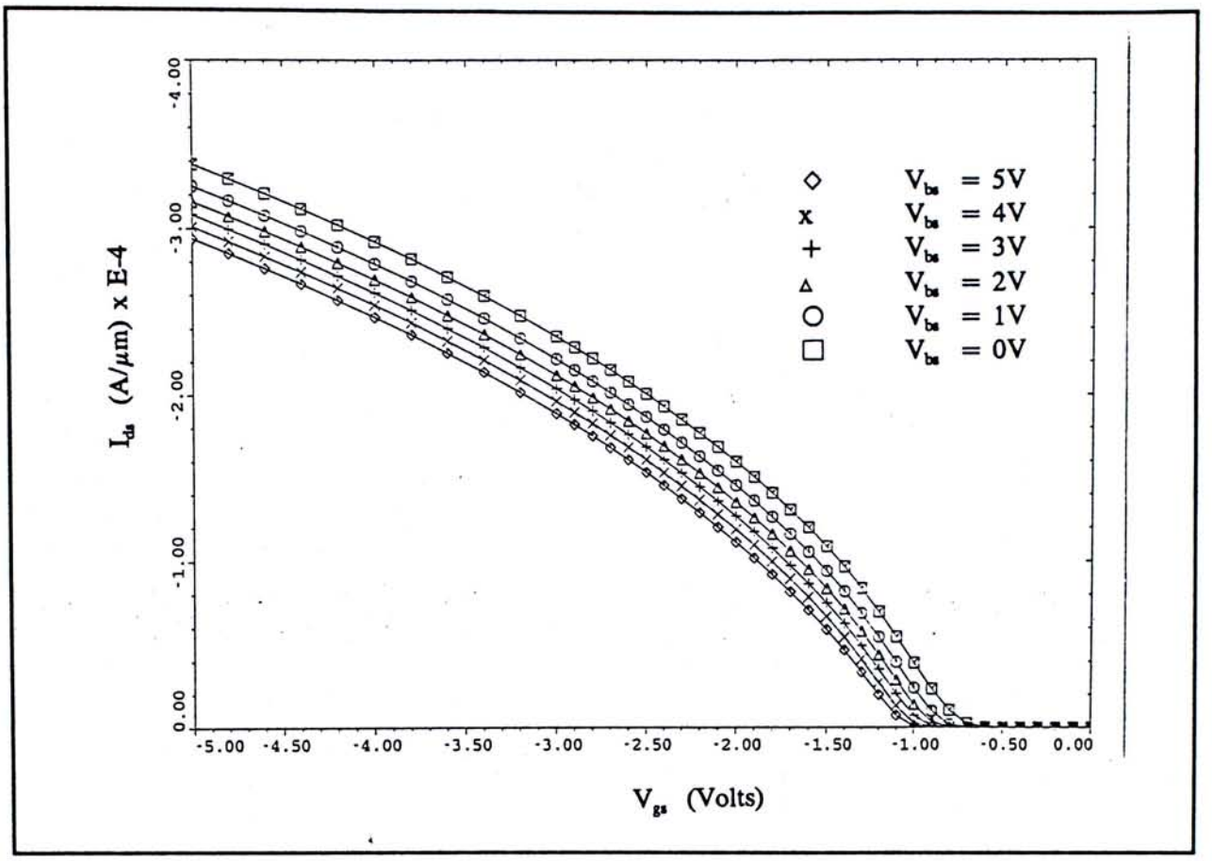


Figure 6.1 Simulated body factor graph of a pMOS on BCSOI SIMNI structure

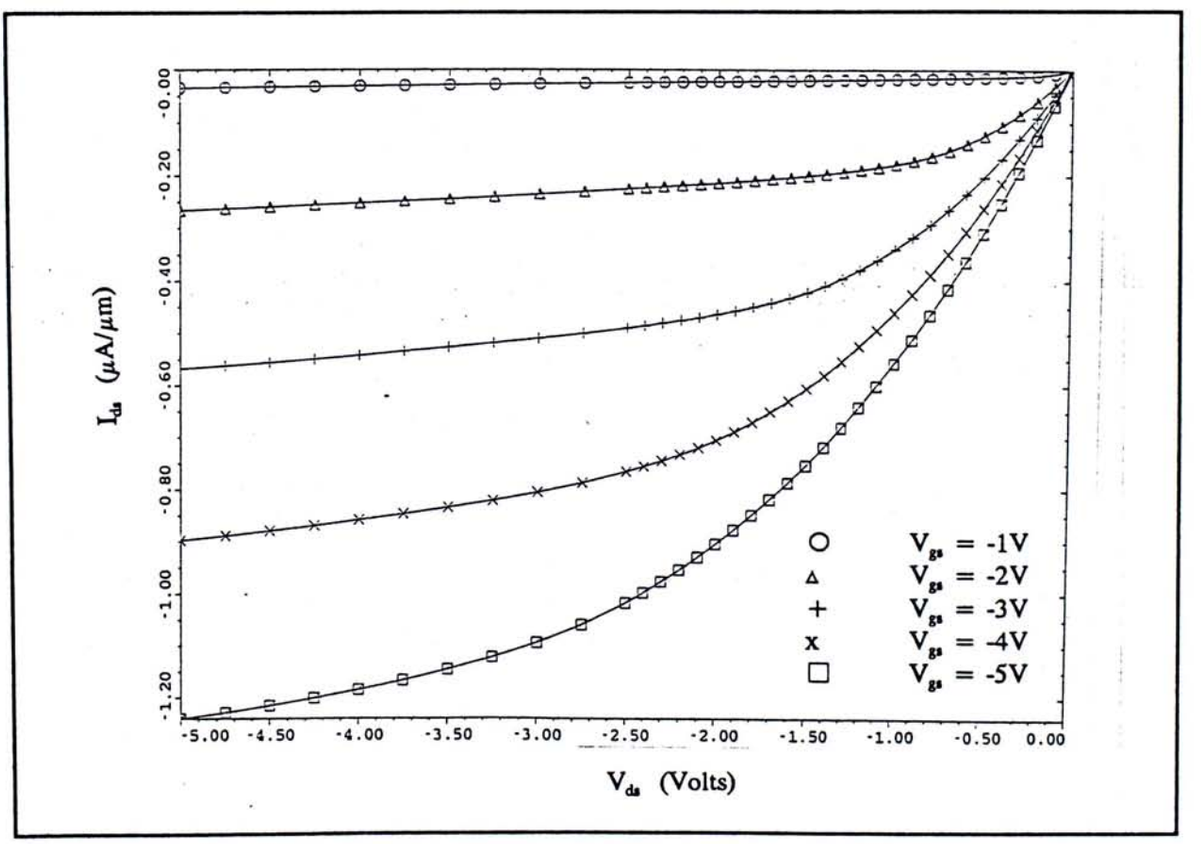


Figure 6.2 Simulated I-V curves of a pMOS on BCSOI SIMNI structure.

6.2.3 Transconductance

Transconductance g_m of the pMOS transistor are extracted from the linear region of the I-V characteristics. The results are plotted in Figure 6.3. The values of g_m are found to be increasing with drain bias as if in nMOS transistor. Yet, it is clear that g_m is less then those in nMOS transistor for all V_{gs} bias.

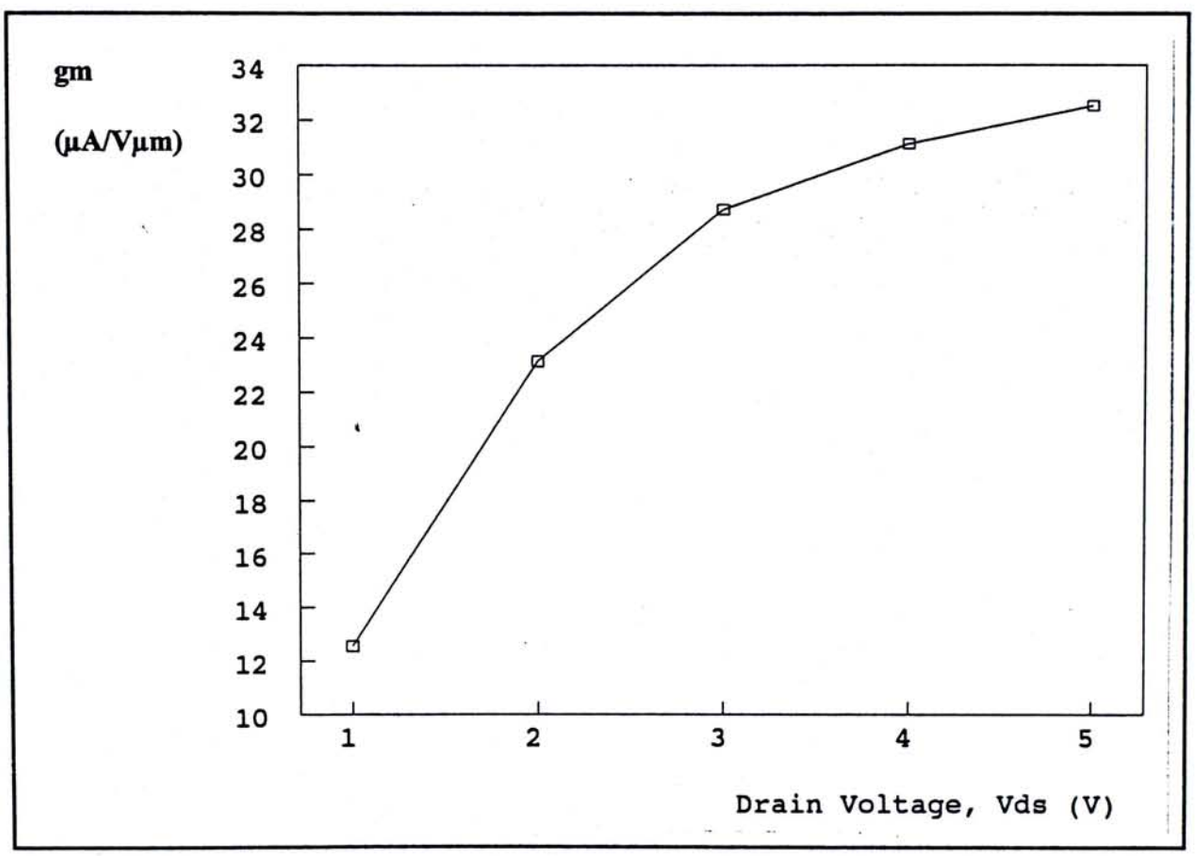


Figure 6.3 Extracted g_m of the pMOS under simulation.

6.2.4 Subthreshold Swing

Shown in Figure 6.4 is the subthreshold swing characteristics of the pMOS transistor. A well behaved subthreshold swing is observed. Again, the value of subthreshold swing St is extracted as the inverse of the slope of the "linear" region on the swing characteristics. The results are:

St = 92.68 mV/decade for V_{ds} = -0.05V; and

St = 102.37 mV/decade for V_{ds} = -5.0V.

Also, the leakage current at subthreshold region are deduced and they are:

$I_{leakage}$ = 1.91 E -16 A/μm for V_{ds} = -0.05V; and

$I_{leakage}$ = 1.13 E -14 A/μm for V_{ds} = -5.0V.

Based on the overall performance simulation results, the pMOS transistor under simulation is found to be well behaved. Such a pMOS transistor will then be employed to form an inverter with the nMOS transistor on BCSOI SIMNI structure for latch-up susceptibility studying.

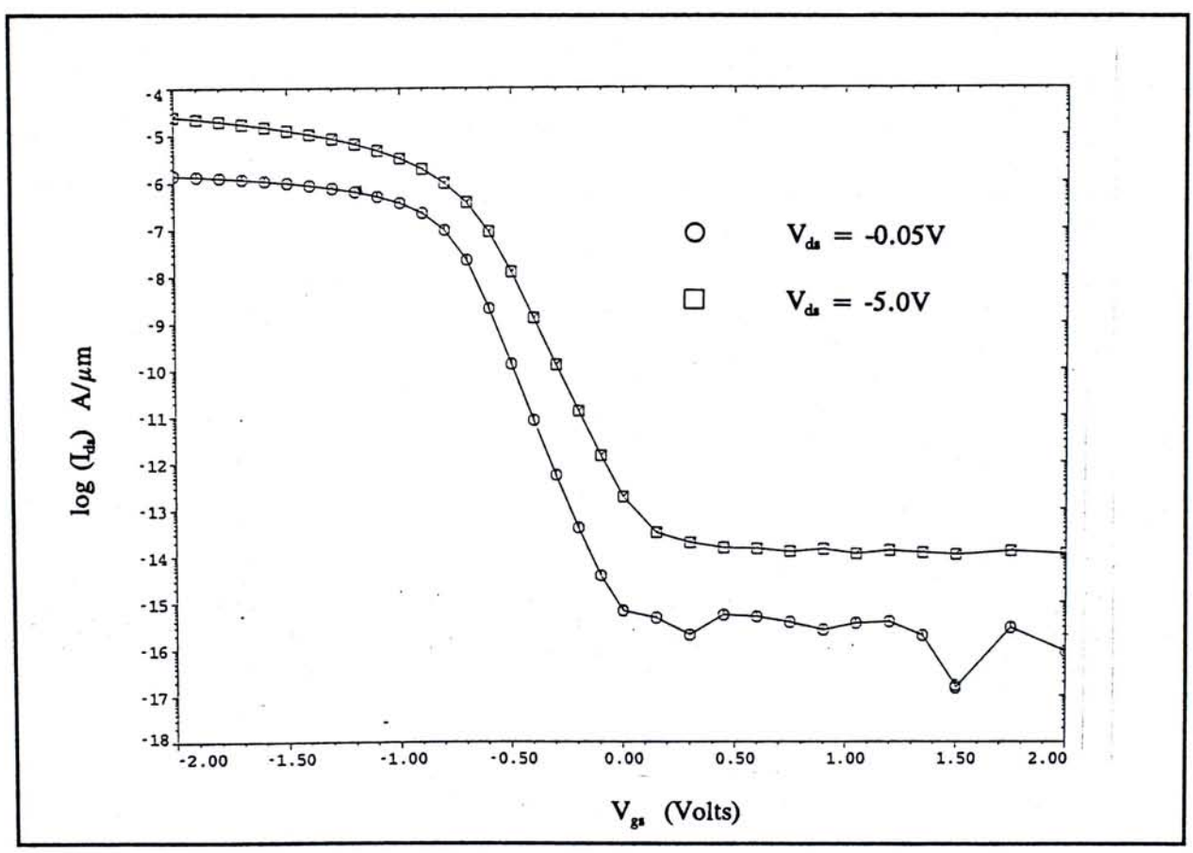


Figure 6.4 Subthreshold swing characteristics of the pMOS under simulation.

6.3 Mechanisms of Latch-up in CMOS

In fine geometry bulk silicon CMOS circuits, one of the major problems is device latch-up, an internal feedback mechanism that incurs temporary or permanent

loss of circuit function.

When a p-channel and a n-channel transistors are placed on the same bulk silicon substrate to form CMOS circuits, such as the simple inverter structure as shown in Figure 6.5, the p-tub and n-tub concentration profiles, the separation between n+ and p+ regions have to be carefully considered.

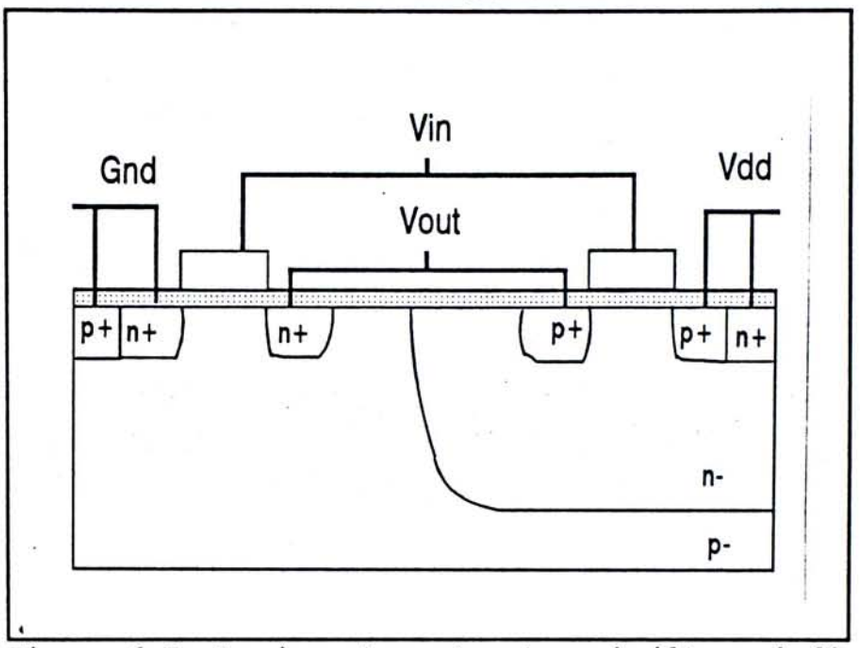


Figure 6.5 An inverter structure built on bulk silicon substrate.

In fact, inherent to such a structure, the p+ source, n-tub (or n-well) and p-sub form a vertical pnp bipolar transistor; whereas the n+ source, p-tub and n-well construct a lateral npn bipolar transistor. Such a configuration constitutes a pnpn thyristor structure (Figure 6.6), in which the device can operate in high impedance state to block conduction or low impedance state to carry a large current flow.

Figure 6.7 shows the characteristics of a pnpn thyristor. In the regions **a to b**, the structure is in forward blocking or OFF state with very high impedance. Forward breakover occurs when dV/dI =0. At this particular moment, the device is said to be switched on. The switching voltage, V_{sw}, and switching current, I_{sw}, are defined to be the voltage and current at this point. They represent the conditions

when the thyristor structure is switched on. Large values of V_{sw} and I_{sw} mean that the inverter is more resistant to switching on.

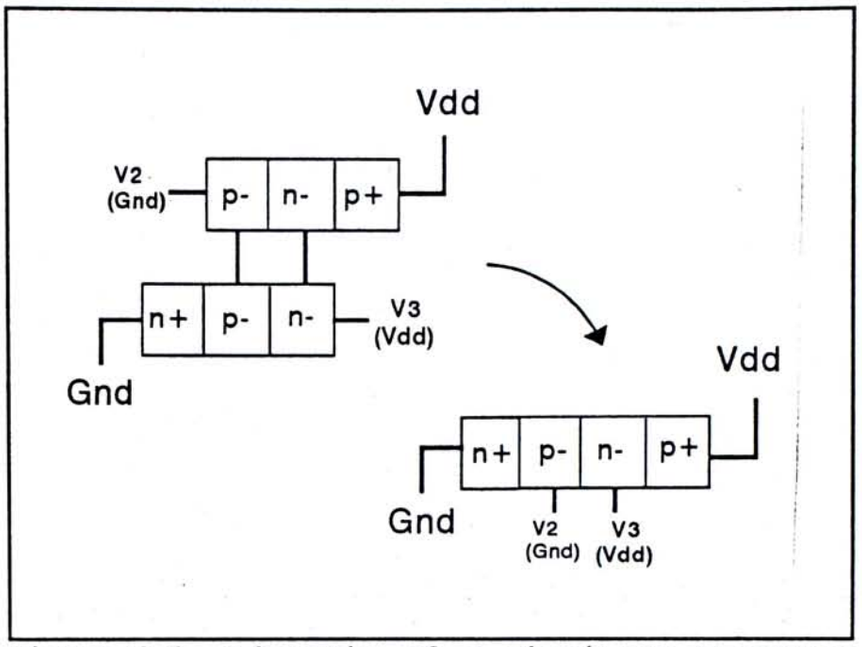


Figure 6.6 Schematic of a thyristor structure exist in an inverter structure.

The segment **b to c** is the negative resistance region, i.e., the current increases as the voltage decreases. At point c, where again dV/dI =0, the device is in the forward conducting or ON state at which the impedance is very low. The voltage and current values at this particular point are known as the holding voltage V_{hold} and holding current I_{hold}. Large values of V_{hold} and I_{hold} mean that higher voltage and current from the supply source are required to sustain the latch-up condition.

The latch-up behaviour of the inverter is characterized by four parameters, V_{sw}, I_{sw}, V_{hold} and I_{hold}. They are therefore used as latch-up susceptibility comparison indices.

The current-voltage characteristics in Figure 6.7 also shows a reverse blocking state (a-b') and a reverse breakdown region (b'-c'). However, these situations rarely occur in CMOS inverter operation so these two states will not be discussed.

Despite of the similarities in the pnpn structures of a thyristor and a CMOS circuit, the latch-up phenomenon in CMOS circuits is more complicated, primarily

due to the existence of the base resistors, i.e., the series resistors of p-tub and n-tub. Such resistors modulate the current flow and therefore the potential across the p-tub and the n-tub region. A detailed description of the latch-up mechanism in bulk silicon structure is given as follows.

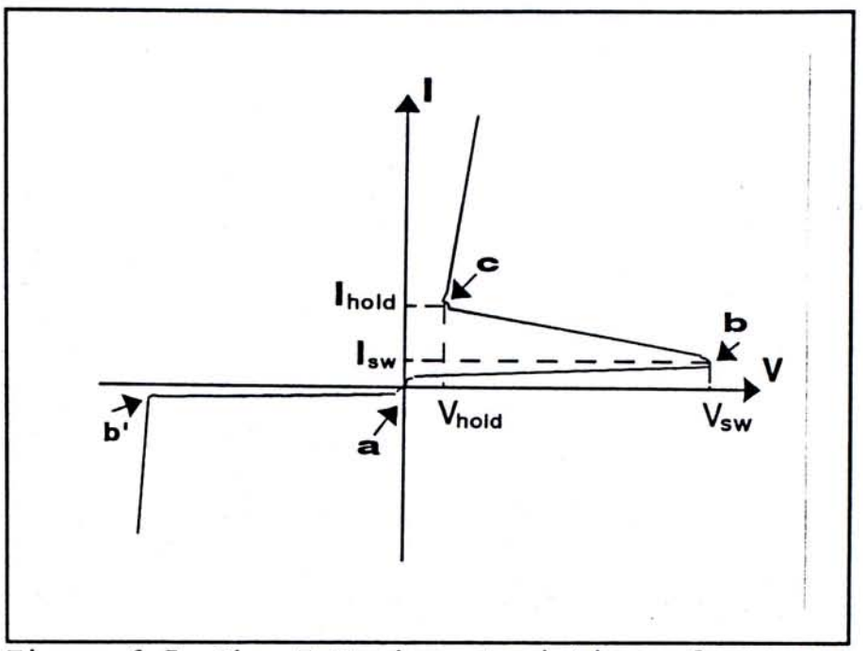


Figure 6.7 The I-V characteristics of a pnpn thyristor.

Consider the inverter structure as shown in Figure 6.5, during operation, starting from the pMOS transistor inside the n-tub, substrate current is generated at the drain and injected into the n-tub. Some of them are collected by the tub-contact to V_{dd}. Because of the finite tub resistance, there is a potential drop caused by the flow of electrons to V_{dd}. For those electrons that are not collected, they diffuse through the tub junction and are injected into p-tub with an amplified magnitude. When such a current become significant, it turns on the lateral bipolar transistor, current are then amplified again and injected back to n-tub. When the combined gain of such a loop become larger than unity, loop current become very huge and the inverter is said to be driven into the latch-up state.

The parasitic bipolar configuration is designed in such a way that the combined gain of them will not exceed unity under normal working conditions. However, there are many abnormal transient phenomenon which would trigger the

inverter into latch-up state. The triggering effects can be divided into external and internal cases:

(a) External Excitation

External excitation such as overshoot or undershoot at the inverter terminals may turn on the corresponding junctions.

(b) Internal Excitation

Excessive current flow inside the structure as a result of punch-through current, leakage current due to avalanche breakdown, Zener breakdown will cause sufficient voltage drop and therefore turn on substrate junction.

External excitation are easier to model by computer simulation and it contributes more in triggering latch-up.

6.4 Construction of a CMOS Inverter for Simulation

The simplest circuit unit in CMOS application is a CMOS inverter. A CMOS inverter consists of an nMOS and a pMOS transistor. The source and substrate terminals of the nMOS are connected to ground; The source and substrate terminals of the pMOS are connected to V_{dd}; The gate of both the transistors are tied together and become the inverter input while the drains of both the transistors are joint together and become the inverter output. The schematic diagram of such an inverter is shown in Figure 6.8 for reference.

To build such an inverter on bulk silicon substrate, sufficient separation between the two transistors is required. A cross-sectional view of such an inverter on bulk silicon substrate using n-well processing technology is already shown in Figure 6.5. Such an inverter configuration is prone to latch-up as discussed in

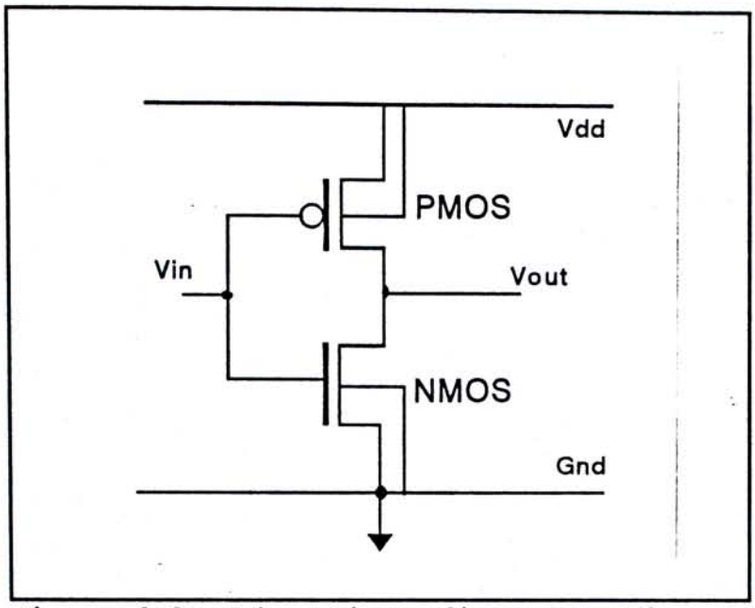


Figure 6.8 Schematic diagram of an inverter structure.

section 6.3.

Now consider building an inverter on the BCSOI silicon-on-nitride substrate, not only all the junctions are blocked by the nitride material, the drain of the nMOS and pMOS transistors can be brought next to each other, realizing the highest packing density as if in conventional SOI structure. Such an advantage is demonstrated in Figure 6.9 for reference. It is observed that openings are made in the buried insulator underneath the entire gate region of both the nMOS and pMOS transistors.

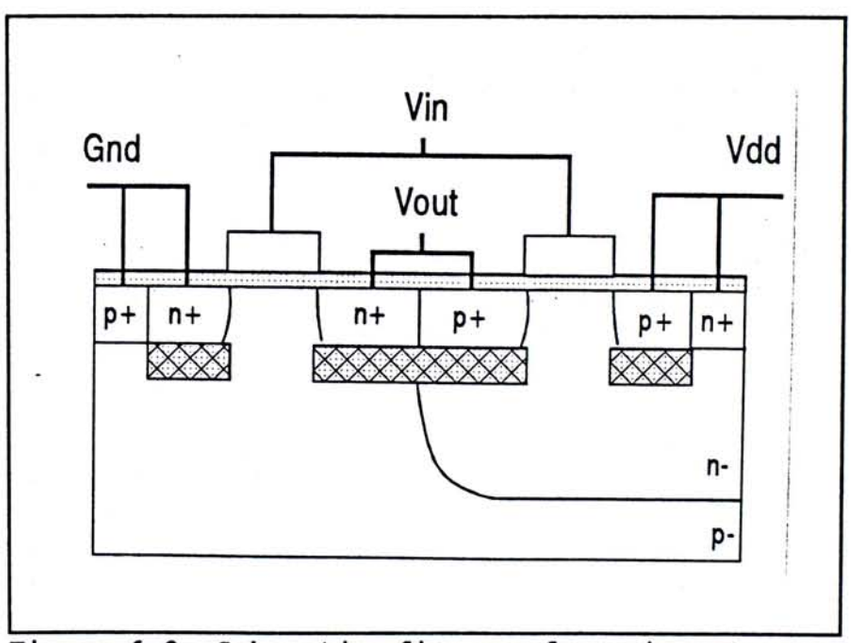


Figure 6.9 Schematic figure of an inverter on novel body contact SIMNI substrate.

Because of the blocking feature of the nitride layer, the drain region can be brought next to each other while preventing direct shorting of n+ drain to n- well or p+ drain to p-substrate.

In other words, as nMOS and pMOS can be placed more closely in the BCSOI structure than in bulk silicon structure, the inverter is already more latch-up resistance than bulk structure.

Simulations on the inverter structure is firstly made by providing proper biasing to all the junctions in the inverter:

1) Inverter input : low at zero volt.

2) Inverter output : high at V_{dd}

3) pMOS source and substrate : high at V_{dd}

4) nMOS source and substrate : low at zero volt, i.e. ground.

The inverter output is then pulled even higher progressively while at the same time, monitoring the output current. If an increase of the current alike those of a thyristor characteristics is recorded, it indicates that the inverter is driven to the latch-up state.

By presenting the graph of the inverter output current versus output voltage, the conditions for latch-up can be detected from the turning points of the curve. Although both the nMOS and pMOS transistors on the inverter to be simulated can work up to 5.0V, in view of the lower supply voltage drive in future, a V_{dd} of 3.0V is preferred in subsequent simulations. Significant savings on computation time is also realized. In fact, no matter it is a 5.0V or 3.0V supply voltage, latch-up occurs, if it occurs, when any of the normally reversely biased junction is turned on, which is 0.7V in excess of the V_{dd} value. In other words, latch-up susceptibility simulation results are not affected by the choice of V_{dd} value.

Shown in Figure 6.10 is the simulated latch-up curve of the reference inverter. Referring to Figure 6.10, values of V_{sw}, I_{sw}, V_{hold} and I_{hold} are deduced as

3.77V, 2.52μA/μm, 3.01V and 50.56μA/μm respectively. These are the latch-up characteristics of such an inverter and will also be used as the base of comparison for simulation on latch-up dependence on structure parameters.

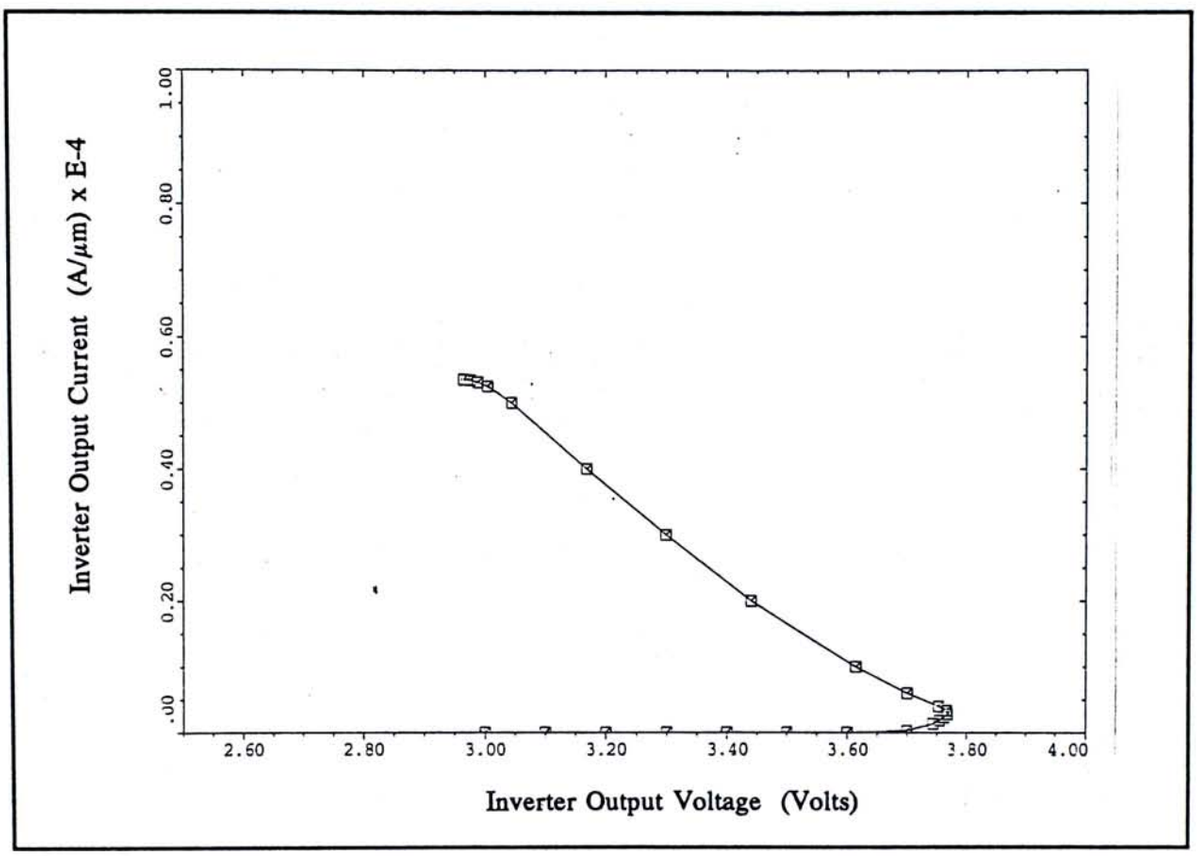


Figure 6.10 Simulated inverter output current versus output voltage characteristics of the reference inverter.

On the other hand, it would be of interest to investigate the potential distributions and current flow of the entire inverter structure at the condition just before and after latch-up state. Such an investigation is made possible by using the CONTOUR command of the MEDICI simulation software, but cannot be found in direct inverter measurement.

In Figure 6.11, the output voltage of the inverter is at 3.0V, i.e., the V_{dd}

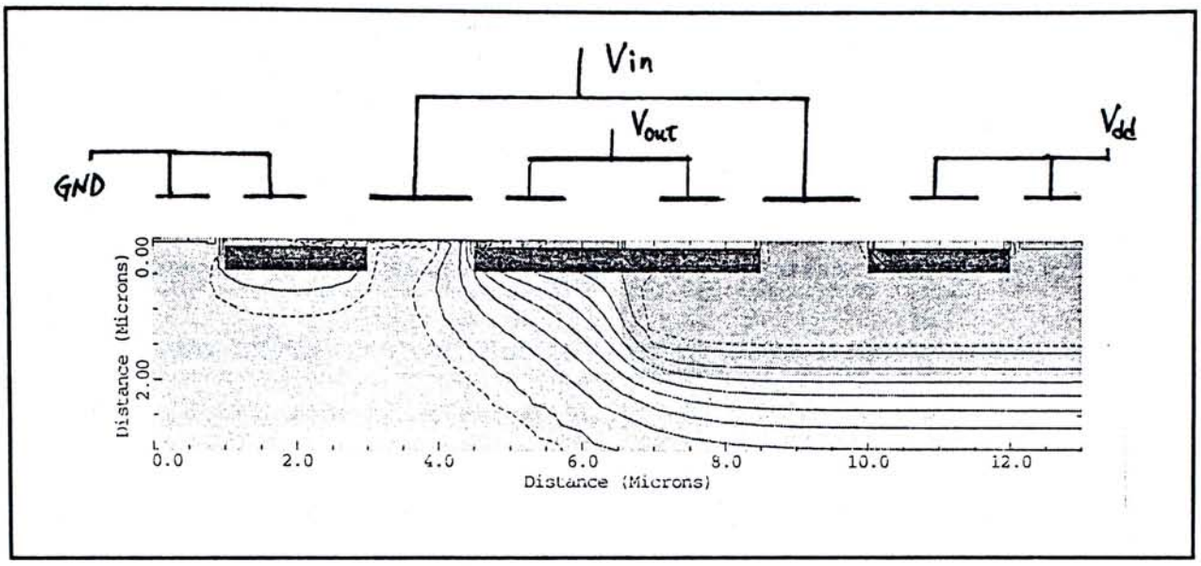


Figure 6.11 The potential contour distribution of the inverter with V_{out} = 3.0V.

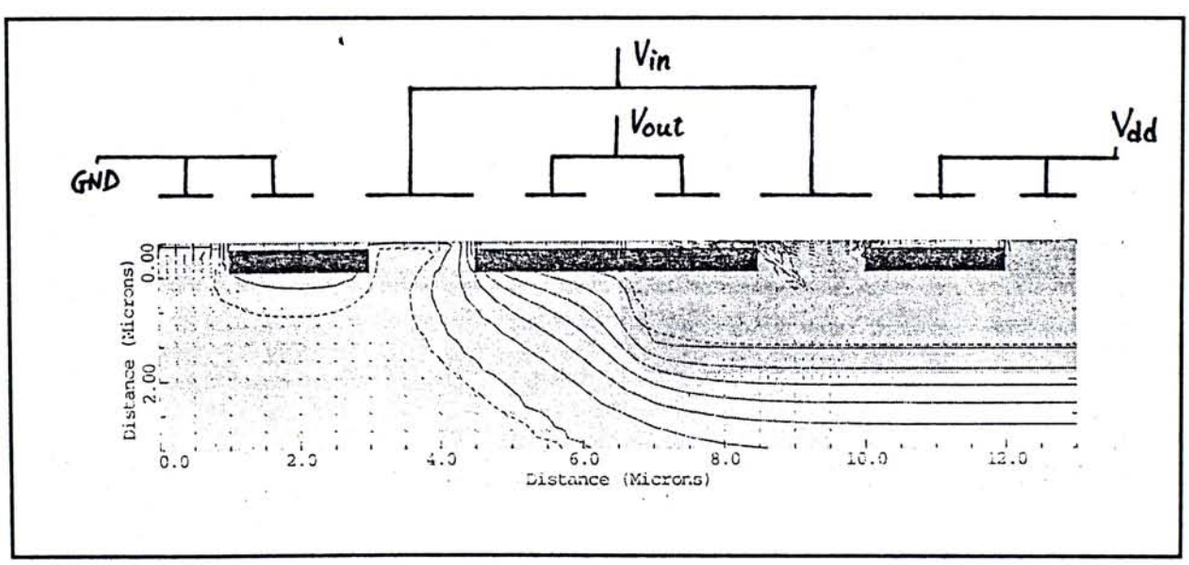


Figure 6.12 The potential contour distribution of the inverter with V_{out} = 3.7V.

value. It is observed that the potential contour distribution is well-behaved, indicating the isolation feature of the tubs are in good reversely biased situation. No current flow within the inverter structure is apparent seen.

When the inverter output voltage, V_{out}, is pulled high to 3.7V, as referred

to Figure 6.12, although the reversely biased isolation feature of the tubs are still maintained, current flow lines are conspicuously observed. At an output bias of 3.7V, the p+ drain junction of the pMOS transistor is at the verge of turnning on. Current flow is therefore seen to be originating from that p+ junction and flow into the n-tub. Some of the carriers flow to the p+ source junction and recombined there; whereas some migrate across the depletion region and are then collected by the p-substrate.

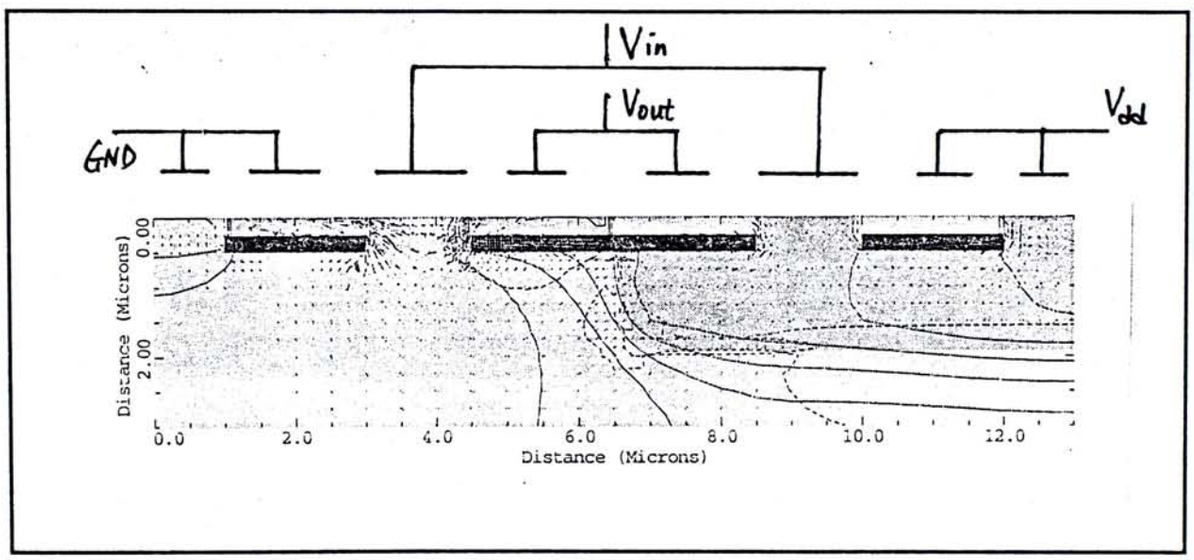


Figure 6.13 The potential contour distribution of the inverter at latch-up state.

Upon further increasing the V_{out} bias, the inverter is driven into the latch-up state with a I-V characteristics shown in Figure 6.10. At the latch-up holding condition, substantial current flows from the V_{dd} to V_{ss}. Referring to Figure 6.13, the potential contour distribution in the inverter structure is very different from the previous two figures. The well-behaved isolation feature is disrupted. A lot of flow lines are observed in the structure, indicating large quantity of current flow within the inverter structure.

6.5 Latch-up Susceptibility Dependence

The inverter structure in Figure 6.9 is reconstructed in Figure 6.14 by adding on it some key parameters which are described as follows:

a) t_{in} : buried insulator thickness;

b) t_{bc} : buried insulator body contact size;

c) D_{nw} : the depth of the n-well. It is the distance between the silicon surface and the metallurgical junction of the n-well.

d) S_{pn} : separation of the p- and nMOS transistors. It is defined as the distance between the neighbouring edge of the polysilicon gate of the p- and n-MOS transistors.

All the above structure parameters are vulnerable to variation on structure manufacturing. Changes on latch-up susceptibility are apparent as a result. To verify their effects, computer simulations is done on the parameters one by one.

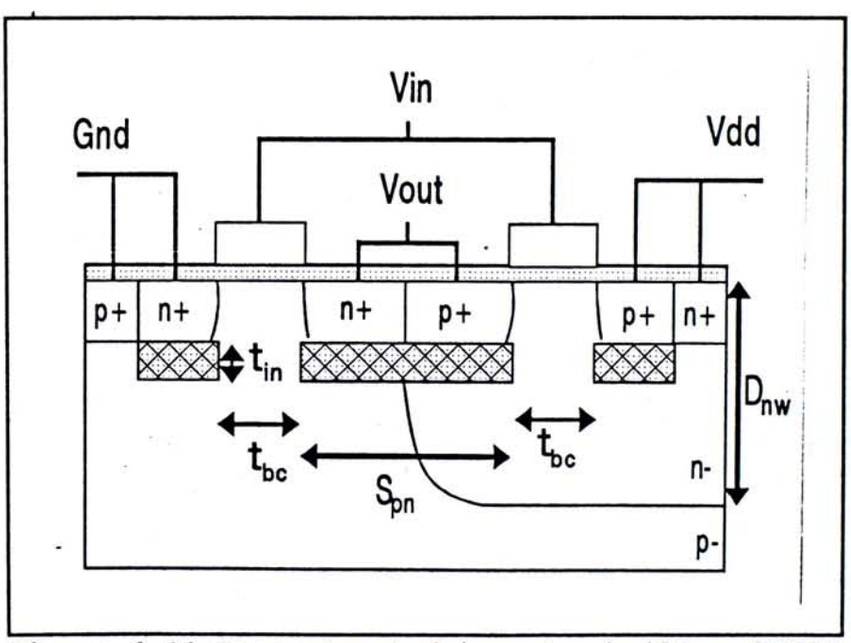


Figure 6.14 Reconstructed invertor built on BCSOI SIMNI substrate.

6.5.1 Dependence in Insulator Thickness

Inverter latch-up susceptibility against the change of insulating nitride thickness, t_{in}, is characterised by extracting the values of V_{sw}, I_{sw}, V_{hold} and I_{hold}

from the simulated "latch-up" curve of structure that are of different t_{in} value. The results are shown in Figure 6.15 to 6.18 for reference.

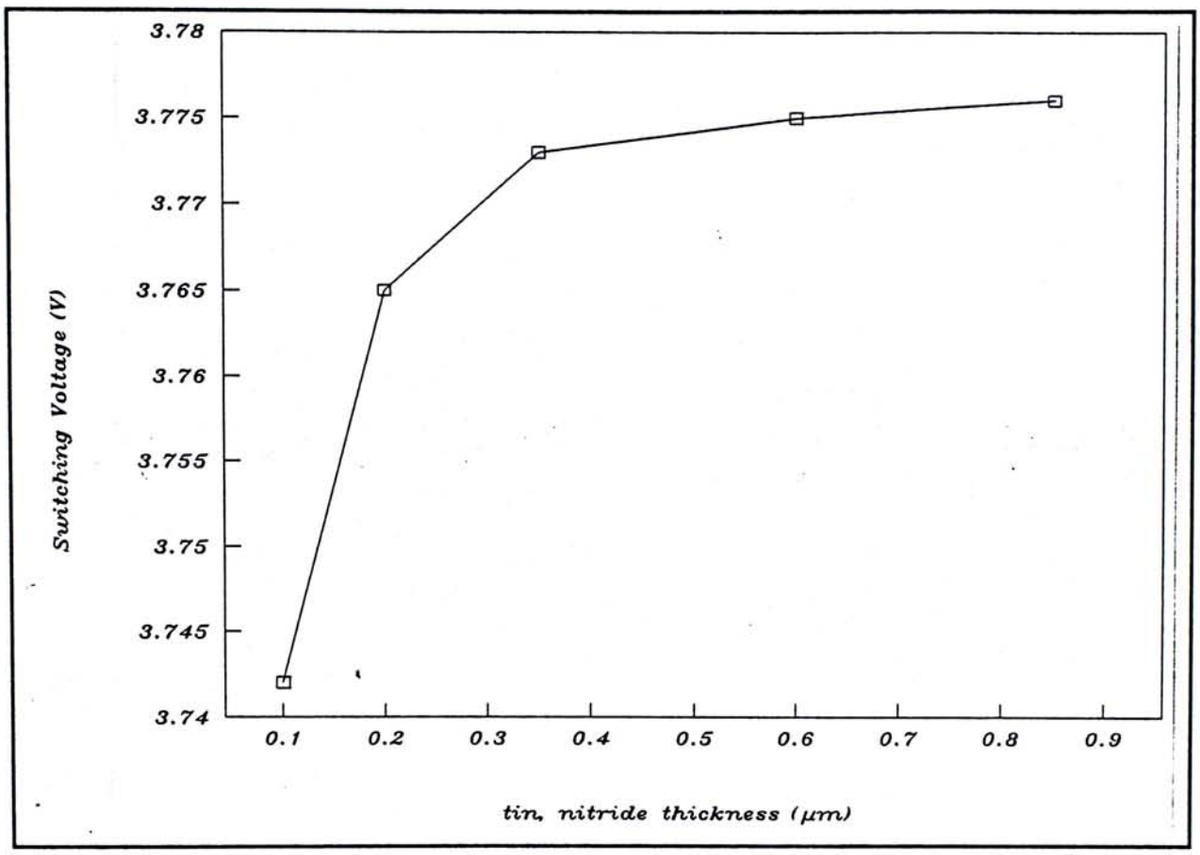


Figure 6.15 Simulated V_{sw} characteristics versus t_{in}.

From Figure 6.15, it is observed that V_{sw} in general increases with the buried nitride thickness. The increment is more rapid when the layer is thin, but becomes stable when it is thick, roughly starting from t_{in}=0.35μm. Yet, the overall V_{sw} increment is only 34mV for t_{in} changing from 0.1μm to 0.85μm.

According to Figure 6.16, the increase of I_{sw} is rather monotonous with the thickness. The overall increment is 18.2%. So far, it appears that a thick insulating nitride layer makes the structure less susceptible to latch-up.

From Figure 6.17, V_{hold} is also found to be increasing with t_{in}. Yet, the overall increment is only 70mV. In Figure 6.18, I_{hold}, in general, was found to be increasing with t_{in}. The increment is more rapid at thin t_{in}, and it starts levelling off

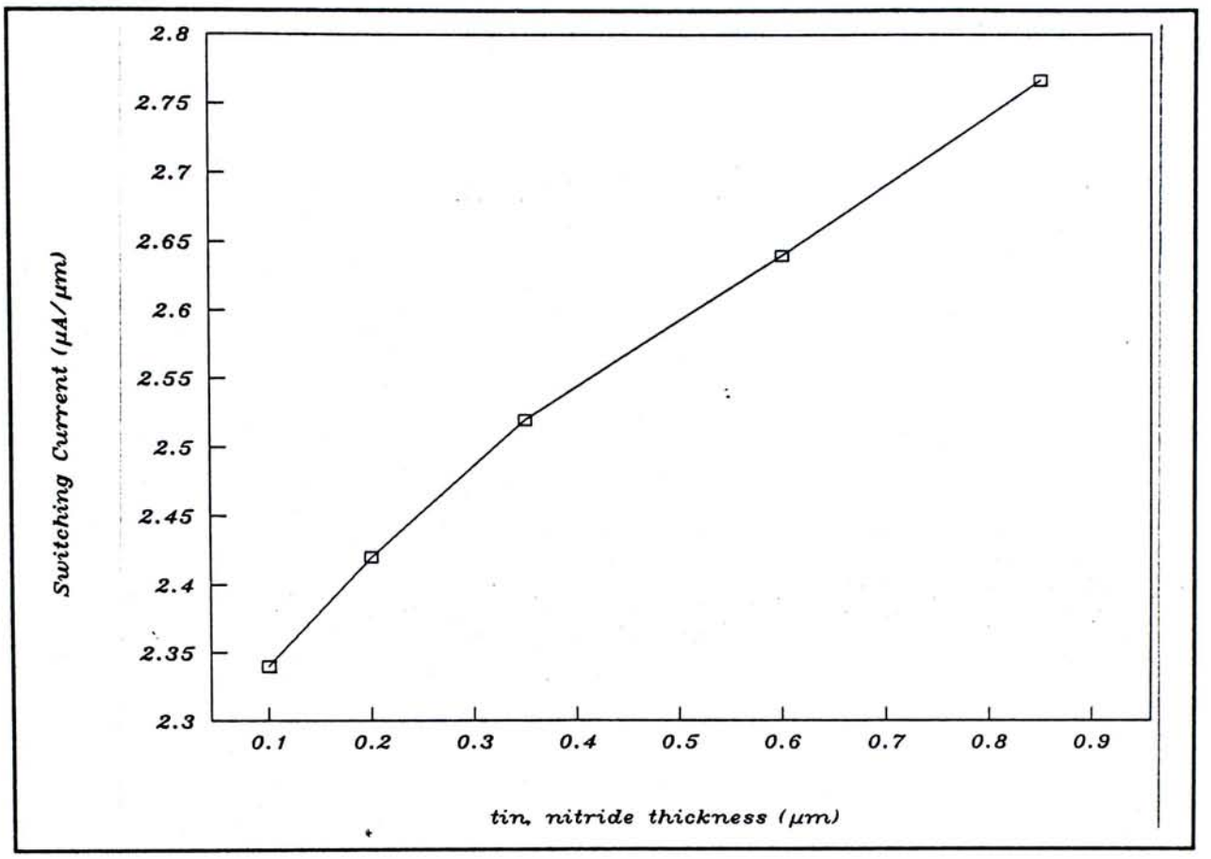


Figure 6.16 Simulated Isw characteristics versus tin.

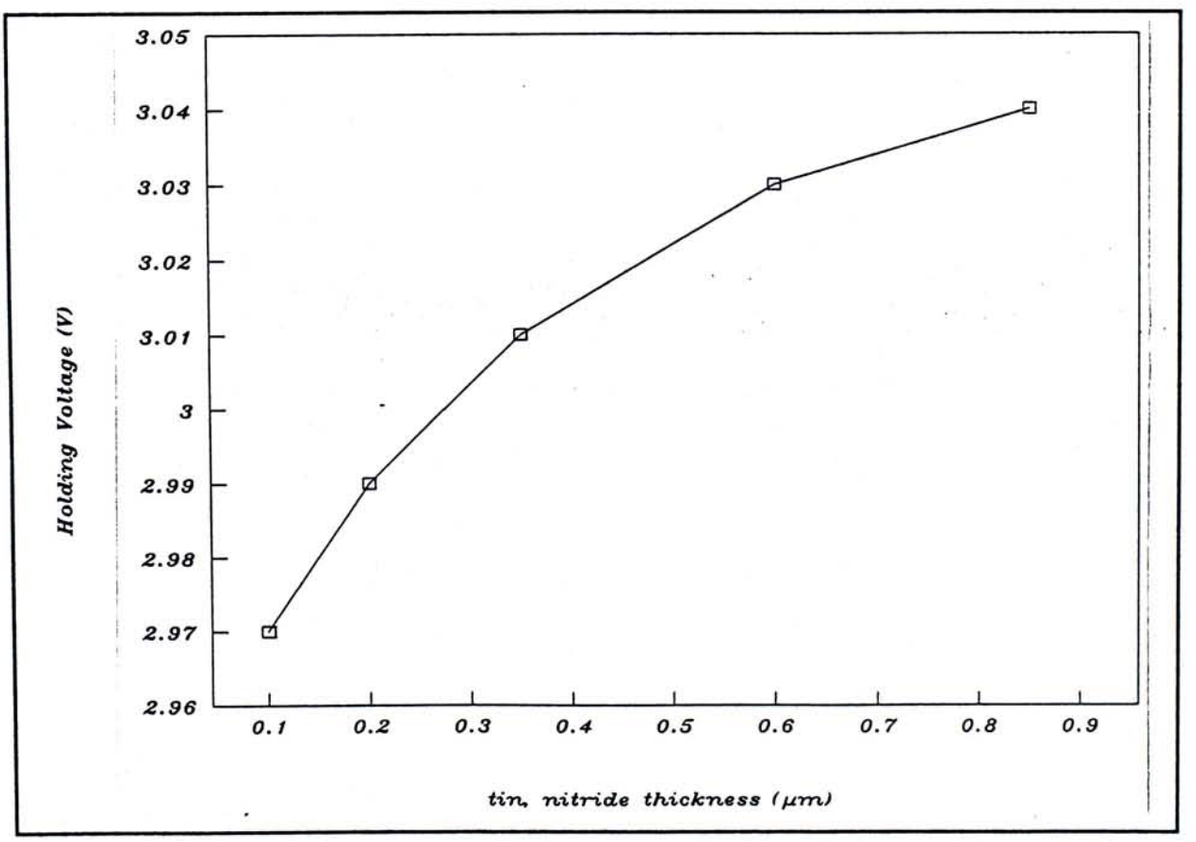


Figure 6.17 Simulated V_{hold} characteristics versus t_{in}.

at thicker t_{in}, roughly from 0.35μm. The overall increment was found to be 119.3%.

It shall be noted that, for all t_{in}, all the recorded V_{hold} are around 3.0V, i.e. the value of V_{dd}. This indicates that, after switching on, the latch-up conditions will easily be held at V_{dd} if the source can supply current in excess of 57.23μA/μm.

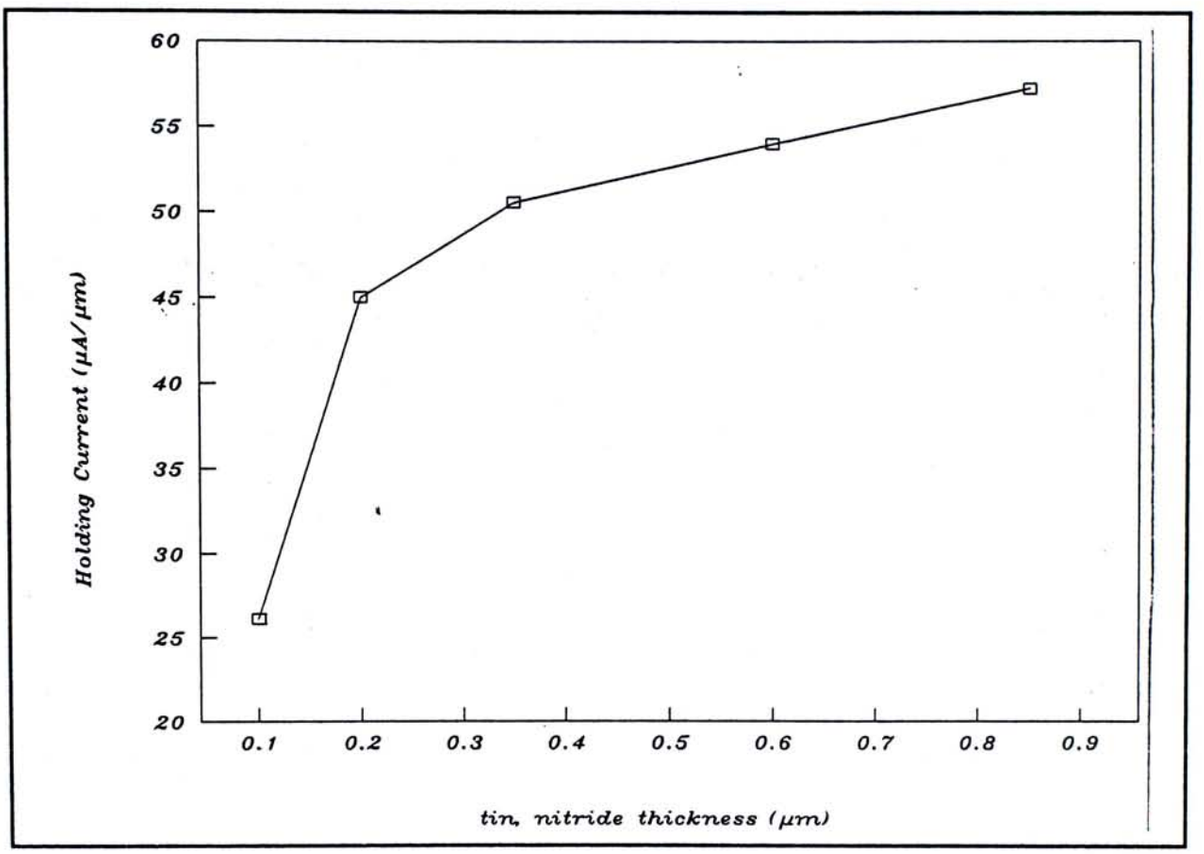


Figure 6.18 Simulated I_{hold} characteristics versus t_{in}.

The simulation results suggest that thick t_{in} is more desirable in terms of higher resistance to latch-up. However, in SIMNI wafer preparation, thicker t_{in} calls for higher substrate manufacturing cost. A t_{in}=0.35μm appears to be quite a good trade-off.

6.5.2 Dependence in N-well Depth

By the same token, the dependence are characterised by extracting data from

computer simulation output files and the results of V_{sw}, I_{sw}, V_{hold} and I_{hold} against N-well depth D_{nw} are shown in Figure 6.19 to 6.22 respectively.

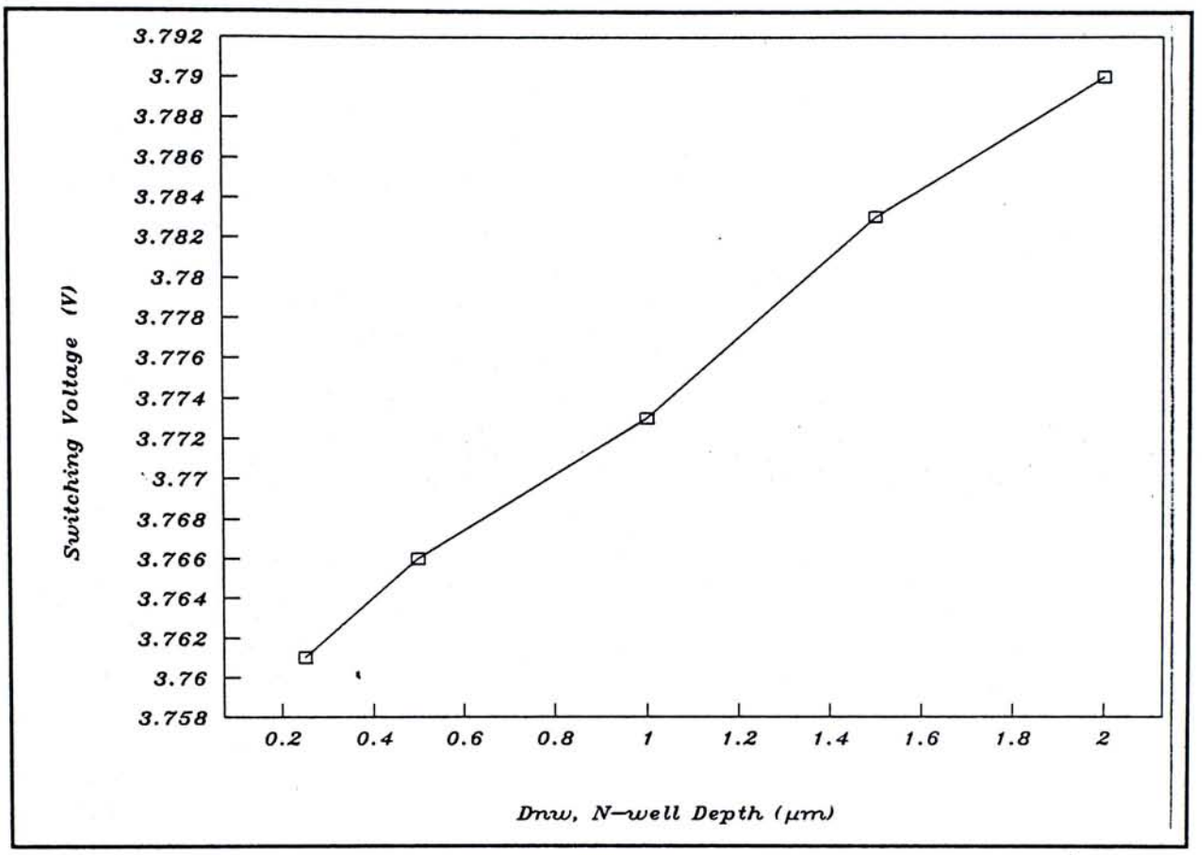


Figure 6.19 Simulated V_{sw} characteristics versus D_{nw}.

From Figure 6.19, V_{sw} is seen to be increasing with D_{nw}. Of the entire eight-fold increment in D_{nw}, the increment in V_{sw} is only 29mV. Usually, D_{nw} is deep with a depth of 2 to 4μm. Good V_{sw} values can be obtained in such a range.

From Figure 6.20, I_{sw} is also seen to be generally increasing with D_{nw}. The increment rate is low ($\approx 0.17\mu A/\mu m^2$) for shallow n-well junction with $D_{nw} < 1\mu m$. For deep n-well depth, the rate is more rapid ($\approx 1.14\mu A/\mu m^2$), a more than six-fold increment in rate. Nevertheless, the overall increment in I_{sw} is 51.8%.

On the contrary, as referred to Figure 6.21, V_{hold} is found to be decreasing with increasing D_{nw} in a fairly monotonous manner. The overall decrement is

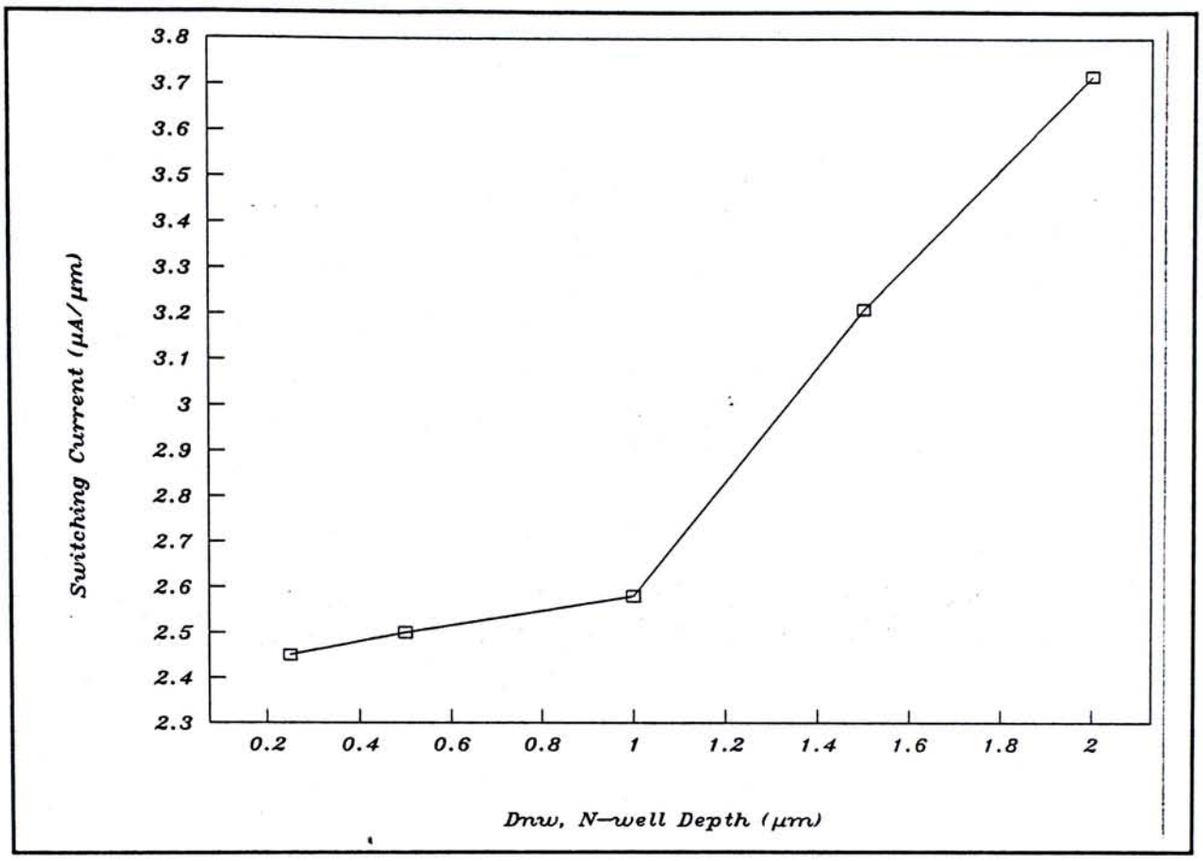


Figure 6.20 Simulated I_{sw} characteristics versus D_{nw}.

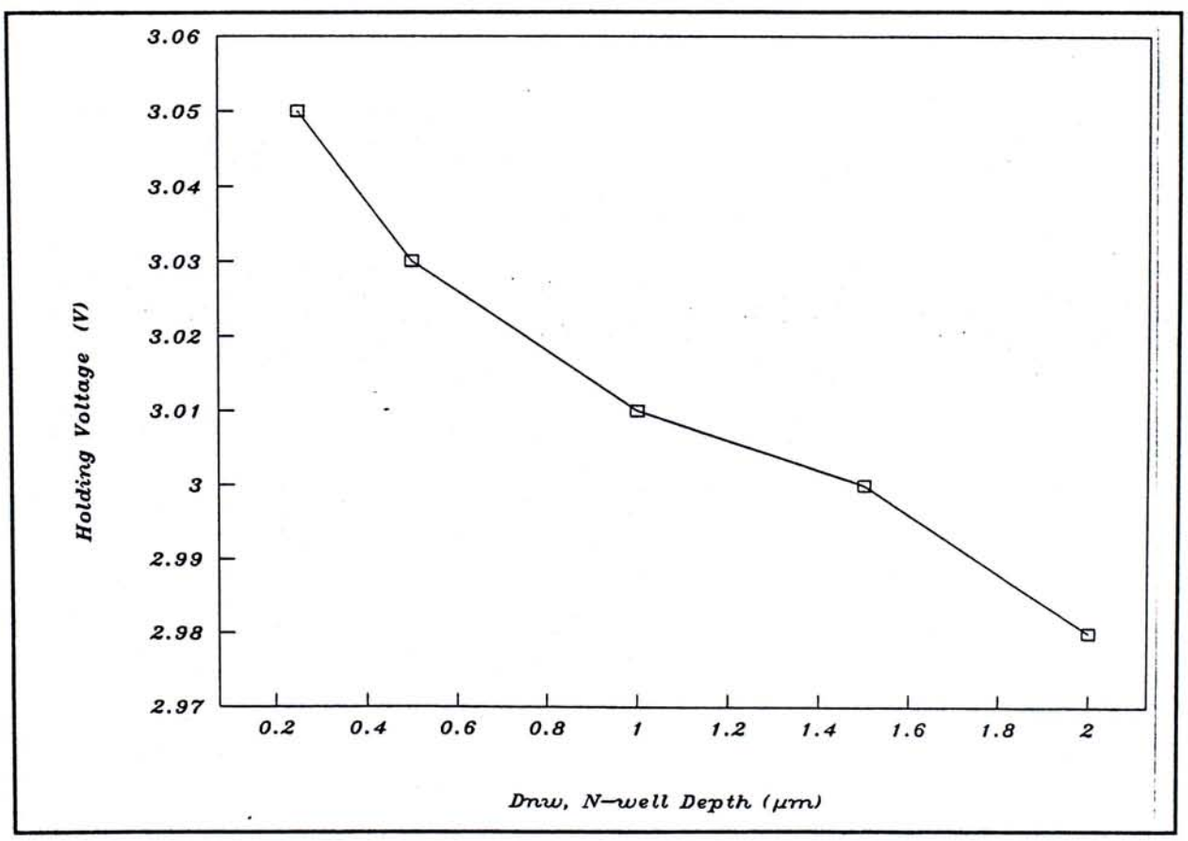


Figure 6.21 Simulated V_{hold} characteristics versus D_{nw}.

extracted to be 70mV. Yet, all the values of V_{hold} are close to V_{dd}, which suggest that the structure is prone to sustain the latch-up state once it is triggered.

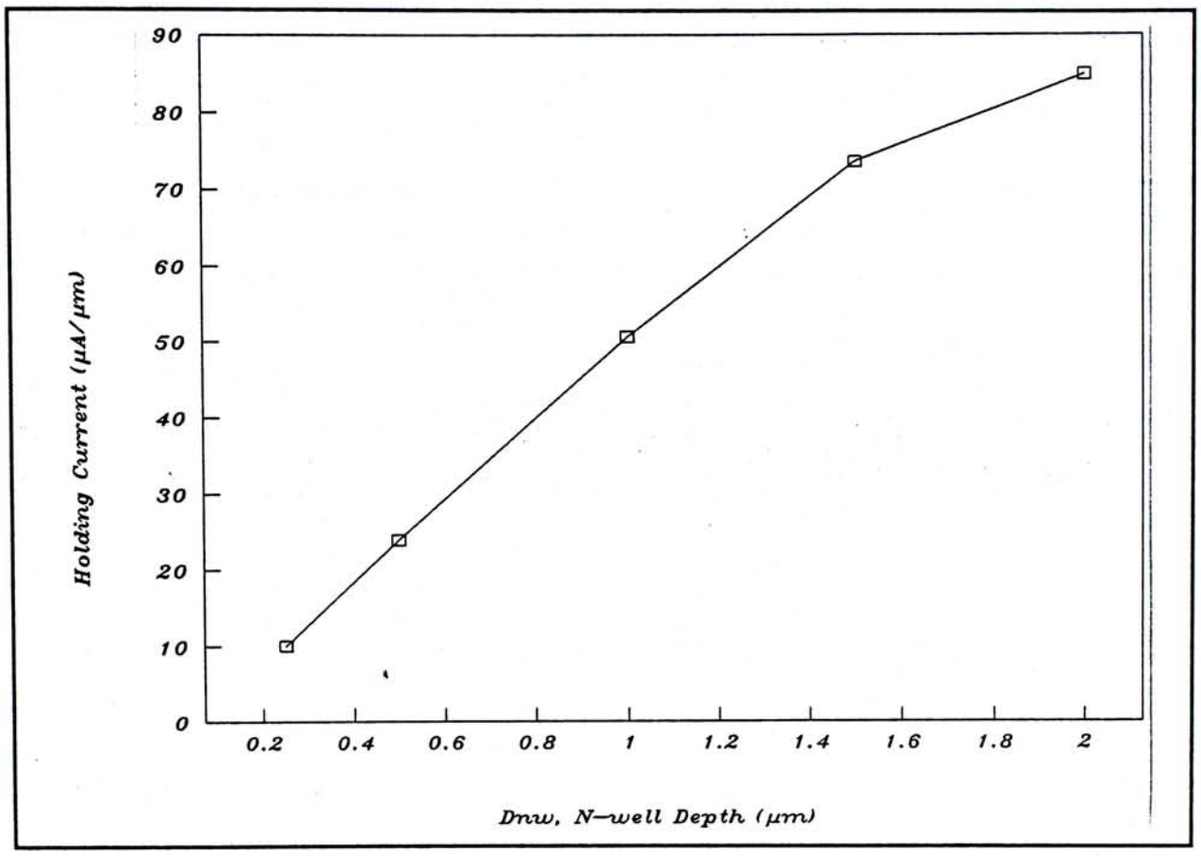


Figure 6.22 Simulated I_{hold} characteristics versus D_{nw}.

In Figure 6.22, it is observed that I_{hold} increases with D_{nw}. The overall increment is a significant 844%, thereby supporting that deep n-well structure is more favourable since much higher hold current is called for so as to sustain the latch-up state.

6.5.3 Dependence in Transistor Separation

The Separation between nMOS and pMOS transistors, S_{pn}, in a CMOS inverter circuit is of great importance in determining packing density of circuits and affect latch-up susceptibility. One may perceive that the larger the S_{pn}, the less

susceptibility of an inverter to latch-up.

As shown in Figure 6.23, the increase in V_{sw} is rather drastic when S_{pn} increases from 1μm to 2μm. A 100mV increment is recorded. For S_{pn} larger than 2μm, the subsequent V_{sw} increment become rather mild. The increment is only 30mV for S_{pn} changes from 2μm to 12μm. A small S_{pn} means a narrow base vertical transistor is formed, resulting in higher loop gain and therefore lower V_{sw}.

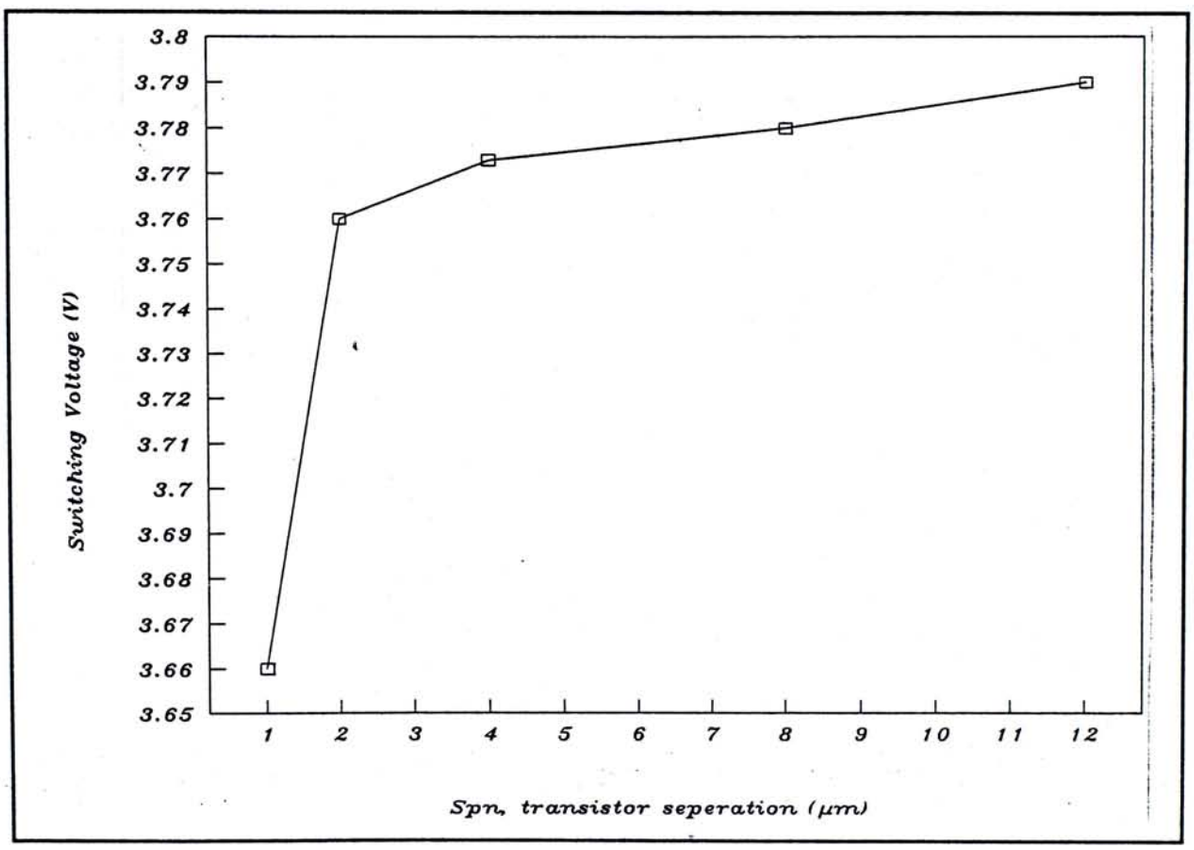


Figure 6.23 Simulated V_{sw} characteristics versus S_{pn}.

On the other hand, as referred to Figure 6.24, I_{sw} is found to be monotonously increasing with S_{pn}. The overall increment is 34.8% for a twelve-fold S_{pn} increment.

Similar to the shape of V_{sw}, as shown in Figure 6.25, V_{hold} is also found to have a more rapid increment at small S_{pn}. Nevertheless, all the values are at the

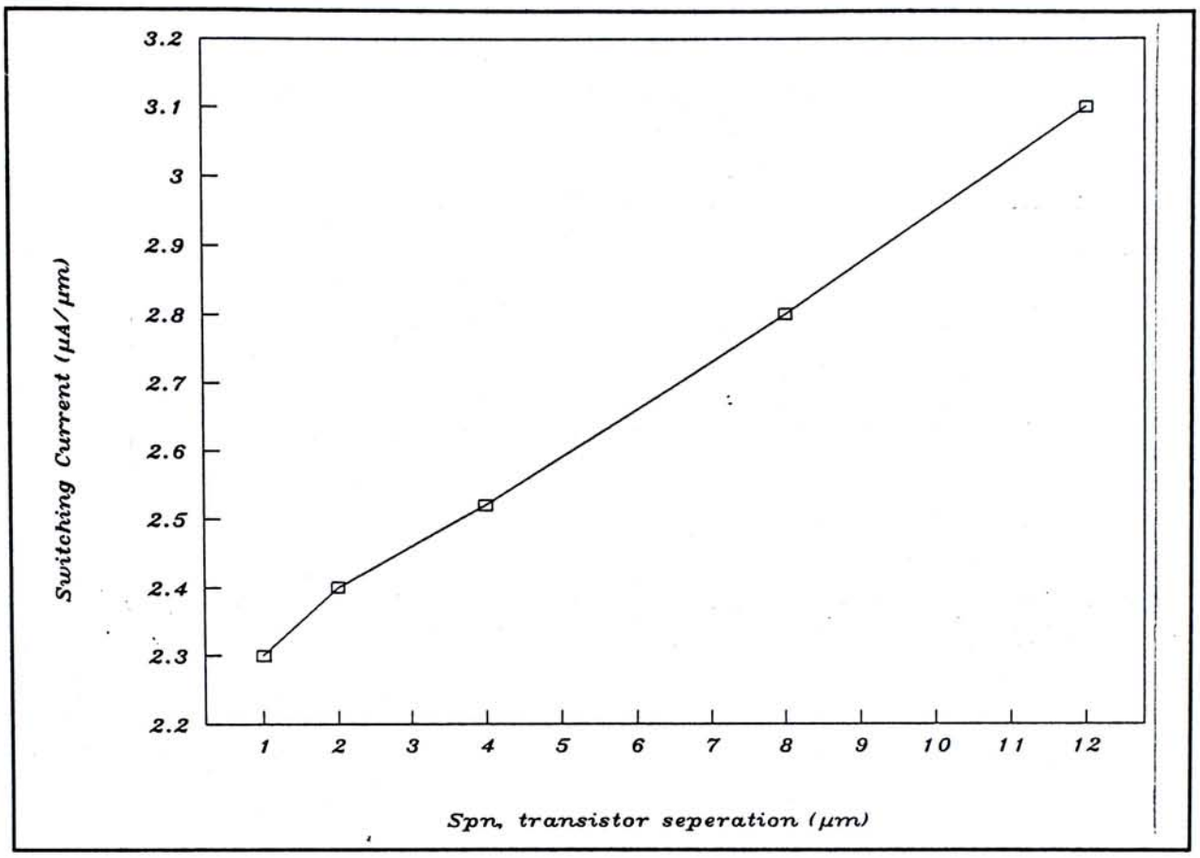


Figure 6.24 Simulated I_{sw} characteristics versus S_{pn}.

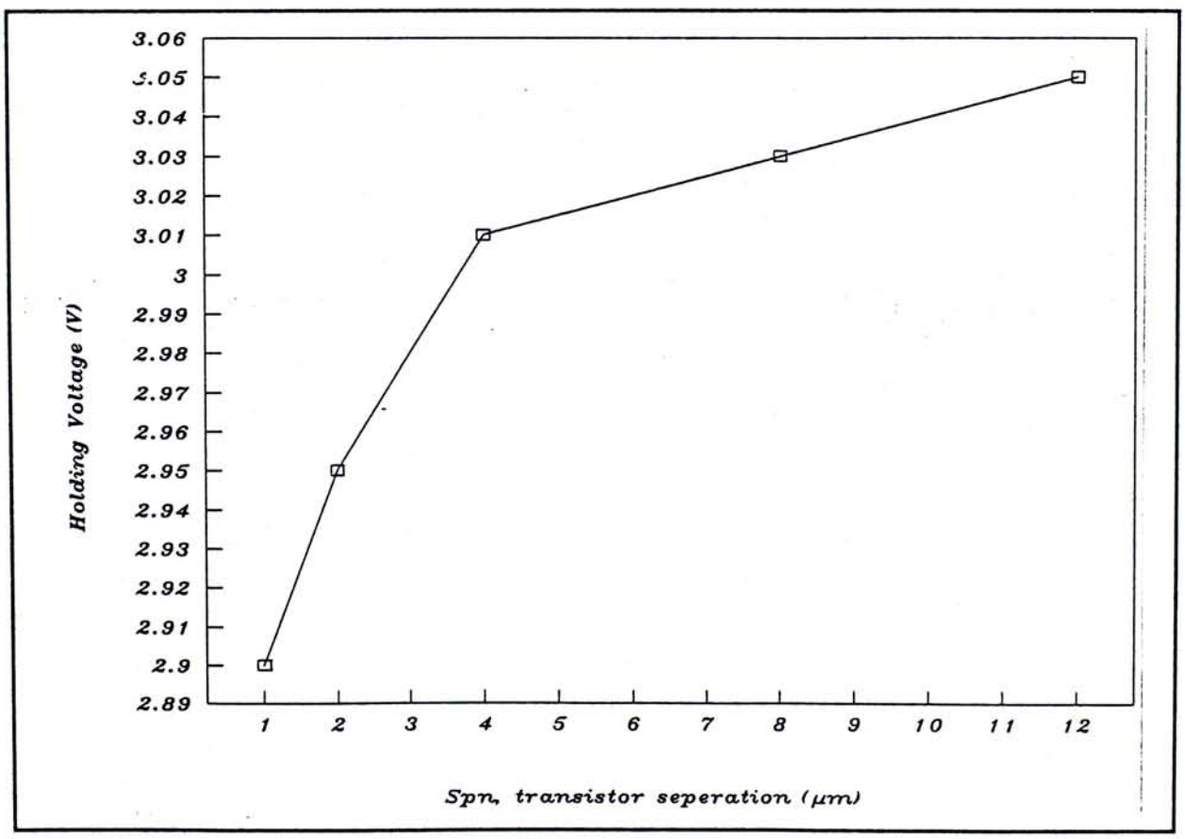


Figure 6.25 Simulated V_{hold} characteristics versus S_{pn}.

vicinity of 3.0V, which means that once the inverter latches, it is easily to be sustained in terms of V_{hold} characteristics. The overall increment is 150mV.

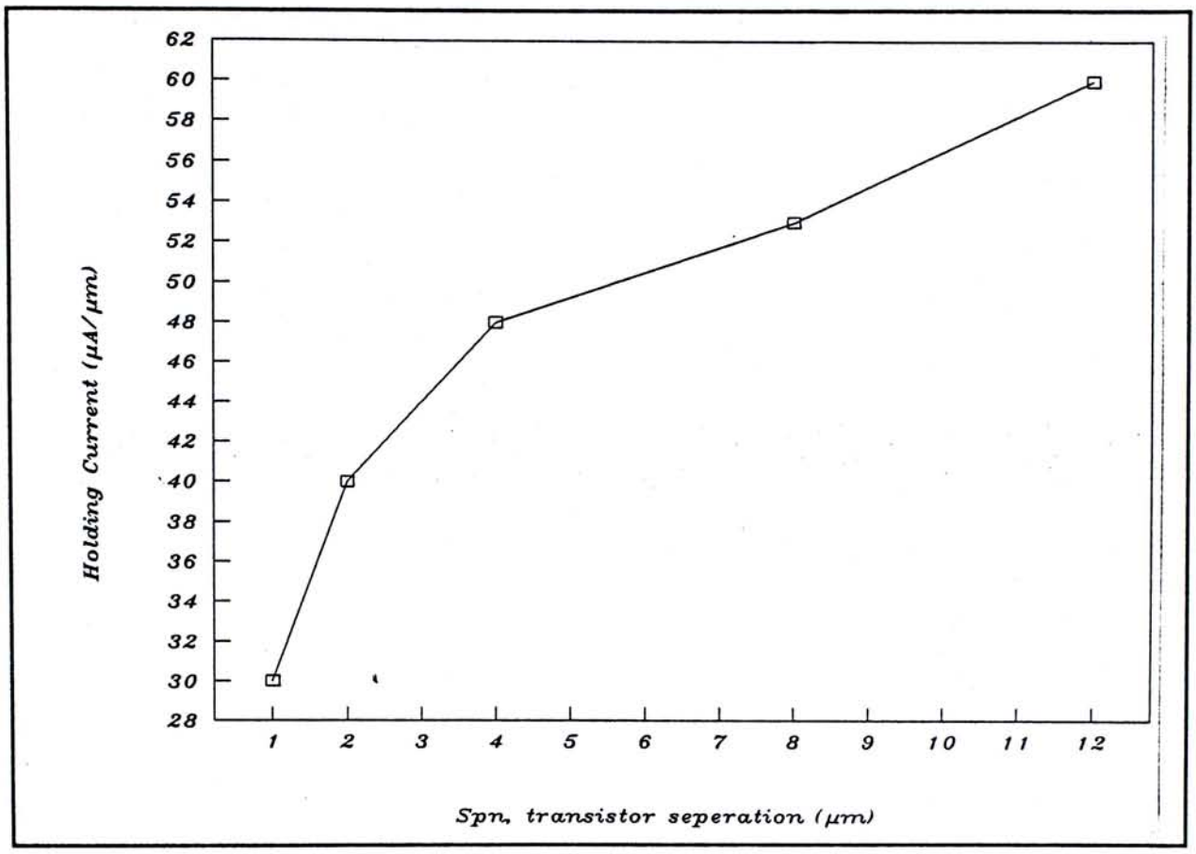


Figure 6.26 Simulated I_{hold} characteristics versus S_{pn}.

Referring to Figure 6.26, the lower I_{hold} at $S_{pn}=1\mu m$ reaffirms that such an inverter structure is very easy to become latch-up. I_{hold} then increases with larger S_{pn}. The overall increment is 200% for a twelve-fold S_{pn} increment. Although a $12\mu m$ separation seems large in reality, it is still of interest for academic studies.

6.5.3 Dependence in Size of Body-Contact

As referred to Figure 6.27, the size of body-contact, t_{bc}, is found to have apparent effect on latch-up susceptibility, in which the smaller the body contact size, the higher the switching voltage is resulted. The change in V_{sw}, as referred to Figure

6.27, are found to be more drastic then other parameters dependence. At t_{bc}=0.25μm, i.e., 20.83% of entire channel length, V_{sw} is found to be 3.837V, which is highest among all other simulated V_{sw} results. The overall V_{sw} increment is a mere 64mV for t_{bc} shrink from 1.2μm to 0.25μm of the 1.2μm channel length.

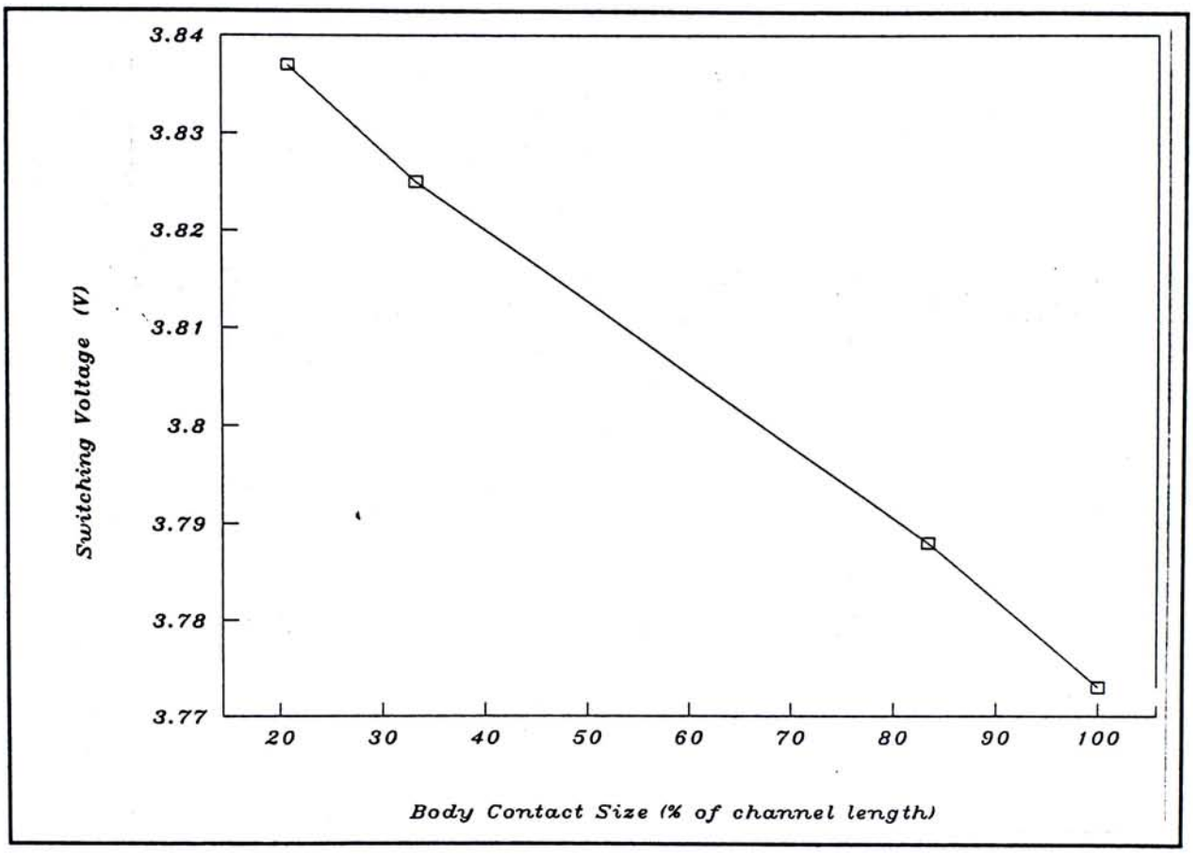


Figure 6.27 Simulated V_{sw} characteristics versus t_{bc}.

On the other hand, as referred to Figure 6.28, a higher I_{sw} is also recorded for a smaller t_{bc} opening. The increment is more rapid for small t_{bc}. The overall increment is 34.76%.

In Figure 6.29, V_{hold} is found to be increasing with smaller t_{bc}. A value of 3.15V is recorded for t_{bc}=0.25μm. Although such a value is merely 0.15V higher than the V_{dd}, it is already the highest holding voltage among all other structure parameters combinations. The overall increment is 140mV.

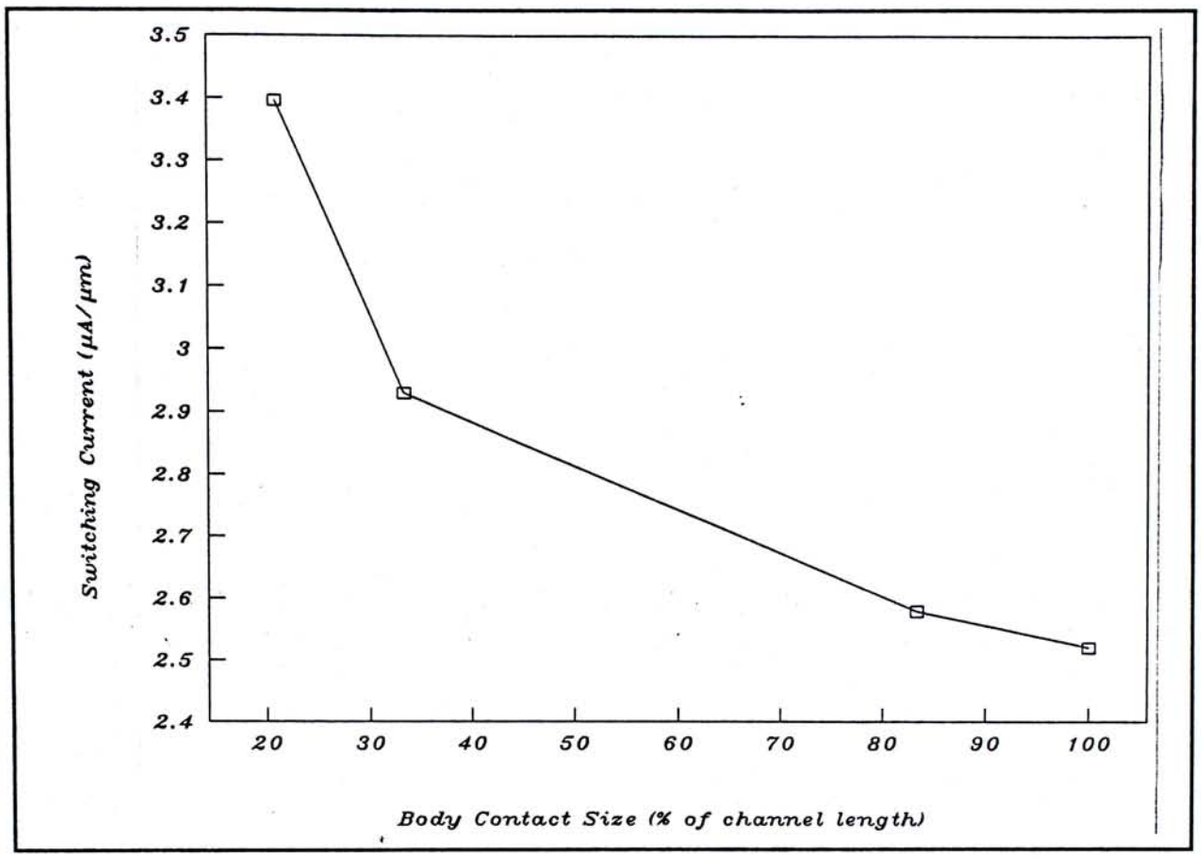


Figure 6.28 Simulated I_{sw} characteristics versus t_{bc}.

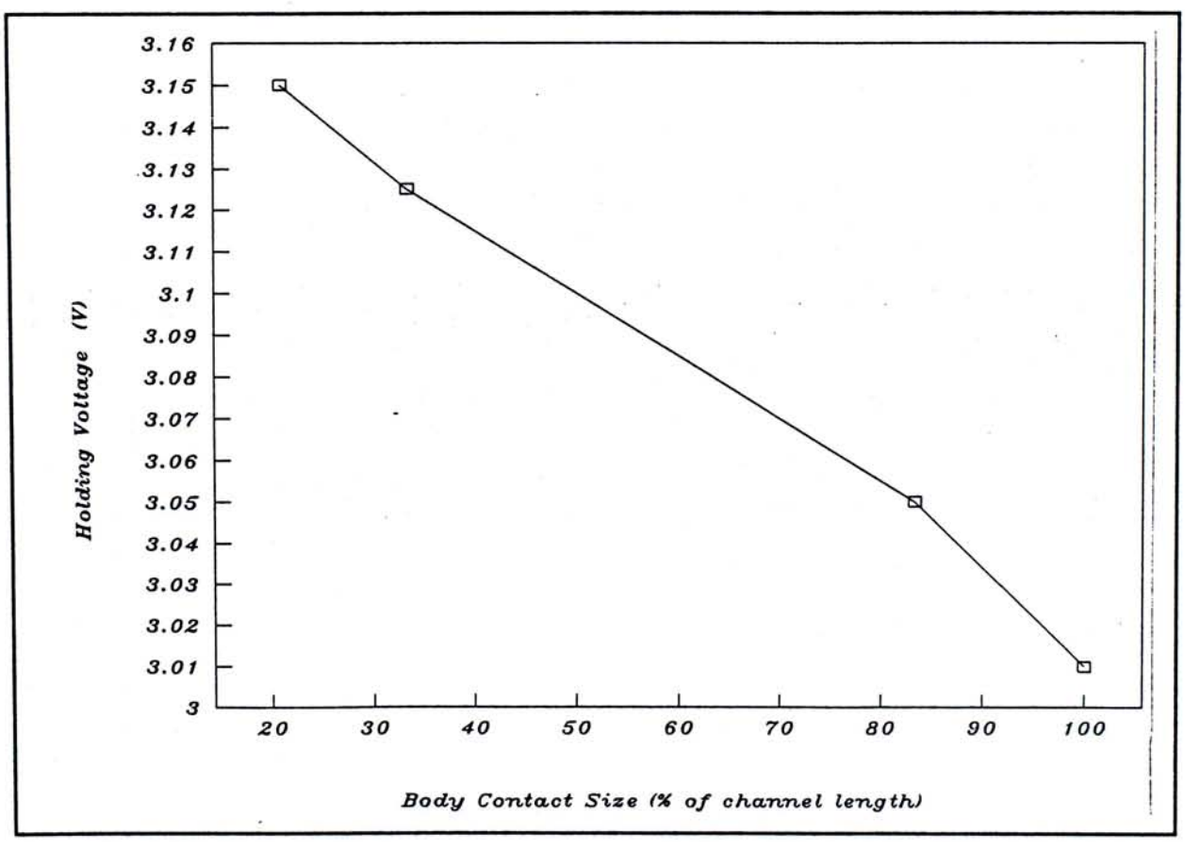


Figure 6.29 Simulated V_{hold} characteristics versus t_{bc}.

Referring to Figure 6.30, I_{hold} is also observed to be increasing with shrinking t_{bc}. Again, this means that a higher current is surmounted to sustain the latch-up state. The overall increment is 23%.

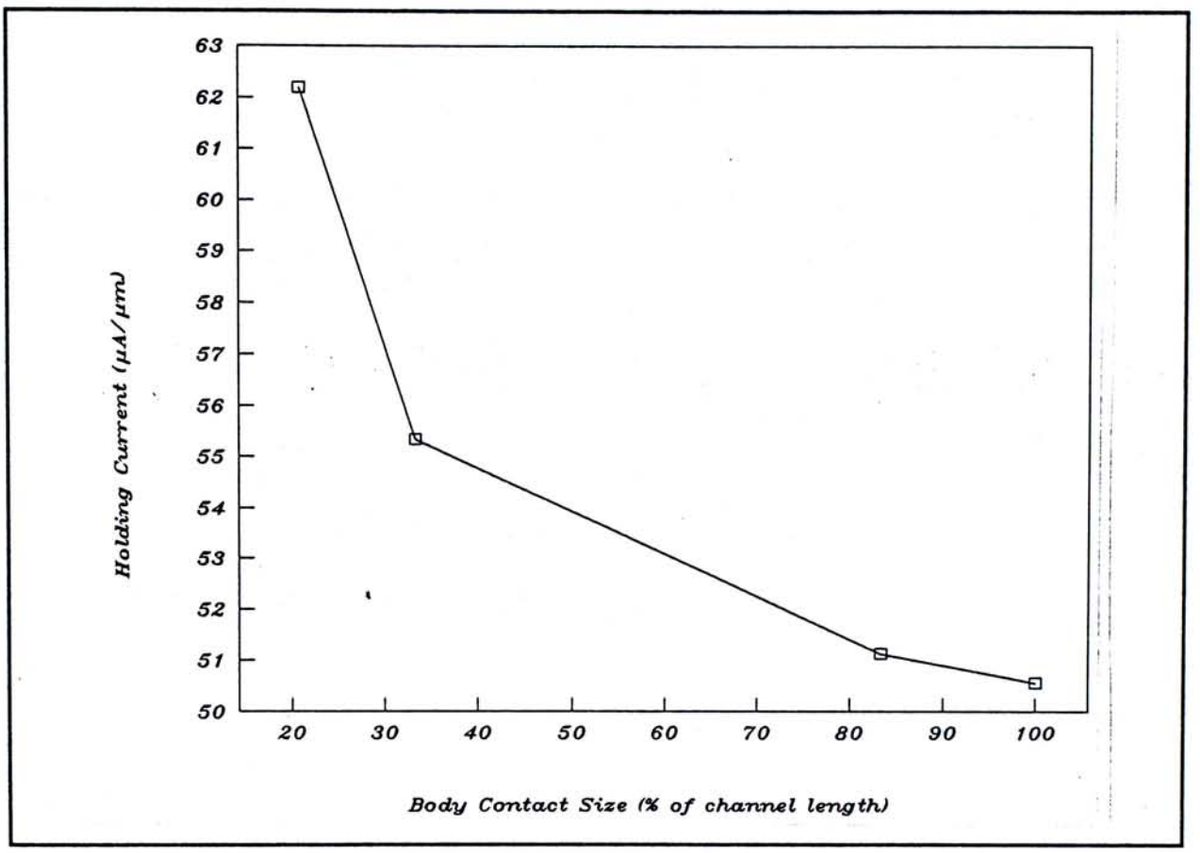


Figure 6.30 Simulated I_{hold} characteristics versus t_{bc}.

All the t_{bc} dependence simulation results suggest that the structure is less susceptible to latch-up when t_{bc} is getting small. This indication is in fact expected as when $t_{bc}=0$, the structure become a conventional FDSOI structure in which latch-up is practically eliminated.

6.6 Summary

The latch-up characteristics of a FDSOI CMOS inverter structure using the described BCSOI implantation-based SIMNI configuration was studied. With a body

contact opening underneath the channel region of both p- and n-MOS transistor, although silicon overlayer quality is able to be made comparable to those in bulk silicon structure, latch-up phenomena are unable to be avoided as in conventional FDSOI structure. The higher packing density feature in conventional FDSOI structure over bulk silicon structure are maintained in the BCSOI structure, thereby suggesting that the BCSOI structure are inherently less susceptible to latch-up than bulk silicon structure.

With regard to the BCSOI structure, latch-up susceptibility dependence on t_{in}, D_{nw}, S_{pn} and t_{bc} were examined in details. The simulation results show that latch-up is more difficult to be triggered on with smaller t_{bc}, deeper D_{nw}, larger S_{pn} and thicker t_{in}. Once the latch-up state is triggered on, the latch-up state is more likely to be sustained with bigger t_{bc}, shallower D_{nw}, smaller S_{pn} and thinner t_{in}.

From the point of view of device manufacturing, thick t_{in}, deep D_{nw} and large S_{pn} are constrained by cost; whereas small t_{bc} are constrained by process capability and controllability. To produce devices with lowest cost, it is more desirable to fabricate the devices with thinner t_{in}, shallower D_{nw}, and finer S_{pn}. Based on the simulation results, it is seen that performance of devices built on the BCSOI structure are undegraded with huge changes on configuration parameters. In other words, a wide latitude exists in processing devices on the BCSOI structure.

Chapter 7 Conclusions

This thesis basically covers the emergence of SOI technology and the applications of simulation software for detailed device simulations.

Under the consideration of emergence of SOI technology, the advantages of SOI devices, their classifications and manufacturing methods are concisely presented. In addition, the future trend of SOI technology and the quest for silicon-on-nitride structure are particularly highlighted. A fully depleted BCSOI structure using implantation-based SIMNI substrate is then described.

Under the consideration of device simulation software, the principle of device simulator MEDICI is described and was used in simulating the performance of devices built on various structure configurations. Based on the simulation results, devices performance are compared. Performance dependence on configuration parameters are also explored. Furthermore, latch-up characteristics of a CMOS invertor built on the BCSOI structure are investigated, giving rise to additional rationale in support of the BCSOI structure.

7.1 Summary

An nMOS transistor built on bulk silicon structure with long channel behaviour as verified by MEDICI software was created and became the basis of simulation comparisons. Conventional FDSOI structures, either having oxide or nitride as the insulator layer, are then directly constructed by adding the insulator layer command lines in the basic bulk silicon structure simulation source file. By

the same token, different command lines are employed in the basic source file to cater for the peculiar fully depleted BCSOI structure. Performance studying of the devices on the five different structures were then simulated.

Performance of a transistor can be evaluated by investigating its body effect, current-voltage characteristics, transconductance, subthreshold leakage current and subthreshold swing. These performance indices of each the transistor of the five respective structures were extracted for comparisons.

It was revealed that transistor on conventional FDSOI structure suffers from floating body effects, thereby limiting their working voltage. Nevertheless, below the breakdown voltage range, the transistor gives out highest transconductance, highest current output level, lowest body effect, lowest subthreshold leakage current and lowest S_t value. All these reaffirm the known advantages of conventional FDSOI devices.

The nMOS transistor built on the fully depleted BCSOI structure was found to be free of floating body effects. Transistors built on those structures do not break down at V_{dd}=5.0V and beyond. Although the overall performance of them are not as good as in conventional FDSOI structure, transistors on the BCSOI structure are superior to those on bulk silicon structure. Despite of using one additional mask, the overall processing cycling time and cost are estimated to be not exceeding those of conventional FDSOI structure. Above all, the fully depleted BCSOI structure enable the ease of oxidation after nitrogen implantation when constructing devices on nitride insulating structure using implantation method. All in all suggest that the fully depleted BCSOI structure is a viable alternative for consideration.

From the viewpoints of device manufacturing, performance of devices shall

have wide tolerance against variation in structure parameters change. Simulation of the dependence on structure parameters such as buried insulator thickness (t_{in}), silicon overlayer thickness (t_{si}) and body-contact size (t_{bc}) show that the overall performance of the nMOS transistor built on the BCSOI SIMNI structure are invariant to change of t_{in} or t_{si}. Yet, improved performance are found to be resulted from smaller t_{bc} opening. Nevertheless, the formation of small openings in a repeated manner would be difficult in the manufacturing's point of view. An opening of roughly the same as the channel length would be easier and already serve the purpose of floating body effect elimination.

The drawback of creating a buried contact is the introduction of latch-up susceptibility. Simulation confirms that latch-up exists in inverter on the BCSOI structure. Yet, the higher packing density advantage of conventional FDSOI structure over bulk silicon structure are also persevered in the BCSOI structure. Dependence of latch-up susceptibility on parameters such as buried insulator thickness (t_{in}), n-well junction depth (D_{nw}), separation between the p- and nMOS transistor (S_{pn}) and body-contact size (t_{bc}) suggest that inverter is more resistant to latch-up by making t_{in} thicker, D_{nw} deeper, S_{pn} wider and t_{bc} smaller. The upper limits is a matter of cost, however.

7.2 Recommendation

The simulation results in this work have presented researchers of SOI technology the starting point of constructing a BCSOI structure using SIMNI substrate and demonstrated the trend and baseline for devices performance optimization.

It is recommended to actually fabricate devices, including p- and nMOS transistor and CMOS inverter, on the said BCSOI structure. Upon characterizing the electrical behaviour of the fabricated devices, their performance can then be compared with the simulated results for verification. Difference in device performance, if any, can be accounted for. The actual fabrication cycle time can also be calculated.

Moreover, by fabricating different device structures, the junction capacitance of the BCSOI structure can also be quantified by direct measurements, rather than by purely estimation from junction model theory as demonstrated in this work. The envisaged good silicon overlayer quality of the BCSOI structure can also be examined by various methods.

Nevertheless, device fabrication not only is a costly and time-consuming process, it also requires state-of-the-art technique and facilities. Nitrogen implantation is a special process. Only few institution or industrial factory in Hong Kong is capable of performing nitrogen implantation for SIMNI substrate preparation. The situation is more complicated if sub-micron geometry device design is sought for. In spite of the difficulties, it is encouraging to know that researches on SOI topic have been on-going in Hong Kong already.

Appendix A

Example of a Source File

To employ MEDICI for device simulation, a source file prepared to the specified format shall be available beforehand.

In previous chapters, portions of the source file for a nMOS transistor built on bulk silicon structure have been described. While the most detailed reference of how to use MEDICI shall be referred to the MEDICI manual, the key items of a source file of the said device will be remarked in this Appendix. The device described in the source file are constructed with the following parameters:

Transistor type	:	n-type
Channel length	:	1.2μm
Gate oxide thickness	:	250Å
Gate material	:	polysilicon, n-type doped
Substrate	:	p-type, 5.5E16/cm^3
Source/drain (n^+) depth	:	0.1μm
Source/drain (n^+) conc.	:	9.0E20/cm^3
Source/drain (n^-) depth	:	0.07μm
Source/drain (n^-) conc.	:	9.0E17/cm^3
Interface charge	:	1.0E10/cm^3

Example of the source file that describe the nMOS transistor built on bulk silicon substrate is listed as follows:

```
TITLE       1.2um Bulk NMOS (LDD) Structure

COMMENT     Specify a 2.2um x 2.0um rectangular mesh
MESH        RECTANGU SMOOTH=1
X.MESH      WIDTH=0.4  H1=0.1
X.MESH      WIDTH=0.2  H1=0.02
X.MESH      WIDTH=1.0  H1=0.1
X.MESH      WIDTH=0.2  H1=0.02
X.MESH      WIDTH=0.4  H1=0.1

Y.MESH      N=1  L=-0.025
Y.MESH      N=5  L=0
Y.MESH      DEPTH=0.20 H1=0.02
Y.MESH      DEPTH=0.25  H1=0.05
Y.MESH      DEPTH=1.55 H1=0.1 RATIO=1.2

COMMENT     Eliminate some unnecessary substrate nodes
ELIMIN      ROWS  X.MIN=0.4 X.MAX=0.6 Y.MIN=0.25 Y.MAX=0.4
ELIMIN      ROWS  X.MIN=1.8 X.MAX=2.0 Y.MIN=0.25 Y.MAX=0.4
ELIMIN      COLUMNS Y.MIN=1.0

COMMENT     Specify oxide and silicon regions
REGION      NUM=1  SILICON
REGION      NUM=2  OXIDE IY.MAX=5

COMMENT     Electrodes: #1=Gate, #2=Substrate, #3=Source, #4=Drain
ELECTR      NUM=1  X.MIN=0.5  X.MAX=1.7 TOP
ELECTR      NUM=2  BOTTOM
ELECTR      NUM=3  X.MAX=0.30  IY.MAX=5
ELECTR      NUM=4  X.MIN=1.90  IY.MAX=5

COMMENT     Specify Substrate, Channel Impurity Profiles
PROFILE     P-TYPE  N.PEAK=5.5E16  UNIFORM     OUTF=NMOS

COMMENT     Specify N- Impurity Profiles
PROFILE     N-TYPE Y.JUNC=0.07  N.PEAK=9.0E17 X.PEAK=0.0 WIDTH=0.5
+           XY.RAT=0.7
PROFILE     N-TYPE Y.JUNC=0.07  N.PEAK=9.0E17 X.PEAK=1.7 WIDTH=0.5
+           XY.RAT=0.7

COMMENT     Specify N+ Impurity Profiles
PROFILE     N-TYPE Y.JUNC=0.1 N.PEAK=9E20 X.PEAK=0.0  WIDTH=0.35
+           XY.RAT=0.8
PROFILE     N-TYPE Y.JUNC=0.1 N.PEAK=9E20 X.PEAK=1.85 WIDTH=0.35
+           XY.RAT=0.8

COMMENT     Specify contact parameters
CONTACT     NUM=1  N.POLY

INTERFAC    QF=1E10

COMMENT     Initial grid structure display
FILL        SET.COLO C.NITRID=6 C.SILIC=-1 C.OXIDE=5 C.POLYSI=3
PLOT.2D     GRID  TITLE="Bulk Silicon NMOS - Initial Grid" FILL  Y.MAX=0.6

COMMENT     Regrid on doping
REGRID      DOPING LOG IGNORE=2 RATIO=2 SMOOTH=1 DOPF=NMOS
```

```
PLOT.2D         GRID FILL Y.MAX=0.6
+               TITLE="Bulk Silicon NMOS - Doping Regrid"

COMMENT         Specify physical models to use
MODELS          CONMOB  FLDMOB  SRFMOB2

COMMENT         Symbolic factorization, solve, regrid on potential
SYMB            CARRIERS=0
METHOD          ICCG  DAMPED
SOLVE

REGRID          POTEN IGNORE=2 RATIO=.2 MAX=1 SMOOTH=1 DOPF=NMOS
+               OUTF=NMOSD
PLOT.2D         GRID TITLE="Bulk Silicon NMOS - Potential Regrid"
+               FILL  Y.MAX=0.6

COMMENT         Impurity profile plots
PLOT.1D         DOPING  X.START=.2  X.END=.2 Y.START=0  Y.END=0.6
+               Y.LOG  POINTS  BOT=1E14  TOP=1E21  COLOR=2
+               TITLE="Bulk Silicon NMOS - Source Profile"

COMMENT         Impurity distribution plot
PLOT.3D         DOPING LOG TITLE="Bulk Silicon NMOS" Y.MAX=0.6
3D.SURF

COMMENT         Solve using the refined grid, save solution for later use
SYMB            CARRIERS=0
SOLVE           OUTF=NMOSGC
```

Example of the source file for a nMOS built on bulk silicon substrate

Every source file starts with **TITLE** command which specify the title of the file. Throughout the source file, **COMMENT** command can be placed at anywhere desired. Information follows **COMMENT** is not executed and is regarded as remarks in MEDICI.

Discretization is inevitable when employing computer for device simulations simulations. The command for grid assignment in MEDICI program is **MESH**. A rectangular mesh is firstly assigned. The density of grid along the x- and y-directions are assigned by commands **X.MESH** and **Y.MESH** respectively. To speed up computation rate, reductant or unnecessary grid nodes can be eliminated by **ELIMIN** command at specified rows or columns.

Command **REGION** is used to define the only two regions, namely oxide and silicon, that exist in a bulk silicon nMOS transistor structure.

The size of the designed gate channel length, its position, together with the placement of the source, drain and substrate electrodes are then defined by command **ELECTR.**

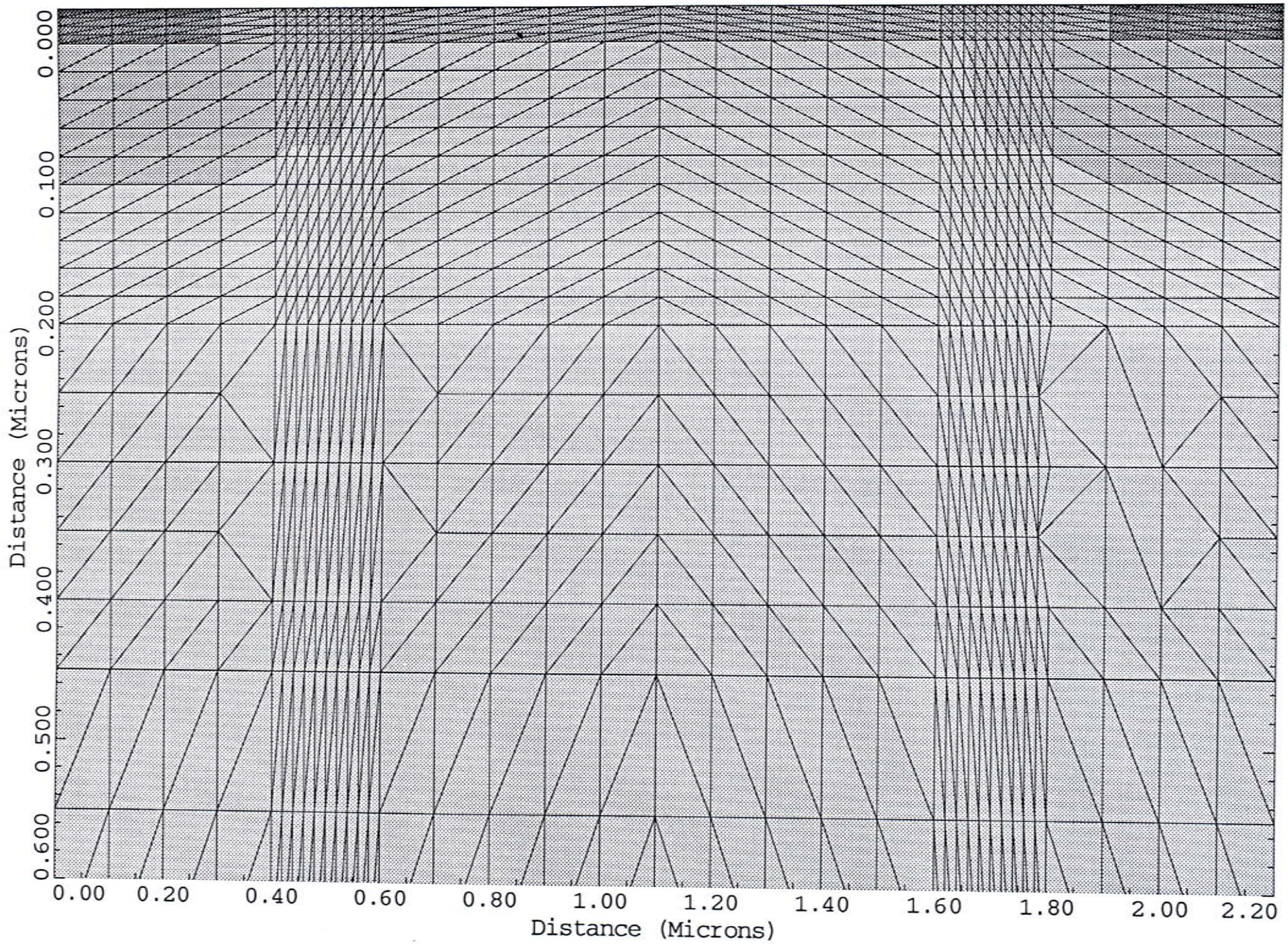
Impurity distributions in the structure are defined by **PROFILE** command. The specification is made by defining the junction depth, peak concentration, position and lateral diffusion ratio. The concentration of interface charges that exist in the oxide layer is defined by command **INTERFAC.** Finally, the gate material is set by **CONTACT** command in which n-type polysilicon material is called for.

The advantage of MEDICI is the capability of re-allocating the initial grid assignment to match with the user-defined device structure by using **REGRID** command. The regrid may either follow impurity doping distribution, a doping regrid, or potential distribution, a potential regrid.

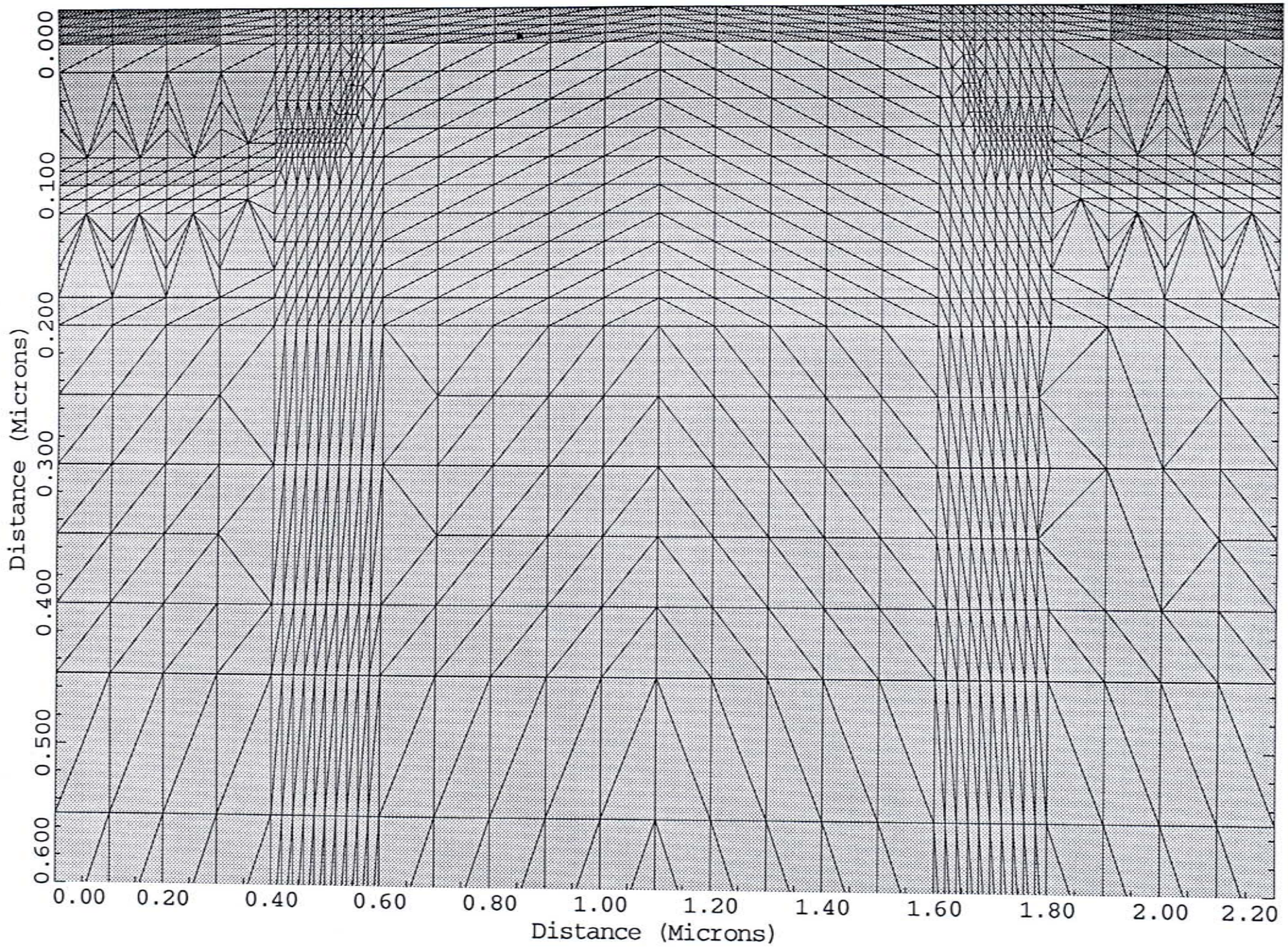
Following the regrid, initial solution can be surmounted by **SOLVE** command upon specifying the solution method by **METHOD** command and the number of carrier under simulation by **SYMB** command.

After all the structure parameters are defined, the structure can be visualized by invoking **PLOT.1D, PLOT.2D** and **PLOT.3D** commands. Different views of the structure can be obtained by specifying the corresponding requirements. Examples of the figure are attached. The figures interested are the initial grid assignment, the grid appearance after doping regrid, the grid appearance after potential regrid, the doping profile at the source region and a 3-dimensional view of the doping distribution of the entire structure.

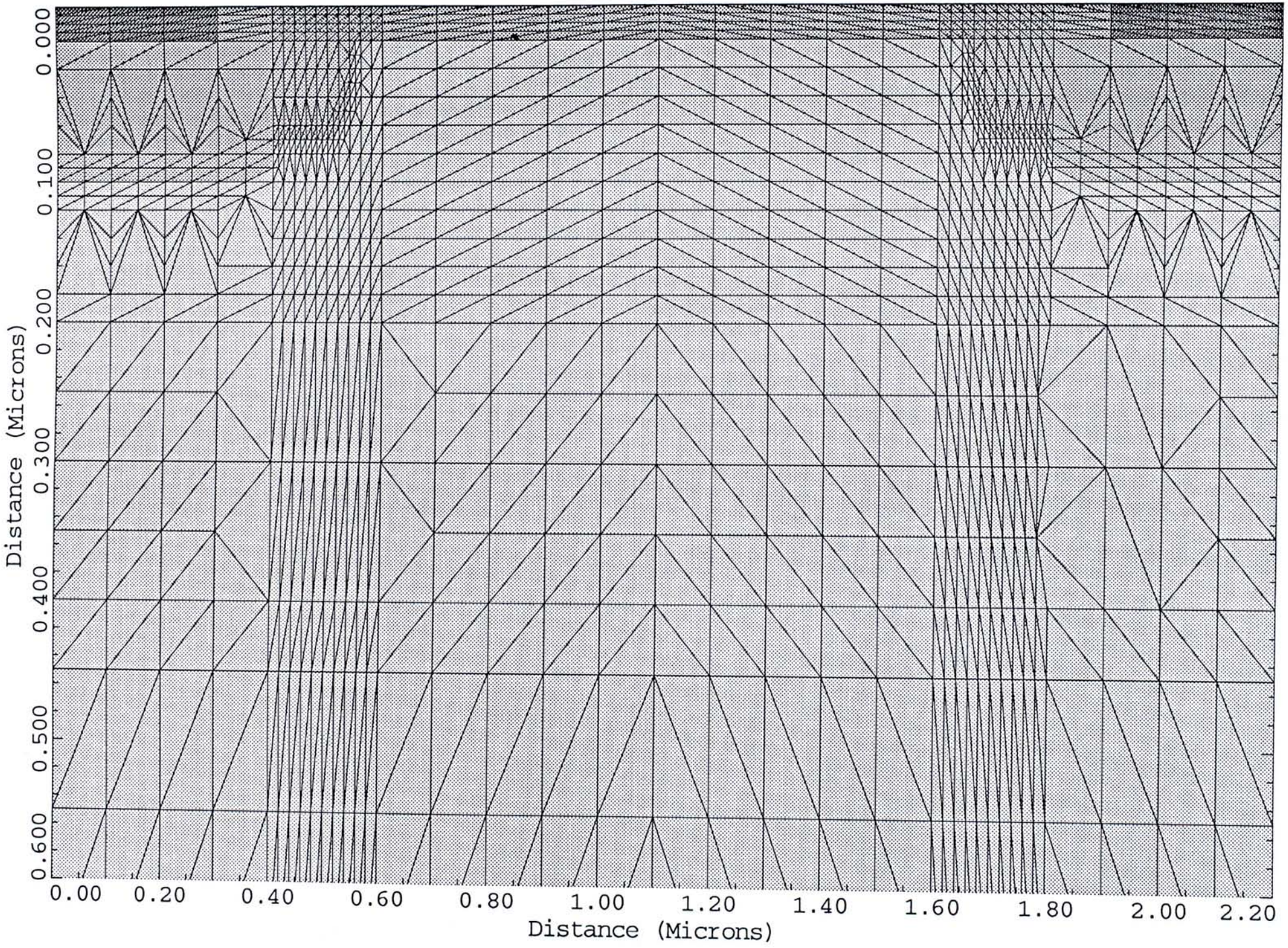
Bulk Silicon NMOS - Initial Grid



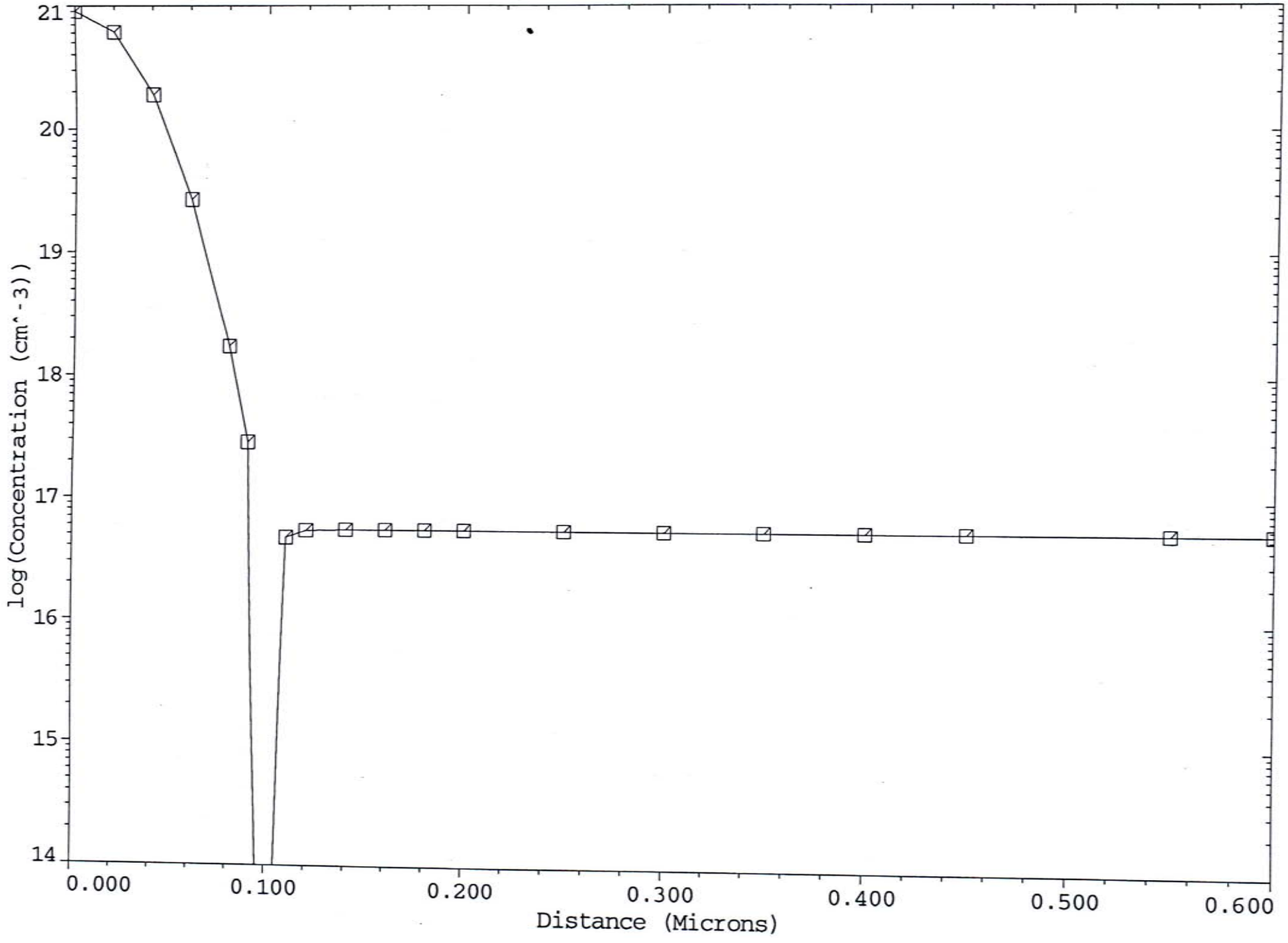
Bulk Silicon NMOS - Doping Regrid



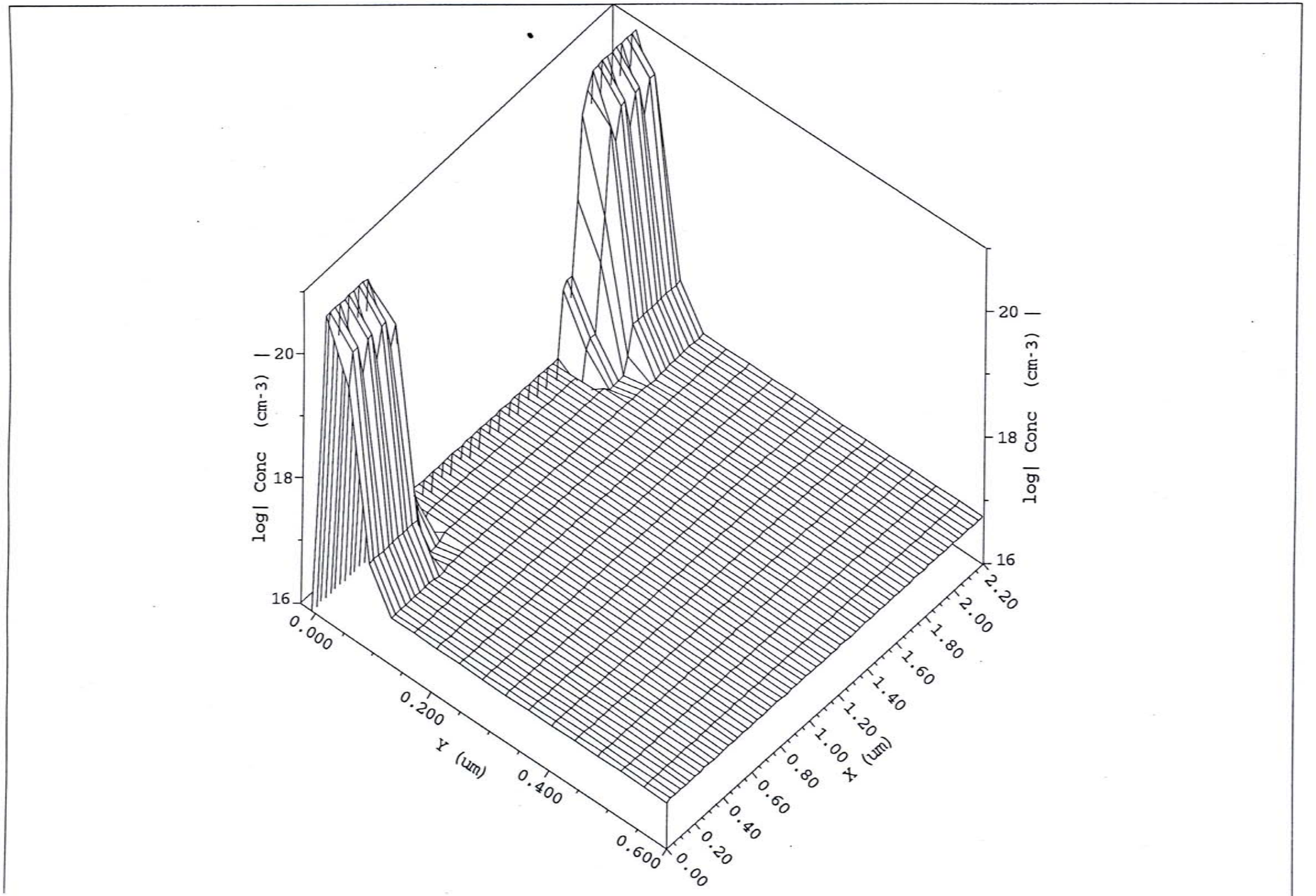
Bulk Silicon NMOS - Potential Regrid



Source Impurity Profile



Bulk Silicon NMOS



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