Operational Transconductance Amplifier with a Rail-to-rail Constant Transconductance Input Stage

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Abstract

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Operational Transconductance Amplifier with a Rail-to-rail Constant Transconductance Input Stage

Submitted by CHAN Shek Hang

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The demands for low-voltage and low-power integrated circuits have an enormous impact on the dynamic range of amplifiers. On the up side, the dynamic range is lowered because of the lower input signal voltages. On the down side, it is reduced because of the larger noise voltages due to the smaller supply currents. In order to maximize the dynamic range, a low-voltage amplifier must be able to deal with signal voltages that extend from rail-to-rail.

This thesis presents the design of a single stage operational transconductance amplifier with a rail-to-rail constant transconductance input stage. A new constant-g_m bias circuit architecture is proposed and successfully implemented. It is fabricated in low-cost commercial CMOS 0.6μm process. We have found that the measurement results show good conformity with the simulation results. The OTA is designed to work at a 3V supply voltage.

The proposed architecture can achieve a constant overall transconductance over the whole common mode range with only 6.54%

variation. To the best of our knowledge, this is the lowest variations of g_m ever reported for CMOS opamp operating in saturation region. The total harmonic distortion is only 0.033% which is smaller than the conventional architecture.

The circuit area is only 212μm × 120μm and the power consumption is only 0.85mW. Even this is just a single stage OTA but we still can achieve an open-loop gain of 65.8dB at such a low power consumption level.

摘要

集成電路的低電壓低功耗的要求對放大器的動態工作範圍具有非常巨大的影響。在高電壓部分，因爲所允許的信號電壓較低，動態工作範圍就比較小。在低電壓部分，因爲比較小的電流所引起的比較大的電壓噪聲，動態工作範圍也比較小。爲了使這個動態範圍最大化，一個低壓放大器一定要能處理全電壓範圍信號。

這篇論文介紹了一個全電壓範圍的常跨導輸入級的單級運算跨導放大器的設計。在這個設計中提出了一個新的常量跨導偏置電路結構並且實現了。它用低成本的商業 CMOS 0.6um 過程製造。我們已經發現測試結果很好地支持了模擬的結果。這個 OTA 是設計在 3V 電壓下工作的。

這個結構能夠達到一個在整個共態範圍上整體恆定的跨導，它僅僅有 6.54%變化，根據我們的認知,這個結果應該是目前最低的跨導變化。總諧波失真亦只有 0.033%，比傳統的結構要小得多。

這個電路只有 212umX120um 大，功耗只有 0.85mW。即使這只是一個單級 OTA,但是在這樣一個低功耗的水平下我們還是可以獲得一個 65.8dB 的開環增益。

Acknowledgement

I am grateful to my supervisor, Professor Chan Cheong Fat, for his patient guidance in these few years. He has given me much invaluable opinions and encouraged me on this project.

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Chapter 1 Introduction

1.1 Overview

We have been targeting to reduce the supply voltage and power of mixed analog-digital integrated circuits for the past ten years. The maximum allowable power supply voltage is reduced from 5V to 3.3V. This is primarily due to the increasing demand of battery powered electronics, and a continuing down-scaling of device sizes [1] [2].

The low-voltage and low-power digital circuits, on the one hand, can easily obtain good processing qualities, such as high accuracy and good signal-to-noise ratio [3]. In addition, the size of digital circuit drastically reduces with smaller features sizes. On the other hand, low-voltage and low-power analog circuits with good processing qualities are more difficult to obtain. For instance, the dynamic range of an operational amplifier substantially decreases when the supply voltage is reduced. Furthermore, analog circuits cannot be designed using minimum size devices, for reasons of gain, offset, noise etc. As a consequence, the chip area of analog circuits cannot be drastically reduced with smaller feature sizes.

The low-voltage and low-power demand has an enormous impact on the dynamic range of an amplifier. On the up side, the dynamic range is lowered because of the lower input signal voltages. On the down side, the dynamic range is reduced because of the larger noise voltages due to the smaller supply currents. In order to maximize the dynamic range, a low-voltage amplifier must be able to deal with signal voltages that extend from rail-to-rail. This thesis is focused on the design of 3V operational

transconductance amplifier (OTA) with a rail-to-rail constant transconductance input stage. The simplest way to obtain rail-to-rail input stage is to place an N-channel and a P-channel differential pairs in parallel [4] as indicated in Figure 1.1.

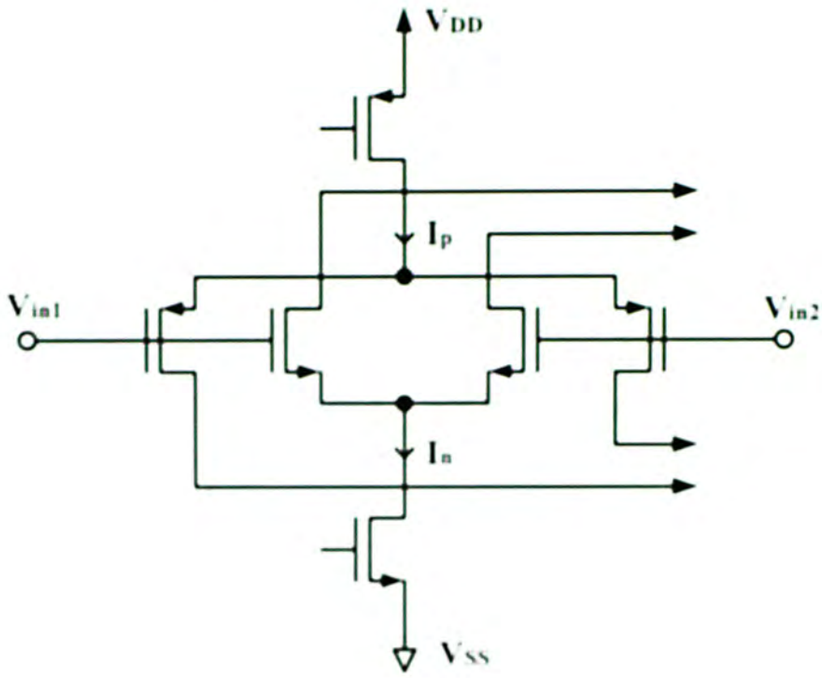

Figure 1.1 Rail-to-rail input stage

1.2 Significance of the research

In the past few years, operational transconductance amplifier-capacitor (OTA-C) filters or $g_m - C$ filters [5][6][7] have been implemented in MOS technology. Since a $g_m - C$ filter utilizes the transconductance (g_m) of an OTA to evaluate time constant, the circuit can be operated at much higher frequencies compared to opamp based filters. However, because OTAs are used in an open loop manner, their linear input range directly affects the dynamic range of the entire filter. Moreover, the time constant determining parameter, g_m, is dependent on

the MOS transistor parameters, thus the time constant is not as accurate as in opamp based SC-filters.

The significance contribution of this research is a new circuit design technique which enables rail-to-rail operation without any performance degradation on g_m.

1.3 Objectives

In this project, design and implementation of operational transconductance amplifier (OTA) with constant g_m input stage is designed and demonstrated.

The following are the design criteria:

- Operating at supply voltage 3V – as 3.3V power supply will be a standard for commercial digital integrated circuit, this opamp should be operated at 3V (assuming 10% error).
- Rail-to-rail input range – the dynamic range of opamp is limited by the input range, so a rail-to-rail input range is needed to maximize the dynamic range.
- Constant overall transconductance (g_{mT}) of the input stage – a rail-to-rail input stage suffers from a large variation (about) 100% of the g_{mT} across the input common-mode range. This makes it difficult to optimize the compensation network, so a constant g_{mT} input stage is needed.
- 10pf loading capacitance – the value of load capacitance will affect the maximum operating frequency of the OTA. Thus, we have assumed a maximum load capacitance of 10pf.

- The OTA should operate in strong inversion – for a given drain current and device geometry, weak inversion mode is attractive when minimal offset voltage is important, whilst strong inversion mode must be used where high speed and high gain are required.
- Low total harmonic distortion (THD) – THD is the easiest way to look at the effect on the variation of g_{mT} at the voltage follower configuration.

1.4 Thesis outline

The operating principle and background theory of MOS transistor and rail-to-rail opamp are discussed in Chapter 2, followed by the needs and problems caused by the rail-to-rail opamp.

Chapter 3 will give an overview of different published architectures on the transconductance control circuit. The principles and performance of different architectures will be presented.

In chapter4, the basic principle of using translinear loop to control the overall transconductance will be presented. After that it will be the principle of the proposed architecture. Chapter 5 will cover all the simulation results of the proposed OTA.

Chapter 6 will discuss the layout issues. All the measurement results of the proposed OTA will be given in chapter 7.

Finally, Chapter 8 will give a concise conclusion of the research and contributions . The appendix and bibliography are put in chapter 9 and 10 respectively.

Chapter 2 Background theory

2.1 Introduction

In this chapter, the electrical properties of MOS transistor will be discussed which is used to explain the reason of choosing the operation region of the MOS transistors of this project. The needs for rail-to-rail input range will be analyzed. A conventional rail-to-rail input stage and the problems associate with it will be presented. At the end of this chapter, the nature of opamp distortion will be focused.

2.2 Electrical properties of MOS transistors

Gate-source voltage is the most important electrical property of an MOS transistor for low voltage design, because it determines the minimum supply voltage of the amplifier and the transconductance of the transistor.

2.2.1 Strong inversion

A MOS transistor is operating in strong inversion region when its gate-source voltage is larger than the threshold voltage.

$$|V_{gs}| \geq |V_{th}| \tag{2.1}$$

In this region the transistor (both nmos and pmos) saturates when

$$|V_{ds}| \geq |V_{gs} - V_{th}| \tag{2.2}$$

where V_{ds} and V_{th} are the drain-source voltage and the threshold voltage, respectively. The drain-source voltage at which a transistor begins to saturate is called the saturation voltage, V_{dsat}.

In saturation, the relation between the drain current, I_{ds} and the gate-source voltage, V_{gs} is expressed by [8]

$$I_{ds} = \frac{1}{2}\frac{W}{L}\frac{\mu C_{OX}}{1+(V_{gs}-V_T)\left(\Theta+\frac{\xi}{L}\right)}(V_{gs}-V_T)^2 \tag{2.3}$$

Where μ is the mobility of the charge carriers, C_{ox} is the normalized oxide capacitance, V_{gs} is the gate-source voltage, and V_T is the threshold voltage. W and L are the width and the length, respectively. The parameter Θ models the effect of the gate electrical field, while ξ expresses the effect of the source-drain electrical field. Typical values of Θ and ξ are 0.1 V^{-1} and 0.3 $\mu m/V$, respectively [9].

A key small-signal parameter of a MOS transistor is the transconductance. It can be determined by differentiating the drain current of a transistor with respect to the gate-source voltage.

$$g_m = \sqrt{2\mu C_{OX}\frac{W}{L}I_d} \tag{2.4}$$

The g_m of the transistor can be increased by increasing the W/L ratio and the drain current. In this way, the transconductance increases with a factor n.

2.2.2 Weak inversion

A MOS transistor operates in weak inversion region, or subthreshold region, when its gate-source voltage is slightly below the threshold

voltage.

$$|V_{gs}| < |V_{th}| \tag{2.5}$$

In this region, the transistor saturates when

$$V_{ds} > 3 \text{ to } 4\, V_{tm} \tag{2.6}$$

where V_{tm} is the thermal voltage, kT/q, which is about 25 mV at room temperature. In general, the saturation voltage of a MOS transistor operating in weak inversion is lower than that of a device working in strong inversion.

In the saturation region, the relation between the drain current and the gate-source voltage of a MOS transistor operating in weak inversion can be described by [10]

$$I_{ds} = I_S e^{\frac{V_{gs}-V_T}{nV_{tm}}} \tag{2.7}$$

Where n is the weak inversion slope factor and I_S is the specific current, which is given by

$$I_S = 2n\mu C_{OX} V_{tm}^2 \frac{W}{L} \tag{2.8}$$

Typical values of I_S are between 2 nA to 200 nA [10].

The transconductance of a MOS transistor operating in weak inversion is given by

$$g_m = \frac{I_{ds}}{nV_{tm}} \tag{2.9}$$

We can conclude from this formula that g_m of a MOS transistor operating in weak inversion only depends on the drain current. If a transistor requires a larger transconductance, the drain current of the transistor has to be increased. However, if the drain current is increased too much, the transistor ends up in strong inversion. Although the transistor can be kept

in weak inversion by increasing the W/L ratio, however, increasing W/L will also increases the parasitic capacitances of the device, that will reduce the bandwidth of the circuit.

2.2.3 Moderate inversion

In practice, there is a smooth transition region between weak and strong inversion regions, which is called moderate inversion. By approximation, the transistor is in moderate inversion region when the drain current is between $1/8I_s$ and $8I_s$ [11].

$$\frac{1}{8}I_S < I_{ds} < 8I_S \tag{2.10}$$

2.2.4 The transistors biased in this work

In this work, all the transistors, including the input differential pairs, are biased in the strong inversion region. It is because this provides the largest voltage gain for a given drain current and device geometry.

2.3 Rail-to-rail signals

In this thesis, we want to have a rail-to-rail input stage so as to maximize the common mode input range. This will be discussed, employing two widely used opamp applications, the inverting and the non-inverting feedback configuration.

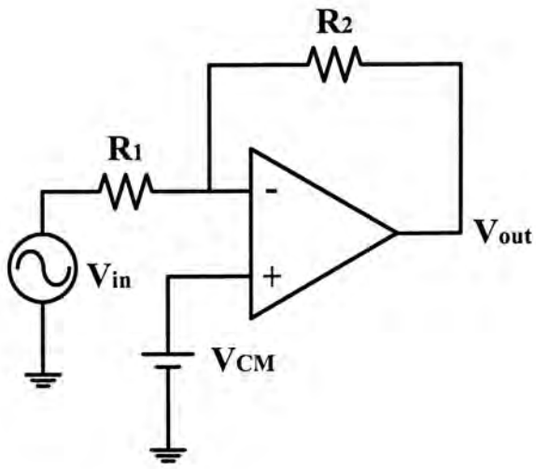

Figure 2.1: Inverting amplifier

Figure 2.1 shows an inverting amplifier, with a gain of

$$A_{inv} = \frac{V_{out}}{V_{in}} = -\frac{R_2}{R_1} \tag{2.11}$$

The demand on common mode input voltage range is more relaxed. This range can be small because the positive input of the amplifier is biased at a fixed voltage. Although, this input V_{CM} can be biased at any voltage, it is usually biased at half of the supply voltage to maximize positive and negative voltage swing.

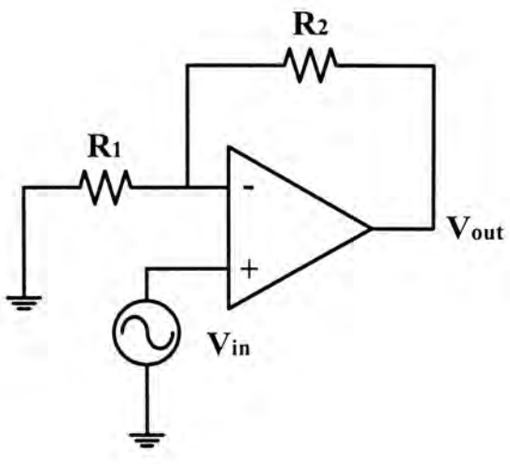

Figure 2.2: Non-inverting amplifier

Figure 2.2 shows another frequently used application, an amplifier connected in a non-inverting feedback configuration. In system design, this configuration is frequently used for buffering or signal amplification. The non-inverting feedback amplifier has a gain of

$$A_{non-inv} = \frac{V_{out}}{V_{in}} = 1 + \frac{R_2}{R_1} \tag{2.12}$$

The demand on the common mode input range are less relaxed than the inverting amplifier. Since the input is connected to the positive terminal thus the common mode voltage is equal to the input signal. Assuming the output voltage can swing from rail to rail, we can calculate the maximum common mode input voltage

$$V_{CM} = \frac{V_{out}}{A_{non-inv}} = \frac{V_{DD} - V_{SS}}{A_{non-inv}} \tag{2.13}$$

It can be concluded that the common mode input range has to increase when the gain decreases. In the limiting case, the non-inverting amplifier operates with a gain of one, thus, the input common mode voltage must equal to V_{DD}-V_{SS}.

2.4 Rail-to-rail operational amplifier

2.4.1 Rail-to-rail differential input pairs

2.4.1.1 Principle

The input stage of a rail-to-rail amplifier is shown in Figure 2.3. The circuit requires both N-channel and P-channel input stages to achieve full rail-to-rail operation [12].

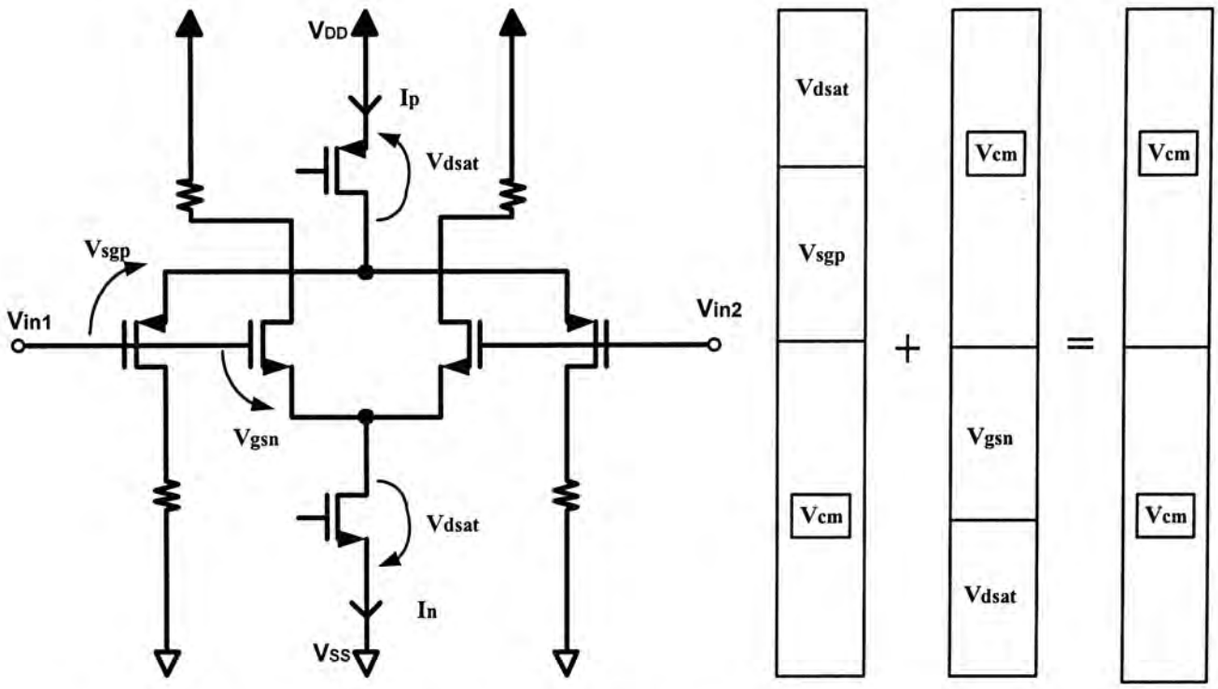

Figure 2.3: Common mode input range of a rail-to-rail input stage

The N-channel input pair is able to reach the positive supply rail while the P-channel one can operate at the negative supply rail. In order to ensure a full rail-to-rail common mode input range, the supply voltage of the rail-to-rail input stage must satisfy the following condition:

$$V_{DD} - V_{SS} = V_{sgp} + V_{gsn} + 2Vdsat \tag{2.14}$$

The common mode input voltage range can be divided into the following three operating regions:

- Low common mode input voltages: only the P-channel input pair is operating.
- Intermediate common mode input voltages: both P-channel and N-channel input pairs are operating.
- High common mode input voltages: only the N-channel input pair is operating.

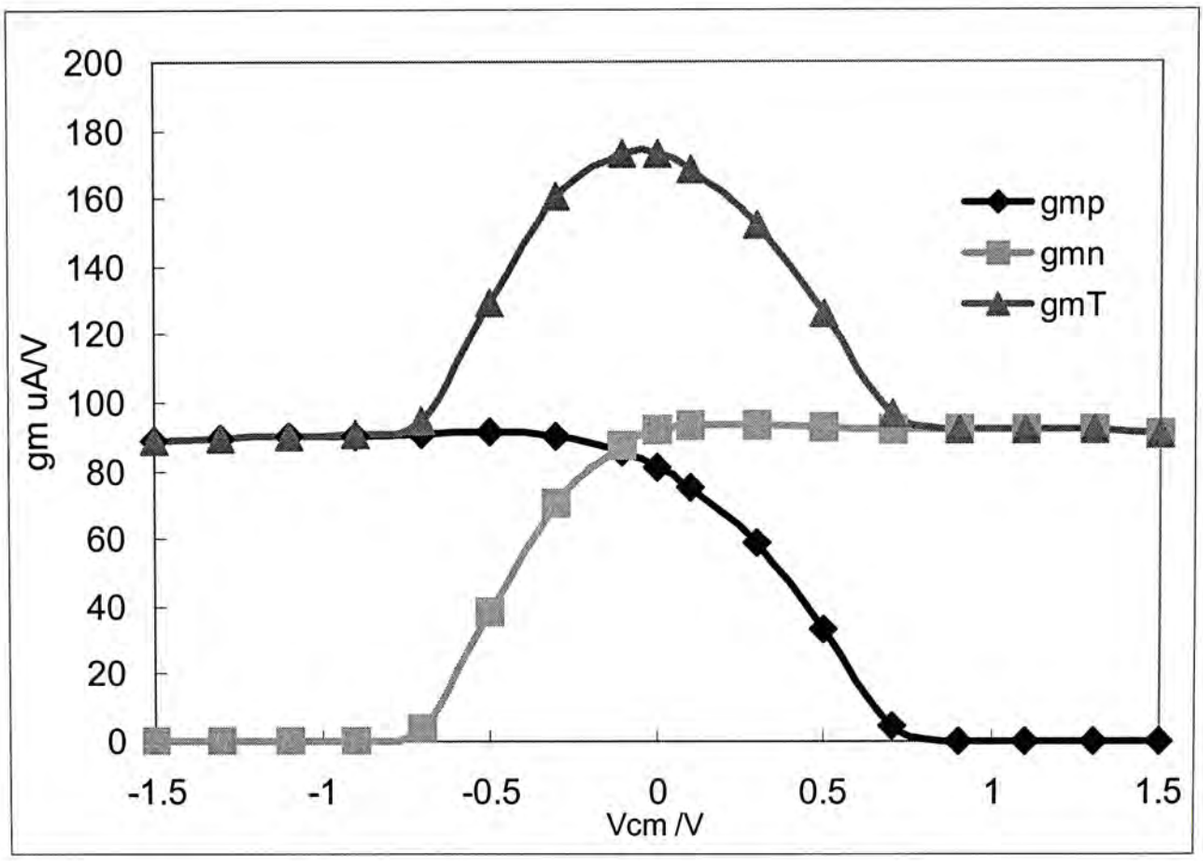

Figure 2.4: Transconductance of a rail-to-rail CMOS input stage as a function of the common mode input voltage

Figure 2.4 shows the simulated transconductance g_m of the input stage operating between +/-1.5V. For low common mode input voltage (i.e. from –1.5V to –0.9V), as only the P-channel pair is on so the g_m of N-channel is nearly zero. On the other hand for the high common mode input voltage (i.e. from 0.9V to 1.5V), as only the N-channel pair is on so the g_m of P-channel is nearly zero. In intermediate common mode input voltage, both pairs operate at the same time so the overall transconductance g_{mT} (by equation (2.15)) is almost double when compare to only one pair is operating.

$$g_{mT} = g_{mn} + g_{mp} \tag{2.15}$$

2.4.1.2 *Two stage operational amplifier*

A block diagram of an ideal opamp model and a small signal model are in Figure 2.5 and Figure 2.6. The input resistance R_{in} is considered to be infinite and the input signal $v_{in} = V_+ - V_-$.

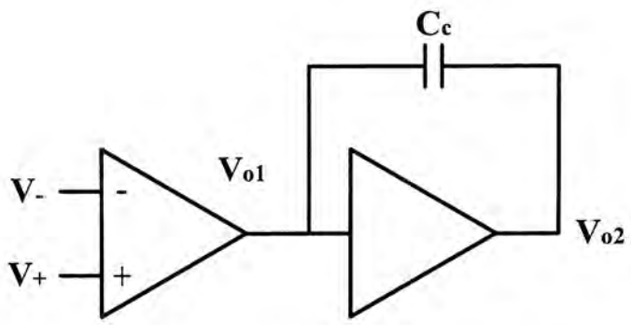

Figure 2.5: A block diagram of a two stage opamp

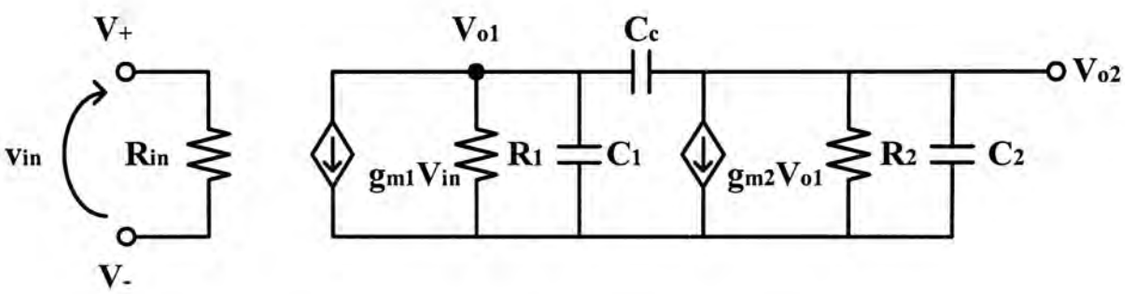

Figure 2.6: Small signal model of a two stage opamp

We can derive the following opamp characteristics.

$$A_V = g_{m1} g_{m2} R_1 R_2 \tag{2.16}$$

$$P_1 = -\frac{1}{g_{m2} R_1 R_2 C_C} \tag{2.17}$$

$$P_2 = -\frac{g_{m2}}{C_2} \tag{2.18}$$

$$Z_1 = \frac{g_{m2}}{C_C} \tag{2.19}$$

Where A_V is the signal gain, P_1 and P_2 are the first (dominant) and the

second poles, and Z_1 is the right hand plane zero. Assuming that P_2 is located at a very high frequency, then the unity gain frequency, ω_u, is given by

$$\omega_U = A_V P_1 = \frac{g_{m1}}{C_C} \tag{2.20}$$

In order to maintain a sufficient amount of phase margin, P_2 must be placed at about two and half times ω_u. In other words, for a given g_{m1} and P_2, C_C should be chosen such that $\omega_u = P_2/2.5$ to maximize the opamp gain-bandwidth while maintaining a good opamp performance. All this would be possible provided that g_{m1} is constant regardless of the value of the large signal, V_{CM}. However, we have shown in the previous section that g_{m1} can change by as much as 100% for a rail-to-rail opamp. From the equations (2.16) - (2.20), we know that g_{m1} affects many opamp performance criteria. Thus, it is very important to design an opamp with a constant g_{m1}.

2.4.2 Folded-cascode gain stage

In order to achieve a high gain one stage opamp, we can use the folded-cascode architecture. The block diagram of the one stage opamp is shown in Figure 2.7.

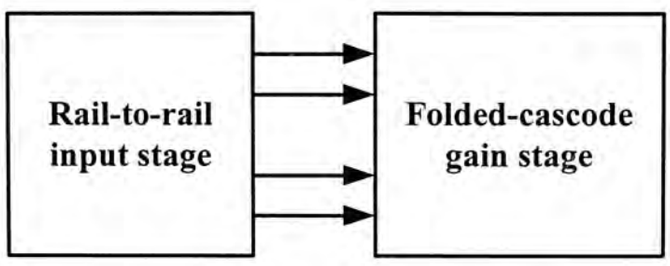

Figure 2.7: Block diagram of the one stage opamp used

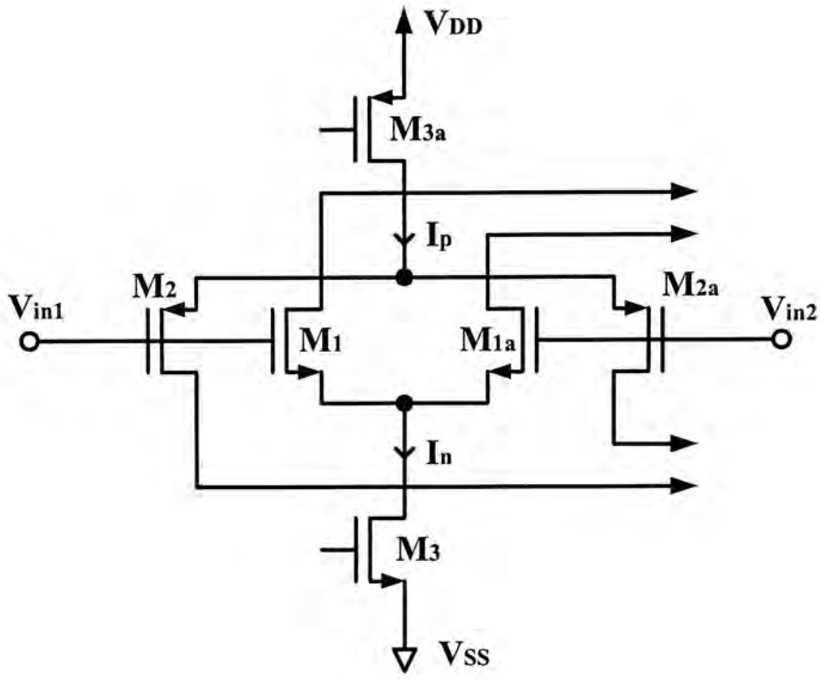

Figure 2.8: Rail-to-rail input stage

The rail-to-rail input stage is shown in Figure 2.8, where M_1 M_{1a} and M_2 M_{2a} are the input pairs to achieve rail-to-rail, and M_3 M_{3a} providing dc bias for the input pairs. Instead of using a conventional folded-cascode gain stage, a self-biased complementary folded-cascode stage[13] is used as shown in Figure 2.9. The advantage of this configuration is that no external bias network is needed, and it is fortunate to apply this design at 3V supply.

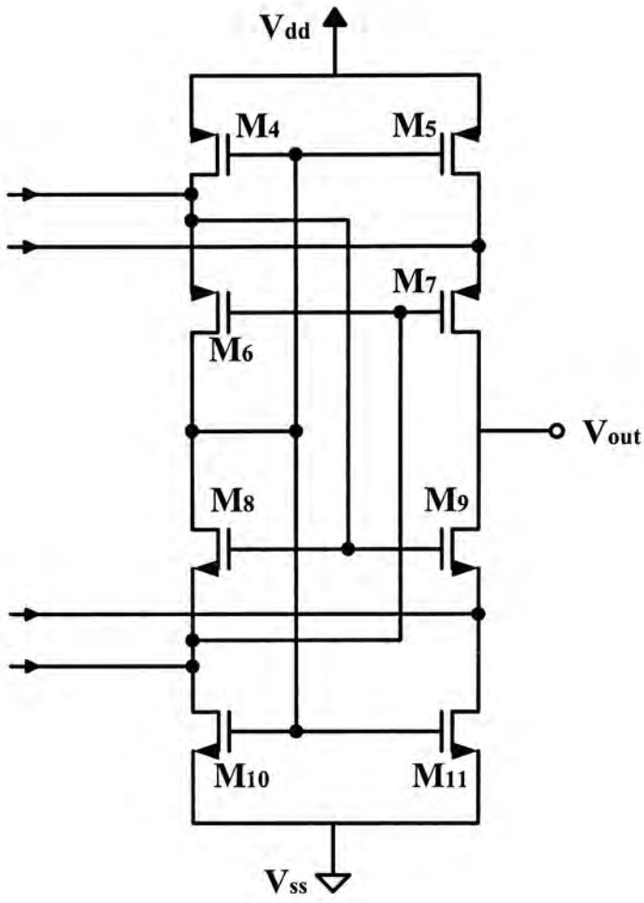

Figure 2.9: Self-biased complementary folded-cascode gain stage

2.5 The nature of operational amplifier distortion

Numerous practical limitations introduce distortion in an opamp. The nonlinear transfer characteristics of transistors, the voltage coefficients of junction capacitances, the hyperbolic responses of differential stages, thermal feedback, and other effects produce distortion. Fortunately, the feedback circuit of the opamp expresses most of these unwanted effects. We cab easily calculated an input-referred error, and knowing this input-referred error for a given opamp permits the prediction of output

distortion.

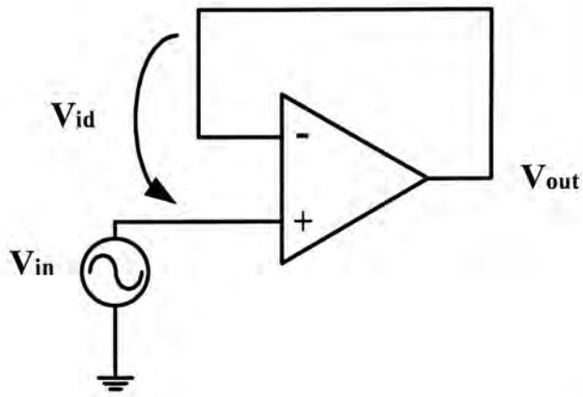

Figure 2.10: Unity gain connected opamp

The voltage follower (Figure 2.10) demonstrates the input-referred error. The input signal v_{in} produces an approximately equal output signal v_{out} plus an differential input error signal v_{id}. For this circuit, a simple loop equation locates any distortion introduced by the opamp through

$$v_{out} = v_{in} - v_{id} \tag{2.21}$$

As trivial as this equation seems, it demonstrates the concept of input-referred error. Distortion introduced by the opamp produces a difference between the follower's input and output signals. This equation states that the output signal v_{out} remains a replica of the input signal v_{in} plus an input error signal v_{id}. Thus v_{id} must include all distortions introduced by the amplifier.

2.5.1 The total harmonic distortion

The easiest way to see the effects of non-constant transconductance (g_{mT}) on the circuit is to look at the total harmonic distortion (THD) [14] consider the unity gain connected opamp (Figure 2.10). If $v_{in} = A_M \sin$

(2000ωt) is applied to the positive input terminal of an opamp with a direct feedback from the output terminal to the negative input terminal. This input voltage is the common mode input voltage which affects gm_T (Figure 2.4). Let the gain of the opamp be given by

$$A(v_{in}) = g_{mT}(v_{in})R_O \tag{2.22}$$

Where R_O is the output resistance. Then the output voltage is given by

$$v_O = \frac{A(v_{in})v_{in}}{1+A(v_{in})} = F(v_{in}) \tag{2.23}$$

This can be expanded into

$$v_O = F(0) + F'(0)v_{in} + F''(0)\frac{v^2(in)}{2} + \ldots \tag{2.24}$$

where the coefficients F"(0), F"(0)/2, etc. are used to determine THD, and they can be easily calculated as follows.

$$F(0) = 0 \tag{2.25}$$

$$F'(0) = \frac{A(0)}{1+A(0)} \tag{2.26}$$

$$F''(0) = \frac{2A'(0)}{(1+A(0))^2} \tag{2.27}$$

$$\vdots$$

Note that since the ideal expression for the output voltage is $v_o = v_{in}$, A(0) should be as large as possible. Moreover, in order to minimize the distortion caused by input voltage, opamp gain A(0) must be much larger than A'(0) and the other higher derivatives; in other words, the more constant $A(v_{in})$ or $g_{mT}(v_{in})$ becomes, the less distortion the input stage would cause.

The total harmonic distortion (THD) is defined as 100% times the rms sum of all distortion harmonics (Figure 2.11) divided by the rms value of the signal fundamental. In equation form,

$$THD = \frac{\sqrt{E_2^2 + E_3^2 + E_4^2 + E_5^2 + ... + +E_n^2}}{E_1} \times 100\% \quad (2.28)$$

Here E_1 represents the fundamental and E_2 through E_n represent the harmonics. In each case, the capital letter E represents the rms value of the signal, rather than the instantaneous value.

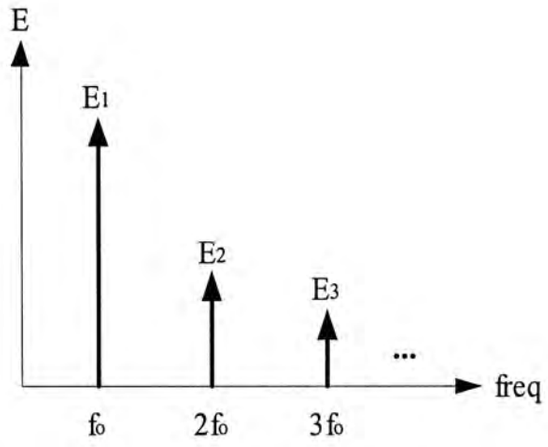

Figure 2.11: frequency spectrum shows the individual harmonics

Chapter 3 Constant transconductance rail-to-rail input stage

3.1 Introduction

In last chapter, we have discussed about the problems of rail-to-rail input stage. This chapter starts with a review of different types of CMOS rail-to-rail constant-g_m input stage topologies.

3.2 Review of constant-g_m input stage

We will give a brief review of some of the common CMOS rail-to-rail constant-g_m input stage architectures in this section. As the method of constant-g_m control is dependent on the operation region of the input pairs, thus only the methods with constant-g_m control input stage operating in strong inversion will be discussed.

3.2.1 Rail-to-rail input stages with current-based g_m control

The overall transconductance g_{mT} of an input stage is shown in equation (3.1), if the input stage is operating in strong inversion saturation region, then the g_{mT} can be defined as shown in equation (3.2).

$$g_{mT} = g_{mn} + g_{mp} \tag{3.1}$$

$$\begin{aligned} g_{mT} &= \sqrt{\mu_n C_{ox}\left(\frac{W}{L}\right)_n I_n} + \sqrt{\mu_p C_{ox}\left(\frac{W}{L}\right)_p I_p} \\ &= \sqrt{2K_n I_n} + \sqrt{2K_p I_p} \end{aligned} \tag{3.2}$$

Where μ_n and μ_p are the mobility of electron and hole, C_{ox} is the oxide capacitance per unit area, K_n and K_p are the transconductance parameters, which are constant for a given W/L. As a result, if we want to keep g_{mT} constant, then it is equivalent of keeping $\sqrt{I_n} + \sqrt{I_p}$ constant.

3.2.1.1 g_m controlled by three-times current mirror

The transconductance of an rail-to-rail input stage operating in strong inversion can be made constant by keeping the sum of the square roots of the tail currents of the complementary input pairs constant, as shown in the following equations

$$\sqrt{I_n} + \sqrt{I_p} = 2\sqrt{I_{ref}} \tag{3.3}$$

where it is assumed that the W over L ratio of the input transistors obey the condition

$$\frac{\left(\frac{W}{L}\right)_p}{\left(\frac{W}{L}\right)_n} = \frac{\mu_n}{\mu_p} \tag{3.4}$$

A brute-force implementation of equation (3.3) is applied to the rail-to-rail input stage as shown in Figure 3.1 [15][16]. The input stage consists of a rail-to-rail input stage, M_1-M_4. The g_m of this input stage is regulated by

means of two current switches, M_9 and M_{10}, and two current mirrors, M_5-M_6 and M_7-M_8, each with a gain of three.

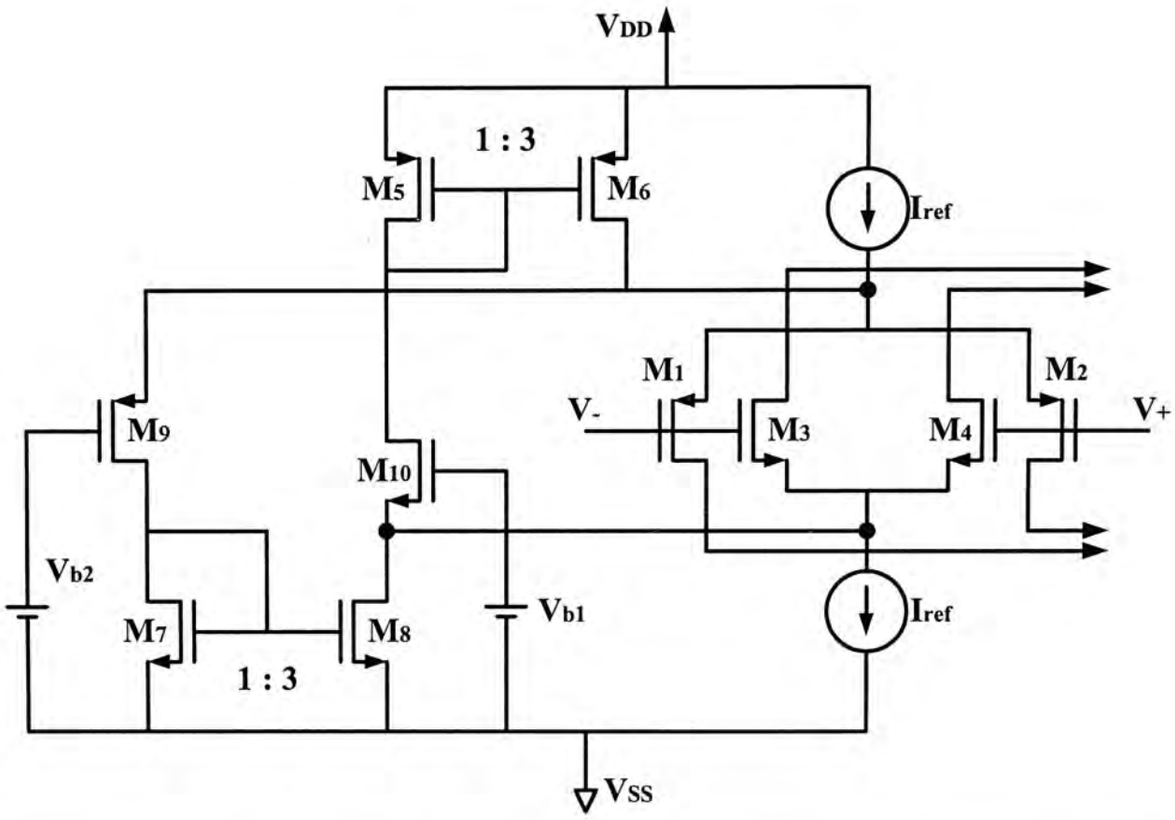

Figure 3.1: Rail-to-rail input stage with g_m controlled by two three-times current mirrors

In the middle of the common mode input range both current switches are off. The result is that the complementary input pairs are biased by a current of I_{ref}. And thus the tail currents obey equation (3.3).

If the common mode input voltage decreases below V_{b1}, the current switch, M_{10}, takes away the tail current of the N-channel input pair and feeds it into the current mirror M_5-M_6. Here it is multiplied by a factor three and added to the tail current of the P-channel input pair. The result is that the tail current of the P-channel input pair is equal to $4I_{ref}$. Since the tail current of the N-channel input pair is zero in this part of V_{CM}, equation (3.3) is fulfilled. Similarly, it can be explained that, for large

common mode input voltages, the g_m control regulates the tail current of the N-channel input pair at a value of $4I_{ref}$. The summary of the tail currents over the whole common mode input voltage range is shown in Table 3.1. The overall g_{mT} of this input stage is kept at constant within 15% variation with the value

$$g_{mT} = 2\sqrt{\mu_n C_{ox}\left(\frac{W}{L}\right)_n I_{ref}} = 2\sqrt{\mu_p C_{ox}\left(\frac{W}{L}\right)_p I_{ref}} \tag{3.5}$$

	I_n	I_p	$\sqrt{I_n}+\sqrt{I_p}$
Low V_{CM}	0	$4I_{ref}$	$2\sqrt{I_{ref}}$
Intermediate V_{CM}	I_{ref}	I_{ref}	$2\sqrt{I_{ref}}$
High V_{CM}	$4I_{ref}$	0	$2\sqrt{I_{ref}}$

Table 3.1: Summary of the tail currents over the common mode range

3.2.1.2 g_m controlled by square root current control

In this design, the g_m control is implemented by means of a square root circuit [15][17], as shown in Figure 3.2. The heart of this circuit is the translinear loop M_6-M_9. Apply Kirchhoff's voltage law to the translinear loop

$$V_{sg6} + V_{sg7} = V_{sg8} + V_{sg9} \tag{3.6}$$

If all the transistors are biased in strong inversion saturation region, then equation (3.6) can be simplified to equation (3.7)

$$\sqrt{I_{d8}} + \sqrt{I_{d9}} = \sqrt{I_{d6}} + \sqrt{I_{d7}} \qquad (3.7)$$
$$= 2\sqrt{I_{ref}}$$

where it is assumed that M_6-M_9 are match(same W/L ratio).

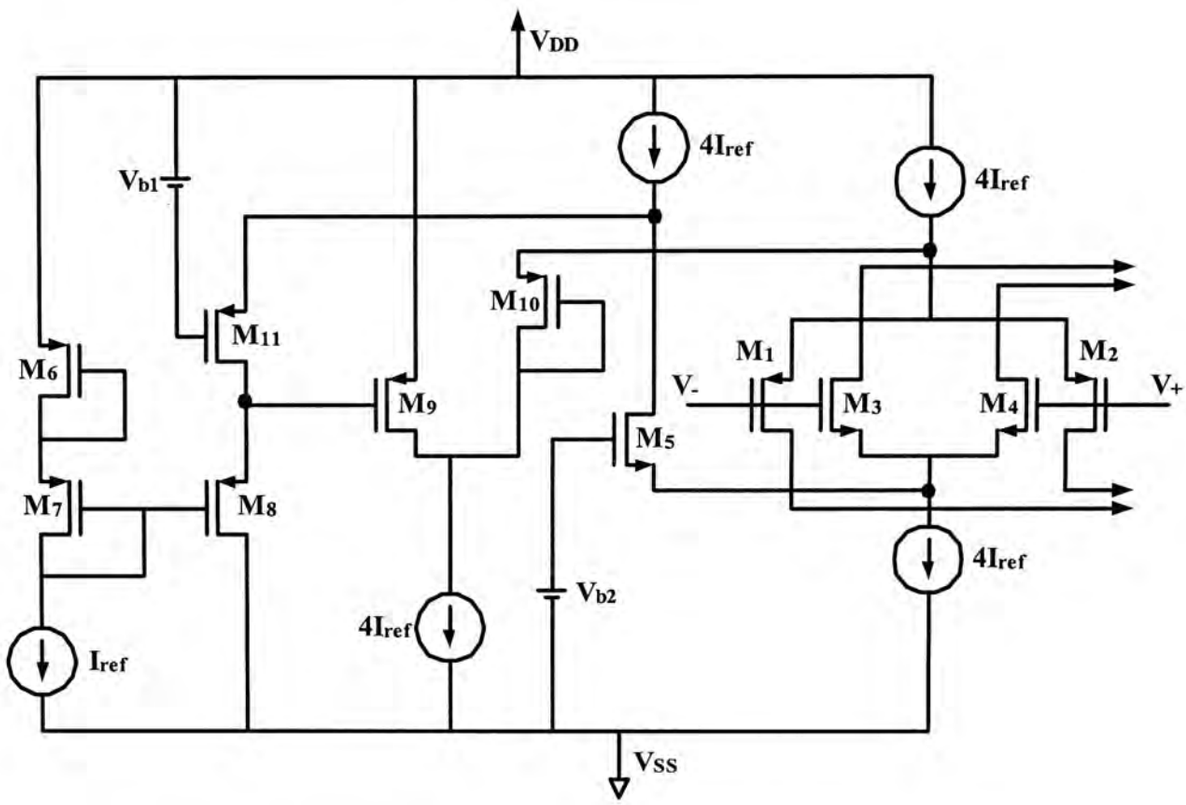

Figure 3.2: Rail-to-rail input stage with g_m controlled by a square root circuit

The current through M_8 is made equal to the tail current of the N-channel input pair. To achieve this, the current switch M_5 together with a current source measure the tail current of the N-channel input pair, and feeds this via M_{11} into M_8. The translinear loop forces a current into M_9 which obeys equation (3.7). This current is directed through the diode M_{10}, as a tail current into the P-channel input pair.

The diode-connected transistor M_{10} functions as a current limiter. If the current through M_9 is smaller than 4Iref, which is the case in the intermediate and upper part of the common mode input range, the current

limiter is not active and passes the current through M_9 into the tail of the P-channel input pair. For low common mode input voltages, the tail current of the N-channel input pair, and therefore the current through M_8 is smaller than its threshold voltage, and thus the current through M_9 becomes larger than the desired value of $4I_{ref}$. As follows from equation (3.7), using this current as a tail current for P-channel input pair will result in a larger transconductance in the lower part of the common mode input range. To avoid this, the diode-connected transistor M_{10} limits the tail current of the P-channel input transistor to desired value of $4I_{ref}$. The transistor M_{11} is inserted for basing purposes only, it does not affect the g_m control. Thus, the overall transconductance shown in equation (3.8) is ideally constant with only variation approximately 12% over the common mode input range.

$$g_{mT} = 2\sqrt{\mu_n C_{ox}\left(\frac{W}{L}\right)_n I_{ref}} = 2\sqrt{\mu_p C_{ox}\left(\frac{W}{L}\right)_p I_{ref}} \tag{3.8}$$

A drawback of the square root current control circuit is that is introduces several additional current paths between the supply rails, which considerably raise the power consumption of the input stage.

3.2.1.3 g_m controlled by using current switches only

The g_m control is implemented by four current switched M_5-M_8 as shown in Figure 3.3 [18]. Since, the g_m control consists of current switched only, it has a very good high-frequency reponse.

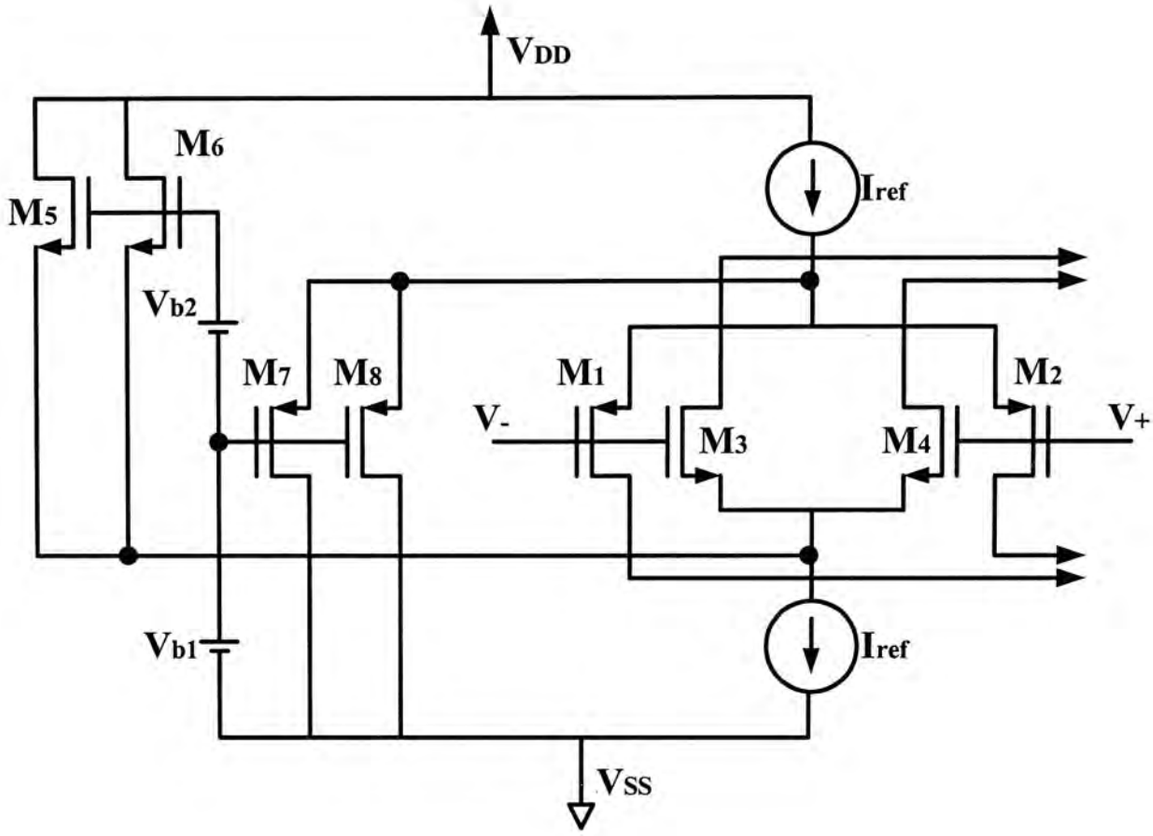

Figure 3.3: Rail-to-rail input stage with g_m controlled by current switches only

The current switches compare the common mode input voltage with their respective gate voltages. In the lower part of common mode input range, that is the V_{CM} below $V_{SS}+V_{b1}$, the current switches M_7M_8 are switched off. As a consequence, the P-channel input pair is biased with a tail current of I_{ref}. The N-channel current switches take away the tail current from the N-channel input pair, and thus the N-channel input pair is turned off at the lower part of the common mode input range. Similarly, it can be explained that for common mode input voltages above $V_{SS}+V_{b1}+V_{b2}$, that the g_m control regulates the tail current of the N-channel input pair at a value of I_{ref}. For common mode voltages between the $V_{SS}+V_{b1}$ and $V_{SS}+V_{b1}+V_{b2}$, the current switches take away part of the

current of both tail current source to control the g_m of the rail-to-rail input stage. In order to obtain a constant g_m over the whole common mode input range, the voltage source V_{b2} and the current switches have to be dimensioned properly.

For operating in strong inversion, the current switches and the input transistors should be dimensioned with the following W/L ratios

$$\frac{\left(\frac{W}{L}\right)_7}{\left(\frac{W}{L}\right)_1} = \frac{\left(\frac{W}{L}\right)_6}{\left(\frac{W}{L}\right)_3} = 3 \tag{3.9}$$

where it is assumed that M_5-M_6 matches M_7-M_8. In the outer parts of the common mode input range when only one of the input pair is operating, the tail current of the actual active input pair is regulated at a value of I_{ref}. In the intermediate part of the common mode input voltage range both current switches take away part of the tail current I_n and I_p. If the common mode input voltage is equal to the bias voltage of the gate voltages of the current switches, then the current through the switches is three times larger than the current through the input transistors. As a result, the tail current of the input pair equal $0.25I_{ref}$. Hence, the transconductance of the input stage has the same value as in other parts of the common mode input range.

Thus, the overall transconductance shown in equation (3.10) has a maximum variations of approximately 17% over the entire common mode range.

$$g_{mT} = \sqrt{\mu_n C_{ox}\left(\frac{W}{L}\right)_n I_{ref}} = \sqrt{\mu_p C_{ox}\left(\frac{W}{L}\right)_p I_{ref}} \tag{3.10}$$

3.2.2 Rail-to-rail input stages with voltage-based g_m control

Apart from keeping the sum of the square roots of the tail currents of the complementary input pairs constant, the g_m of a rail-to-rail input stage can also be made constant by keeping the sum of the gate-source voltages of the input transistors constant, as the g_m of an MOS transistor biased in strong inversion is proportional to its gate-source voltage. The overall transconductance g_{mT} expressed in equation (3.2) can also expressed in voltage

$$g_{mT} = \mu_n C_{ox}\left(\frac{W}{L}\right)_n V_{gsn,eff} + \mu_p C_{ox}\left(\frac{W}{L}\right)_p V_{sgp,eff} \tag{3.11}$$

where $V_{gs,eff}$ is the effective gate-source voltage of an input transistor.

$$V_{gs,eff} = \sqrt{\frac{2}{\mu C_{ox}}\frac{L}{W}I_d} + I_d\frac{\left(\Theta + \frac{\xi}{L}\right)}{\mu C_{ox}}\frac{L}{W} \tag{3.12}$$

The parameter Θ models the effect of the gate electrical field, while ξ expresses the effect of the source-drain electrical field. Typical values of Θ and ξ are 0.1 V^{-1} and 0.3 μm/V, respectively [9]. Thus for a constant g_m, the gate-source voltages of the input device have to obey

$$V_{gsn,eff} + V_{sgp,eff} = V_{ref} \tag{3.13}$$

3.2.2.1 g_m controlled by an ideal zener diode

Figure 3.4 shows the implementation of a g_m control using an ideal zener diode which complies with equation (3.13) [19][20]. In order to obtain a constant g_m, the zener voltage has to have a constant value V_C

where

$$V_C = V_{tn} - V_{tp} + V_{ref} \tag{3.14}$$

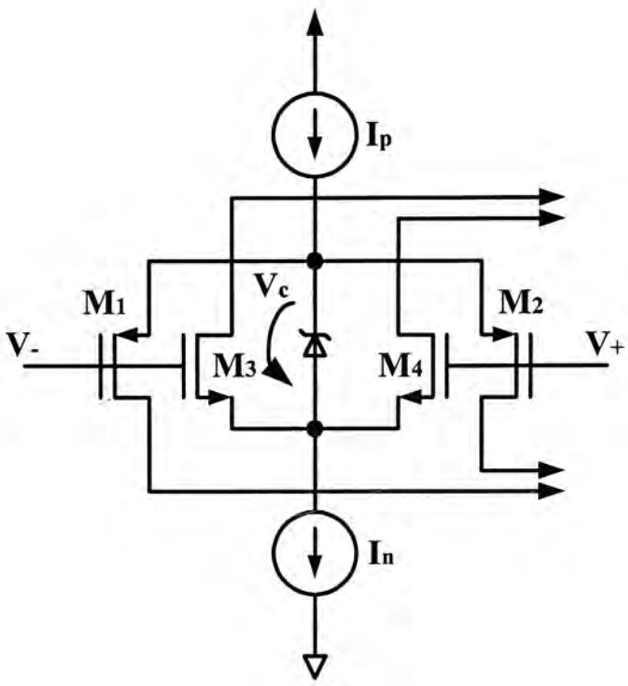

Figure 3.4: Rail-to-rail input stage with g_m controlled by an zener diode

In low or high common mode input voltages are applied, the voltage across the zener is smaller than V_C, and thus the current flowing through it is zero. As a consequence, the actual active input pair is biased with a tail current that is equal to $4I_{ref}$. In the intermediate part of the common mode input range, the zener keeps the sum of the gate-source voltages of the input pairs equal to the zener voltage, V_C. This results in a current through the zener of $3I_{ref}$, and thus both input pairs are biased with an effective tail current of I_{ref}. The overall transconductance of the rail-to-rail stage with an ideal zener diode is given by

$$g_m = \mu C_{ox} \frac{W}{L} V_{ref} = \sqrt{2\mu C_{ox} \frac{W}{L} I_{ref}} \tag{3.15}$$

3.2.2.2 g_m controlled by two diodes

Standard CMOS process does not support on-chip zener diode, especially when the voltage of zener diode has to match with the threshold voltage of the MOS transistor. To overcome this problem, zener diode is replaced by MOS diode as shown in Figure 3.5 [19][20].

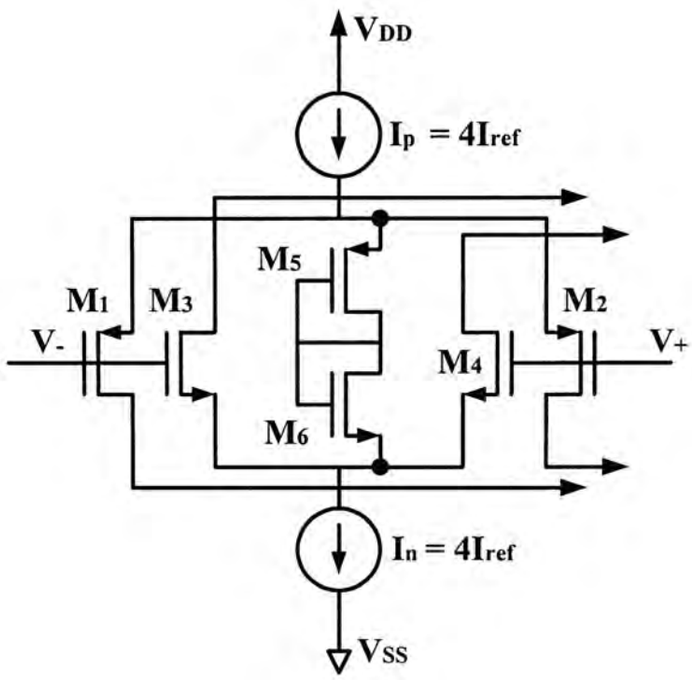

Figure 3.5: Rail-to-rail input stage. The zener is implemented by means of two diodes.

The zener diode is implemented by means of two complementary diode connected transistors, M_5M_6. In order to give the two diodes a zener voltage according to equation (3.14), the W/L ratios of the diodes are made six times larger than that of the input transistors. In this way, the current through the diodes is equal to the desired value of $3I_{ref}$ in the intermediate part of the input range. In the outer parts of the common mode input

range, the voltage across the diodes is too small to allow a current flowing through them. The overall transconductance varies by about 23% over the common mode range

$$g_m = \mu C_{ox} \frac{W}{L} V_{ref} = \sqrt{2\mu C_{ox} \frac{W}{L} I_{ref}} \tag{3.16}$$

The variation of the g_m is present because the voltage across the two diodes, in contrast to a zener, depends on the current through them.

3.2.2.3 g_m controlled by an electronic zener

The current dependency of the zener voltage can be decreased by putting more gain into the electronic zener. Figure 3.6 shows the implementation of such a zener [20]. Again, two complementary diode connected transistors, M_5 and M_6, determine the zener voltage. In order to obtain a zener voltage according to equation (3.14), the W/L ratio of the diodes have to be equal to that of the input transistors, and M_{10} has to be eight times smaller than M_{11}. Transistor M_{12} drains away the current of M_{10}. If the zener is active, the control transistor M_8 removes a part of the tail currents, such that the current through M_7 is equal to the constant current of M_{16}, which has a value of a $0.5I_{ref}$. This current also flows through the diode-connected transistors M_5 and M_6, because M_6 and M_7 have the same W/L ratios. As a result the voltage across the two complementary diodes, and therefore the sum of the gate-source voltages of the input transistors, will be constant. Transistor M_9 limits the drain voltage of M_{10}. If the drain voltage of M_{10} exceeds a certain value, determined by V_b, M_9 starts to conduct, and passes the current through M_{10} to tail of the N-channel input pair. The overall transconductance

varies about 8% over the common mode input range with value

$$g_m = \mu C_{ox} \frac{W}{L} V_{ref} = \sqrt{2\mu C_{ox} \frac{W}{L} I_{ref}} \tag{3.17}$$

This variation is smaller compared to that of the input stage with two complementary diodes because the electronic zener has a higher internal gain.

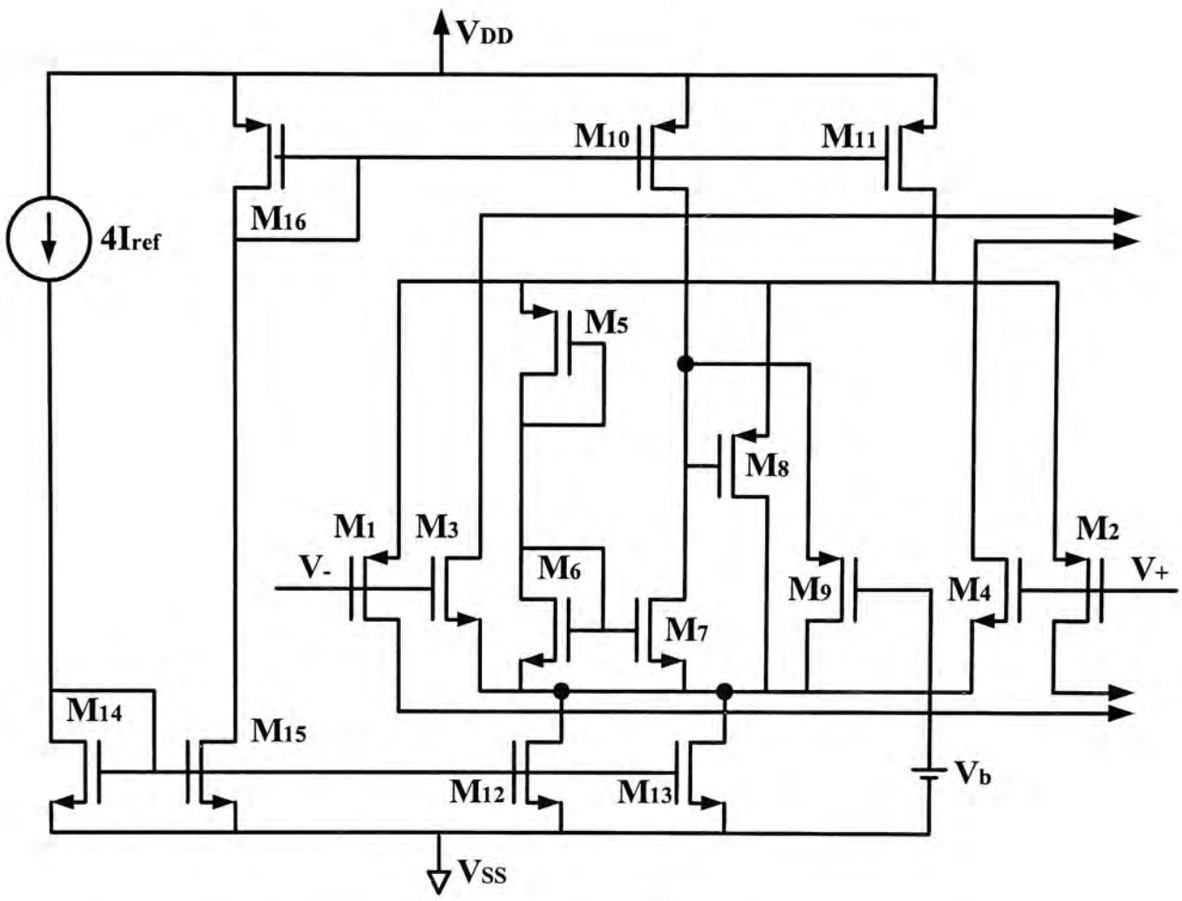

Figure 3.6: Rail-to-rail input stage with g_m control by an electronic zener

3.3 Conclusion

In this chapter, several techniques has been described to regulate the overall transconductance of a rail-to-rail input stage operating in strong inversion at a constant value. Basically there are two different methods to

control the transconductance of a rail-to-rail input stage. They control: the tail currents of the input pairs and the gate-source voltages of the input transistors. Table 3.2 summarizes the different properties of the input stage discussed before.

	3TCM	**SRC**	**CSO**	**2Diodes**	**EZener**
Power Consumption	3	2	4	4	3
g_{mT} variations	15%	12%	17%	23%	8%
Complexity	4	3	2	4	3

5: excellent 4: good 3: average 2: poor 1: very poor

Table 3.2: Summary on the properties of the different input stages

3TCM : g_m control by three times current mirrors

SRC : g_m control by a square root circuit

CSO : g_m control by current switches only

2Diodes : g_m control by two diodes

EZener : g_m control by an electronic zener

Chapter 4 Proposed constant transconductance rail-to-rail input stage

4.1 Introduction

In the previous chapter, we have introduced different constant g_{mT} rail-to-rail input stage architectures. Most of the existing architectures still have about 10% variation on the overall transconductance. It seems too much when compare with input stage operating in weak inversion which only has 5% variation on the overall transconductance. Therefore, we have proposed a new input stage so as to achieve a lower variation on the overall transconductance.

In this thesis, we will focus on the architecture of square root current control. It is because it can directly implement the equation (3.2) to control the g_{mT}, so we hope this may further decrease the variation on the g_{mT}. Furthermore, this architecture is suitable for standard CMOS process.

4.2 Principle of the conventional input stage

4.2.1 Translinear circuit

The square root current control circuit can be implemented by using a translinear circuit. The translinear (TL) circuit principle was originally formulated as a practical means of implementing nonlinear signal processing functions for bipolar analog circuit [21]. A CMOS equivalent translinear circuit with MOS operating in strong inversion [22] is shown below.

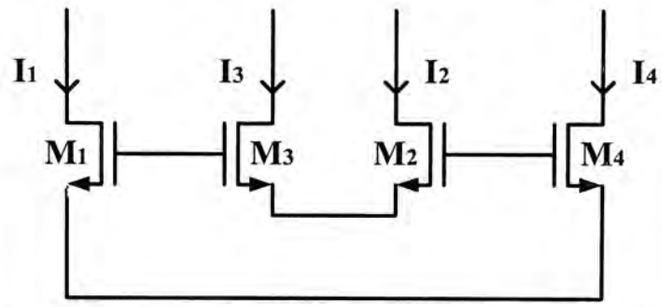

Figure 4.1: Translinear circuit – square root current control

The influence of the body effect can be significantly reduced if an up-down topology is used. A translinear circuit with such a topology which implements the square root current control is shown in Figure 4.1 [22]. The sources of M_1 and M_4 are connected clockwise, where the sources of M_2 and M_3 are connected counter clockwise. The body-effect is the same for each pair of transistors with their sources connected together. The source potential of M_1 and M_4, M_2 and M_3 are the same by connecting

them together, so

$$V_{sg1} + V_{gs3} = V_{sg4} + V_{gs2} \tag{4.1}$$

$$V_{gs1} + V_{gs2} = V_{gs3} + V_{gs4} \tag{4.2}$$

If all transistors are biased in strong inversion saturation region, then

$$\sqrt{\frac{I_1}{K_{n1}}} + V_{tn1} + \sqrt{\frac{I_2}{K_{n2}}} + V_{tn2} = \sqrt{\frac{I_3}{K_{n3}}} + V_{tn3} + \sqrt{\frac{I_4}{K_{n4}}} + V_{tn4} \tag{4.3}$$

$$\sqrt{I_1} + \sqrt{I_2} = \sqrt{I_3} + \sqrt{I_4} \tag{4.4}$$

Equation (4.4) follows from equation (4.3) if all transistors are match. Then a square root current control circuit is made.

4.3 Previous work

4.3.1 Input bias circuit

The circuit shown in Figure 4.1 is implemented by NMOS transistors which is not suitable for rail-to-rail input pairs. As a result, a constant-g_m bias circuit of using both NMOS and PMOS is shown in Figure 4.2 [23].

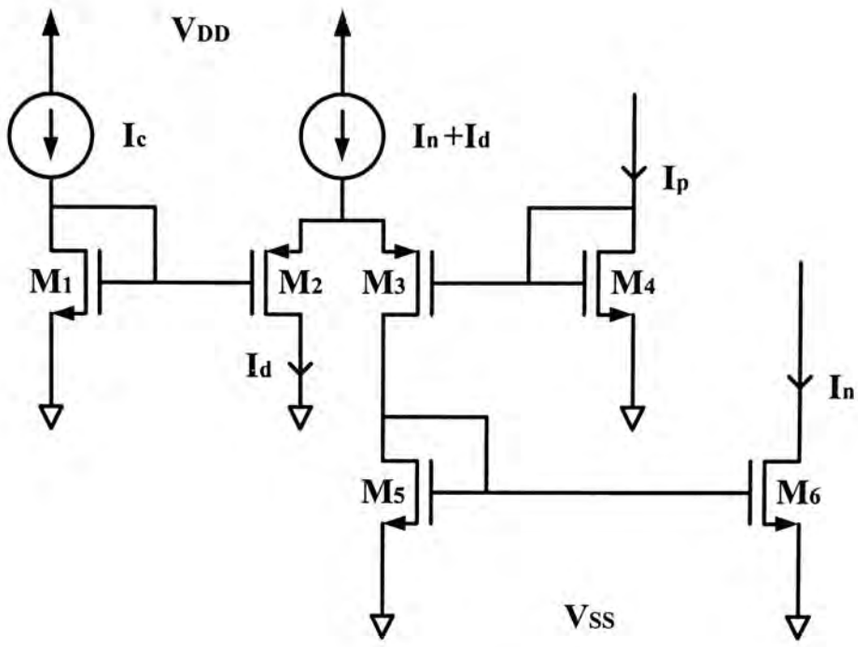

Figure 4.2: A constant-g_m bias circuit using constant bias currents

The current I_p being fed to the transistor M_4 is the input to the bias circuit and I_n which is sourced by M_6 is the output. Transistors M_1 through M_4 from a circuit which maintains the relation between I_p and I_n for a constant g_m. The drain current in M_3 is I_n and this current is fed back into the source terminals of M_2 and M_3; a constant current I_d+I_n is also fed into this terminal and thus the current in M_2 is equal to I_d. A constant current I_c is fed into a diode connected M_1, then since both M_1 and M_2 are carrying constant currents, their gate to source voltages are constant. This establishes a constant voltage node at the source terminal of M_3. Since the source terminals of M_1 and M_4 are both ground, the following is always true.

$$V_{sg1} + V_{gs2} = V_{sg4} + V_{gs3} \tag{4.5}$$

$$V_{gs1} + V_{sg2} = V_{gs4} + V_{sg3} \tag{4.6}$$

Assuming that all the transistors are operating in the strong inversion saturation region, equation (4.6) can be written as

$$\sqrt{\frac{I_c}{K_n}}+V_{tn1}+\sqrt{\frac{I_d}{K_p}}+V_{tp2}=\sqrt{\frac{I_p}{K_n}}+V_{tn4}+\sqrt{\frac{I_n}{K_p}}+V_{tp3} \tag{4.7}$$

Since the p-channel transistors M_2 and M_3 have the same source terminals, the body effect on these transistor should cancel to the first order, that is, we can assume $V_{tp2} = V_{tp3}$. This is true for the n-channel transistors M_1 and M_4 and then $V_{tn1} = Vtn_4$ is also assumed. Using these, equation (4.7) becomes

$$\sqrt{\frac{I_c}{K_n}}+\sqrt{\frac{I_d}{K_{p2}}}=\sqrt{\frac{I_n}{K_p}}+\sqrt{\frac{I_p}{K_n}} \tag{4.8}$$

$$\sqrt{2I_cK_p}+\sqrt{2I_dK_n}=\sqrt{2I_nK_n}+\sqrt{2I_pK_p} \tag{4.9}$$

where the right hand side of the equation equal to g_{mT} of the input differential pairs.

$$\begin{aligned} g_{mT} &= \sqrt{2I_nK_n}+\sqrt{2I_pK_p} \\ &= \sqrt{2I_cK_p}+\sqrt{2I_dK_n} \end{aligned} \tag{4.10}$$

As a result, the g_{mT} can be kept as constant when using 2 constant current source I_c and I_d.

4.3.2 Weak inversion operation

So far all circuit designs are carried out assuming all the transistors are biased in strong inversion but in reality when $V_{gs} < V_{th}$ the transistor simply leaves the strong inversion and enters the weak inversion region in which the relationship between the current and the voltages is shown in equation (4.11) [10], where n is the weak inversion slope factor.

$$I_d = 2n\mu C_{OX} V_{th}^2 \frac{W}{L} e^{\frac{V_{gs}-V_T}{nV_{th}}} \tag{4.11}$$

When V_{cm} becomes close to V_{DD}, I_p that flows into M_4 becomes very small and the assumption is only half true, i.e., it is still operating in saturation region, but it is no longer in the strong inversion. If I_p becomes zero, according to equation (4.7) V_{gs4} is zero and is represented by V_{tn4} which is a constant; However, it was just shown that when the transistor is in weak inversion, V_{gs} decreases with I_d according to equation (4.11). Since the sum of V_{sg3} and V_{gs4} is guaranteed to be constant, when V_{gs4} becomes less than its intended value (V_{tn4}), V_{sg3} becomes larger than its maximum intended value. This of course makes I_n and g_{mn} larger than what they should be when I_p is very small and g_{mT} is no longer constant. Figure 4.3 shows V_{gs} of M_4 as a function of V_{cm}. It can be seen that as V_{cm} is increased, V_{gs4} is reduced as a result of the decrease in I_p. When V_{cm} is about 0.64V, V_{gs4} equal to V_{tn4}. when V_{cm} is increased further, V_{gs4} does not remain at V_{tn4} but it keeps decreasing. The effect of this is shown in Figure 4.4 and Figure 4.5.

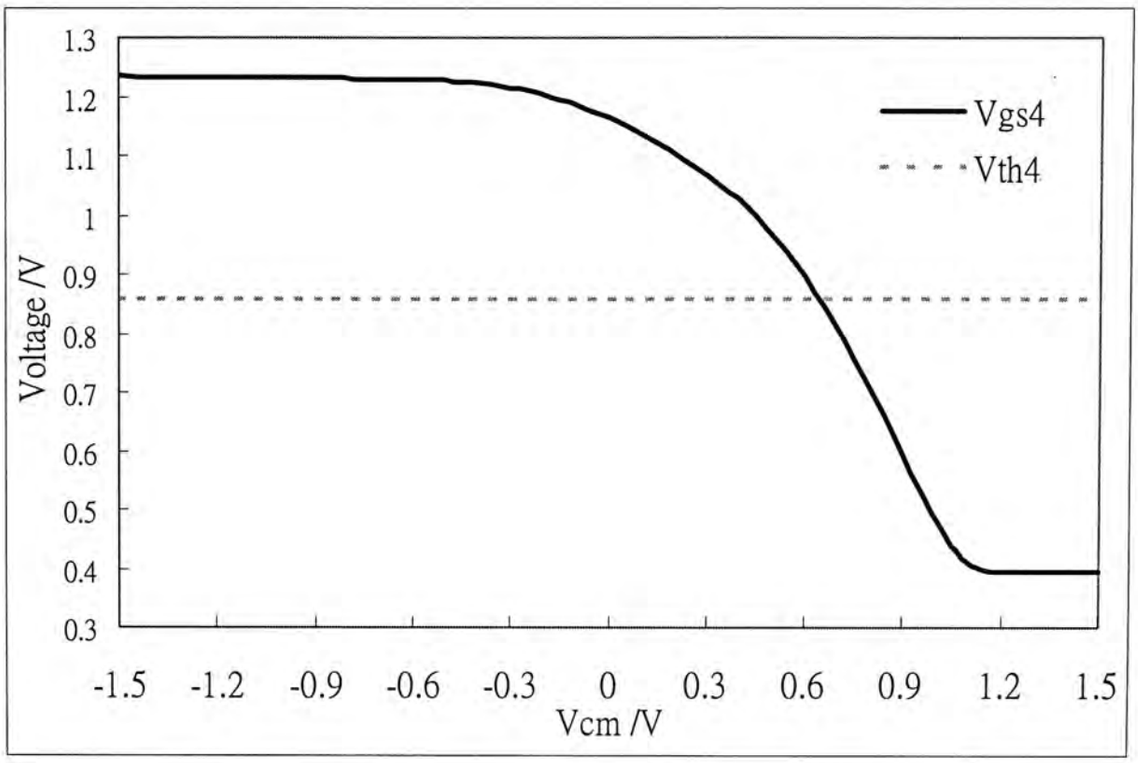

Figure 4.3: V_{gs4} as a function of V_{cm}, showing the effect of weak inversion

The results show that I_n and g_{mn} for $V_{cm} > 0.9V$ (only the n-channel differential pair contributes to g_{mT}) are significantly larger than those for $V_{cm} < -0.9V$ (only the p-channel pair contributes to g_{mT}). Note that in the simulation, V_{gs4} converged to about 0.4V for large V_{cm}; however, in reality this value of g_{mn} is also unpredictable. That is, this problem cannot be corrected by simply optimizing the transistor sizes, and it requires an additional circuit technique to be used.

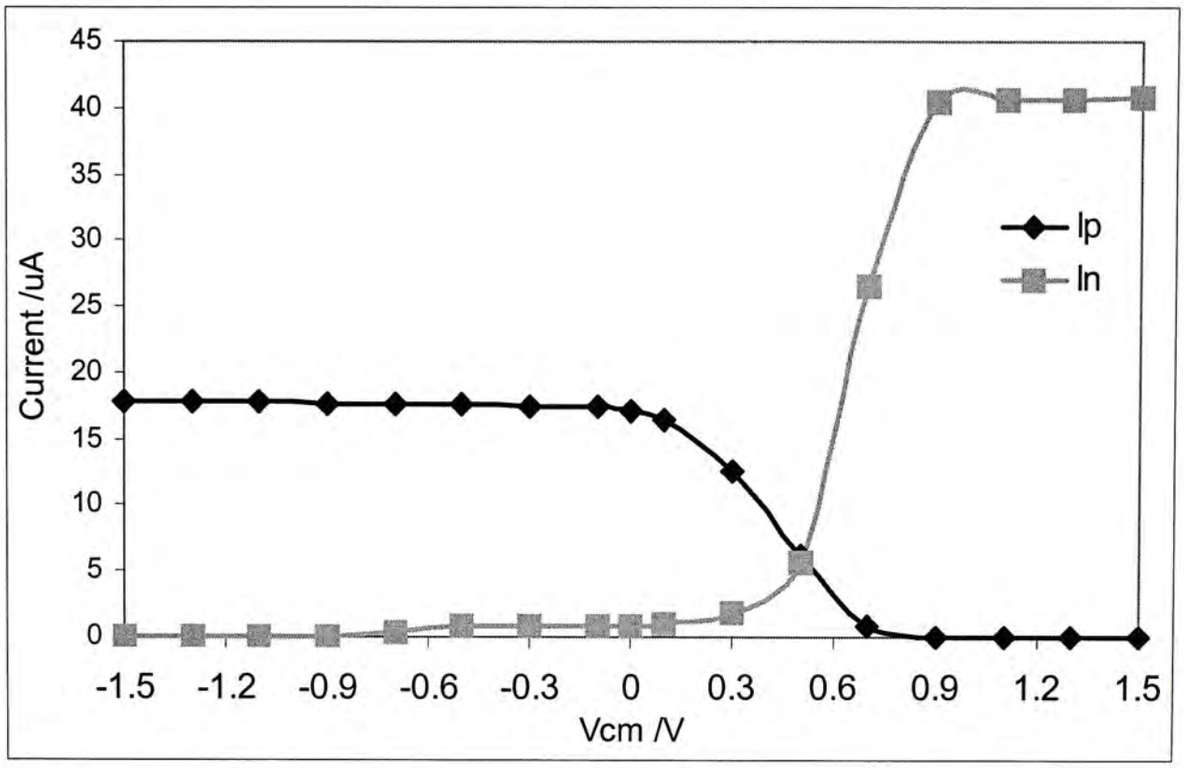

Figure 4.4: Simulation results of the differential pair currents, showing the effect of weak inversion

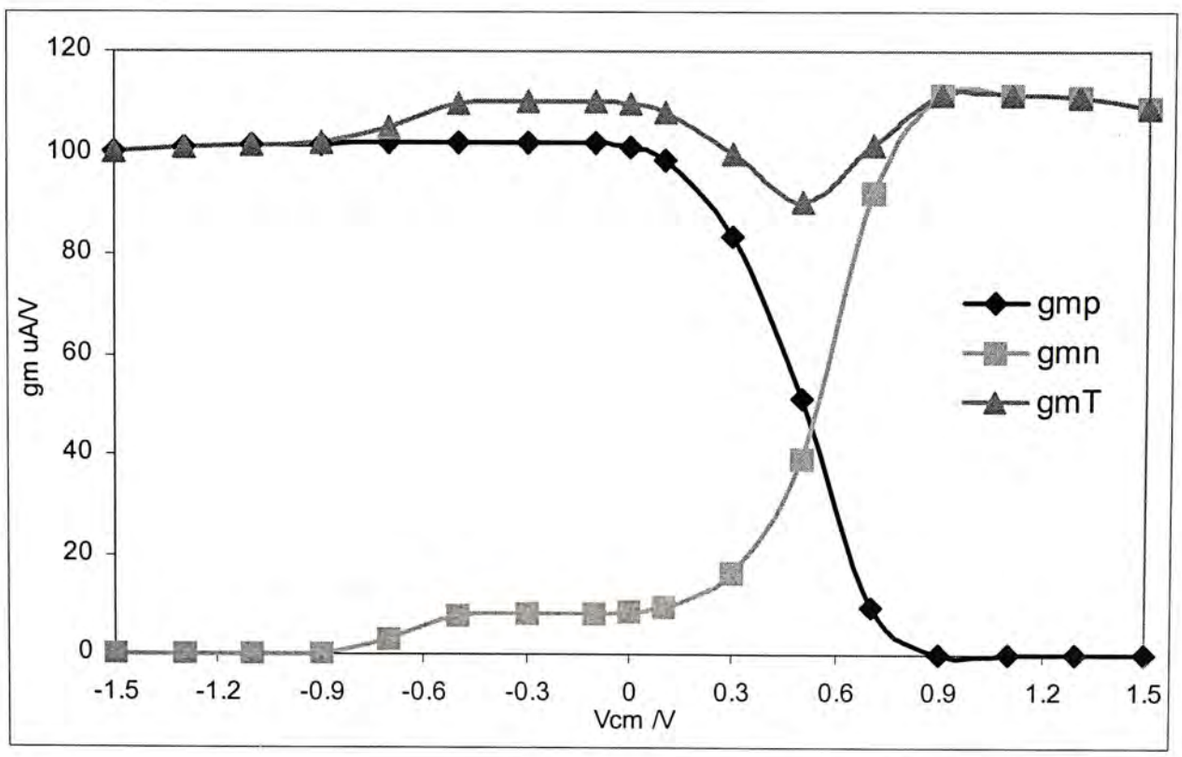

Figure 4.5: Simulation results of the differential pair transconductance, showing the effect of weak inversion

One way to overcome the problem caused by the weak inversion region operation of M_4 is to hard limit the value of I_n, just as I_p is limited to I_{ref}. The circuit shown in Figure 4.6 [23] can solve the above problem by a current conveyer [24] consisting of M_8, M_9, M_{10} and M_{11}. The drain currents in M_8 and M_9 are the same because of the current mirror $M_{10}M_{11}$, which had identical source voltage. A constant current source I_{nmax} control the maximum value of I_n even M_4 go into the weak inversion region.

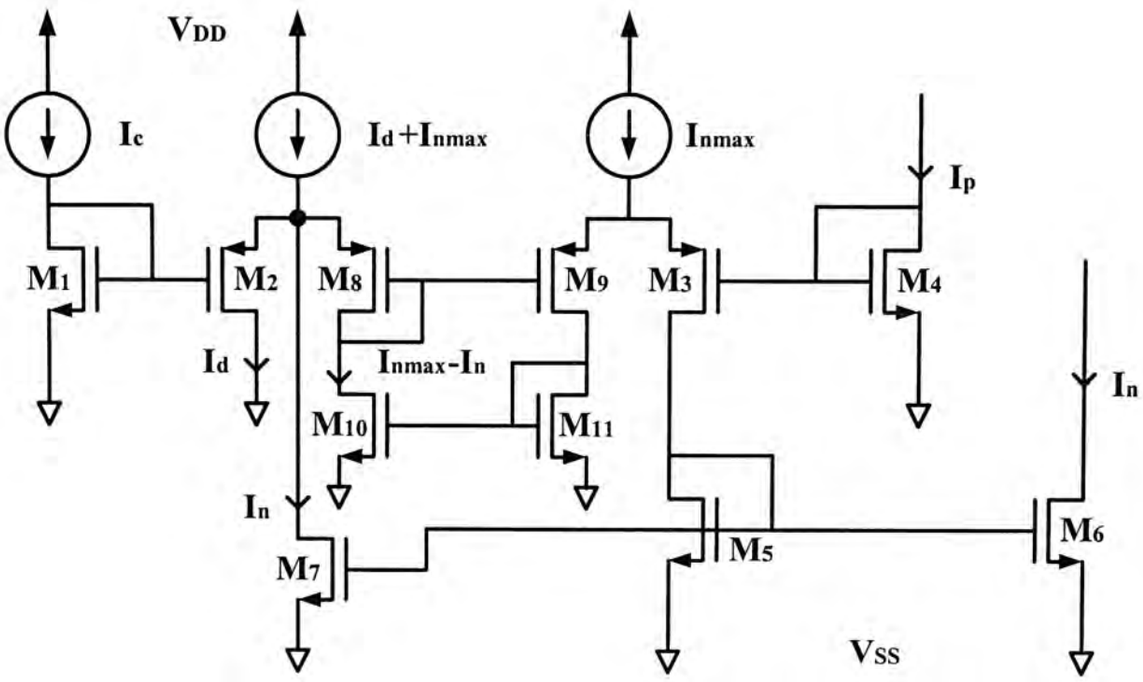

Figure 4.6: Input bias circuit overcome the weak inversion problem

This input bias circuit can keep the overall transconductance constant by the following equations:

$$V_{sg1} + V_{gs2} + V_{sg8} = V_{sg4} + V_{gs3} + V_{sg9} \tag{4.12}$$

Equation (4.12) is the same as equation (4.5) because

$$V_{sg8} = V_{sg9} \tag{4.13}$$

The overall transconductance variation of using such a control circuit can

be less than 10% [23].

4.3.3 Power up problem

A serious problem is observed from the simulation of the input bias circuit shown in Figure 4.6. The drain current flow in the current conveyer M_8 to M_{11} is zero if the V_{cm} is 1.5V when the circuit is powered up. The simulation result is shown in Figure 4.7. The drain current remains at zero even the V_{cm} change from 1.5V to –1.5V. It is because the drain current of M_9 should be equal to I_{nmax}-I_n but if the V_{cm} is 1.5V during power up, the I_n reach it's maximum value I_{nmax} and so the drain current of M_9 I_{d9} becomes zero.

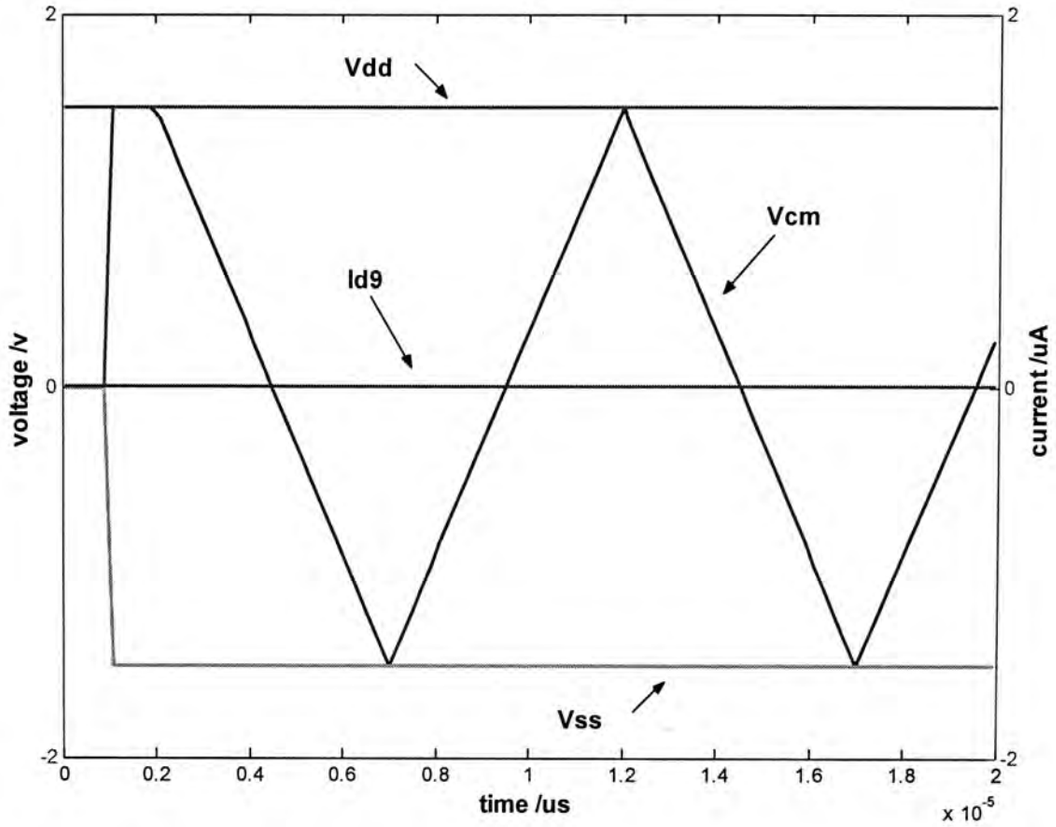

Figure 4.7: The drain current of M_9 for the V_{cm} is 1.5V when power up

The current conveyer is completely turned off and never being able to turn on again. The current conveyer can operate normally for V_{cm} equals to –1.5V when the circuit is powered up as indicated in the simulation result shown in Figure 4.8.

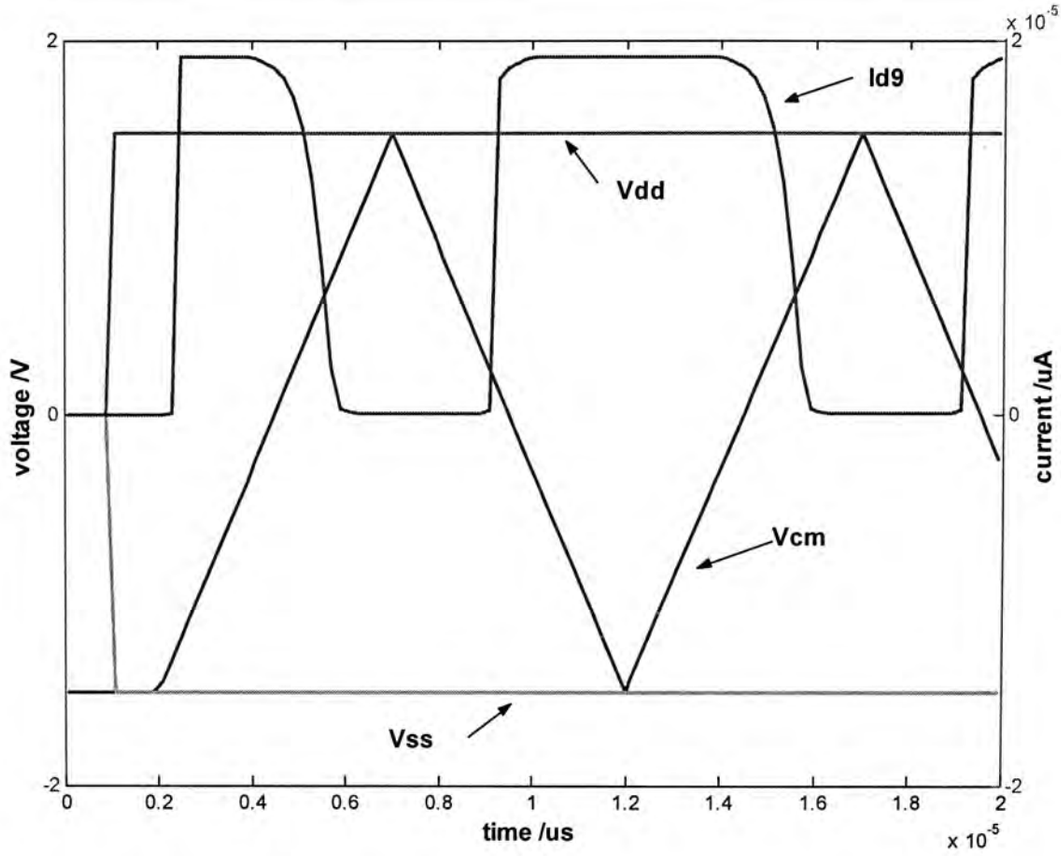

Figure 4.8: The drain current of M_9 for the V_{cm} is -1.5V when power up

Note that if a very small part of I_{nmax} connected to M_9 and M_3 flows into M_9 during power up. The circuit will operate properly. Thus, a method can solve the above problem by placing a switch M_{12} between the two nodes of the current conveyer as shown in Figure 4.9.

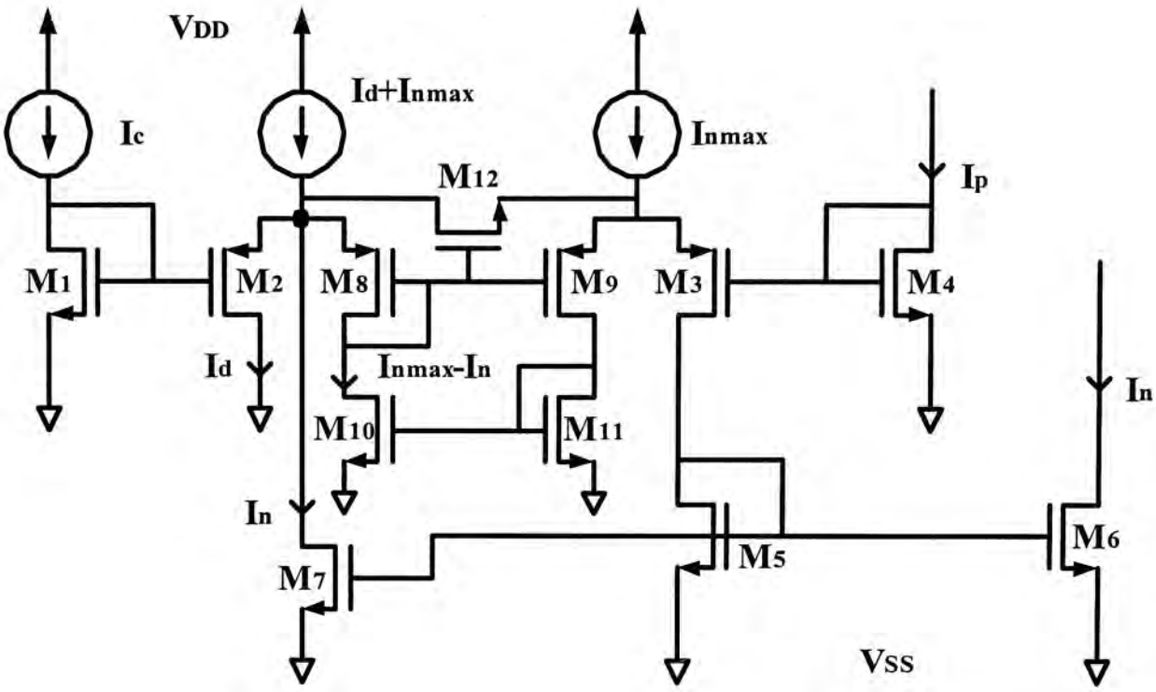

Figure 4.9: Constant-g_m bias circuit with switch M_{12} added to prevent the power up problem

The solution is to put a switch, which will turn on to short the two nodes M_{d2} and M_{d3} during power up. Even though the NMOS switch M_{12} does not turn on fully, its presence is sufficient to provide M_8 to M_{11} with some current such that they are not completely and indefinitely turned off. The simulation result shown in Figure 4.10, which shows the current conveyer operate normally even with V_{cm} equals to 1.5V during powered up.

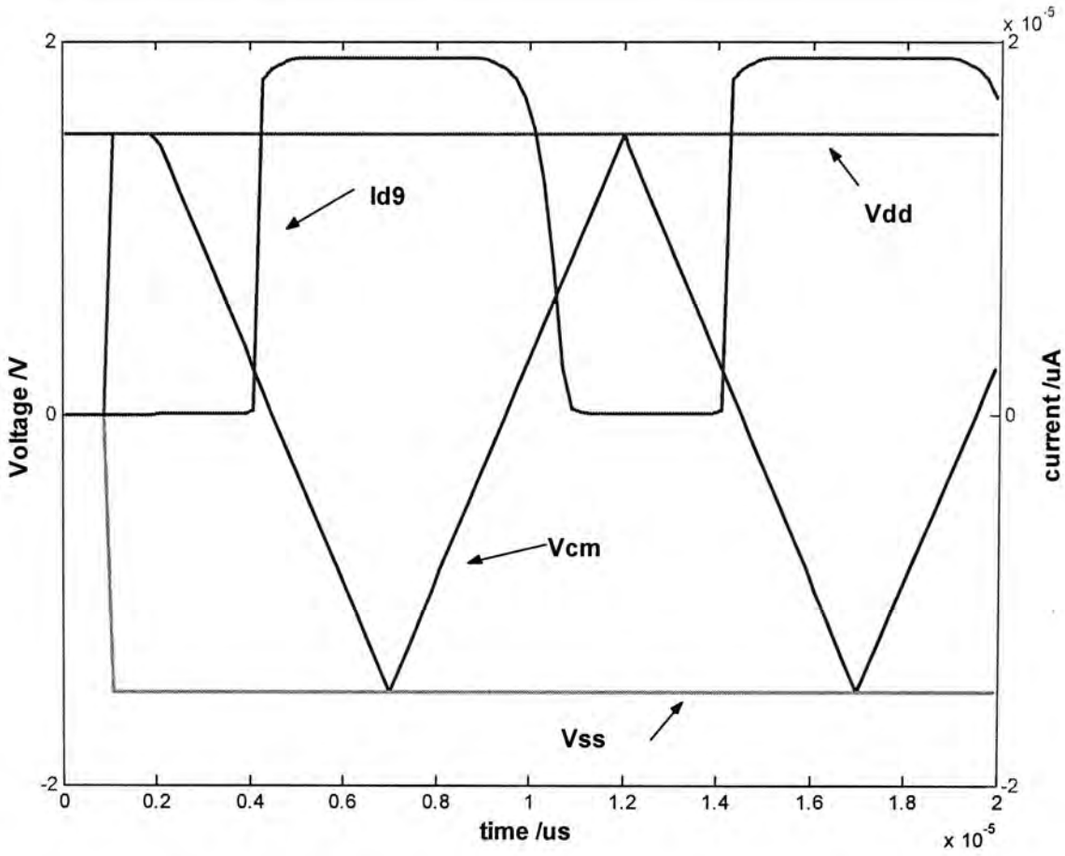

Figure 4.10: The drain current of M_9 with switch M_{12} for the V_{cm} is 1.5V when power up

4.4 Operational transconductance amplifier with proposed input biased stage

4.4.1 Proposed input biased stage architecture

A conventional architecture of a constant-g_m rail-to-rail input stage which uses square root current control circuit is shown in Figure 4.11. The maximum value of the drain current of the P-channel input pair is limited

by a constant current source I_{pmax}. The current examined by the P-channel differential pair I_p will flow into a g_m control circuit so as to generate a current I_n which satisfies the equation (4.10). Then this current I_n will flow into the N-channel differential pair.

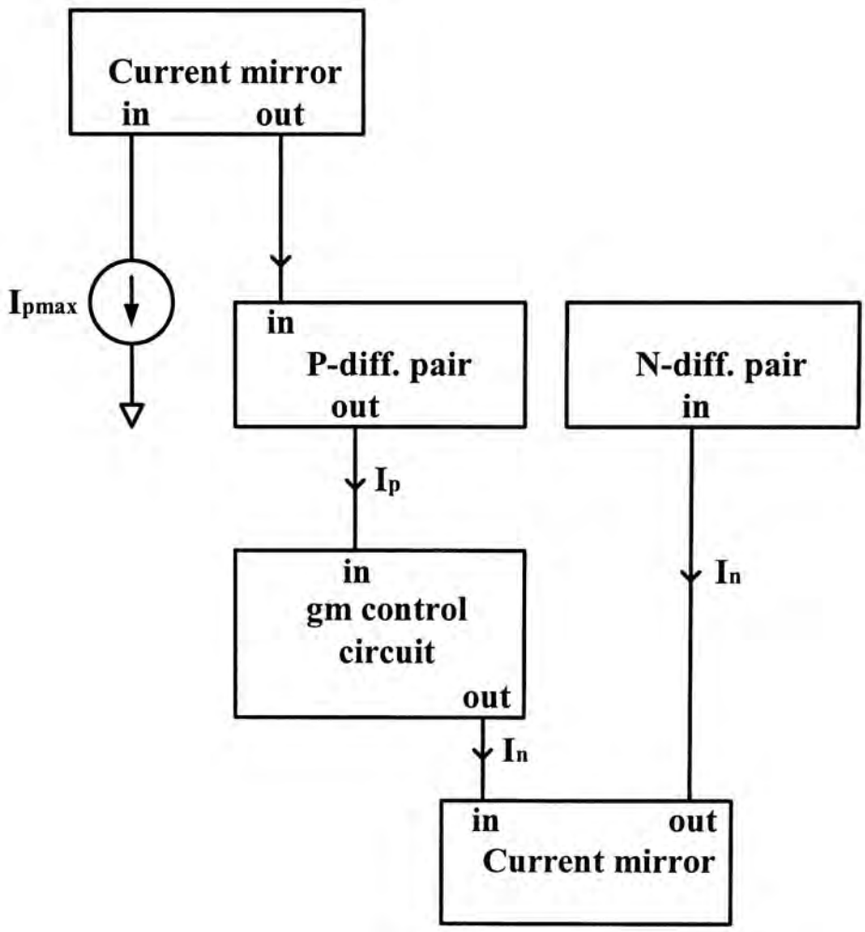

Figure 4.11: Block diagram of a conventional current control input bias stage

From this architecture, only the drain current of N-channel pair I_n will depend on the drain current of P-channel pair I_p by equation (4.10) but I_p is totally independent of I_n. This may be the main reason that such a input stage still have about 10% variation on the overall transconductance. So a new architecture is proposed which is shown in Figure 4.12, such that I_n and I_p are dependent on each other.

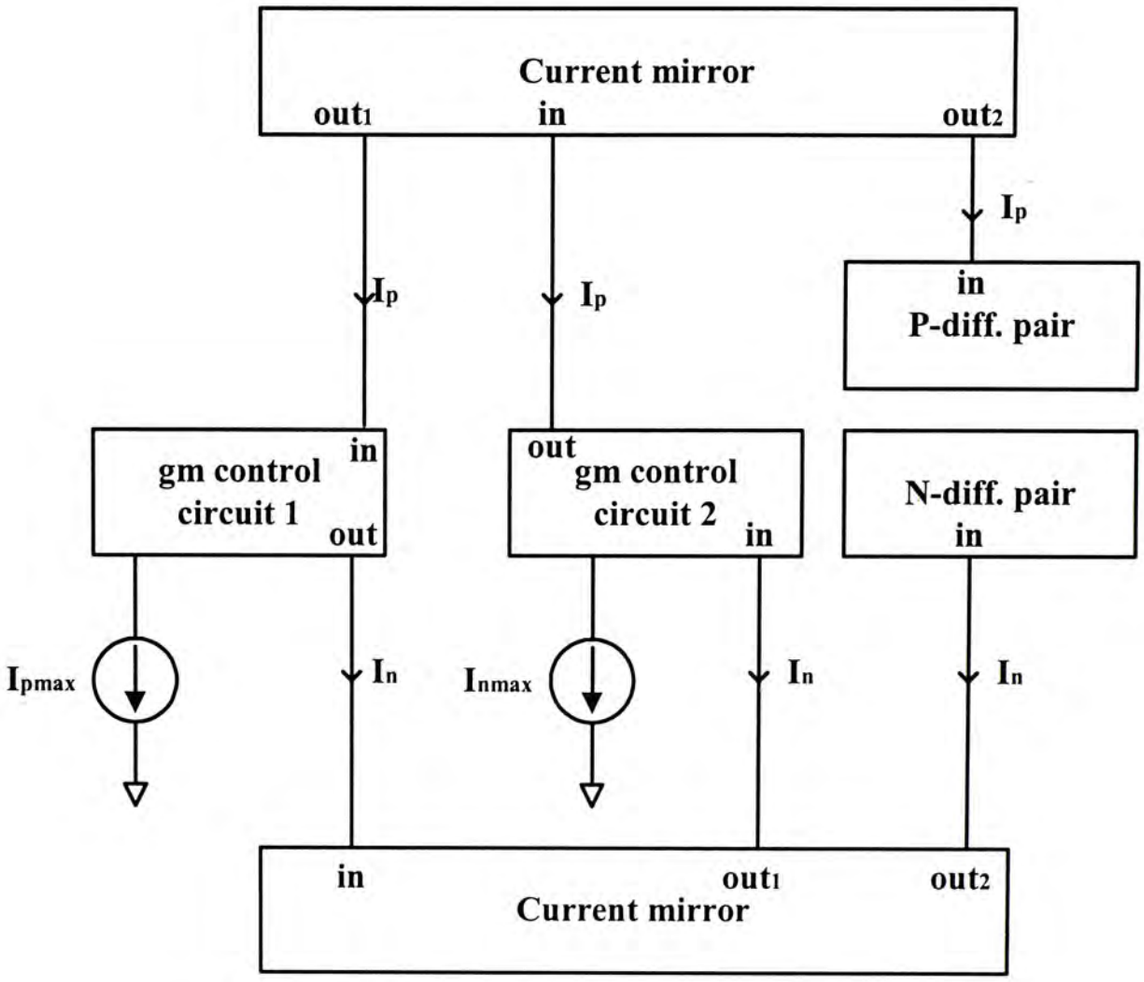

Figure 4.12: Proposed architecture of the input stage

From this proposed architecture, two g_m control circuits are used to achieve I_p and I_n depending on each other. Same as before, I_{pmax} is used to control the maximum value of I_p, the current I_p is used to generate the current I_n by g_m control circuit 1 with the relationship shown in equation (4.10). The I_n generated by g_m control circuit 1 is used to generate I_p by g_m control circuit 2 with equation (4.10). Also, the maximum value of I_n is limited by a constant current source I_{nmax}. Then the I_p will flow back into g_m control circuit 1 to generate I_n again. By this feedback system, I_n and I_p are dependent on each other by equation (4.10).

4.4.2 *Proposed input biased stage with 2 g_m control circuits*

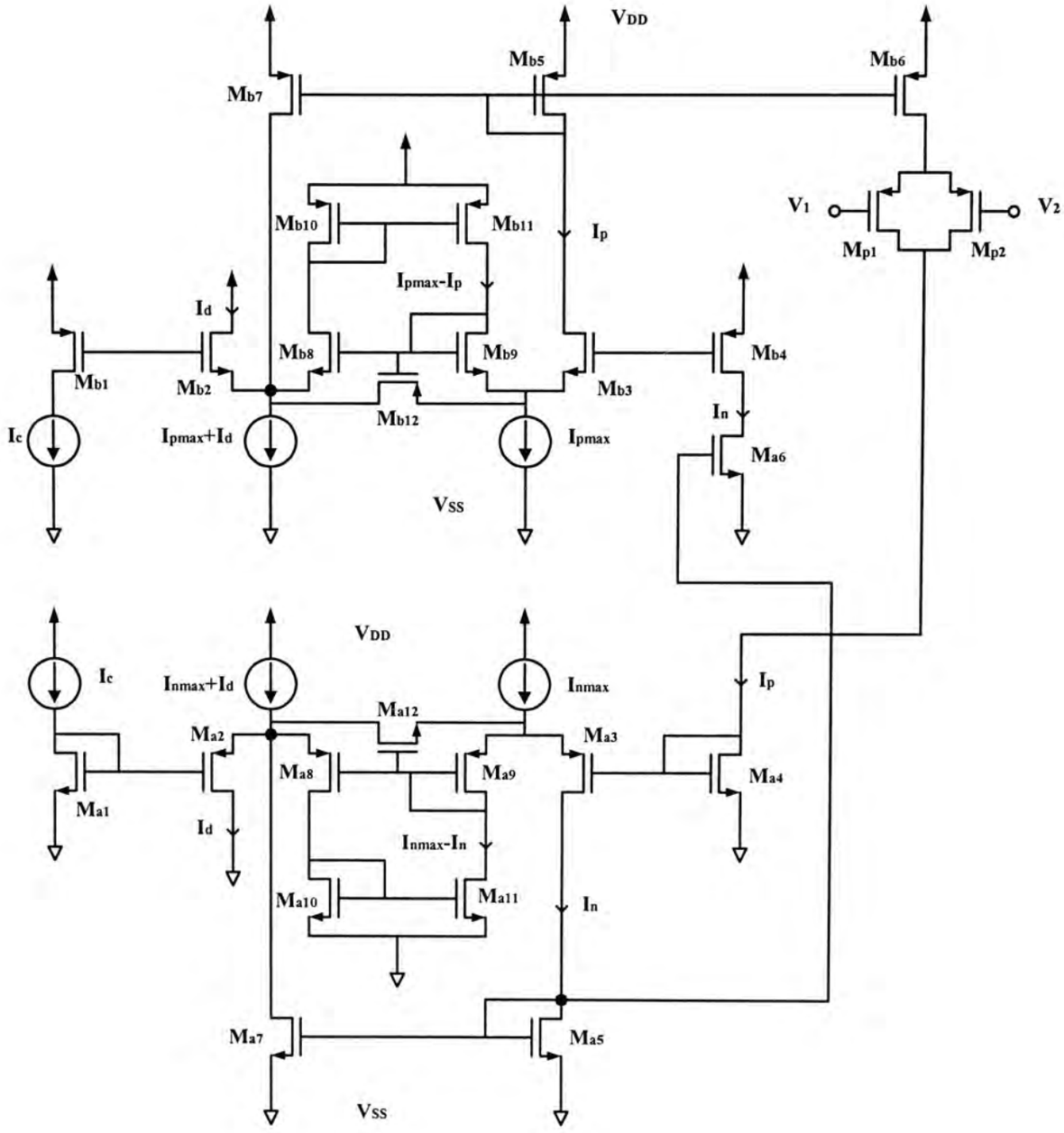

Figure 4.13: The proposed input bias circuit with using 2 g_m control circuit

The input biased circuit used in this project is shown in Figure 4.13, the g_m control circuit 1 consists of M_{a1} to M_{a12} and the g_m control circuit 2 consists of M_{b1} to M_{b12}. The g_m control circuit 1 is same as the one shown in

Figure 4.9 which is discussed before. The g_m control circuit 2 is similar to that of circuit 1 with swaping the position of nmos and pmos of circuit 1. The theory of g_m control circuit 2 is similarly

$$V_{sgb1} + V_{gsb2} + V_{sgb8} = V_{sgb4} + V_{gsb3} + V_{sgb9} \tag{4.14}$$

which is the same as equation (4.9). The transistors M_{p1} and M_{p2} are used to copy the exact value of the drain current of the P-channel differential pair, because they have the same W/L ratio and gate voltage of that of the input pair.

4.4.3 OTA with proposed input biased stage

The full schematic diagram of the operational transconductance amplifier is shown in Figure 4.14 (the schematic diagram of the OTA with physical sizes is shown in appendix). The OTA can be split into three parts, the constant-g_m control circuit shown in Figure 4.12, the rail-to-rail input differential pairs shown in Figure 2.8 and the self-biased folded-cascode gain stage shown in Figure 2.9.

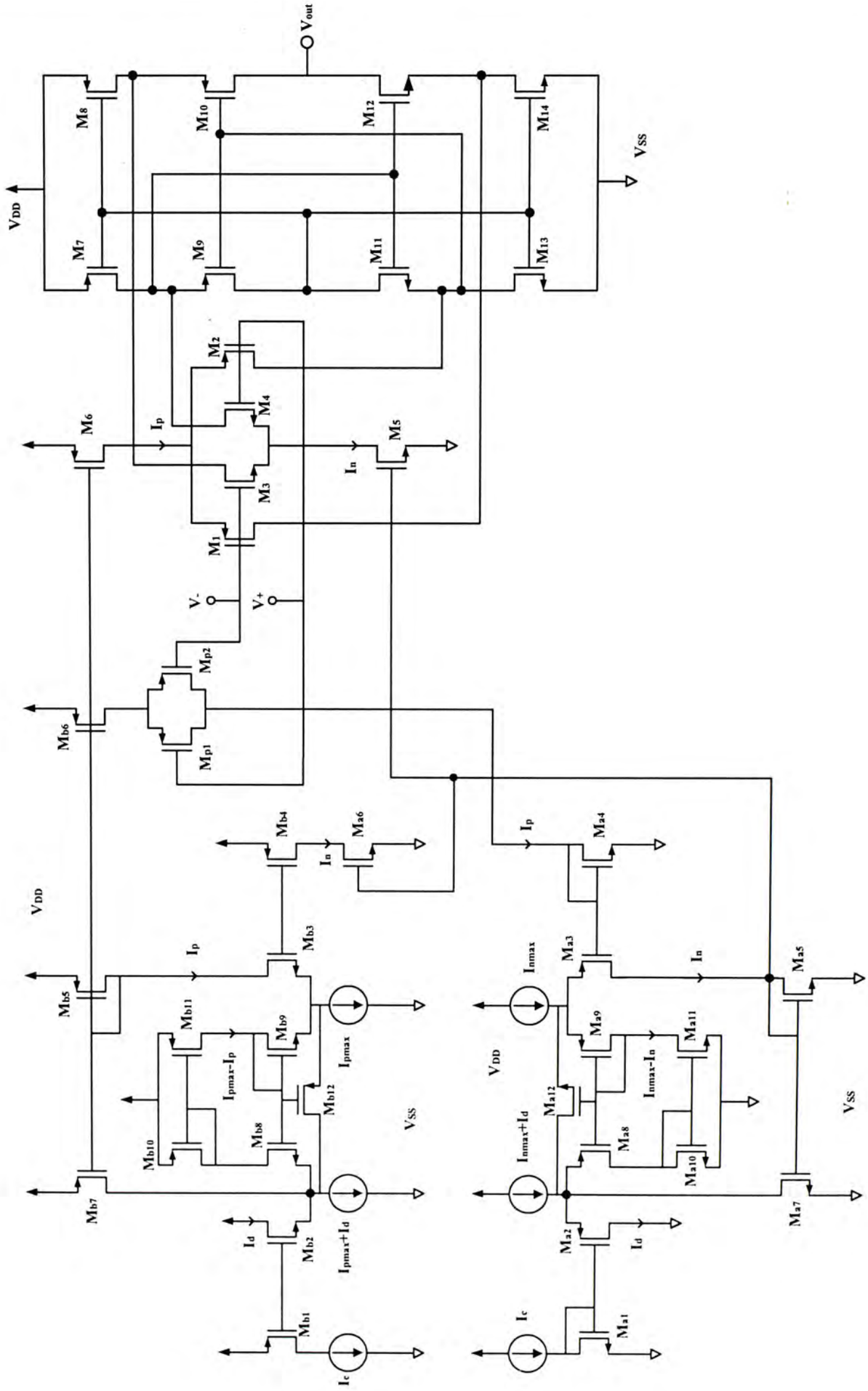

Figure 4.14: The full schematic diagram of the OTA

The open-loop gain of the OTA is given by

$$Av = g_{mT} R_o \tag{4.15}$$

where g_{mT} is the total transconductance of the rail-to-rail input pairs, which is given by

$$g_{mT} = g_{mp} + g_{mn} = g_{m1} + g_{m3} \tag{4.16}$$

and the R_o is the small signal resistance looking into the drain of M_{10} (R_{o10}) and M_{12} (R_{o12}) which are given by

$$R_{o10} = g_{m10} r_{o8} r_{o10} \tag{4.17}$$

$$R_{o12} = g_{m12} r_{o12} r_{o14} \tag{4.18}$$

Then the equation (4.15) will become

$$A_V = g_{mT} \left(g_{m10} r_{o8} r_{o10} \,||\, g_{m12} r_{o12} r_{o14} \right) \tag{4.19}$$

For a one-stage opamp, the unity-gin frequency is approximately [25]

$$\omega_U = \frac{g_{mT}}{C_l} \tag{4.20}$$

where C_l is the output loading capacitance.

All the simulation results of the OTA with proposed input biased stage will be presented in next chapter.

Chapter 5 Simulation Results

5.1 Introduction

In this chapter, we will present the simulation results of the proposed opamp. All the simulation results, including transient and frequency characteristics, are simulated by HSPICE and SpertreS.

5.2 DC bias simulation

5.2.1 Total transconductance variation

The aim of this project is to lower the variation of the total input transconductance of the input stage. From equation (3.2), the transconductance is highly dependent on the drain current of the input differential pairs. The simulation results of the drain current I_p and I_n are shown in Figure 5.1, from this one can see that the N-channel pair will not operate at low common mode voltage and P-channel pair will not operate at high common mode voltage. Which means the single stage OTA can handle rail-to-rail input signal.

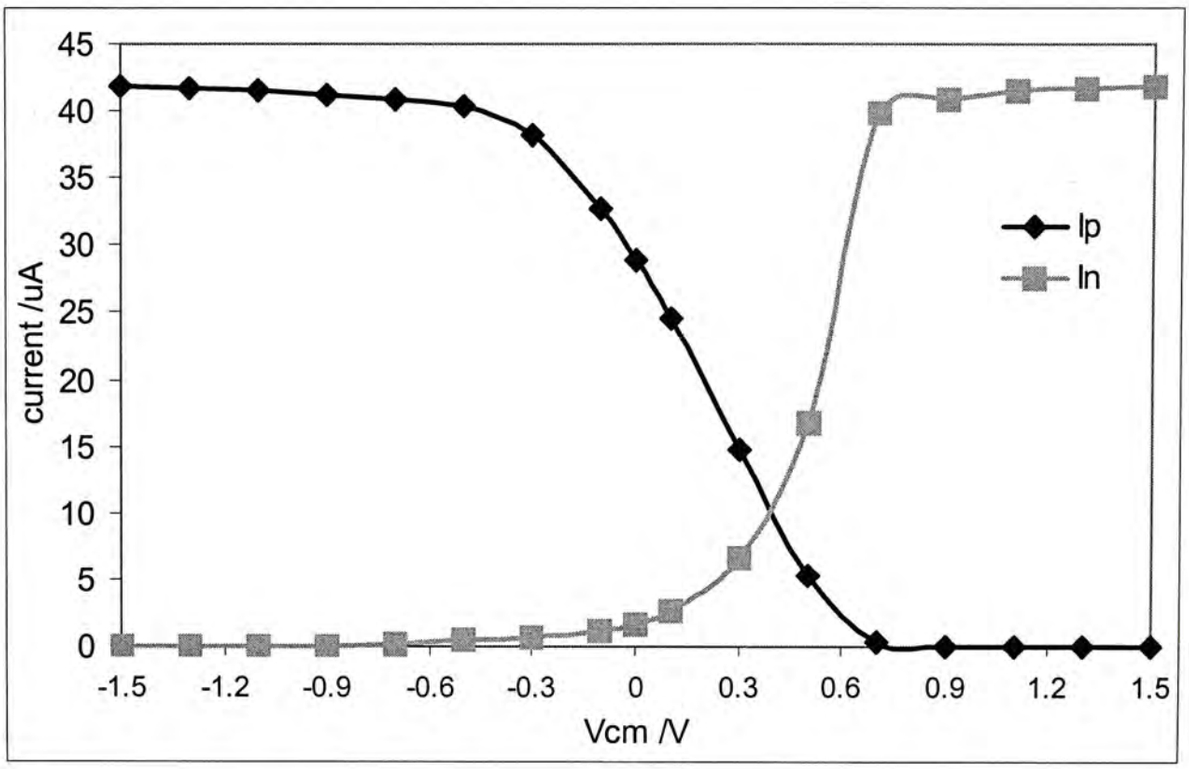

Figure 5.1: The drain current of the input pairs over the common mode range

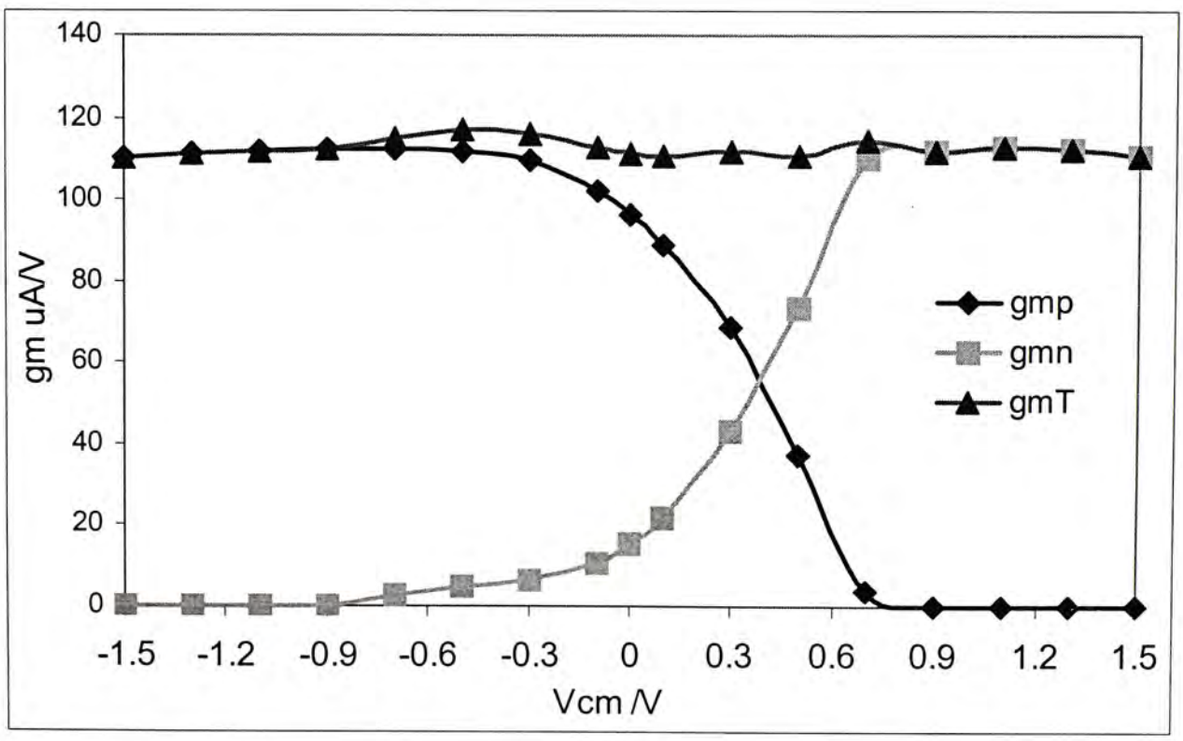

Figure 5.2: The transconductance of the input pairs over the common mode range

The simulation results of the N-channel pair transconductance g_{mn}, the P-channel pair transconductance g_{mp} and the overall transconductance g_{mT} are shown in Figure 5.2. The variation on the overall transconductance of the proposed architecture is only 5.9% which is given by

$$Variation = \frac{g_{mT}|_{\max} - g_{mT}|_{\min}}{g_{mT}|_{\min}} \times 100\% \tag{5.1}$$

There are two small peaks appear at the V_{cm} is about –0.4V and 0.7V. We have assumed the input pairs are in strong inversion saturation region when we divided equation (4.3), but this is not always true. In this case, the N-channel pair and P-channel pair are operated in strong inversion linear region when the V_{cm} is about –0.4V and 0.7V. The transconductance of the MOS in linear region is given by

$$g_m = \frac{W}{L}\mu C_{ox} V_{DS} \tag{5.2}$$

which no longer behave as square root of the drain current. Thus, the g_m control circuit cannot keep the g_{mT} constant by keeping constant of the sum of the square root of the drain current.

5.2.2 Power consumption

The root-mean-square current drawn from the power supply is found from the simulation to be about 0.253mA and thus the power consumption of the operational amplifier at a +/- 1.5V supply is only 0.76mW.

5.3 AC simulation

In this section, the frequency response of the proposed OTA will be

presented. As discussed in last chapter, the open-loop gain and other ac characteristics are highly dependent on the input transconductance, which means the variation on the g_{mT} will affect the ac characteristics, or the ac characteristics is a function of the common mode range.

5.3.1 Open-loop gain

The simulation result of the frequency response with V_{cm} equal to 0V is shown in Figure 5.3, which shows that the dc open-loop gain is 70dB with gain-bandwidth product 1.72MHz.

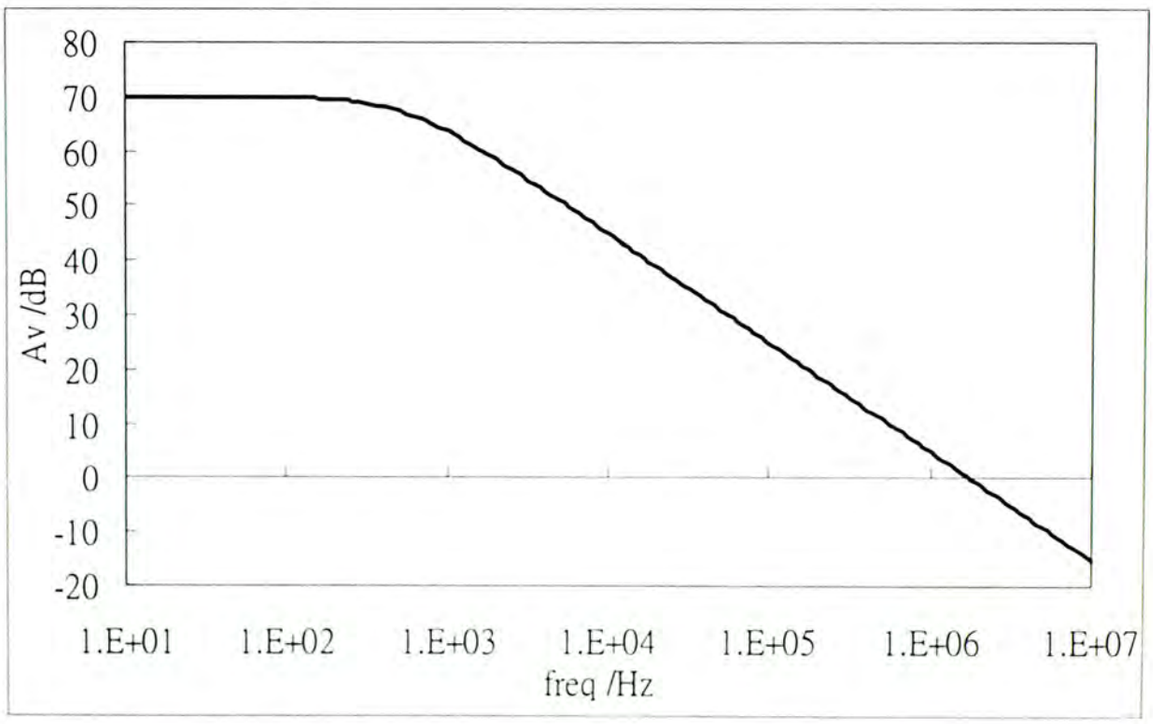

Figure 5.3: The frequency response of the OTA with Vcm equal to 0V

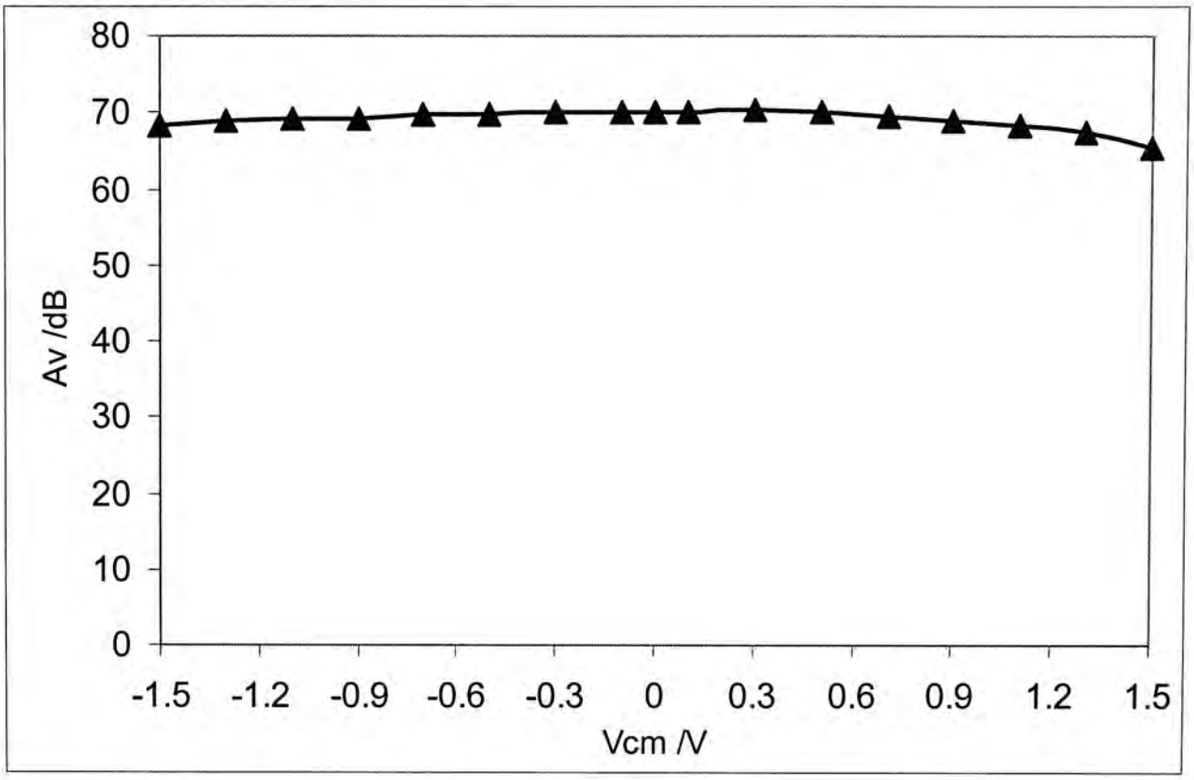

Figure 5.4: The open-loop gain of the OTA over the common mode range

The open-loop gain of the OTA as a function of common mode range is shown in Figure 5.4, we can see that the open-loop gain is almost constant (70dB) because of the small variation on the g_{mT} (only 5.9%). The open-loop gain drops drastically for $V_{cm} > 1.1V$ and $V_{cm} < -1.3V$ because the transistors of the folded-cascode stage (Figure 2.9) are pushed into the triode region. The reduce gain is caused by the reduction of output impedance at the linear region. So the open-loop gain drops when the output voltage is close to the two supply rails.

5.3.2 *Gain-bandwidth product*

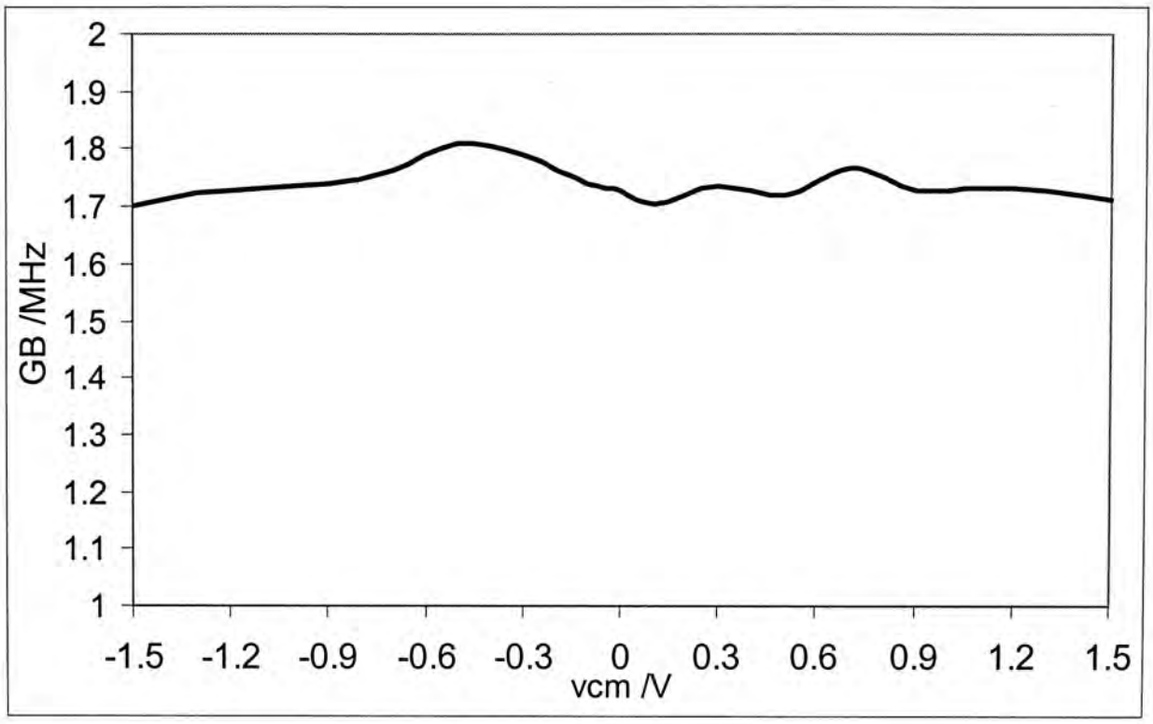

Figure 5.5: The gain-bandwidth of the OTA over the common mode range

The simulation result of the gain-bandwidth product over the common mode range is plotted in Figure 5.5. It shows that there is a variation about 6.3% on the gain-bandwidth product due to the variation on the g_{mT} by equation (4.20). The minimum value of the gain-bandwidth product, which is equal to 1.7MHz, appears at the V_{cm} such that the g_{mT} is minimum .The maximum value of the gain-bandwidth product is 1.8MHz which appears at the V_{cm} such that the g_{mT} is maximum.

5.3.3 *Phase margin*

The simulation result of the phase margin of the OTA over the common mode input range is shown in Figure 5.6, which can be found that the phase margin is almost constant at about 89° over the common mode

range. This is because the OTA is a single stage amplifier, which has only one pole.

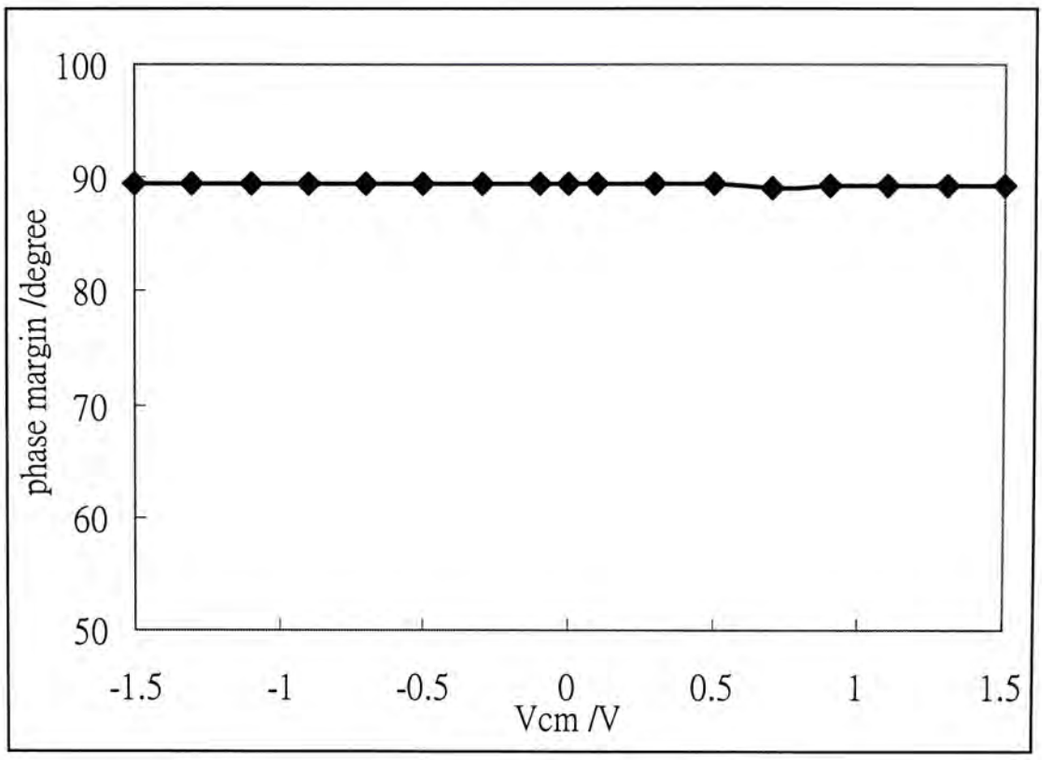

Figure 5.6: The phase margin of the OTA over the common mode range

5.4 Transient simulation

In this section, the transient response of the OTA, connected as a voltage follower configuration is presented. The aim is to concentrate on the performance of rail-to-rail signal.

5.4.1 Voltage follower

Figure 5.7 shows the simulation of the voltage follower with a $1V_{p\text{-}p}$ 100kHz sine wave input signal. The relationship of the input voltage and output voltage is shown in Figure 5.8. The output voltage cannot reach the two supply rails. It is because the transistors in folded-cascode gain stage

are forced into the triode region. The output transistors require some finite biasing voltage (V_{DS}) to operate. As a result, the output voltage cannot reach the two supply rails.

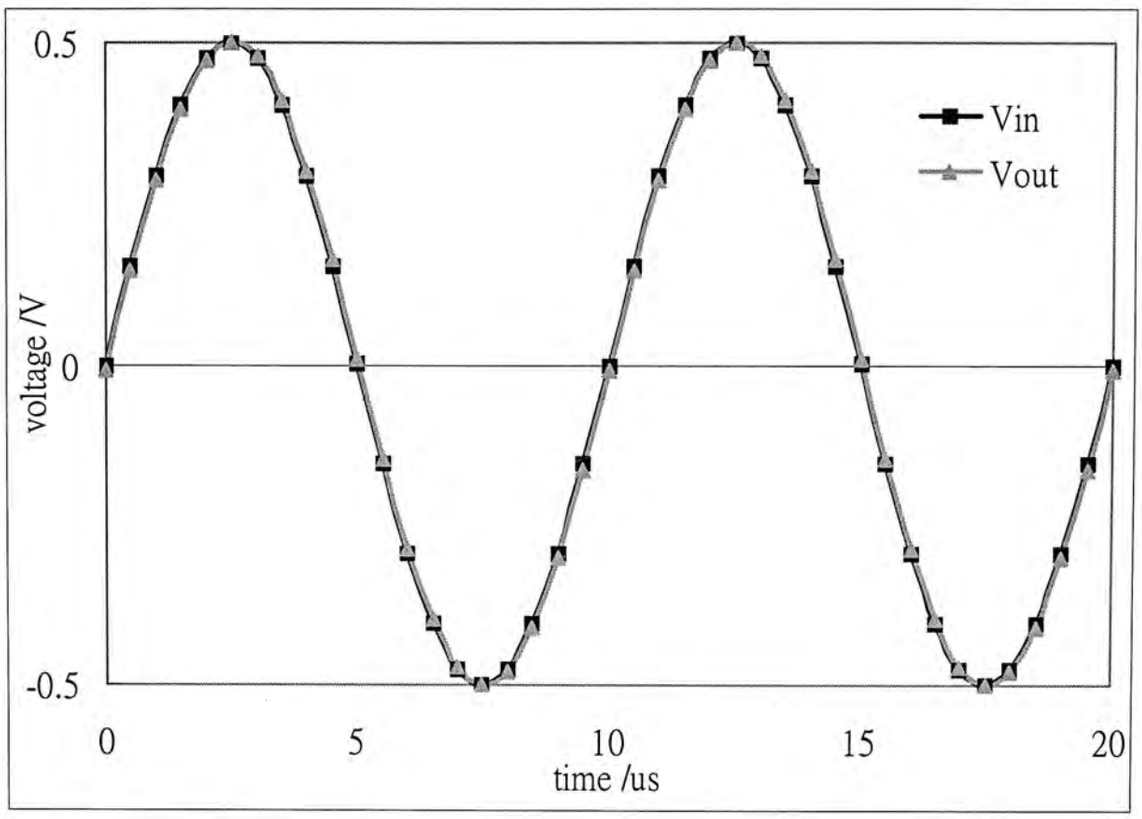

Figure 5.7: The transient response of the OTA in voltage follower configuration with a $1V_{p\text{-}p}$ 100kHz sine wave

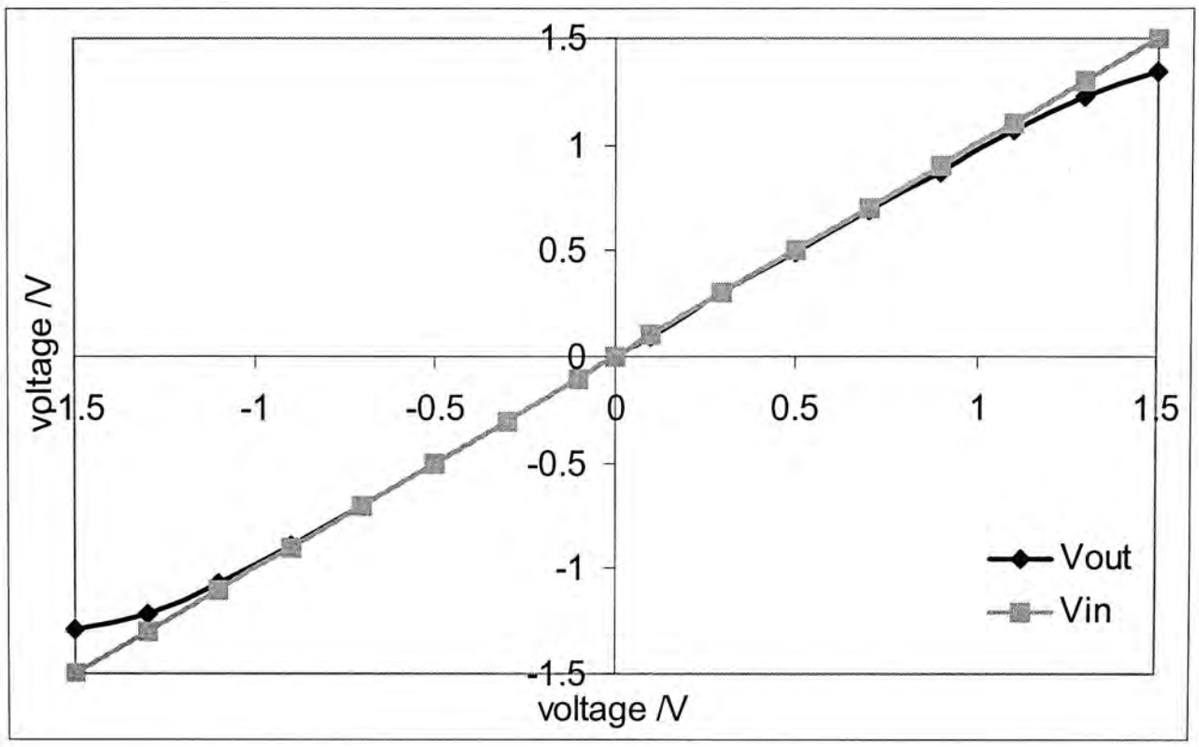

Figure 5.8: The input and output voltage characteristics of the voltage follower

5.4.2 Total harmonic distortion

The simulation result of the total harmonic distortion is shown in Figure 5.9. The result is come from Fourier Transform of the input and output signal of the voltage follower with an input signal of $0.2V_{p\text{-}p}$ 100kHz sine wave. The upper one is the input signal and the lower one is the output signal. We can see that the noise floor of the output signal is approximately –100dB. At 200kHz (2^{nd} harmonic), there is a relatively high spike of noise which is the second harmonic distortion.

Frequency	Amplitude level
100kHz (main tone)	0dB
200kHz (2^{nd} harmonic)	-74.3dB
300kHz (3^{rd} harmonic)	-88.9dB

Table 5.1: The harmonic distortion of the voltage follower

The total harmonic distortion can be found by equation (2.28) with the data given in Table 5.1. It is found to be 0.0196%.

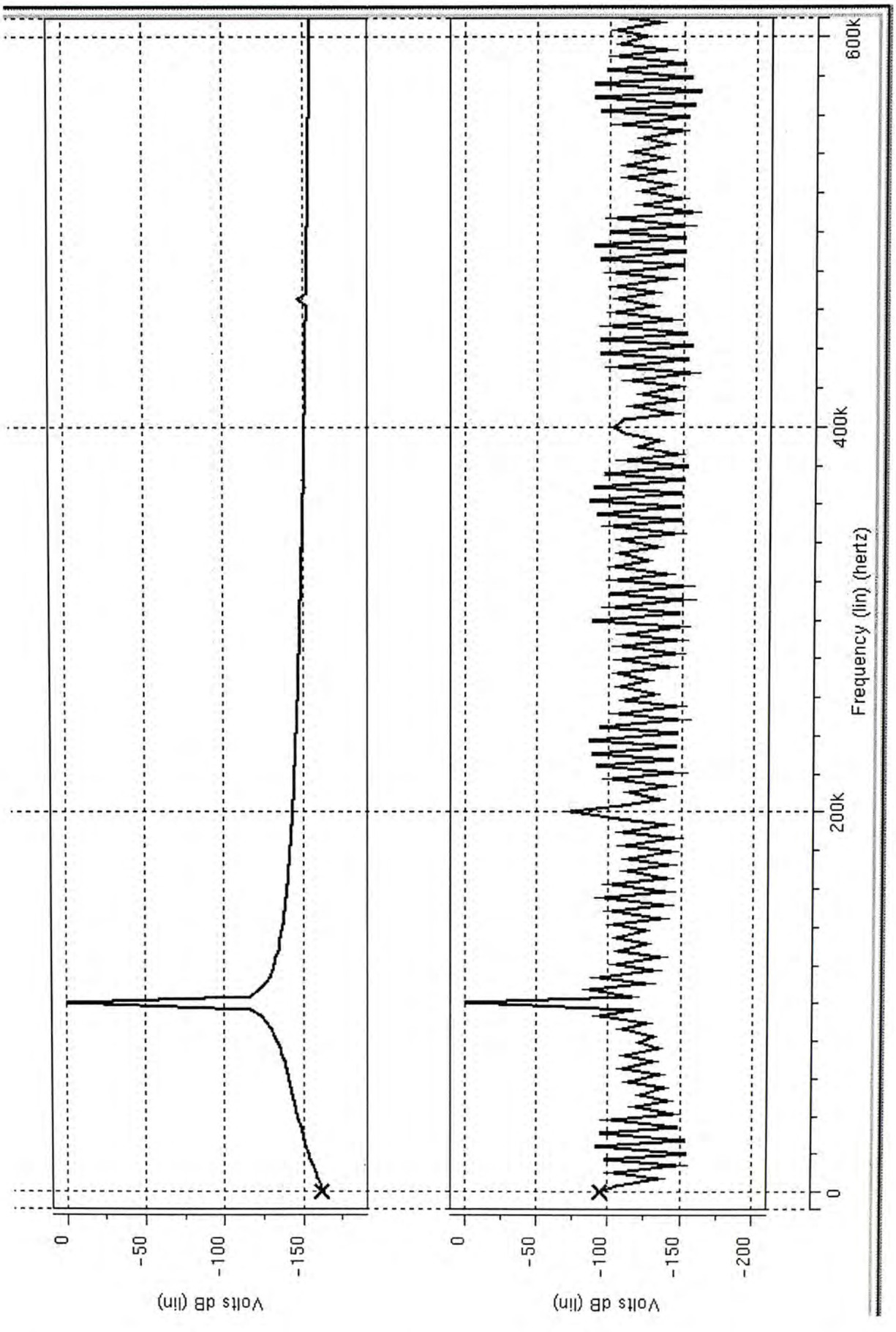

Figure 5.9: The total harmonic distortion (i) upper one is input signal, (ii) lower one is the output signal

5.4.3 Step response

In this section, the simulation results on the step response are presented. We can find out the overshoot and the slew rate of both rising and falling step from these simulations. The input step is a $1V_{p\text{-}p}$ pulse signal.

The slew rate of the rising step can be found from Figure 5.10 which shows the rising step response and it's value is 58.82V/μs. The slew rate of the falling step can be found from Figure 5.11 which shows the falling step response is 72.01V/μs.

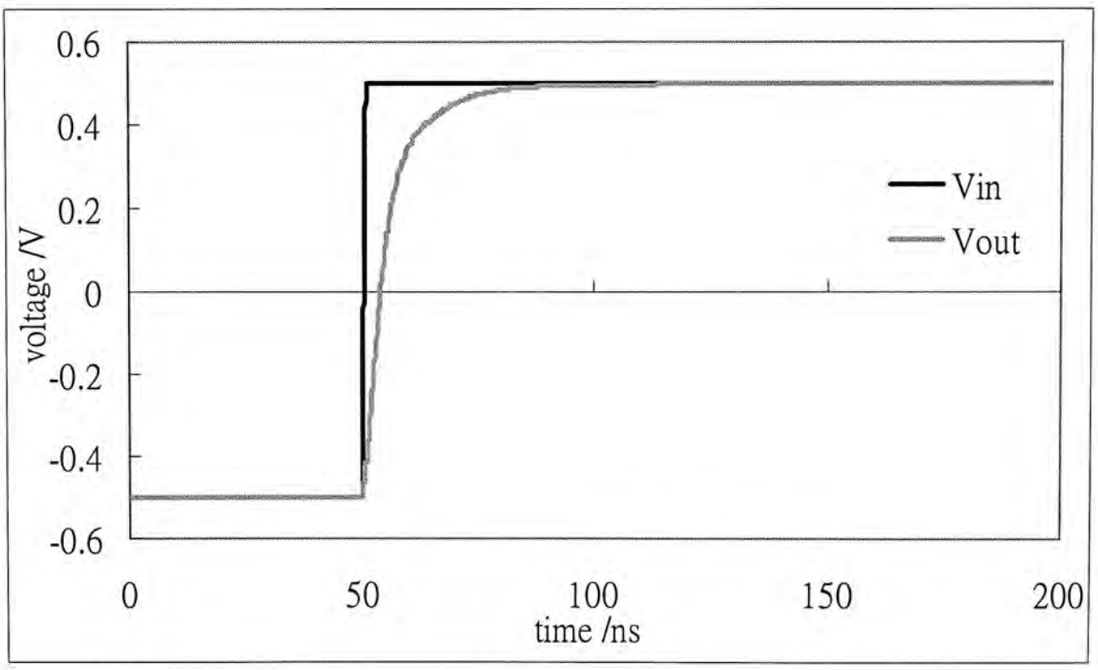

Figure 5.10: The rising step response

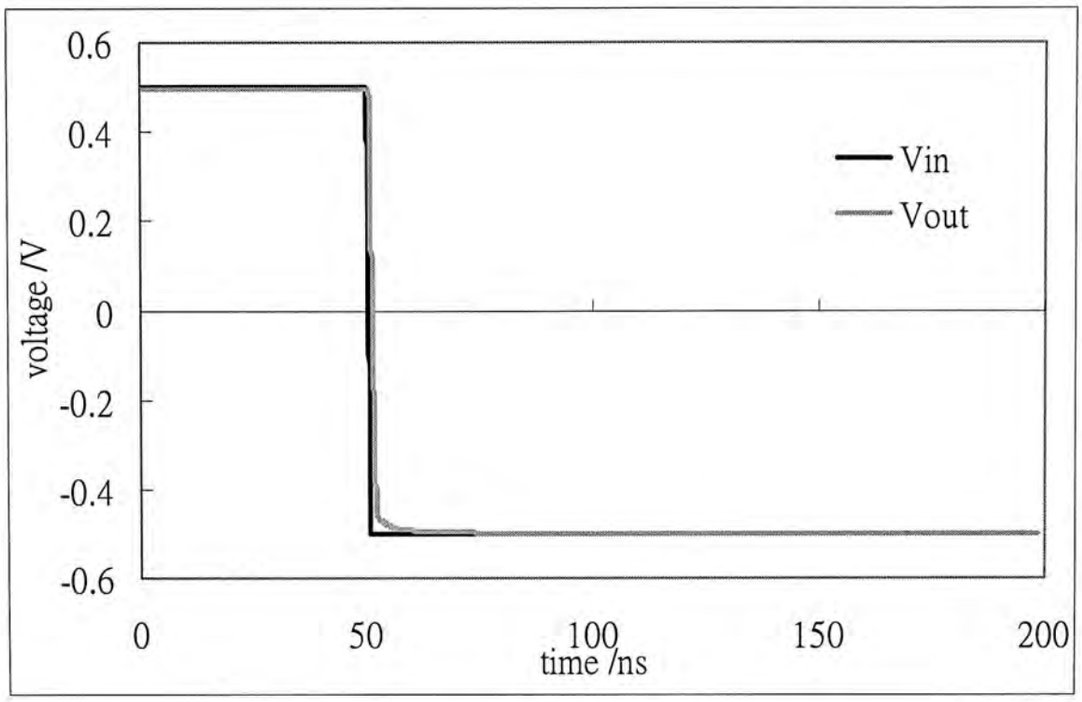

Figure 5.11: The falling step response

The simulation result of the overshoot is shown in Figure 5.12, which

$$Overshoot = \frac{1.016-1}{1} \times 100\% = 1.6\%$$

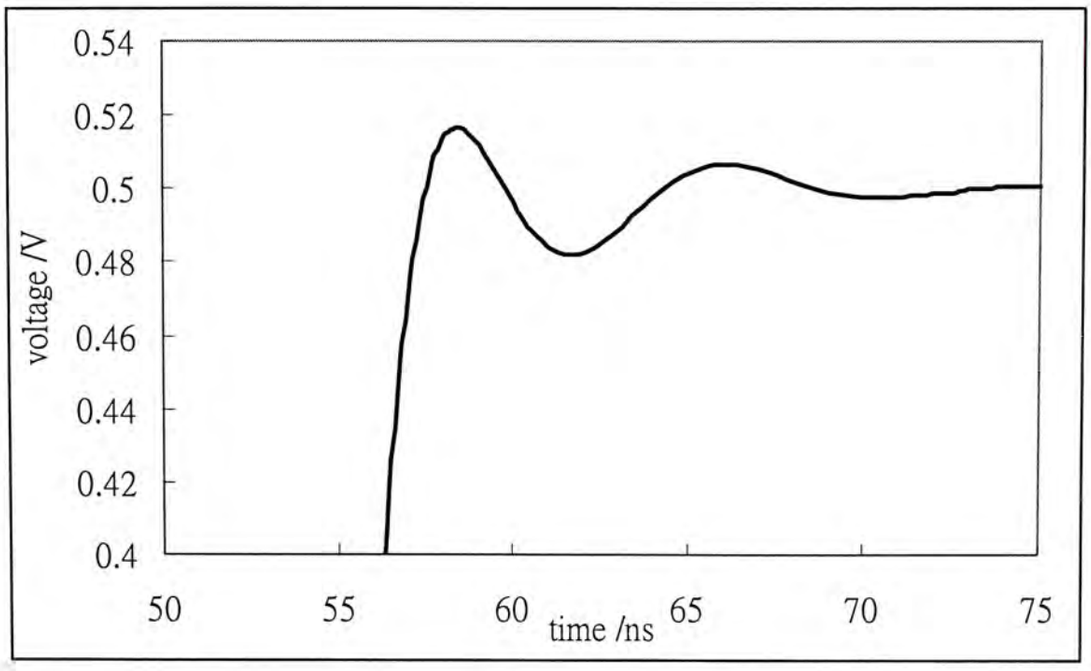

Figure 5.12: The overshoot of the step response

5.5 Conclusion

In this chapter, all the simulation results are presented. The single stage operational transconductance amplifier with the proposed architecture can achieve constant g_m over the whole common mode range with only 5.9% variation. The AC and DC simulation results are summarized in Table 5.2.

V_{DD} = 1.5V V_{SS} = -1.5V C_{load} = 10pF

Power consumption	0.76mW
g_{mT} variation	5.9%
DC open-loop gain (V_{cm}=0V)	70dB
Phase margin	89°
Slew rate (rise)	58.82V/μs
Slew rate (fall)	70.01V/μs
CMRR (V_{cm}=0V)	71.88dB
Gain-bandwidth product (V_{cm}=0V)	1.72MHz
Common mode input range	Exceeds both supply rails
Output swing	V_{SS}+0.2V, V_{DD}-0.15
DC offset	<15μV
THD	0.0196%
Overshoot	1.6%

Table 5.2: Specifications of the single stage OTA with proposed architecture

Chapter 6 Layout Consideration

6.1 Introduction

In this project, all the circuits were fabricated with a 0.6μm CMOS process (AMS CMOS CUP 0.6μ). It is a 3 metal layers and 2 polysilicon layers process. The wafer cross-section diagram of this process is shown in Figure 6.1 [26].

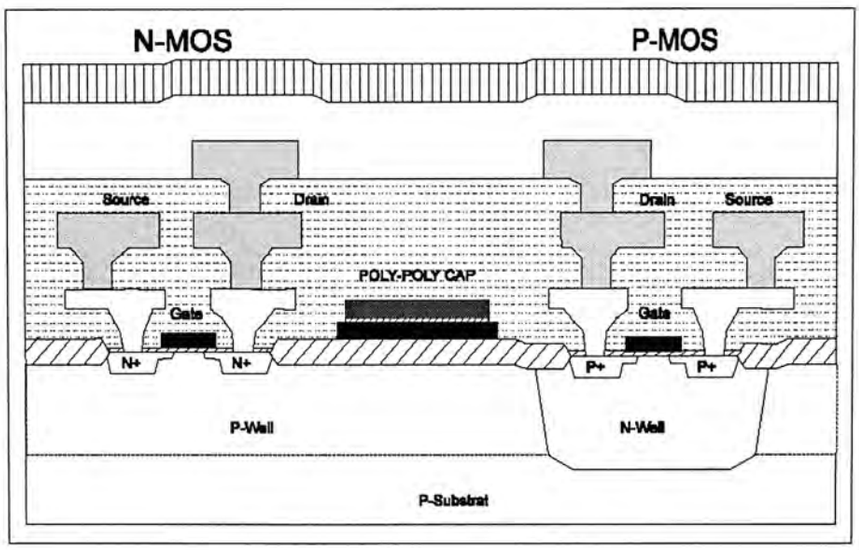

Figure 6.1: Wafer cross-section diagram in AMS CMOS CUP 0.6μm Process

6.2 Substrate tap

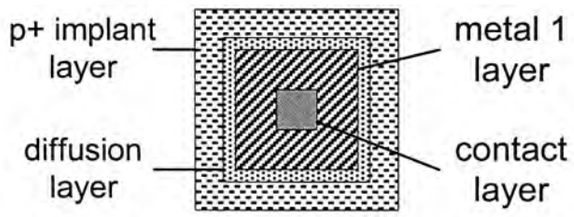

Figure 6.2: Layout of a substrate tape

In the AMS CMOS 0.6 CUP technology, p-type wafer is provided and

the n-channel MOSFETs are fabricated directly on the p-type wafer. Substrate taps must be provided to connect the p-type substrate to the ground.

6.3 Input protection circuitry

For those input pads which are directly connected to the gates of transistors, ESD (Electrostatic discharge) must be included in these pads in order to avoid the destruction of transistors due to gate-oxide breakdown by static electrical charge. This could easily happen when the static charge stored in the gate capacitance of a transistor and hence the E-field generated exceeds some certain values. The oxide insulating properties break down and the transistor no longer functions properly.

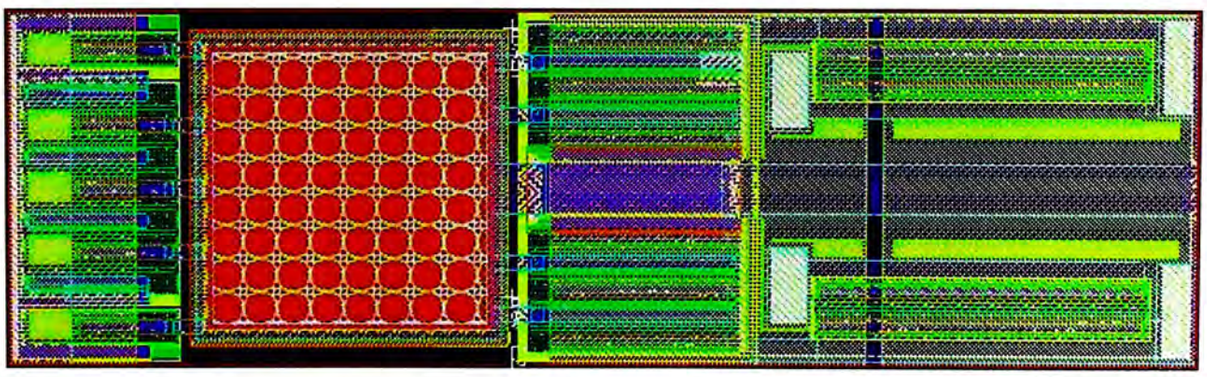

Figure 6.3: The physical layout of the I/O pad IOA5P

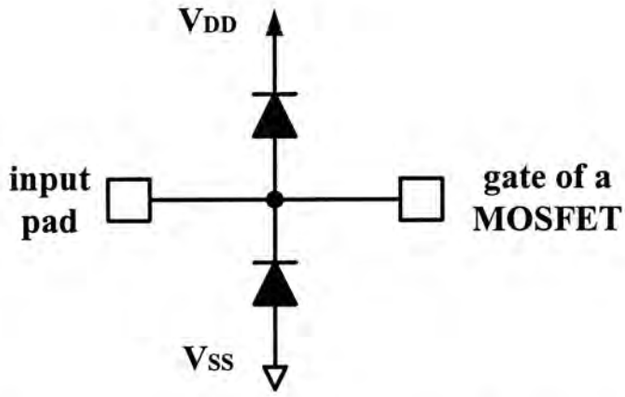

Figure 6.4: The schematic diagram of the I/O pad IOA5P

The analog I/O pad IOA5P [27] is used in this project, the physical layout and the schematic diagram are shown in Figure 6.3 and Figure 6.4. IOA5P is an analog input/output pad cell with zero ohms series resistor and CLAMP diodes. The working principle of this circuit is very simple, the two diodes form alternate charge flow paths when a very large voltage is applied to the input pad. One of the diodes will forward bias to discharge the extra energy into ground or power supply.

6.4 Die micrographs of the OTA

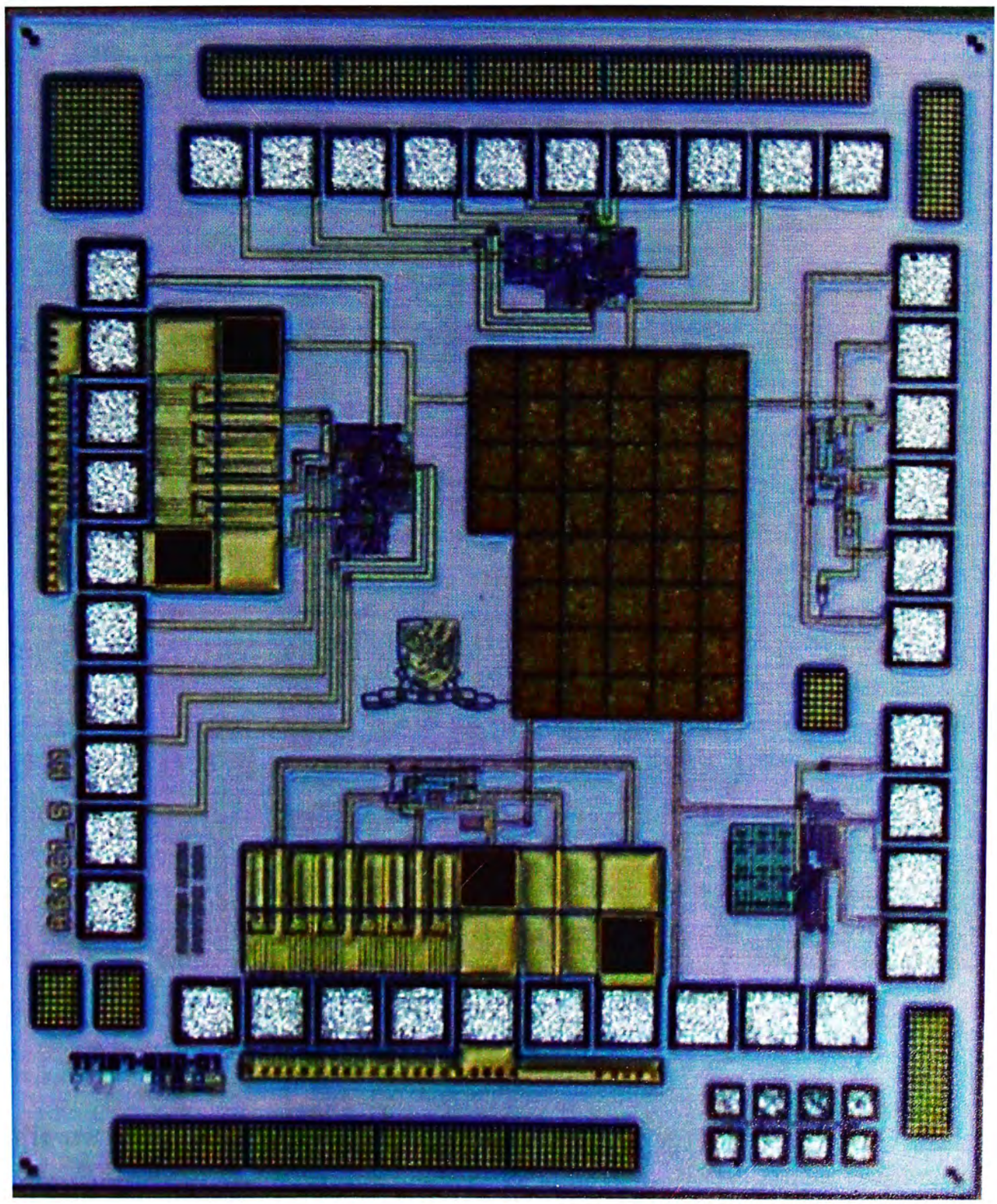

Figure 6.5: Micrograph of the die

Figure 6.5 shows the micrograph of the die, there are 5 circuits on the die and only two (the one at the top and on the left) are belonged to this

project.

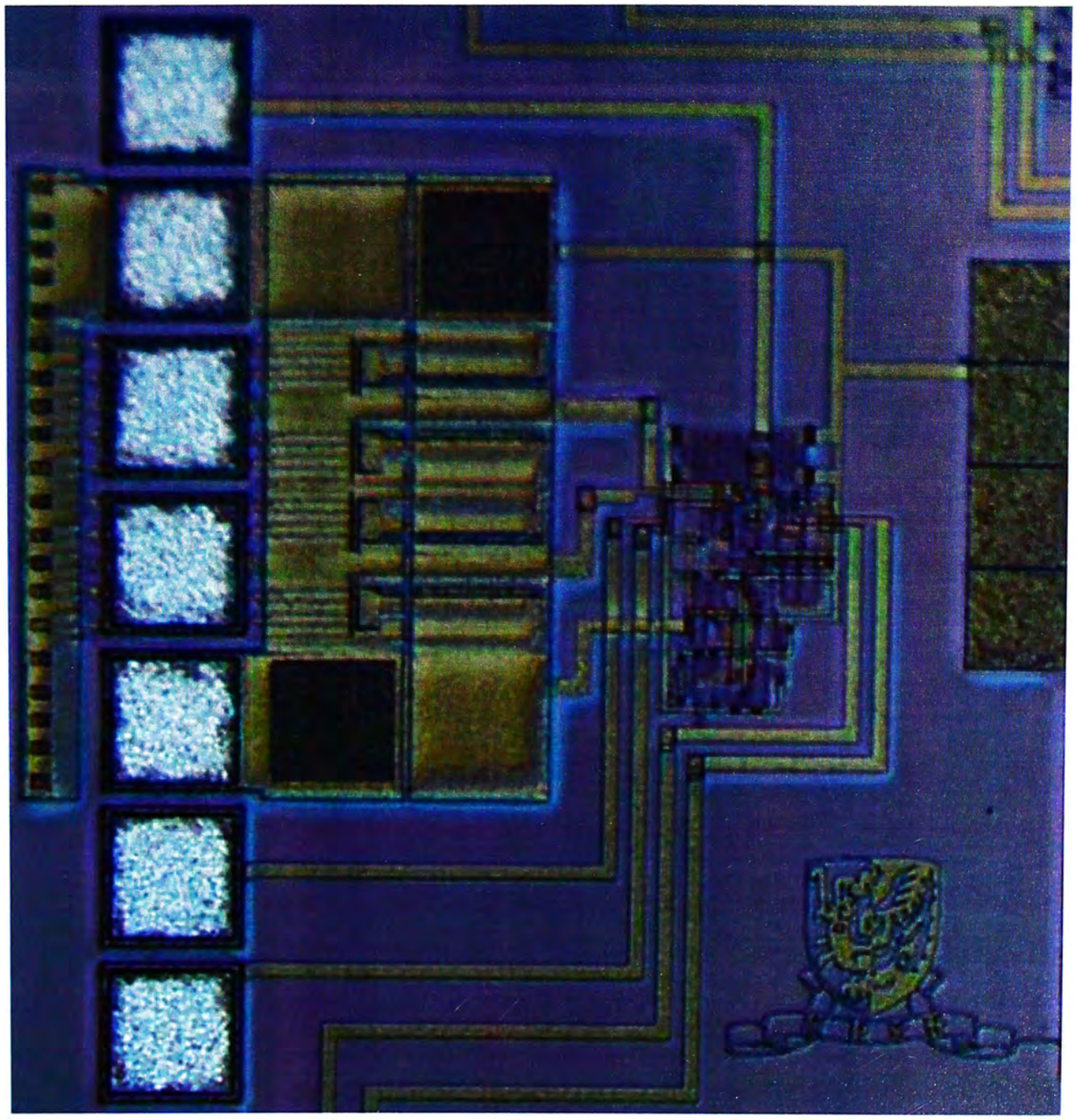

Figure 6.6: Micrograph of the OTA with ESD pad

Figure 6.6 shows the micrograph of the OTA with the ESP I/O pads. Figure 6.7 shows the micrograph of only the OTA, the circuit area is 212μm × 120μm.

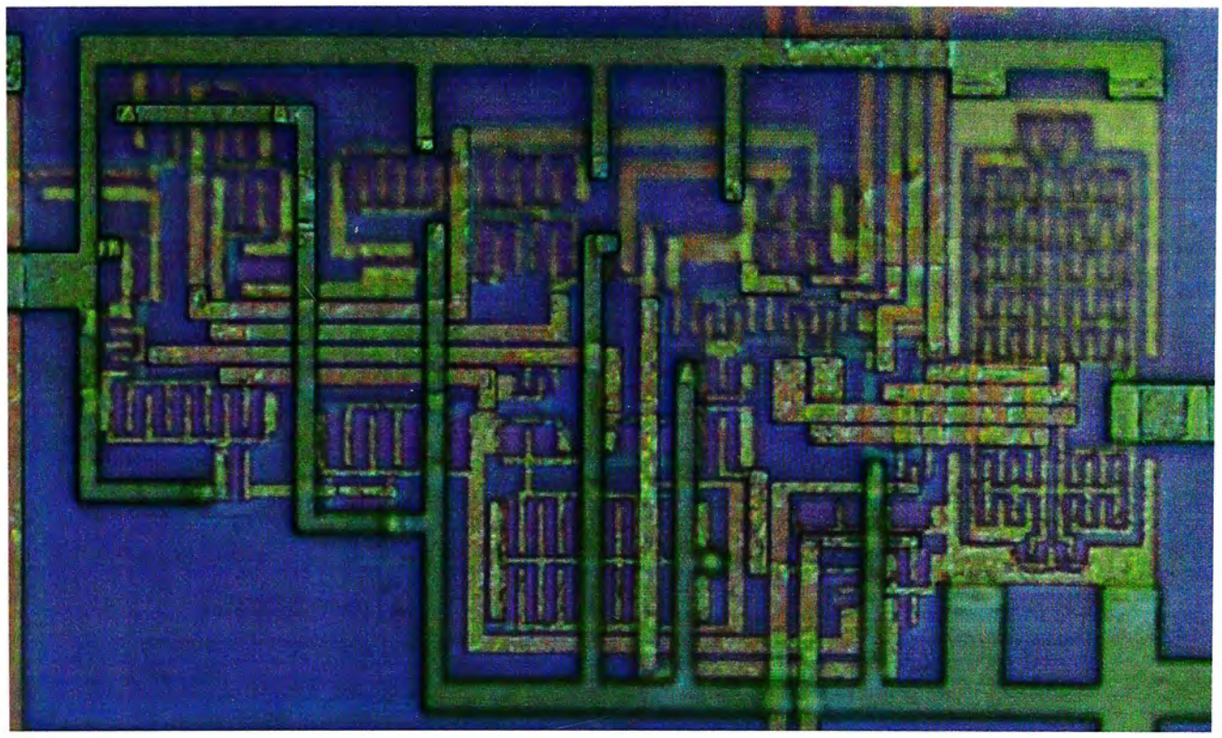

Figure 6.7: Micrograph of the OTA

Chapter 7 Measurement Results

7.1 Introduction

In this chapter, we will present the measurement results of the new g_m controlled OTA. All the equipment used in the experiment are shown in Table 7.1.

Equipment	Model
DC power supply	HP E3631A
Multimeter	HP 34410A
Signal generator	Rohde&Schwarz SML01
Function generator	Hameg HM8130
Oscilloscope	HP infinium oscilloscope (500MHz)

Table 7.1: The equipment used in the experiment

7.2 DC bias measurement results

7.2.1 Total transconductance variation

As we have discussed at earlier chapter, the transconductance is highly dependent on the drain current of the input differential pairs. The schematic diagram of measuring the drain current is shown in Figure 7.1. A multimeter HP 34410A with a sensitivity of 0.1μA is used for this measurement. The measurement result is shown in Figure 7.2.

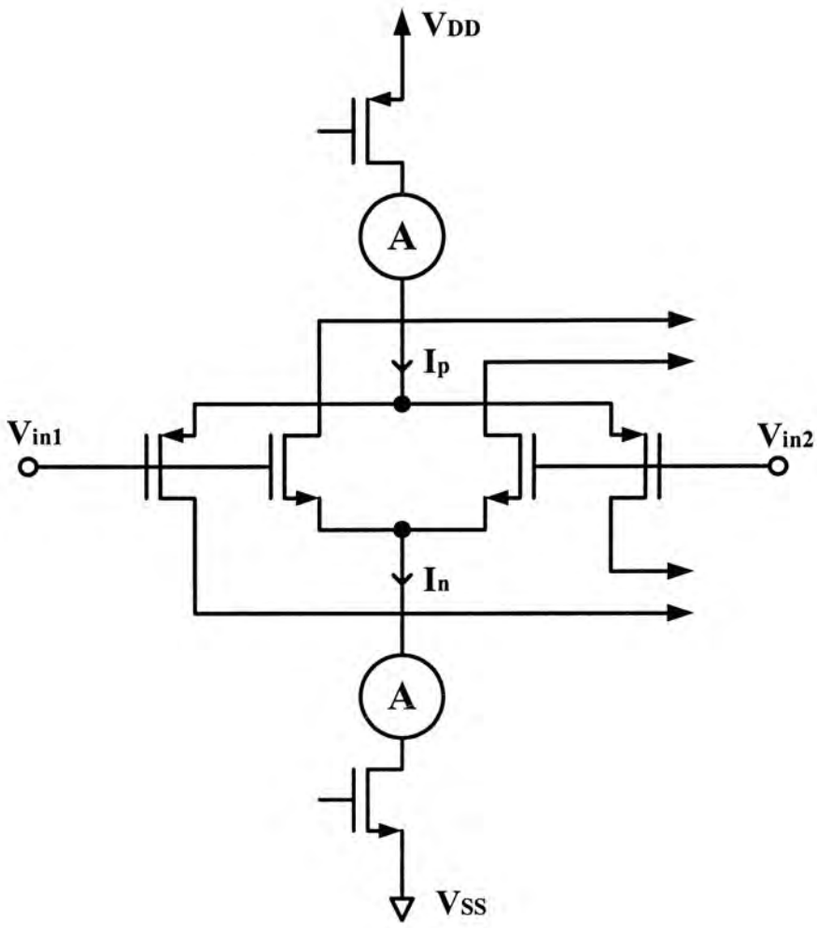

Figure 7.1: The schematic of measuring the drain current

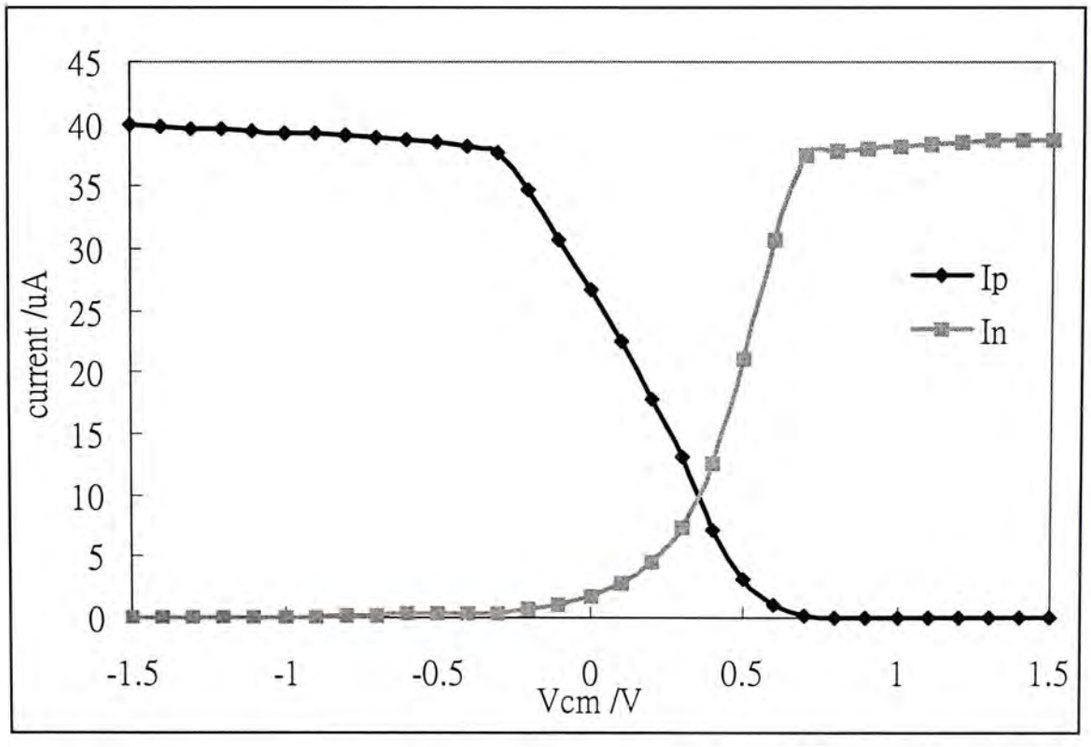

Figure 7.2: The drain current of the input pairs over the common mode range

To measure the transconductance of a transistor, whose source terminal is connected to a fixed voltage, one can simply increment the gate voltage and observe the change in the drain current. That is, g_m of the transistor at $V_g = V_{g0}$ can be found by sweeping V_g from $V_{g0}-\Delta V_g/2$ to $V_{g0}+\Delta V_g/2$ and measuring I_d at each V_g. Then,

$$g_m = \frac{\Delta I_d}{\Delta(V_g - V_s)} \tag{7.1}$$

The measurement result of the transconductance is shown in Figure 7.3. The variation on the overall transconductance of the proposed architecture is 6.54%. The difference is caused by the resistance and bias current.

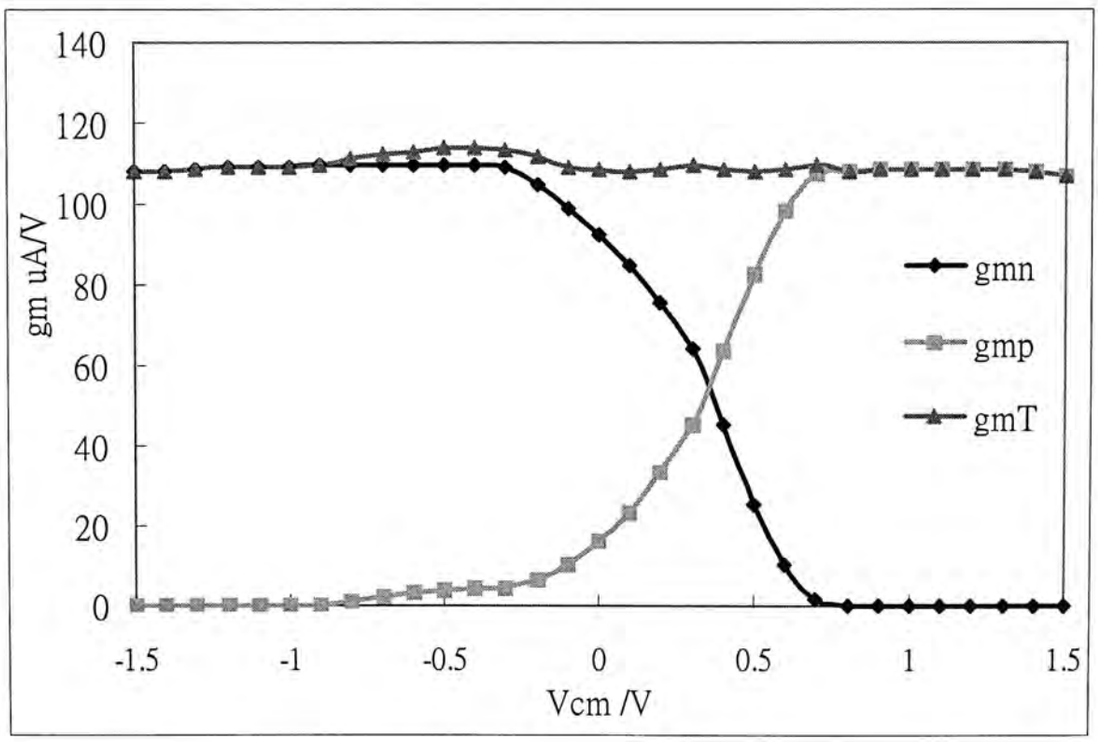

Figure 7.3: The transconductance of the input pairs over the common mode range

The comparison between the measurement and simulation results is shown in Figure 7.4. They got the same shape over the common mode

range, the only difference is the amplitude level of measurement is smaller.

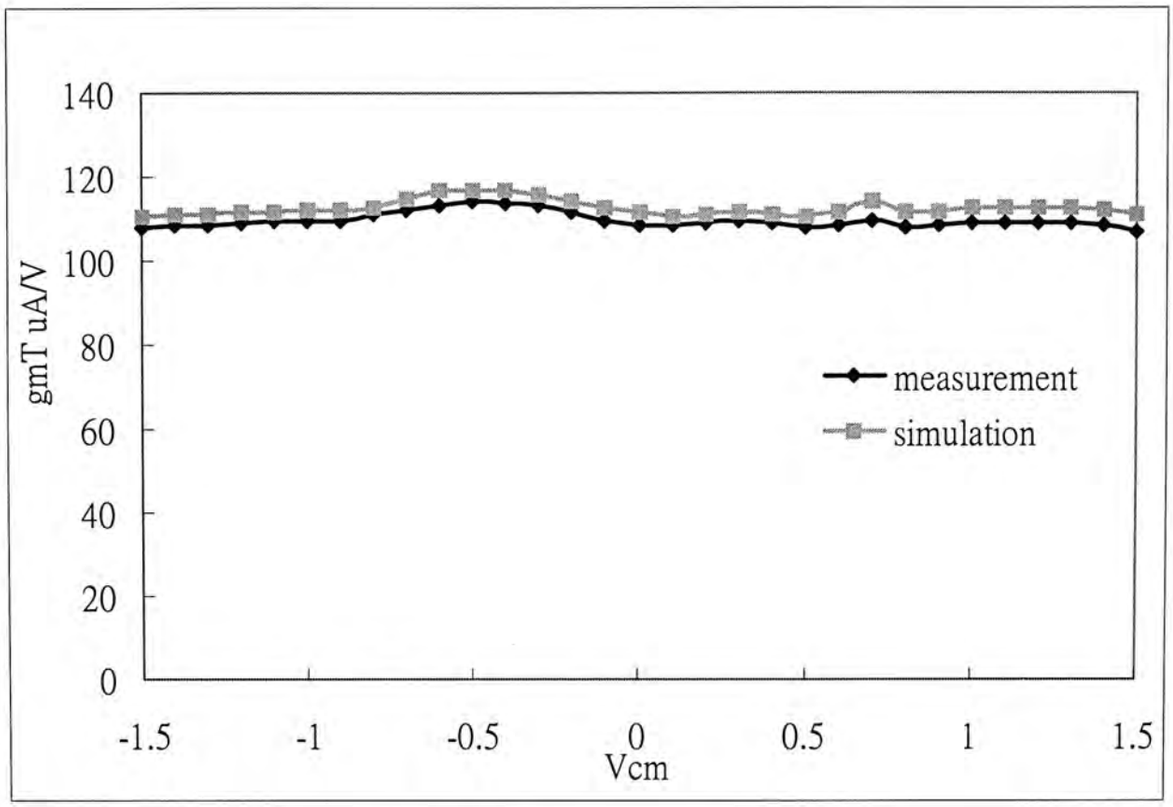

Figure 7.4: The results of the measurement and simulation on the g_{mT}

7.2.2 Power consumption

The measured DC current is equal to 0.284mA at +/-1.5V supply, thus the power consumption of the operational amplifier at a +/- 1.5V supply is 0.852mW.

7.3 AC measurement results

7.3.1 Open-loop gain

The open-loop gain is measured buy using the test circuit shown in Figure 7.5 [28]. In the test circuit, there is a buffer in the feedback loop. This extra buffer does provide the feedback signal, but the input signal can never pass through the buffer.

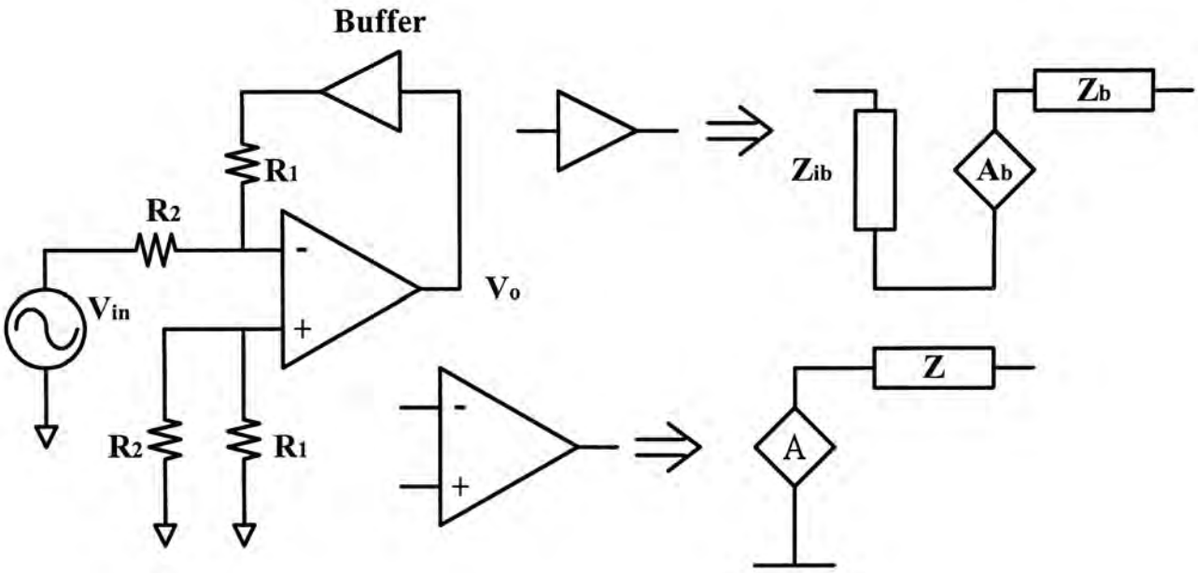

Figure 7.5: Test circuit for open-loop gain measurement

The open-loop gain and the output impedance of the operational amplifier (A and Z), the input impedance, the output impedance and the open-loop gain of the buffer are Z_{ib}, Z_b and A_b. If we assume that (with an error of 1%)

1. $R_1 > 100Z_b$
2. $Z_{ib} > 100Z_b$
3. $Z_{ib} > 100Z$

The following equation can be written:

$$V_o\left(1-\frac{Z}{Z_{ib}}\cdot\frac{A_b}{1+A_b}\right)=V_-\cdot\left(\frac{Z\cdot Z_b}{Z_{ib}\cdot R_1}-A+\frac{Z_b\cdot Z}{Z_{ib}\cdot R_1}\cdot\frac{A_b}{1+A_b}\right) \tag{7.2}$$

The maximum value of $A_b/(1+A_b)$ is unity. For the worst case,

$$V_o\left(1-\frac{Z}{Z_{ib}}\right)=V_-\cdot\left(2\frac{Z\cdot Z_b}{Z_{ib}\cdot R_1}-A\right) \tag{7.3}$$

Assuming,

$$A>200\cdot\frac{Z\cdot Z_b}{Z_{ib}\cdot R_1} \tag{7.4}$$

The transfer function between V_o and V- is finally given by

$$V_o=-A\cdot V_- \tag{7.5}$$

The circuit board for this measurement is shown in Figure 7.6, the buffer used in the experiment is Intersil 3140E. The measurement result of the frequency response with V_{cm} equal to 0V is shown in Figure 7.7, which shows that the open-loop gain is 65.4dB at 10Hz with gain-bandwidth product 1.68MHz.

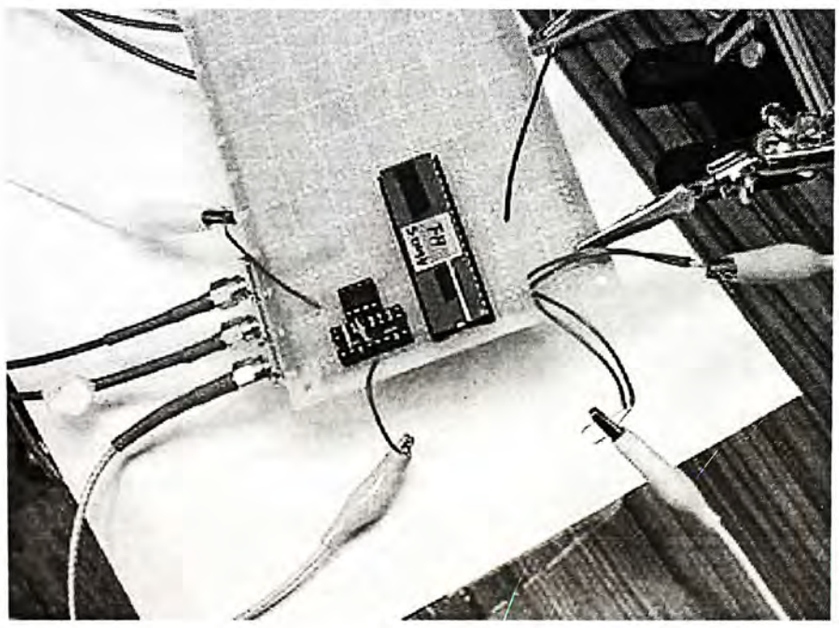

Figure 7.6: The circuit board for the open-loop gain measurement

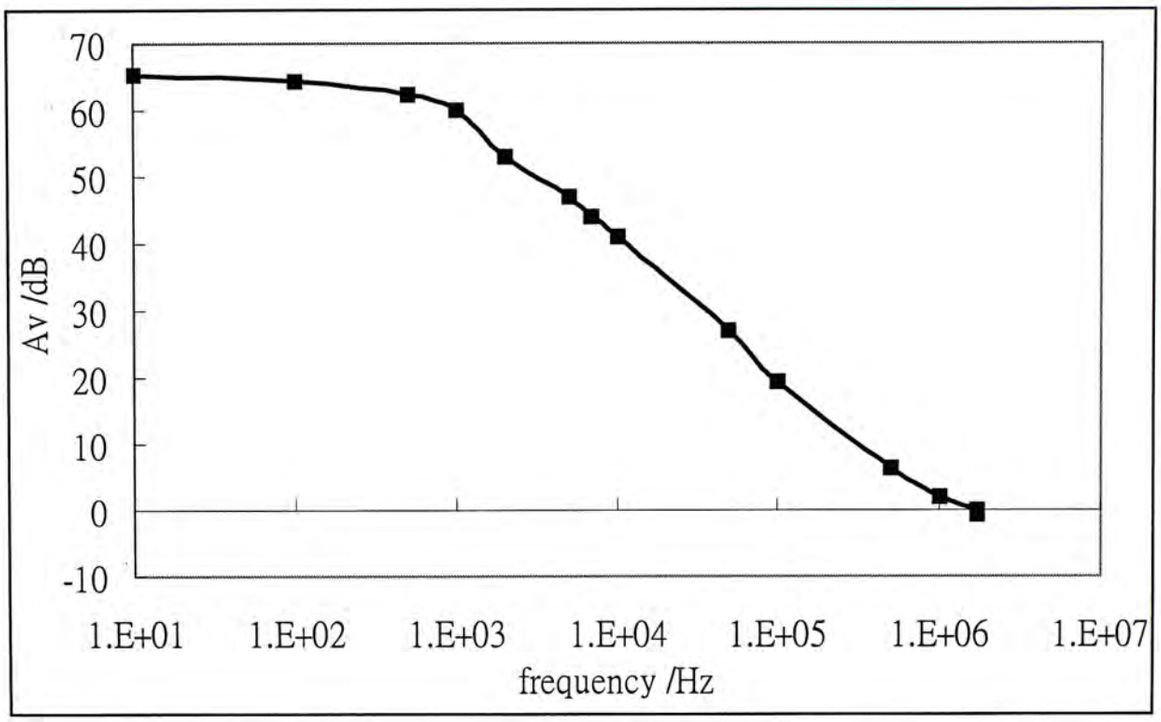

Figure 7.7: The frequency response of the OTA with V_{cm} equal to 0V

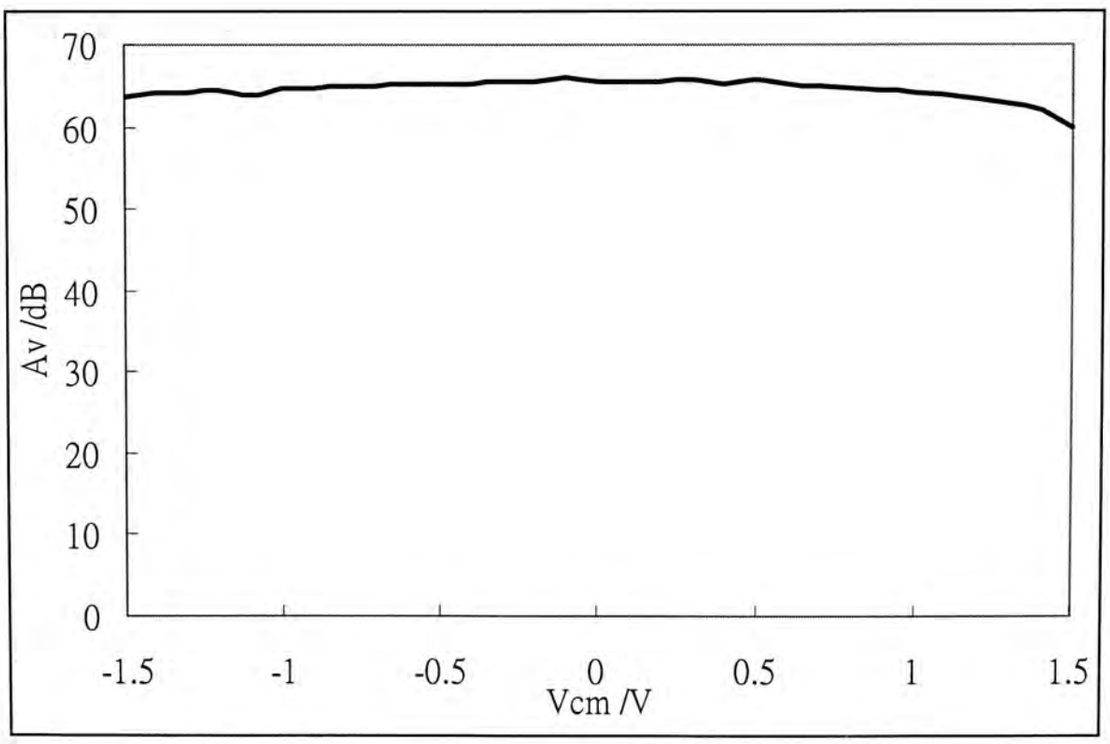

Figure 7.8 : The open-loop gain of the OTA over the common mode range

The open-loop gain of the OTA over the common mode range is shown in

Figure 7.8, we can see that the open-loop gain is almost constant (65dB). The drop of the open-loop gain is mainly due to the drop of the overall transconductance.

7.3.2 *Gain-bandwidth product*

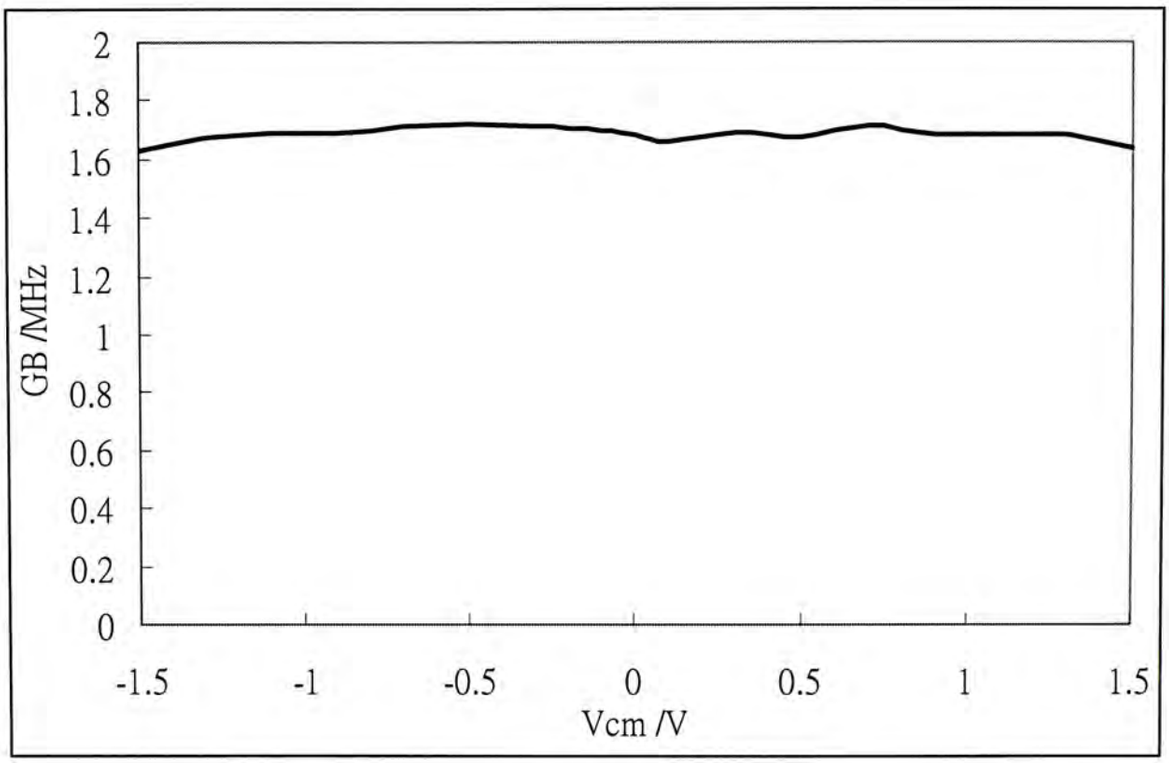

Figure 7.9: The gain-bandwidth of the OTA over the common mode range

The measured gain-bandwidth product over the common mode range is plotted is Figure 7.9. It shows that there is a variation about 6.9% on the gain-bandwidth product which the minimum value is 1.63MHz and the maximum value is 1.72MHz.

7.3.3 *Phase margin*

The phase margin can be calculated based on overshoot measurement [29] which will be shown in the next section. For phase margin calculations, use the following:

$$Percentage\ Ovreshoot = e^{\frac{-\pi\xi}{\sqrt{1-\xi^2}}} \tag{7.6}$$

$$\Phi_m = \tan^{-1}\left(2\xi\sqrt{\frac{1}{\sqrt{4\xi^4+1}-2\xi^2}}\right) \tag{7.7}$$

The overshoot measured was 2.687% and ξ = 0.755, resulting in a measured phase margin of 67.89°.

7.4 Transient measurement result

7.4.1 Voltage follower

The circuit board of the voltage follower is shown in Figure 7.10. The experimental setup for the measurement of the transient response is shown in Figure 7.11.

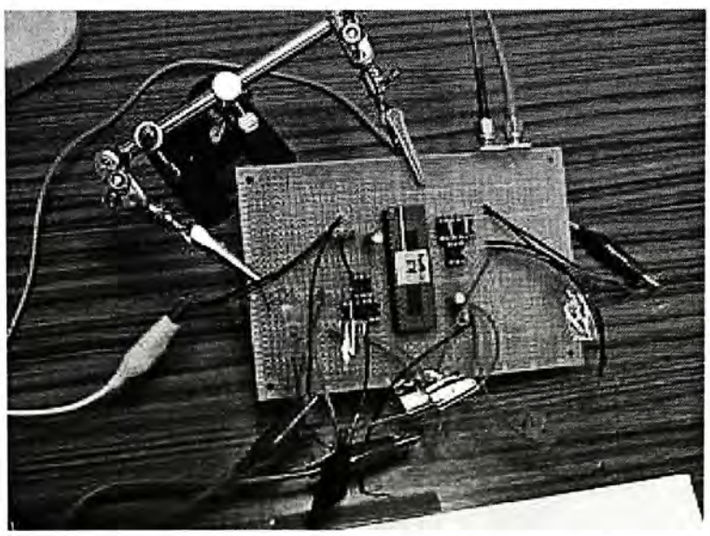

Figure 7.10: The circuit board of the voltage follower

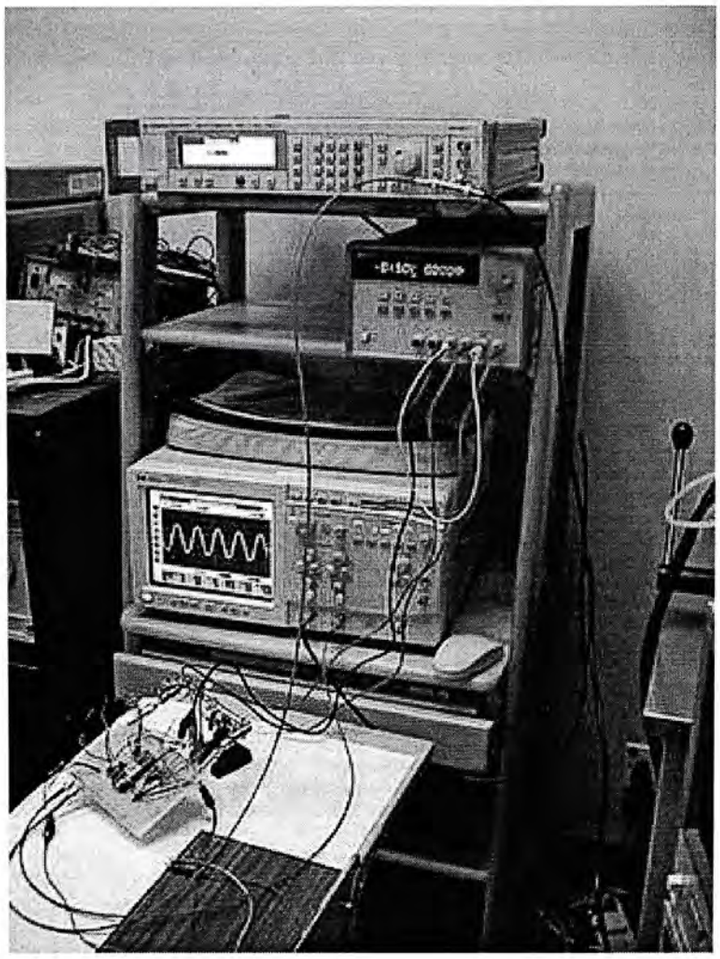

Figure 7.11: Experimental setup for the transient response

Figure 7.12 shows the measurement result on the voltage follower with a $0.5V_{p\text{-}p}$ 100kHz sine wave input signal. The relationship of the input voltage and output voltage is shown in Figure 7.13.

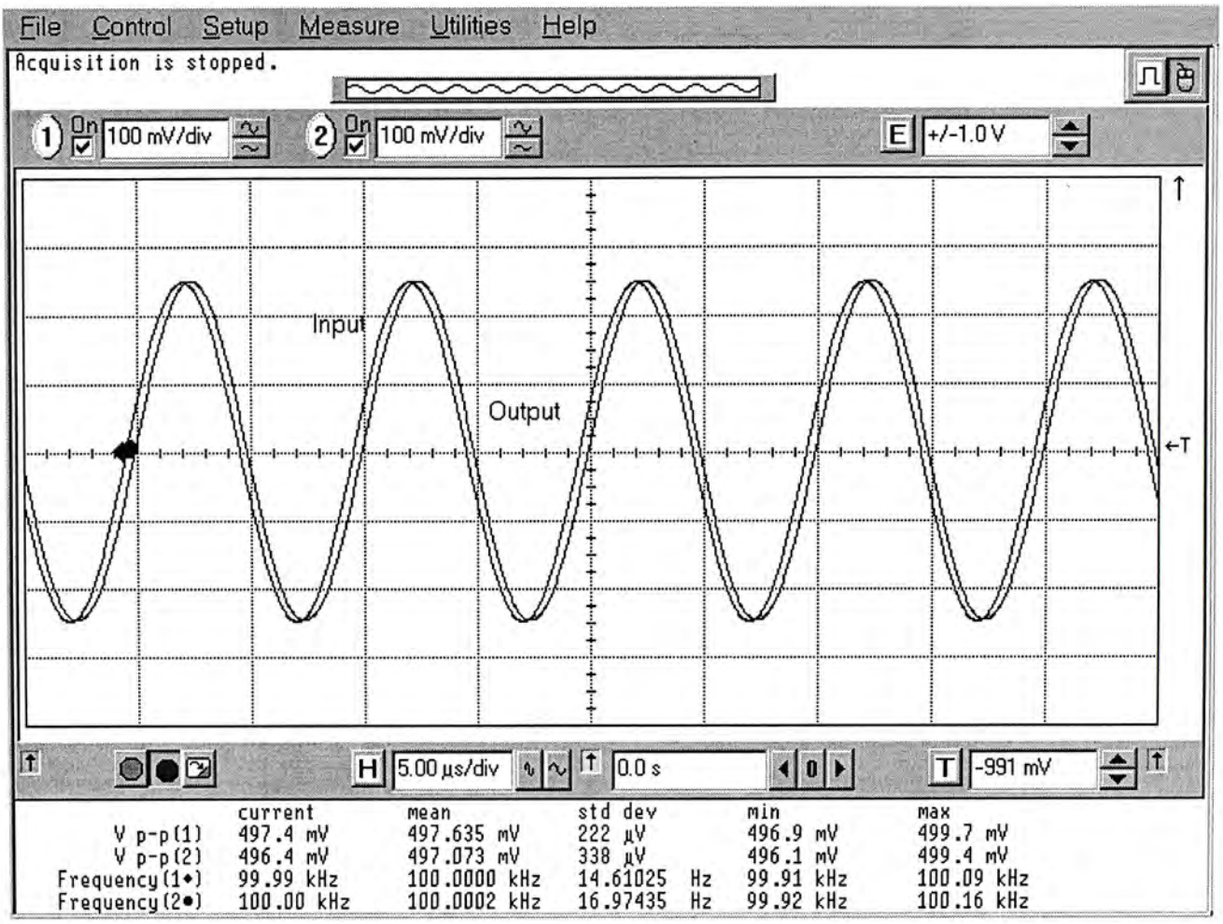

Figure 7.12: The transient response of the OTA in the voltage follower with a $0.5V_{p-p}$ 100kHz sine wave

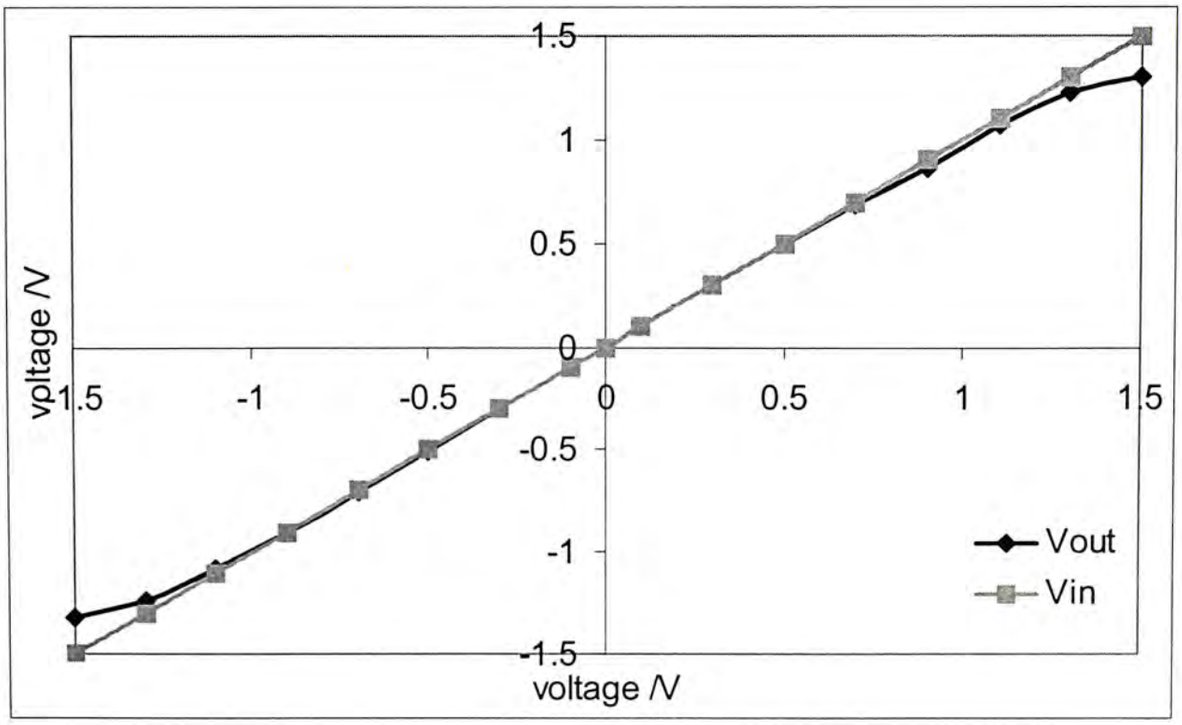

Figure 7.13: The input and output voltage characteristics of the voltage follower

Figure 7.14 shows the measurement result on the voltage follower with a $0.59V_{p-p}$ 1.68MHz sine wave input signal, which is the maximum operating frequency of the OTA, the output signal is 3dB less than the input signal which means the amplitude of the output is 0.707 of the input.

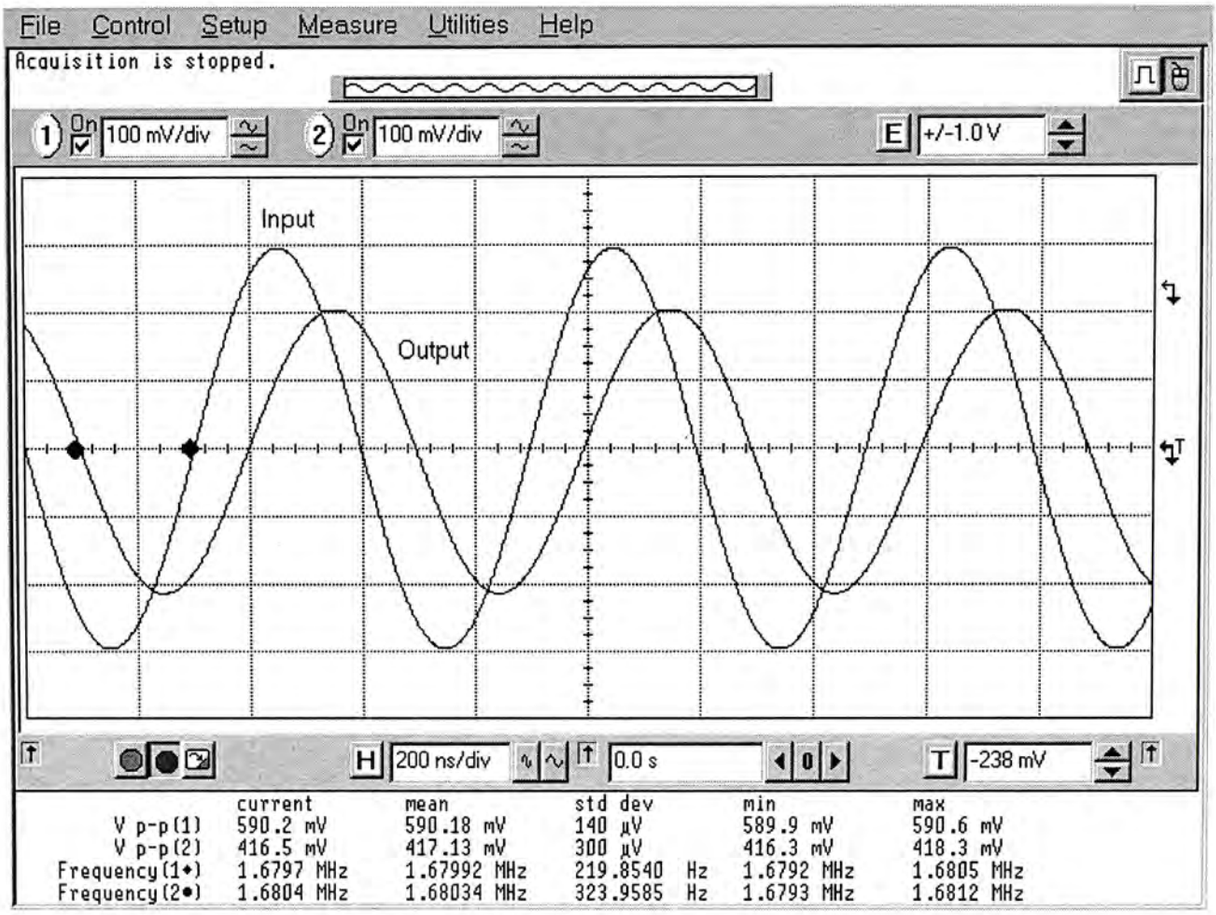

Figure 7.14: The transient response of the OTA in the voltage follower with a $0.59V_{p-p}$ 1.68MHz sine wave

7.4.2 Total harmonic distortion

The measured total harmonic distortion is shown in Figure 7.15. The result is come from the function of Fourier Transform given by HP infinium oscilloscope (500MHz) on an input signal of $0.2V_{p-p}$ and 100kHz sine wave.

Frequency	Amplitude level	
	Input	Output
100kHz (main tone)	-11.58	-11.67
200kHz (2nd harmonic)	-53.41	-53.21
300kHz (3rd harmonic)	-56.22	-55.82

Table 7.2: The harmonic distortion of the voltage follower

The total harmonic distortion can be found by equation (2.28) with the data given in Table 7.2. It is found to be 0.033%

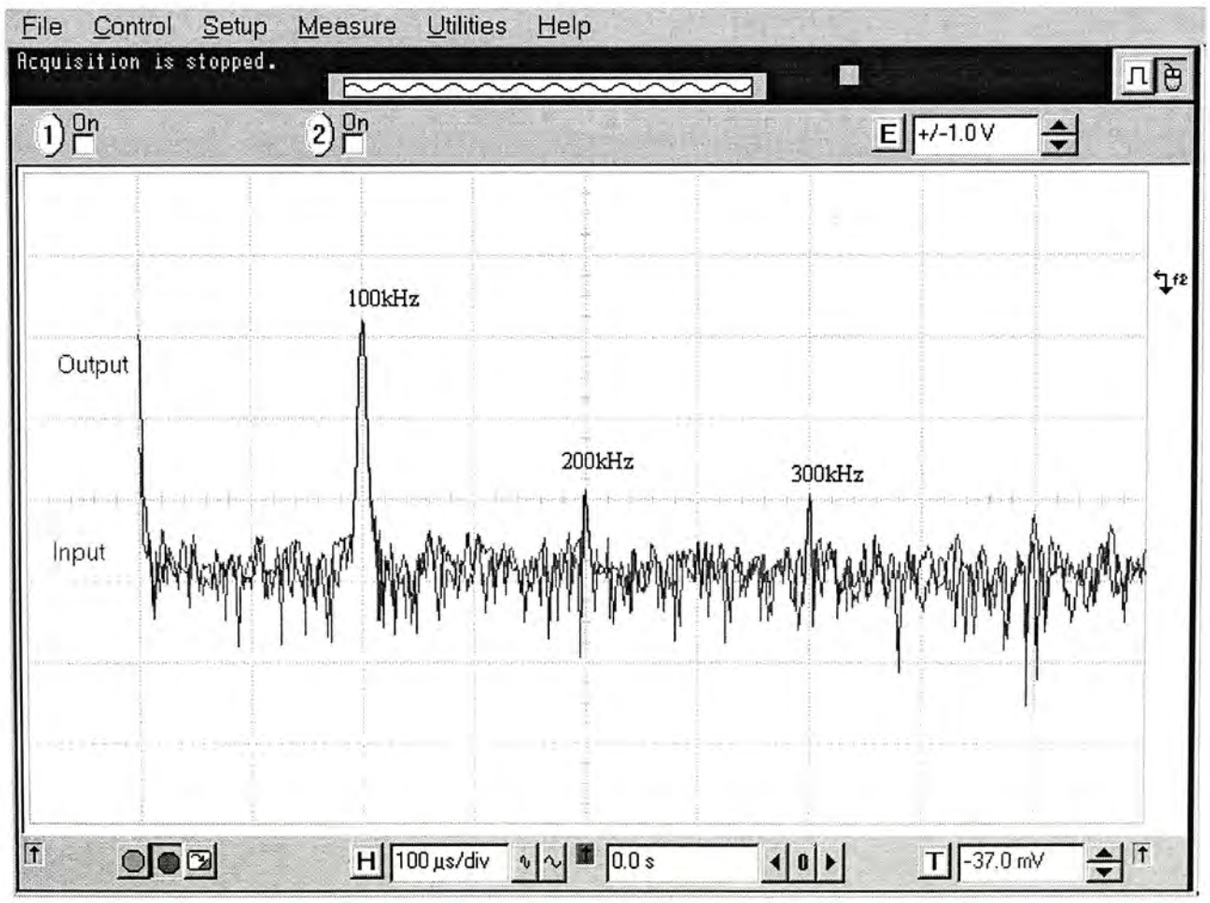

Figure 7.15: The measurement result of total harmonic distortion with a input $0.2V_{p-p}$ 100kHz sine wave

7.4.3 *Step response*

The measurement result of the overshoot is shown in Figure 7.16, the step input is a $1V_{p-p}$ (-0.5V to 0.5V) pulse signal. The maximum output is 0.52687V, thus, the overshoot is found to be 2.687%. The slew rate of the rising step is 20.5V/μs and the slew rate of the falling step is 26V/μs. This shows a large difference between the simulation result and measurement result. It is because the input impedance of the oscilloscope is 9pF and the bond pad gives 1pF more, so the loading capacitance of the voltage follower is 10pF which limits the slew rate. Table 7.3 shows the slew rate comparison between the simulation and measurement result with a 10pF load.

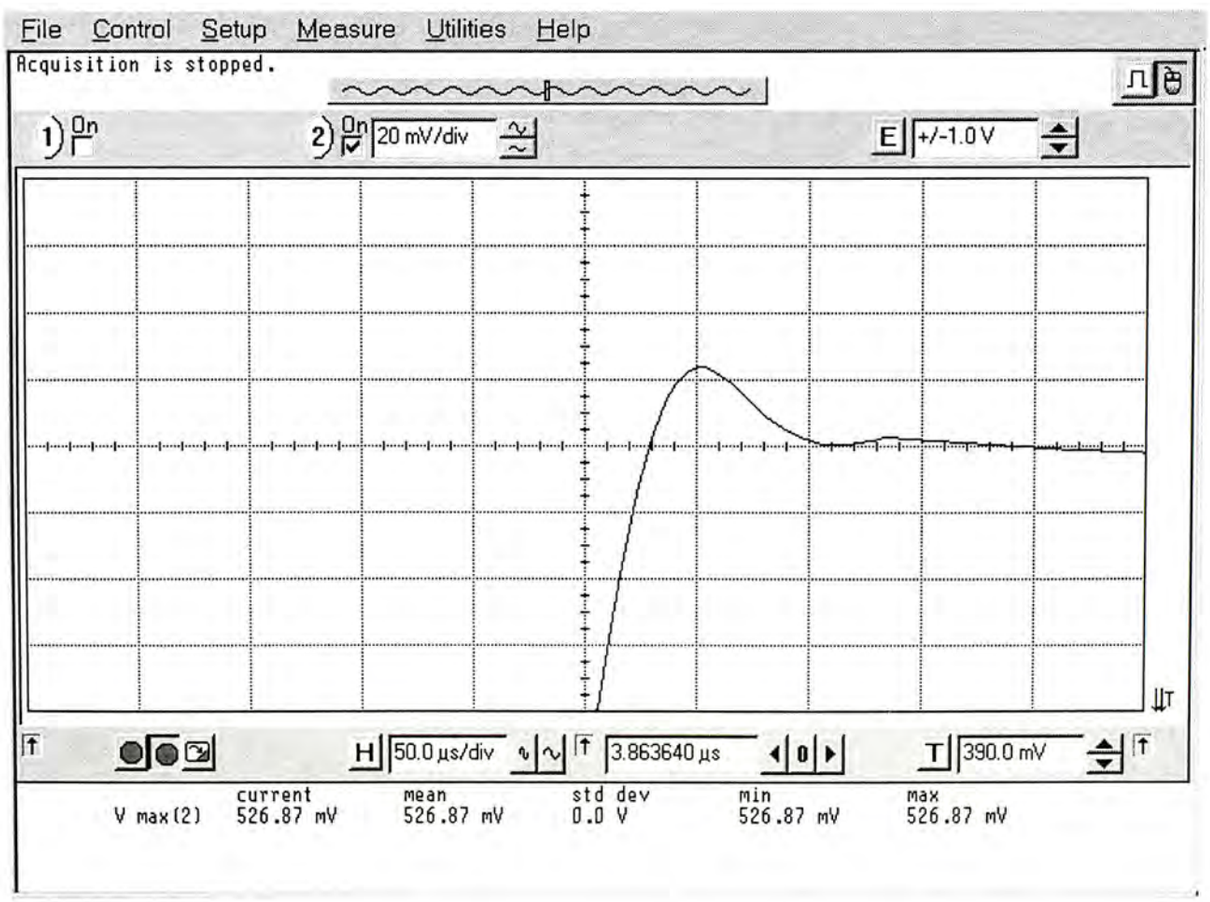

Figure 7.16: The overshoot of the step response

	Simulation	Measurement
Slew rate (rise)	22V/μs	20.5V/μs
Slew rate (fall)	33V/μs	26V/μs

Table 7.3: The slew rate comparison between simulation and measurement both with a 10pF load

7.5 Conclusion

In this chapter, all the measurement results are presented. The single stage operational transconductance amplifier with the proposed architecture can achieve constant-g_m over the whole common mode range with only 6.54% variation. To summarize, AC simulation results along with DC characteristics are shown in Table 7.4.

V_{DD} = 1.5V V_{SS} = -1.5V C_{load} = 10pF R_{load} = 10MΩ

Power consumption	0.85mW
g_{mT} variation	6.54%
DC open-loop gain (V_{cm}=0V)	65.4dB
Phase margin	67.89°
Slew rate (rise)	20.5V/μs
Slew rate (fall)	26V/μs
CMRR (V_{cm}=0V)	66.4dB
Gain-bandwidth product (V_{cm}=0V)	1.68MHz
Common mode input range	Exceeds both supply rails
Output swing	V_{SS}+0.19V, V_{DD}-0.2
DC offset	<2mV
THD	0.033%
Overshoot	2.687%

Table 7.4: Specifications of the single stage OTA with proposed architecture

Chapter 8 Conclusion

8.1 Contribution

This thesis presents the design of a single stage operational transconductance amplifier with a rail-to-rail constant transconductance input stage. A new constant-g_m bias circuit architecture is proposed and successfully implemented. It is fabricated in low-cost commercial CMOS 0.6μm process. We have found that the measurement results show good conformity with the simulation results. The OTA is designed to work at a 3V supply voltage.

The proposed architecture can achieve a constant overall transconductance over the whole common mode range with only 6.54% variation. It is much lower than those which operated in strong inversion and published before (about 10%). The total harmonic distortion is only 0.033% which is smaller than the conventional architecture [23] which is 0.047%.

The circuit area is only 212μm × 120μm and the power consumption is only 0.85mW. Even this is just a single stage OTA but we still can achieve an open-loop gain of 65.8dB at such a low power consumption level.

We have designed a new architecture of the input bias circuit for the rail-to-rail constant-g_m input stage OTA, which have compatible or better performance than other published bias circuit.

8.2 Further development

Since only one stage of OTA is designed and a folded-cascode gain stage is used which is suitable for capacitive loading only but not for resistive loading. If a resistive loading is preferred, then multi-stage may be needed, for example, a buffer may need to be added or a gain stage may be added so as to increase the overall gain. Moreover, the gain-bandwidth product is not large enough. It is because the GB is limited by the loading capacitance which is fixed by the bond pad capacitance and the input impedance of the equipment.

Furthermore, there is still a variation of about 6.54% on the g_{mT} over the common mode range. This is come from the assumption of the input pairs are either operated in strong inversion saturation region or turned off. But there is one more region that the input pair may operate which is strong inversion linear region, in such region g_m is not simply relate to the square root of the drain current. So a control circuit may be added such that it control the g_m of the transistors operated in linear region to be constant and a switch can be used to select the active control circuit.

Chapter 9 Appendix

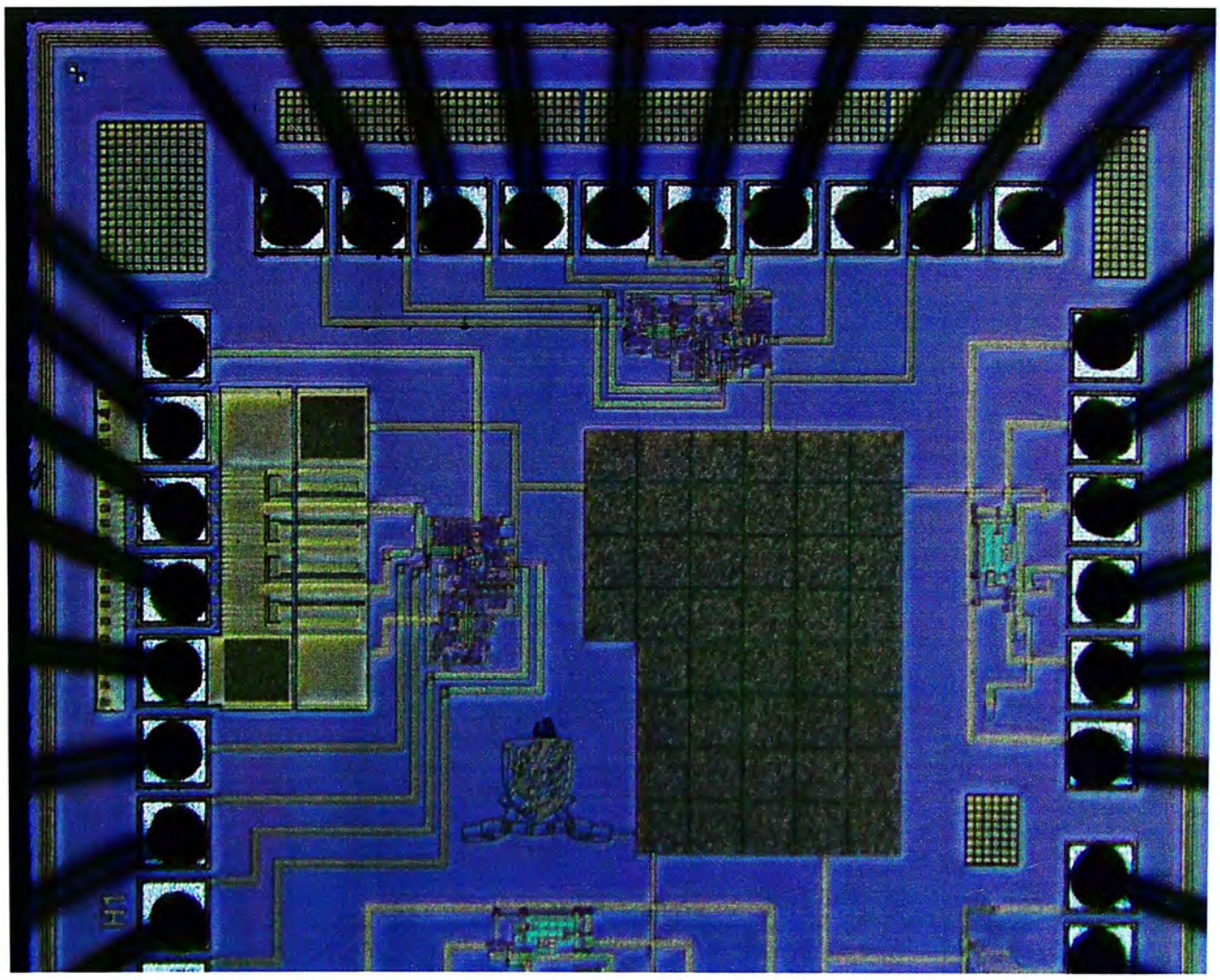

Figure 9.1: Micrograph of the chip with bonding wires

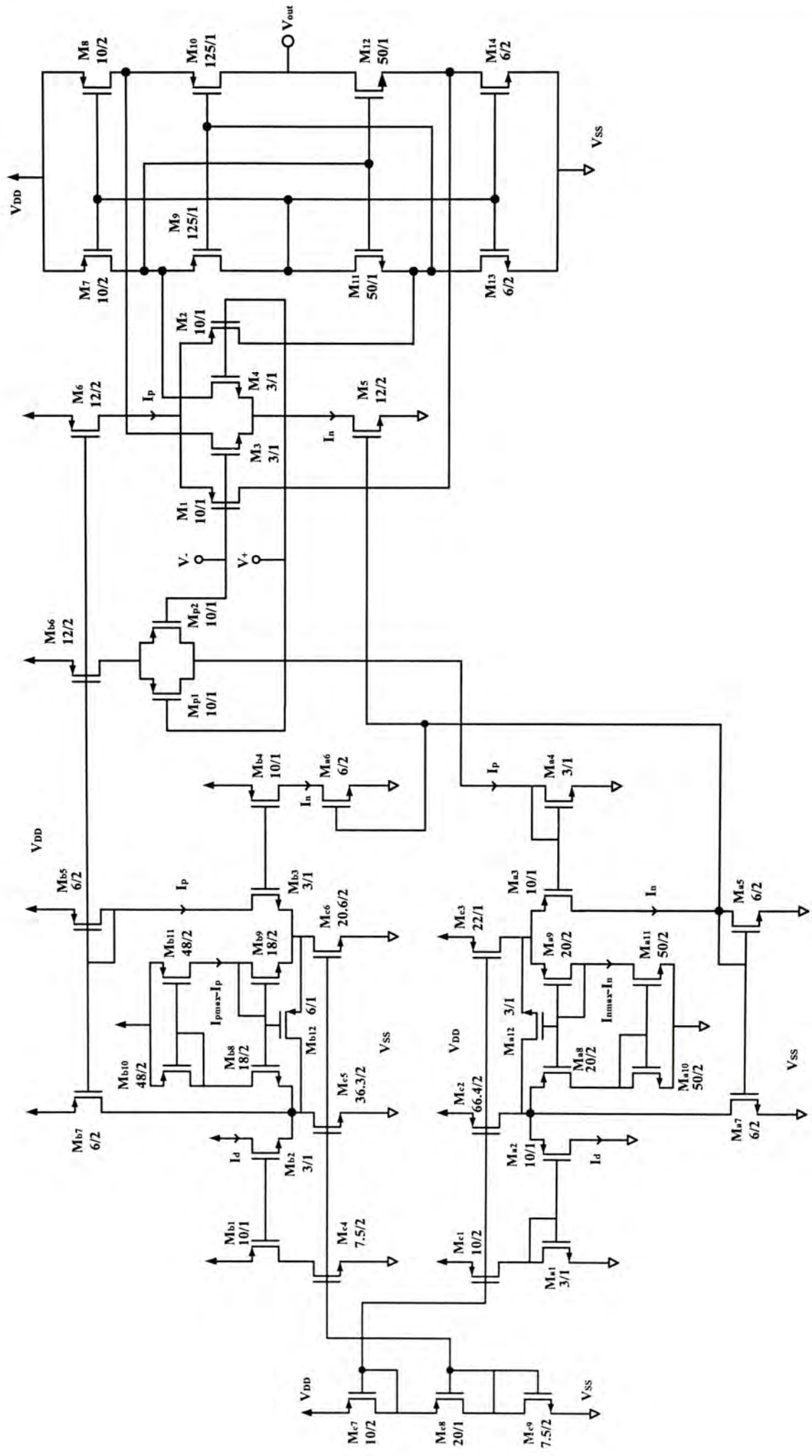

Figure 9.2: The full schematic diagram with physical sizes of the OTA

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