Frequency Compensation of CMOS Operational Amplifier

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Abstract

Abstract of thesis entitled:

Frequency Compensation of CMOS Operational Amplifier

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Cascode stages amplifiers is a classical approach of increasing the gain of an amplifier without deteriorating the frequency characteristics. This technique is commonly used in CMOS amplifiers to minimize the number of gain stages and keep the frequency compensation circuit simple. However, cascode is prohibited in many low voltage operations due to the relatively high voltage requirement. Thus, additional gain stages are necessary to counteract the gain loss and frequency compensation techniques are needed to shape the frequency response to stabilize the circuit under a large range of conditions.

This thesis presents two CMOS implementations of operational amplifier. Special designed frequency compensation circuits are used to solve the high stage count problem. The first design is a two-stage current feedback operational amplifier. The output voltage swing and open loop transimpedance gain are improved by the additional gain stage. Active current mode compensation is used to preserve the bandwidth in the presence of additional signal delay in the second stage. This compensation method uses embedded

current buffer that requires no additional components. Thus, the resulting circuit topology can be kept simple and power consumption is minimized.

The second design is a three-stage voltage feedback operational amplifier, which is stabilized by an improved version of reversed nested Miller compensation. The compensation method features sign inversion of the right half complex plane zero of reverse nested Miller compensation. The improvement in phase margin is converted to bandwidth and slew rate through the scaling down of compensation capacitors. Moreover, the compensation network multiplies the frequency of the complex conjugate poles and improves the transient response such as settling time. Although a nulling resistor is used, it is not a pole-zero cancellation technique and the nulling resistance is lower than the other nulling resistor based compensation scheme by a gain stage order. Thus, high precision and low resistive poly resistor can be used. As a result, gain-bandwidth product and slew rate is enhanced without any significant increase of power consumption and chip area.

The two operational amplifiers were fabricated with a 0.6μm CMOS technology and they were verified experimentally. In this thesis, the theories and measurement results for these two designs will be discussed with details.

摘要

於傳統的運算放大器中，疊接技術在不影響頻率反應的情形下，被廣泛利用於加強訊號的增益，這個技術在運算放大器中能減少增益級數和使頻率補償保持簡單。然而，疊接式放大器的操作需要相對地高的電壓，所以疊接式放大器在許多情況下受到限制。因此，多增益級數的運算放大器將會在低電壓運作的前題下被採納，而頻率補償技術會被應用於確保運算放大器的回授穩定。

本文將會介紹兩個由互補金氧集成電路技術所製成的運算放大器。於這兩個設計當中，頻率補償方法將會被提出，以解決多增益級數所帶來的回授穩定問題。第一個設計是一個兩級的電流回授運算放大器。附加的一個增益級數有利於增加輸出電壓的擺動範圍和整個放大器的開環增益。但因爲附加增益級會帶來信號耽擱，所以活躍電流模式補償會被用作保存頻寬。這個電流模式補償方法只需要一個電路嵌入的電流緩衝器所構成，因此不需要任何額外部分。這樣能夠使電路結構保持簡單，並且使電能消耗減到最低。

第二個設計是一個三級的電壓回授運算放大器，這是運用一個經改良的補償方法以確保回授穩定。這種補償方法的特性在於將相反巢窩式米勒補償中的正零倒置，使到相位邊緣有所改進，最後透過補償電容器值的減小，使額外的相位邊緣給轉換成頻寬和迴轉比率。此外，補償電路使複雜極的頻率成倍增加，這有助於放大器的瞬時回應如穩定時間。雖然補償電路中使用了一個電阻器，但這個補償方法並不是一般極零取消技術，而且電阻器的阻力值比其他以電阻器爲基礎的補償方法爲低。因此高精度的鈔電阻器能夠被使用。頻寬和回轉比率結果得到提升，而不需增加電能消耗和晶片面積。

這兩個運算放大器是利用 0.6 微米互補金氧集成電路技術所製成，他們的特性均在實驗上被驗証。在本文中，將會詳細討論這兩個設計的背後理論和測試結果將會。

Acknowledgements

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I also want to express my gratitude to all of my colleagues in the Chinese University of Hong Kong. They are my good companions and have given me much assistance in the course of my study in these two years.

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Chapter 1 Introduction

Overview

Operational amplifier describes an important amplifier circuit that can perform mathematical operations such as addition, subtraction, multiplication, division, differentiation and integration as illustrated in figures 1.1 to 1.5. Its applications involve audio and video amplifiers, filters, buffers, instrumentation amplifiers, oscillators and many other analogue circuits.

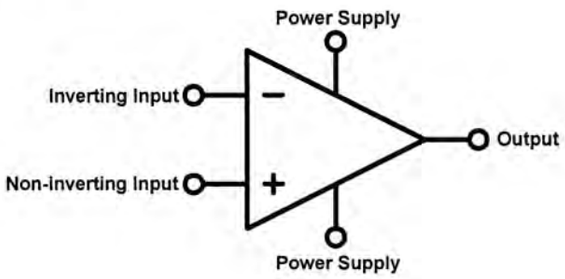


Figure 1.1: Symbol of Operational Amplifier

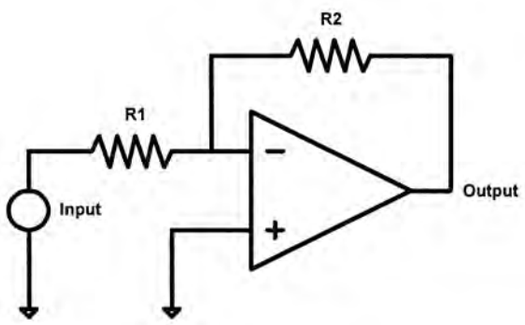


Figure 1.2: Inverting Amplifier

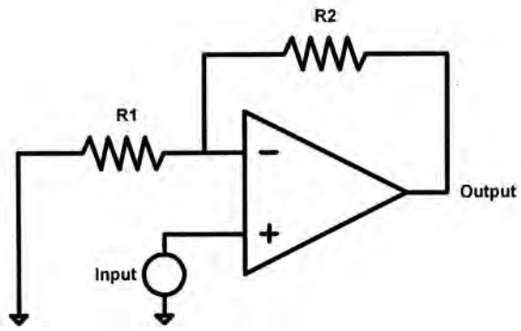


Figure 1.3: Non-inverting Amplifier

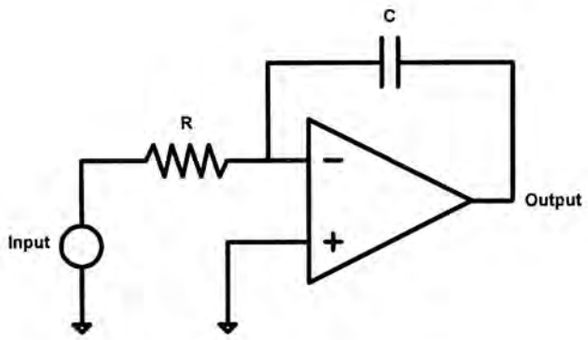


Figure 1.4: Integrator

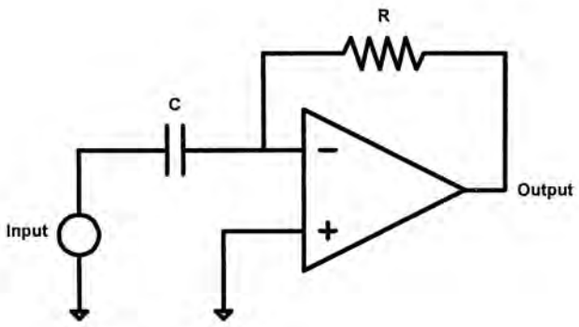


Figure 1.5: Differentiator

The operational amplifier must have feedback in order to perform useful functions. Most designs use negative feedback to control the gain and provide linear operations. Negative feedback is provided by components, such as resistors and capacitors, between the output and the inverting input of the operational amplifier. Positive feedback is only employed in some non-linear applications such as oscillator circuits.

Objective

Feedback systems involving operational amplifiers must ensure closed-loop stability. Operational amplifiers must have enough phase margin to prevent the application circuit from going into oscillation. Frequency compensation or phase compensation is the name given to the process of tailoring the gain magnitude/phase characteristics of the operational amplifier to give an adequate phase margin.

With the rapid decrease in the supply voltage in VLSI, a single stage cascode architecture is no longer suitable for operational amplifier design. Moreover, short-channel effect of the sub-micron CMOS transistor degrades output impedance and hence the gain of the amplifier [16]. Thus, multistage topology with cascaded wideband gain stages will become the main architecture in future operational amplifier design [8].

However, all multistage amplifiers suffer bandwidth reduction and closed-loop stability problems due to their multiple-pole nature. In this thesis, the stability problem of multistage operational amplifier is studied. Moreover, circuit topologies are derived to relax the stability requirement. Finally, analytical and experimental results are demonstrated for these new compensation methods.

Thesis Organization

Two main classes of operational amplifiers are studied in this project. They are the current feedback operational amplifier and voltage feedback operational amplifier.

This thesis is divided into 9 chapters. It starts with an introduction of the fundamentals of operational amplifiers in chapter 2. Definitions of the technical terms will be given here. In chapter 3, the operating principle and the design methodology of an actively compensated CMOS current feedback operational amplifier are discussed.

Moreover, voltage feedback operational amplifiers compensated by reversed nested Miller compensation and its improved version are compared in chapter 4 and chapter 5. Chapter 6 discusses the physical layout issues. All the measurement of the circuits designed in this project will be given in chapter 7. Finally, chapter 8 gives a conclusion about the research completed and the contribution in this project. The appendix and bibliography are in chapter 9 and chapter 10.

Chapter 2 Fundamentals of Operational Amplifier

2.1 Definitions of Commonly Used Figures

There are many different types of operational amplifier on the market. Hence, some considerations of performance parameters of each type of operational amplifier are needed. This chapter will describe the various operational amplifier specifications normally included in a manufacturer's data sheet. The significance of these parameters will also be discussed.

2.1.1 Input Differential Voltage Range

The voltage between the input terminals of an operational amplifier is left to a very small value by negative feedback. If negative feedback is not used, the differential input voltage may exceed this small value and the output of the operational amplifier will saturate.

The input differential voltage range is defined as the maximum differential signal that can be applied between the two inputs without driving the operational amplifier into saturation.

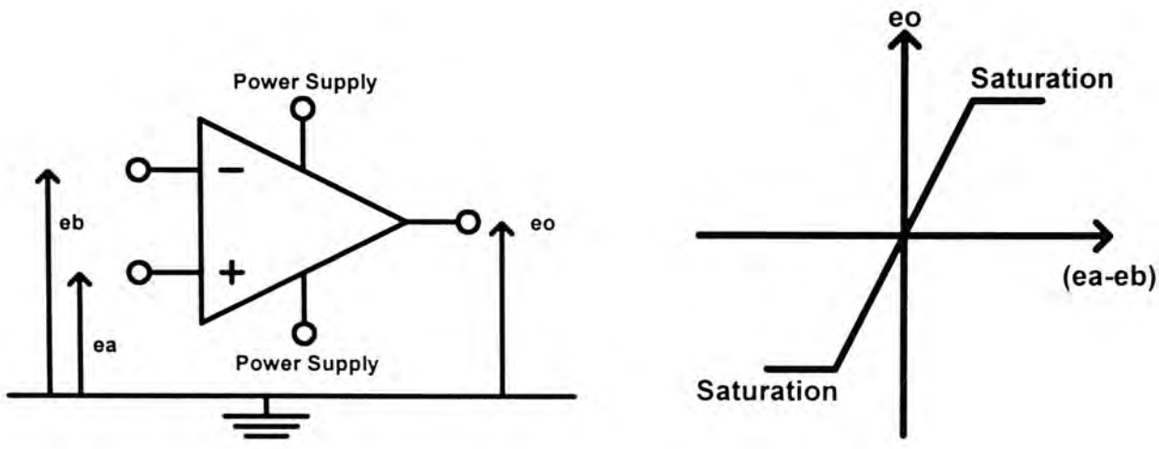


Figure 2.1: Ideal transfer curve for an operational amplifier

2.1.2 Maximum Output Voltage Swing

The maximum output voltage swing is the maximum change in output voltage (positive and negative), measured with respect to a reference potential. The value of maximum output voltage range is usually quoted under a specified load and power supply.

2.1.3 Input Common Mode Voltage Range

The common mode voltage is the average input voltage on the two inputs relative to each other.

This is the maximum positive or negative voltage that we can apply to an operational amplifier inputs without driving the operational amplifier into saturation.

2.1.4 Input Offset Voltage

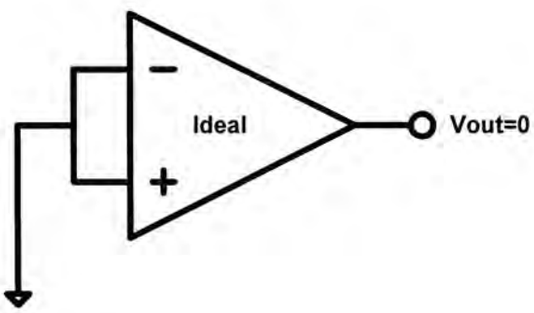


Figure 2.2: Ideal operational amplifier with zero output offset error

For a non-ideal operational amplifier, the output voltage is not equal to zero when the two inputs are connected together. One way to model this non-ideal output voltage is to reflect it back to the input as shown in figure 2.2 and 2.3, where figure 2.2 represents an operational amplifier with zero offset voltage.

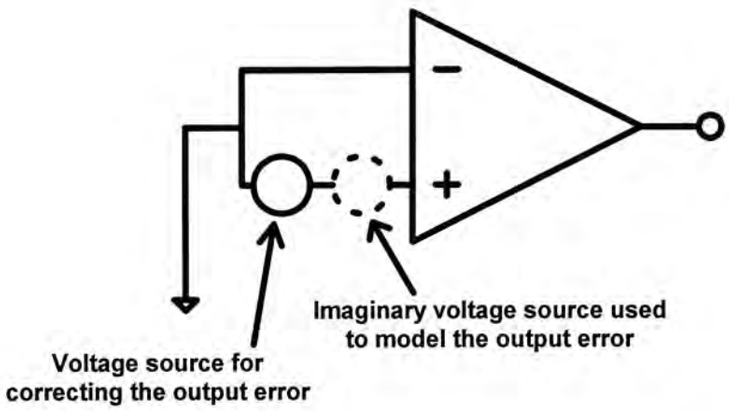


Figure 2.3: Operational amplifier with output error corrected

Input offset voltage is the DC voltage that must be applied between the input terminals of an operational amplifier to reduce the DC output voltage to zero. The input offset voltage is usually due to the mismatch between threshold voltages of the input MOS transistor pairs.

2.1.5 Gain Bandwidth Product

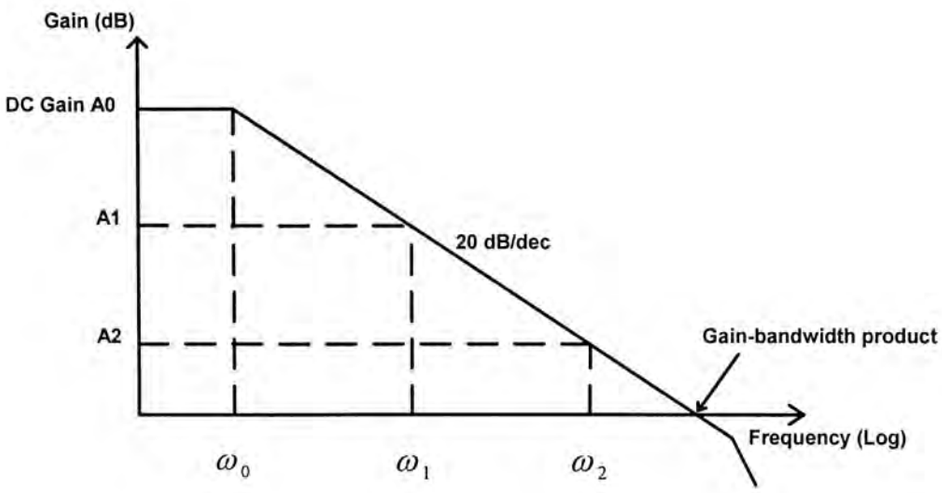


Figure 2.4: Gain magnitude of a typical operational amplifier

Gain bandwidth product can be described as the product of the open loop gain times the frequency of the dominant pole.

$$GBW = A_0\omega_0$$

Gain bandwidth product is constant for a given operational amplifier. The frequency response of an operational amplifier circuit depends only upon the gain bandwidth product and not upon the gain and the bandwidth individually.

$$A_0\omega_0 = A_1\omega_1 = A_2\omega_2$$

Hence, there is a trade-off between gain and bandwidth for a given operational amplifier design such as high gain at a lower frequency or lower gain at a higher frequency.

2.1.6 Phase Margin

Phase margin is defined as 180^o plus the phase angle of the transfer function $T(j\omega)$ at unity gain. For a stable system, it is necessary that the phase margin is greater than zero. A typical phase margin is greater than 45 degrees.

2.1.7 Slew Rate

Slew rate of an operational amplifier is defined as the maximum rate of change of the output voltage. Figure 2.5 illustrates an output caused by slew rate limitation. The triangular wave output is caused by the operational amplifier output simply cannot move fast enough to follow the sine wave input.

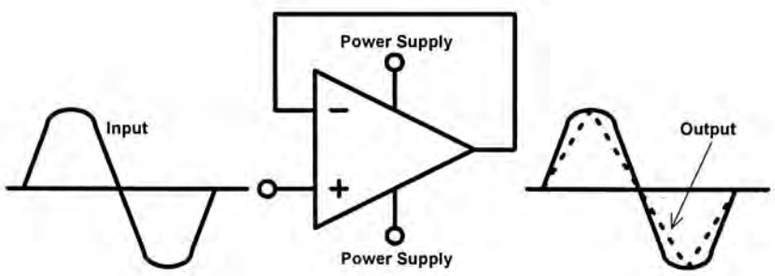


Figure 2.5: Voltage follower circuit with slew rate limited output

2.1.8 Settling Time

This is the time required for the output signal of an operational amplifier to settle within some defined error band of the steady state value. Typically, this band is $\pm 0.1\%$. This specification is very important for operational amplifier to be used in application such as Analog-to-Digital and Digital-to-Analog converters.

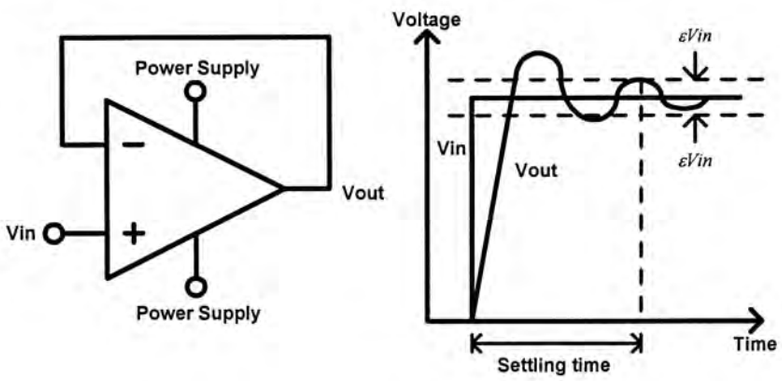


Figure 2.6: Settling time of an operational amplifier as a voltage follower

2.1.9 Common Mode Rejection Ratio

This is defined as the absolute value of the ratio of the differential open-loop gain to the common mode open-loop gain, expressed as

$$CMRR = \left| \frac{A_{Diff}}{A_{CM}} \right|$$

Or in decibels as

$$CMRR = 20 \log_{10} \left| \frac{A_{Diff}}{A_{CM}} \right|$$

2.2 Frequency Compensation of Operational Amplifier

2.2.1 Overview

An operational amplifier is first of all a DC amplifier. However, applications of operational amplifier usually involve feedback circuits. Thus, feedback stability is an important consideration for operational amplifier designs.

Frequency compensation circuit is used to shape the gain-magnitude and phase-angle frequency responses. The frequency compensation of an operational amplifier implies controlling the stability of the circuit by eliminating all higher order poles or pushing all higher order poles out of the unity gain frequency.

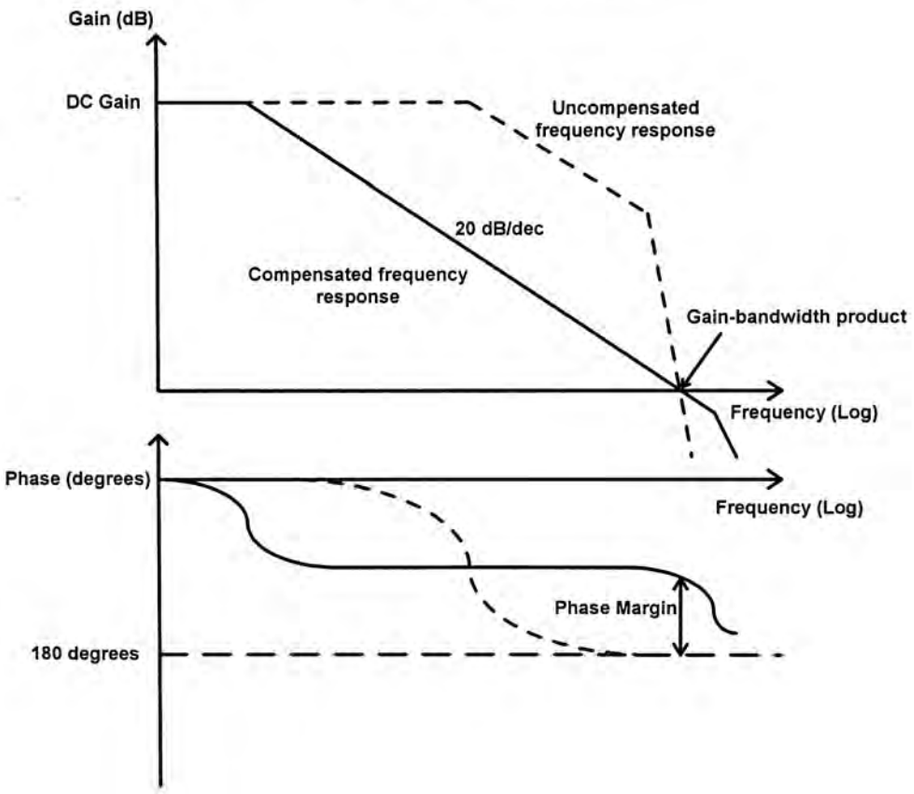


Figure 2.7: Frequency response of a two stages operational amplifier before and after compensation

The gain of an uncompensated operational amplifier is flat up to the first pole and then it falls off steeply because of the combined effect of high order poles. The phase

angle attains the critical value of -180^{o} at a gain greater than one as shown in figure 2.7. To make sure this operational amplifier is stable under any conditions, the first pole is pushed back to a low frequency while the second pole is pushed to a higher frequency as shown in the solid line of figure 2.7. This technique is known as pole splitting.

2.2.2 Miller Compensation

Miller theorem is an important compensation technique. Consider the situation shown in figure 2.8. An admittance Y is connected between nodes 1 and 2. Miller's theorem provides the means for replacing the admittance Y with two admittances: Y1 between node 1 and ground, and Y2 between node 2 and ground.

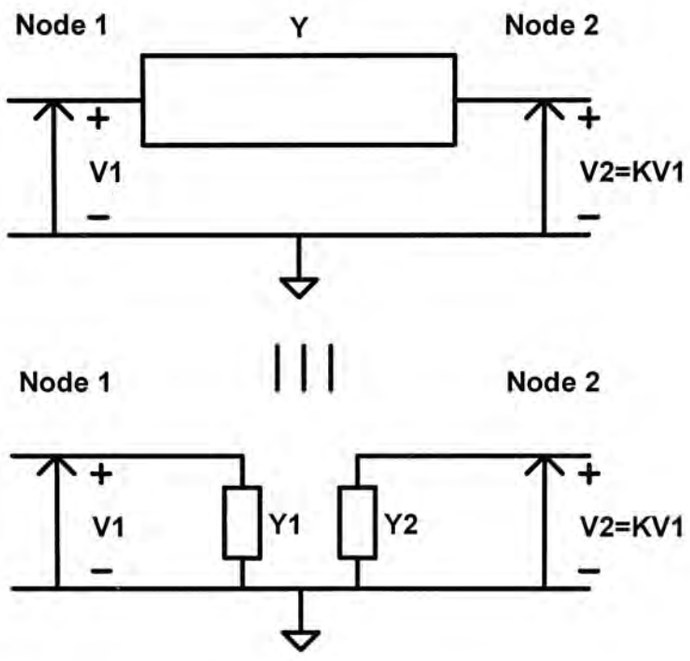


Figure 2.8: Graphical illustration of Miller's theorem

The Miller replacement illustrated in figure 2.8 is based on the assumption that it is possible, by independent means, to determine the voltage gain K from node 1 to node 2. Once the gain is known, we can compute Y1 and Y2 as follows.

$$Y_1 = (1-K)Y$$

$$Y_2 = (1-\frac{1}{K})Y$$

Consider a two-stage amplifier with a compensation capacitor connected between the two high impedance nodes as illustrated in figure 2.9.

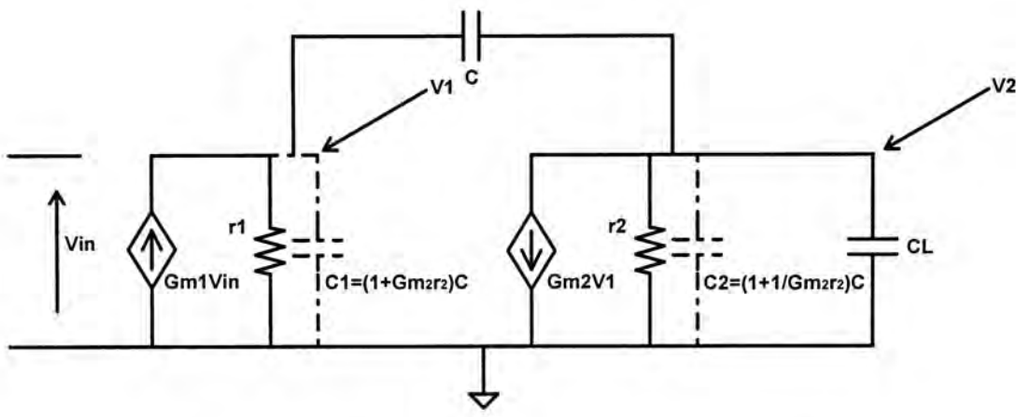


Figure 2.9: Capacitance multiplication by Miller effect

Phase inversion and amplification occurs at the second stage such that:

$$V_2 = -gm_2 r_2 V_1$$

Applying Miller's theorem, the compensation capacitor is effectively replaced by two capacitors drawn by dotted line, C1 and C2. It can be observed that capacitor C1 is equal to capacitor C multiplied by a factor of $(1+gm_2 r_2)$. This is the advantage of Miller compensation as the feedback capacitance is amplified by the Miller effect, so a very small capacitor can be used. In addition, a small capacitor can improve the bandwidth and slew rate of the compensated amplifier.

Chapter 3 CMOS Current Feedback Operational Amplifier

3.1 Introduction

The current feedback operational amplifier (CFOA), as introduced by Nelson and Evans, has been available as a commercial product for a number of years. Ideally, the bandwidth of a current feedback operational amplifier is independent of the close loop gain [1-4]. This is a major advantage over the traditional voltage feedback operational amplifier, which has a constant gain-bandwidth product.

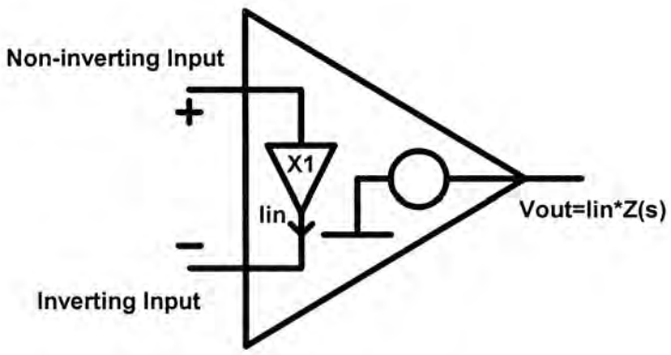


Figure 3.1: Simple current feedback operational amplifier model

The simplest model of a current feedback amplifier is shown in figure 3.1. In this model, the input of a current feedback amplifier is a voltage buffer, connected between the non-inverting and inverting inputs. The non-inverting input is connected to the buffer input and has a high input impedance. The inverting input is connected to the buffer output and has a low impedance. Current can flow in and out of the low impedance inverting input. An internal transimpedance amplifier senses the current flow and produces a voltage output proportional to the current. Current flowing out of the inverting

input produces a positive output voltage. Current flowing into the inverting input produces a negative output voltage.

A modern single stage current feedback operational amplifier is shown in the appendix. The majority of commercial current feedback operational amplifiers are a variation of this circuit. In the following section, the dynamics of current feedback operational amplifier is studied together with a suggested compensation method. The difference in dynamics between voltage feedback amplifier and the current feedback amplifier can be readily visible.

3.2 Current Feedback Operational Amplifier with Active Current Mode Compensation

Apart from the advantages mentioned in the previous section, conventional current feedback operational amplifiers usually have a single stage topology with stacked transistors. Consequently, the DC gain error is poor due to the limited transimpedance gain. Moreover, the output voltage swing is also reduced due to the series connected transistors.

According to these problems, a two-stage CFOA topology with improved open loop transimpedance gain and output voltage swing is suggested. Active current mode compensation is used to eliminate the loading effect of the internal high impedance node due to the compensation capacitor. Thus, bandwidth is preserved even in the presence of additional signal delay at the second gain stage. In addition, the small value of the compensation capacitor is also suitable for integration.

3.2.1 Circuit Description

The CFOA consists of three parts, as shown in Figure 3.2. The first part is a voltage buffer formed by differential amplifier (M1-M4) in an unity gain feedback configuration. The second part is a common gate amplifier consisting of transistors M6-M8, where M6 is the driver, and M7 and M8 are the active loads. The active loads are responsible for the generation of voltage swing from the feedback current. The third part is a common source amplifier consisting of transistor M9 and current source Ib4, and provides additional transimpedance gain. The common source output stage also provides a 180-degree phase shift, so that a negative feedback system is formed through the resistor feedback network of R1 and R2. Moreover, this output stage can improve the output voltage swing. The aspect ratio of the transistors and the biasing voltages are summarized in the table 3-1 and 3-2 respectively.

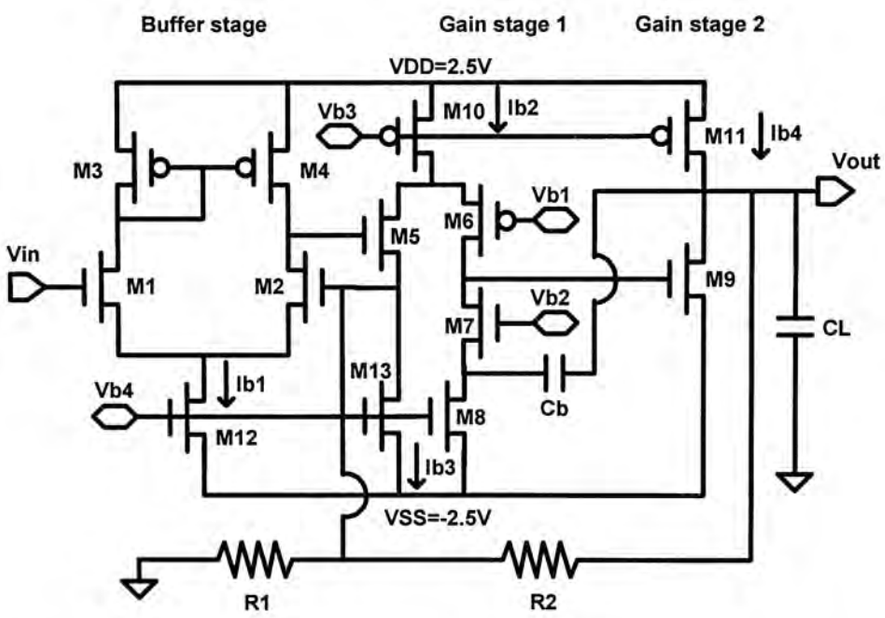


Figure 3.2: Schematic of the suggested current feedback operational amplifier

Transistors	W/L
M1, M2	16u/0.6u
M3, M4	32u/0.6u
M5	10u/0.6u
M6	30u/1u
M7	320u/1u
M8	90u/1u
M9	320u/1u
M10	160u/0.6u
M11	640u/1u
M12	32u/0.6u
M13	10u/0.6u

Table 3-1: Aspect ratio of the transistors in the current feedback operational amplifier

Biasing Points	DC Voltage (V)
Vb1	1
Vb2	-1
Vb3	1.5
Vb4	-1.5
Power Supply	±2.5

Table 3-2: Biasing voltages of the current feedback operational amplifier

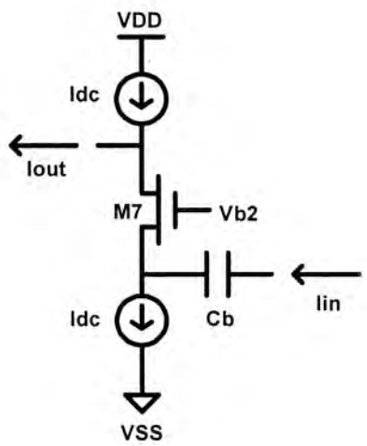


Figure 3.3: Current feedback buffer circuit formed by the transimpedance stage

The CFOA is actively compensated without adding a single extra component to the basic amplifier topology. It is not difficult to recognize that there is a current buffer embedded in the amplifier, as shown in Figure 3.3.

The relatively low impedance input and high impedance output of the current buffer are located at the source and the drain of transistor M7. The drain node of transistor M7 is designed to be of high impedance for high transimpedance gain, any increase of capacitance at this node will introduce a significant phase shift in the forward signal path. With the help of the current buffer, the drain node of transistor M7 is isolated from the compensation capacitance and the large loading capacitance at the output node. Consequently, bandwidth can be persevered even though a two gain stages topology is employed. Thus, transistors M6-M8 not only form the common gate stage, they also constitute the feedback circuitry for the active compensation.

3.2.2 Small Signal analysis

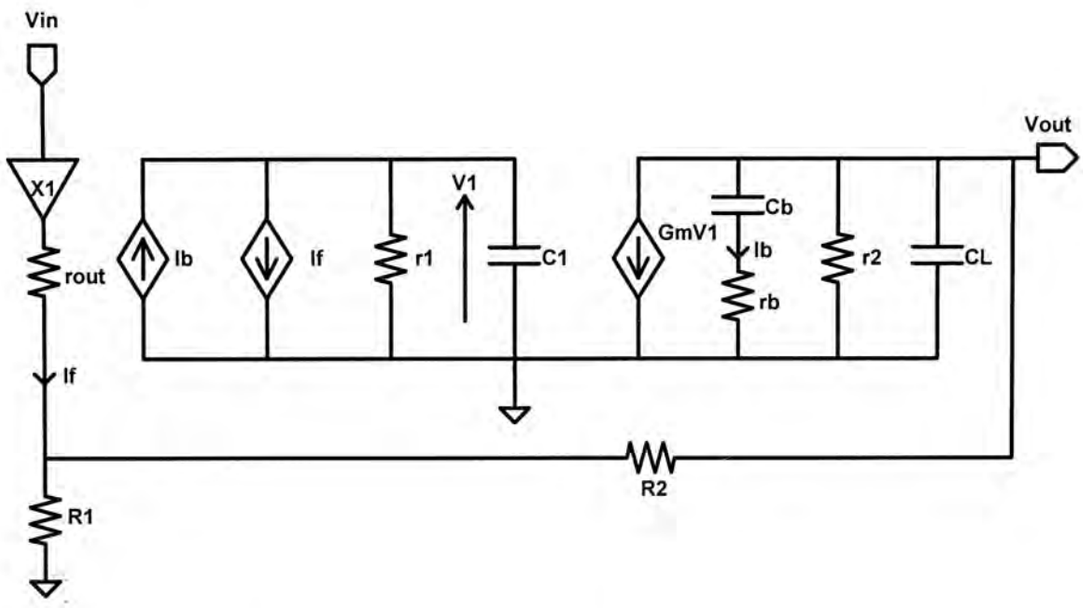


Figure 3.4: Small signal model of the current feedback operational amplifier

The small signal model of the CFOA is shown in Figure 3.4. The input of the current buffer is modeled by a finite input resistance rb. A current controlled current source Ib models the current output of the feedback circuitry. With this model, the transfer function of this circuit is approximately given by equation (3.1). The detailed derivation steps are summarized in the appendix B.

$$\frac{V_{OUT}}{V_{IN}} \approx \frac{1}{G_m R_1 r_1} \frac{(R_1 + G_m R_1 r_1 + G_m R_2 r_1 + sR_1 r_1 C_1)(1 + sr_b C_b)}{(1 + sR_2 C_b)\left[\frac{r_b C_1 C_L}{G_m} s^2 + (\frac{C_1}{G_m} + \frac{C_1 C_L}{G_m C_b})s + 1\right]} \quad (3.1)$$

The above expression is derived under the assumptions of rout ≈ 0, CL > C1 and Cb, and r1 > r2, R1 and R2. Similar to conventional CFOA, the bandwidth or dominant pole is given by a RC time constant and does not depend on the closed loop gain:

$$\frac{1}{R_2 C_b} \quad (3.2)$$

From equation (3.1), two high frequency poles can be observed. To have real poles, the following condition must be satisfied.

$$r_b \leq \frac{C_1 C_L}{4 G_m C_b^{\,2}} \quad (3.3)$$

The locations of the second pole and the third pole are obtained by solving the quadratic dominator of equation (3.1). Their locations are respectively given by:

$$\omega_{p2} \approx \frac{2 G_m C_b}{C_1 C_L} \quad (3.4)$$

$$\omega_{p3} \approx \frac{1}{2 r_b C_b} \quad (3.5)$$

As the bandwidth of CFOA is independent of the close loop gain, so the unity-gain frequency is directly proportional to the closed loop gain:

$$\omega_u = \frac{G}{R_2 C_b} \quad (3.6)$$

Where G is the closed loop gain of the amplifier

To ensure closed loop stability, the non-dominant pole must be equal or greater than the unity gain frequency:

$$\frac{2 G_m C_b}{C_1 C_L} \geq \omega_u \quad (3.7)$$

Combining equation (3.7) with equation (3.6) and this implies:

$$G \leq \frac{2 G_m R_2 C_b^{\,2}}{C_1 C_L} \quad (3.8)$$

The phase margin is given by [5]:

$$PM = \tan^{-1}\frac{\omega_{p2}}{\omega_u} \quad (3.9)$$

This gives:

$$PM \approx \tan^{-1}\frac{2G_m R_2 C_b^{\,2}}{GC_1 C_L} \quad (3.10)$$

Equation (3.10) has demonstrated the significance of this work. It shows that the phase margin is inversely proportional to the close loop gain and the size of the loading capacitor. This observation is not difficult to understand. Moreover, the phase margin is directly proportional to R_2 and the square of the compensation capacitor C_b. Although increasing the value of R_2 can benefit the phase margin, it leads to bandwidth reduction as given by equation (3.2). The tangent of phase margin has a square dependence on the compensation capacitor and it indicates that a smaller capacitor is sufficient for a given phase margin. With this small compensation capacitor, the bandwidth can be preserved and chip area can be saved.

3.2.3 Simulation Results

A Current Feedback operational amplifier test chip was designed with a 0.6-micron triple metals CMOS technology. All the simulation results listed below are obtained from post-layout simulation. Figure 3.5 illustrates the frequency response of the CFOA in non-inverting amplifier configurations. R_2 and C_b are respectively given by 50kΩ and 1.6pF.

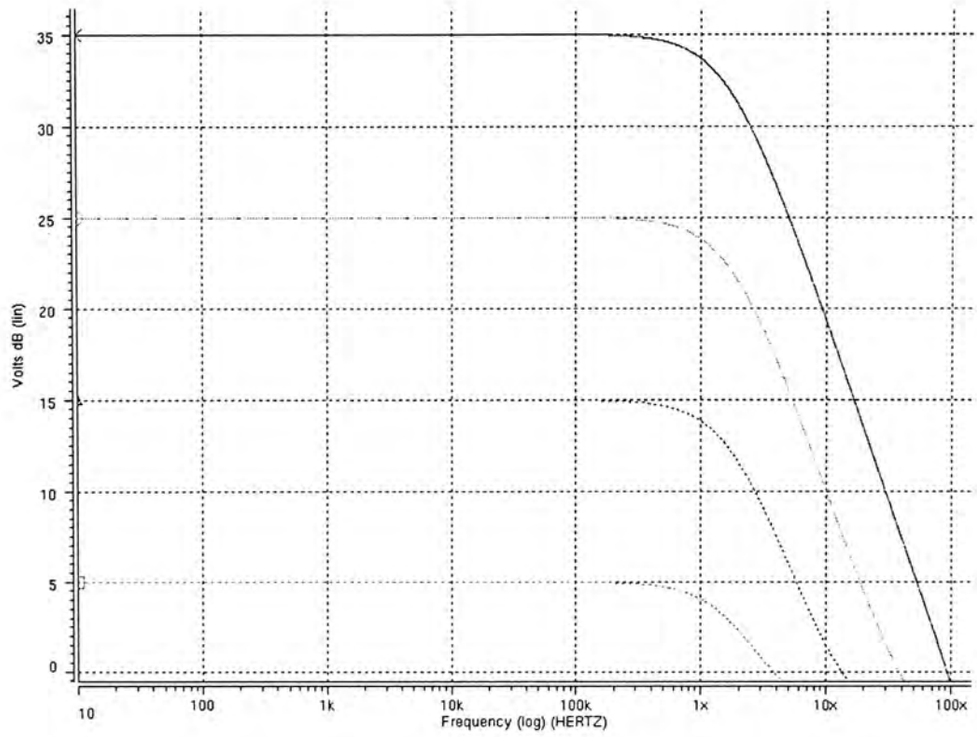


Figure 3.5: Frequency response of the CFOA with different closed loop gain configurations

Table 3-3 shows a numerical summary of the 3-dB bandwidth, unity gain frequency, and phase margin as a function of the closed loop gain. The calculated closed loop 3-dB bandwidth is approximately equal to 1/R2Cb, which predicts a value of 1.99MHz for R2 equals to 50kΩ and Cb equals to 1.6pF. This is very close to the simulated close loop gain, which is between 5dB to 35dB.

Closed Loop Gain (non-inverting)	3dB Bandwidth (MHz)	Unity Gain Frequency (MHz)	Phase Margin (Degree)
5dB	2.18	3.79	153.1
15dB	1.79	13.3	147.6
25dB	1.77	38.4	115.6
35dB	1.63	92.5	59.0

Table 3-3: Numerical summary of the frequency response in non-inverting amplifier configuration with R2=50kOhm

Table 3-4 also shows the bandwidth as a function of the closed loop gain. However, this time the value of R2 is changed to 10kΩ, and the 3dB bandwidth is predicted to be near 9.95MHz.

Closed Loop Gain (non-inverting)	3dB Bandwidth (MHz)	Unity Gain Frequency (MHz)	Phase Margin (Degree)
10dB	10.0	38.4	120
20dB	8.90	91.6	63.0

Table 3-4: Numerical summary of the frequency response in non-inverting amplifier configuration with R2=10kOhm

The step response is shown in Figure 3.6, and the transient simulation of the amplifier with a 20dB gain at 1MHz is shown in Figure 3.7. A brief performance summary is provided in Table 3-5.

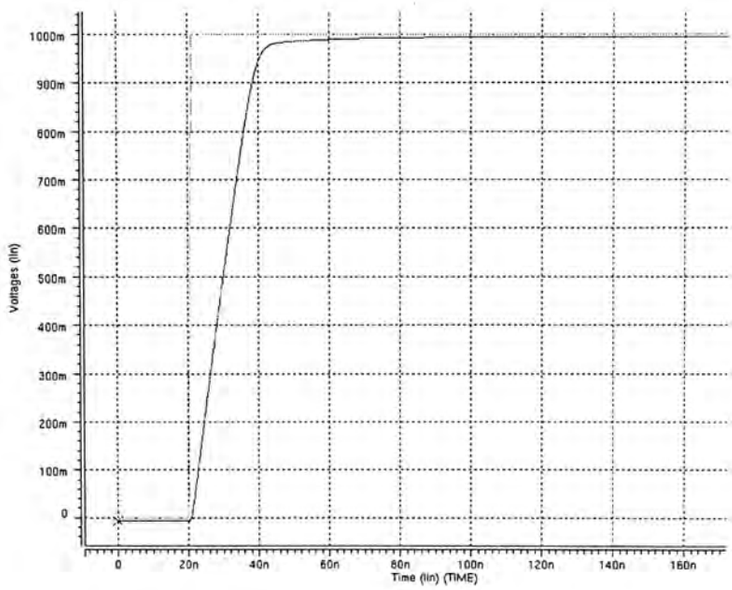


Figure 3.6: Transient response to 1V input step size

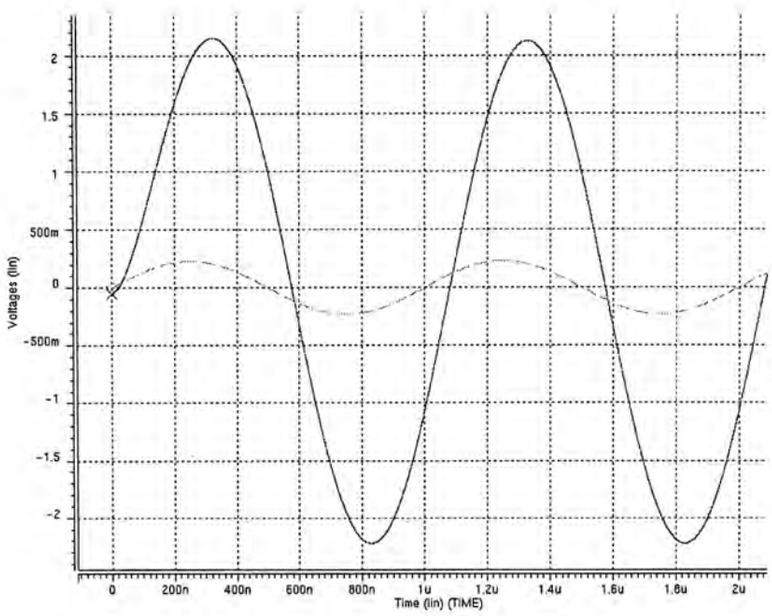


Figure 3.7: Transient response with 20dB of voltage gain

Power Supply (V)	± 2.5
Input Biasing Current (uA)	0.2964
Input Resistance of Inverting Input (Ω)	97.7
Slew Rate + (V/μs) Gain = +1	54.79
Slew Rate - (V/μs) Gain = +1	44.94
Open Loop Transimpedance Gain (dBΩ)	148

Table 3-5: Performance summary

Chapter 4 Reversed Nested Miller Compensation

4.1 Introduction

With the decrease in supply voltage of VLSI system, single stage cascode architecture is no longer suitable for operational amplifier design, due to the limitation of supply voltage. In addition, short-channel sub-micron CMOS transistor has very poor output impedance that will degrade the gain of the amplifier [16]. Thus, multistage topology with cascaded wideband gain stages will become the main architecture in future operational amplifier designs.

However, multistage amplifier designs suffer bandwidth reduction and close-loop stability problems due to their multiple-pole nature. In this work, one of the compensation techniques for stabilizing multistage amplifiers is studied and it is called reversed nested Miller compensation [8]. A block diagram of a three-stage amplifier using reversed nested Miller compensation is shown in figure 4.1.

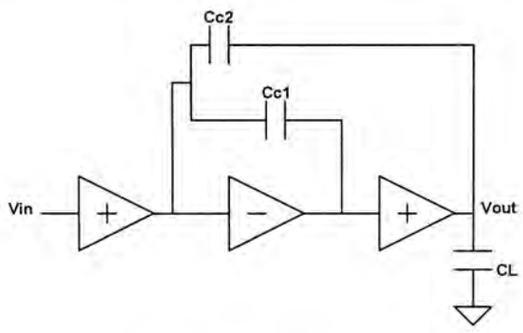


Figure 4.1: Block diagram of a three stages amplifier using reversed nested Miller compensation

The circuit in figure 4.1 contains two Miller capacitors, Cc_1 and Cc_2. The feedback loop of Cc_2 encloses the loop of Cc_1. Because of this topology with local feedback loops at several levels, the structure is labeled as nested Miller compensation.

4.2 Frequency Response

The detailed zero and pole positioning of reversed nested Miller compensation is analyzed through the small signal model shown in figure 4.2.

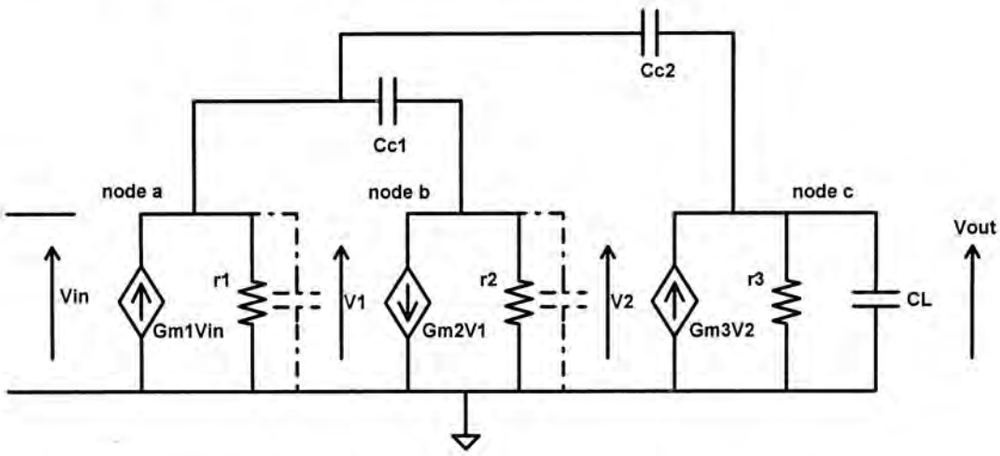


Figure 4.2: simplified small signal model of amplifier using reversed nested Miller compensation

In the small signal model shown in figure 4.2, parameters Gm_i and r_i are the i-th stage transconductance and output impedance, respectively. Capacitor C_L is the loading capacitor, which is a lumped model originated from the parasitic capacitances of bonding pad, packaging, printed circuit board and measuring instrument. The capacitors drawn by dotted line represent the equivalent capacitances at the output of each stage, which will be neglected due to their relatively low values when comparing with the feedback capacitors [13]. Under these assumptions, the transfer function of the circuit in figure 4.2 is obtained by solving for $\frac{Vout}{Vin}$. The detailed derivations are shown in appendix C.

$$A_{RNMC}(s) \approx \frac{A_{DC}\left(1-\left(\frac{Cc_1}{g_{m2}}+\frac{Cc_2}{g_{m2}g_{m3}r_2}\right)s-\frac{Cc_1Cc_2}{g_{m2}g_{m3}}s^2\right)}{\left(Cc_2gm_2gm_3r_1r_2r_3s+1\right)\left(\frac{Cc_1C_L}{gm_2gm_3}s^2+\left(\frac{Cc_1(Cc_2+C_L)}{Cc_2gm_3}-\frac{Cc_1}{gm_2}\right)s+1\right)} \quad (4.1)$$

where $A_{DC}=-gm_1gm_2gm_3r_1r_2r_3$

Equation (4.1) can also be written in the form as shown in equation (4.2). The reason of writing equation (4.1) in the following format will be explain in section 4.3.

$$A_{RNMC}(s) \approx \frac{-\left(1-\left(\frac{Cc_1}{g_{m2}}+\frac{Cc_2}{g_{m2}g_{m3}r_2}\right)s-\frac{Cc_1Cc_2}{g_{m2}g_{m3}}s^2\right)}{\frac{Cc_2}{gm_1}s\left(\frac{Cc_1C_L}{gm_2gm_3}s^2+\left(\frac{Cc_1(Cc_2+C_L)}{Cc_2gm_3}-\frac{Cc_1}{gm_2}\right)s+1\right)} \quad (4.2)$$

4.2.1 Gain-bandwidth product

The transfer function shown in (4.1), the location of the dominant pole and the DC gain are given by $\frac{-1}{Cc_2gm_2gm_3r_1r_2r_3}$ and $-gm_1gm_2gm_3r_1r_2r_3$ respectively. As the gain-bandwidth product is equal to the DC gain multiplied by the frequency of the dominant pole [15]. Thus, the expression for the gain-bandwidth product is given by:

$$\omega_{GBW} = \frac{DC\ Gain}{Frequency\ of\ the\ do\min ant\ pole} = \frac{-(-gm_1gm_2gm_3r_1r_2r_3)}{Cc_2gm_2gm_3r_1r_2r_3}$$

$$\omega_{GBW} = \frac{gm_1}{Cc_2} \quad (4.3)$$

From equation (4.3), the gain bandwidth product is determined by the transconductance of the first stage and the outermost capacitive feedback path Cc_2. This property is the same as the two-stage amplifier compensated by Miller compensation [15].

4.2.2 Right half complex plane zero

In addition to the dominant pole, the transfer function in (4.1) also shows that the amplifier have two other zeros located at higher frequencies. As the coefficients of the s and s^2 terms in the numerator are both negative, a right half complex plane (RHP) zero is created that is located at a lower frequency than the other left half complex plane

(LHP) zero [8]. Thus, RHP zero has dominant effect to the frequency response of the amplifier.

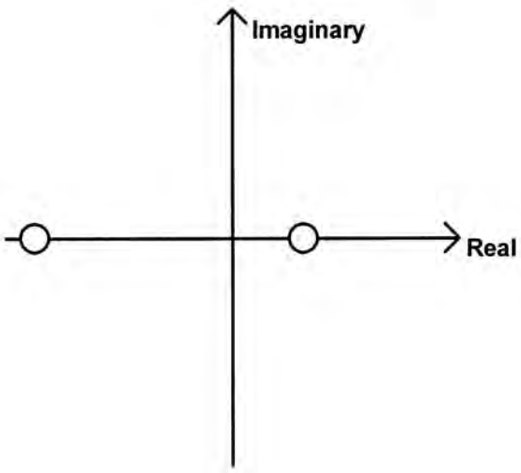


Figure 4.3: Relative positions of zeros in reversed nested Miller compensation

Solving the roots of the numerator in equation (4.1), we have the locations of the two zeros:

$$\omega_{RHPZ} = \frac{gm_3}{2Cc_2}\left(-1+\sqrt{1+4\frac{Cc_2}{Cc_1}\frac{gm_2}{gm_3}}\right) \quad (4.4)$$

$$\omega_{LHPZ} = \frac{gm_3}{2Cc_2}\left(-1-\sqrt{1+4\frac{Cc_2}{Cc_1}\frac{gm_2}{gm_3}}\right) \quad (4.5)$$

At this moment, the contribution from the LHP zero is ignored because it is located at a relatively high frequency when comparing with the RHP zero. The transfer function is assumed to consist of a dominant pole, a RHP zero and two non-dominant poles ω_{P1} and ω_{P2}. Under this assumption, the phase margin of the amplifier is given by the following expression:

$$PM = 90^o - \tan^{-1}\frac{\omega_{GBW}}{\omega_{RHP}} + \tan^{-1}\frac{\omega_{GBW}}{\omega_{P1}} + \tan^{-1}\frac{\omega_{GBW}}{\omega_{P2}} \quad (4.6)$$

Obviously, the RHP zero has negative contribution to the phase margin by referring to equation (4.6).

By increasing the output stage transconductance gm_3 , the RHP zero can effectively be shifted to a higher frequency as indicated by equation (4.4). Its negative contribution to the open loop transfer function can then be neglected. However, there will be a corresponding increase in DC power consumption and thus, this method cannot be generally accepted.

Another way of removing the RHP zero is to use a smaller value of Cc_2 . However, the non-dominant poles will be allocated on the RHP and exponential terms with positive power will be created in the amplifier's impulse response if Cc_2 is too small [11]. Thus, the RHP zero decreases the phase margin or stability and represents an optimization problem in amplifiers compensated by reversed nested Miller compensation.

4.2.3 The Pair of Complex Conjugate Poles

Second Order System formed by the Non-dominant Poles

Apart from the RHP zero, there are also two non-dominant poles in the transfer function shown in equation (4.1).

In linear-time invariant system, the principle of superposition can be applied [17]. The third-order transfer function of the amplifier in equation (4.1) can be considered as the sum of a first-order system and a second-order system. Since the first and second order transfer functions have been studied extensively in both time and frequency domain, their properties can be applied directly to the analysis of the amplifier.

The transfer function of the amplifier is considered as in the figure 4.4. The input signal convolves with the two systems and their corresponding outputs sum up at the

output node. By using this model, the two high frequency poles in the lower signal path can be considered as a separated system.

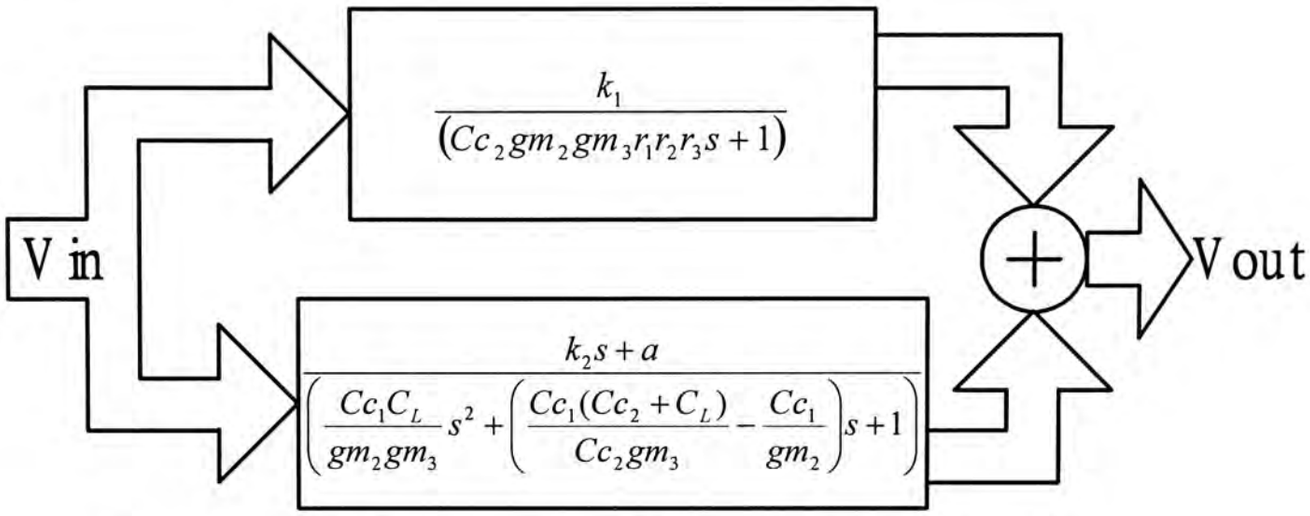


Figure 4.4: A first order system and a second order system build up the amplifier

Nature of the Non-dominant Poles

In this section, we start to consider the two high frequency poles as a separated system. This is a pair of complex conjugate poles with symmetrical locations about the real axis in the complex plane [8][10][11][12][13]. We will study the properties of these two poles and their contribution to the amplifier's frequency response and transient response.

Condition to avoid Positive Exponential Term

First of all, the coefficient of the s term in the quadratic equation containing the complex conjugate poles must be larger than 0, because this condition will allocate the two poles to the left half complex plane. Thus, the time domain impulse response of the amplifier can free from the exponential term with positive power.

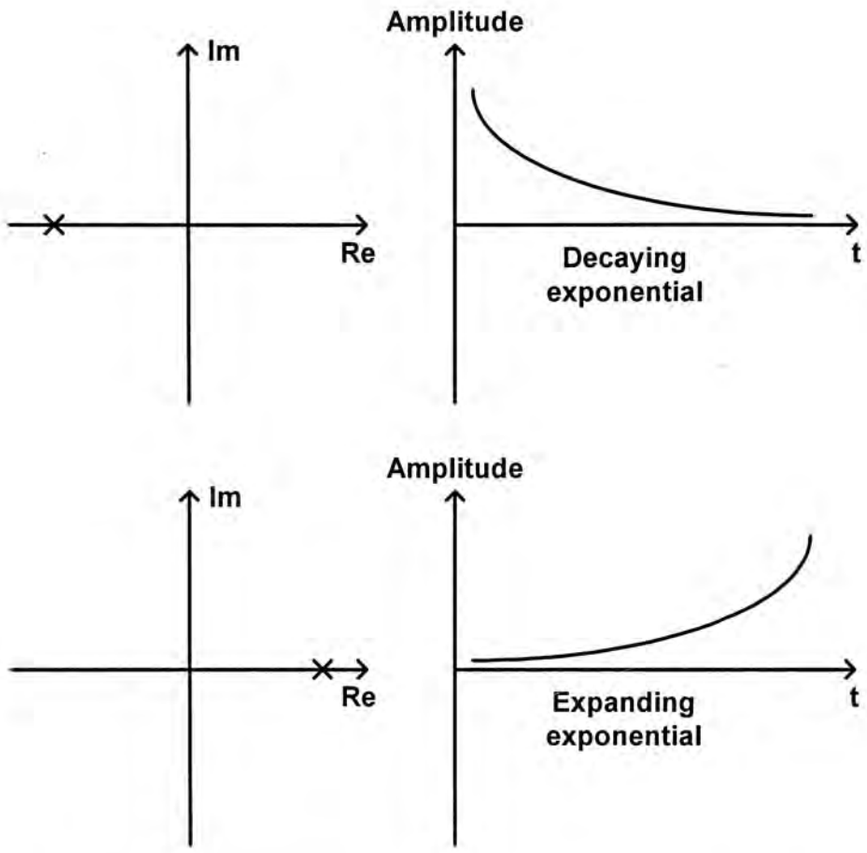


Figure 4.5: The difference between LHP pole and RHP pole in time domain impulse response

The stated condition implies,

$$Cc_2 > \frac{\frac{gm_2}{gm_3} C_L}{1 - \frac{gm_2}{gm_3}} \quad (4.7)$$

When comparing equation (4.7) with (4.4), we know that the RHP zero can be allocated to higher frequency by scaling down the feedback capacitor Cc_2. However, this scaling is limited by the condition stated in equation (4.7). This is because the complex conjugate poles will be allocated to the RHP if the value of Cc_2 is scaled down too much. Thus, the present of RHP zero and complex conjugate poles has made the reversed nested Miller compensation to be a difficult optimization problem.

Phase Margin of the Amplifier

The real part of these complex conjugate poles is given by:

$$\omega_{CP\_REAL} = \frac{-b}{2a} = \frac{gm_3 - \dfrac{gm_2(Cc_2 + C_L)}{Cc_2}}{2C_L}$$

Under the effect of RHP zero and a pair of complex conjugate poles, the phase margin of the amplifier is given by:

$$PM = 90^o - \tan^{-1}\frac{\omega_{GBW}}{\omega_{RHP}} + 2\tan^{-1}\frac{\omega_{GBW}}{\omega_{CP\_REAL}}$$

$$PM = 90^o - \tan^{-1}\frac{\omega_{GBW}}{\omega_{RHP}} + 2\tan^{-1}\frac{2gm_1C_L}{(gm_3 - gm_2)Cc_2 - gm_2C_L} \quad (4.7)$$

Transient Response

In time domain analysis, the second order system containing complex conjugate poles is usually termed as underdamped system with standard transfer function in the form shown in equation (4.8). The function is characterized by two time domain physical constants called underdamped natural frequency ω_n and the damping ratio ζ [18].

$$G(s) = \frac{\omega_n^{\,2}}{s^2 + 2\zeta\omega_n s + \omega_n^{\,2}} \quad (4.8)$$

The relationship between the two time domain physical constants and the locations of the complex poles in the complex plane is shown in figure 4.6.

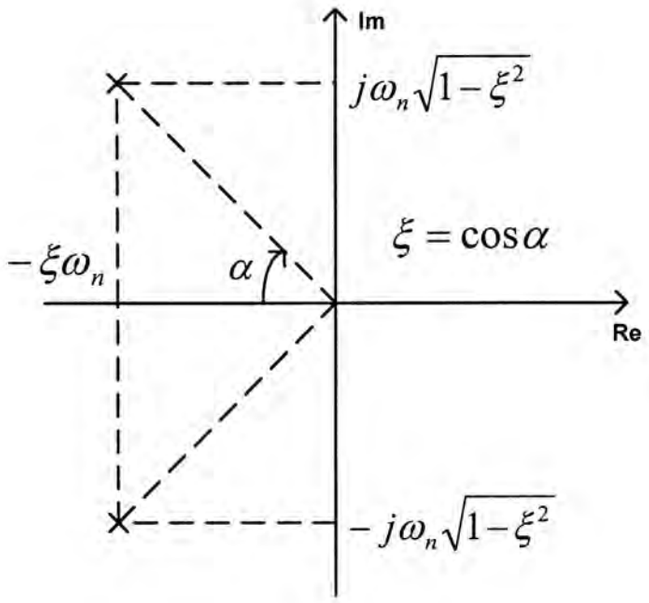


Figure 4.6: Relationship between the locations of the complex poles and the two physical constants

By taking inverse Laplace transform to $G(s)$, the unit-impulse response of equation (4.8) is given by,

$$g(t) = \frac{\omega_n}{\sqrt{1-\xi^2}} e^{-\xi\omega_n t} \sin\sqrt{1-\xi^2}\,\omega_n t \quad (4.9)$$

From equation (4.9), it can be observed that the unit-impulse response of the complex poles in reversed nested Miller compensation consists of underdamped sinusoidal with an exponential decay factor equal to $e^{-\xi\omega_n}$. By comparing coefficients, the underdamped natural frequency ω_n and the damping ratio ζ for the reversed nested Miller compensation are respectively given by:

$$\omega_n = \sqrt{\frac{gm_2 gm_3}{Cc_1 C_L}} \quad (4.10)$$

$$\zeta = \frac{1}{2}\sqrt{\frac{Cc_1 gm_2 gm_3}{C_L}}\left(\frac{Cc_2 + C_L}{Cc_2 gm_3} - \frac{1}{gm_2}\right) \quad (4.11)$$

4.3 Components Sizing

In this section, the components sizing for reversed nested Miller compensation is introduced. To begin, assuming that the effect of the zeros is negligible and considering that the poles of the amplifier in unity-feedback configuration have third-order Butterworth frequency response [8] [10] [11], the transfer function in unity-gain feedback $H(s)$ with cut-off frequency ω_o is given by:

$$H(s) = \frac{A_{RNMC}(s)}{1 + A_{RNMC}(s)}$$

$$H(s) = \frac{1}{1 + s(\frac{2}{\omega_o}) + s^2(\frac{2}{\omega_o^2}) + s^3(\frac{1}{\omega_o^3})} \quad (4.12)$$

unity feedback configuration with Butterworth response

To obtain (4.12), the open loop transfer function of the amplifier should be in the following format:

$$A_{RNMC}(s) = \frac{1}{s\frac{2}{\omega_o}\left[1 + s(\frac{1}{\omega_o}) + s^2(\frac{1}{2\omega_o^2})\right]} \quad (4.13)$$

By using this model, three equations are obtained by comparing the coefficients in the dominator of equation (4.2) with those of equation (4.13).

$$\frac{2}{\omega_o} = \frac{Cc_2}{gm_1}$$

$$\frac{1}{\omega_o} = \frac{Cc_1(Cc_2 + C_L)}{gm_3 Cc_2} - \frac{Cc_1}{gm_2}$$

$$\frac{1}{2\omega_o^2} = \frac{Cc_1 C_L}{gm_2 gm_3}$$

By solving the above equations, the dimensions of the two compensation capacitors are respectively given by:

$$Cc_2 = \frac{(4gm_1 + gm_2)C_L}{gm_3 - gm_2} \approx \frac{4gm_1 C_L}{gm_3} \quad (4.14)$$

$$Cc_1 = \frac{2gm_2 gm_3 (gm_1 - \frac{gm_2}{4})^2}{gm_1^{\,2}(gm_3 - gm_2)^2} C_L \approx \frac{2gm_2}{gm_3} C_L \quad (4.15)$$

It can be observed that the two compensation capacitors are directly proportional to the loading capacitor and inversely proportional to the transconductance of the output stage.

4.4 Circuit Simulation

In order to verify the design equations, a three-stage operational amplifier is designed using reversed nested Miller compensation. The target gain-bandwidth product is set to about 10MHz. For worst-case estimation, the loading capacitor is selected to be 15pF for the representation of loading from bonding pad (1pF) and measuring instruments (9pF). Moreover, the phase margin of the operational amplifier is set to about 60^o, which is an industrial standard for general-purpose operational amplifier [13].

The operational amplifier is constructed with a differential amplifier and a common source amplifier as the first and second stage respectively. A diode loaded common source amplifier is cascaded with another common source amplifier to form the output stage as shown in figure 4.7.

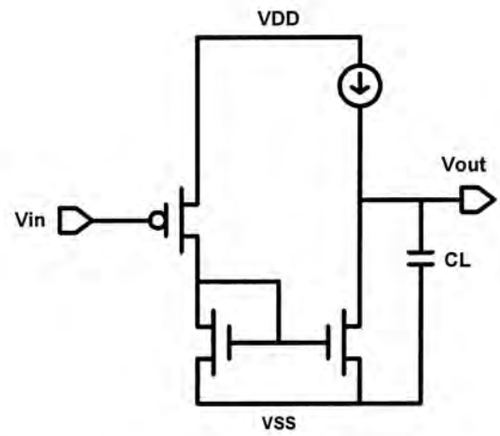


Figure 4.7: The non-inverting output stage

Although the non-inverting stage contains two gain nodes, the pole associated with the diode loaded common source amplifier is located at a relatively high frequency. Thus, the output stage can still be approximated as a first order system. The completed schematic of the three-stage operational amplifier is shown in figure 4.8 and the aspect ratio of the transistors is summarized in the table 4-1.

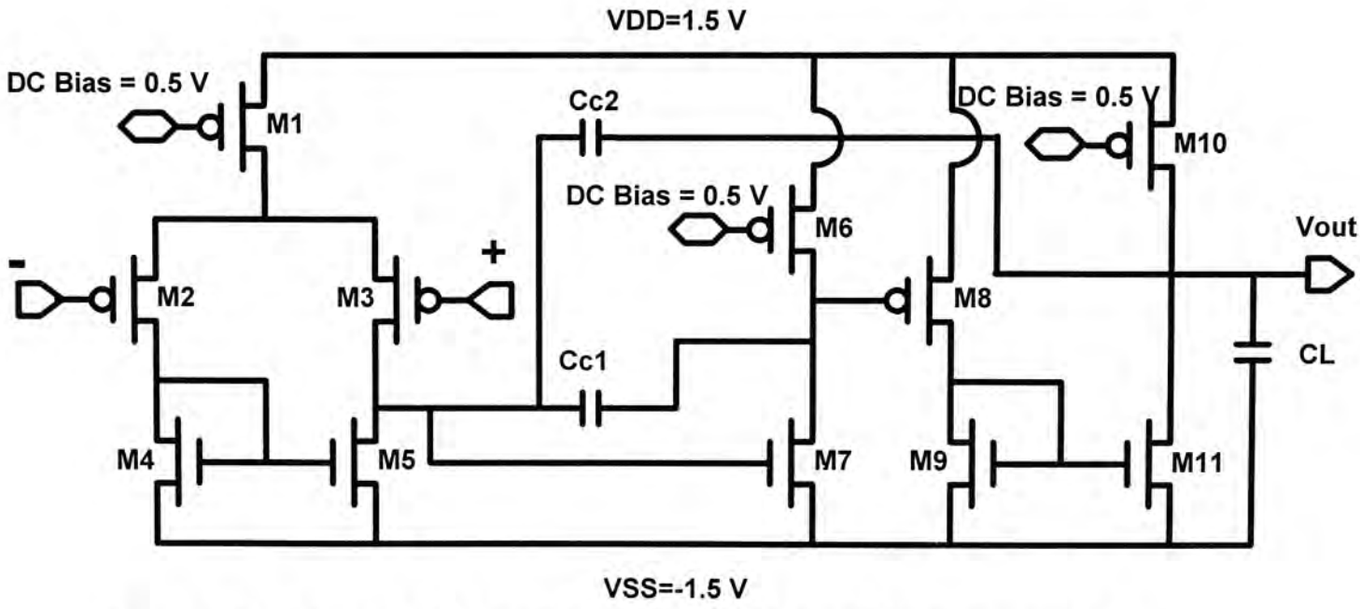


Figure 4.8: The schematic of the amplifier using reversed nested Miller compensation

Partitions of the amplifier	Transistors	W/L
First gain stage (differential amplifier)	M1	460u/1u
	M2, M3	27.6u/1u
	M4, M5	50u/1u
Second gain stage	M6	320u/1u
	M7	56u/1u
Third gain stage	M8	30u/1u
	M9	12u/1u
	M10	320u/1u
	M11	56u/1u

Table 4-1: Aspect ratio of the transistors in the three-stage amplifier

This operational amplifier is designed with AMS 0.6um CMOS technology and simulated by Hspice. The simulation results are shown in the following diagrams.

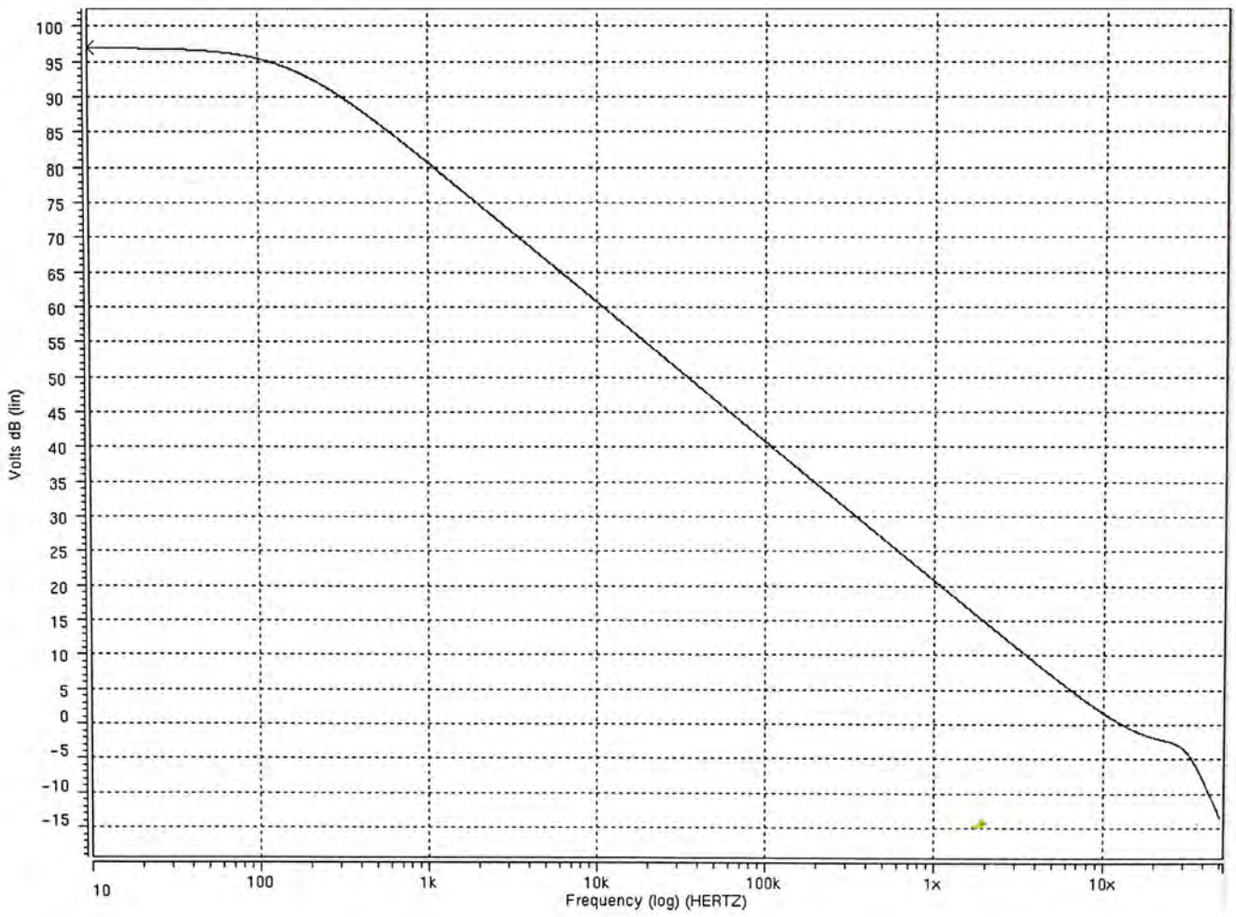


Figure 4.9: Stimulated gain response of three-stage operational amplifier compensated by reversed nested Miller compensation

Figure 4.10 is a close-up of the frequency response near the gain-bandwidth product. It can be seen that the RHP zero is located at a lower frequency than the two complex conjugate poles. Moreover, all of them are within one decade above the gain-bandwidth product and they are responsible for the rapid phase shift beyond the gain bandwidth product.

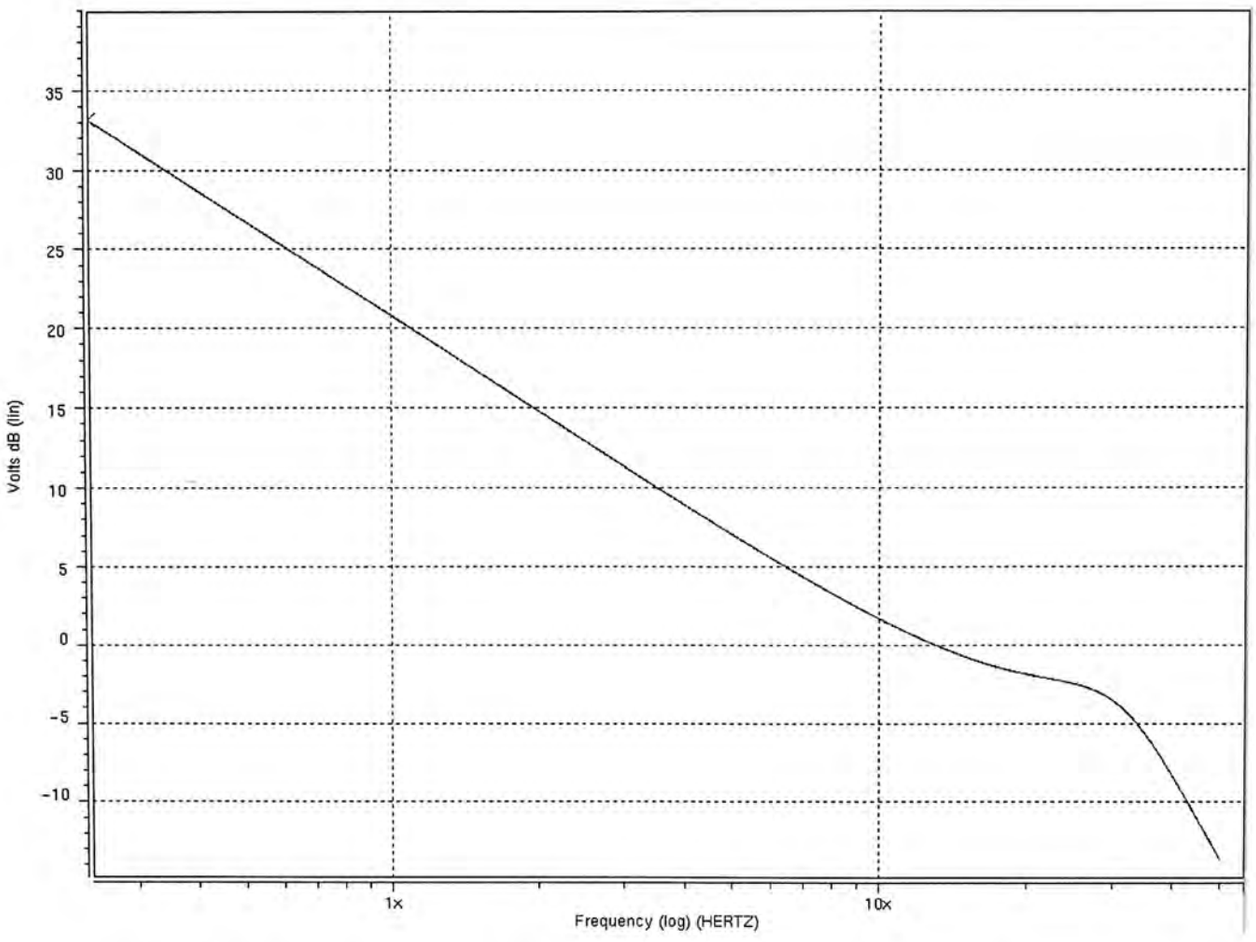


Figure 4.10: Close-up image showing the positions of the complex conjugate poles and the RHP zero

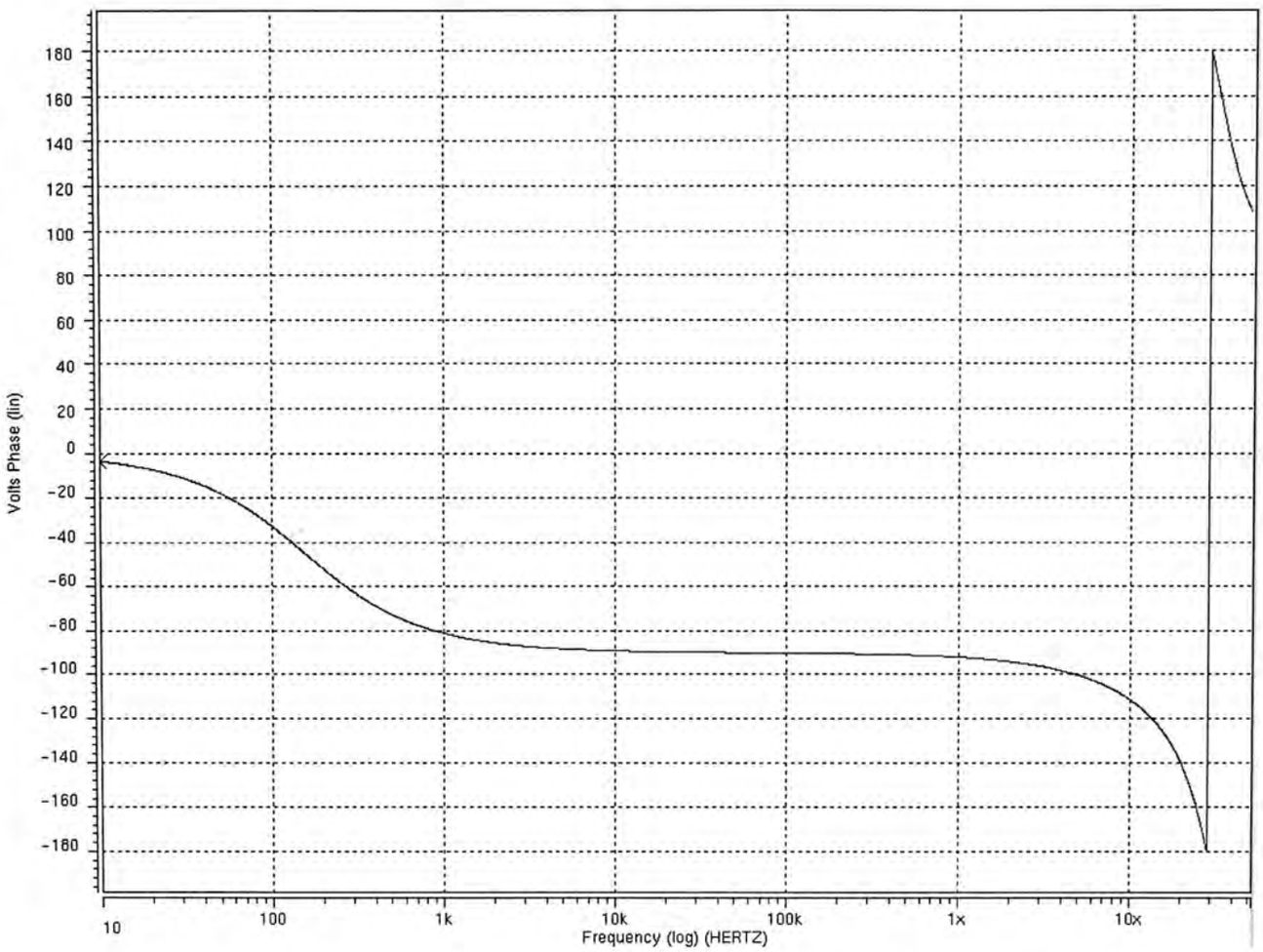


Figure 4.11: Stimulated phase response of the three-stage operational amplifier

Figure 4.12 illustrates the step response of the operational amplifier in unity gain configuration. The complex conjugate poles are responsible for the underdamped sinusoidal and hence the slow settling component in the transient response. The long settling time will limit the operational amplifier to be used in discrete time application such as D/A [6]. Finally, the performance summary of the operational amplifier is shown in table 4-2.

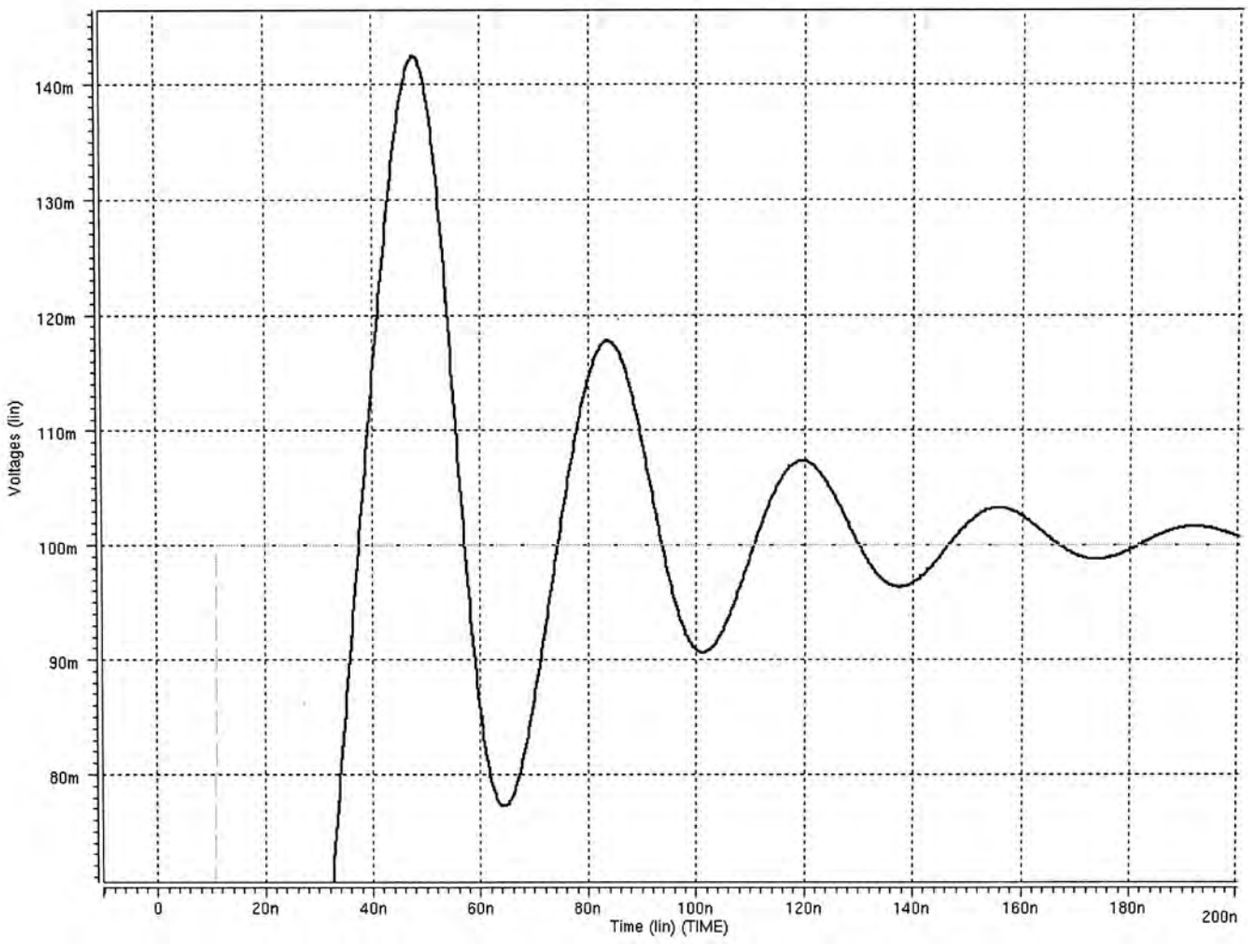


Figure 4.12: Step response of the amplifier using reversed nested Miller compensation

	Reversed Nested Miller Compensation (Schematic simulation results)
Loading Capacitance (pF)	15
DC gain (dB)	96.9
Gain-bandwidth product (MHz)	10.97
Phase Margin (degrees)	61.2
Settling time (Within 1% of input step size in unity gain configuration) (ns)	194.9
+ Slew rate (Gain=1) (V/μs)	5.68
- Slew rate (Gain=1) (V/μs)	10.16
Cc_2 (pF)	5.8
Cc_1 (fF)	1300
DC Power Consumption (mW)	1.46
Supply Voltage (V)	±1.5

Table 4-2: Performance summary of the three-stage operational amplifier compensated by reversed nested Miller compensation

Chapter 5 Enhancement Technique for Reversed Nested Miller Compensation

5.1 Introduction

We have presented an introduction of reversed nested Miller compensation along with the RHP zero and complex conjugate poles characteristics. In this section, a circuit technique is proposed to modify the properties of these zero and complex conjugate poles in order to enhance the performance of reversed nested Miller compensation.

Firstly, the presentation will start with the idea behind the technique. Secondly, small signal analysis and circuit simulation will be used to verify the improvement in performance. Finally, the experimental results for this circuit technique will be presented in chapter 7.

5.2 Working principle of the proposed circuit

Miller theorem is the foundation of reversed nested Miller compensation [8]. The capacitive feedback loops stabilize the amplifier by introducing negative feedback. However, the capacitive feedback paths represent a form of internal loading inside the amplifier. The feed forward effect from these compensation capacitors creates a RHP zero, because the feed forward current in these capacitors is out of phase with the current flowing into the loading capacitor [12] [13] [14]. Moreover, the loading capacitor has low impedance for frequency beyond the gain-bandwidth product of the amplifier. With the present of the compensation capacitors, the output impedances of the first and second

stages are pulled down to that of loading capacitor. Hence the gain and phase margin of the amplifier drop rapidly beyond the gain-bandwidth product.

5.2.1 The introduction of a nulling resistor

From the previous analysis of reversed nested Miller compensation, we have already known that the output impedance of the first stage chiefly determines the gain-bandwidth product of the amplifier ($\omega_{GBW} = \frac{gm_1}{Cc_2}$) . Thus, modification of output impedance level at the first stage is the starting direction for the proposed technique.

According to these observations, a nulling resistor is introduced at the output node of the capacitive feedback paths. The nulling resistor has the function of blocking the feed forward paths. Thus, it can prevent the output impedance of the first stage from being pulled down at high frequency.

5.2.2 The introduction of a voltage buffer

The transfer function for the complex conjugate poles in reversed nested Miller compensation is recalled here:

$$C(s) = \frac{1}{\left(\frac{Cc_1 C_L}{gm_2 gm_3} s^2 + \left(\frac{Cc_1(Cc_2 + C_L)}{Cc_2 gm_3} - \frac{Cc_1}{gm_2}\right)s + 1\right)} \quad (5.1)$$

In considering a polynomial, we know that the coefficient of the highest order term has the strongest effect on the roots. By taking the above quadratic equation as an example, the real part of complex conjugate poles will be allocated to higher frequency if the second order term in the dominator can be diminished.

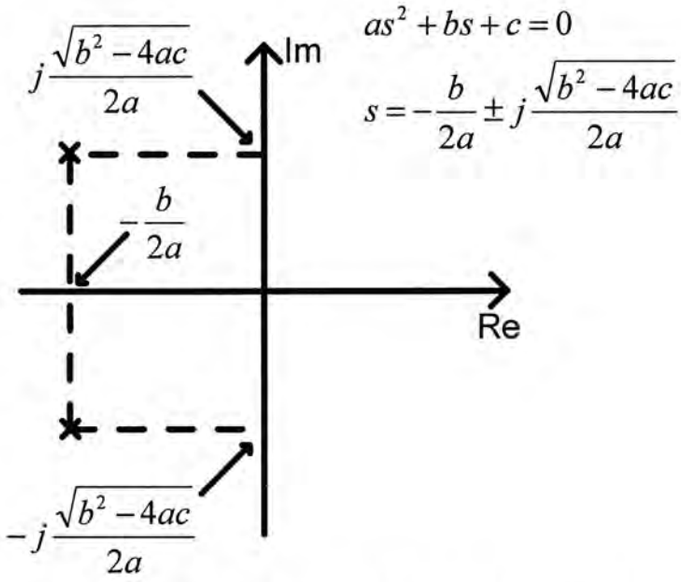


Figure 5.1: The complex conjugate poles can be allocated to higher frequency by diminishing the second order term a

In equation (5.1), there are four variables in the second order term of the quadratic equation containing the complex conjugate poles. By increasing the transconductance of the second or third stage can suppress the second order term. However, it will increase the power consumption or transistor aspect ratio. In addition, we cannot alter the value of the loading capacitor because it depends on the next stage to be driven by the amplifier. In order to have consistence results between measurement and simulation, the minimum value of the loading capacitor should be at least equal to the capacitive loading from the measuring instruments. So the only one item we can make changes is the feedback capacitor Cc_1.

In the proposed compensation network, a voltage buffer is inserted at the input of the inner feedback path. The voltage buffer implements an impedance transformation, such that the infinite input impedance of the voltage buffer eliminates the loading effect

of the second stage. In addition, the low output impedance of the voltage buffer replaces the high impedance output of the second stage to drive the feedback capacitor Cc_1. Effectively, the relatively large RC time constant associated with the output of the second stage is replaced by a smaller one located at the output of the voltage buffer.

In the following section, the small signal model of the proposed circuit will be formulated. The reversed nested Miller compensation and the proposed compensation technique will be compared with analytical and simulation results.

5.2.3 Small Signal Analysis

Figure 5.2 illustrates the general structure of the proposed amplifier. The assumptions used in the analysis of reversed nested Miller compensation will also be applied here.

The small signal model is formulated as in figure 5.3. The parasitic capacitances at the output of the first and second stage are neglected, because their effects are insignificant when comparing with the two-feedback capacitors. This model takes into the account of non-ideal voltage buffer and rout models the finite output resistance of the voltage buffer.

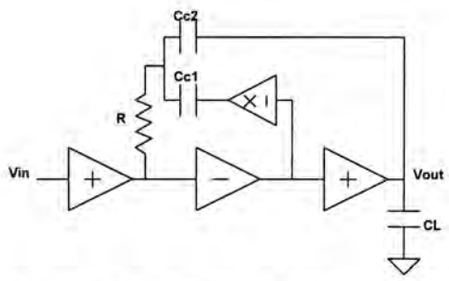


Figure 5.2: General structure of the proposed amplifier

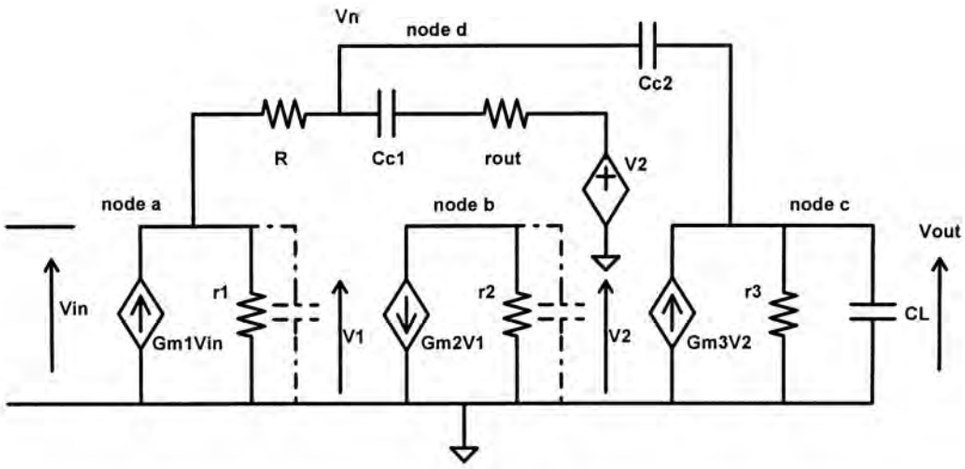


Figure 5.3: Simplified small signal model of the amplifier using the proposed compensation network

Solving for $\frac{Vout}{Vin}$, the transfer function of the proposed circuit is approximately given by equation 5.2. The detailed derivation steps are summarized in the appendix D.

$$A_{IRNMC}(s) \approx \frac{A_{DC}\left(1+\left(R(Cc_1+Cc_2)+Cc_1 rout-\frac{Cc_2}{gm_2 gm_3 r_2}\right)s+Cc_1Cc_2R\left(\frac{1}{gm_3}+rout\right)s^2\right)}{(Cc_2 gm_2 gm_3 r_1 r_2 r_3 s+1)\left(\frac{rout}{r_2}\frac{Cc_1C_L}{gm_2 gm_3}s^2+\left(\frac{Cc_1C_L}{Cc_2 gm_3}+\frac{Cc_1(1+gm_3 rout)}{gm_3}\right)s+1\right)} \quad (5.2)$$

where $A_{DC} = -gm_1 gm_2 gm_3 r_1 r_2 r_3$

It can also be written as:

$$A_{IRNMC}(s) \approx \frac{-\left(1+\left(R(Cc_1+Cc_2)+Cc_1 rout-\frac{Cc_2}{gm_2 gm_3 r_2}\right)s+Cc_1Cc_2R\left(\frac{1}{gm_3}+rout\right)s^2\right)}{\left(\frac{Cc_2}{gm_1}s\right)\left(\frac{rout}{r_2}\frac{Cc_1C_L}{gm_2 gm_3}s^2+\left(\frac{Cc_1C_L}{Cc_2 gm_3}+\frac{Cc_1(1+gm_3 rout)}{gm_3}\right)s+1\right)} \quad (5.3)$$

Similar to the reversed nested Miller compensation, the gain-bandwidth product is given by:

$$\omega_{GBW} = \frac{gm_1}{Cc_2} \quad (5.4)$$

5.2.4 Sign Inversion of the RHP Zero with Nulling Resistor

By observing the transfer function, there is certain freedom to modify the characteristic of the numerator through the use of a nulling resistor. By setting the first order term in the numerator to be positive, the roots of the numerator will always be located on the LHP. Effectively, the RHP zero in the reversed nested Miller compensation is inverted in sign to the LHP in the proposed circuit. The condition for the sign inversion to take place is approximately given by:

$$R \geq \left(\frac{Cc_2}{Cc_1 + Cc_2}\right)\left(\frac{1}{gm_2 r_2}\right)\left(\frac{1}{gm_3}\right) \quad (5.5)$$

RHP zero cancellation technique using nulling resistor is common in two-stage operational amplifier [12] [14]. However, there are several reasons to make the proposed compensation strategy different from the traditional one. Firstly, the suggested solution inverts the sign of RHP zero. In traditional technique, a nulling resistor is used to generate a pole over the RHP zero to exactly cannel it. Unfortunately, process tolerance or temperature variation often makes the resistance different from the theoretical value [16]. Consequently, the pole cannot fall exactly over the RHP zero and closely spaced pole-zero doublets are usually left. These doublets do not have significant effect on the phase margin or closed loop stability. However, these doublets introduce slow settling component in the step response [7], and settling time is usually a deterministic parameter for operational amplifier to be used in discrete time application [16].

In traditional compensation network, the nulling resistor value is equal to the reciprocal of output stage transconductance $\frac{1}{gm}$ [12] [15]. Under the requirement of low

power consumption, the output stage transconductance may be in the order of 10^{-4} or even lower. As a result, the corresponding resistance will be about tens of kilo ohms. The large resistor will consume chip area and its parasitic capacitance cannot be simply neglected. In this work, the nulling resistor is suppressed by a factor equal to the gain of the second stage as given by equation (5.4). The reduced nulling resistance enables the resistor to be implemented by the degenerated polysilicon gate of the transistor. It can provide a more accurate implementation and reduce the associated parasitic capacitances [16].

5.2.5 Frequency Multiplication of the Complex Conjugate Poles

Same as the analysis of reversed nested Miller compensation, the principle of superposition is applied again by considering the complex conjugate poles as a separated system [17].

$$\frac{1}{\left(\frac{rout}{r_2}\frac{Cc_1C_L}{gm_2gm_3}s^2+\left(\frac{Cc_1C_L}{Cc_2gm_3}+\frac{Cc_1(1+gm_3rout)}{gm_3}\right)s+1\right)} \quad (5.6)$$

Equation (5.6) shows the complex conjugate poles of the proposed compensation scheme. It can be observed that there is a factor equal to $\frac{rout}{r_2}$ in the highest order term of dominator. This observation has proved the significance of impedance transformation by the voltage buffer. In circuit level, the expression means that, the low output impedance of the voltage buffer replaces the high output impedance of the second gain stage to drive the inner feedback path Cc_1. In frequency domain, the expression represents that, the real part of the complex conjugate poles is multiplied by a factor roughly equal to $\frac{r_2}{rout}$. As a

result, the gain-bandwidth product of the amplifier can be enhanced by scaling down the compensation capacitor Cc_2 and at the same time, closed loop stability or phase margin is not degraded.

In addition, the implementation is economic because the modification of one circuit node leads to the frequency multiplication of two complex conjugate poles. Although the voltage buffer may consume extra power, the loading isolation by the voltage buffer can minimize the driving power of the second gain stage. Thus, the power consumption is not significantly increased after the circuit modification.

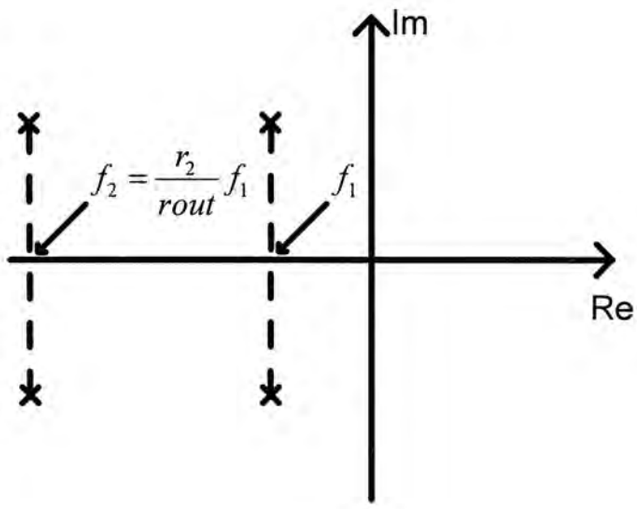


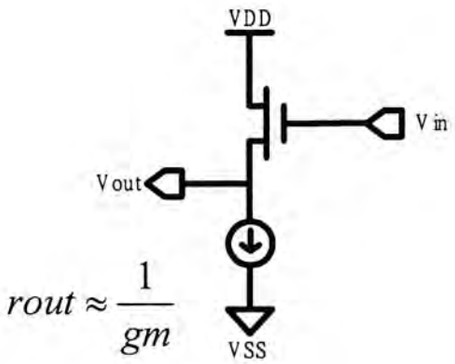
Figure 5.4: Frequency multiplication of the complex conjugate poles by the impedance transformation

By comparing the coefficients in expressions (5.6) and (4.8), the natural frequency ω_n and the damping factor for these complex conjugate poles are respectively given by:

$$\omega_n = \sqrt{\frac{r_2}{rout}}\sqrt{\frac{gm_2 gm_3}{Cc_1 C_L}} \quad (5.7)$$

$$\zeta = \frac{1}{2}\sqrt{\frac{r_2}{rout}}\sqrt{\frac{Cc_1 gm_2 gm_3}{C_L}}\left(\frac{C_L}{Cc_2 gm_3} + \frac{1+gm_3 rout}{gm_3}\right) \quad (5.8)$$

Comparing the two corresponding parameters in reversed nested Miller compensation, it can be seen that the natural frequency and the damping factor in the suggested circuit are enhanced by a factor roughly equal to $\sqrt{\frac{r_2}{rout}}$, where r_2 and $rout$ are the output resistances of the second gain stage and the voltage buffer respectively. If the second gain stage is a simple common source amplifier with long channel transistor (1um channel length is used to balance the trade-off between dc gain and bandwidth), the output resistance is generally in the range of about 100kΩ.



$$rout \approx \frac{1}{gm}$$

Figure 5.5: Voltage buffer implementation by common drain configuration

Moreover, the output resistance of a common drain voltage buffer is about 2-3 kΩ. With the above conditions, it is not difficult to draw the following conclusion.

$$\frac{r_2}{rout} > 10 \quad (5.9)$$

Hence, the real part of the complex conjugate poles is multiplied up by at least one decade in the frequency domain. In time domain response, the frequency multiplication leads to the enhancement of damping factor and minimization of the settling time.

5.2.6 Stability Conditions

In the suggested circuit, the first order term in the polynomial containing complex conjugate poles becomes always positive after the modification. It means that the complex conjugate poles will always be located on the LHP. In other words, positive exponential terms due to this pair of complex poles can never appear in the impulse response. This is an inherent feature of the suggested circuit and no special biasing scheme is required to achieve this.

In order to set the real parts of the complex conjugate poles outside the unity gain frequency, the following condition must be satisfied.

$$Cc_2 > \frac{\left(\frac{2gm_1 rout}{gm_2 r_2} - 1\right)}{1 + gm_3 rout} C_L \qquad (5.10)$$

The analytical method used in reversed nested Miller compensation is applied to here again. Assuming that the effect of the zeros is negligible and considering that the poles of the amplifier in unity-feedback configuration with a third-order Butterworth frequency response [8] [9] [10], the transfer function of unity-gain feedback $H(s)$ with cut-off frequency ω_o is given by:

$$H(s) = \frac{A_{IRNMC}(s)}{1 + A_{IRNMC}(s)}$$

$$H(s) = \frac{1}{1 + s(\frac{2}{\omega_o}) + s^2(\frac{2}{\omega_o^{\,2}}) + s^3(\frac{1}{\omega_o^{\,3}})} \qquad (5.11)$$

unity feedback configuration with Butterworth response

To obtain (5.11), the open loop transfer function of the amplifier should be in the format shown in (5.12):

$$A_{IRNMC}(s) = \frac{1}{s\frac{2}{\omega_o}\left[1 + s(\frac{1}{\omega_o}) + s^2(\frac{1}{2\omega_o^{\,2}})\right]} \qquad (5.12)$$

By using this model, three equations are set up by comparing the coefficients of the dominator in expression (5.3) with those of (5.12).

$$\frac{2}{\omega_o} = \frac{Cc_2}{gm_1}$$

$$\frac{1}{\omega_o} = \frac{Cc_1 C_L}{Cc_2 gm_3} + \frac{Cc_1(1 + gm_3 rout)}{gm_3}$$

$$\frac{1}{2\omega_o^{\,2}} = \frac{rout}{r_2}\frac{Cc_1 C_L}{gm_2 gm_3}$$

By solving the above equations, the dimensions of the two compensation capacitors are respectively given by:

$$Cc_2 = \frac{1}{4gm_1\left(rout + \frac{1}{gm_3}\right)}\left(4\frac{gm_1}{gm_3}\right)C_L \qquad (5.13)$$

$$Cc_1 = \left(\frac{1}{4gm_1(rout + \frac{1}{gm_3})}\right)^2\left(\frac{r_2}{rout}\right)\left(2\frac{gm_2}{gm_3}\right)C_L \qquad (5.14)$$

In equations (5.13) and (5.14), we have obtained sufficient information for the sizing of the compensation capacitors. Up to here, the analytical results for the reversed nested Miller compensation are recalled and compared with those of the proposed compensation scheme in table 5-1.

	Reversed Nested Miller Compensation	Improved Reversed Nested Miller Compensation
Gain-bandwidth product	$\frac{gm_1}{Cc_2}$	$\frac{gm_1}{Cc_2}$
Cc_2	$4\frac{gm_1}{gm_3}C_L$	$\frac{1}{4gm_1\left(rout+\frac{1}{gm_3}\right)}\left(4\frac{gm_1}{gm_3}\right)C_L$
Cc_1	$2\frac{gm_2}{gm_3}C_L$	$\left(\frac{1}{4gm_1(rout+\frac{1}{gm_3})}\right)^2\left(\frac{r_2}{rout}\right)\left(2\frac{gm_2}{gm_3}\right)C_L$
Underdamped natural frequency ω_n	$\sqrt{\frac{gm_2gm_3}{Cc_1C_L}}$	$\sqrt{\frac{r_2}{rout}}\sqrt{\frac{gm_2gm_3}{Cc_1C_L}}$
Damping factor ξ	$\frac{1}{2}\sqrt{\frac{Cc_1gm_2gm_3}{C_L}}\left(\frac{Cc_2+C_L}{Cc_2gm_3}-\frac{1}{gm_2}\right)$	$\frac{1}{2}\sqrt{\frac{r_2}{rout}}\sqrt{\frac{Cc_1gm_2gm_3}{C_L}}\left(\frac{C_L}{Cc_2gm_3}+\frac{1+gm_3rout}{gm_3}\right)$

Table 5-1: Analytical results for the reversed nested Miller compensation and the proposed compensation scheme

From table 5-1, the two compensation methods share the same expression for their gain-bandwidth products $\frac{gm_1}{Cc_2}$. However, the compensation capacitor Cc_2 has been suppressed by a factor $\frac{1}{4gm_1\left(rout+\frac{1}{gm_3}\right)}$ in the proposed circuit. In other words, the gain-bandwidth product of the proposed circuit is improved by a factor of $4gm_1\left(rout+\frac{1}{gm_3}\right)$ without increasing the transconductance of the first stage. Moreover, the damping factor for the complex conjugate poles has been improved by a factor

roughly equal to $\sqrt{\frac{r_2}{rout}}$. This modification leads to improvement in transient response such as settling time. In order to verify the analytical results listed in table 5-1, circuit simulation results will be presented in the next section.

5.3 Performance Comparison

In this section, a three-stage operational amplifier is designed using the improved reversed nested Miller compensation techniques. To facilitate the comparison, the phase margin and the power consumption will be set equal to that of the previous design in chapter 4. Finally, the performance parameter of the two designs will be compared.

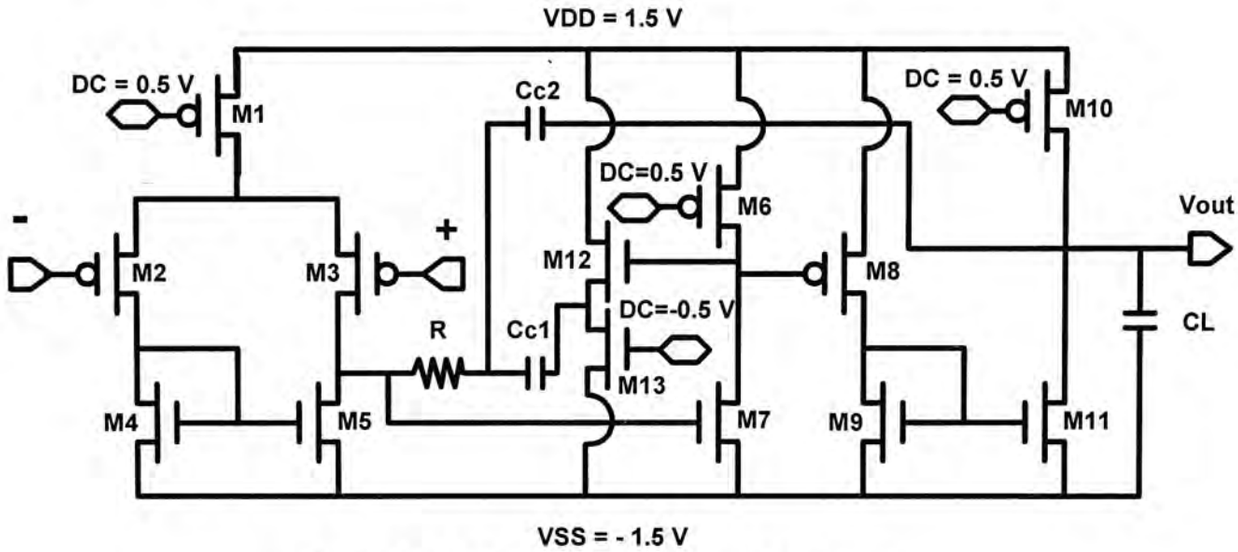


Figure 5.6: Schematic of the proposed amplifier

The schematic of the proposed amplifier is shown in the figure 5.6. The input and output stages are identical to the amplifier described in the previous chapter. In the second stage, loading isolation from the voltage buffer minimizes the driving power of the common source amplifier. Thus, power consumption is not increased although the proposed circuit introduces two additional transistors for the implementation of common

drain buffer. The aspect ratio for the transistors of the proposed amplifier is summarized in table 5-2.

Partitions of the amplifier	**Transistors**	**W/L**
First gain stage (differential amplifier)	M1	460u/1u
	M2, M3	27.6u/1u
	M4, M5	50u/1u
Second gain stage	M6	80u/1u
	M7	20u/1u
Third gain stage	M8	30u/1u
	M9	12u/1u
	M10	320u/1u
	M11	56u/1u
Common drain buffer	M12, M13	10u/0.6u

Table 5-2: Aspect ratio for the transistors in the proposed amplifier

The two amplifiers are designed with AMS 0.6 μm CMOS technology and their performance parameters are summarized in table 5-3. The step responses, gain responses and phase responses of the two amplifiers are shown in the figures 5.7, 5.8 and 5.9 respectively. The results of the proposed circuit are shown by solid line.

	Reversed Nested Miller Compensation (Schematic simulation)	Improved Reversed Nested Miller Compensation (Post-layout simulation)
Loading Capacitance (pF)	15	
Phase Margin (degrees)	61.2	59.7
DC Power Consumption (mW)	1.46	1.44
Gain-bandwidth product (MHz)	10.97	19.60
Settling time (Within 1% of step size) (ns)	194.9	64.22
+ Slew rate (Gain=1) (V/μs)	5.68	6.23
- Slew rate (Gain=1) (V/μs)	10.16	12.25
Cc_2 (pF)	5.8	3.0
Cc_1 (fF)	1300	700
R (Ω)	-	300
DC gain (dB)	96.9	96.9

Table 5-3: Performance summary of the two operational amplifiers

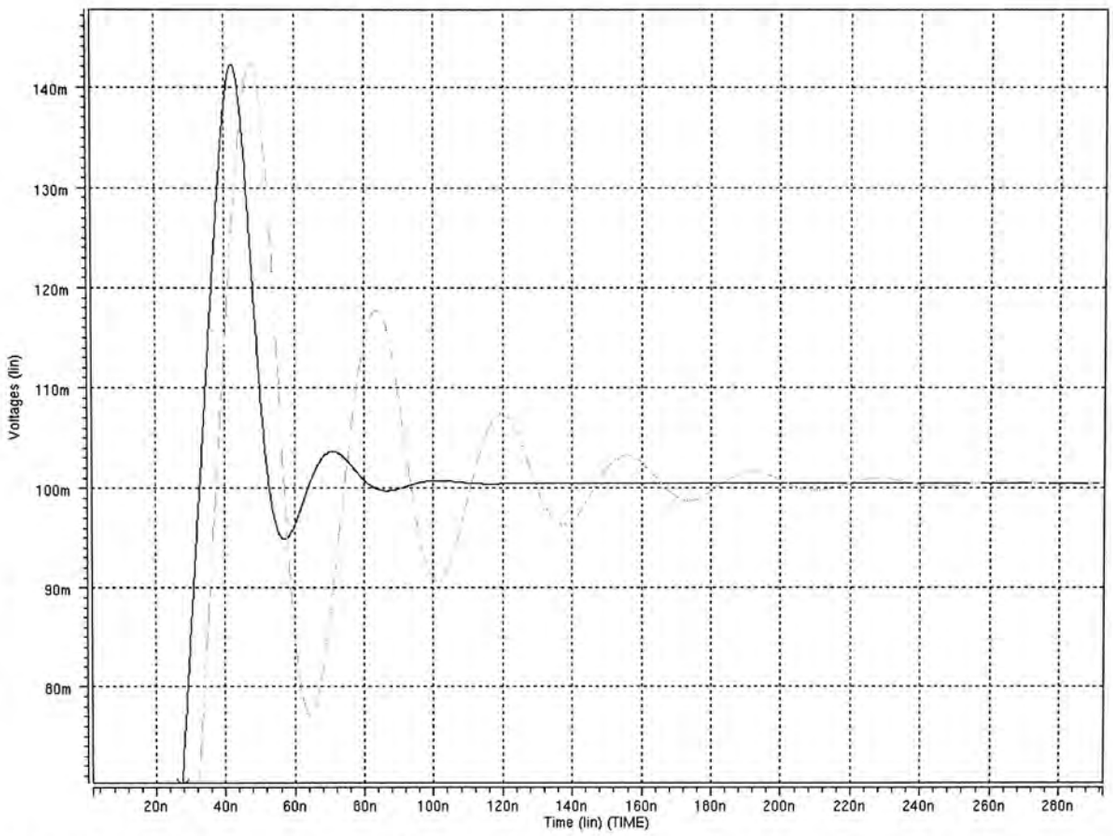


Figure 5.7: Transient response showing the shortened settling time of the proposed circuit

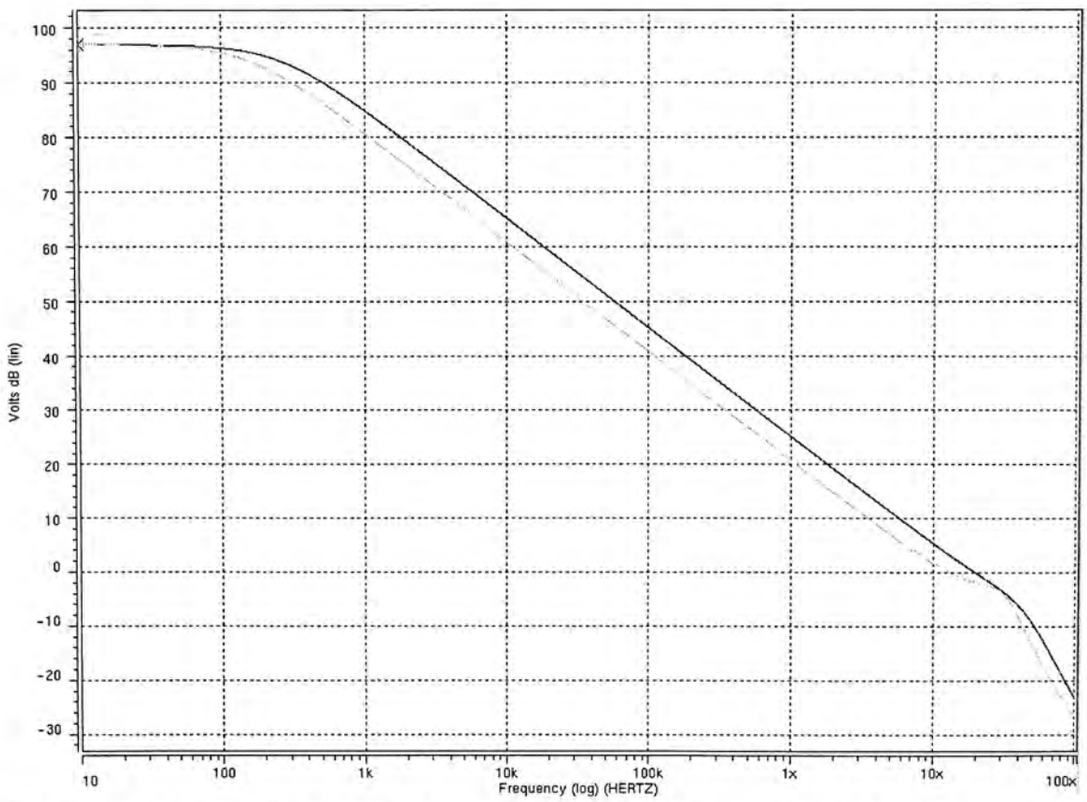


Figure 5.8: Gain responses of the amplifiers compensated by reversed nested Miller compensation and the proposed compensation technique

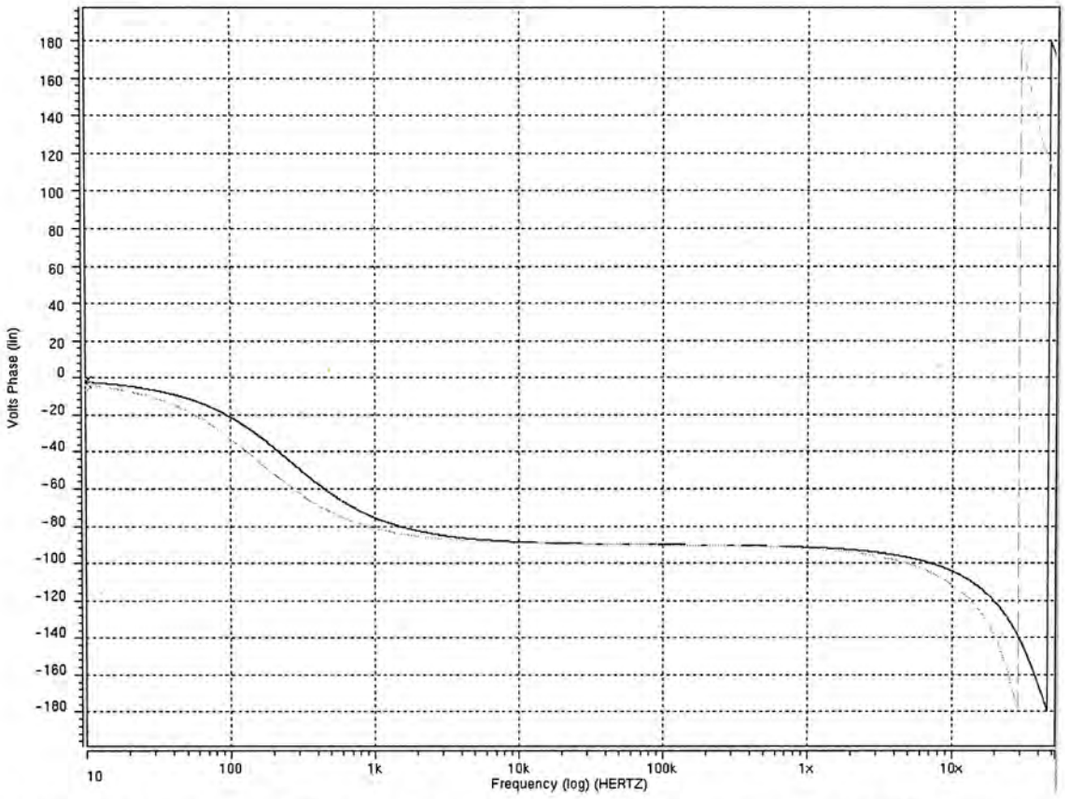


Figure 5.9: Phase responses of the amplifiers compensated by reversed nested Miller compensation and the proposed scheme

5.4 Conclusion:

Up to here, some conclusions about the improvement of reversed nested Miller compensation can be drawn.

5.4.1 Circuit Modifications:

1.) The RHP zero in reversed nested Miller compensation is inverted in sign and placed in LHP.

2.) The frequency of the complex conjugate poles is multiplied by a factor with magnitude larger than 10.

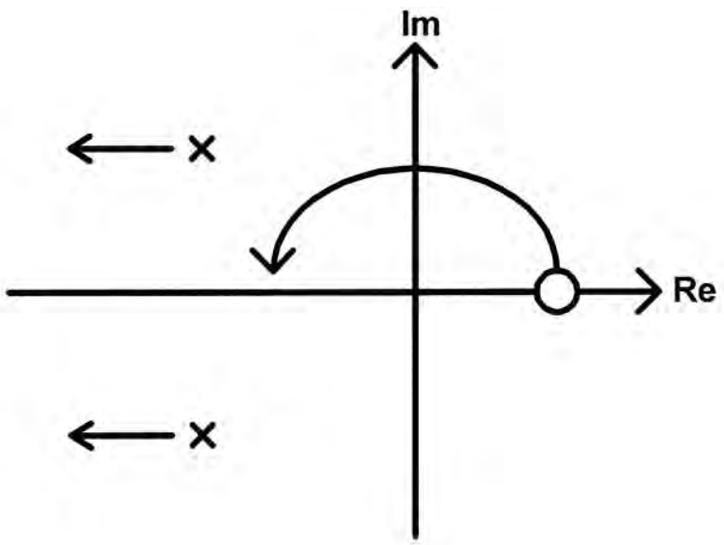


Figure 5.10: Positioning of the poles and zero after the circuit modification

5.4.2 Advantages:

1.) Gain-bandwidth product is improved without degrading stability or phase margin.

2.) Settling time is minimized due to the enhancement of damping factor for the complex conjugate poles.

3.) The small nulling resistance facilitates the implementation. Variations due to process tolerance can also be minimized because this is not a pole-zero cancellation technique and the resistance does not need to be exact.

Chapter 6 Physical Design of Operational Amplifier

6.1 Introduction

When the functionality of the circuit is verified at the schematic level, a layout representation of the circuit is made. The extracted layout contains the parasitic information, which is inherently present. A post-layout simulation can be carried out and it gives a more realistic and better performance evaluation of the circuit.

6.2 Transistor Layout Techniques

In analog circuit, the transistors are much bigger than those in digital circuit. Moreover, matching between transistors is essential in analog circuits such as the transistors in a differential pair. With a view to these requirements in analog circuit layouts, special transistor layout techniques are used to reduce area and parasitic capacitances associated with the transistors. The layout techniques are important because the parasitic capacitances will affect the speed and performance of the circuits.

6.2.1 Multi-finger Layout Technique

For a large transistor, it is usually realized using a parallel combination of small transistors. Those transistors have their source and drain terminals shared with their neighbors. It is clear that total source and drain areas are reduced and hence transistor area and parasitic capacitances. A layout diagram showing a large transistor is realized using four smaller transistors is shown in figure 6.1. Each smaller transistor has the same length as the large transistor, but its width is one-fourth of the large transistor.

It is obvious from figure 6.1 that node 1 contains two junctions J2 and J4, while node 2 contains three junctions J1, J3 and J5. Node 1 is usually the drain node as this

node has smaller junction area and hence less parasitic capacitance than node 2. The parasitic capacitance in the source node has no adverse effect if the source node is connected either to ground for a n-channel MOS or to supply for a p-channel MOS. This is due to the fact that the parasitic capacitances are shorted in these two cases.

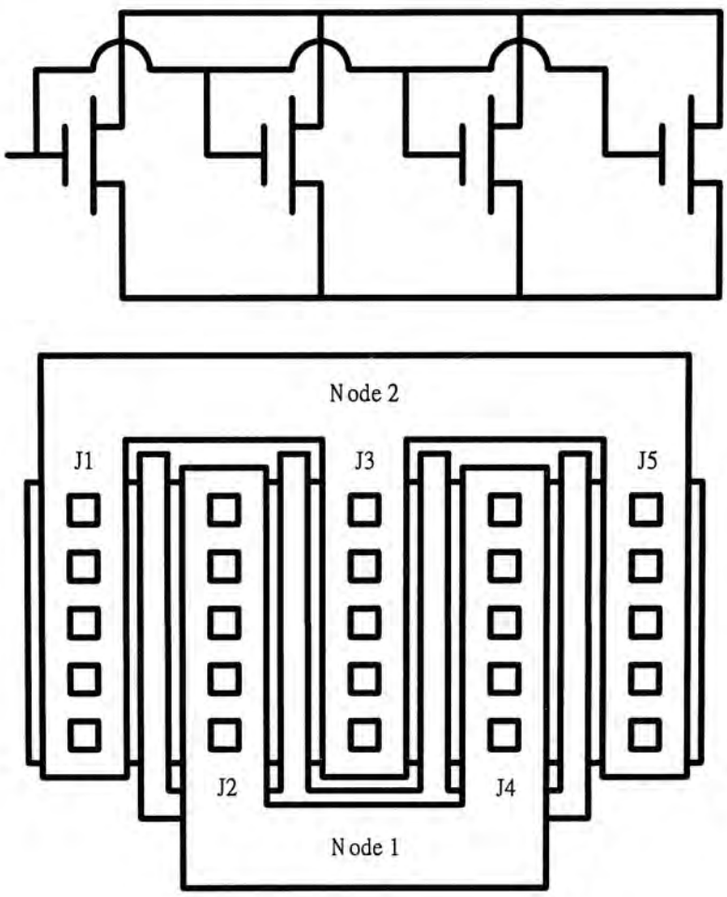


Figure 6.1: Multifinger layer technique for large transistor

6.2.2 Common-Centroid Structure

Some analog circuit building blocks like the differential pair and current mirror with unity gain demand two transistors to be identical or closely matched. These building blocks can be large in size. In order to minimize the gradient effects such as process and temperature variation across the circuit, they are realized by using multiple-gate fingers structure shown in figure 6.1. The fingers of one transistor are placed alternatively with

those of the second transistor. This structure is commonly known as common-centroid layout technique for minimization of error caused by gradient effects. A common centroid layout of a differential pair is shown in figure 6.2.

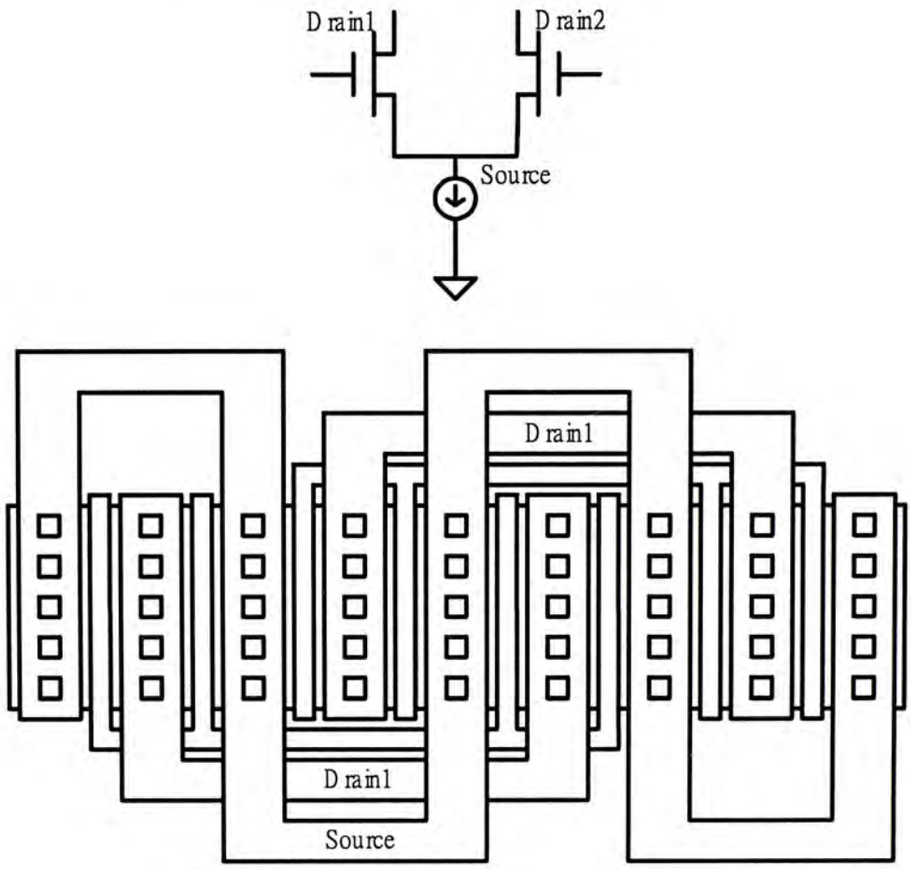


Figure 6.2: Common centroid layout technique for the differential pair

6.3 Layout Techniques of Passive Components

6.3.1 Capacitor Layout

Capacitors prove indispensable in most of today's analog CMOS circuits. Several parameters of capacitors are critical in analog design: nonlinearity (voltage dependence), parasitic capacitance to the substrate, series resistance, and capacitance per unit area. In CMOS technologies modified for analog design, capacitors are fabricated as "poly-diffusion," "poly-poly," or "metal-poly" structures. The poly-poly structure is used in this

project and its structure is illustrated in figure 6.3. The idea is to grow or deposit a relatively thin oxide between two floating conductive layers, thereby forming a dense capacitor with moderate bottom-plate parasitic.

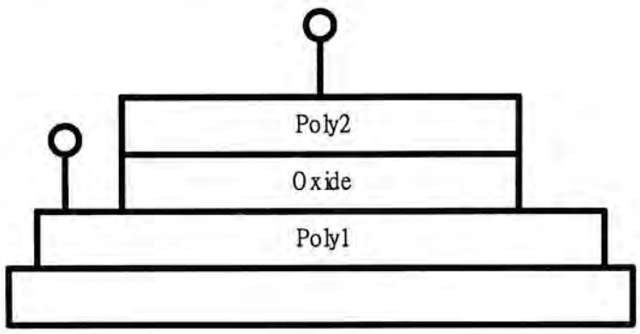


Figure 6.3: Capacitor with poly-poly structure

6.3.2 Resistor Layout

A CMOS process may be modified so as to provide resistors suited to analog design. A common method is to selectively "block" the silicide layer that is deposited on top of the polysilicon, thereby creating a region having the resistivity of the doped polysilicon.

The use of silicide on the two ends of the resistor in figure 6.4 results in a much lower contact resistance than that obtained by directly connecting the metal layer to doped polysilicon. This improved both the definition of the resistor value and the matching with identical structures. Also, for a given resistance, poly resistors typically exhibit much less capacitance to the substrate than other types. These resistors are quite linear, especially if they are long. The primary difficulties with silicide-block poly resistors are variability, mask cost and process complexity.

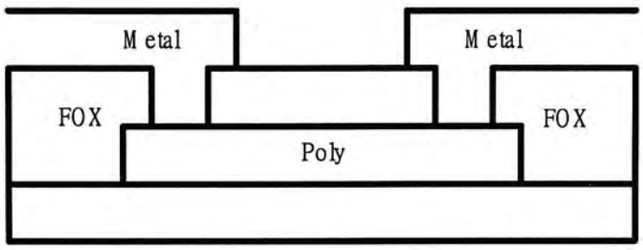


Figure 6.4: Poly resistor structure

Chapter 7 Measurement Results

7.1 Overview

The two operational amplifiers presented in the previous chapters are fabricated with AMS 0.6μm CMOS technology. The test chips are experimental evaluated and the measurement results are presented in this chapter.

7.2 Measurement Results for the Current Feedback Operational Amplifier

7.2.1 Frequency Response of the inverting amplifier

The setup shown in figure 7.1 is used to measure the frequency response of the inverting amplifier constructed by the current feedback operational amplifier. Micro-photographs of both chips are shown in the appendix.

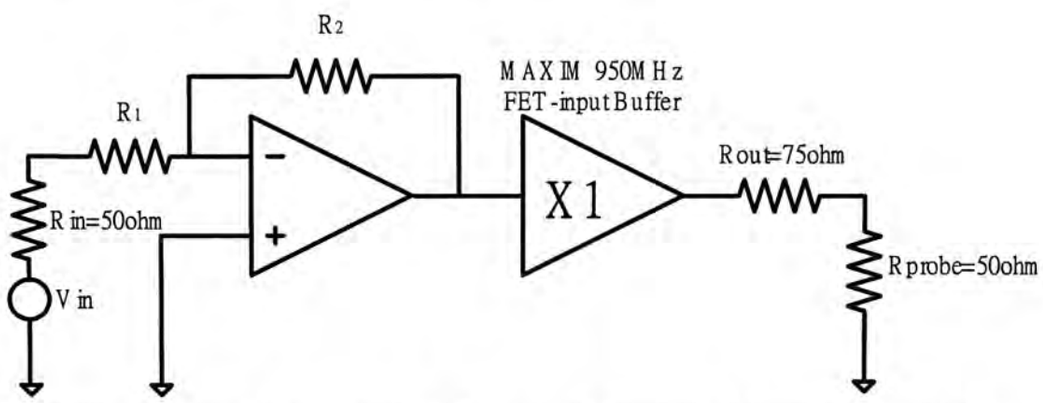
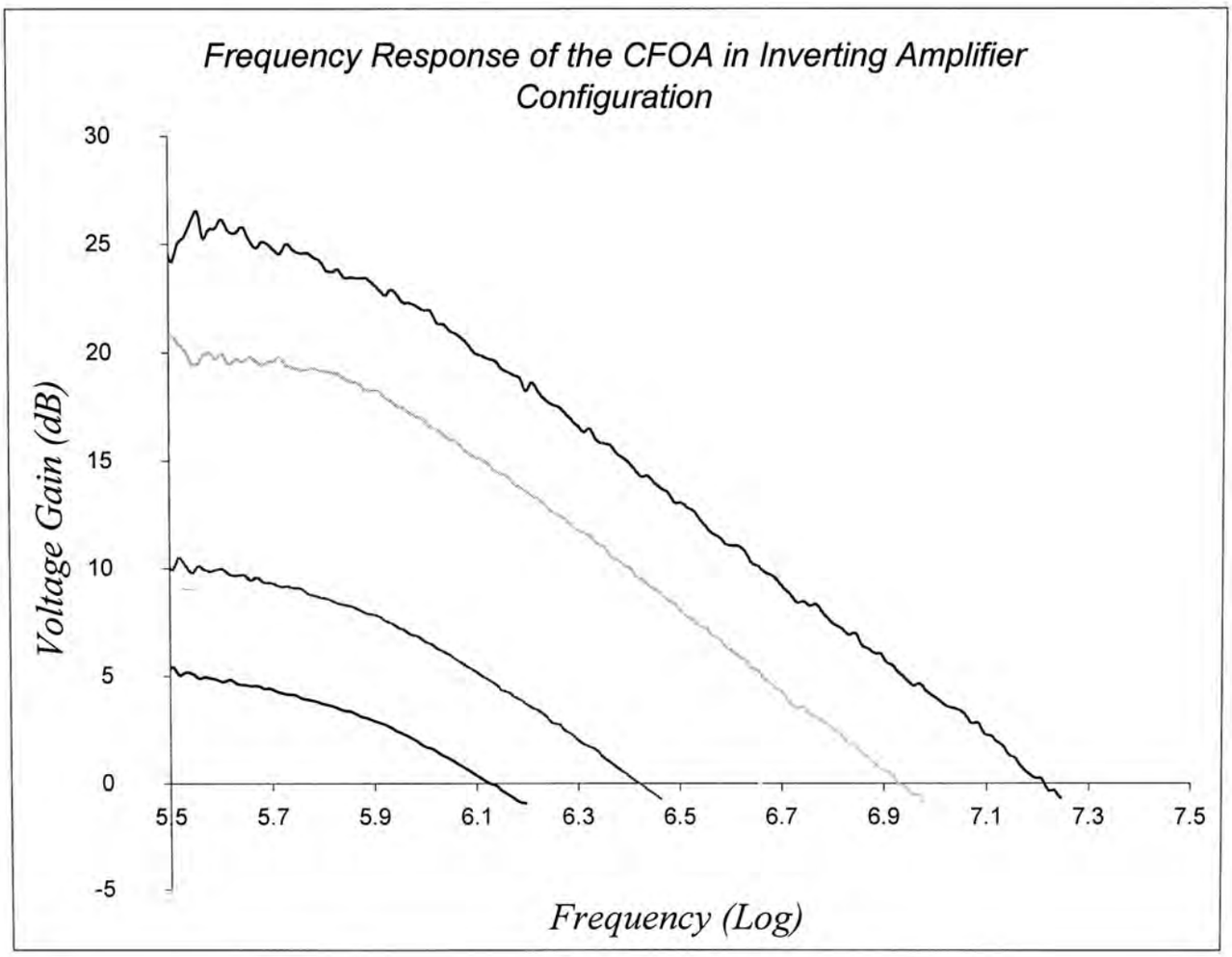


Figure 7.1: Setup for measuring the frequency response of inverting amplifier

A 50 Ohms resistor models the input impedance of the network analyzer. A voltage buffer is used to isolate the inverting amplifier from the network analyzer and eliminate the loading effect to the amplifier by having a FET-input and 75 Ohms output impedance. The gain responses of the inverting amplifier were measured by the s-parameter S21.

The frequency responses of the inverting amplifier with various gain configurations are shown in the following figure. The 3dB bandwidth is relatively constant and thus the unity gain frequency increases linearly with the gain of the amplifier. Table 7-1 shows a numerical summary of the AC performance of the inverting amplifier.



Closed-loop Gain	3-dB Bandwidth	Unity gain frequency	Phase Margin (degree)
10 dB	1.284MHz	4.26MHz	96.0
15 dB	1.123MHz	6.08MHz	81.2
20 dB	1.023MHz	10.78MHz	79.7
25 dB	925.5kHz	16.04MHz	51.1

Table 7-1: 3-dB bandwidth, unity gain frequency and phase margin as a function of closed-loop gain

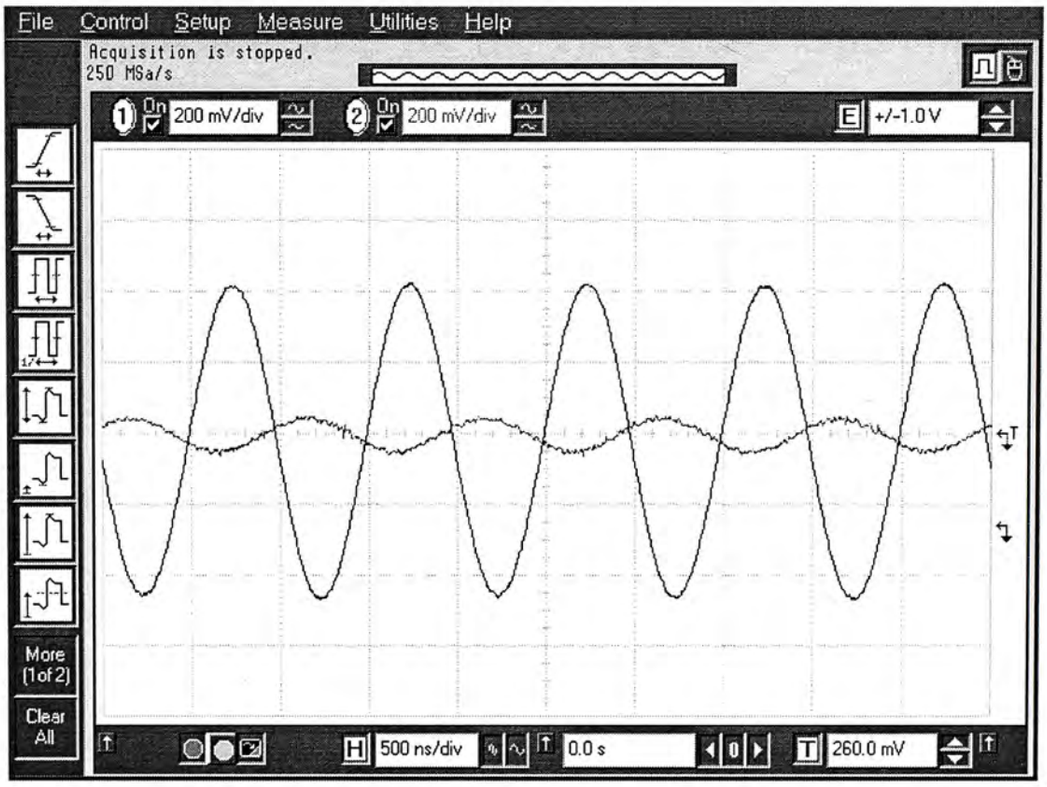


Figure 7.2: Waveform of inverting configuration with 20dB of gain at 1MHz

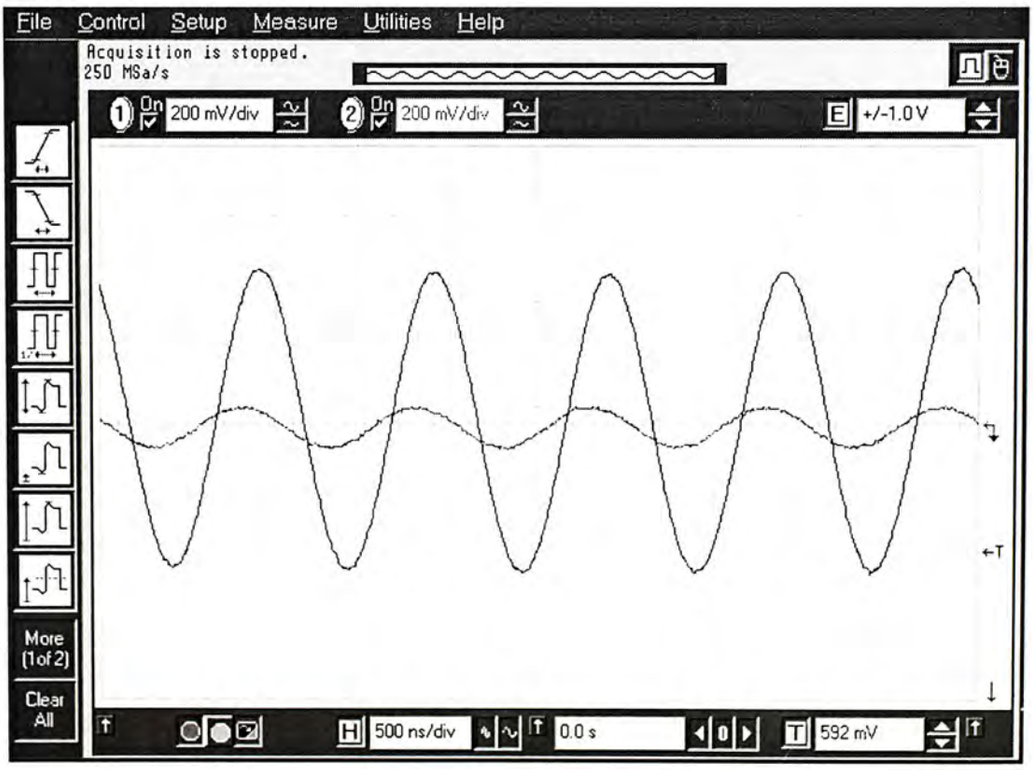


Figure 7.3: Waveform of non-inverting configuration with 20 dB of gain at 1MHz

7.3 Measurement Results for the Three-Stage Operational Amplifier

7.3.1 Input Offset Voltage Measurement

By connecting the operational amplifier in unity gain configuration, the input offset voltage is measured at the output node with the input connected to ground. The circuit schematic is shown in the figure 7.4.

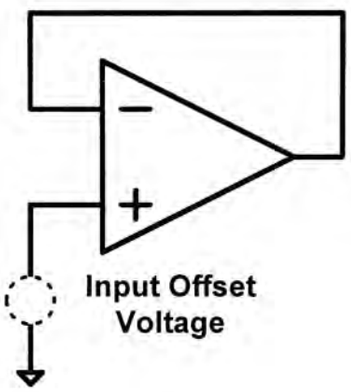


Figure 7.4: Setup for measuring the input offset voltage

The measured input offset voltage is equal to 7.4mV.

7.3.2 Input Common Mode Range Measurement

With the same setup for measuring the input offset voltage, the DC transfer characteristic for the unity gain configuration is obtained by sweeping the input DC source. The output voltage is plotted against the corresponding input in figure 7.5. The input common mode range is between -1.4V to +1.27V as shown in figure 7.5.

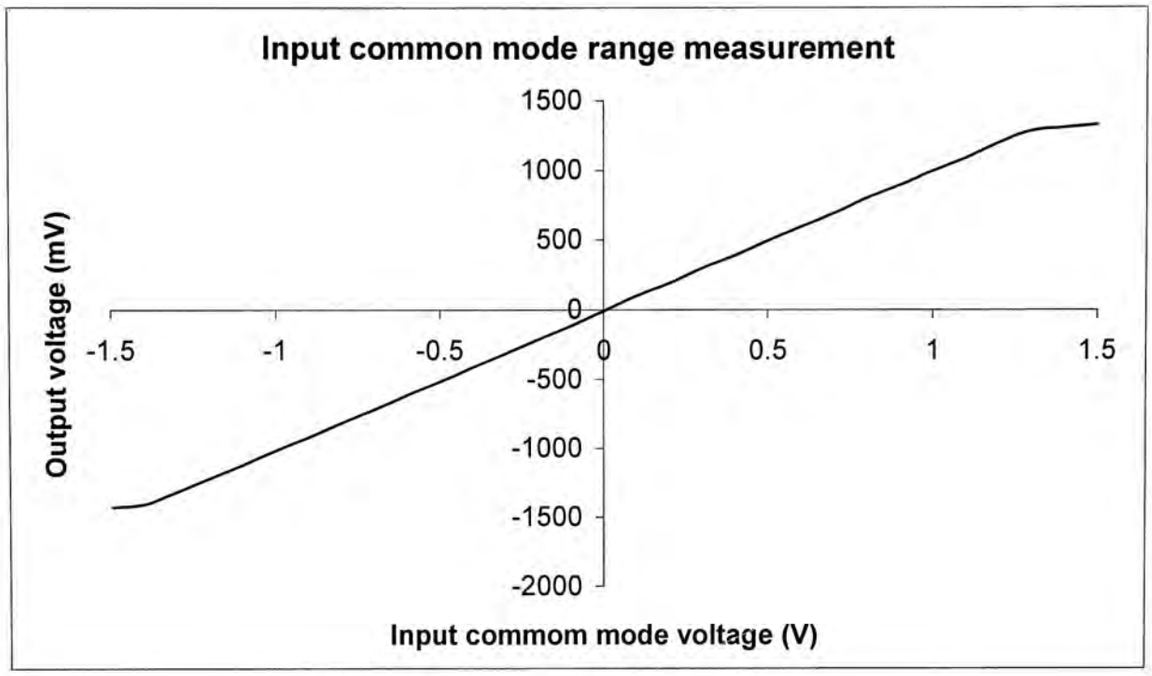


Figure 7.5: DC transfer characteristic of the unity gain configuration

7.3.3 Gain Bandwidth Measurement

The oscillator circuit in figure 7.6 is used to determine the gain bandwidth product of the voltage feedback operational amplifier [20]. Without an input signal source, the gain bandwidth product is measured by determining the oscillation frequency and the values of the passive components.

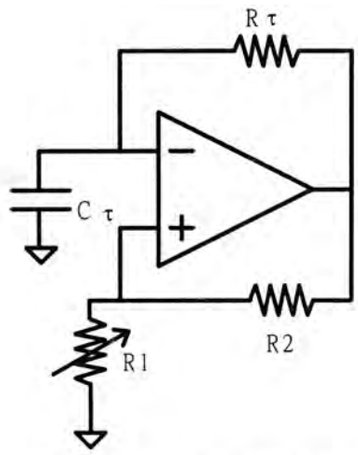


Figure 7.6: Circuit for determining the gain-bandwidth product of the operational amplifier

The following model is used to understand the nature of the oscillator circuit shown in figure 7.6. The relationship between the gain-bandwidth product and the oscillation frequency is derived with the help of the following model.

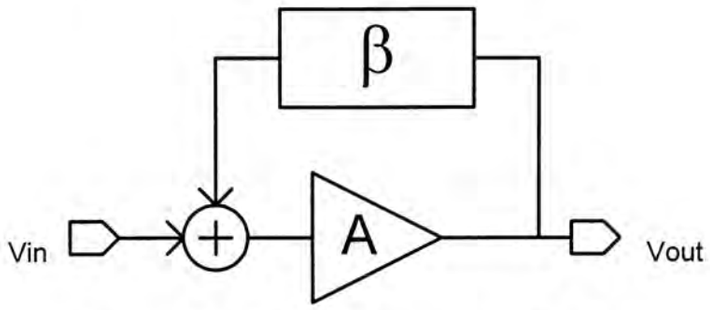


Figure 7.7: Model for the oscillator circuit

The transfer function of the circuit shown in figure 7.7 is given by:

$$\frac{V_{out}}{V_{in}} = \frac{A}{1 - A\beta} \quad (7.1)$$

From the circuit schematic in figure 7.6,

Positive feedback factor, $\beta + = \frac{R_1}{R_1 + R_2}$ (7.2)

Negative feedback factor, $\beta - = \frac{\frac{1}{sC_\tau}}{R_\tau + \frac{1}{sC_\tau}} = \frac{1}{1 + sR_\tau C_\tau}$ (7.3)

Assume that the open loop transfer function of the operational amplifier is given by,

$$A = \frac{A_0}{1 + \frac{s}{\omega_0}} \quad (7.4)$$

By putting equations (7.2), (7.3) and (7.4) into equation (7.1), the closed loop transfer function of the oscillator circuit is given by,

$$\frac{V_{out}}{V_{in}} = \frac{A}{1 - A\beta} \quad where \ \beta = \beta_+ - \beta_-$$

$$\frac{V_{out}}{V_{in}} = \frac{A_0\omega_0(s + \frac{1}{R_\tau C_\tau})}{s^2 + s(\frac{1}{R_\tau C_\tau} + \omega_0 - A_0\omega_0\beta_+) + \frac{\omega_0}{R_\tau C_\tau}(1 + A_0 - A_0\beta_+)} \quad (7.5)$$

By adjusting the resistance of R_1 or the positive feedback factor to satisfy the condition in equation (7.6),

$$\beta_+ = \frac{\frac{1}{R_\tau C_\tau} + \omega_0}{A_0\omega_0} \quad (7.6)$$

The first order term in the dominator becomes zero and the pair of complex conjugate poles is placed exactly on the imaginary axis.

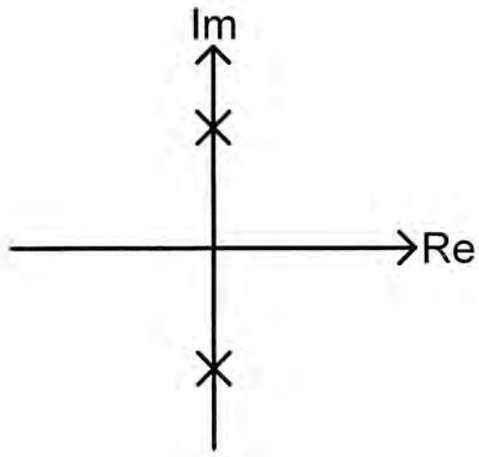


Figure 7.8: Locations of the complex conjugate poles

The circuit in figure 7.6 starts to oscillate and the natural frequency of the oscillation is given by,

$$\omega^2 = \frac{\omega_0}{R_\tau C_\tau}(1 + A_0 - A_0\beta_+)$$

$$\omega^2 \approx \frac{\omega_0}{R_\tau C_\tau} A_0(1 - \beta_+)$$

$$\omega^2 \approx \frac{GBW}{R_\tau C_\tau}(1 - \beta_+) \quad (7.7)$$

By putting equation (7.6) into equation (7.7),

$$GBW = R_\tau C_\tau \left(\omega^2 + \frac{\frac{1}{R_\tau C_\tau} + \omega_0}{R_\tau C_\tau} \right)$$

$$GBW = R_\tau C_\omega \omega^2 + \frac{1}{R_\tau C_\tau} + \omega_0$$

$$GBW \approx R_\tau C_\tau \omega^2 + \frac{1}{R_\tau C_\tau} \quad (7.8)$$

The experimental values for the passive components are listed in the following table. The waveform of oscillation is captured together with the period of oscillation.

Component	Measured values
$R_\tau(k\Omega)$	1.3571
$C_\tau(\mu F)$	0.01

Table 7-2: Component values used in the experiment

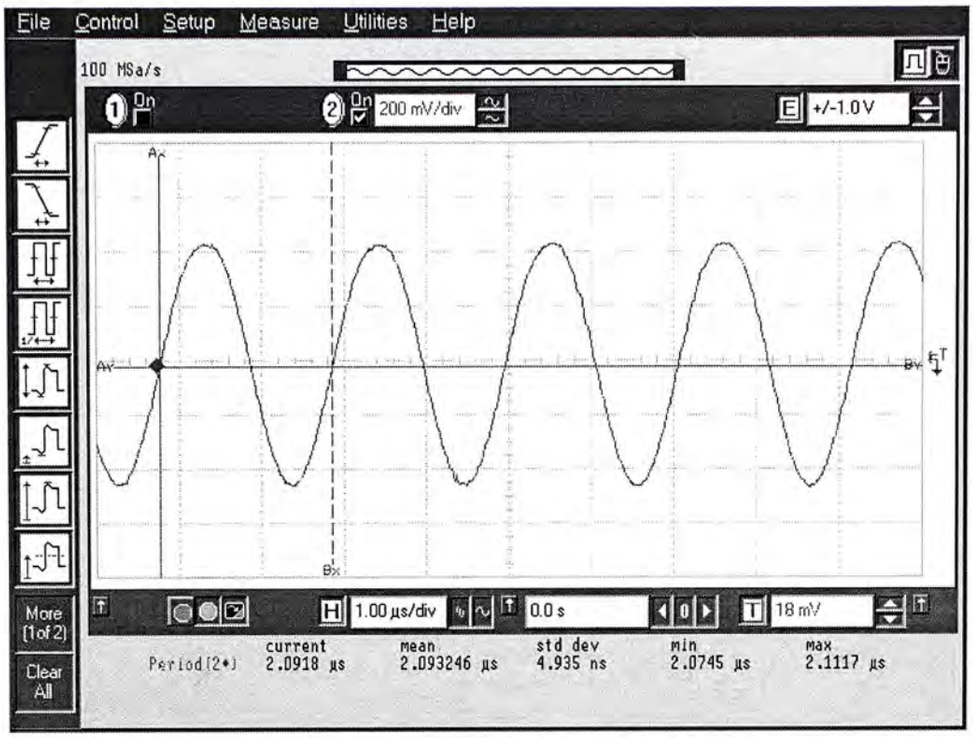


Figure 7.9: Waveform of the oscillator for determining the gain-bandwidth product of the operational amplifier

The mean period of oscillation was measured to be 2.093246 μs

$$GBW = (1.3571\times10^{3})(0.01\times10^{-6})(\frac{2\pi}{2.093246\times10^{-6}})^{2} + \frac{1}{(1.3571\times10^{3})(0.01\times10^{-6})}$$

$$GBW \approx \underline{\underline{19.47MHz}}$$

7.3.4 DC Gain measurement

With the same setup for the measurement of gain-bandwidth product, the DC gain of the operational amplifier is estimated by using the positive feedback factor.

From the previous analysis, we already know that the positive feedback factor is given by:

$$\beta_+ = \frac{\frac{1}{R_\tau C_\tau} + \omega_0}{A_0 \omega_0}$$

$$\beta_+ = \frac{\frac{1}{R_\tau C_\tau} + \frac{GBW}{A_0}}{GBW}$$

By rearrange the terms, we have

$$A_0 = \frac{GBW}{\beta_+ GBW - \frac{1}{R_\tau C_\tau}} \qquad (7.9)$$

The experiment for the measurement of gain-bandwidth product was repeated to obtain another set of data.

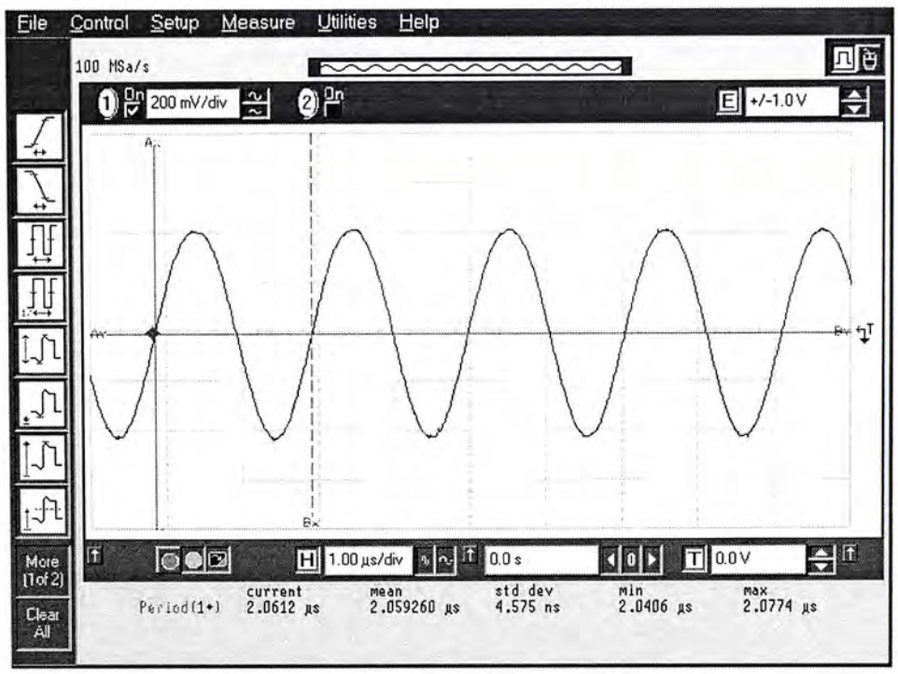


Figure 7.10: Waveform of the oscillator for determining the DC gain of the operational amplifier

Period of oscillation (µs)	2.059260
Rτ (kΩ)	1.3571
Cτ (µF)	0.01
R2 (kΩ)	99.804
R1 (Ω)	65.184

Table 7-3: Numerical summary for the determination of the DC gain

$$A_0 = \frac{(2\pi \times 20.12 \times 10^6)}{\frac{65.184(2\pi \times 20.12 \times 10^6)}{65.184 + 99.804 \times 10^3} - \frac{1}{(1.3571 \times 10^3)(0.01 \times 10^{-6})}}$$

$$A_0 \approx \underline{\underline{83.12dB}}$$

Thus, the DC gain was estimated to be 83.12 dB.

7.3.5 Slew Rate Measurement

The slew rate of the operational amplifier was measured by using the unity gain configuration. The high impedance input of the oscilloscope was modeled by using a 10MΩ resistor and a 10pF capacitor.

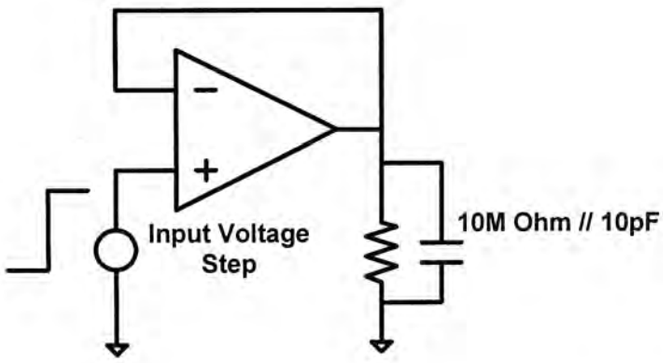


Figure 7.11: Setup for the measurement of the slew rate

The captured waveforms of the above schematic are shown below. The slew rate is given by the maximum rate of change of the output voltage.

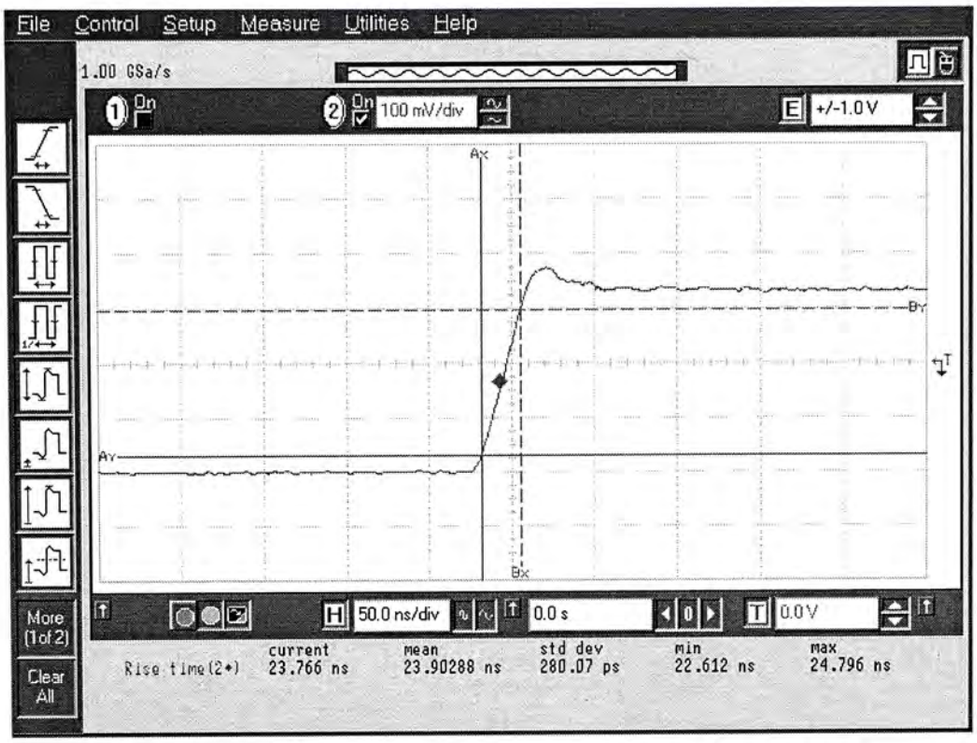


Figure 7.12: Waveform for the measurement of the slew rate

With this method, the + slew rate and – slew rate were measured to be 11.1 V/μs and 16.5 V/μs respectively.

7.3.6 Phase Margin

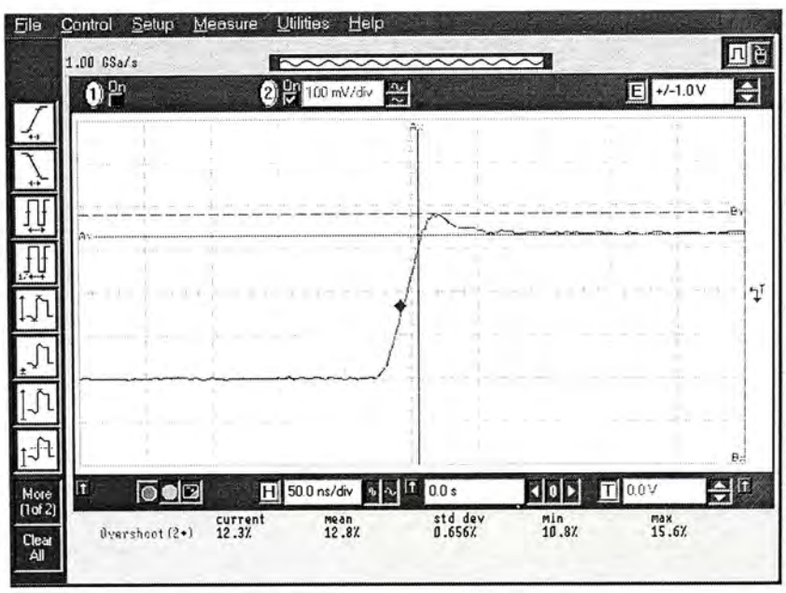


Figure 7.13: Waveform for the measurement of percentage overshoot

The percentage overshoot was measured to be about 12.8% and the phase margin was determined by the expressions (7.10) and (7.11) [21] [22].

$$Percentage\ \ Overshoot = e^{\frac{-\pi\xi}{\sqrt{1-\xi^2}}} \qquad (7.10)$$

$$Phase\ \ M\arg in = \tan^{-1}\left\{2\xi\sqrt{\frac{1}{\sqrt{4\xi^4+1}-2\xi^2}}\right\} \qquad (7.11)$$

The phase margin was determined to be about 55.50^{o}

7.3.7 Performance Summary

VDD (V)	1.5
VSS (V)	-1.5
Pbias (V)	0.5
Nbias (V)	-0.5
Input offset voltage (mV)	7.4
Input common mode voltage range	-1.4V to +1.27V
Loading capacitance (pF)	15
Gain-bandwidth product (MHz)	19.46
Phase margin (degree)	55.50
DC Gain (dB)	83.12
+ Slew rate (V/μs)(Unity gain configuration)	11.1
- Slew rate (V/μs)(Unity gain configuration)	16.5
Overshoot (%)	12.8
Settling time (ns) (Within 1% of the step size)(unity gain +1)	114.95
DC power consumption (mW)	1.4

Table 7-4: Measurement results of the voltage feedback operational amplifier

Chapter 8 Conclusions

In this work, a two-stage current feedback operational amplifier and a three-stage voltage feedback operational amplifier were designed. Due to the gain degradation in modern sub-micron CMOS technology, multistage architecture was adopted in these two designs and compensation methods were suggested to relax the bandwidth reduction and stability problem in these multiple poles system.

The first design is a two-stage current feedback operational amplifier. The open loop transimpedance gain and output voltage swing are improved by the two-stage architecture. Active current mode compensation is used to preserve the bandwidth in the presence of additional signal delay in the second gain stage. This compensation technique made use of an embedded current buffer with no extra component is needed. Thus, the resulting circuit topology can be kept simple and power consumption is minimized. The design of this current feedback operational amplifier is summarized in chapter 3 and the measurement results are reported in chapter 7.

In the three-stage voltage feedback operational amplifier, an enhancement technique for reversed nested Miller compensation is proposed. In contrast to previous reported techniques, we invert the sign of the RHP zero rather than exactly cancelled it or shifted it to higher frequency. Thus, the stability problem due to the RHP zero is completely solved. In addition, the real part of the complex conjugate poles is multiplied by a factor with magnitude larger than 10. Consequently, the complex conjugate poles are shifted up by at least one decade in the frequency domain. As a result, gain bandwidth product and settling time are improved without degrading the stability. Moreover, the small nulling resistance facilitated the physical implementation. Variations due to process tolerance

could be minimized because this is not a pole-zero cancellation technique and the nulling resistance does not need to be very accurate.

In order to verify the proposed technique, a test chip was fabricated with 0.6um CMOS technology. The measurement results show good agreement with the analytical and simulation results. The gain-bandwidth product and phase margin of this three-stage operational amplifier are equal to 19.46MHz and 55.5° respectively, with a capacitive loading of 15pF. Moreover, a measured DC open loop gain of 83.12 dB and the fast settling time has demonstrated.

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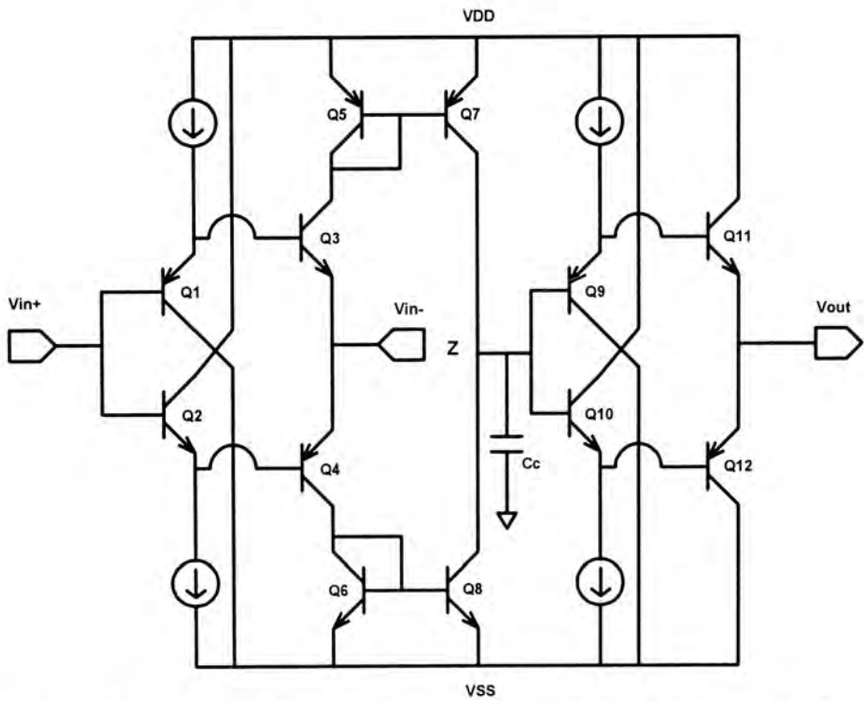
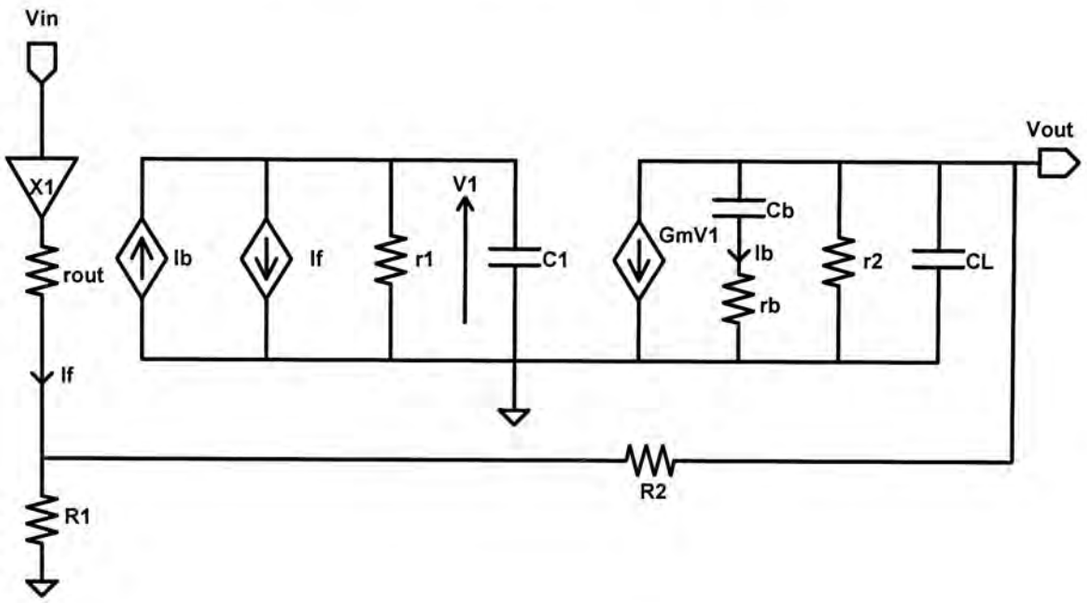
Chapter 9 Appendix

Appendix A: Schematic of a Conventional Current Feedback Operational Amplifier



The input unity gain buffer consists of transistors Q1-Q4. Q3 and Q4 are a complementary pair and they are configured to form a push pull stage with low output impedance. Q5 and Q6 sense the feedback current and then mirror the current to the high impedance node formed by Q7 and Q8. The output stage consisting of Q9-Q12 buffers the voltage at the high impedance node Z to the output, thereby providing low output impedance. Dominant pole compensation is realized by placing a capacitor between the high impedance node and ground.

Appendix B: Derivation of transfer function for the current feedback operational amplifier



By applying KCL, four equations are written down.

$$V_1 - \left(Iin - \frac{Vin - V_2}{rout} \right)\left(\frac{r_1}{1 + r_1 C_1 s} \right) = 0$$

$$Iin - \frac{sC_b Vout}{1 + r_b C_b s} = 0$$

$$gm_2 V_1 + Iin + \frac{(1 + r_2 C_L s)Vout}{r_2} - \frac{V_2 - Vout}{R_2} = 0$$

$$\frac{Vout - V_2}{R_2} + \frac{Vin - V_2}{rout} - \frac{V_2}{R_1} = 0$$

By solving the above equations, $\frac{Vout}{Vin}$ is given by:

$$rout \approx 0$$

$$\frac{Vout}{Vin} \approx \frac{r_2(1 + r_b C_b s)(R_1 + gm_2 r_1 R_1 + gm_2 r_1 R_2 + C_1 r_1 R_1 s)}{C_1 C_b C_L r_1 r_2 R_1 R_2 r_b s^3 + (C_1 C_b r_1 r_2 R_1 R_2 + C_1 C_L r_1 r_2 R_1 R_2 + C_1 C_b r_1 r_2 r_b R_1 + C_1 C_b r_1 r_b R_1 R_2 + C_b C_L r_2 r_b R_1 R_2)s^2 + (C_1 r_1 r_2 R_1 + C_1 r_1 R_1 R_2 + C_b r_2 R_1 R_2 + C_L r_2 R_1 R_2 + C_b r_2 r_b R_1 + C_b r_b R_1 R_2 + C_b gm_2 r_1 r_2 R_1 (R_2 + r_b))s + R_1 r_2 + gm_2 r_1 r_2 R_1 + R_1 R_2}$$

In the dominator,

The constant term is given by:

$$= R_1 r_2 + gm_2 r_1 r_2 R_1 + R_1 R_2$$
$$\approx R_1 r_2 + gm_2 r_1 r_2 R_1$$

The first order term is given by:

$$= C_1 r_1 r_2 R_1 + C_1 r_1 R_1 R_2 + C_b r_2 R_1 R_2 + C_L r_2 R_1 R_2 + C_b r_2 r_b R_1 + C_b r_b R_1 R_2 + C_b gm_2 r_1 r_2 R_1 (R_2 + r_b)$$
$$\approx C_1 r_1 r_2 R_1 + C_b gm_2 r_1 r_2 R_1 (R_2 + r_b)$$

The second order term is given by:

$$= C_1 C_b r_1 r_2 R_1 R_2 + C_1 C_L r_1 r_2 R_1 R_2 + C_1 C_b r_1 r_2 r_b R_1 + C_1 C_b r_1 r_b R_1 R_2 + C_b C_L r_2 r_b R_1 R_2$$
$$\approx C_1 C_b r_1 r_2 R_1 R_2 + C_1 C_L r_1 r_2 R_1 R_2$$

By using the approximated values, the transfer function is simplified as:

$$\frac{Vout}{Vin} \approx \frac{r_2(1 + r_b C_b s)(R_1 + gm_2 r_1 R_1 + gm_2 r_1 R_2 + C_1 r_1 R_1 s)}{C_1 C_b C_L r_1 r_2 R_1 R_2 r_b s^3 + (C_1 C_b r_1 r_2 R_1 R_2 + C_1 C_L r_1 r_2 R_1 R_2) s^2 + (C_1 r_1 r_2 R_1 + C_b gm_2 r_1 r_2 R_1 (R_2 + r_b)) s + R_1 r_2 + gm_2 r_1 r_2}$$

$$\frac{Vout}{Vin} \approx \frac{(1 + r_b C_b s)(R_1 + gm_2 r_1 R_1 + gm_2 r_1 R_2 + C_1 r_1 R_1 s)}{C_1 C_b C_L r_1 R_1 R_2 r_b s^3 + (C_1 C_b r_1 R_1 R_2 + C_1 C_L r_1 R_1 R_2) s^2 + (C_1 r_1 R_1 + C_b gm_2 r_1 R_1 (R_2 + r_b)) s + R_1 + gm_2 r_1 R_1}$$

$$\frac{Vout}{Vin} \approx \frac{1}{gm_2 r_1 R_1} \frac{(1 + r_b C_b s)(R_1 + gm_2 r_1 R_1 + gm_2 r_1 R_2 + C_1 r_1 R_1 s)}{\frac{C_1 C_b C_L R_2 r_b}{gm_2} s^3 + \frac{(C_1 C_b R_2 + C_1 C_L R_2)}{gm_2} s^2 + \frac{(C_1 + C_b gm_2 (R_2 + r_b))}{gm_2} s + 1}$$

By using the dominant pole approximation,

The dominant pole is

$$= -\frac{1}{\frac{(C_1 + C_b gm_2 (R_2 + r_b))}{gm_2}}$$

$$= -\frac{gm_2}{C_1 + C_b gm_2 (R_2 + r_b)}$$

$$\approx -\frac{gm_2}{C_b gm_2 (R_2 + r_b)}$$

$$\approx -\frac{1}{C_b R_2}$$

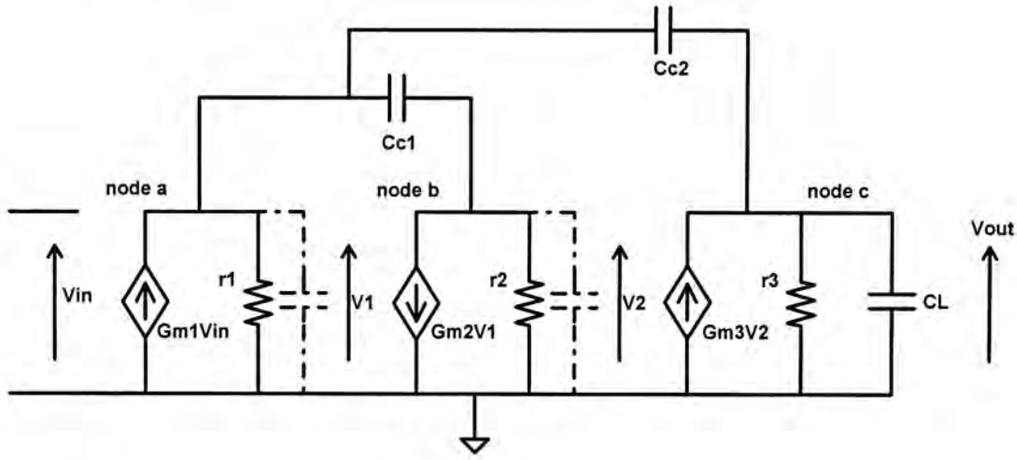
Thus, the transfer function can be written in the following format,

$$\frac{Vout}{Vin} \approx \frac{1}{gm_2 r_1 R_1} \frac{(1 + r_b C_b s)(R_1 + gm_2 r_1 R_1 + gm_2 r_1 R_2 + C_1 r_1 R_1 s)}{(C_b R_2 s + 1)(as^2 + bs + 1)}$$

With further simplification, the transfer function is given by:

$$\frac{V_{OUT}}{V_{IN}} \approx \frac{1}{G_m R_1 r_1} \frac{(R_1 + G_m R_1 r_1 + G_m R_2 r_1 + sR_1 r_1 C_1)(1 + sr_b C_b)}{(1 + sR_2 C_b)\left[\frac{r_b C_1 C_L}{G_m} s^2 + (\frac{C_1}{G_m} + \frac{C_1 C_L}{G_m C_b})s + 1\right]}$$

Appendix C: Derivation of transfer function for the amplifier using reversed nested Miller compensation



By applying KCL, three equations are written down:

$$node\,a: \quad \frac{V_1}{r_1} + sCc_1(V_1 - V_2) + sCc_2(V_1 - Vout) - gm_1 Vin = 0$$

$$node\,b: \quad \frac{V_2}{r_2} + sCc_1(V_2 - V_1) + gm_2 V_1 = 0$$

$$node\,c: \quad \frac{Vout}{r_3} + sC_L Vout + sCc_2(Vout - V_1) - gm_3 V_2 = 0$$

By solving these equations, the exact solution for $\frac{Vout}{Vin}$ is given by:

$$\frac{Vout}{Vin} = \frac{-gm_1 gm_2 gm_3 r_1 r_2 r_3 \left(1 - \left(\frac{Cc_1}{g_{m2}} + \frac{Cc_2}{g_{m2} g_{m3} r_2}\right)s - \frac{Cc_1 Cc_2}{g_{m2} g_{m3}} s^2\right)}{Cc_1 Cc_2 C_L r_1 r_2 r_3 s^3 + \left(Cc_1 Cc_2 (r_1 r_2 + r_1 r_3 + r_2 r_3 + gm_2 r_1 r_2 r_3 - gm_3 r_1 r_2 r_3) + Cc_2 C_L r_1 r_3 + Cc_1 C_L (r_1 + r_2 + gm_2 r_1 r_2) r_3\right)s^2 + \left(Cc_2 r_1 + Cc_1 (r_1 + r_2 + gm_2 r_1 r_2) + Cc_2 r_3 + C_L r_3 + Cc_2 gm_2 gm_3 r_1 r_2 r_3\right)s + 1}$$

In the dominator,

The first order term is given by:

$$= \left(Cc_2 r_1 + Cc_1 (r_1 + r_2 + gm_2 r_1 r_2) + Cc_2 r_3 + C_L r_3 + Cc_2 gm_2 gm_3 r_1 r_2 r_3\right)$$
$$\approx Cc_2 gm_2 gm_3 r_1 r_2 r_3$$

The second order term is given by:

$$= \left(Cc_1Cc_2\left(r_1r_2 + r_1r_3 + r_2r_3 + gm_2r_1r_2r_3 - gm_3r_1r_2r_3\right) + Cc_2C_Lr_1r_3 + Cc_1C_L\left(r_1 + r_2 + gm_2r_1r_2\right)r_3\right)$$
$$\approx Cc_1Cc_2\left(gm_2r_1r_2r_3 - gm_3r_1r_2r_3\right) + Cc_1C_Lgm_2r_1r_2r_3$$

By using the approximated values, the transfer function is simplified as:

$$\frac{Vout}{Vin} = \frac{-gm_1gm_2gm_3r_1r_2r_3\left(1 - \left(\frac{Cc_1}{g_{m2}} + \frac{Cc_2}{g_{m2}g_{m3}r_2}\right)s - \frac{Cc_1Cc_2}{g_{m2}g_{m3}}s^2\right)}{Cc_1Cc_2C_Lr_1r_2r_3s^3 + \left(Cc_1Cc_2\left(gm_2r_1r_2r_3 - gm_3r_1r_2r_3\right) + Cc_1C_Lgm_2r_1r_2r_3\right)s^2 + Cc_2gm_2gm_3r_1r_2r_3s + 1}$$

By using the dominant pole approximation,

$$\text{The dominant pole} = -\frac{1}{\textit{first order term in the do}\min\textit{ator}} = -\frac{1}{Cc_2gm_2gm_3r_1r_2r_3}$$

Thus, the transfer function can be further simplified in the following format:

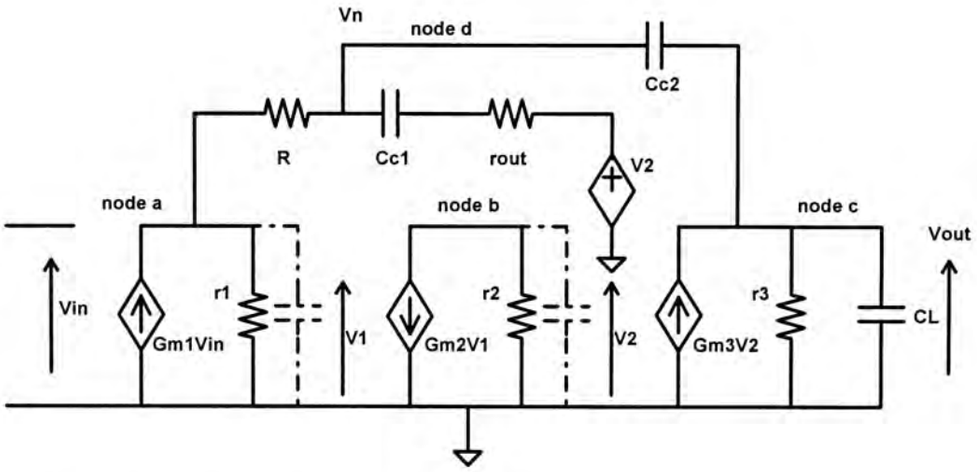
$$\frac{Vout}{Vin} = \frac{-gm_1gm_2gm_3r_1r_2r_3\left(1 - \left(\frac{Cc_1}{g_{m2}} + \frac{Cc_2}{g_{m2}g_{m3}r_2}\right)s - \frac{Cc_1Cc_2}{g_{m2}g_{m3}}s^2\right)}{\left(Cc_2gm_2gm_3r_1r_2r_3s + 1\right)\left(as^2 + bs + 1\right)}$$

With further factorization, the transfer function is then given by:

$$\frac{Vout}{Vin} \approx \frac{A_{DC}\left(1 - \left(\frac{Cc_1}{g_{m2}} + \frac{Cc_2}{g_{m2}g_{m3}r_2}\right)s - \frac{Cc_1Cc_2}{g_{m2}g_{m3}}s^2\right)}{\left(Cc_2gm_2gm_3r_1r_2r_3s + 1\right)\left(\frac{Cc_1C_L}{gm_2gm_3}s^2 + \left(\frac{Cc_1(Cc_2 + C_L)}{Cc_2gm_3} - \frac{Cc_1}{gm_2}\right)s + 1\right)}$$

where $A_{DC} = -gm_1gm_2gm_3r_1r_2r_3$

Appendix D: Derivation of transfer function for the amplifier using the proposed compensation scheme



By applying KCL, four equations are written down:

$$node\,a: \quad \frac{V_1}{r_1}+\frac{V_1-Vn}{R}-gm_1 Vin=0$$

$$node\,b: \quad \frac{V_2}{r_2}+gm_2 V_1=0$$

$$node\,c: \quad \frac{Vout}{r_3}+sC_L Vout+sCc_2(Vout-Vn)-gm_3 V_2=0$$

$$node\,d: \quad sCc_2(Vn-Vout)+\frac{Vn-V_2}{rout+\dfrac{1}{sCc_1}}-\frac{V_1-Vn}{R}=0$$

By solving these equations, the exact solution for $\frac{Vout}{Vin}$ is given by:

$$\frac{Vout}{Vin}=\frac{-gm_1gm_2gm_3r_1r_2r_3\left(1+\left(R(Cc_1+Cc_2)+Cc_1rout-\dfrac{Cc_2}{gm_2gm_3r_2}\right)s+Cc_1Cc_2R\left(\dfrac{1}{gm_3}+rout-\dfrac{rout}{gm_2gm_3Rr_2}\right)s^2\right)}{Cc_1Cc_2C_Lr_3rout(R+r_1)s^3+\left(\begin{array}{l}Cc_1Cc_2Rr_3+Cc_1C_LRr_3+Cc_2C_LRr_3+Cc_1Cc_2r_1r_3+Cc_1C_Lr_1r_3+Cc_2C_Lr_1r_3+\\Cc_1C_Lgm_2r_1r_2r_3+Cc_1Cc_2Rrout+Cc_1Cc_2r_1rout+Cc_1Cc_2r_3rout+Cc_1C_Lr_3rout+\\Cc_1Cc_2gm_2r_1r_2r_3(1+gm_3rout)\end{array}\right)s^2}$$
$$(Cc_1R+Cc_2R+Cc_1r_1+Cc_2r_1+Cc_1gm_2r_1r_2+Cc_2r_3+C_Lr_3+Cc_2gm_2gm_3r_1r_2r_3+Cc_1rout)s+1$$

In the dominator,

The first order term is given by:

$$= \left(Cc_1R + Cc_2R + Cc_1r_1 + Cc_2r_1 + Cc_1gm_2r_1r_2 + Cc_2r_3 + C_Lr_3 + Cc_2gm_2gm_3r_1r_2r_3 + Cc_1rout\right)$$
$$\approx Cc_2gm_2gm_3r_1r_2r_3$$

The second order term is given by:

$$= \begin{pmatrix} Cc_1Cc_2Rr_3 + Cc_1C_LRr_3 + Cc_2C_LRr_3 + Cc_1Cc_2r_1r_3 + Cc_1C_Lr_1r_3 + Cc_2C_Lr_1r_3 + \\ Cc_1C_Lgm_2r_1r_2r_3 + Cc_1Cc_2Rrout + Cc_1Cc_2r_1rout + Cc_1Cc_2r_3rout + Cc_1C_Lr_3rout + \\ Cc_1Cc_2gm_2r_1r_2r_3\left(1 + gm_3rout\right) \end{pmatrix}$$
$$\approx Cc_1C_Lgm_2r_1r_2r_3 + Cc_1Cc_2gm_2r_1r_2r_3\left(1 + gm_3rout\right)$$

By using the approximated values, the transfer function is simplified as:

$$\frac{Vout}{Vin} = \frac{-gm_1gm_2gm_3r_1r_2r_3\left(1 + \left(R\left(Cc_1 + Cc_2\right) + Cc_1rout - \frac{Cc_2}{gm_2gm_3r_2}\right)s + Cc_1Cc_2R\left(\frac{1}{gm_3} + rout - \frac{rout}{gm_2gm_3Rr_2}\right)s^2\right.}{Cc_1Cc_2C_Lr_3rout\left(R + r_1\right)s^3 + \left(Cc_1C_Lgm_2r_1r_2r_3 + Cc_1Cc_2gm_2r_1r_2r_3\left(1 + gm_3rout\right)\right)s^2 + Cc_2gm_2gm_3r_1r_2r_3s + 1}$$

By using the dominant pole approximation,

$$\text{The dominant pole} = -\frac{1}{first\ order\ term\ in\ the\ do\min ator} = -\frac{1}{Cc_2gm_2gm_3r_1r_2r_3}$$

Thus, the transfer function can be further simplified in the following format:

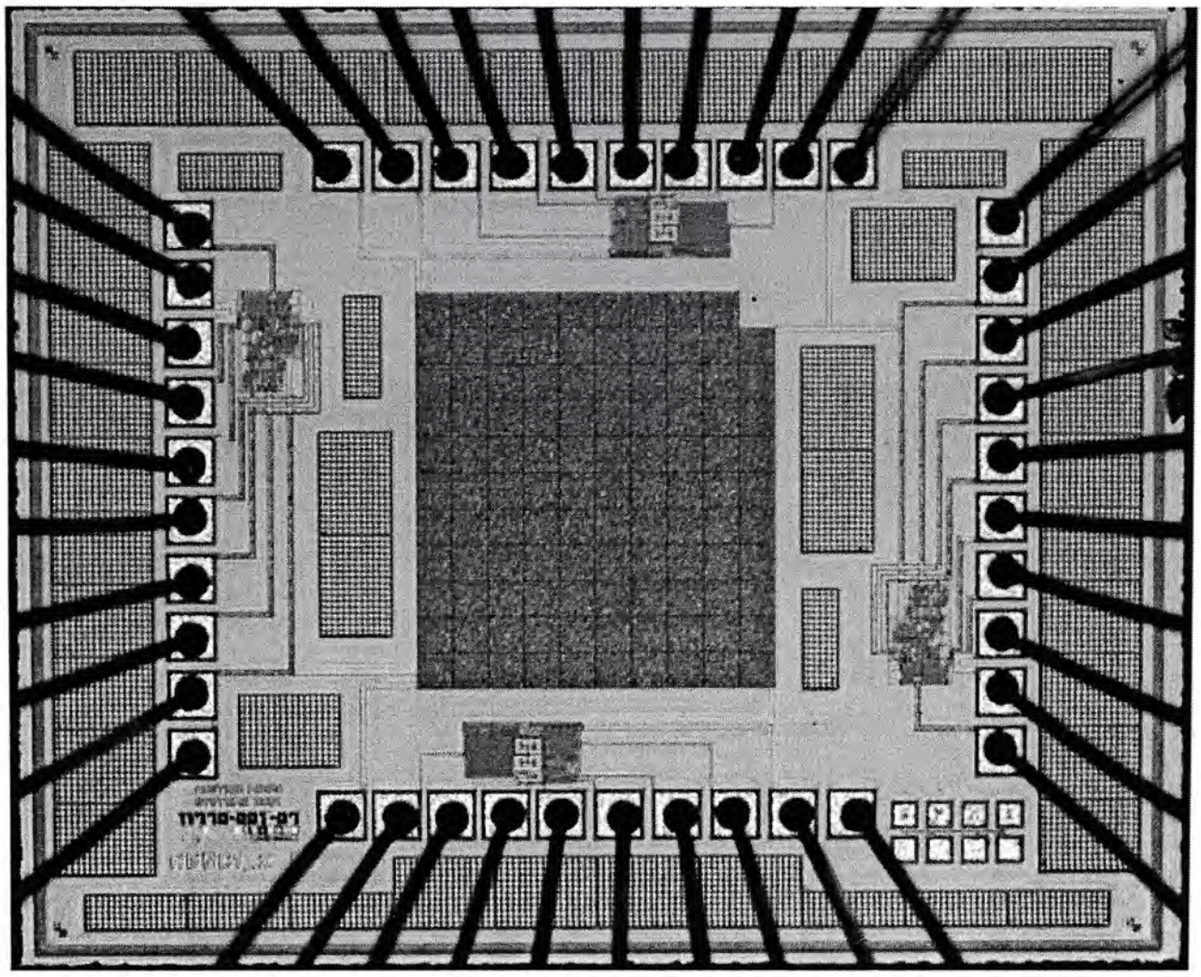
$$\frac{Vout}{Vin} = \frac{-gm_1gm_2gm_3r_1r_2r_3\left(1 + \left(R\left(Cc_1 + Cc_2\right) + Cc_1rout - \frac{Cc_2}{gm_2gm_3r_2}\right)s + Cc_1Cc_2R\left(\frac{1}{gm_3} + rout - \frac{rout}{gm_2gm_3Rr_2}\right)s^2\right.}{\left(Cc_2gm_2gm_3r_1r_2r_3s + 1\right)\left(as^2 + bs + 1\right)}$$

With further factorization, the transfer function is then given by:

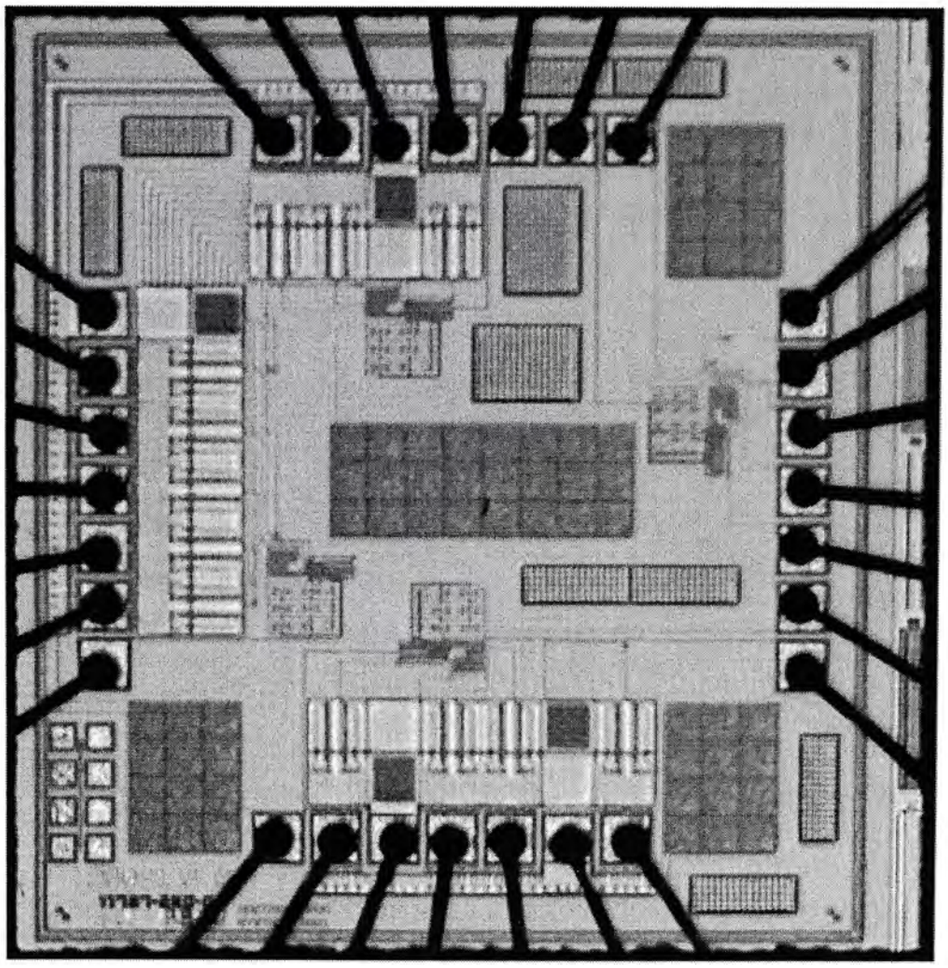
$$\frac{Vout}{Vin} \approx \frac{A_{DC}\left(1+\left(R(Cc_1+Cc_2)+Cc_1 rout-\frac{Cc_2}{gm_2 gm_3 r_2}\right)s+Cc_1 Cc_2 R\left(\frac{1}{gm_3}+rout\right)s^2\right)}{(Cc_2 gm_2 gm_3 r_1 r_2 r_3 s+1)\left(\frac{rout}{r_2}\frac{Cc_1 C_L}{gm_2 gm_3}s^2+\left(\frac{Cc_1 C_L}{Cc_2 gm_3}+\frac{Cc_1(1+gm_3 rout)}{gm_3}\right)s+1\right)}$$

where $A_{DC} = -gm_1 gm_2 gm_3 r_1 r_2 r_3$

Appendix E: Microphotography of the current feedback operational amplifier



Appendix F: Microphotography of the three-stage voltage feedback operational amplifier



PUBLICATION

K. P. Ho, C. F. Chan, C. S. Choy and K. P. Pun, A CMOS Current Feedback Operational Amplifier with Active Current Mode Compensation, 2002 IEEE International Symposium on Circuits and Systems.