Design and Implementation of Fully Integrated Low-Voltage Low-Noise CMOS VCO

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Abstract

Voltage-controlled oscillators (VCOs) are critical components for signal generation in RF transceivers. Recently, there has been considerable interest in monolithic integration of inductance-capacitance (LC) tank oscillators for highly integrated RF transceivers. Technologies such as Si CMOS and Si/SiGe BiCMOS are of interest in light of the potential for integration with digital functions. However, in Si technologies, the Q of the inductor is usually the limiting factor. Traditionally, inductors have been incorporated as discrete components located off-chip, often as small surface-mount parts. Alternatively, some VCO designs have utilized bonding wires as hybrid inductors. While bonding wires can offer a relatively high Q, they also suffer from large variations in inductance value.

In this thesis, the design and implementation of low phase noise fully integrated CMOS LC differential voltage-controlled oscillators is presented. The new circuit topology offers: (1) Resonator with enhanced quality factor; and (2) Reduction of noise up-conversion coefficient. The proposed design is verified experimentally by the fabrication of 1.5 GHz LC VCO circuits using 0.6 micron standard CMOS technology. The phase noise and frequency tuning performances of the oscillators are also shown for comparison.

摘要

在無線電收發機內，電壓控制振盪器是其中一個較爲重要的部分。近年，有關把電感電容差分電壓控制振盪器整合於單晶片無線電收發機上的研究，引起了極大關注。藉著利用互補金屬氧化物半導體或雙極互補金屬氧化物半導體技術，更可把振盪器與數位電路結合在一單晶片上。但是，在矽技術當中，電感器的 Q 值往往是一個限制。

本論文將會講述有關如何利用嶄新的共振器結構，設計出低相位雜訊的電感電容差分電壓控制振盪器。這技術不但能提高共振器的 Q 值，並且能減少振盪器的嘈音上載指數。

本論文所提出的電感電容差分電壓控制振盪器設計，是透過標準零點六微米互補金屬氧化物半導體技術的研製下，電路運作在一千五百兆頻，並在相位雜訊和頻率調整的性能上作出分析及比較。

Acknowledgement

I would like to express my sincere thanks to my supervisor, Prof. K. K. Cheng, for his generous, guidance and continued support throughout my research study. I also thank my family for their love and encouragement. My associate examiner, Prof. K. L. Wu, and my colleagues have also helped in many ways. I would like to single out Mr. C. W. Fan, Ms. W. Y. Leung, Mr. P. Y. Lin for their assistance and helpful suggestions.

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1.1 Motivation

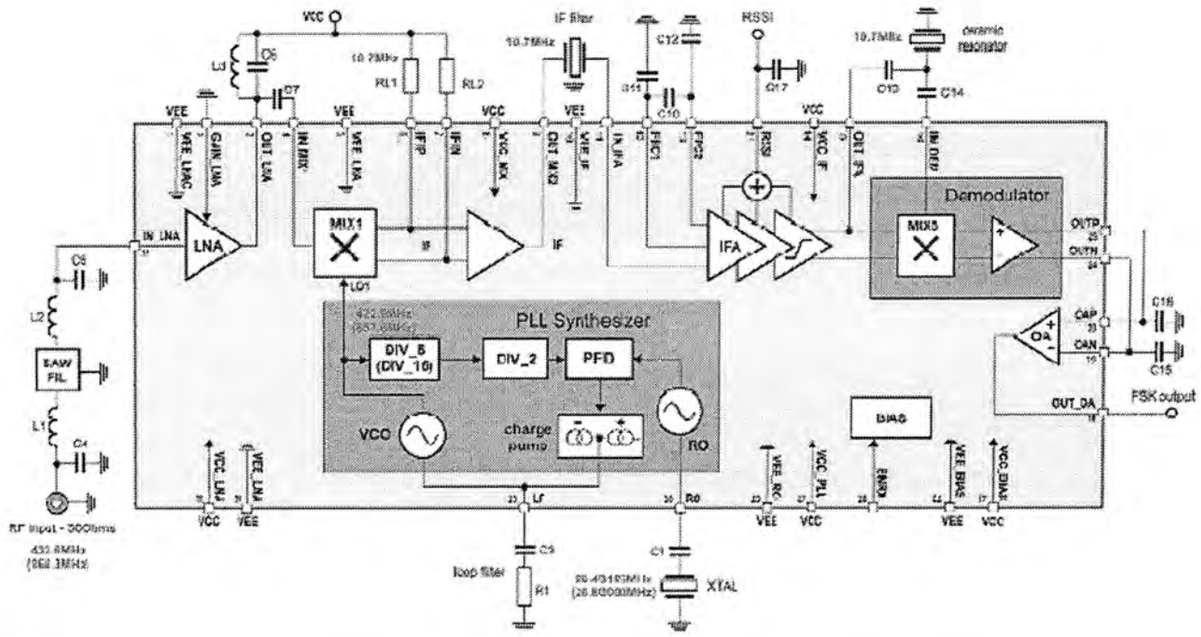


Figure 1.1 Block diagram of typical RF receiver

Oscillators are used at various places in an RF transceiver system. Figure 1.1 illustrates this with a block diagram of a superhet receiver. The local oscillator (LO) provides the mixer with a signal which is equal, in frequency, to the difference of the RF carrier and the intermediate frequency (IF). The LO is part of a phase locked loop (PLL), and uses a crystal oscillator as reference.

The LO in RF transceivers is often implemented using an LC oscillator with lumped LC resonator which can be on-chip or off-chip. Piezoelectric material is used in SAW (Surface Acoustic Wave) oscillators, which offers excellent spectral purity and also very good long-term frequency stability. Another example of a very stable resonator is a dielectric resonator (DR).

Recently, there has been considerable interest in monolithic integration of LC oscillators for highly integrated RF transceivers. Technologies such as Silicon CMOS and BiCMOS are of interest in light of the potential for integration with digital functions. In BiCMOS technologies, the bipolar device co-exists along with the MOS device on the same Si substrate. There are obvious advantages here: Since the RF system is usually implemented using bipolar transistors and the baseband subsystem is a complex digital CMOS system, the BiCMOS technology allows for the complete integration of a mobile communication system on a single chip. Disadvantages of BiCMOS technologies are the increased process cost compared to a simple CMOS process. Recent advances in CMOS technologies and in particular the continuous shrinkage in transistors' channel length, makes the MOS device comparable to the bipolar transistor in terms of speed of operation.

It is well known that the output power spectrum of an oscillator features a peak at oscillation frequency ω_o and tails in both sidebands, decreasing as the frequency offset α from ω_o. Generally speaking, they are ascribed to the presence of noise sources in the circuit, and they are more precisely referred to as the oscillator phase noise.

The noise performance of an oscillator are quantitatively assessed by defining a suitable signal to noise ratio, i.e. the single sideband-to-carrier ratio (SSCR). This figure is the ratio between the output noise power in a 1-Hz bandwidth at the frequency offset α from the carrier and the power of the carrier, and is usually expressed in dBc/Hz, i.e., decibels relative to the carrier. For instance the GSM standard asks for a SSCR of about –115dBc/Hz at 100kHz form the carrier frequency.

In realizing microwave oscillators, phase noise performance is usually the main concern. Suppose the receiver tunes to a weak desired signal in the presence of a strong interferer in an adjacent channel, as shown in Figure 1.2. If the local oscillator has large phase noise, the interfering signal will also be down-converted to almost the same intermediate frequency. The resulting interference will significantly degrade

the dynamic range of the receiver. Note that a high Q resonator strongly reduces both the phase noise and power consumption of an oscillator.

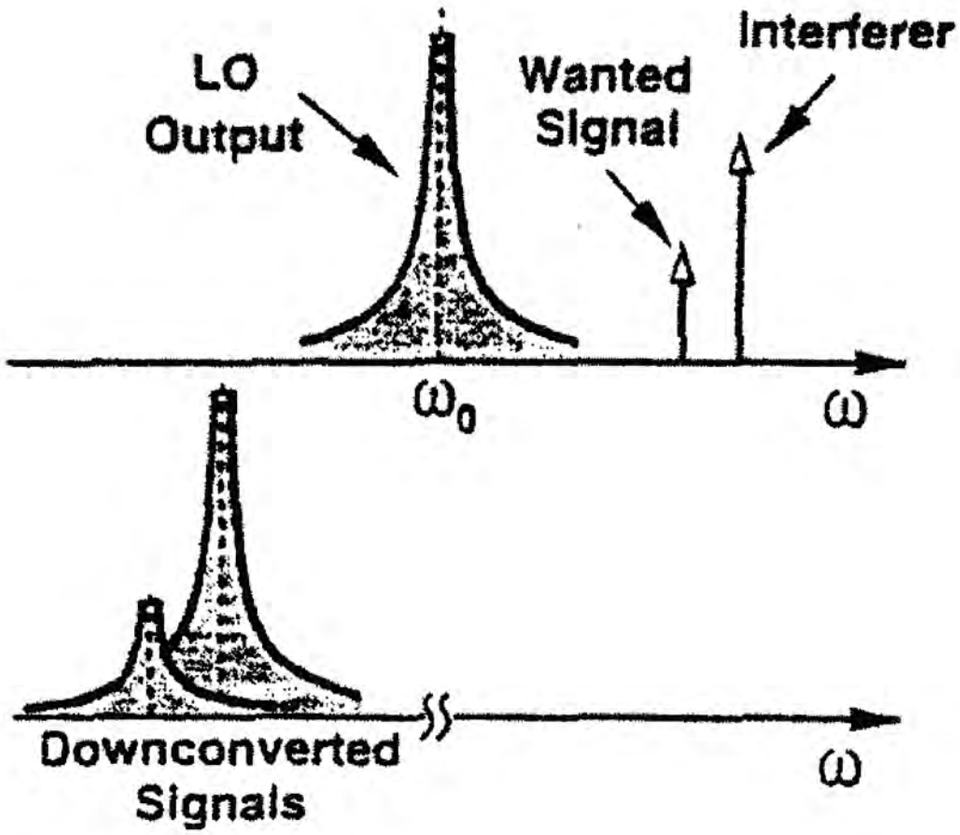


Figure 1.2 Reciprocal Mixing

Conventionally, Resonant tanks in RF oscillators are usually implemented with high-quality discrete components located off-chip, often as small surface-mount parts. Alternatively, some oscillators have employed bonding wires as hybrid inductors. While bonding wires can offer a relatively high Q, they also suffer from large variation in inductance value. Monolithic inductors fabricated as single planar spirals

are widely used on GaAs substrates with Qs in the range of 20-40. However, inductor Qs on standard Si substrates are much lower. The L of a monolithic inductor is defined solely by its geometry. Since modern photolithographic processes provide extremely tight geometric tolerances, monolithic inductors have very small variations in their performance. This is the main reason for the widespread efforts in the IC community to improve the quality of fully integrated inductors in silicon, especially in the last few years.

In addition, flicker noise is upconverted to $1/f^3$ - shaped phase noise close to the carrier. When the oscillator is not carefully designed, flicker noise can deteriorate the phase noise at higher offset frequencies important for communication systems, e.g., 600kHz, by several dB. This is especially true in MOS VCO's because of the higher flicker noise of MOS transistors compared to bipolar transistors. It has been shown elsewhere that upconversion is highly dependent on the symmetry of the output waveform [21].

The aim of this work is to clarify how the noise sources of the electronic devices contribute to the output phase noise of the oscillator, thus giving some guidelines for the circuit optimization.

1.2 Objective

This research work is to investigate, both theoretically and experimentally, the design and optimization of low phase noise voltage-controlled oscillators fabricated using standard CMOS technology. New circuit topology is proposed which offers: (1) Resonator with enhanced quality factor; and (2) Reduction of noise up-conversion factor. This thesis is divided into seven chapters. Chapter 2 covers the background theories of oscillator design. In chapter 3, we introduce the fundamentals of the nonlinear analysis of the noise and we show that the nonlinear behavior of the transconductor causes a folding of the wide-band noise sources like the thermal noise of the transistor. Moreover, noise reduction techniques, particularly for the design of differential LC VCOs, are presented. Chapter 4 describes the CMOS technology adopted and addresses the issues of device modeling. Chapter 5 details the design and implementation of CMOS VCO circuits. Measured results such as phase noise and tuning characteristics are presented in chapter 6. Finally, chapter 7 concludes this thesis and provides recommendation for future work.

Chapter 2 Theory of Oscillators

2.1 Oscillator Design

This chapter deals with the analysis and design of oscillators, or more specifically, the voltage controlled oscillators (VCOs). Beginning with a general study of oscillation in feedback systems, we introduce the LC differential oscillators along with methods of varying the frequency of oscillation.

2.1.1 Loop-Gain Method

An oscillator is considered as an amplifier with feedback in the loop gain method. Figure 2.1 shows the block diagram representation which consists of an ideal amplifier with gain A, in cascaded with frequency selective networks characterized by transfer function $H_1(f)$ and $H_2(f)$.

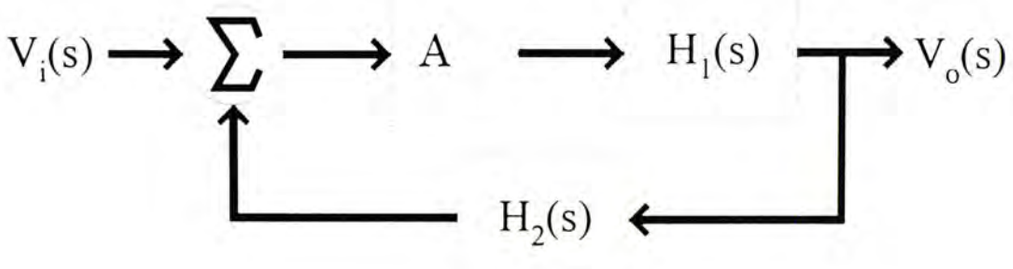


Figure 2.1 Block diagram of an amplifier with feedback

The overall transfer function of the feedback amplifier is given by equation 2.3.

$$\frac{V_o(s)}{V_i(s)} = \frac{A \times H_1(s)}{1 - A \times H_1(s) \times H_2(s)} \tag{2.3}$$

An oscillator is obtained when an output signal appears in the absence of an external input signal. This is possible only if the Barkhausen criteria[1] is satisfied:

$$\begin{aligned} &| A \times H_1(j\omega) \times H_2(j\omega) | = 1 \\ &Phase\ [A \times H_1(j\omega) \times H_2(j\omega)] = 0 \end{aligned} \tag{2.4}$$

It is the condition for steady state oscillation since it states that, at the frequency of oscillation, the signal must go around the loop with no attenuation and zero phase shift. In practice, due to the component tolerances and the non-linearity of the amplifier, the loop-gain value of the circuit must be greater than unity for startup of oscillation. Steady-state oscillation is reached when the signal amplitude is self-limited by the nonlinear nature of active devices. At this point, the loop-gain value equals unity and the Barkhausen criteria is met.

2.1.2 Negative Resistance-Conductance Method

At microwave frequencies, Gunn diodes and IMPATT diodes are examples of device which exhibit negative resistance. Since a positive resistance dissipates power, it is reasonable to assume that a device which exhibits negative resistance could be

used to generate an RF signal. With a potentially unstable transistor, a negative resistance can effectively be created by terminating the device with an impedance designed to drive it into the unstable region[1]. When a resonator is connected to a network exhibiting negative resistance, oscillation builds up until limiting reduces the net resistance to zero. Referring to Figure 2.2, for oscillation to occur, we have

$$R_L + R_{in} = 0 \text{ and } X_L + X_{in} = 0 \tag{2.5}$$

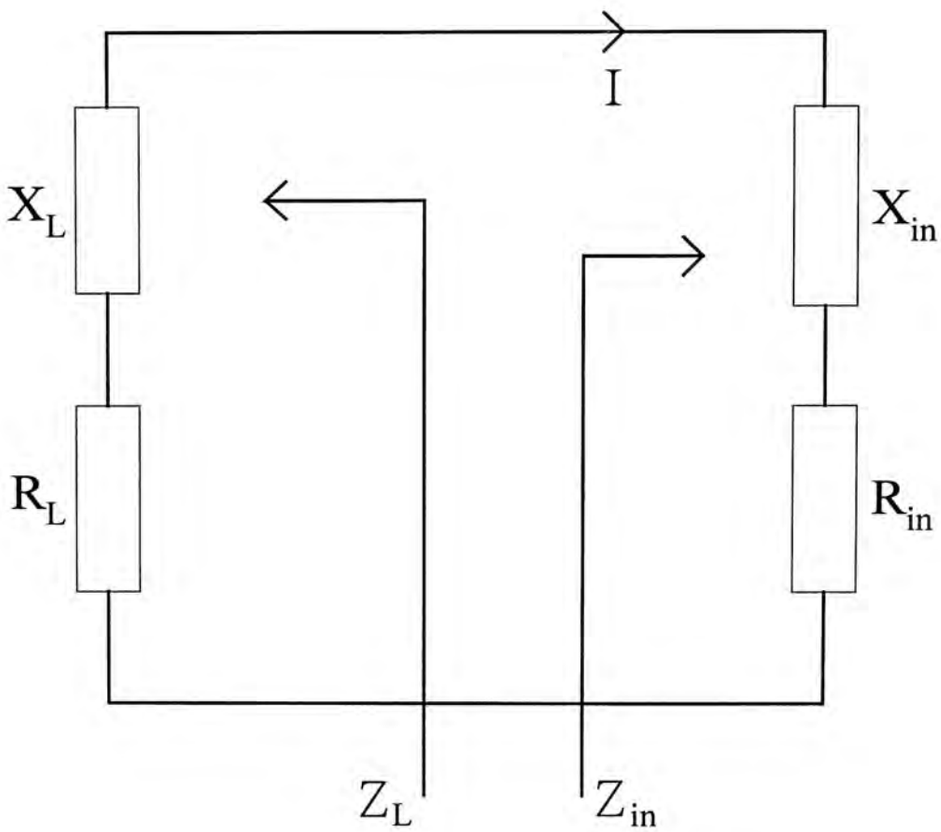


Figure 2.2 Negative Resistance Circuit

In practice a value of $R_L = |R_{in} / 3|$ is commonly used. During power on, any transient excitation or noise causes oscillation to build at frequency ω_o. As the

current increases, the value of R_{in} becomes less negative until $R_L + R_{in} = 0$. The oscillator is now operating in a stable state.

2.1.3 Crossed-Coupled Oscillator

CMOS oscillators in today's technology are typically implemented as "ring oscillators" or "LC oscillators". As ring oscillators are very sensitive to noise in the switching thresholds and charging currents, it is a common practice to use LC oscillators for higher frequency stability and spectral purity. MOS differential voltage-controlled oscillator with integrated LC resonator[13], as shown in figure 2.4, are most widely used integrated oscillators in silicon ICs.

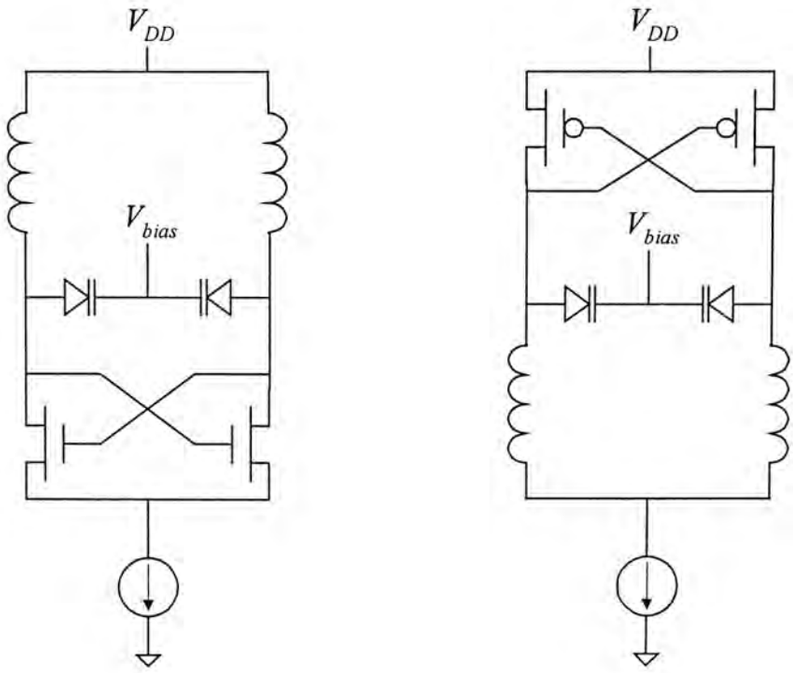


Figure 2.4 (a) NMOS VCO, (b) PMOS VCO

The above VCO use cross-coupled FETs to generate negative resistance so as to compensate for the loss of the LC tank and start-up oscillation. The current source at the bottom is used for controlling the current flowing through the cross-coupled FETs. A pair of inductors and varactors constitutes the LC tank. V_{bias} is used to control the biasing voltage of varactors, producing different capacitance value, and therefore to tune the oscillating frequency of the VCO circuits.

Consider another type of oscillator design, as shown in Figure 2.5, where an LC tank operates as the load. At resonance, the voltage gain should be equal to $-g_{m1}R_p$ and $jC_p\omega=1/(jL_p\omega)$. When the circuit is biased at a drain current I_1 and small sinusoidal voltage at the resonance frequency is applied to the input. V_{out} should be an inverted sinusoid with an average value near V_{DD} [31].

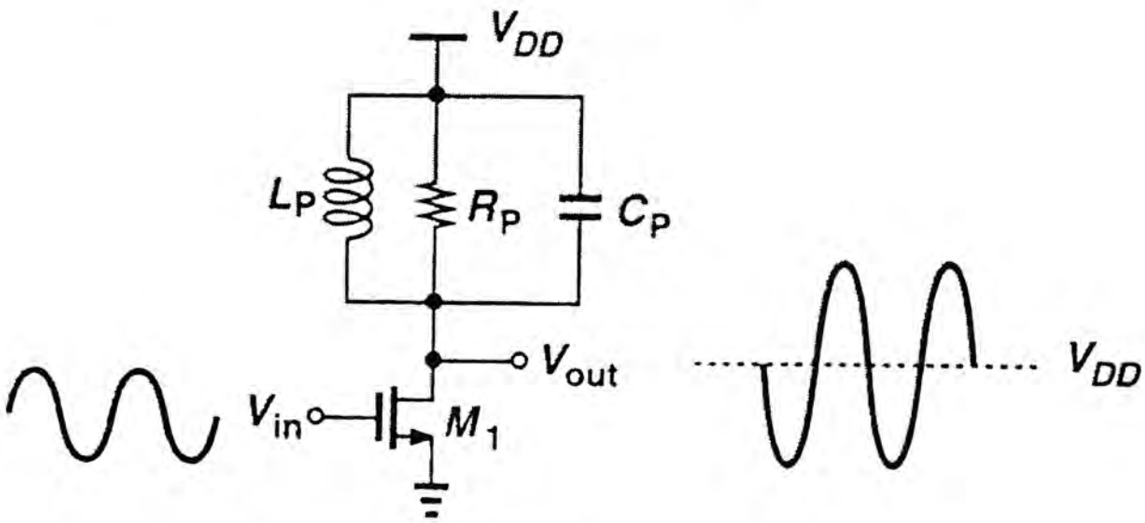


Figure 2.5 Common-source configuration with parallel tank as load

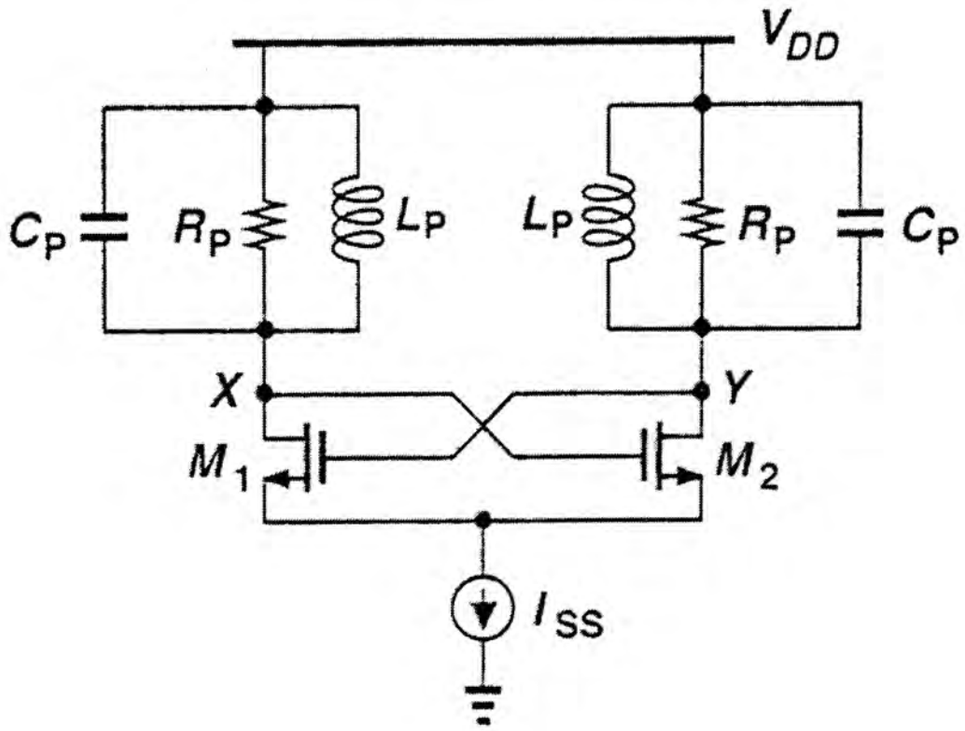


Figure 2.6 Two common-source configuration connected with positive feedback loop

Suppose we place two circuit of Figure 2.5 in a cascade, as shown in Figure 2.6 [31]. Note that when $(-g_{m1}R_p) \times (-g_{m2}R_p) > 1$, then oscillation will take place. The output waveform of V_X and V_Y are differential in nature. Furthermore, at resonance, the total phase shift around the loop is zero because each stage contributes zero frequency –dependent phase shift, as illustrated in Figure 2.7.

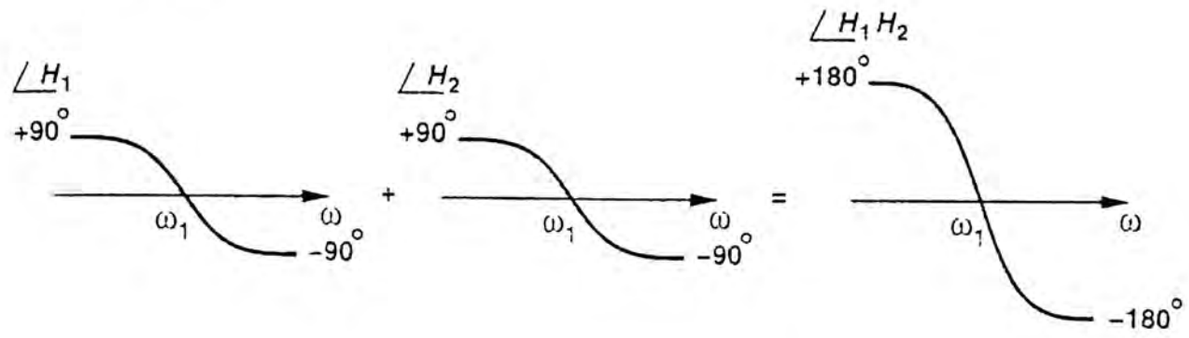


Figure 2.7 Phase characteristics of the circuit shown in Figure 2.5

When we apply the supply voltage V_{DD} to the cross-coupled oscillator, then $V_X = V_Y = V_{DD}$, Two transistors share the tail current I_{SS} equally. When $(-g_{m1}R_p) \times (-g_{m2}R_p) > 1$, noise components at the resonance frequency are continually amplified by M_1 and M_2, allowing the oscillation to grow. The drain currents of both transistors vary according to the instantaneous value of $V_X - V_Y$[31].

The oscillation amplitude will continue to grow until the voltage or current gain drops at the peaks. The voltage gain waveforms vary between zero and $V_X - V_Y$ whereas current gain waveforms vary between zero and I_{SS}, as shown in Figure 2.8.

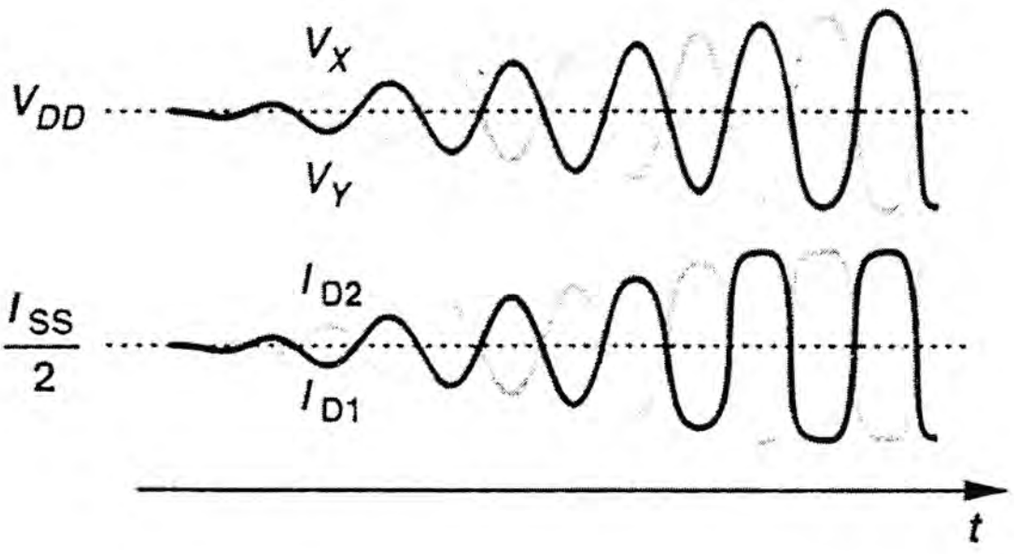


Figure 2.8 Transient response of V_X, V_Y, I_{D1} and I_{D2}

In analyzing this kind of oscillator, we can also merge two tanks into one, as shown in Figure 2.9. Note that the cross-coupled pair should provide a negative resistance of $-R_P$ between nodes X and Y to enable oscillation. This resistance equals

to $-2 / g_m$ [31]. That means it is necessary for $R_P \geq 1 / g_m$ so as to start oscillation.

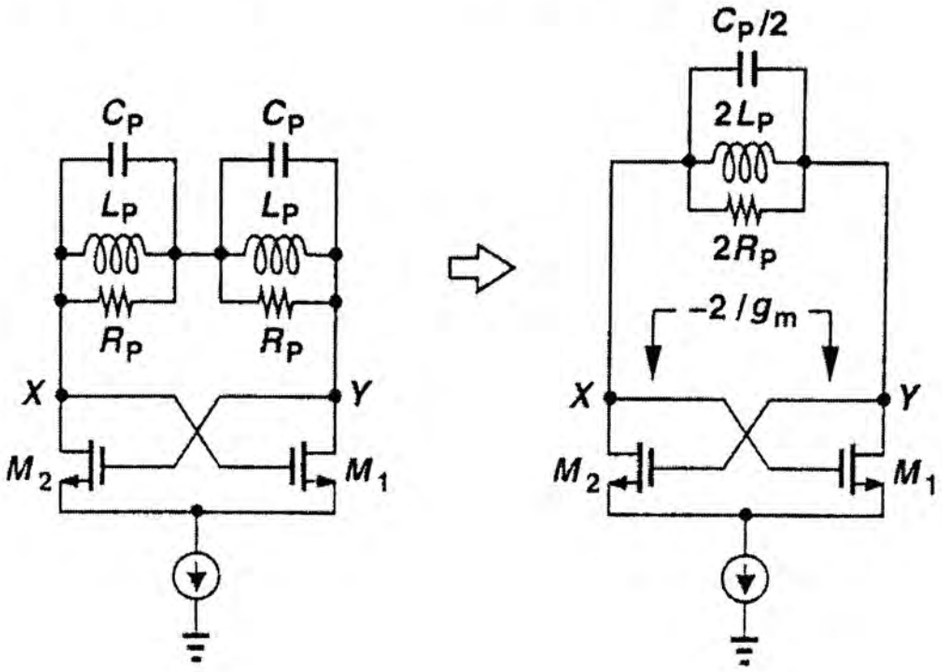


Figure 2.9 Equivalent circuit of Figure 2.6

Chapter 3 Noise Theory of Oscillators

The importance of oscillator phase noise in RF and other communication circuits has made it one of the most extensively studied subjects in electronics. Journal papers on the subject can be found from each of the last six decades. Experimentally, the qualitative behavior of phase noise has been well known. An oscillator's output power spectrum consists of a peak at the carrier frequency surrounded by a noise skirt symmetrical to the carrier frequency. Irrespective of the exact implementation, the noise skirt has the following characteristics:

- The noise spectral density is inversely proportional to the frequency offset from the carrier, except very close to the carrier frequency, where the influence of up-converted flicker noise dominates or the presence of the strong carrier begins to limit the measurement accuracy.

- The same noise manifests itself in the time domain as jitter around the oscillation's zero-crossing points, which can only be caused by noise in the phase of the oscillation rather than that super-imposed on its amplitude. Oscillator noise is therefore usually referred to as phase noise.

Today, RF oscillators are implemented with high-quality inductors and capacitors outside the chip containing the active devices. This is the main reason for the wide-spread efforts in the integrated circuit community to improve the quality of fully integrated inductors on silicon, especially in the last few years. Despite the avalanche of research papers, the quality factor Q of on-chip inductors at 1GHz has hardly improved by a factor of two (from $Q \leq 3$ to $Q \leq 6$) in the last 10 years. Reported phase noise level, however, vary by as much as 20dB at 100kHz offset. This underlines the fact that other factors than the Q of the tank also affect the oscillator phase noise strongly.

In this chapter, we will review typical existing phase noise models of oscillators. Finally, phase noise reduction techniques based on a new oscillator circuit topology is presented.

3.1 Origin of Noise Sources

3.1.1 Flicker Noise

One of the sources of noise associated with solid-state devices, the amplitude of which varies inversely with frequency. It is also referred to as 1/f noise. The mathematical expression for flicker noise is [25],

$$\frac{\overline{i_n^2}}{\Delta f} = \Delta f \times \frac{Kg_m^2}{fWLC_{ox}^2} \tag{3.1}$$

where

K is Flicker noise parameter,

L and W are the effective channel length and width respectively,

g_m *is the transconductance of active device,*

C_{ox} *is the intrinsic gate oxide capacitance of the active device.*

For lower flicker noise generation, a large MOSFET device should be adopted since the gate capacitance of MOSFET smoothens the fluctuations in channel charge. The main drawback is the increased parasitic capacitance as the size of the device is enlarged.

3.1.2 Thermal Noise

In CMOS-type oscillator, the dominant thermal noise is contributed from the gate channel of FETs [25]. There are two mathematical expressions for channel thermal noise:

For long-channel device,

$$\frac{\overline{i_{nd}^2}}{\Delta f} = 4kT\,\gamma\,g_m \tag{3.2}$$

For short-channel device,

$$\frac{\overline{i_{nd}^2}}{\Delta f} = 4kT\,\frac{I_{bias}}{E_{sat}L}$$

where

k = Boltzman Constant

T = temperature in Kelvin

γ = 0.67 (long-channel devices)
= 2.5 (short-channel devices)

I_{bias} = drain current of the FET

E_{sat} = field strength

3.1.3 Noise Model of Varactor

Since a varactor can be modeled as a capacitor and a resistor connected in series [26], hence, the noise power can be described by,

$$\frac{\overline{i_n^2}}{\Delta f} = \frac{4kT}{R_{\text{var}}} \tag{3.3}$$

where R_{var} equals the effective resistance in series with the capacitor.

3.1.4 Noise Model of Spiral Inductor

Spiral inductor can also be modeled as an inductor and a resistor connected in series[26] since the metal track of the spiral inductor introduces ohmic loss. The expression is shown below:

$$\frac{\overline{i_n^2}}{\Delta f} = \frac{4kT}{R_L} \tag{3.4}$$

where R_L equals the equivalent series resistance of the spiral inductor.

3.2 Derivation of Resonator

The most common definitions of quality factor Q are:

1. $Q = 2\pi \dfrac{\text{Energy Stored}}{\text{Energy Dissipated per Cycle}}$

2. $Q = \dfrac{\omega_o}{\Delta\omega}$

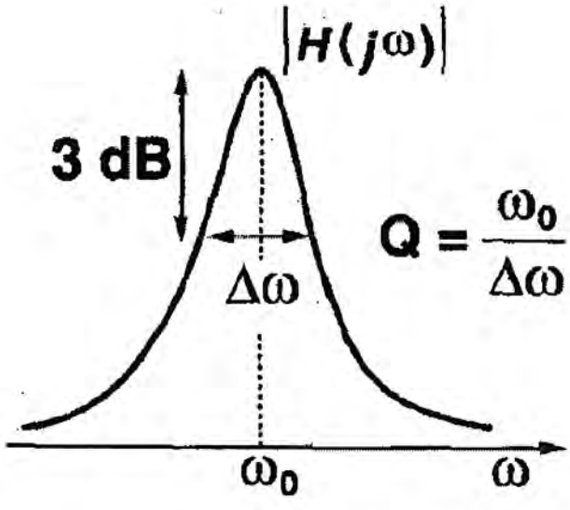


Figure 3.1 A definition of Q

3. For a simple LC shunt circuit (Figure 3.2):

$$Q = \frac{\omega_o}{2}\frac{\partial \Phi}{\partial \omega},$$

where ω_o is the resonant frequency and Φ denotes the phase response of the circuit admittance.

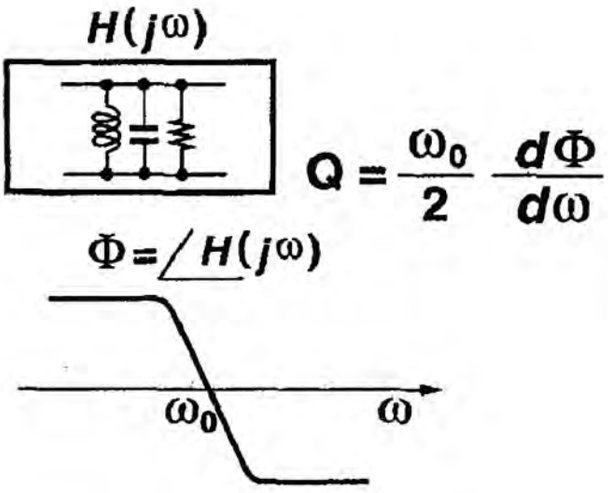
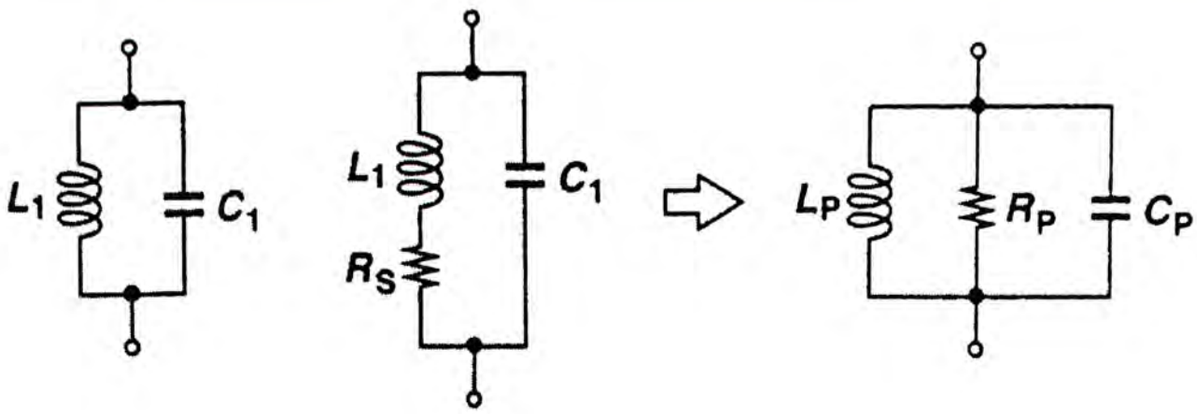


Figure 3.2 Another definition of Q

As shown in Figure 3.3(a), an inductor L_1 placed in parallel with a capacitor C_1 resonates at a frequency $\omega_{res} = 1/\sqrt{L_1 C_1}$. We say the circuit has an infinite quality factor, Q. In practice, inductors (and capacitors) suffer from resistive components. For example, the series resistance of the metal wire used in the inductor can be modeled as shown in Fig. 3.3(b). We define the Q of the inductor as $L_1\omega / R_S$. For this circuit, the reader can show that the equivalent impedance is given by

$$\left|Z_{eq}(s = j\omega)\right|^2 = \frac{R_S^2 + L_1^2\omega^2}{(1 - L_1 C_1 \omega^2)^2 + R_S^2 C_1^2 \omega^2} \tag{3.5}$$



(a) (b) (c)

Figure 3.3 (a) Ideal, (b) realistic LC tanks; and (c) equivalent circuit

That is, the impedance does not go to infinity at any s = jω. We say the circuit has a finite Q. For a narrow frequency range, it is possible to convert the circuit to the parallel configuration of Figure 3.3(c). Recall that $L_1\omega / R_S = Q$, a value typically greater than 3 for monolithic inductors. Thus, we have

$$L_p \approx L_1 \tag{3.6}$$

$$R_p \approx \frac{L_1^2\omega^2}{R_S} \approx Q^2 R_S \tag{3.7}$$

The insight gained from the parallel combination is that at $\omega_1 = 1/\sqrt{L_p C_p}$, the tank reduces to a simple resistor; i.e., the phase difference between the voltage and current of the tank drops to zero. Note that the behavior is inductive for $\omega < \omega_1$ and capacitive for $\omega > \omega_1$.

The Q defined in the preceding sections is a characteristic of the resonant circuit

itself, in the absence of any loading effects caused by external circuitry, and so is called the unloaded Q. In practice, however, a resonant circuit is invariably coupled to other circuitry, which will always have the effect of lowering the overall Q of the circuit.

3.3 Oscillator Phase Noise Model

Any oscillator has noise sidebands at frequencies f_m offset from the carrier frequency. For increasing distance from the carrier the noise sidebands decay ultimately at 6dB/octave into the noise floor, as shown in Figure 3.4.

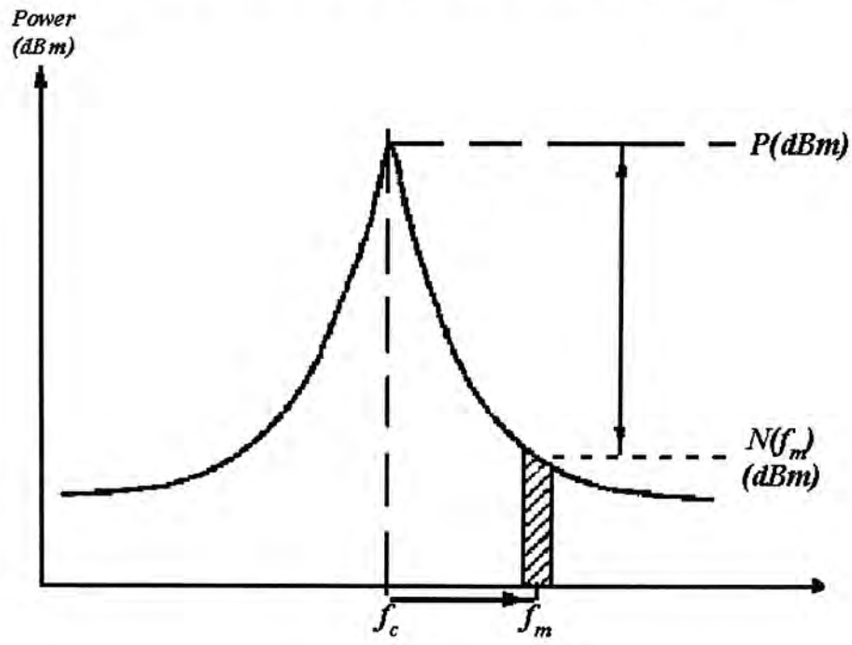


Figure 3.4 Single resonator oscillator spectrum

Thermal noise causes fluctuations in both amplitude and phase, usually denoted as AM noise and PM noise. However, all practical oscillators employ same form of amplitude limiting, as noted previously. Consequently, amplitude variations in real

oscillators are attenuated and phase fluctuations dominate. Additionally, we are often more interested in how large this noise in relative to the carrier, rather than its absolute value:

$$L\{\Delta f\} = \frac{\text{Noise Power at } \Delta f \text{ offset with 1Hz Bandwidth}}{\text{Carrier Power}} \tag{3.8}$$

3.3.1 Leeson's Model

The most common phase noise model is proposed by Leeson [20]:

$$L(\Delta f) = \frac{1}{2}\frac{FkT}{C}\left[\frac{1}{4Q^2}\left(\frac{f_o}{\Delta f}\right)^2 + 1\right] \times \left(\frac{f_c}{\Delta f} + 1\right) \tag{3.9}$$

where

Q is the quality factor of the resonator

F is an empirical parameter of noise figure

C is the output power of the oscillator

f_o is the oscillation frequency

Δf is the offset frequency

f_c is the flicker noise corner of the oscillator

Equation (3.9) shows that the phase noise at a given offset improves as both the

carrier power and Q increase. Leeson's formula also includes the introduction of a factor F to account for the increased noise in the $1/\Delta f^2$ region, an extra term of unity(inside the brackets) to account for the noise floor, and a multiplicative factor to provide a $1/\Delta f^3$ behavior at small offset frequencies(Figure 3.5).

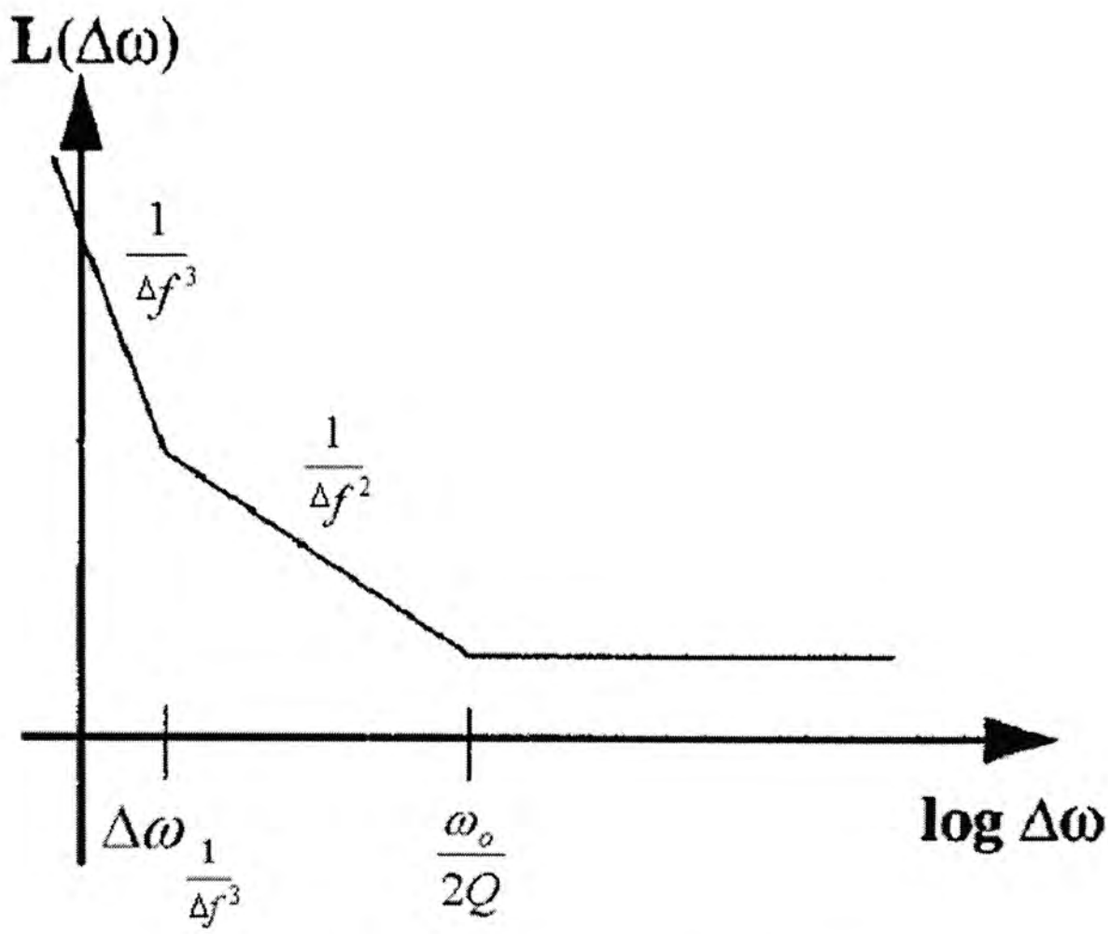


Figure 3.5 Phase Noise versus offset frequency

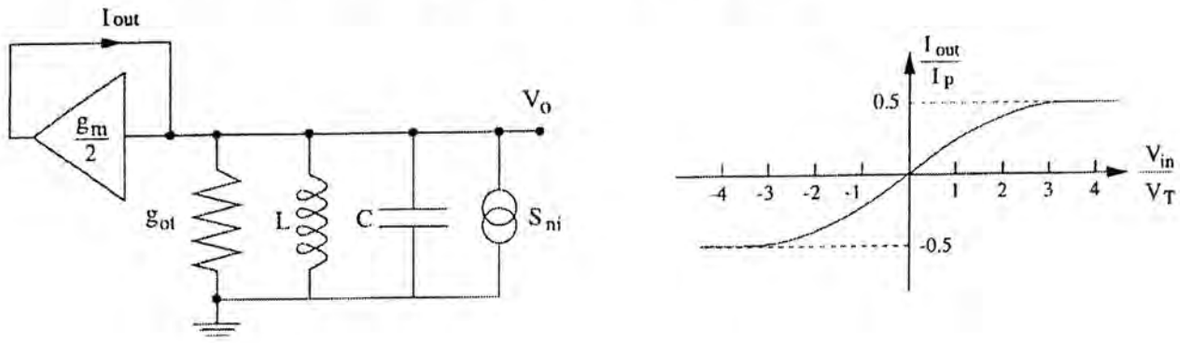
3.3.2 J. Cranincks and M. Steyaert Noise Model [25]

J. Cranincks and M. Steyaert have developed a similar model for predicting the phase noise of oscillators. The expression is given by:

$$L\{\Delta f\} = 10\log\left\{\frac{kTR_{eff}[1+F]}{V_{\max}^2/2}\left(\frac{f_o}{\Delta f}\right)^2\right\} \tag{3.10}$$

F is a term that includes the excess noise of the oscillator's negative resistance, V_{max} is the differential output amplitude, and R_{eff} is the LC-tank's effective resistance, which is mainly determined by the inductor. The inductor's series resistance must be reduced so as to lower the phase noise as well as the power consumption. For mass production, fully integrated spiral inductors on silicon substrates without extra post-processing steps are required. The quality of these inductors is limited by the parasitic effects, such as skin effect, eddy currents in the substrate.

3.3.3 Non-linear Analysis of Phase Noise



(a) (b)

Figure 3.6 (a) Single-ended equivalent circuit with the current noise source accounting for the additive noise;
(b) The figure shows the I-V characteristics of the transconductor.

Figure 3.6 shows a single-ended equivalent of the oscillator. It is well known that in the small signal regime the cross-coupled pair features a negative resistance equal to $-2 / g_m$, where g_m is the transconductance of each transistor. The figure also shows the characteristic of the transconductor with the input and the output variables normalized to the thermal voltage V_T and to the tail current I_P, respectively. We denote with $\omega_o = 1/\sqrt{LC}$ the central frequency of the bandpass loop filter, while the losses are represented by the equivalent conductance g_{ot} in parallel to the tank.

The self-sustaining oscillation occurs for $\omega = \omega_o$, and if the differential pair is driven well beyond the input linear range, the transconductor output current resembles a square wave at ω_o. However, the harmonic component at ω_o is the only component of the signal passing through the loop filter. If Q is high enough all the

other harmonic components are cut-off. Therefore the transconductor transfer may be quantitatively characterized by introducing an effective transconductance g_{meff}, given by the ratio between the output current component at ω_o and the input voltage amplitude at the same frequency. If the amplitude of the voltage signal is small, the effective transconductance is coincident with the small signal parameter $g_m / 2 = I_p / 4V_T$. As the input amplitude A_o increases beyond the input linear range, the effective transconductance decreases below $g_m / 2$ and in the hard limiting regime, when the current output waveform is a square wave, it approaches the value $g_{meff} = 2I_p / \pi A_o$.

Finally, we remind that the oscillation is self-sustaining when the loop gain at ω_o is equal to one, i.e., $g_{meff} / g_{ot} = 1$. This means that the losses, g_{ot}, are perfectly balanced by the transconductance of the positively fed back transconductor and the tank reduces to a parallel connection between the inductor and the capacitor.

The noise spectral density of the output voltage, S_{nv}, is usually estimated by representing the overall circuit noise with a current noise source S_{ni} in parallel to the tank. This noise is usually referred to as additive noise. The current noise generator forces an impedance $Z(\omega)$ given by the parallel of L and C. By taking α as the frequency offset from ω_o, for $\alpha \ll \omega_o$, we may write

$$\left|Z(\omega_o \pm \alpha)\right|^2 \approx \frac{1}{(2\alpha C)^2} \tag{3.11}$$

Thus,

$$S_{nv}(\alpha) = \frac{S_{ni}}{(2\alpha C)^2} = \frac{1}{4}\frac{S_{ni}}{g_{ot}C}\frac{\omega_o}{Q}\frac{1}{\alpha^2} \tag{3.12}$$

Due to the sharp resonance of the LC network, the output spectrum shows tails decreasing from ω_o as α^2.

A first contribution to S_{ni} arises from the thermal noise $2kTg_{ot}$ of the ohmic parasitics of the loop filter. In other terms, the equivalent conductance g_{ot} appears not only into the quality factor of the filter, but it also accounts for the thermal noise due to the parasitic resistances of the tank. The noise of the transconductor may be instead represented by adding a current spectral density $2kTg_{ot}F$, where F is a suitable noise factor. Therefore we have $S_{ni} = 2kTg_{ot}(1+F)$, the output voltage noise may be written as

$$S_{nv}(\alpha) = \frac{1}{2}\frac{kT}{C}\frac{\omega_o}{Q}\frac{1}{\alpha^2}(1+F) \tag{3.13}$$

All the difficulty of the noise calculations is now hidden within F, the noise factor of the differential stage.

For totally uncorrelated noise one half of the total noise power contributes to the AM and the other half gives a PM. If $A_o \gg 2V_T$, the differential stage behaves as a

hard limiter and only the PM component is transmitted to the output. It follows that the noise power spectral density, must be divided by a factor 2, thus obtaining

$$S_{nv}(\alpha) = \frac{1}{4}\frac{kT}{C}\frac{\omega_o}{Q}\frac{1}{\alpha^2}(1+F) \tag{3.14}$$

However, the nonlinear behavior of the stage has an impact larger than the simple introduction of the above factor 2. We will show in the following that intermodulations between the carrier and wide-band noise sources cause noise folding that increases the transconductor noise factor F.

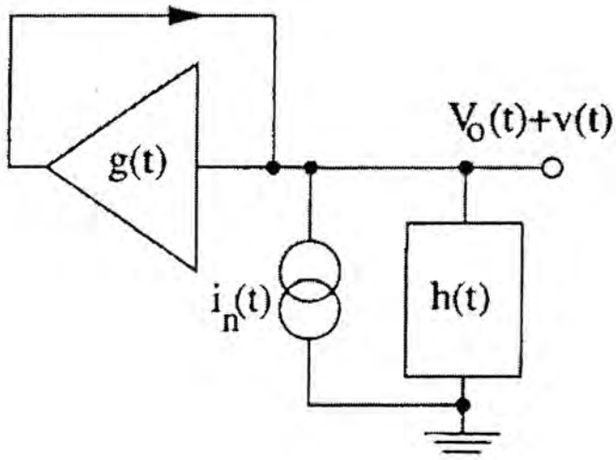


Figure 3.7 Single-ended equivalent circuit

The solution can be found analytically [23] when the transconductor behaves as a hard limiter. Each noise component, I_n, is delivered to the tank via the switching transconductor, i.e. multiplied by a square wave T(t) with a frequency ω_o. We have

$$\left(\frac{\bar{I}_n}{2}e^{j\omega t} + \frac{\bar{I}_n^*}{2}e^{-j\omega t}\right)\sum_{n=-\infty}^{+\infty} T^{(2n+1)}e^{j(2n+1)\omega_o t} \tag{3.15}$$

where $\bar{I}_n$ is the generic noise tone, $T^{(2n+1)} = e^{jn\pi} / \pi(2n+1)$, and $T^{(2n+1)} = T^{-(2n+1)}$. It

turns out that the noise tones $\bar{I}_u$ and $\bar{I}_l$, at frequency $\omega_o \pm \alpha$, are due to the noise components around the even harmonics of ω_o, i.e. $2n\omega_o \pm \alpha$. Analytically we have

$$\begin{bmatrix} \bar{I}_l^*/2 \\ \bar{I}_u/2 \end{bmatrix} = \begin{bmatrix} T^{(-1)} & T^{(1)} & T^{(-3)} & \dots \\ T^{(1)} & T^{(3)} & T^{(-1)} & \dots \end{bmatrix} \begin{bmatrix} \bar{I}_n(\alpha)/2 \\ \bar{I}_n^*(2\omega_o - \alpha)/2 \\ \bar{I}_n(2\omega_o + \alpha)/2 \\ \bar{I}_n^*(4\omega_o - \alpha)/2 \\ \dots \end{bmatrix} \tag{3.16}$$

In reality the folding factor will depend on both the I(V) characteristic of the transconductor and its bandwidth. The transconductor output noise spectrum is obtained from the convolution between these delta functions and the wideband noise (Figure 3.8). The convolution gives rise to a noise folding, similar to what happens in sampled systems.

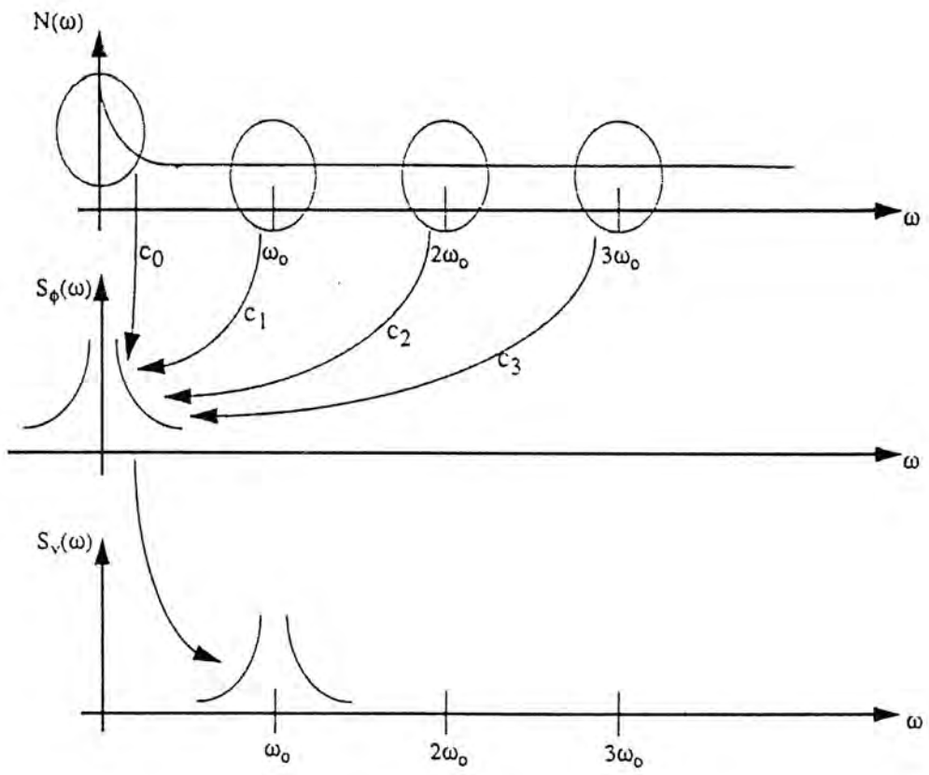


Figure 3.8 Evolution of noise

3.3.4 Flicker-Noise Upconversion Mechanism

Compared to bipolar transistors, MOS transistor generates more flicker noise. In oscillator, flicker noise is upconverted to $1/f^3$ phase noise. Consequently, the $1/f^3$ phase noise will be much higher in MOS oscillators than in bipolar oscillators and becomes an effect that has to be taken into account.

The mechanism of flicker-noise upconversion can be examined as follows. Flicker noise from the tail current source that enters the LC-tank will be upconverted due to the mixing action of the VCO circuit. Additionally, when the single differential oscillator circuit is unbalanced, the common-mode node of the current source will oscillate at twice the oscillator center frequency, $2\omega_o$, because the current source will be pulled every time one of the NMOS transistors switches on. Through channel length modulation, the noise of the trail current source is upconverted to $2\omega_o$. The upconverted noise enters the LC-tank and is mixed with the fundamental oscillator frequency, resulting in phase-noise sidebands at the oscillator frequency. Therefore, to minimize the upconversion of flicker noise from the tail current source, all even harmonics must be suppressed, meaning that the circuit must be as symmetric as possible. Odd harmonics have little importance for flicker-noise upconversion because they do not affect the symmetry, and noise at odd harmonics

does not result in sidebands around the fundamental frequency when mixed. Flicker noise from the tail current source will be the main contributor to $1/f^3$ phase noise. Flicker noise is correlated noise and can only exist in systems with memory. When transistors are ideally switched, all memory and consequently the flicker noise is removed. When the switching is not ideal, a small amount of the NMOS transistor flicker noise will be upconverted.

In some oscillator designs, the main source of upconverted flicker noise is the current source. Therefore, a PMOS transistor was chosen for the tail current source because of its inherently lower flicker noise (approximately 10dB), compared to NMOS transistors. The area of the PMOS transistor is increased, by designing the transistor length larger than the minimum length, to further minimize the flicker-noise contribution. Additional circuit techniques have also been reported to further minimize the flicker-noise upconversion. A capacitance and a cascode transistor are added to the common-mode node of the tail current source to suppress all common-mode node variations. As a result, noise upconversion due to channel length modulation by higher (and especially the second) order harmonics is suppressed.

3.4 Phase Noise Reduction Techniques

As mentioned previously, the phase noise associated with a VCO is determined by:

(a) Q factor of the resonator

(b) Q factor of the varactor diode

(c) effective noise factor of the active devices used

(d) power supply noise

(e) external tuning voltage supply noise

The noise contribution made by (d) and (e) can be minimized by careful choice of the power supplies. The phase noise of the VCO is therefore governed primarily by the overall Q of the circuit, and the noise up-conversion factor.

3.4.1 Conventional Tank Circuit Structure

As stated in the previous sections, the standard NMOS cross-coupled differential oscillators with symmetrical structure can be transformed into a single-sided equivalent circuit, as shown in Figure 3.9. Differential topologies are advantageous in integrated circuit because they offer common-mode rejection. Therefore, differential circuits are less susceptible to supply noise present in on-chip power rails. Differential VCO topologies also avoid the need for single-ended to

differential conversion circuitry for the LO drive of a Gilbert-cell mixer.

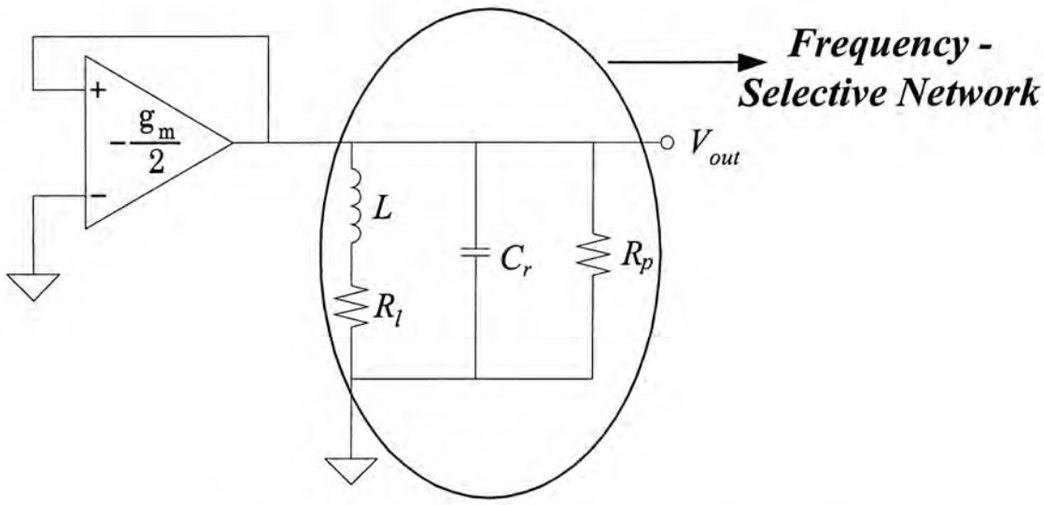


Figure 3.9 Single-sided equivalent circuit

The frequency-selective network can be transformed into an LC tank network with parallel loss only (Figure 3.10):

$$\frac{1}{R_{p,total}} = \frac{1}{R_l(Q_l^2+1)} + \frac{1}{R_p} \tag{3.17}$$

where $Q_l = \frac{\omega L}{R_l}$

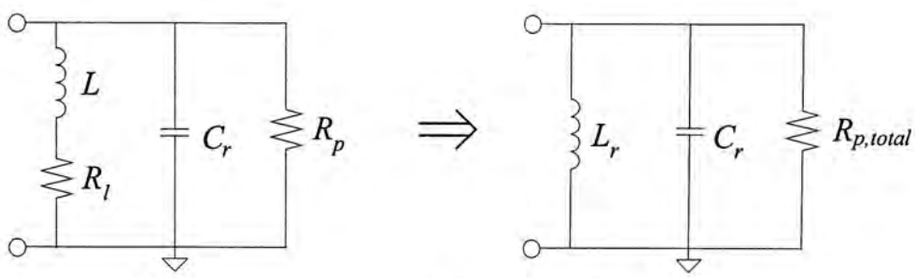


Figure 3.10 The resonator of single-sided equivalent circuit

Subsequently, the overall Q of the resonator can be derived as follows:

$$Y_{in} = j\omega C_r + \frac{1}{j\omega L_r} + \frac{1}{R_{p,total}}$$

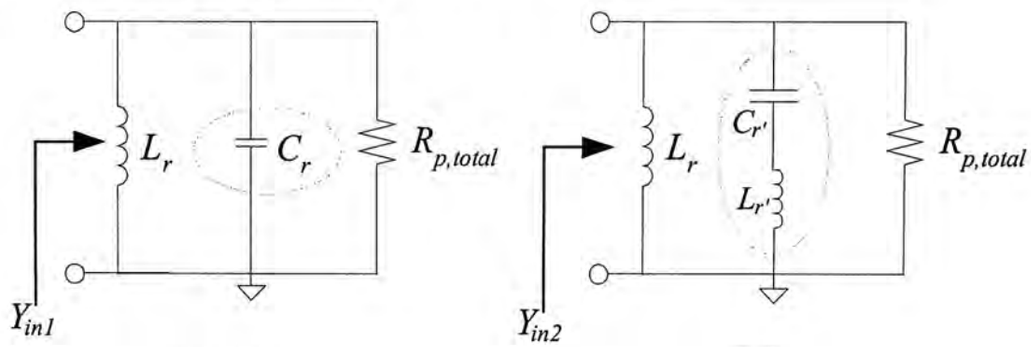
$$\Rightarrow \quad \phi = \tan^{-1}\left[\omega R_{p,total}\left(C_r - \frac{1}{\omega^2 L_r}\right)\right]$$

$$\Rightarrow \quad \left.\frac{\partial\phi}{\partial\omega}\right|_{\omega=\omega_o} = 2R_{p,total}C_r$$

By using $Q_L = \frac{\omega_o}{2}\left.\frac{\partial\phi}{\partial\omega}\right|_{\omega=\omega_o}$

$$\Rightarrow \quad Q_L = \omega_o R_{p,total} C_r \tag{3.18}$$

3.4.2 Enhanced Q Tank Circuit Structure



(a) (b)

Figure 3.11 Two different frequency-selective networks

Assuming that the two resonant circuits shown in Figure 3.11 exhibit the same resonant frequency, then the relationship between the element values is given by,

$$C_r = \frac{1}{\omega_o^2 L_r} \tag{3.19}$$

$$C_{r'} = \frac{C_r}{1+\omega_o^2 L_{r'} C_r} \tag{3.20}$$

As a result, the loaded quality factor of circuit(b) can be derived as:

$$Y_{in2} = \frac{1}{\frac{1}{j\omega C_{r'}} + j\omega L_{r'}} + \frac{1}{j\omega L_r} + \frac{1}{R_{p,total}} \tag{3.21}$$

$$\Rightarrow \phi = \tan^{-1}\left[R_{p,total} \times \left(\frac{\omega C_{r'}}{1-\omega^2 L_{r'} C_{r'}} - \frac{1}{\omega L_r} \right) \right]$$

$$\Rightarrow \left.\frac{\partial \phi}{\partial \omega}\right|_{\omega=\omega_o} = 2R_{p,total}C_r + 2\omega_o^2 C_r^2 L_{r'} R_{p,total} = 2R_{p,total}C_r\left(\frac{C_r}{C_{r'}}\right) \tag{3.22}$$

Thus,

$$Q_L = \frac{\omega_o}{2}\left.\frac{\partial \phi}{\partial \omega}\right|_{\omega=\omega_o} = \omega_o R_{p,total} C_r \left(\frac{C_r}{C_{r'}}\right)$$

Since the value of C_r is always larger than $C_{r'}$ and thus, the loaded Q of circuit(b) is always larger than the loaded Q of circuit(a). Subsequently, we can define the noise reduction factor (NRF) as,

$$\begin{aligned} NRF = 10\log\left\{\frac{Phase\ noise\ of\ circuit(a)}{Phase\ noise\ of\ circuit(b)}\right\} &\approx 20\log\frac{Q_{L,b}}{Q_{L,a}} \\ &\approx 20\log\frac{C_r}{C_{r'}} \end{aligned} \tag{3.23}$$

For illustration, the noise reduction performance of the proposed tank structure versus $\frac{C_r}{C_{r'}}$ is plotted in Fig 3.12. It indicates that a larger value of $\frac{C_r}{C_{r'}}$ is desirable for better phase noise improvement. However, in practice, the adoption of a

smaller capacitance $C_{r'}$ leads to a higher inductance value ($L_{r'}$) and inductor series resistance, which limits the highest attainable Q factor of the tank circuit.

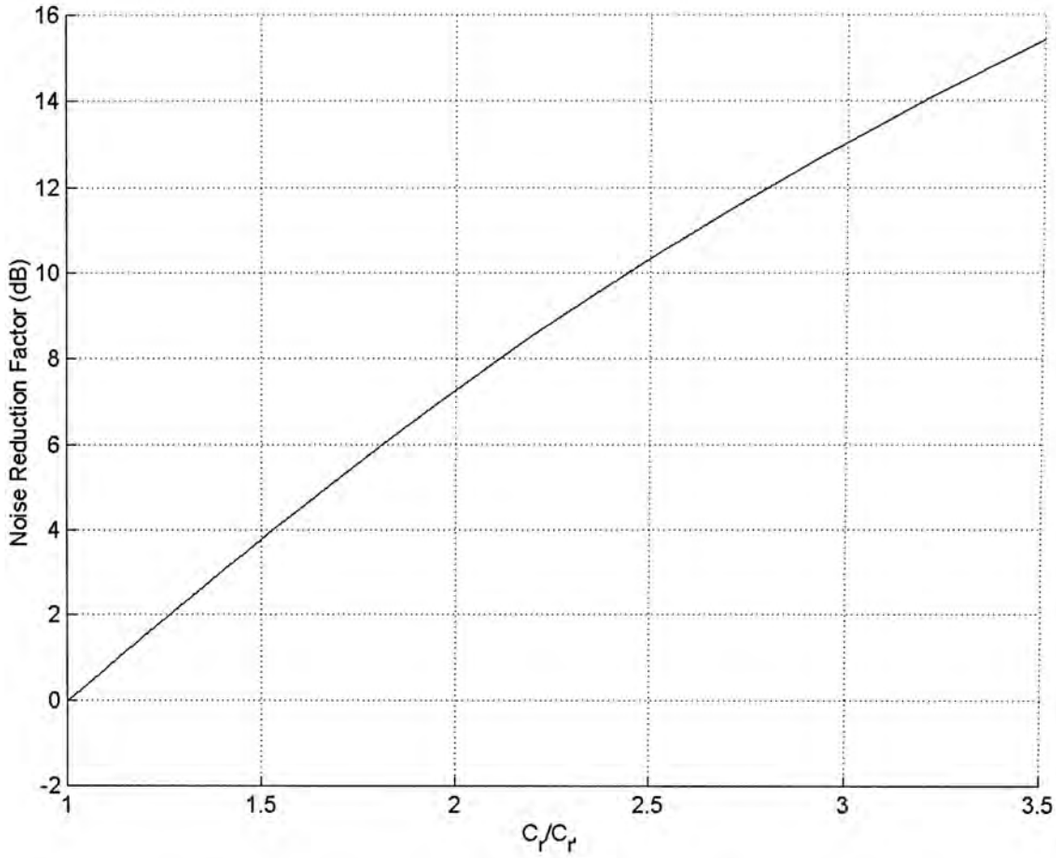


Figure 3.12 Predicted noise reduction performance of the proposed VCO Circuit

3.4.3 Tank Circuit with parasitics

Figure 3.13 shows the equivalent circuit of the modified tank circuit with parasitics such as inductor loss resistance $R_{L'}$ and gate capacitance C_g of the FET.

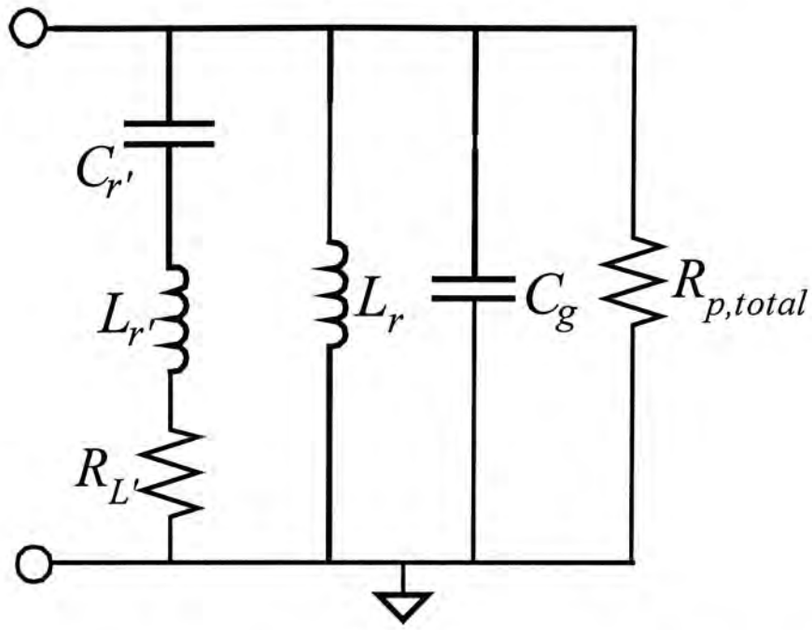


Figure 3.13 Enhanced Q resonant tank with parasitics

The input admittance of the LC tank is given as,

$$Y_{in} = \frac{1}{\frac{1}{j\omega C_{r'}} + j\omega L_{r'} + R_{L'}} + \frac{1}{j\omega L_r} + j\omega C_g + \frac{1}{R_{p,total}}$$

$$\Rightarrow \phi = \tan^{-1}\left[-\frac{Z_L}{L_r}\left(\frac{1-\omega^2 C_g L_r}{\omega} + \frac{\omega^2 L_r L_{r'} - \frac{L_r}{C_{r'}} - R_{p,total} R_{L'}\left(1-\omega^2 C_g L_r\right)}{\omega\left(R_{L'}^2 + \left(\omega L_{r'} - \frac{1}{\omega C_{r'}} \right)^2 + R_{p,total} R_{L'} \right)} \right) \right]$$

By using the formula, $Q_L = \frac{\omega_o}{2} \frac{\partial \phi}{\partial \omega}\Big|_{\omega=\omega_o}$, the variation of Q_L versus $\frac{C_r}{C_{r'}}$ is plotted in Figure 3.14. The results indicate that the noise reduction factor deteriorates as the unloaded Q value of the inductor decreases.

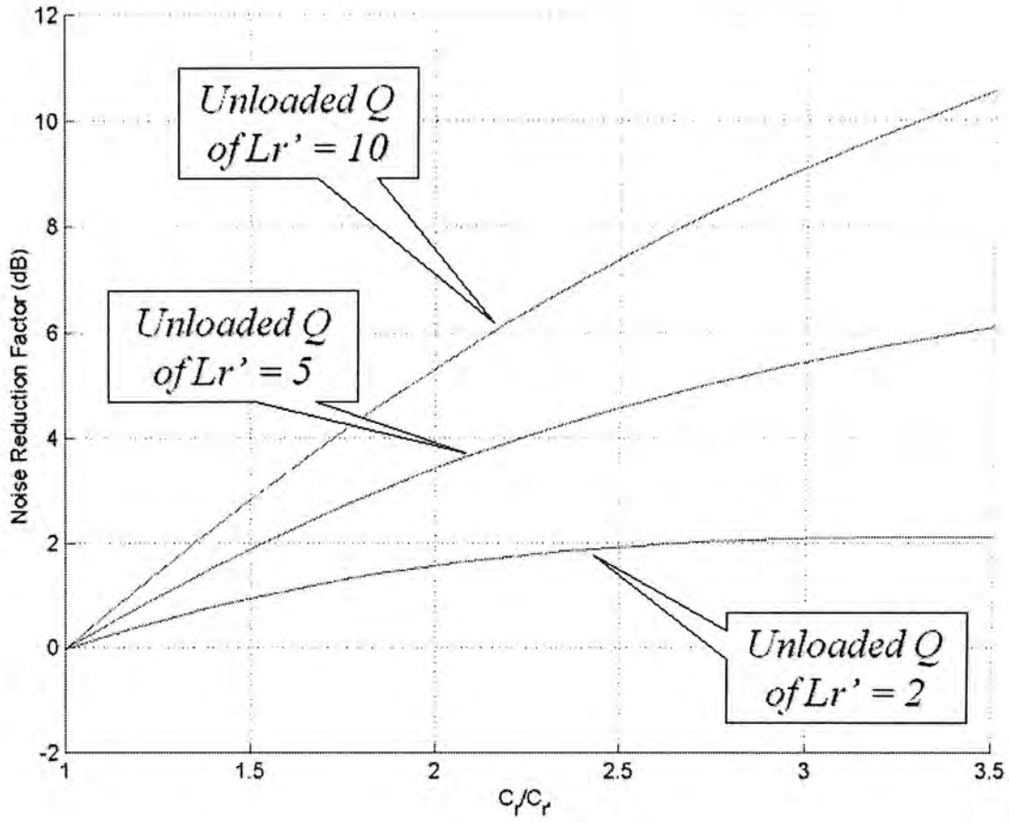


Figure 3.14 Noise Reduction Factor versus $\frac{C_r}{C_{r'}}$, as a function of unloaded inductor Q

3.4.4 Reduction of Second-Harmonic Induced Up-converted Noise

In section 5.3, we have discussed the transfer of the noise sources in a differential LC tuned oscillator. We have shown that the nonlinear operation of the transconductor stage has to be properly accounted for since it introduces spectrum folding.

When an inductor is connected in series with the capacitor in the LC tank

(Figure 3.11), a transmission zero is introduced at a frequency given by,

$$\omega_z = \sqrt{\frac{1}{L_{r'}C_{r'}}} \tag{3.24}$$

Therefore, for the suppression of the second harmonic component, we have,

$$\omega_z = \sqrt{\frac{1}{L_{r'}C_{r'}}} = 2\omega_o \tag{3.25}$$

Combining equation (3.20) and (3.25), we get,

$$C_r = \frac{C_{r'}}{1-\omega_o^2 L_{r'}C_{r'}} = \frac{C_{r'}}{1-\frac{1}{4}} = \frac{4}{3}C_{r'} \tag{3.26}$$

Figure 3.15 shows the plot of input impedance variations of circuit (a) and (b) as a function of normalized frequency. It can be seen from the diagram that a short-circuit is present at the second harmonic.

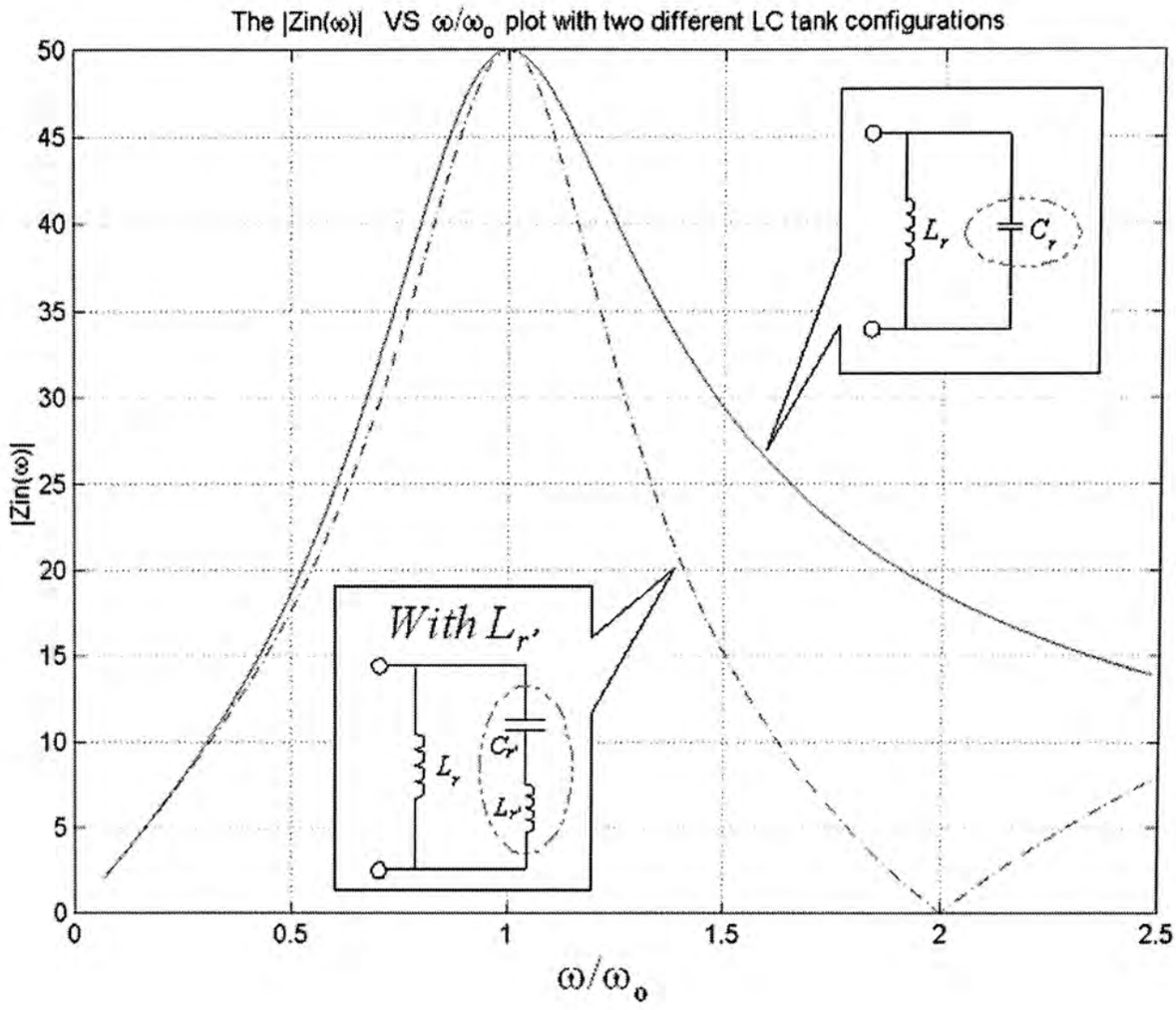


Figure 3.15 Variation of Input impedance versus frequency of LC tank circuits

Chapter 4 CMOS Device Modeling

At the dawn of its fifth decade, the semiconductor industry continues to grow at an amazing pace. High-speed and low-power CMOS integrated circuits (IC) are used in an ever expanding trend. Thus, a critical part of this technology is high-quality circuit design. In this project, all oscillators are implemented with AMS CUP 0.6 micron process technology. These oscillators are fully integrated with planar spiral inductors. This chapter describes the corresponding technologies in designing the oscillator circuits, particularly the development of device model for FET, inductor as well as varactor in CMOS process.

4.1 Device Modeling

4.1.1 FET model

Circuit simulator is an essential tool in designing integrated circuits. The accuracy of circuit simulation highly depends on the types of transistor model used. Reduction in transistor size continually complicates the device physics and makes device modeling more challenging and sophisticated. BSIM3v3 (BSIM stands for Berkeley Short-channel IGFET Model) was selected as the industrial MOSFET model by many leading companies in the semiconductor industry such as Cadence design

Systems, Hewlett Packard, Mentor Graphics, ...etc. It is a model developed by the BSIM Research Group in UC Berkeley. Details of this model can be found in the following website: ***http://www-device.eecs.berkeley.edu/~bsim3***

This model explicitly takes into account the effects of many physical and process variables for good device scalability and predictability. The short channel and narrow width effects as well as high-field effects are well modeled. The minimum channel length that can be modeled is 0.15 micron.

The list below shows the typical SPICE circuit netlists of BSIM3v3 model.

NMOS	**PMOS**
*model = bsim3v3	*model = bsim3v3
*Berkeley Spice Compatibility	*Berkeley Spice Compatibility
* Lmin= .35 Lmax= 20 Wmin= .6 Wmax= 20	* Lmin= .35 Lmax= 20 Wmin= .6 Wmax= 20
.model N1 NMOS	.model P1 PMOS
+Level= 8	+Level= 8
+Tnom=27.0	+Tnom=27.0
+Nch= 2.498E+17 Tox=9E-09 Xj=1.00000E-07	+Nch= 3.533024E+17 Tox=9E-09 Xj=1.00000E-07
+Lint=9.36e-8 Wint=1.47e-7	+Lint=6.23e-8 Wint=1.22e-7
+Vth0= .6322 K1= .756 K2= -3.83e-2 K3= -2.612	+Vth0=-.6732829 K1= .8362093 K2=-8.606622E-02 K3= 1.82
+Dvt0= 2.812 Dvt1= 0.462 Dvt2=-9.17e-2	+Dvt0= 1.903801 Dvt1= .5333922 Dvt2=-.1862677
+Nlx= 3.52291E-08 W0= 1.163e-6	+Nlx= 1.28e-8 W0= 2.1e-6
+K3b= 2.233	+K3b= -0.24 Prwg=-0.001 Prwb=-0.323
+Vsat= 86301.58 Ua= 6.47e-9 Ub= 4.23e-18 Uc=-4.706281E-11	+Vsat= 103503.2 Ua= 1.39995E-09 Ub= 1.e-19 Uc=-2.73e-11
+Rdsw= 650 U0= 388.3203 wr=1	+ Rdsw= 460 U0= 138.7609
+A0= .3496967 Ags=.1 B0=0.546 B1= 1	+A0= .4716551 Ags=0.12
+ Dwg = -6.0E-09 Dwb = -3.56E-09 Prwb = -.213	+Keta=-1.871516E-03 A1= .3417965 A2= 0.83
+Keta=-3.605872E-02 A1= 2.778747E-02 A2= .9	+Voff=-.074182 NFactor= 1.54389

+Voff=-6.735529E-02 NFactor= 1.139926 Cit=	Cit=-1.015667E-03
1.622527E-04	+Cdsc= 8.937517E-04
+Cdsc=-2.147181E-05	+Cdscb= 1.45e-4 Cdscd=1.04e-4
+Cdscb= 0 Dvt0w = 0 Dvt1w = 0 Dvt2w = 0	+ Dvt0w=0.232 Dvt1w=4.5e6 Dvt2w=-0.0023
+ Cdscd = 0 Prwg = 0	+Eta0= 6.024776E-02 Etab=-4.64593E-03
+Eta0= 1.0281729E-02 Etab=-5.042203E-03	+Dsub= .23222404
+Dsub= .31871233	+Pclm= .989 Pdiblc1= 2.07418E-02 Pdiblc2=
+Pclm= 1.114846 Pdiblc1= 2.45357E-03 Pdiblc2=	1.33813E-3
6.406289E-03	+Drout= .3222404 Pscbe1= 118000 Pscbe2= 1E-09
+Drout= .31871233 Pscbe1= 5000000 Pscbe2=	+Pvag= 0
5E-09 Pdiblcb = -.234	+kt1= -0.25 kt2= -0.032 prt=64.5
+Pvag= 0 delta=0.01	+At= 33000
+ Wl = 0 Ww = -1.420242E-09 Wwl = 0	+Ute= -1.5
+ Wln = 0 Wwn = .2613948 Ll = 1.300902E-10	+Ua1= 4.312e-9 Ub1= 6.65e-19 Uc1= 0
+ Lw = 0 Lwl = 0 Lln = .316394	+Kt1l=0
+ Lwn = 0	
+kt1=-.3 kt2=-.051	
+At= 22400	
+Ute=-1.48	
+Ua1= 3.31E-10 Ub1= 2.61E-19 Uc1= -3.42e-10	
+Kt1l=0 Prt=764.3	

Nowadays, as transistors were scaled to submicron dimensions, it became increasingly more difficult to introduce physically meaningful equations that would be both accurate and computationally efficient. BSIM adopted a different approach: numerous empirical parameters were added in order to simplify the equations. A feature of BSIM is the addition of a simple equation to represent the geometry dependences of many device parameters. For example:

$$P = P_o + \frac{\alpha_P}{L_{eff}} + \frac{\beta_P}{W_{eff}}$$

where P_o is the value of empirical parameter of a long, wide transistor, α_p and β_p are fitting factors.

BSIM model has three generations. Each generation has some special features. They are:

BSIMv1:

- Using approximately 50 parameters;
- Dependence of mobility upon the vertical field includes the substrate voltage;
- Currents in the weak and strong inversion regions are derived such that their values and first derivatives are continuous;
- Simplify the drain current equations, new expressions are devised for velocity saturation, dependence of mobility upon the lateral field, and the saturation voltage.

BSIMv2:

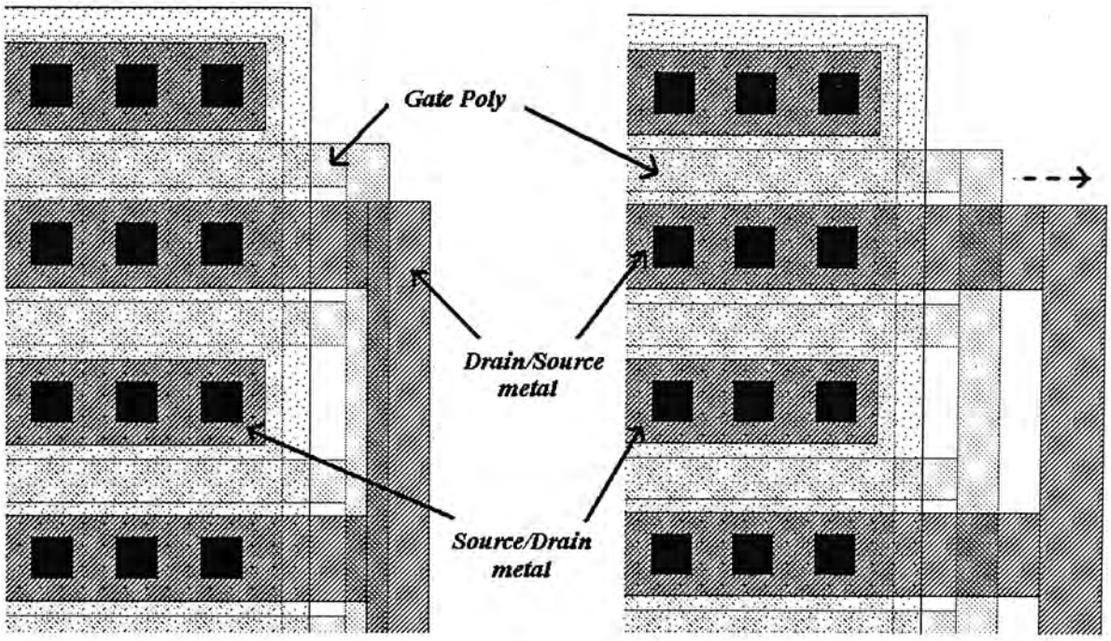
- Using approximately 70 parameters;
- Employs new expressions for mobility, drain current, and subthreshold conduction;
- Suffers from large errors in the triode region for short, narrow transistors

BSIMv3:

- Using approximately 180 parameters;
- Returns to the physical principles of device operation while maintaining many of the useful features of BSIM and BSIM2.
- Provides reasonable accuracy for subthreshold and strong inversion operation while still suffering from large errors in predicting the output impedance for short channel length FET.

4.1.2 Layout of Interdigitated FET

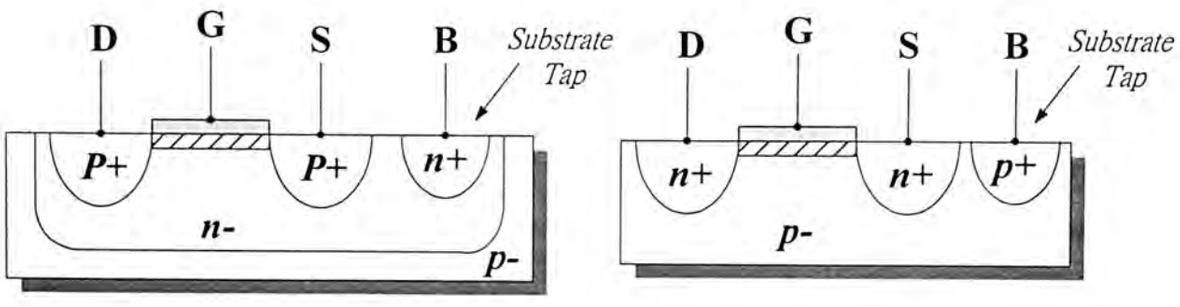
- In designing multi-finger FETs, as in figure 7.1(a), the overlapping of Drain/Source metal to gate poly will generate more parasitic loss. Figure 4.1(b) shows a common practice to move the Drain/Source metal trace far apart from the gate poly, to get rid of parasitic capacitance.



(a) (b)

Figure 4.1 Minimize gate poly-to-drain/source metal capacitance

- Furthermore, for the proper operation of FETs in CMOS process, it is necessary to provide a substrate tap. In Figure 7.2 shows the example of adding substrate tap to NMOS and PMOS. In order to eliminate the bulk resistance of the FETs, extra substrate taps should be placed close to the FETs.



(a) (b)

Figure 4.2(a) NMOS with substrate tap, (b) PMOS with substrate tap

Moreover, vias are needed to connect the source/drain diffusion region to the metal segment (Figure 4.3). As a rule of thumb, via are added at equal distance to reduce the internal resistance associated with the interconnect, as depicted in Figure 4.4.

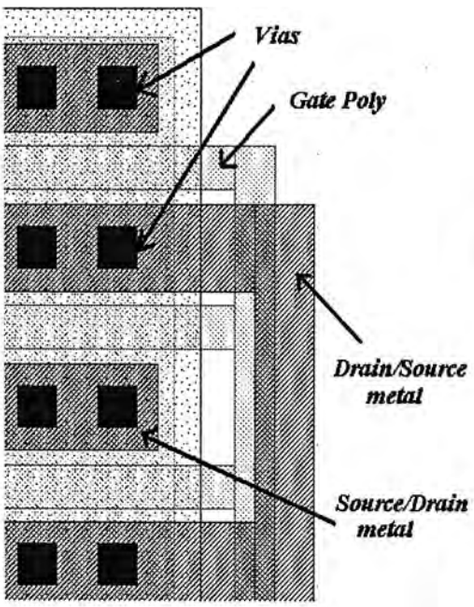


Figure 4.3 Layout of Vias in FETs

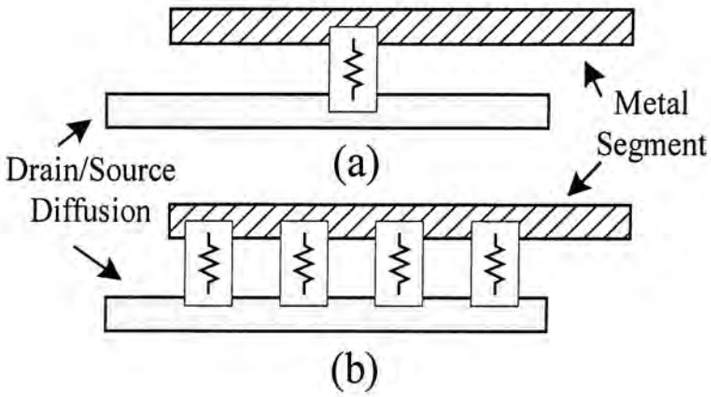


Figure 4.4 Connection of metal segment and drain/source diffusion with (a) a via, (b) four vias

4.1.3 Planar Inductor

Recently, bonding wire is used as inductor in CMOS process due to its low series resistance. A typical use of bonding wire is to connect the bond pad on top of the wafer die to the lead of the package or to another bond pad. Unfortunately, these hybrid inductors suffer from large variations in inductance value due to manufacturing tolerances.

Monolithic inductors fabricated as simple spirals on Si substrate, are often associated with lower Q factor due to resistive loss and substrate loss. The inductance of a monolithic inductor is defined solely by its geometry. Since modern photolithographic processes provide extremely tight geometric tolerances, monolithic inductors have very small variations in their performance. There are many ways to layout a planar spiral inductor. The optimum structure is a circular spiral. This structure places the largest amount of conductors in the smallest possible area, reducing the series resistance of the spiral. This structure, however, is often not used because it is not supported by many mask generation systems. For the CMOS process used here, the standard square spiral structure are recommended, as shown in Figure 4.5(a).

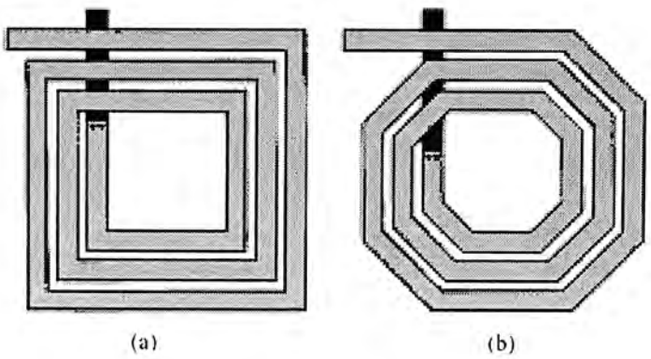


Figure 4.5 Spiral Inductor Layout: (a)square and (b)octagonal.

The total inductance value of the spiral can be computed by using Greenhouse's method [17]. Basically, the spiral square inductor is split up into sections consisting of straight conductors, and the self-inductance of the sections is calculated and summed.

4.1.4 Circuit Model of Planar Inductor

The self-inductance for a straight conductor is,

$$L = 0.002l\left[\ln\left(\frac{2l}{GMD}\right) - 1.25 + \frac{AMD}{l} + \left(\frac{\mu}{4}\right)T\right] \tag{4.1}$$

where L is the self-inductance in μH, l is the conductor length in cm, m is the conductor permeability, and T is the frequency correction parameter.

Geometric Mean Distance (GMD) is the distance between two infinitely thin imaginary filaments whose mutual inductance is equal to the mutual inductance between the two original conductors. The GMD is equal to 0.44705 times a side in the case of a square cross section.

Arithmetic Mean Distance (AMD) is the average of all the distances between the points of one conductor and the points of another. For a single conductor, the arithmetic mean distance is the average of all possible distances within the cross section.

If the top layer of metal is used for the layout of the spiral inductor, we can consider it as a thin-film inductor with rectangular cross section. Thus, equation(4.1) can be simplified as,

$$L = 0.002l\left[\ln\left(\frac{2l}{a+b}\right) + 0.50049 + \frac{a+b}{3l}\right] \tag{4.2}$$

where a, b are the rectangular dimension of the cross section. The magnetic permeability m is 1, and the skin-depth phenomenon has little effect on thin film, T is an empirical parameter, which should be considered to have a value of 1 for

microwave frequencies.

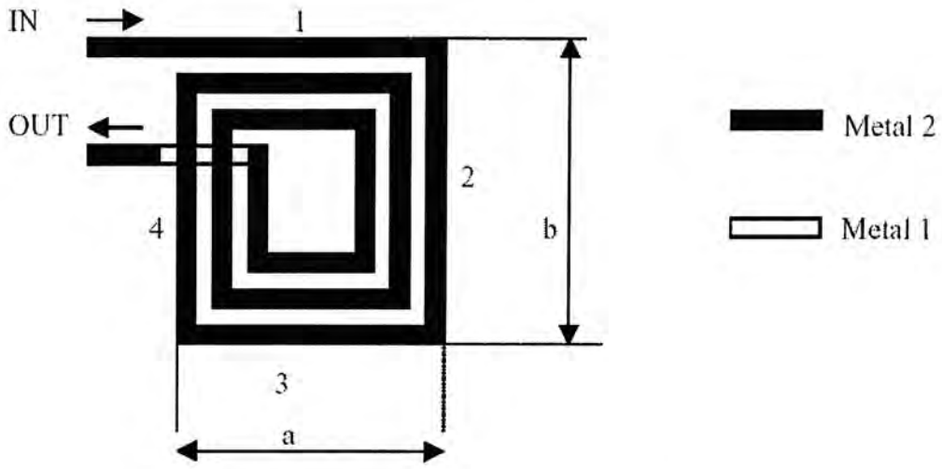


Figure 4.6 Layout of a typical rectangular spiral inductor.

There are several sources of loss in a spiral inductor. The most obvious loss mechanism is the series winding resistance. The interconnect metal used in most CMOS processes has typically been aluminum. Depending on the metalization thickness and particular aluminum alloy used, the sheet resistivity can be anywhere from 30-70 mΩ / □. However, at higher frequencies, the resistance of the spiral increases due to the skin effect and "current crowding" at the corners of each turn. On the other hand, standard CMOS substrate losses ultimately remain the limiting factor, even when the conductivity of the spiral windings is no longer an issue.

In an CMOS process, the windings of the spiral are separated from the substrate by a thin layer of Silicon dioxide. This creates capacitance between the spiral and the surface of the substrate. Thus, the heavily doped p-type substrate appears as a

grounded resister in series with this capacitance.

There are also losses due to the magnetic field in the inductor structure. The magnetic field extends around the windings of the spiral and into the substrate. This field forces an image current to flow in the substrate. These currents can account for 50% or more of the losses in a CMOS inductor. Use of non-standard high-resistivity Si substrates, or a post-process to etch the substrate away under the inductor, can minimize these losses.

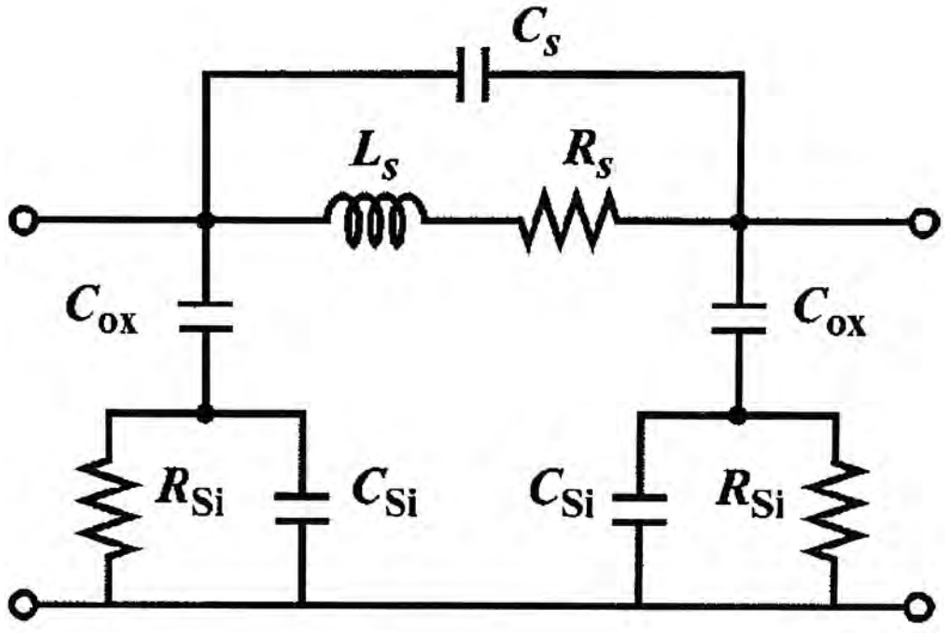


Figure 4.7 Lumped physical model of spiral inductor on Silicon

A general circuit model for a monolithic inductor on a low-resistivity substrate is

shown in Figure 4.7 [15]. This model includes circuit elements that model the winding less as well as the substrate loss. The model parameters can be evaluated by the following equations:

$$R_s = \frac{\rho \times l}{w \times \delta \times \left(1 - e^{-t/\delta}\right)}$$

$$C_s = n \times w^2 \times \frac{\varepsilon_{ox}}{t_{ox_{metal}}}$$

$$C_{ox} = \frac{1}{2} \times l \times w \times \frac{\varepsilon_{ox}}{t_{ox}} \tag{4.3}$$

$$C_{si} = \frac{1}{2} \times l \times w \times C_{sub}$$

$$R_{si} = \frac{2}{l \times w \times G_{sub}}$$

where

L_s stands for spiral inductance

R_s stands for series sheet resistance

C_s represents the capacitance due to the overlaps between the spiral and the center-tap underpass

C_{si} models the silicon substrate capacitance

R_{si} models the silicon substrate resistance

n stands for number of turns of spiral trace

ρ stands for metal resistivity,

l stands for total length of the spiral

w stands for metal width

δ stands for metal skin depth

t stands for metal thickness

tox_{metal} represents the thickness of the oxide insulator between the spiral and underpass

tox represents the thickness of the oxide layer between the spiral and substrate.

ε_{os} stands for permittivity of the oxide

Gsub stands for substrate conductance

Csub stands for capacitance per unit area

4.1.5 Inductor Layout Consideration

In order to minimize the parasitic loss of inductors, some precaution should be taken in constructing the layout of CMOS spiral inductors [3]:

- Metal trace width should be limited: as the skin effect will reduce the current flow in the center of wide conductor. Thus, wide metal conductors are not efficient.

- Minimize the number of turns: at high frequency, generation of eddy currents will deteriorate the overall quality factor of inductors. Since the innermost turns of the coil suffer from an enormous increase in resistance, while their contribution to the inductance value is minimal.

- Area occupied by the spiral should be reduced: magnetic field generated by inductor induces currents in the substrate at high frequency, which cause a decrease in inductance value and extra resistive losses. Thus, large spirals are not efficient as the magnetic field of small coils penetrates less deep into the substrate. Large spiral inductor consumes too much substrate area and therefore, inductors with inductance value greater than 10nH is not recommanded.

4.1.6 CMOS RF Varactor

There are many types of CMOS varactors, such as junction diode, MOS Varactor[10], Gated Varactor[11] and Three-Terminal Varactor[12]. VCO's based on MOS varactors, a device readily available in any CMOS process, have been reported in the literature.

In the standard CMOS process, junction diode is formed by providing p+ active area in an n-well. The junction diode is operated in reverse-bias mode, and therefore its junction capacitance can be made tunable by a voltage. The disadvantages of diode varactors are:

- large wafer area is needed to provide higher capacitance value,
- lack of high frequency model

It is well known that an MOS transistor with drain, source, and bulk connected together realizes an MOS capacitor with capacitance value dependent on the voltage between the bulk and gate (Figure 4.8). The capacitance variation of a typical PMOS varactor as a function of V_{BG} is illustrated in figure 4.9.

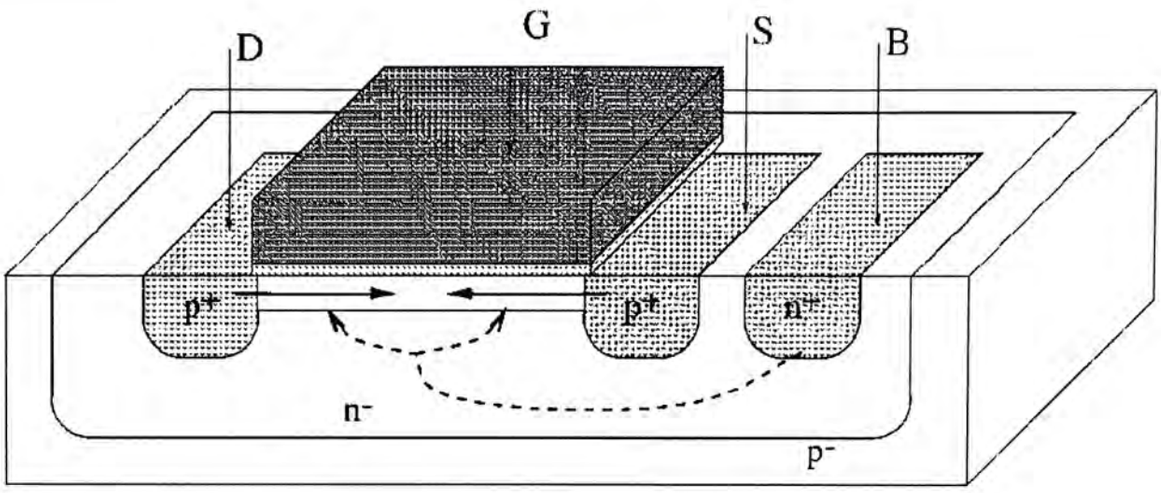


Figure 4.8 Cross-section area of PMOS varactor by connecting D, S and B together

When V_{BG} is negative and high enough to allow electrons to move freely, the concentration of surface majority carrier increases. In this case, the MOS varactor is said to be in deep accumulation, and the resulting capacitance is mainly composed of gate-body capacitance. In the accumulation region, no channel is induced between drain and source region. Thus, MOS capacitance is equal to the gate oxide capacitance: $C_{ox} = \varepsilon_{ox} S / t_{ox}$, where S and t_{ox} are the transistor channel area and the oxide thickness, respectively.

For $V_{BG} > |V_T|$, some free electrons are repelled from the channel region below the gate and pushed downward into the substrate. Depletion layer is formed under the gate oxide layer, and the MOS capacitance can be modeled as C_{ox} in series with $C_b//C_i$. C_b accounts for the modulation of the depletion region, while C_i is related to the

variation of the number of holes at the gate oxide interface. As the value of V_{BG} increases, the depletion region widens and the capacitance is reduced further until it reaches its minimum.

When V_{BG} becomes very much larger than $|V_T|$, more free holes are attracted into the channel region. As a result, an inversion layer with mobile holes is formed in the channel area. MOS capacitance equals the gate oxide capacitance C_{ox}, as in the accumulation region.

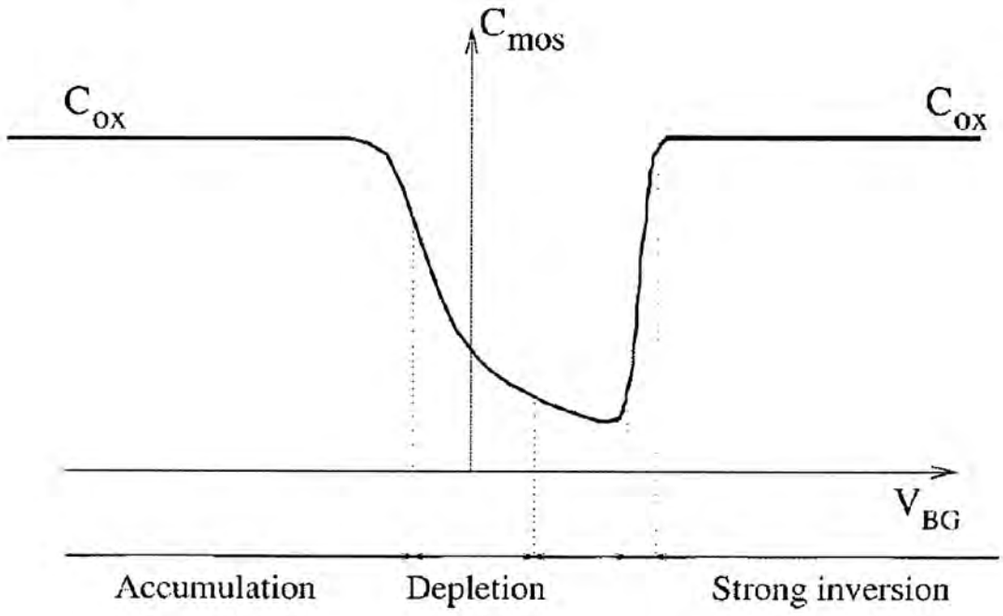


Figure 4.9 Capacitance variation versus tuning voltage of typical PMOS varactor

4.1.7 Parasitics of PMOS-type varactor

It is well-known that the quality factor Q of the MOS varactor has a strong influence on the phase noise performance of VCOs. As a result, the layout design of

the PMOS varactor must be done with care as the parasitics are directly associated with the device geometry. In [19], the parasitic resistance of a PMOS varactor working in strong inversion is given by,

$$R_{mos} = \frac{L}{12k_p W(V_{BG} - |V_T|)} \tag{4.4}$$

where W, L, and k_p are the width, length, and gain factor of the PMOS transistor. Thus, it is seen that a transistor with large W/L ratio should be chosen in order to minimize R_{mos} (Figure 4.10).

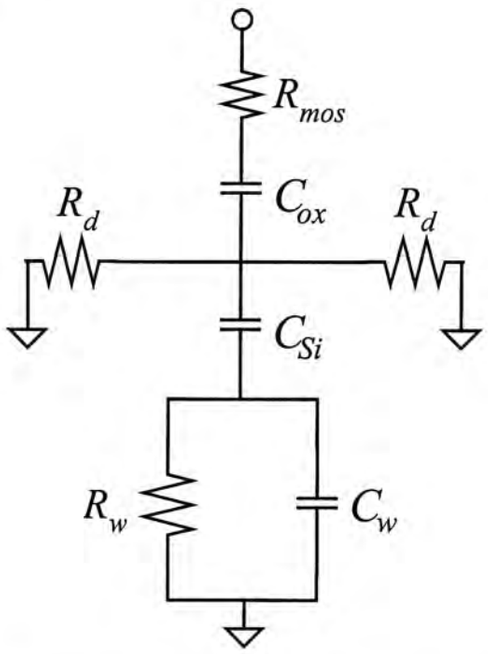


Figure 4.10 Equivalent model of typical PMOS varactor

Chapter 5 Design and Implementation of Integrated CMOS VCO

The Local Oscillator is one of the most fundamental blocks in a telecommunication transceiver. The voltage-controlled oscillator is an integral part of the LO, characterized by very stringent design requirements. Today, the VCO circuits are usually realized using one of the semiconductor technologies: GaAs, bipolar, BiCMOS, SiGe or CMOS. Recent advances in CMOS technology and in particular the continuous shrinkage in transistors' channel length, makes the MOS device comparable to the bipolar transistor in terms of the highest frequency of operation. This chapter deals with the design of CMOS LC oscillators by using two pairs of NMOS/PMOS transistors coupled in positive feedback [9].

5.1 1.5 GHz CMOS VCO Design

5.1.1 Equivalent circuit model of differential LC VCO

Figure 5.1 and 5.2 show the equivalent single-sided model of the differential LC VCO, equivalent model of the resonant tank circuit with all associated losses. The parameters are defined by,

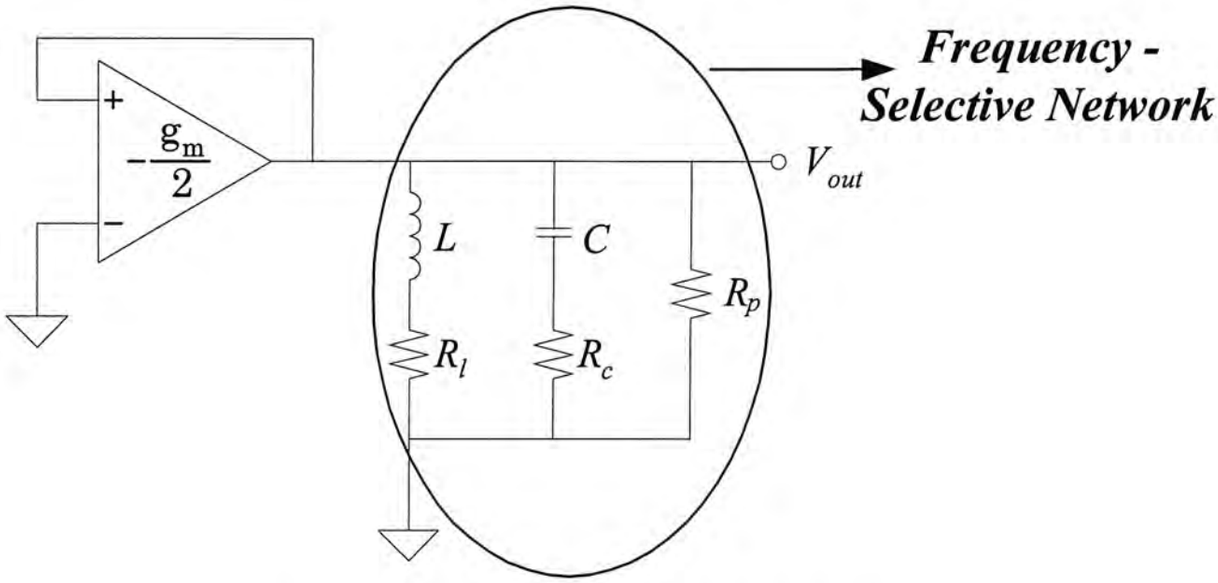


Figure 5.1 Single-sided equivalent circuit

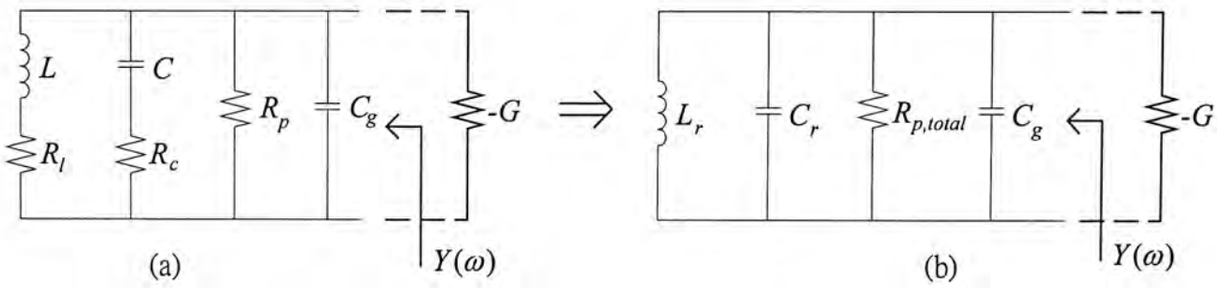


Figure 5.2 (a) LC Tank including all parasitic loss
(b) equivalent LC tank with all losses represented by parallel losses

$$R_{p,total} = \frac{1}{\frac{1}{R_l(Q_l^2+1)} + \frac{1}{R_c(Q_c^2+1)} + \frac{1}{R_p}} \tag{5.1}$$

$$Y(\omega) = j\omega C_r + \frac{1}{j\omega L_r} + \frac{1}{R_{p,total}} + j\omega C_g$$

$$C_r = C\left(\frac{Q_c^2}{Q_c^2+1}\right)$$

$$L_r = L\left(\frac{Q_l^2+1}{Q_l^2}\right)$$

where C_g is the gate capacitance of the FET; C is the varactor capacitance.

Therefore, the frequency of oscillation can be approximated by:

$$f_o = \frac{1}{2\pi\sqrt{L_r\left(C_r + C_g\right)}} \tag{5.2}$$

5.1.2 Reference Oscillator Circuit

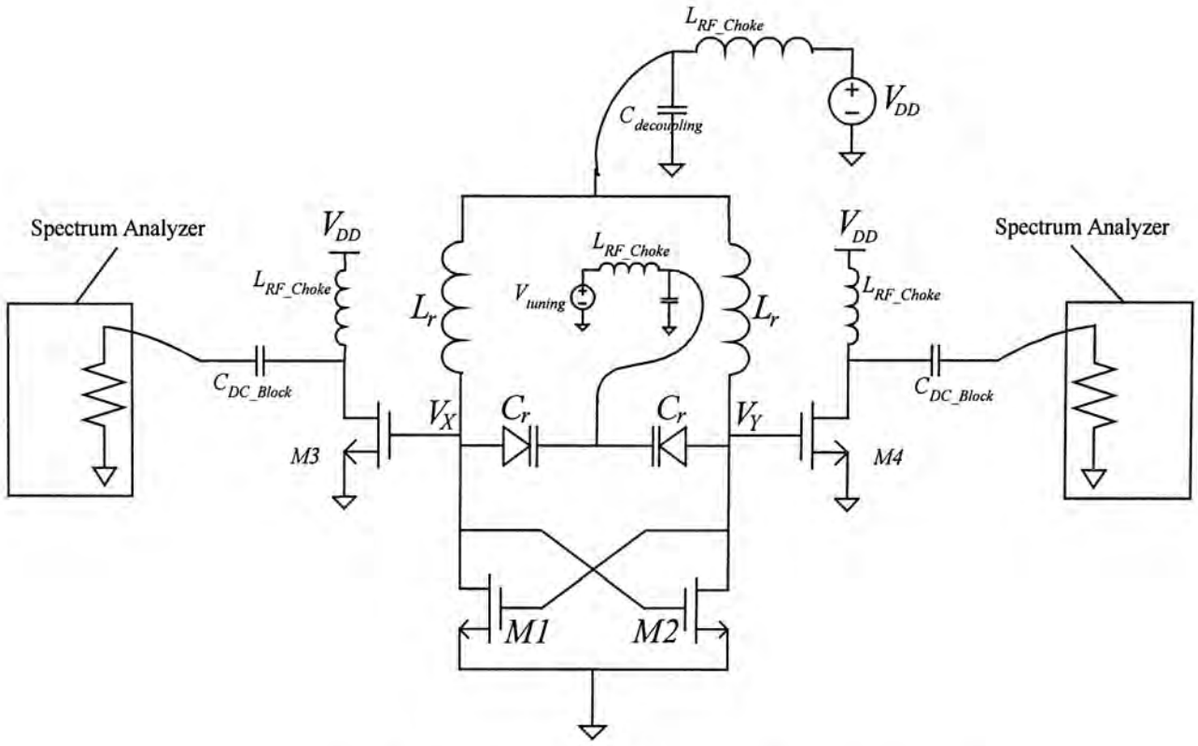


Figure 5.3 Schematic of reference VCO design

In the reference design, two NMOS transistors (M1 and M2) are coupled in positive feedback to provide a negative resistance. The on-chip spiral inductor and PMOS varactor (L_r and C_r) together forms a resonant tank. The oscillating frequency is made variable by using PMOS varactor with the drain, source and substrate all connected to the tuning voltage V_{tuning}, while the gate poly of the varactor is connected to the drain terminals of the NMOS transistor.

According to equation (5.2), with L_r = 3.2nH, the capacitance associated with the tank circuit must be set equal to 3.5pF in order to give an oscillation frequency of 1.5GHz. This capacitance is mainly composed of the inductor-to-substrate capacitance (0.2pF), the gate-source capacitance of the NMOS transistor (1pF), and the capacitance of the PMOS transistor (2.3pF at zero bias).

5.1.3 Proposed Oscillator Circuit

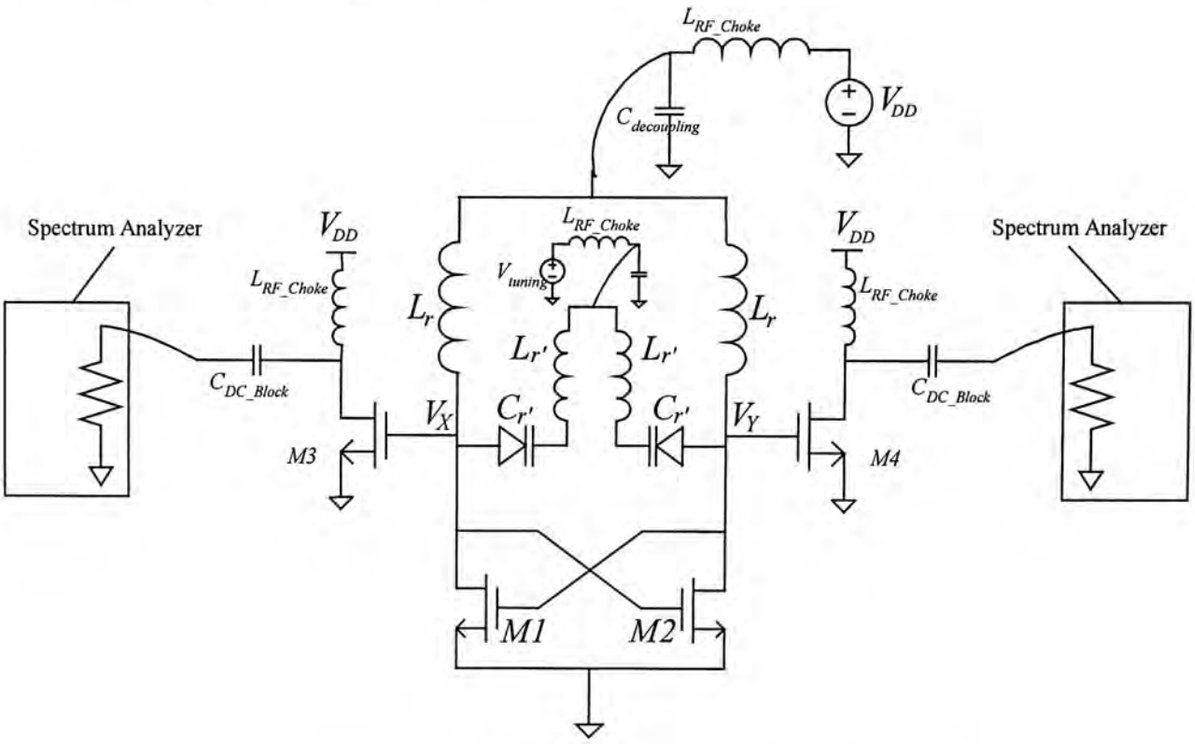
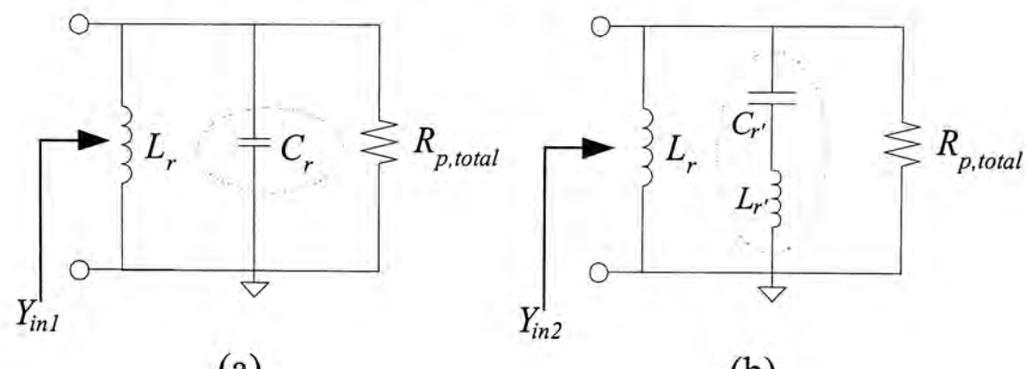


Figure 5.4 Schematic of proposed VCO design



(a) (b)

Figure 5.5 Two different frequency-Selective Networks

Figure 5.5 shows the topology of the LC tank adopted in the reference and proposed VCO circuits. According to the formulas derived in chapter 3, the expression for the component values are simply,

$$C_{r'} = \frac{C_r}{1+\omega_o^2 L_{r'} C_r} \tag{5.3}$$

$$L_{r'} = L_r \left(\frac{C_r}{C_{r'}} - 1 \right) \tag{5.4}$$

Subsequently,

$$C_{r'} = \frac{3}{4} C_r = \frac{3}{4} \times 2.3pF = 1.72pF \tag{5.5}$$

Hence, if the capacitance value of the PMOS varactor is set equal to 1.5pF, we obtain,

$$L_{r'} = L_r \left(\frac{C_r}{C_{r'}} - 1 \right) = 3.2\times10^{-9} \times \left(\frac{2.3\times10^{-12}}{1.5\times10^{-12}} - 1 \right) = 1.70\text{nH} \tag{5.6}$$

5.1.4 Output buffer

Note that the parasitics associated with the bond pads may affect the performance of the VCO circuits, or even preventing them from oscillation. It is a common practice to insert a common-source stage (M3 and M4) for output buffer, as depicted in Figure 5.6.

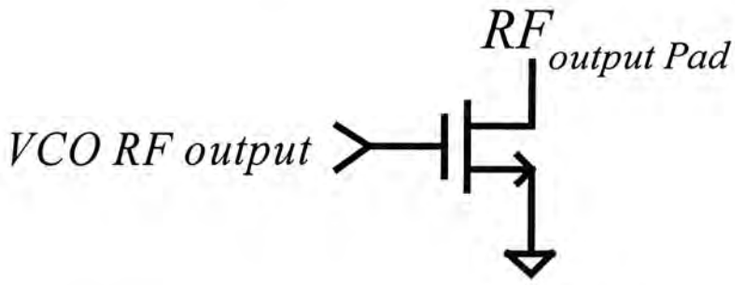


Figure 5.6 Common-source output buffer

5.1.5 Biasing Circuitry

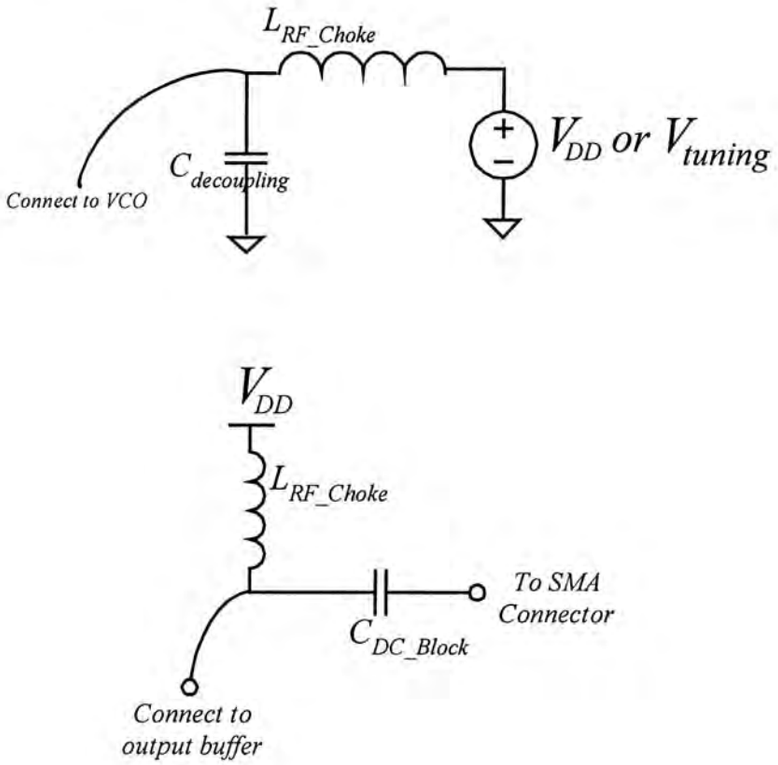


Figure 5.7 Biasing circuit of VCO circuits

Figure 5.7 shows the biasing networks for the VCO circuits. The RF choke presents a high impedance to high frequency signal and a low impedance DC path. The decoupling capacitor provides a proper RF ground at the required frequency range. The function of C_{DC_Block} is to prevent any DC voltage appearing at the output

from entering the measurement equipment. Surface-mount components of 10nH, 10μF and 2.5pF are chosen for L_{RF_Choke}, $C_{decoupling}$ and C_{DC_Block}, respectively.

5.2 Spiral Inductor Design

It has been reported that the GreenHouse's Method is rather accurate in estimating the inductance value of the spiral inductor. Some computer-aided design tools are also available for solving the respective calculations. ASITIC [30] (*Analysis of Si Inductors and Transformers for ICs*), a CAD tool that can be used to optimize the design of spiral inductors, is adopted here.

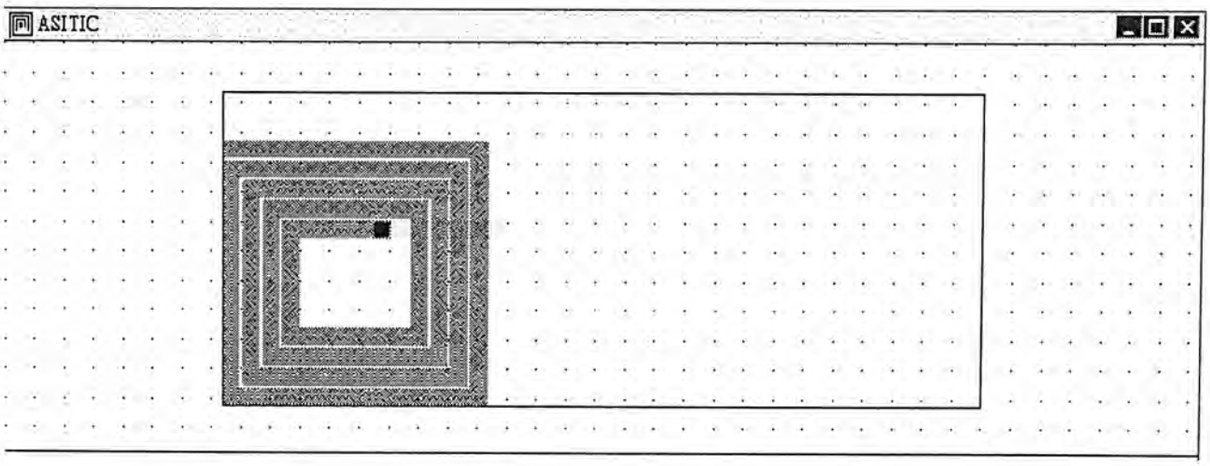


Figure 5.8 Screenshot of CAD tool – ASITIC

Figure 5.8 shows the screenshot of ASITIC. The required process parameters such as the layer thickness and the resistivity of the layer, are contained in a

technology file as input data, see Appendix B. Table 5.1 summaries the basic steps in creating the spiral inductor and extracting circuit model using ASITIC.

Steps	Action
1	Use command "sq" to start create rectangular spiral inductor
2	Type the name, inner dimension, no. of turn, metal width, metal-to-metal spacing, etc... of the spiral.
3	Type "ind <SpiralName>" to ask for inductance of the spiral. (i.e. The value of L_s)
4	Type "res <SpiralName>" to ask for total sheet resistance of the spiral. (i.e. The value of R_s)
5	Type "geom. <SpiralName>" to ask for all dimensions of the spiral. (i.e. Total length (l)

Table 5.1 Procedure of spiral inductor design using ASITIC

Once the dimensions of the spiral inductors are known, equation 4.3 can be used to calculate all element values in the lumped equivalent model of the spiral inductor. A matlab program is written for these calculations and the code is given in Appendix C.

Based on the process parameter provided by the foundry, we can create a technology file suitable for use by ASITIC. For example, the dimensions of a square spiral inductor of 3.2nH are given below:

- inner dimension = 180 micron
- number of turns = 3
- metal used = metal 3

- metal width = 12 micron
- metal-to-metal spacing = 1.5 micron

Then, by using the Matlab program, the parameter values in the equivalent inductor model are simply equal to:

$$R_s = 15.2\Omega$$
$$C_s = 21.0fF$$
$$C_{ox} = 140.2fF$$
$$C_{si} = 11.1pF$$
$$R_{si} = 719.7\Omega$$

5.3 Determination of W/L ratio of FET

Assuming the cross-coupled FETs are symmetrical, we can calculate the transconductance as follows:

$$\begin{aligned} \frac{g_m}{2} &\geq \alpha \times \text{Real}\{Y(\omega)\} \\ &= \frac{\alpha}{R_{p,total}} \\ &= \alpha \times \left(\frac{1}{R_l(Q_l^2+1)} + \frac{1}{R_c(Q_c^2+1)} + \frac{1}{R_p} \right) \end{aligned} \tag{5.7}$$

In many cases, the value of α is set between 1 to 2 so as to ensure start-up oscillation. Since the quality factor of CMOS varactors(>20) is usually much higher than spiral inductors, it is reasonable to assume that $\frac{1}{R_c(Q_c^2+1)} \approx 0$.

As a result, we have

$$g_m \geq \frac{2\alpha}{R_l(Q_l^2+1)} \tag{5.8}$$

At an oscillating frequency of 1.5GHz, the unloaded quality factor of the spiral inductor is thus given by,

$$Q_l = \frac{2\pi \times (1.5\times 10^9) \times 3.2\times 10^{-9}}{15.2} = 1.98 \tag{5.9}$$

For safety reason, we set $\alpha = 1.5$, which gives,

$$g_m \geq \frac{2\times 1.5}{15.2\times(1.98^2+1)} = 40.1mS \tag{5.10}$$

Subsequently, with V_{dd} = 1.5V, the size of the NMOS transistor can be evaluated by,

$$\frac{W}{L} = \frac{g_m}{\mu C_{ox}(V_{GS}-V_T)} = \frac{0.0401}{1.18\times 10^{-4}\times(1.5-0.7)} = 424.92 \tag{5.11}$$

For L = 0.6μm, the width of the active device should be set equal to 250μm.

5.4 Varactor Design

The physical dimensions of the PMOS varactor may be estimated from the lowest tuning capacitance value required in the VCO design. It is very difficult to determine the exact capacitance value of the varactor by using simple formulas, and therefore we will leave this calculation to the simulation program.

In the reference VCO design, the total tank capacitance required is approximately 3.5pF for an oscillation frequency of 1.5GHz. This capacitance consists of the spiral inductor to substrate capacitance (0.2pF), varactor capacitance and the parasitics of the FET. For NMOS transistor with a gate-length of 0.6μm and a gate-width of 250μm, the parasitic capacitance which consists of the gate-drain, drain-bulk and gate-source capacitances may be calculated by,

$$\begin{aligned} C_{\text{FET Parasitic}} &= 250\mu m \times 4fF/\mu m \\ &= 1pF \end{aligned} \tag{5.12}$$

Consequently, the capacitance value of the varactor is simply,

$$\begin{aligned} C_r &= 3.5\text{pF} - C_{Inductor\ Parasitic} - C_{FET\ Parasitic} \\ &= 3.5pF - 0.2pF - 1pF \\ &= 2.3pF \end{aligned} \tag{5.13}$$

By using the circuit simulator, the gate-width of the varactor is found to be 250μm, based on the 0.6μm CMOS technology.

Similarly, for the proposed VCO circuit, a capacitance value of 1.5pF is required which corresponds to a PMOS varactor with a gate-width of 150μm.

5.5 Layout (Cadence)

Cadence® is an electronic design automation (EDA) software technology that help to design and develop integrated circuits (ICs) and systems. In this work, Cadence® is employed to prepare the IC schematics and layout (Figure 5.9 and 5.10). This

software can also be used to do design rule check, and to generate the circuit netlist for further simulations.

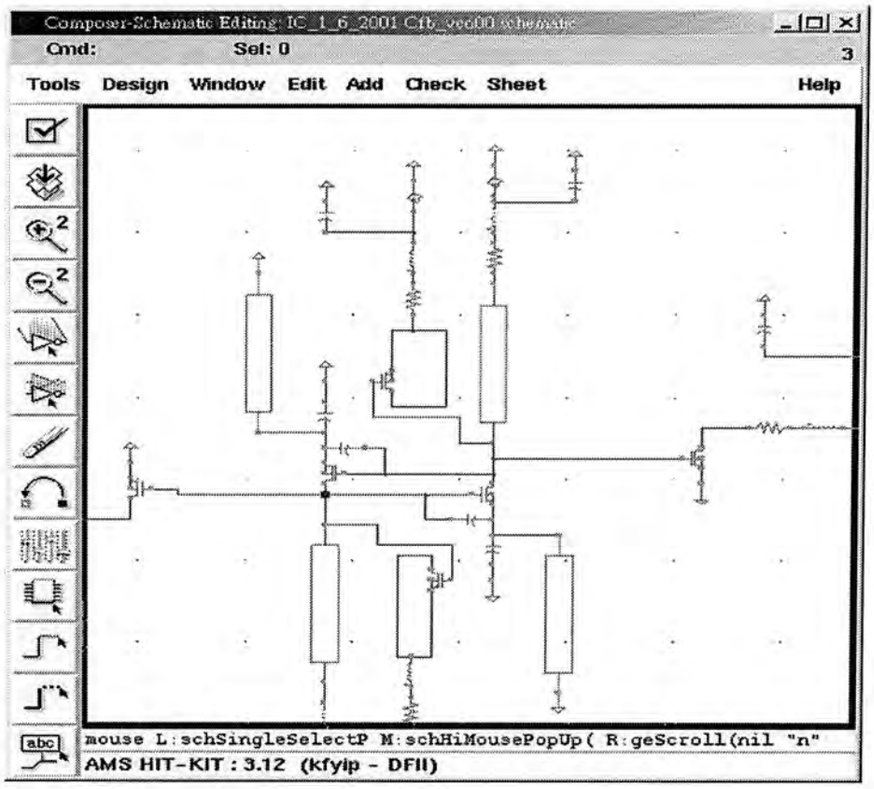


Figure 5.9 Screenshot of Schematic of Cadence®

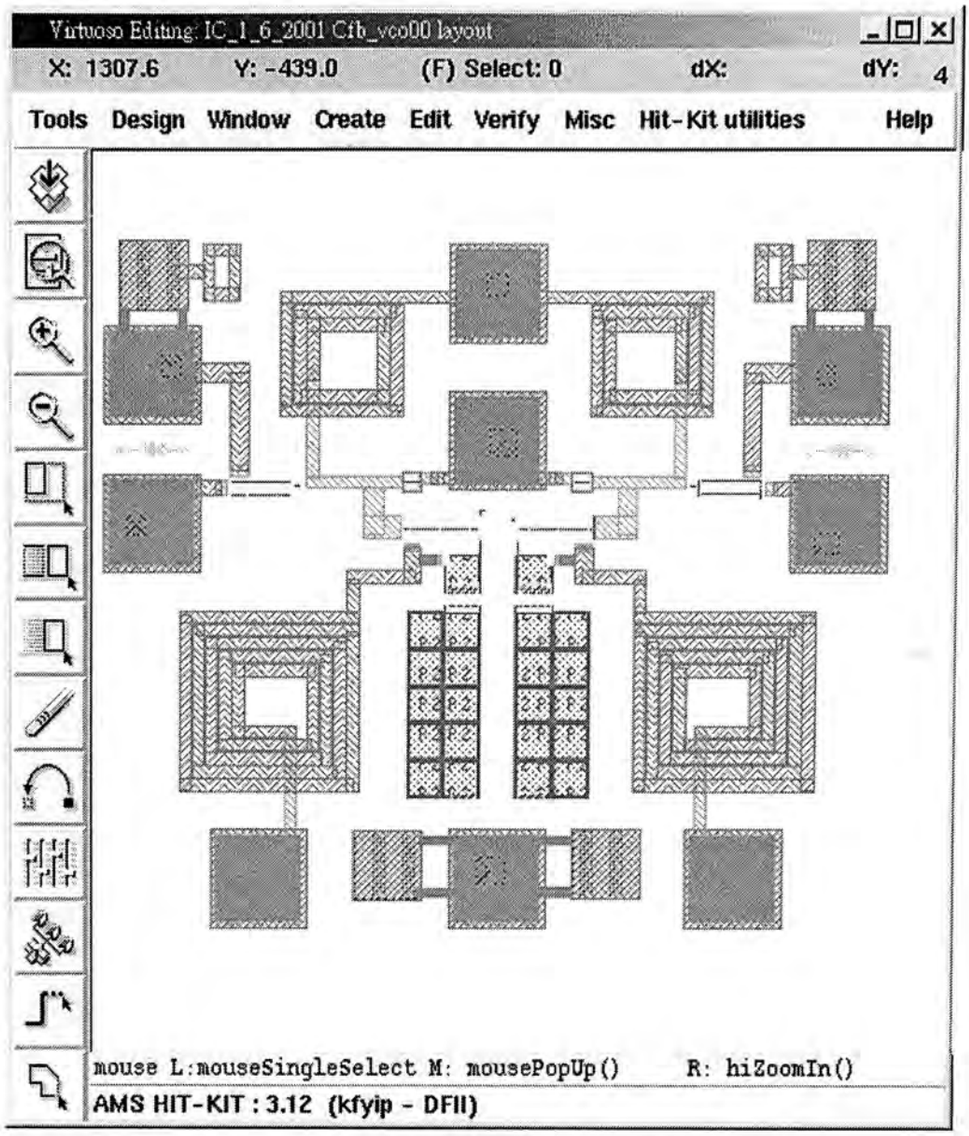


Figure 5.10 Screenshot of Layout of Cadence®

In CMOS circuit design, dimensions in a layout are governed by "design rules", which is imposed by both lithography and processing capabilities of the technology. Thus, each foundry will have its own design rules for the designer, to guarantee proper fabrication. Some major design rules are listed below:

- Minimum Width
  - For example, polysilicon width should not be less than 0.6μm for 0.6μm CMOS process technology. Otherwise, it may simply break or suffer from

a large local resistance.

- Minimum Spacing
  - For example, the spacing between two polysilicon lines should not be less than 0.8μm, otherwise, they may be shorted.

- Minimum Enclosure
  - For example, the n-well and the p^+ implant should surround the transistor with margin larger than 0.8μm in order to guarantee the formation of PMOS transistor.

- Minimum Extension
  - For example, gate polysilicon must have a minimum extension of 3μm beyond the active area to ensure proper transistor action at the edge.

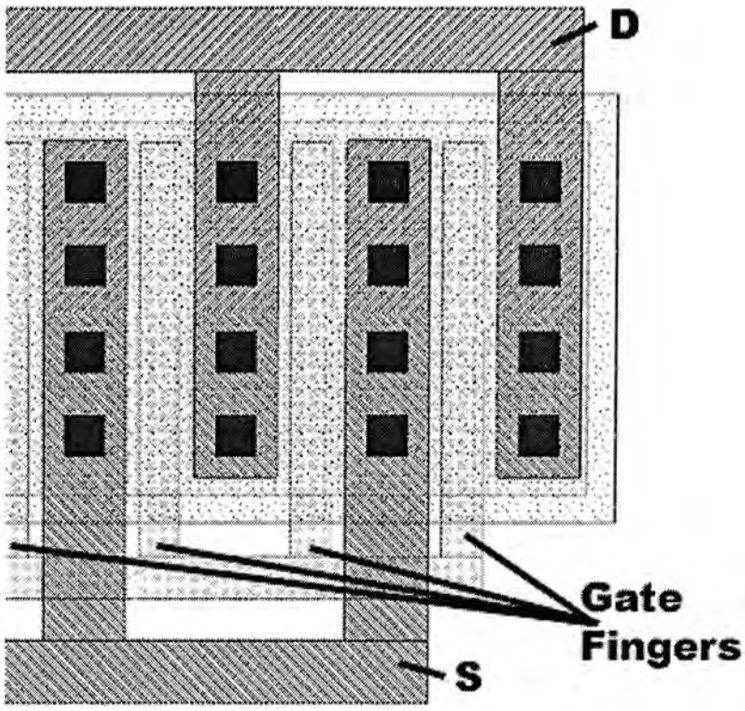


Figure 5.11 Layout of a transistor using multi-fingers

Furthermore, for the design of wide transistors, "multfinger" structure (Figure 5.11), should be adopted to lower the internal resistance associated with the gate fingers. It is a common practice to set the gate resistance lies between 1/5 and 1/10 of $1/g_m$, for low-noise applications. Gate resistance of FET can be calculated by,

$$R_g = \frac{W}{L} \times \frac{R_{sh}}{3N^2} \tag{5.14}$$

where

W is total FET width,

L is the channel length,

R_{sh} is the polysilicon sheet resistance,

N is number of gate fingers in FET

Therefore, for an FET of W/L ratio equals 250/0.6. The minimum number of gate fingers required may be calculated as,

$$N \geq \sqrt{\frac{W}{L} \times \frac{R_{sh}}{3R_g}} = \sqrt{\frac{W}{L} \times \frac{R_{sh}}{3} \times 5g_m}$$

$$= \sqrt{\frac{250}{0.6} \times \frac{0.2 \times \frac{250}{0.6}}{3} \times 5 \times 40.1mS} \approx 48$$

5.6 Circuit Simulation (SpectreRF)

Spectre is an advanced circuit simulator that simulates analog and digital circuits at the differential equation level. The simulator uses improved algorithms that offer higher simulation speed and better convergence characteristics over SPICE. Besides the basic capabilities, the Spectre circuit simulator provides additional capabilities such as the efficient calculation of the operating point, transfer function, noise, and distortion of electronic circuits. Figure 5.12 illustrates the simulated transient response of the voltage-controlled oscillator designed.

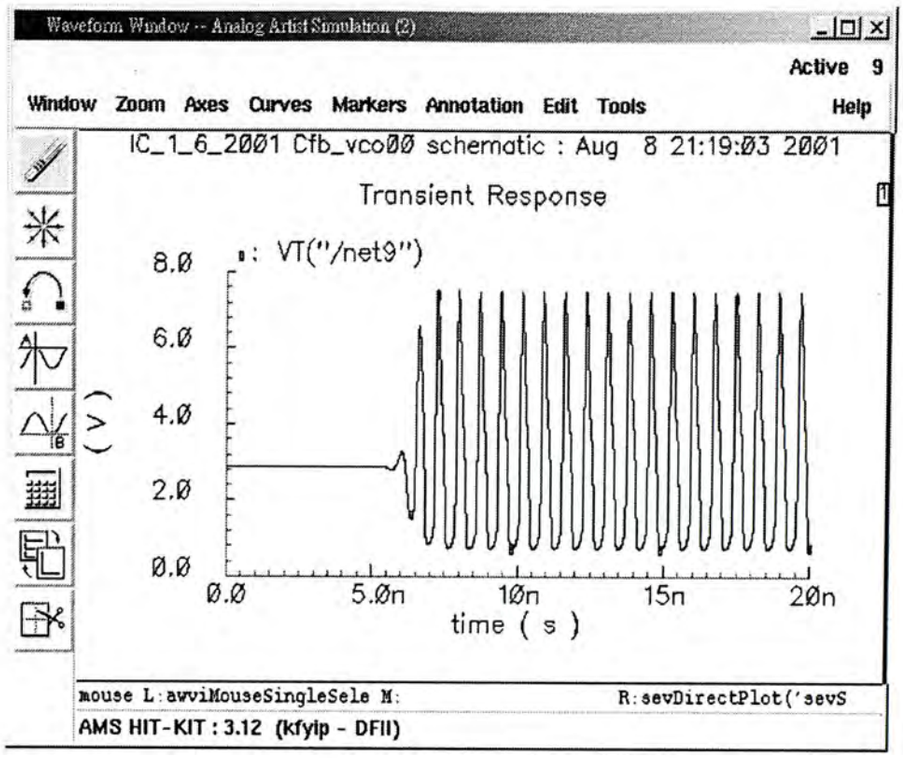


Figure 5.12 The plot of simulation result in "Waveform Window"

Chapter 6 Experimental Verification

6.1 Measurement Setup

The designed VCO circuits were fabricated using tri-metal 0.6μm CMOS process. For measurement purposes, the chip is mounted on top of a PCB and connected to the microstrip lines by using bondwires, as shown in Figure 6.3.

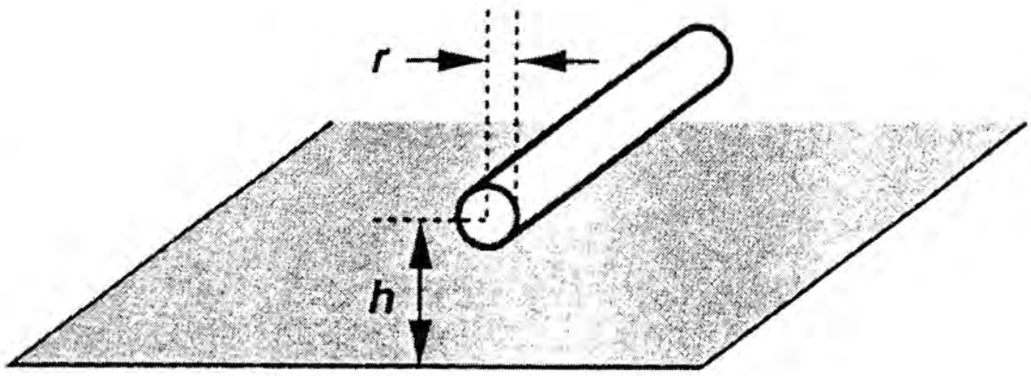


Figure 6.1 Geometry of bondwire

When the round bondwire is located above a ground plane, as shown in Figure 6.1, the self-inductance is governed by [31],

$$L \approx 0.2 \ln \frac{2h}{r} \text{ nH/mm} \tag{6.1}$$

which amounts to roughly 1nH/mm for typical bond wires. The effective resistance per length of bondwire can be by calculated by [27]:

$$\frac{R}{l} \approx \frac{1}{2\pi r \delta \sigma} \tag{6.2}$$

Typically, the resistance of bondwire at 1GHz is about 125mΩ/mm.

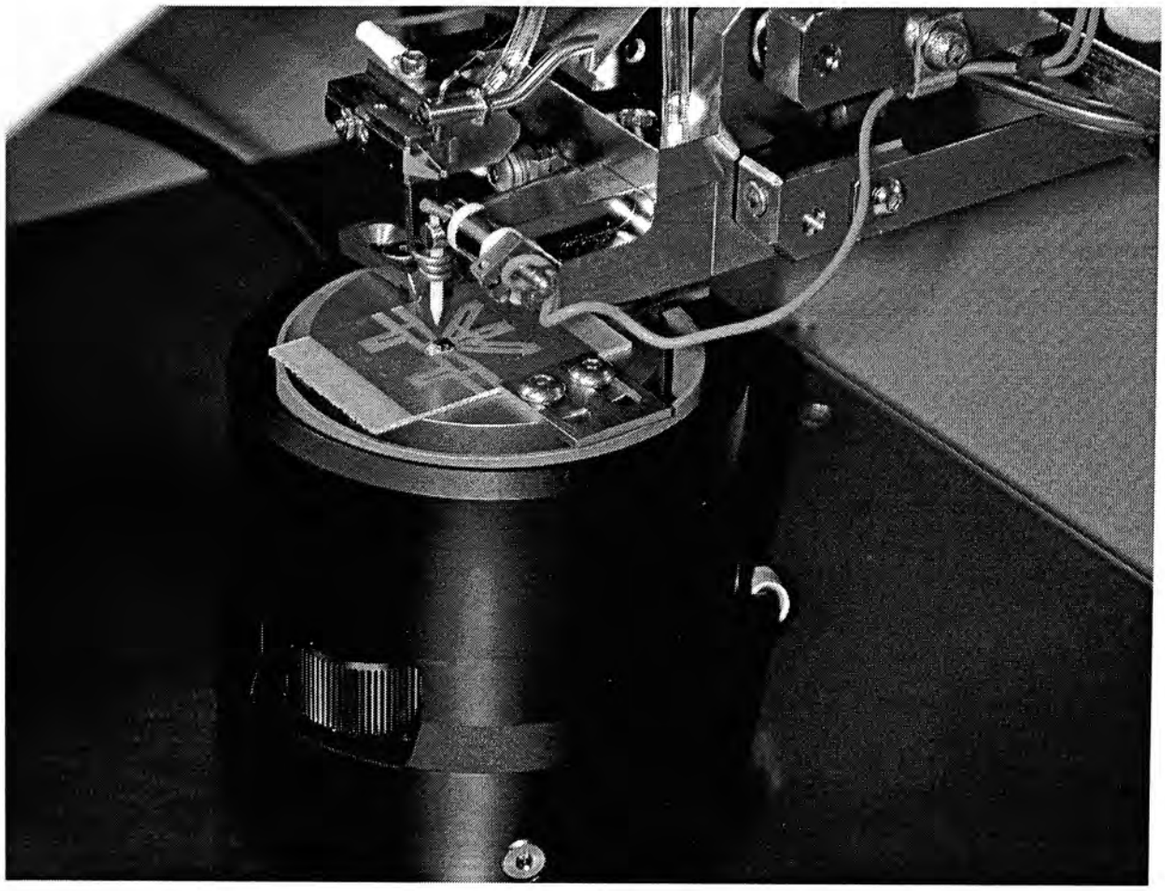


Figure 6.2 Diagram of bonding machine

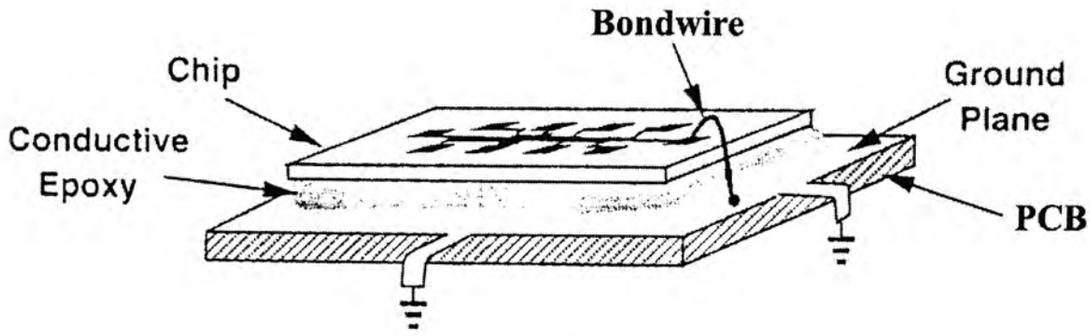


Figure 6.3 Mounting of IC on PCB substrate

The printed circuit boards used in these experiments are made from double-sided FR4 material. One side of the board is used as the ground plane whereas the other side is used for mounting the die and the necessary external components, as depicted in Figure 6.4 and 6.5.

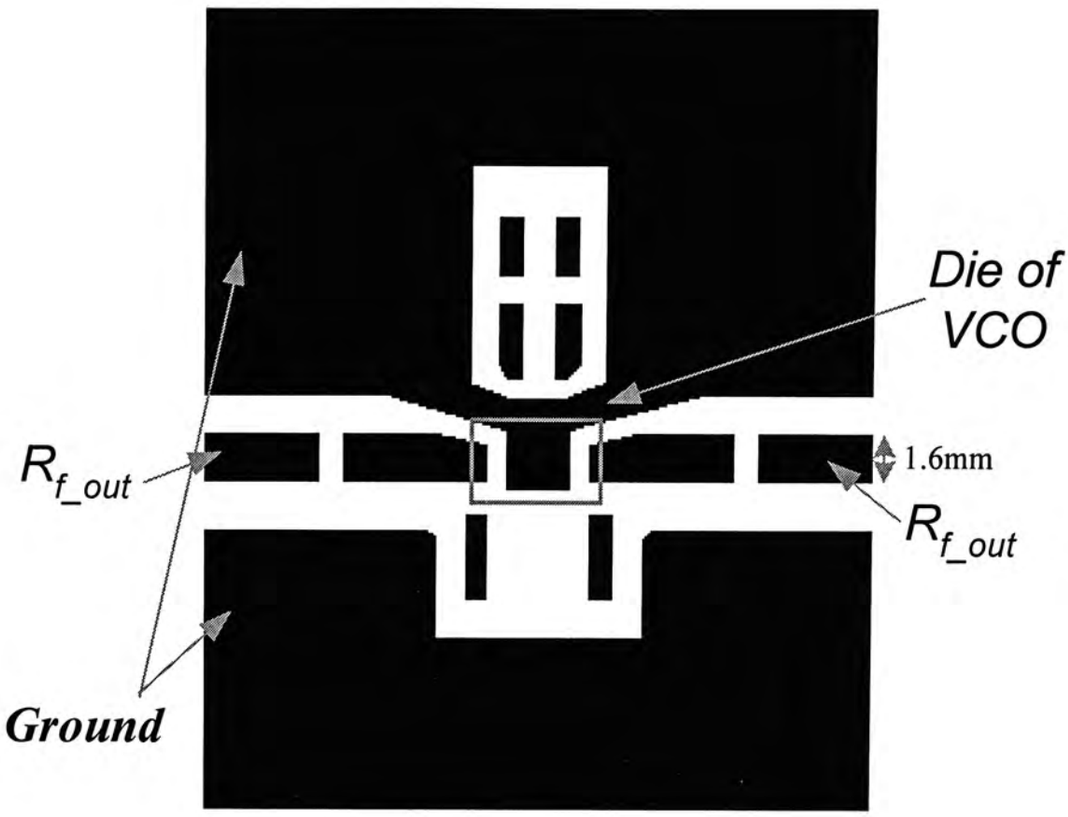


Figure 6.4 Printed Circuit Board of the CMOS VCO

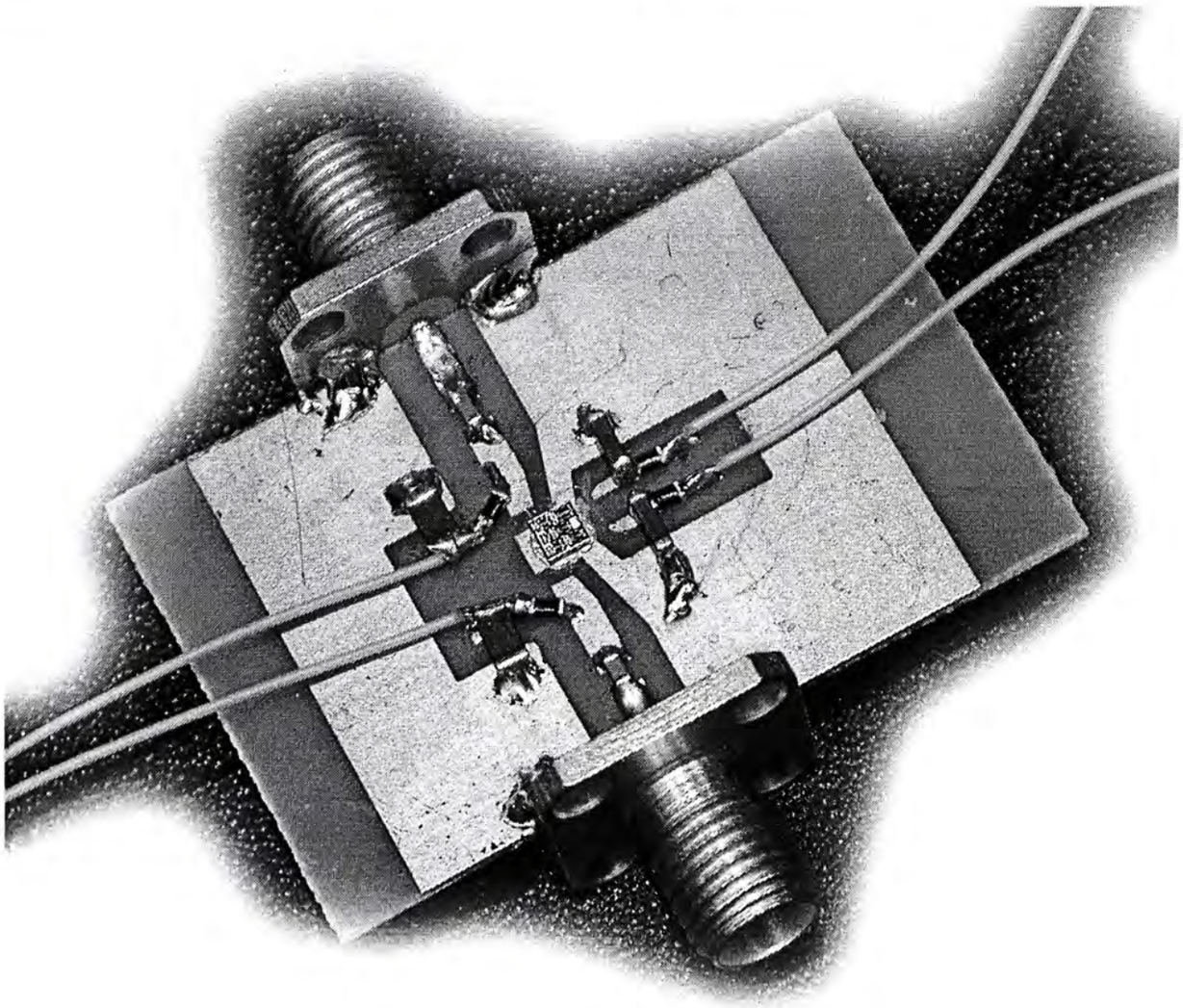


Figure 6.5 Constructed VCO circuit

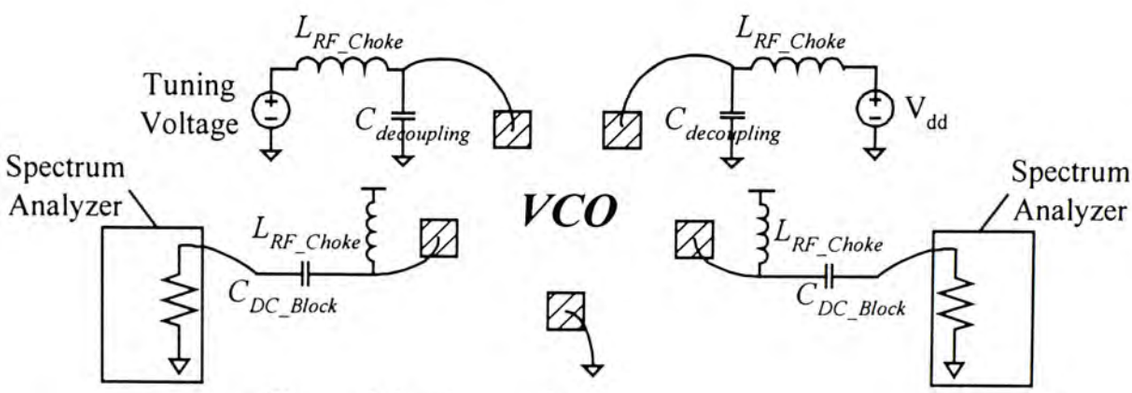


Figure 6.6 A complete measurement setup

Figure 6.6 shows the complete measurement setup employed for testing the CMOS VCO circuits. In the diagram, a spectrum analyzer HP4396A is used to determine the output power, power spectrum, harmonic content and the frequency of

oscillation. All phase noise characterization were a performed with a dedicated VCO/PLL signal Test System (HP4352B), as shown in Figure 6.7.

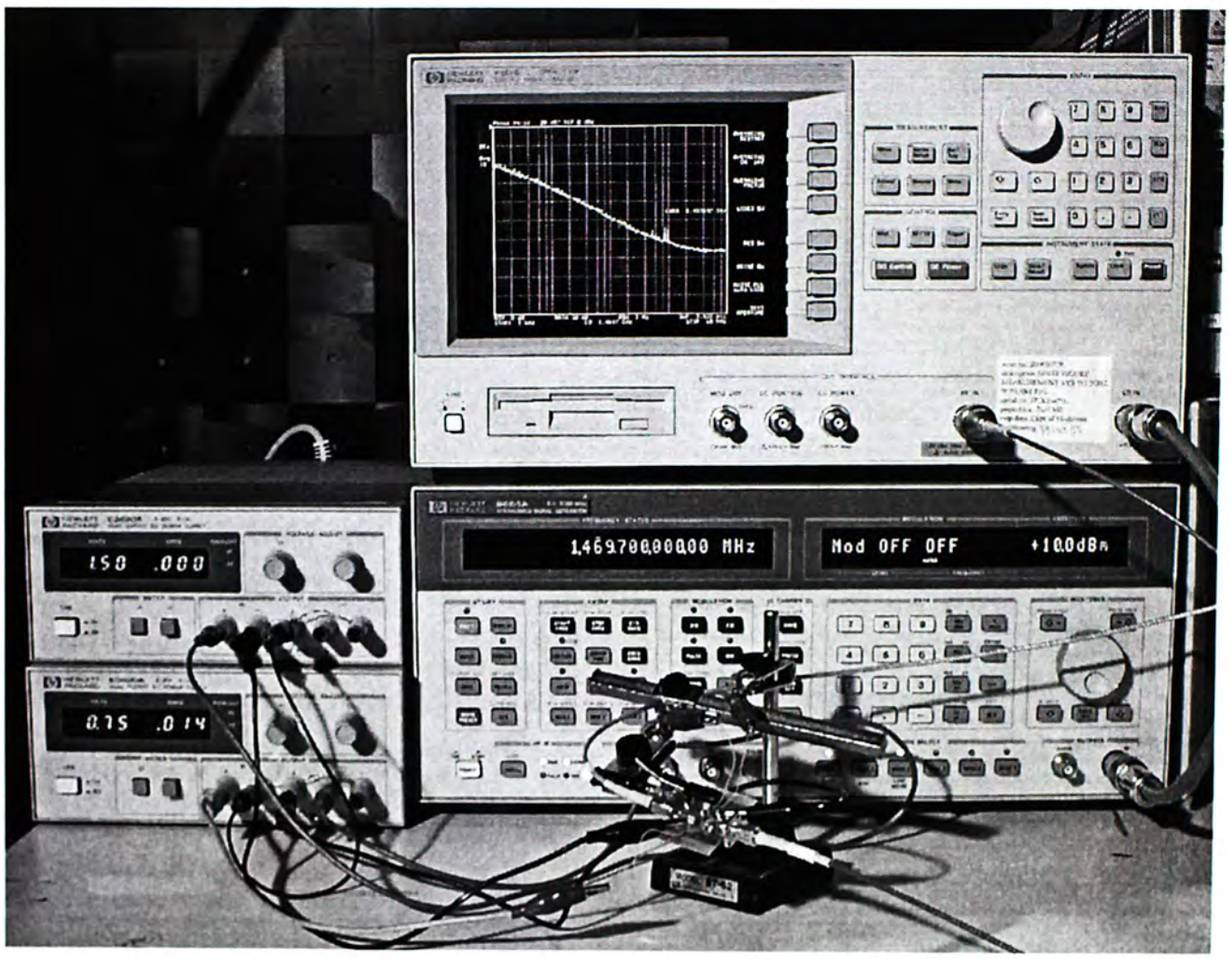


Figure 6.7 Phase noise measurement setup

6.2 Measurement results: Reference Oscillator Circuit

6.2.1 Output Spectrum

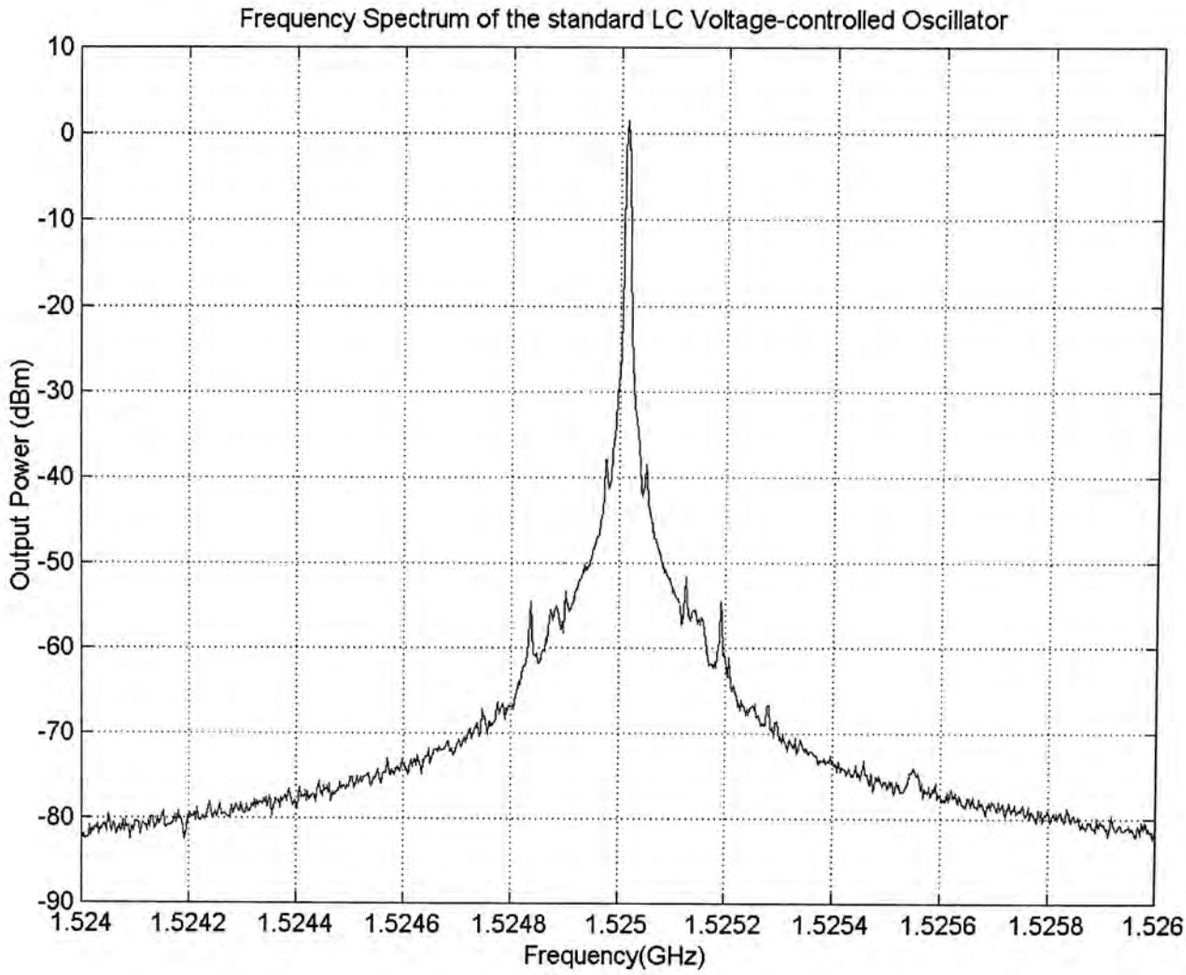


Figure 6.8 Frequency spectrum of the reference VCO circuit

Figure 6.8 shows the measured frequency spectrum of the reference LC differential CMOS voltage-controlled oscillator fabricated. The tuning voltage and supply voltage of the VCO are 0.85V and 1.5V, respectively. The circuit can deliver 1.5dBm output power at an oscillating frequency of 1.525 GHz. Moreover, the power level of the second harmonic (3.05GHz) is approximately –17.2dBm.

6.2.2 Phase Noise Performance

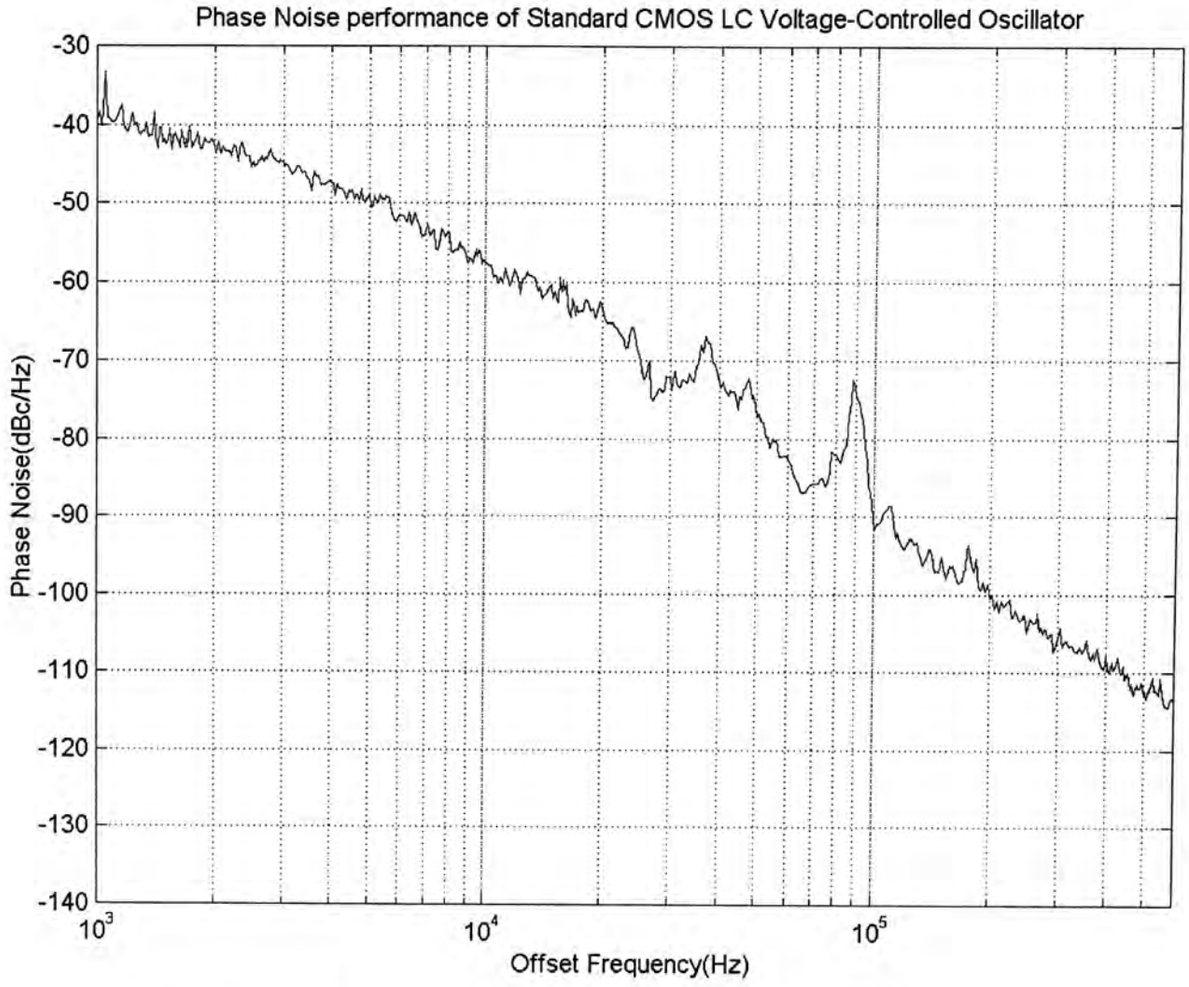


Figure 6.9 Phase Noise spectrum of reference VCO circuit

Figure 6.9 shows the measured phase noise spectrum of the reference VCO. When the VCO is operated at 1.525 GHz, the phase noise level of the circuit is found to be approximately –114dBc/Hz at offset frequency of 600kHz. The phase noise performance was achieved at a power consumption of roughly 15mA from a 1.5V power supply.

6.2.3 Tuning Characteristic

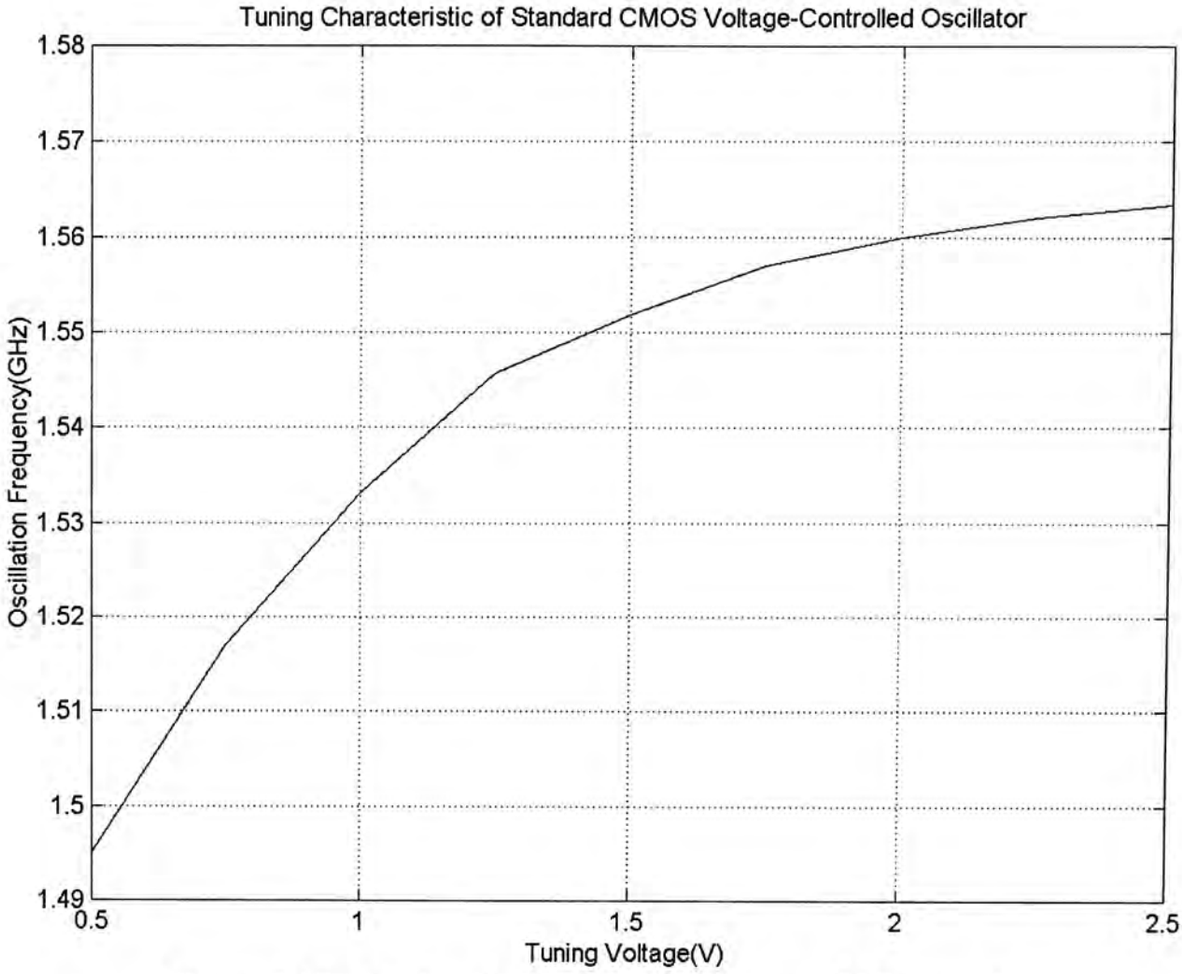


Figure 6.10 Tuning characteristic of reference VCO circuit

Figure 6.10 shows the frequency tuning characteristic of the reference VCO circuit. The oscillating frequency varies from 1.495GHz to 1.563GHz, cover a bandwidth of almost 70MHz, when the tuning voltage is changed from 0.5V to 2.5V. The poor tuning linearity of the VCO is mainly due to the nonlinear capacitance of the PMOS varactor, particularly when the device is driven from deep accumulation to deep depletion region.

6.2.4 Microphotograph

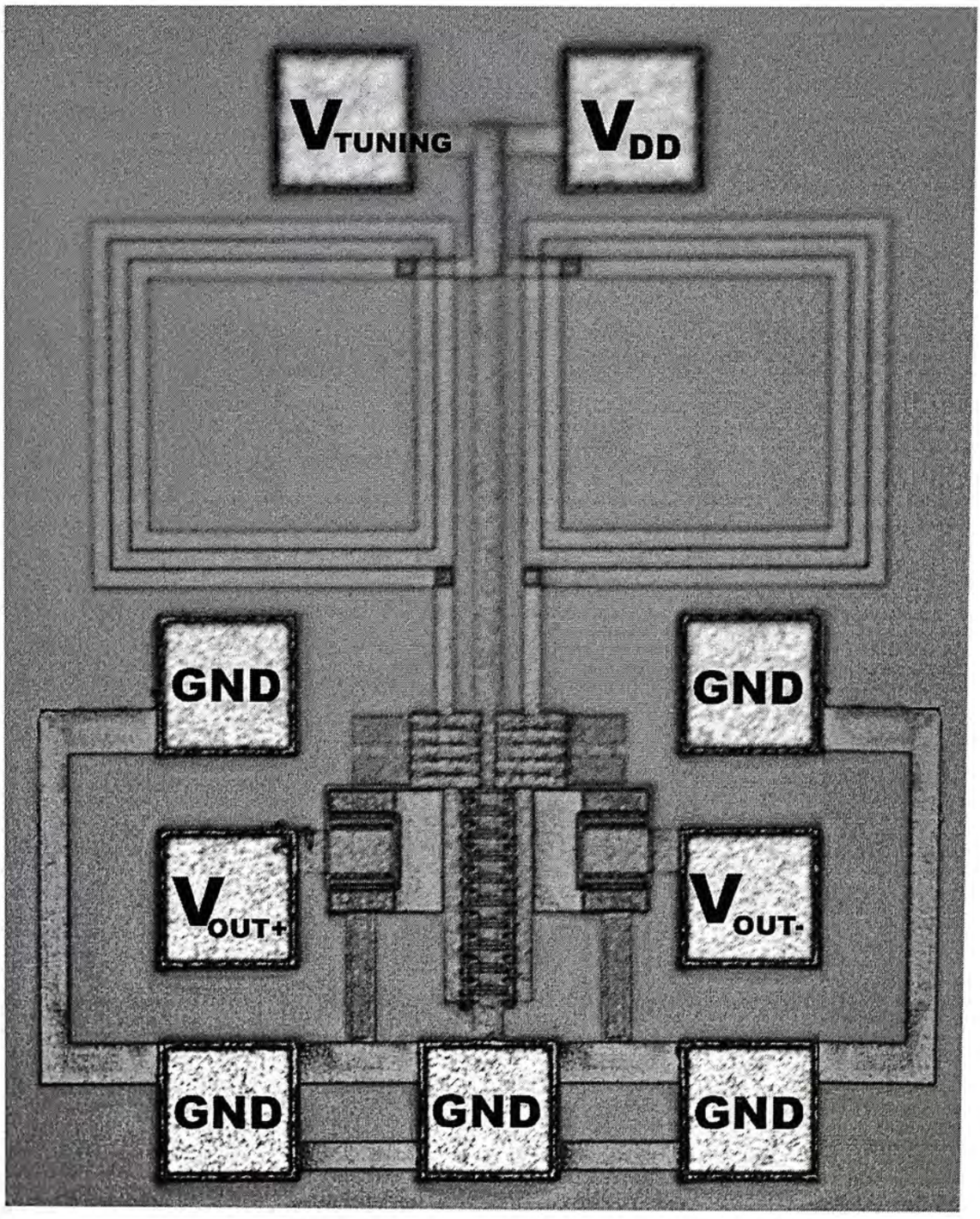


Figure 6.11 Microphotograph of the reference VCO Circuit

Microphotograph of the VCO circuit is presented in Figure 6.11. The dimension of the circuit is measured to be 0.81 mm x 0.63 mm. These VCO circuits are realized using 0.6μm standard digital CMOS process with three metal layers.

6.3 Measurement results: Proposed Oscillator Circuit

6.3.1 Output Spectrum

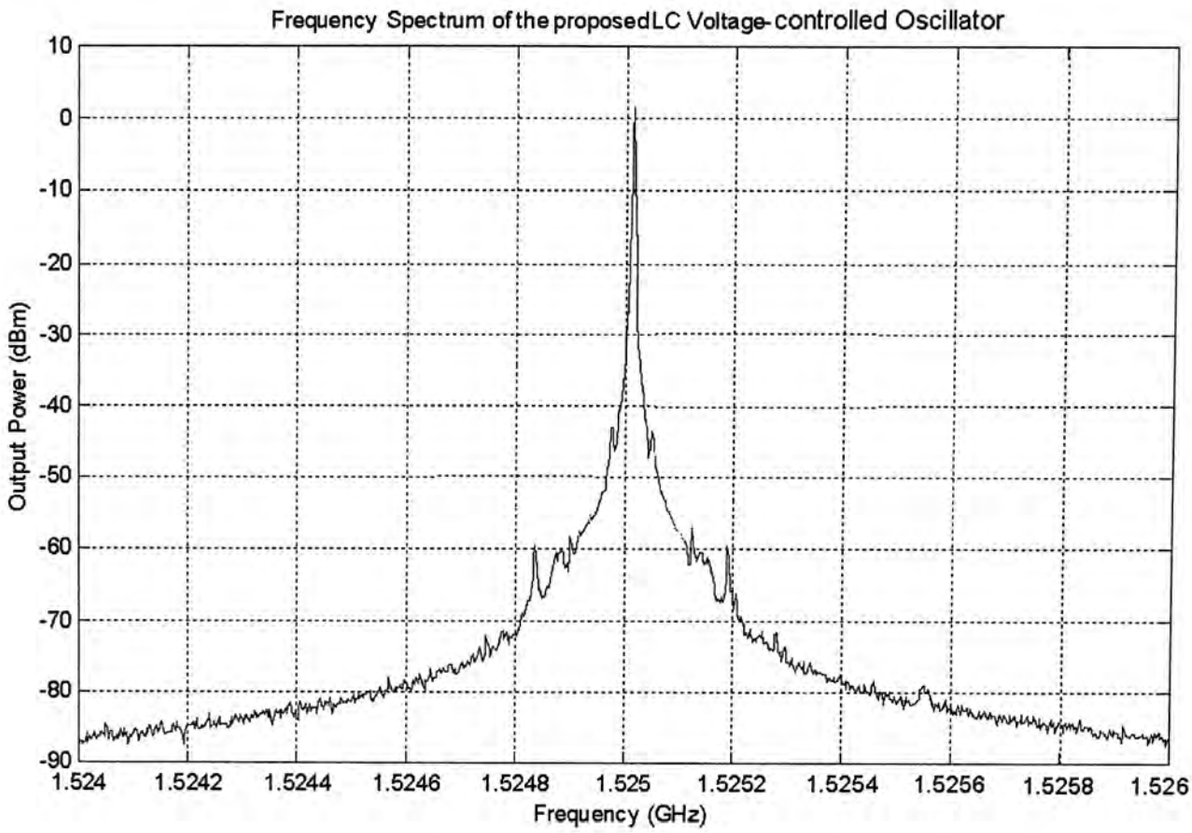


Figure 6.12 Frequency spectrum of proposed VCO circuit

Figure 6.12 shows the frequency spectrum of proposed LC differential CMOS voltage-controlled oscillator. The circuit delivers 1.5dBm output power at an oscillating frequency of 1.525GHz. The tuning and supply voltages are set equal to 0.85V and 1.5V, respectively. Moreover, the power level of the second harmonic (3.05GHz) is approximately –22.1dBm.

6.3.2 Phase Noise Performance

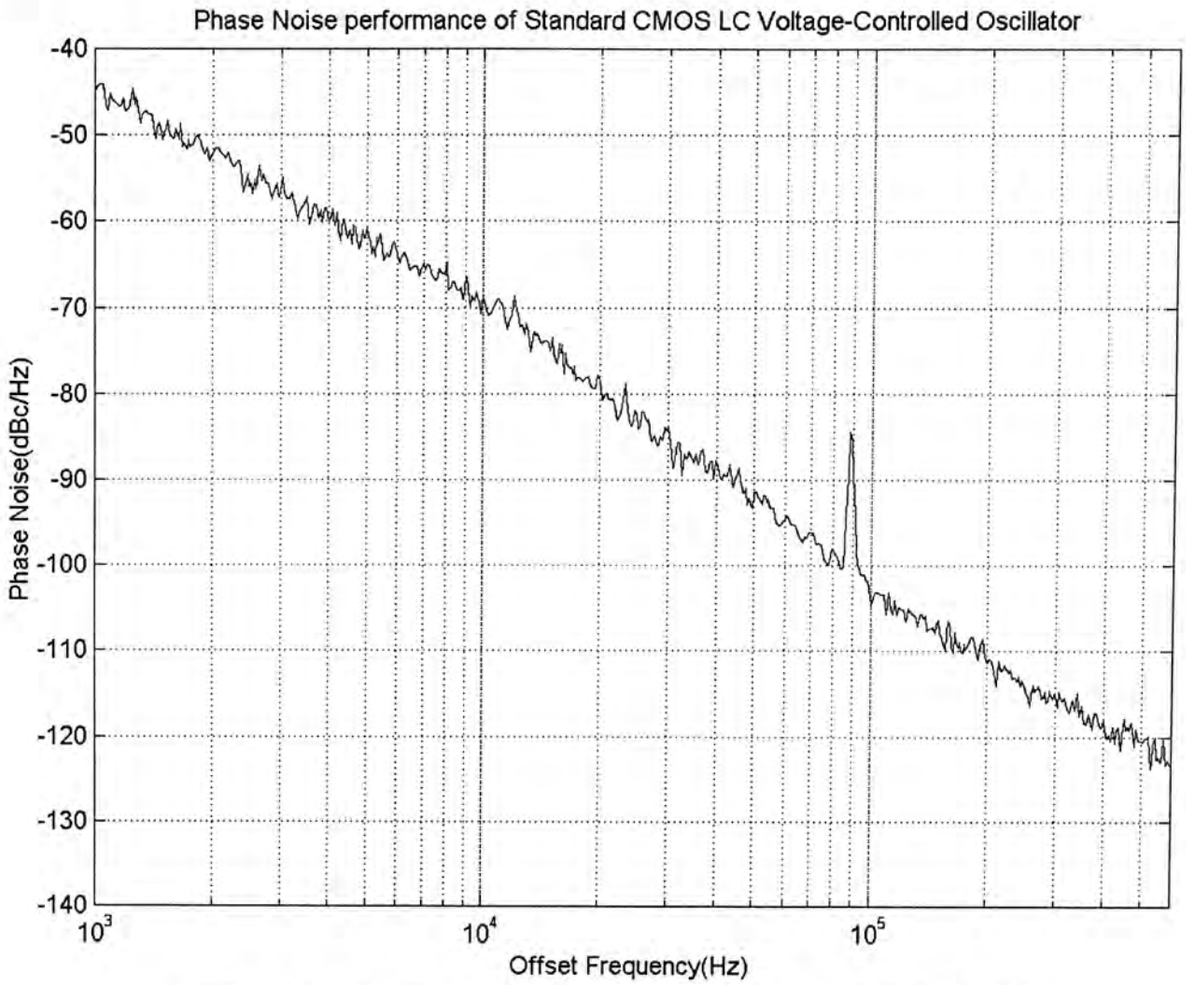


Figure 6.13 Phase Noise spectrum of proposed VCO circuit

Figure 6.13 shows the measured phase noise spectrum of the proposed VCO. The phase noise level of the circuit is measured to be approximately –123dBc/Hz at offset frequency of 600kHz, with an oscillation frequency of 1.525 GHz.

6.3.3 Tuning Characteristic

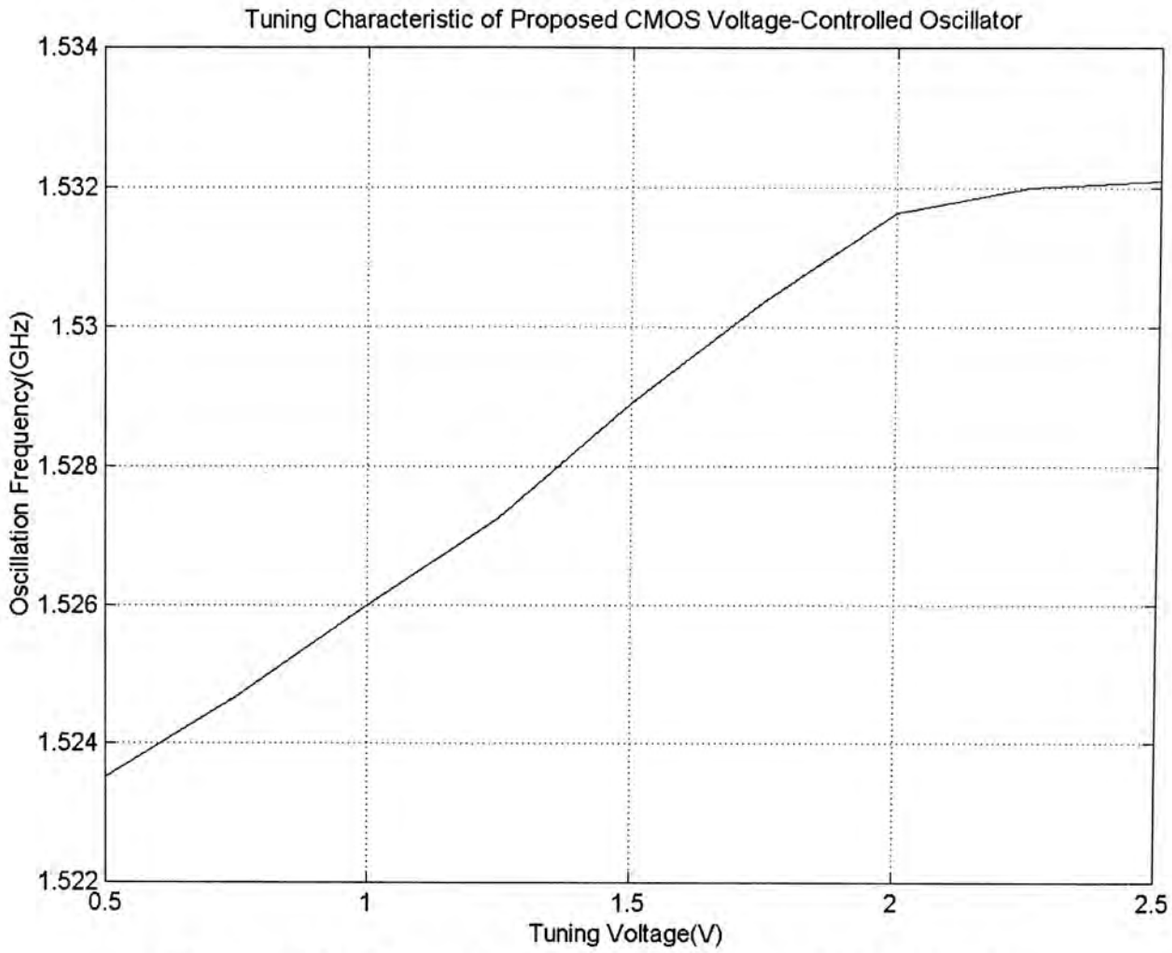


Figure 6.14 Tuning characteristic of proposed VCO circuit

Figure 6.14 shows the frequency tuning characteristic of the proposed VCO circuit. The tuning range is 1.5235GHz to 1.5322GHz, for a tuning voltage of 0.5V to 2.5V. The poor tuning linearity of the VCO is mainly due to the nonlinear capacitance of the PMOS varactor, particularly when the device is driven from deep accumulation to deep depletion.

6.3.4 Microphotograph

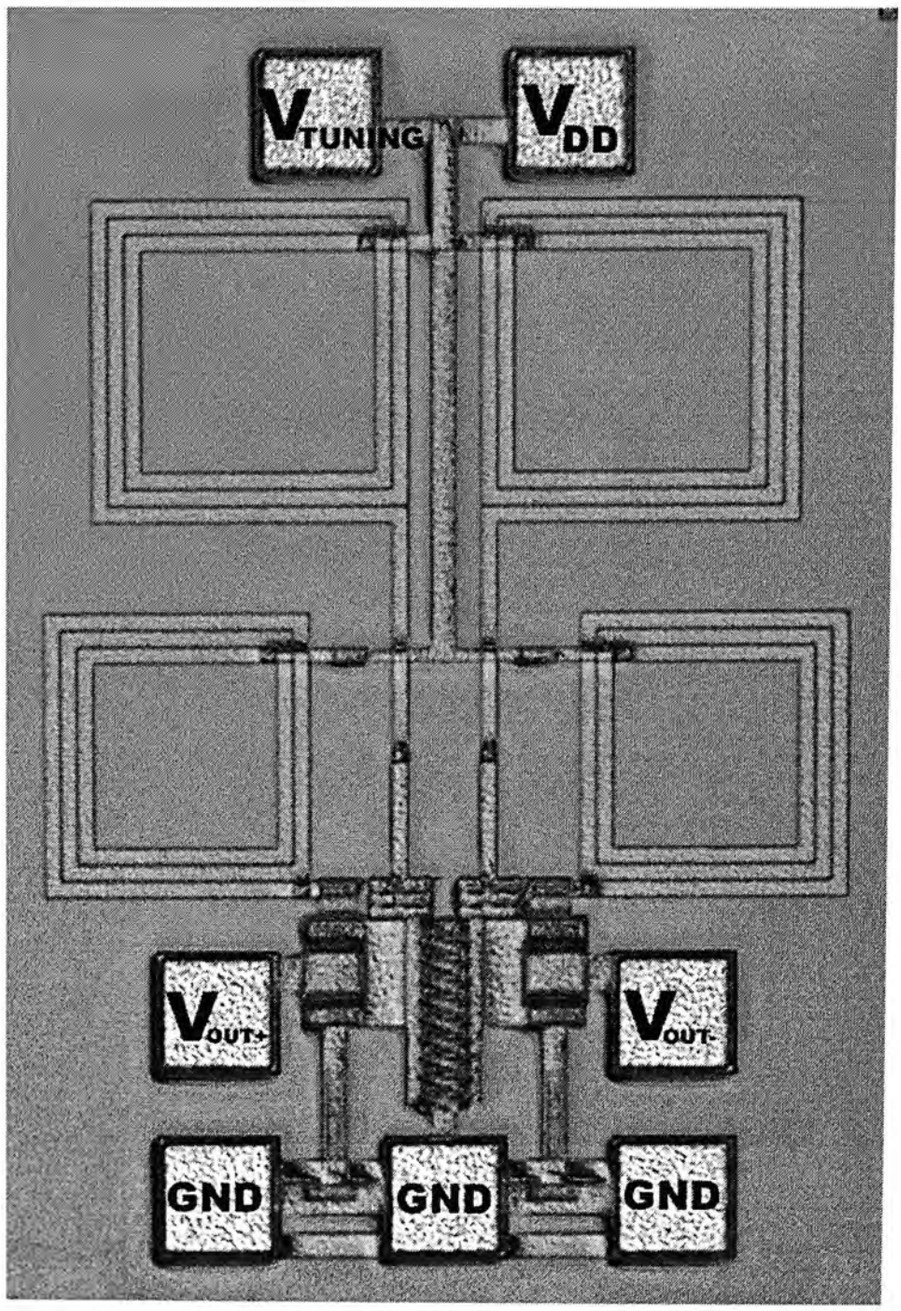


Figure 6.15 Microphotograph of proposed VCO Circuit

Microphotograph of the proposed VCO circuit is given in Figure 6.15. The physical size of the circuit is measured to be 0.92 mm x 0.71 mm. These VCO circuits are realized using 0.6μm standard digital CMOS process with three metal layers.

6.4 Performance Evaluation

6.4.1 Phase Noise Performance

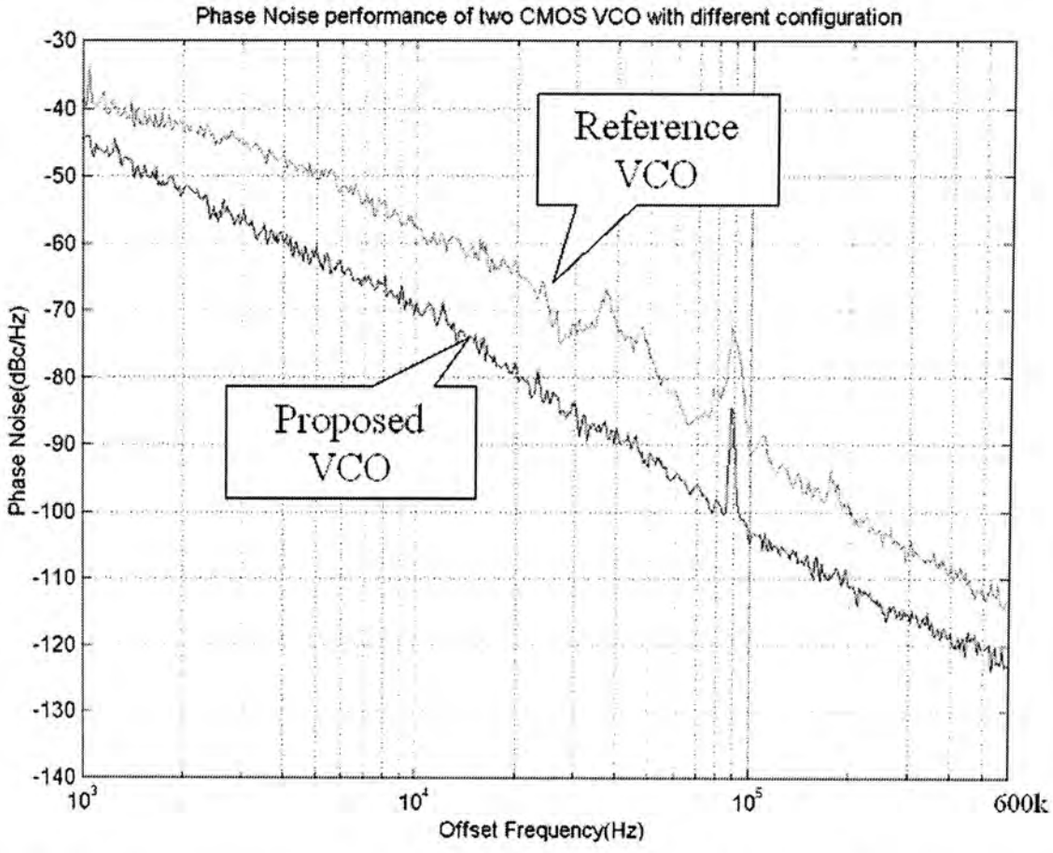


Figure 6.16 Comparison of phase noise performance between the reference and proposed VCO circuits

Figure 6.16 shows the phase noise performance of the reference and proposed VCO circuits, at an oscillating frequency of 1.525 GHz. The measured phase noise levels of the reference and proposed VCO circuits are respectively, –114dBc/Hz and –123dBc/Hz, at offset frequency of 600kHz. The results indicate that the phase noise level is improved by 7-10dB, over an offset frequency range from 1kHz to 600kHz. The phase noise spectrum of the proposed VCO exhibits a slope of roughly 30dB/dec, in the range from 10KHz to 100KHz, and a slope of approximately 25 dB/dec in the range from 100KHz to 600KHz.

6.4.2 Tuning Characteristic

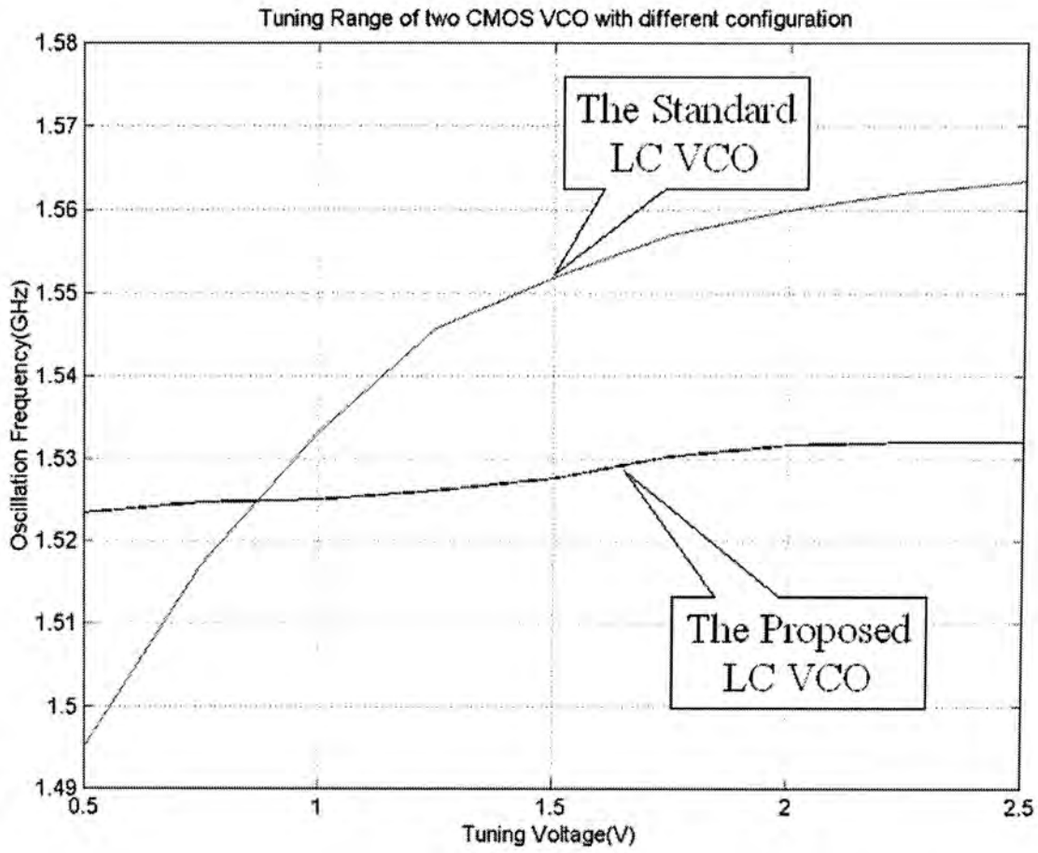


Figure 6.17 Comparison of frequency tuning characteristics between the reference and proposed VCO circuit

Figure 6.17 shows the frequency tuning characteristics of both the reference and proposed VCO circuits. We can see that the tuning range of the reference design is much wider than the proposed one, under the same operating voltage. Table 6.1 summaries the measured characteristics of the reference and proposed VCO circuits, including phase noise, power consumption and tuning range.

	Reference VCO	*Proposed VCO*
Supply Voltage (V)	*1.5*	*1.5*
Power Consumption (mW)	*22.5*	*22.5*
Tuning Range (GHz)	*1.495 – 1.563*	*1.523 – 1.532*
Phase Noise @600kHz offset frequency	*-114*	*-123*
Second harmonic power (dBm)	*-17.2*	*-22.1*

Table 6.1 Summary of measurement results

Moreover, the comparison between the phase noise performance of the proposed circuit and some of the published (Bi) CMOS VCO designs using integrated inductors (unless otherwise stated), are tabulated in Table 6.2 for reference.

Year	*Freq (GHz)*	*Phase Noise (dBc/Hz)*	*Power*	*Technology*
2000 [32]	*1.79 - 2.00*	*-125@600kHz*	*1.8V 19mA*	*Three-metal-layer 0.65μm BiCMOS*
2000 [33]	*1.10 - 1.45*	*-119@600kHz*	*2.0V 6mA*	*0.35μm CMOS (bond wire)*
2000 [34]	*1.10 - 1.20*	*-126@600kHz*	*2.7V 5mA*	*0.8μm CMOS (bond wire)*
2001 [35]	*1.00 - 1.20*	*-130@600kHz*	*2.5V 3.7mA*	*Four-metal-layer 0.6μm BiCMOS*
2002 [36]	*1.69 - 1.96*	*-123@600kHz*	*2.0V 6mA*	*0.35μm CMOS (discrete capacitor required)*
This Work	*1.52 - 1.53*	*123@600kHz*	*1.5V 15mA*	*Three-metal-layer 0.6μm CMOS*

Table 6.2 Comparison of published results

In summary, the improved phase noise of proposed voltage-controlled oscillator is mainly contributed by the following design methods:

1. Enhanced effective quality factor of the modified resonant tank configuration. However, according to the derived results, the reduction in phase noise is limited by the Q factor of the additional inductor.

2. The series-tuned LC tank exhibits low impedance at twice the fundamental oscillating frequency and strongly suppresses the amplitude of the second harmonic voltage. As a result, the up-conversion of noise due to spectrum folding is greatly reduced.

3. The measurement results indicate that the frequency tuning ranges of the reference and proposed VCO topologies are roughly 3.4% and 0.5% respectively. The reasons for the narrow tuning range are due to the large parasitic capacitances associated with the tank circuit as well as the small capacitance tuning range of varactors.

Chapter 7 Conclusion and Future Work

7.1 Conclusion

This thesis illustrates the design of monolithic CMOS voltage-controlled oscillator with low phase noise characteristics. These oscillators are fabricated using three-metal-layer 0.6μm CMOS process and integrated planar inductors. We also present the necessary information for the implementation of CMOS oscillator including the design of the NMOS transistors, inductors, and PMOS varactors. Furthermore, techniques to reduce phase noise in CMOS VCO circuits are proposed and validated experimentally.

Two voltage-controlled oscillators have constructed and tested. The first one is a LC differential voltage-controlled oscillator using a simple LC tank topology. It operates at 1.5V supply voltage with a drain current of 15mA. It has a wide tuning range, from 1.495GHz to 1.564 GHz. The tuning sensitivity is 34.5MHz/V. The phase noise level is approximately –114dBc/Hz at 600kHz offset frequency.

The second design is a LC differential voltage-controlled oscillator with a modified tank circuit. It also operates at 1.5V supply voltage with 15mA drain

current. It has a narrow tuning range from 1.523GHz to 1.533GHz. The tuning sensitivity is only 5MHz/V. However, the phase noise performance is better than –123dBc/Hz at 600kHz offset frequency. The measured phase noise exceeds the most stringent specification for DCS-1800 systems.

7.2 Future Work

In this research, the tri-metal 0.6μm CMOS process is used for the fabrication of the oscillator circuits. However, 0.13μm CMOS process is now very popular in ASIC design and it is well known that CMOS device with shorter gate-length can operate at higher frequency. Thus, it is possible to design VCO circuits at even higher oscillating frequency for applications such as wireless LAN systems. Moreover, it is an advantage to use more metal layers to realize inductors with better quality factor and higher resonant frequency. Finally, new circuit topologies should be investigated to achieve both low phase noise performance as well as wide tuning range.

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Appendix A

Terms Definition

I. Voltage Controlled Oscillator

This is a kind of oscillator that the output frequency can be changed by applying a voltage to its tuning port.

II. Frequency Drift with Temperature

It is the frequency drift of the voltage-controlled oscillator with temperature at a fixed tuning voltage. It can be expressed as a relative percentage change per unit temperature, or as a frequency change per unit temperature.

III. Center Frequency

It can be defined as the output frequency that the oscillator outputs maximum power. It usually abbreviated as f_o or ω_o and their units are Hz and rad/sec respectively.

IV. Tuning Range

When you adjust the tuning voltage of oscillator, the center frequency will shift. Tuning range defines as the full range of frequency shift by adjusting the tuning voltage.

V. Tuning Sensitivity

It defines as the change of output oscillating frequency per unit change of the tuning voltage. Its unit equals Hz/V.

VI. Frequency Tuning Characteristic

It defines as frequency versus tuning voltage performance for a given VCO. This is usually graphed as frequency versus voltage.

VII. Output Power

It defines as the fundamental sinusoidal frequency output of the oscillator measured into a 50 ohm load.

VIII. Varactor Diode

It is a type of diode operated in a reverse biased condition providing a

junction capacitance that is a function of the applied reverse bias voltage. We usually use it as a variable capacitor in voltage controlled oscillators.

IX. Phase Locked Loop (PLL)

It is a widely used feedback circuit in which the VCO frequency and phase is locked to the frequency and phase of a stable reference signal.

XI. Spurious Signal Responses

Spurious frequencies are non-harmonically and unwanted signals present at the oscillator output. Spurious response is usually expressed in terms of dBc.

Appendix B

Below shows the technology file that given in generic CMOS process, which is used in inductance-generation software – ASITIC:

>---------- Start of CMOS.tek ----------<

```
; Sample CMOS technology file
<chip>

    chipx = 512    ; dimensions of the chip in x direction
    chipy = 512    ; dimensions of the chip in y direction
    fftx = 128; x-fft size (must be a power of 2)
    ffty = 128; y-fft size
    TechFile = CMOS.tek
    TechPath = .
    freq = 1.8          ; frequency of operation

<layer> 0               ; p(-) bulk layer
    rho = 0.006         ; ohm-cm
    t    = 350          ; microns
        eps = 11.9

<layer>  1              ; Oxide Layer
    rho = 1e20
    t = 50
    eps = 3.9

<metal> 0
        layer = 1       ; in oxide layer
        rsh = 65        ; sheet resistance3
        t    = 0.5      ; thickness
        d = 1.3             ; distance from bottom of layer
        name = m1
        color = yellow

<metal> 1
        layer = 1
        rsh = 120
        t = 0.72
        d = 1.4
        name = m2
        color = LightSkyBlue1

<metal> 2
        layer = 1
        rsh = 130
        t = 0.65
        d =   2.77
        name = m3
        color = red

<metal> 3
```

```
        layer = 1
        rsh = 60
        t = 0.94
        d =  4.07
        name = m4
        color = blue

    <metal> 4
        layer = 1
        rsh = 30
        t = 1
        d =  6
        name = m5
        color = grey

    <via> 0                 ; metal 1 to metal 2
        top = 1
        bottom = 0
        r = 4
        width = .5
        space = 1.1
        overplot1 = .2      ; to metal 1
        overplot2 = .2      ; to metal 2
        name = via1
        color = purple
    <via> 1                 ; metal 2 to metal 3
        top = 2
        bottom = 1
        r = 0.8
        width = .7
        space = 0.7
        overplot1 = .2      ; to metal 1
        overplot2 = .2      ; to metal 2
        name = via2
        color = cyan1
    <via> 2                 ; metal 3 to metal 4
        top = 3
        bottom = 2
        r = 0.8
        width = .7
        space = 0.7
        overplot1 = .2
        overplot2 = .2
        name = via3
        color = white

    <via> 3                 ; metal 3 to metal 4
        top = 4
        bottom = 3
        r = 4
        width = .4
        space = 1.2
        overplot1 = .2
        overplot2 = .2
        name = via4
        color = yellow

>---------- The end of CMOS.tek ----------<
```

Appendix C

Below shows the technology file that given in generic CMOS process, which is used in inductance-generation software – ASITIC:

>---------- Start of Inductor_Parasitic.m ----------<

```
% Calculate parameters of equivalent L model

clear all;

% R_sheet for met3 only
R_sheet=70e-3;
resistivity_Sub=14;
Sub_thick=500e-6;
for i = 1 : 100
  freq(i) = 0.4e9 + i * 0.02e9;
end
L_value=input('Please input L value(nH): ');
L_value=L_value/1e9;

inner=input('Please input Inner dimension(micron): ');
inner=inner/1e6;

turns=input('Please input no. of turns: ');

width=input('Please input metal width(micron): ');
width=width/1e6;

spacing=input('Please input metal spacing(micron): ');
spacing=spacing/1e6;


length = 4 * turns * (inner + (turns - 0.5)*(spacing + width));
resistance_L = length * R_sheet / width;
Rsub = resistivity_Sub * Sub_thick * length / width;
% Rsub = 50 always
C1 = length * width * 20e-6 * 0.5;
C2 = length * width * 20e-6 * 0.5;
C3 = 0.085e-9 * length / (turns - 1);

fprintf('\n\nR   = %g ohm', resistance_L);
fprintf('\nC1   = %g pF', C1 * 1e12);
fprintf('\nC2   = %g pF', C2 * 1e12);
fprintf('\nC12  = %g pF', C3 * 1e12);
fprintf('\nRsub = %g ohm', Rsub);
```

>---------- Start of Inductor_Parasitic.m ----------<