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Effective mobilities in pseudomorphic Si/SiGe/Si *p*-channel metal-oxide-semiconductor field-effect transistors with thin silicon capping layers

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The room-temperature effective mobilities of pseudomorphic $Si/Si_{0.64}Ge_{0.36}/Si$ *p*-metal-oxide-semiconductor field effect transistors are reported. The peak mobility in the buried SiGe channel increases with silicon cap thickness. It is argued that SiO_2/Si interface roughness is a major source of scattering in these devices, which is attenuated for thicker silicon caps. It is also suggested that segregated Ge in the silicon cap interferes with the oxidation process, leading to increased SiO_2/Si interface roughness in the case of thin silicon caps. © *2001 American Institute of Physics.* [DOI: 10.1063/1.1354662]

Incorporation of pseudomorphic SiGe layers into Si complementary metal-oxide-semiconductor (CMOS) technology has prospects of improving the hole channel mobility to approach that of the bulk silicon electron channel. SiGe metal-oxide-semiconductor field effect transistors (MOSFETs) normally require a Si spacer between the SiO_2 and the SiGe layer to avoid the pile up of unoxidized Ge behind the oxide front (snow plow effect) which leads to a degradation of the oxide/semiconductor interface quality.[1–3] The maximum benefit from incorporation of SiGe in CMOS may expected to occur when the alloy layer is placed as close as possible to the oxide. Unfortunately, as Ge content or alloy growth temperature increases, strain-driven long range roughening of the upper Si/SiGe heterointerface may occur[4] which sets a limit on the Si cap thickness. Previously, when this type of material was oxidized to retain a 2.5 nm Si capping layer,[1] there was a severe degradation in mobility with the observation of oxide pinholes.

Here, we report electrical measurements on pseudomorphic $Si/Si_{0.64}Ge_{0.36}/Si$ *p*-metal-oxide-semiconductor (*p*-MOS) devices fabricated from solid source molecular beam epitaxial (SS-MBE) material grown using a low growth temperature (450 °C), postgrowth anneal (800 °C) technique.[5] The pseudomorphic $Si_{0.64}Ge_{0.36}$ layers have interfaces[5] without the strain-induced interface roughness that is associated with higher temperature growth and thus these structures are well suited for incorporation into SiGe/MOS technology. The final Si capping layer thicknesses obtained after oxidation were measured by a combination of x ray, cross-sectional transmission electron microscopy (TEM) and capacitance–voltage (*C–V*) measurements, to within an accuracy of ± 0.2 nm. Devices were fabricated in a standard CMOS-type process, but with a reduced thermal budget (maximum 850 °C, 60 s) to maintain the integrity of the SiGe layer. Oxide growth was by dry thermal oxidation at 800 °C. The gate material is *in situ* boron doped polysilicon and source and drain contacts are conventional high doped BF_2 ($5\times10^{15}\,cm^{-2}$, 50 keV) implants. Two different *n*-type substrate doping concentrations (N_{sub}) were used, $2\times10^{17}\,cm^{-3}$ (batch A) and $5\times10^{15}\,cm^{-3}$ (batch B), to investigate punchthrough and drain induced barrier lowering effects which occur at short device channel lengths. A nominally undoped 100 nm Si buffer layer was grown on the substrate, followed by a $Si_{0.64}Ge_{0.36}$ layer of thickness 10 nm. A range of values of the Si capping layer were chosen such that the final values after process cleans and oxidation would be between 2 and 8 nm.

To determine the effective carrier mobility, μ_{eff}, we have used a modified ''split-*C–V*'' technique[6] on large area FETs of length = 300 μm and width = 50 μm. Figures 1 and 2 show plots of μ_{eff} as a function of total carrier sheet density (N_S) for devices fabricated in batches A and B, respectively. The crosses on the plots for W02, W03, and W10 indicate points where marked decreases in effective mobility occur as the total carrier density increases. Simulations indicate that these points are where parasitic conduction at the Si/SiO_2 interface begins to affect the transport characteristics of the device. It should be noted that for both W01 and W09 (nominal 2 nm Si cap), and the Si control (W06), we do not observe any such change in slope ($d\mu_{eff}/dN_s$) in the range of

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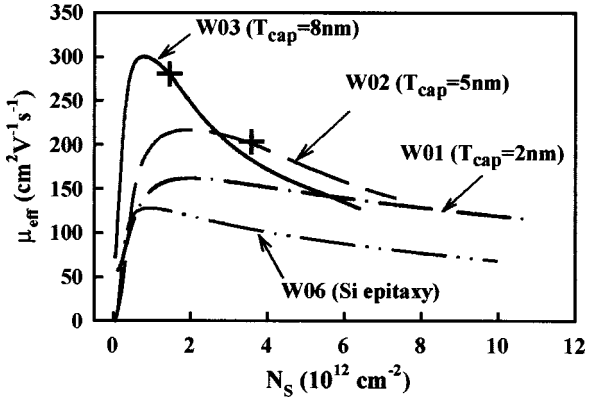

FIG. 1. Batch (A), effective mobility vs carrier sheet density for devices with a 2×10^{17} cm^{-3} substrate doping punchthrough stopper. The observed onset of conduction at the SiO_2/Si interface is marked by a cross (+).

measured data, and this is consistent with our simulations. There is clearly a dependence of peak effective mobility on Si capping layer thickness, with wafer W03, the 8 nm Si capped sample, exhibiting a maximum factor of 2.44 increase (305 $cm^2\,V^{-1}\,s^{-1}$) when compared to the W06 Si standard (125 $cm^2\,V^{-1}\,s^{-1}$).

Lander *et al.*,[7] Whall and Parker,[8] and Kearney and Horrell[9] have provided strong evidence that interface roughness rather than alloy scattering plays a dominant role in limiting the hole mobility in devices of this type. To determine the effect of thickness fluctuations, Δ, in the SiO_2 insulator and Si cap, we have evaluated the associated fluctuations in the electrostatic potential[10] at the Si/SiGe interface using a self-consistent solution of Poisson's and Schrödinger's equations. To compare structures with different Si cap or oxide thicknesses the carrier sheet density in the channel was kept at a constant value of $1.0\times10^{12}\,cm^{-2}$, low enough to ensure that the Si cap would not be populated. The rms potential fluctuation, ΔV, is plotted as a function of rms roughness amplitude in Fig. 3 for typical values[9,11] of Si/SiGe and Si/SiO_2 interface roughness, Δ. It is clear that, for the current specifications, the scattering potential is more sensitive to fluctuations in oxide rather than Si capping layer thickness. In this respect, the situation is similar to the scattering of silicon inversion layer electrons by remote metal/oxide interface roughness.[12] Typical oxide fluctuations of $\Delta_{oxide}\sim0.2$ nm will generate a rms scattering potential of

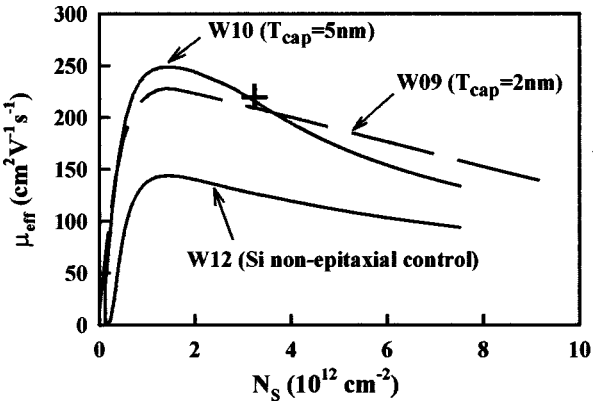

FIG. 2. Batch (B), effective mobility vs carrier sheet density for devices without a punchthrough stopper. The observed onset of conduction at the SiO_2/Si interface is marked by a cross (+).

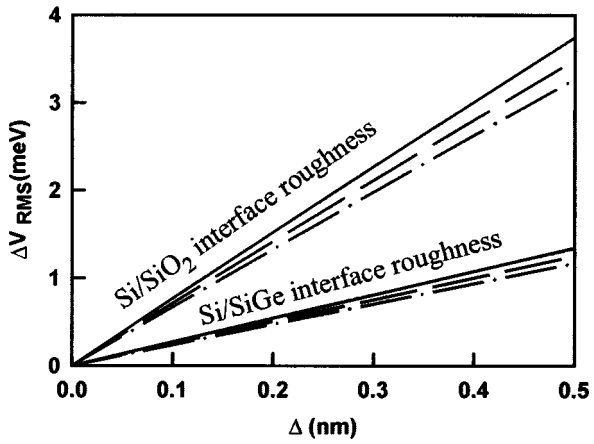

FIG. 3. Calculated rms interface roughness scattering potential (ΔV) due to rms thickness fluctuations, Δ, at the SiO_2/Si interface and at the upper Si/SiGe interface for values of different Si capping layer thickness. Solid lines: 2 nm Si cap; dashed lines: 5 nm Si cap; dot–dashed lines: 8 nm Si cap.

$\sim$1.4 meV. To obtain the same scattering potential, the alloy thickness fluctuations (Δ_{SiGe}) must be 0.4 nm. This difference is attributed to the lower dielectric constant in SiO_2. The interface roughness limited mobility μ_{IR} is predicted to behave as[10]

$$\mu_{IR}\propto(\Delta V)^{-\beta} \tag{1}$$

with $\beta=2$.

In the presence of other scattering mechanisms, e.g., phonon scattering, the resultant mobility will be expected to have a β value of less than 2. However, comparing our experimental results (Fig. 1) with calculated values of ΔV using constant Δ (Fig. 3) and constant effective field of 0.15 MV/cm^{-1} ($N_s=1.5\times10^{12}\,cm^{-2}$) we deduce a value of $\sim$3. This high value appears to be associated with the degradation of SiO_2/Si interface quality with decreasing silicon cap thickness, due to segregation/diffusion of Ge into the cap.[5] Interface state densities, D_{it}, for these samples were deduced from quasistatic C–V measurements[13] and from a comparison of low frequency and high frequency C–V data.[13] Figure 4 shows plots of D_{it} versus energy (measured from the valence band edge of silicon) for wafer W01 (batch A). The

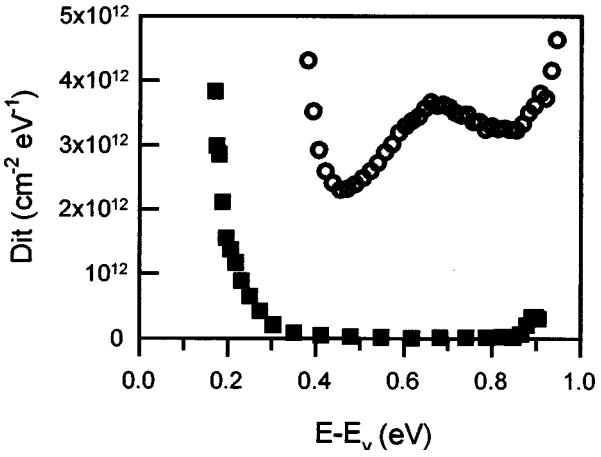

FIG. 4. Interface trapped charge density distributions vs energy measured from the valence band edge of silicon. Samples shown are W01, 2 nm Si cap (○) and W06, epitaxial Si control (■).

TABLE I. Maximum effective mobility, μ_{eff}(max), vs capping layer thickness, T_{cap}. Also shown are the interface trap densities, D_{it}, measured at midgap or at the peak in the energy distribution of D_{it}, shown in Fig. 3. Samples marked † are silicon controls.

Wafer No.	N_{sub} (cm^{-3})	T_{cap} (nm)	μ_{eff}(max) $\text{cm}^2\,\text{V}^{-1}\,\text{s}^{-1}$	D_{it} ($\text{cm}^{-2}\,\text{eV}^{-1}$)
W01(a)	2×10^{17}	2	162	3.8×10^{12}
W02(a)	2×10^{17}	4.5	217	5×10^{11}
W03(a)	2×10^{17}	8	305	$<2\times10^{11}$
†W06(a)	2×10^{17}	24	128	$<2\times10^{11}$
W09(b)	$\sim5\times10^{15}$	2	228	8×10^{11}
W10(b)	$\sim5\times10^{15}$	5	249	$<1\times10^{11}$
†W12(b)	$\sim5\times10^{15}$	0	144	5×10^{10}

peak at ~0.7 eV has been seen previously by Goh *et al.*[3] and has been attributed to Si dangling bonds at the oxide interface, the generation of which is enhanced in the presence of Ge. The maximum mobilities, μ_{max}, for given silicon cap thicknesses are shown in Table I, together with the interface trap densities, D_{it}, either at an observable peak or at midband. There is a clear correlation between μ_{max} and D_{it} for samples containing SiGe in batch A. As might be expected, μ_{max} is lower in the epitaxial Si control (W06) because of the larger effective mass, the absence of light hole/heavy hole splitting and the proximity of the SiO_2/Si interface. Samples of batch B were grown at a slightly lower growth temperature (~430 °C), and since we observe a higher μ_{max} for a given cap thickness, this implies that there is less Ge segregation. Nevertheless, the SiGe samples show the same correlation with D_{it} as those in batch A. These SiO_2/Si interface states, if charged, would not be expected to give rise to appreciable scattering of carriers in the buried alloy.[14] We suggest that an increased roughening of the SiO_2/Si interface accompanies the generation of these interface states, possibly due to the presence of microscopic clusters of SiGe which may have a different rate of oxidation from silicon.[15] This roughness would be responsible for the decrease in mobility. A similar correlation between D_{it} values and the rms amplitude, Δ, of the roughness has been demonstrated for Si MOS structures by Koga *et al.*,[16] but the underlying mechanisms which give rise to this effect are probably different from the present case.

In conclusion, we have shown that, depending on the oxide and silicon cap thickness, SiO_2/Si as opposed to Si/SiGe interface roughness can limit the hole mobility in the strained SiGe channel. It is argued that this interface roughness scattering is less for devices having thicker silicon caps, not only because the magnitude of the Coulomb potential fluctuation in the channel for a given SiO_2/Si interface roughness is reduced, but because the smaller amplitude of the Ge segregation tail at the SiO_2/Si boundary leads to a smoother interface.

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