2 MeV electron irradiation effects on the electrical characteristics of metal-oxide-silicon capacitors with atomic layer deposited Al_2O_3, HfO_2 and nanolaminated dielectrics

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ABSTRACT

The effects of 2 MeV electron irradiation on the electrical characteristics of atomic layer deposited (ALD) high permittivity (high-k) layers of Al_2O_3, HfO_2 and a nanolaminate of them are evaluated. Metal-oxide-semiconductor capacitors with a nominal dielectric physical thickness of 10 nm were fabricated on different p-type and n-type silicon substrates. The capacitance-voltage (C-V) and current-voltage (I-V) characteristics of the different structures are analyzed as a function of electron irradiation. A progressive negative shift of the C-V characteristics is observed with increasing electron irradiation, indicating the generation of effective positive charges. Similar generation rates for effective trapped charges and interface states are obtained for all the different high-k dielectric layers studied. The hysteresis of the C-V curves after irradiation increases in the case of Al_2O_3 samples, for HfO_2 decreases while the irradiation has little impact on the hysteresis of the nanolaminate stack. A progressive increase of the leakage current with electron irradiation dose is observed for all the studied dielectrics. The analysis of the current-voltage characteristics measured at different temperatures point to Poole-Frenkel as the dominant conduction mechanism. Under the studied conditions, no impact of electron irradiation fluence on dielectric breakdown voltage has been appreciated.

Keywords: electron irradiation effects; high-k dielectrics; Al_2O_3; HfO_2; nanolaminate

1. Introduction

A number of high permittivity (high-k) dielectrics have been investigated as candidates to replace the SiO_2 as gate dielectric in complementary metal-oxide-semiconductor (CMOS) technologies, being Al_2O_3 and HfO_2 among the most studied ones [1-4]. Apart from CMOS technologies, high-k dielectrics are also of strong interest for a wide range of micro/nanoelectronics applications, including, dynamic random access memories (DRAM) [5], emerging nanodevices [6,7], organic light emitting diodes [8], as a surface passivation layer on high-efficiency crystalline silicon solar cells [9], and for a variety of microelectromechanical systems [10]. For all these applications, atomic layer deposition (ALD) has shown great potential to meet the requirements concerning dielectric properties, large area uniformity, conformality and accurate thickness control. Moreover, taking advantage of ALD unique properties, some works have also studied the possibility to deposit alternate layers of different high-k materials (nanolaminates). This can be useful to tailor the dielectric properties of the stack, reduce leakage currents in the presence of possible crystallization processes or improve the interface in contact with the semiconductor [11-13].

The integration of new materials and processes requires the study of different aspects for technology assessment. In recent years, a lot of work has been devoted to physical and electrical characterization, as well as to reliability issues, of alternative high-k dielectrics [14-16]. However, much less is known about their behaviour in radiation-harsh environments. The study of ionizing radiation effects on high-k dielectrics is of special interest for space applications [17], but also for high energy physics experiments and even to gain insight into

possible effects of some advanced micro/nanofabrication processes like e-beam or X-rays lithography.

Since the early days of microelectronics, radiation-induced effects on conventional SiO_2 dielectrics for CMOS technologies have been investigated [18,19]. Total ionizing dose (TID) damage, with charge trapping in the gate dielectric and interface states generation at the silicon interface, have been the main radiation-induced degradation mechanisms for a wide range of SiO_2 layer thickness [20]. A trap assisted tunnelling phenomenon, the radiation-induced leakage current (RILC), was observed for SiO_2 layers with thickness in the range of about 3 nm to 8 nm [21,22]. Fortunately, the continuous miniaturization process has led to radiation-harder SiO_2 layers, with reduced charge trapping and flat band voltage shifts [23], and with thickness below the trapped-hole tunnelling limit (around 3 nm) [20].

The introduction of high-k dielectrics brings some uncertainty in terms of their radiation hardness. Moreover, due to the dependence of TID damage on the physical dielectric thickness, the radiation response could be an issue for such thicker high-k dielectric layers used in place of SiO_2 [24]. Although some works have already been published on radiation effects on a few high-k dielectrics, these have been mostly limited to irradiations with heavy ions or X-rays, and only separated studies addressing either capacitance-voltage or current-voltage characterization have been generally considered [24-29].

In this work, the effects of different doses of 2 MeV electron irradiation on the electrical characteristics of ALD-deposited layers of Al_2O_3, HfO_2 and a nanolaminate of them are evaluated. Metal-oxide-semiconductor (MOS) structures with a nominal high-k dielectric

physical thickness of 10 nm were fabricated on p-type and n-type silicon substrates. The capacitance-voltage and current-voltage characteristics of the different structures are analyzed as a function of electron irradiation dose paying special attention to the study of the effective trapped charges, generation of interface states, presence of hysteresis and electrical conduction through the layers.

2. Experimental

2.1. Atomic layer deposition and fabrication of MOS capacitors

Three high-k dielectric layers, Al_2O_3, HfO_2 and a nanolaminate of them, are studied in the present work. The layers were deposited by ALD in a Cambridge NanoTech Savannah 200 system, by using Trimethylaluminium (TMA), Tetrakis(Dimethylamido)-Hafnium (TDMAH) and H_2O as precursors, and N_2 as carrier and purge gas. In the case of Al_2O_3, the ALD process was done at 200ºC with 95 cycles, for HfO_2, a 100 cycles deposition process was carried out at 225ºC and in the case of the nanolaminate, a 5-layer stack ($Al_2O_3/HfO_2/Al_2O_3/HfO_2/Al_2O_3$) was deposited at 225ºC, using 20 ALD-cycles for each layer. A detailed description of the ALD process for each case can be found in [30].

The film thickness of the as-deposited layers was measured on p-type silicon substrates by means of a Rudolph Research Auto EL ellipsometer, using an index of refraction (n) of 1.64 in the case of Al_2O_3, and 2.07 in the case of HfO_2. Under these conditions the physical thickness of the as-deposited layers is 11.6 nm and 10.5 nm, respectively. In the case of the

nanolaminate, a layer thickness estimation of 10 nm can be made using the growth-per-cycle obtained for each dielectric [31,32]; this has been also corroborated by cross-sectional TEM results [33].

Metal-oxide-semiconductor (MOS) capacitors were fabricated on 100 mm-diameter (100)-oriented Czochralski-grown silicon wafers. Three types of silicon substrates were used: n-type (phosphorus-doped with a resistivity 1-12 Ω·cm), and two p-type with different doping concentrations of boron, giving resistivity ranges of 4-40 Ω·cm and 0.1-1.4 Ω·cm, which are referred here as p-type 10 Ω·cm and p-type 1 Ω·cm, respectively.

The fabrication process started with standard wafer cleaning followed by a wet thermal oxidation process at 1100ºC leading to a 400 nm-thick SiO_2 layer. This field oxide was patterned by photolithography and wet etching. The deposition of the high-k dielectric layer by ALD was carried out immediately after cleaning in H_2O_2/H_2SO_4 and a dip in HF(5%). A 500 nm-thick Al(99.5%)/Cu(0.5%) layer was deposited as the metal gate of the MOS capacitors. After patterning the metal layer by photolithography and wet etching, the back of the wafers was also fully metalized for electrically contacting the silicon substrate. Finally, the wafers underwent a forming gas (N_2/(10%)H_2) annealing step at 350ºC for 20 min, thus being this the highest temperature achieved during the dielectric layers processing. The fabricated MOS capacitors are square-shaped with five different surface areas ranging from 9.604×10^{-3} cm^2 to 6.4×10^{-5} cm^2.

2.2. Electrical characterization and irradiation

In order to evaluate the electrical characteristics of the dielectric layers, capacitance - voltage (C-V) and current - voltage (I-V) were measured, in a light-proof and electrically shielded probe station, using an HP-4192 A LF impedance analyzer and an HP 4155B semiconductor parameter analyzer, respectively. C-V measurements were performed at room temperature and the I-V curves were measured at five different temperatures (-30ºC, -10ºC, 20ºC, 60ºC and 100ºC) by using an Espec ETC-200L thermal system.

C-V measurements were performed at 30 kHz signal frequency (f) for both, inversion to accumulation and accumulation to inversion voltage sweeps. The hysteresis was defined as the difference between the extracted flat-band voltages (V_{fb}) corresponding to the two voltage sweeps (hysteresis = $V_{fb_inv_to_acc}$-$V_{fb_acc_to_inv}$). An estimation of the effective trapped charge density (N_{eff}), defined as a fixed charge located at the insulator/silicon interface, has been obtained from the comparison of the extracted V_{fb} values with the ones expected for an ideal MOS structure with 4.25 eV metal work function, corresponding to the aluminium gate electrode. The conductance versus voltage (G-V) characteristics were also recorded. An estimation of the interface states density (D_{it}) has been obtained from the peak of the parallel conductance (G_p) derived from the G-V measurements [34]:

$$D_{it} \approx \frac{2.5}{q \cdot Area} \cdot \frac{G_p}{2\pi f} \quad (1)$$

where q is the electron charge.

The capacitance of the MOS structures in accumulation regime was used to estimate the equivalent oxide thickness (EOT) and effective permittivity (k) of the dielectric layers. The

obtained EOT values on the different silicon substrates ranged between 5.9 nm and 6.9 nm, 3.2 nm and 3.5 nm, and 4.3 nm and 5.1 nm for the Al_2O_3, HfO_2 and nanolaminate layers, respectively [30]. Following this approach, the corresponding effective permittivity values ranged between 6.5 and 7.7, 11.8 and 13.1, and 8.2 and 9.7, respectively.

For the I-V characterization, the MOS structures were biased in accumulation, i.e., applying negative voltage sweeps to the metal gate with respect to the p-type substrates and positive voltage sweeps in the case of the n-type silicon ones. Dielectric breakdown voltage (V_{bd}) was registered as a sudden increase in the leakage current through the dielectric layer.

2 MeV electron irradiations were performed at room temperature for three different fluences ($\phi = 1\cdot10^{14}$ e/cm^2, $1\cdot10^{15}$ e/cm^2 and $1\cdot10^{16}$ e/cm^2, with total ionizing doses about 2.5 Mrad(Si), 25 Mrad(Si) and 250 Mrad(Si), respectively) using the electron accelerator at Takasaki-JAEA in Japan.

3. Results and discussion

3.1. Capacitance-voltage characteristics

Figure 1 shows an example of typical C-V characteristics measured from inversion to accumulation (lines) and accumulation to inversion (symbols) for Al_2O_3 capacitors on 1 $\Omega\cdot$cm p-type silicon substrate. The different curves correspond to non-irradiated and 2 MeV electron-irradiated devices at different fluences. Although only C-V plots for a single

dielectric and substrate are given in Figure 1, the results are qualitatively similar for all the different conditions studied, where a progressive negative shift of the characteristics is observed with increasing electron irradiation, indicating positive charge build-up for all the irradiated high-k dielectric layers.

An estimation of the effective trapped charge density (N_{eff}) is plotted for the different fluences in Figure 2(a). From the figure, N_{eff} values around $-2{\cdot}10^{12}$ cm^{-2} and $-3{\cdot}10^{12}$ cm^{-2} are observed for most of the studied non-irradiated dielectric and substrate conditions, only some more negative N_{eff} is present for the case of the nanolaminate on 1 Ω·cm p-type Si, whereas the effective trapped charge density is nearly neutral for the HfO_2 on 1 Ω·cm p-type Si.

Interestingly, when exposing the samples to electron irradiation, a common linear-logarithmic trend seems to be observed for the different dielectrics and substrates studied, with radiation-induced N_{eff} generation rates around $1{\cdot}10^{12}$ cm^{-2}-$1.5{\cdot}10^{12}$ cm^{-2} per decade of electron irradiation fluence. Somewhat lower N_{eff} generation rates and/or certain saturation are observed for some samples subjected to the highest fluence ($1{\cdot}10^{16}$ e/cm^2). Although, to our best knowledge, no results about these high-k dielectric layers subjected to electron irradiation have published in literature, a similar degradation trend has been indeed obtained for the cases of Al_2O_3 and HfO_2 ALD layers of similar thickness exposed to comparable high irradiation doses (1-10 Mrad(SiO_2)) with 10-keV X-rays [26-28]. In our study, similar results are also observed for the case of the studied Al_2O_3/HfO_2 nanolaminate dielectric.

As shown in the inset in Figure 1, a peak in the conductance curves is observed after the highest irradiation fluences, which can be attributed to the loss mechanism due to interface trap capture and emission of carriers. In this way, an estimation of the interface states density (D_{it}) has been obtained from the peak of the corresponding parallel conductance (eq. (1)). The extracted results are plotted in Figure 2(b). From the figure, D_{it} values in the range between $1\cdot10^{10}$ $cm^{-2}eV^{-1}$ and $2\cdot10^{11}$ $cm^{-2}eV^{-1}$ are obtained for all the studied non-irradiated dielectric and substrate conditions. It should be noted that these extracted D_{it} values correspond to either interface traps or near-interface traps, which may exist within the dielectric but in close vicinity of the interface, so that they are able to exchange charge with the silicon on the time scale of the electrical measurements (also called “slow” interface states or border traps [35]).

From Fig. 2(b), when exposing the samples to $1\cdot10^{14}$ e/cm^2 electron irradiation there is a slight increase in D_{it}, but for higher fluences, a common trend is observed on the logarithmic-logarithmic plot region for the whole set of studied samples: a potential law, $\Delta D_{it} \propto \phi^n$, with n between 0.45 and 0.75, is inferred. Similar values for n (around 2/3) were reported for the radiation-induced interface states generation in early works dealing with conventional SiO_2 gate dielectrics [36]. However, to our best knowledge, only few results about interface state generation as a function of irradiation have been published in the literature for these high-k dielectric layers under study. Some results were obtained by means of charge pumping measurements on similar Al_2O_3 ALD films subjected to 10-keV X-rays irradiation [37]. Contrary to the results generally obtained for Si/SiO_2 systems, a decrease of interface states after irradiation was observed there, which was attributed to a

possible radiation-induced neutralization of traps in those layers with quite high pre-irradiation interface states densities (in the range of $1{\cdot}10^{12}$ cm^{-2}).

Finally, an additional effect of the irradiation on the characteristics has been observed in the hysteresis of the measured C-V curves. It is already shown in Figure 1, but it has been specifically illustrated in Figure 3 for the different samples under study. For the irradiated Al_2O_3 films on both, p-type and n-type silicon substrates, an increase of the magnitude of the hysteresis is observed. In this way, while small hysteresis values (in the range of 20 mV or 30 mV) are present on the C-V characteristics of the non-irradiated Al_2O_3 layers on p-type silicon, this progressively increases with electron irradiation fluences, reaching hysteresis values up to about 400 mV after $1{\cdot}10^{16}$ e/cm^2. Similarly, the absolute value of the hysteresis also increases for the Al_2O_3 layers on n-type silicon, with hysteresis values around -450 mV for the non-irradiated samples and about -1400 mV after the highest irradiation fluence ($1{\cdot}10^{16}$ e/cm^2). Interestingly, the opposite trend is observed for the HfO_2 dielectrics on both, p-type and n-type silicon substrates: while hysteresis values above 1000 mV are measured on the non-irradiated HfO_2 capacitors on p-type Si, these are reduced by a few hundreds of mV with increasing electron irradiation fluence, reaching hysteresis values around 700 mV or 750 mV after $1{\cdot}10^{16}$ e/cm^2 . Similarly, the absolute value of the hysteresis is also reduced for the irradiated HfO_2 layers on n-type silicon. On the other hand, a lower impact of the electron irradiation on the magnitude of the hysteresis is obtained for the nanolaminate stack, combining Al_2O_3 and HfO_2 layers, on both types of substrates.

It is known, from conventional SiO_2 gate dielectrics, that radiation-induced defects can be responsible for the appearance of hysteresis in C-V curves. This has been proved by means

of electron paramagnetic resonance studies [38]. In the present work, it is believed that defects generated by the 2 MeV electron irradiation may be responsible for the increasing hysteresis observed for the Al_2O_3 dielectric layers. On the other hand, the opposite trend shown by the HfO_2 layers can be originated by their high pre-existing non-irradiated hysteresis values, which is indicative of the presence of some defect instabilities in the gate dielectric stack [39]. With regard to the physical origin of the defects, it is known that hysteresis can be associated with an excess of hydrogen and/or hydroxyl groups in the ALD dielectric layers, that can be especially significant for low temperature deposition processes [32]. In the present study, the 2 MeV electron irradiation could result in hydrogen release from the layers leading to a certain beneficial reduction or passivation of the instabilities responsible for the C-V hysteresis. From Figure 3, the hysteresis reduction in the HfO_2 layers is more significant for low irradiation fluences and slightly diminishes for the highest fluences, where more radiation-induced defects are expected to contribute to the overall C-V curves hysteresis. Finally, the lower impact of the electron irradiation on the magnitude of the C-V curves hysteresis for the nanolaminate stacks can be explained by the combined effects on the Al_2O_3 and HfO_2 layers.

3.2. Current-voltage characteristics

Figure 4 shows the current density versus voltage characteristics measured for Al_2O_3, HfO_2 and nanolaminate MOS capacitors on n-type silicon substrates. From the measurements performed at 20ºC, a progressive increase of the current density through the dielectrics is observed for increasing electron irradiation fluence, thus indicating a radiation-induced

degradation of the layers. Although the results in Figure 4 correspond only to n-type silicon wafers, these were qualitatively similar for the case of the two different p-type substrates studied, with opposite polarities applied (accumulation conditions). However, the leakage current density under substrate injection (n-type substrates with positive gate bias) was found to be much larger than under gate injection (p-type substrates with negative gate bias) for equal absolute voltage values. This is mainly attributed to the different band structures under the two injection modes [3,40].

In order to investigate the origin of the radiation-induced current increase, five different sizes of square-shaped MOS capacitors were measured at various temperatures for the different irradiated dielectrics and substrates under study. As shown in Fig. 5, the current-voltage characteristics were found to scale with active area, thus indicating the degradation to affect the full high-k dielectric region. It is known from SiO_2 gate dielectrics that radiation-induced defects can be detrapped or annealed by tunnel or thermal emission processes [18]. For the present irradiated samples, a good stability of the damage was confirmed by measurements carried out after some months of storage at room temperature conditions.

In view of the basic similarities between the current-voltage characteristics of the non-irradiated and irradiated devices on the different substrates, the increase of the current density can be treated as a certain shift of the I-V characteristics towards lower accumulation voltages. Figure 6 shows the absolute value of the radiation-induced voltage shift of the I-V curves corresponding to a fixed current density level of $1{\cdot}10^{-5}$ A/cm^2. As shown, the largest voltage shifts, i.e., the major impact of irradiation on the I-V characteristics, have been registered for the case of the Al_2O_3 layers.

With regard to measurement temperature, this has been found to have a significant impact on the I-V characteristics. Current variations from about one to three orders of magnitude have been obtained between the measurements performed at the highest (100ºC) and lowest (-30ºC) temperatures, being this effect more important for the case of the HfO_2 layers (Fig. 4(b)). The measurements performed at different temperatures have revealed for some dielectrics a similar impact to the irradiation effect. For example, as it can be appreciated in Fig. 4(c), similar characteristics are obtained for the nanolaminate layer on n-type Si subjected to $1 \cdot 10^{16}$ e/cm^2 and measured at 20ºC or the non-irradiated one measured at 100ºC.

In order to have a better understanding of the impact of electron irradiation and measurement temperature on the leakage current, the conduction mechanisms through the different high-k dielectric layers were investigated. Five basic mechanisms have been considered as candidates to be responsible for the registered electrical conduction: Schottky emission (SE), Tunnel (Direct tunnel (DT) and Fowler-Nordheim (FN)), Poole-Frenkel (PF), hopping and space charge limited [41]. Owing to the different behaviour observed for voltage or electric field dependences, the last two mechanisms were disregarded.

Schottky emission is an electrode-limited mechanism which occurs when an electron overcomes the potential energy barrier at the metal-semiconductor interface via field-assisted lowering, thus, it is basically controlled by the metal-insulator interface. On the other hand, Poole-Frenkel emission is a bulk-limited mechanism which results from the combination of tunnelling to trapped states within the insulator, followed by excitation from

the potential trap well. Therefore, PF mechanism relies on existing traps in the dielectric. In thermal SiO_2, the leakage current is determined by tunnelling mechanisms, direct tunnel through the whole dielectric stack or Fowler-Nordheim tunnelling through a trapezoidal potential barrier, depending on dielectric thickness and applied electric field [41]. However, in high-k dielectrics, trap related mechanisms typically prevail at low voltages, while FN tunnelling may dominate at high fields [40,42].

In the present study, direct tunnel and Fowler-Nordheim may have some contributions to the overall conduction at the lowest and highest voltages, respectively. In particular, FN can be responsible for the conduction at high electric fields, especially for the case of Al_2O_3 near dielectric breakdown, where much weaker temperature dependence is appreciated (Fig. 4(a)). For this high-field regime, reasonable FN barrier height values of about 2.6 eV have been extracted for example for the case of the non-irradiated Al_2O_3 layers on 1 Ω·cm p-type substrate, by considering the effective mass of electrons in alumina as 0.2 times the free electron mass. This result is in good agreement with previous published results in the literature [43,44].

However, in view of the significant temperature dependence observed for the electrical conduction through the different dielectric layers (Fig. 4), direct tunnel and Fowler-Nordheim mechanisms are not thought to play a dominant role in the major portion of the measured characteristics. This is corroborated by the disagreement with FN model for the major part of the characteristics. The SE, PF and FN conduction mechanisms can be distinguished by examining the dependency of the leakage current on the applied field and temperature. An extensive analysis of the electrical conduction through the different high-k

dielectric layers was carried out. This included the p-type and n-type substrates, the different 2 MeV electron irradiation fluences and the measurements carried out at various temperatures (from -30ºC to 100ºC). It is important to note here that the electric field in the different dielectric layers (E) was calculated as the voltage drop across the dielectric layer (V_{ox}) divided by its physical thickness. V_{ox} was estimated by subtracting V_{fb} from the applied gate voltage. Note that in this approach, the existence of any possible thin interfacial layer of SiO_2 between the silicon and the high-k material is neglected.

The results from this study pointed to Poole-Frenkel (eq. (2)) as the conduction mechanism that better fits the experimental results, suggesting it to play a dominant role in the major part of the conduction characteristics of the different dielectric layers studied. As an example, Figure 7 shows a Poole-Frenkel plot of the dependence between measured leakage current and electric field (Ln J/E versus $E^{1/2}$) for the case of non-irradiated HfO_2 MOS capacitors on 1 Ω·cm p-type Si. A good linear fit is obtained for a significant central part of the characteristics, until dielectric breakdown occurs. Moreover, the extracted k_d values from the slopes of the HfO_2 and nanolaminate PF plots (eq. (2)) are bound by the optical dielectric constant ($k_{op}=n^2$, where n is the refractive index) and the static dielectric constant, indicating PF conduction [45]. For the case of the Al_2O_3 layers, k_d values in the range of the refractive index have been obtained, in agreement with previously published results [46-48].

Poole-Frenkel (PF) $$J_{PF} \propto C\ E\ exp\left[-\frac{q\left(\phi_B-\sqrt{\frac{qE}{\pi k_d \varepsilon_0}}\right)}{k_B T}\right] \quad (2)$$

Where ϕ_B is the barrier height, E is the electric field, ε_0 is the permittivity of vacuum, k_d is the dynamic dielectric constant, k_B is the Boltzmann constant, T is the temperature and C is a constant.

Figure 8 shows the Poole-Frenkel plots of the dependence between measured leakage current at 20ºC and electric field for non-irradiated and electron irradiated Al_2O_3, HfO_2 and nanolaminate MOS capacitors. A good linear fit is obtained for a significant central part of the characteristics for both, capacitors on p-type silicon (Fig. 8(a)) and n-type Si (Fig. 8(b)). However, the main difference between the results on the different substrate types is a significant radiation-induced shift of the Poole-Frenkel plots along the electric field axis registered for the case of the p-type samples. This is not observed for the case of the nanolaminate and HfO_2 MOS capacitors on n-type Si, and only some small shifts are registered for the case of the irradiated Al_2O_3 capacitors on n-type Si. This phenomenon could be explained by a combination between the asymmetry of the involved band structures and a local modification of the electric field due to the presence of the radiation-induced damage. In this way, regardless of their position within the high-k dielectrics, the radiation-induced positive trapped charges, which at first instance might be considered to be uniformly created within the high-k layers, are expected to be responsible for a certain increase of the local electric field near the injecting cathode. Under this situation, when considering electron injection from the gate (p-type MOS capacitors), the electric field within the relevant high-k dielectric region for PF conduction (close to the metal gate), can be underestimated by using the applied electric field, thus resulting in a shift of the Poole-Frenkel plots towards lower $\sqrt{E}$ values. A similar mechanism has been proposed in the study of hafnium titanium silicate layers under the presence of negative trapped charges [49].

For the case of the MOS capacitors on n-type Si, the radiation-induced positive trapped charges are also expected to increase the local electric field near the injecting cathode (silicon substrate). However, due to the different band structure, this would not have a significant impact for the case of the HfO_2 (with lower conduction band offset) and nanolaminate layers and only a small impact on the relevant high-k dielectric region for PF conduction (close to the semiconductor interface) would be registered for the case of the Al_2O_3 dielectric with higher conduction band offset, thus resulting in the observed shift of the Poole-Frenkel plots towards lower $\sqrt{E}$ values.

In order to verify whether the observed transport effectively follows an Arrhenius-type PF behaviour with temperature (eq. (2)), J/E has been plotted versus the inverse of temperature at various electric fields, as shown for a particular E value in the inset of Fig. 7. From the Arrhenius plot, the activation energies are extracted at various electric fields and these are plotted against $\sqrt{E}$ to extract the Poole-Frenkel barrier height or trap level energy (ϕ_B in eq. (2)). Figures 9(a) for p-type and 9(b) for n-type substrates show, in accordance with P-F conduction mechanism, that the trap barrier energy height linearly decreases with $\sqrt{E}$, allowing to extract the trap levels energies ϕ_B, which correspond to the intercept with the energy axis at zero electric field. The corresponding extracted ϕ_B values are shown in Figure 9(c).

From figure 9(a), some radiation-induced shift of the activation energies along the electric field axis is observed for the samples on p-type Si, especially for the cases of Al_2O_3 and nanolaminate MOS capacitors, this could give rise to reduced or underestimated PF trap

level energies (ϕ_B) with increasing electron irradiation fluence (Fig. 9(c)). As commented for Fig. 8(a) results, this can be originated by a local modification of the electric field associated with the presence of the radiation-induced positive trapped charges. In spite of the radiation-induced ϕ_B lowering, it has to be noted that the trap energy levels obtained for the non-irradiated samples are in good agreement with previous results published in the literature for Poole-Frenkel emission in similar high-k dielectric layers. In this way, ϕ_B values from 0.5 to 0.7 eV below the conduction band edge have been published in the literature for ALD HfO_2 [16,49,50] and values up to 1.5 for pure Al_2O_3 have been obtained in the case of ALD Hf_xAl_yO thin films with various Hf/Al compositions [50]. However, it is also known that differences in ϕ_B values may be also related to different growth methods, pre- and post-growth processing and devices technologies used [51]. With regard to the dielectric layers on n-type Si (Figures 9(b) and 9(c)), the depth of the dominant trap levels perhaps seem to slightly increase with electron irradiation for the cases of the HfO_2 and nanolaminate, whereas no clear trend is observed for the Al_2O_3 case.

Dielectric breakdown voltage (V_{bd}) was registered during the gate voltage sweeps as an abrupt increase in the leakage current. Figure 10 shows V_{bd} for Al_2O_3, HfO_2 and nanolaminate MOS capacitors as a function of electron irradiation fluence for three different measurement temperatures (-30ºC, 20ºC and 100ºC). Although no statistic evaluation of dielectric breakdown was carried out, no apparent impact of electron irradiation fluence on V_{bd} was observed, suggesting that the radiation-induced damage has no clear impact on the final dielectric breakdown of the layers subjected to such voltage sweep tests. These results are in agreement with previous studies reported in the literature addressing the electrical reliability of ultrathin SiO_2 layers (in the range of 3 nm to 3.2 nm)

irradiated with gamma rays [52], where in spite of the progressive increase of dielectric conduction with irradiation, no statistical differences in the constant voltage stress lifetime distributions where found between non-irradiated and gamma irradiated samples up to total ionizing doses comparable to our studies (30 Mrad(Si)) [52]. This is not the case for heavy ion irradiations, where a progressive reduction of oxide lifetime with irradiation was reported [52]. This reduction was explained in terms of possible weaker areas in the oxide films related to the heavy ions damage tracks, which may suffer from enhanced degradation when subjected to the subsequent electrical stress. Moreover, the dielectric reliability was found to decrease with increasing ion energy transfer or ion fluence [53-55]. In our work, the studied 2 MeV electron irradiations effects are found to be similar to gamma irradiations. Finally, it is known that device reliability decreases with increasing temperature [56] and the obtained V_{bd} values were indeed significantly dependent on the measurement temperature. In this way, $|V_{bd}|$ reductions of about 1 V or 1.5 V were typically observed for both, non-irradiated and irradiated samples, when increasing the measurement temperature from -30ºC to 100ºC.

4. Conclusions

The effects of 2 MeV electron irradiation on the capacitance-voltage (C-V) and current-voltage (I-V) characteristics of metal-oxide-silicon capacitors with three different atomic layer deposited (ALD) high-k dielectrics (Al_2O_3, HfO_2 and a nanolaminate of them) have been evaluated. Similar radiation-induced generation rates for positive trapped charges and interface states have been obtained for all the studied high-k dielectric layers. While a radiation-induced increase of the C-V curves hysteresis is observed for the irradiated Al_2O_3, this is just the opposite for HfO_2 and the irradiation has little impact on the hysteresis of the nanolaminate stack. All the studied dielectric layers showed a progressive increase of the leakage current with electron irradiation dose and Poole-Frenkel emission has been identified as the dominant conduction mechanism. In spite of the radiation-induced damage affecting the C-V and I-V characteristics, no impact of 2 MeV electron irradiation fluence on dielectric breakdown voltage has been appreciated by means of ramped voltage measurements.

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Figure captions

Figure 1: C-V characteristics measured from inversion to accumulation (lines) and accumulation to inversion (symbols) for Al_2O_3 MOS capacitors on 1 Ω·cm p-type silicon substrate. The different curves correspond to non-irradiated and 2 MeV electron-irradiated devices at different fluences. The corresponding measured conductance characteristics are given in the inset. Capacitor area is $2.304 \cdot 10^{-3}$ cm^2.

Figure 2: Extracted (a) effective trapped charges (N_{eff}) and (b) interface states (D_{it}) densities for non-irradiated and 2 MeV electron-irradiated Al_2O_3, HfO_2 and nanolaminate MOS capacitors on p-type and n-type silicon substrates.

Figure 3: Magnitude of C-V curve hysteresis for non-irradiated and 2 MeV electron-irradiated Al_2O_3, HfO_2 and nanolaminate MOS capacitors on p-type and n-type silicon substrates.

Figure 4: Current density (J=I/Area) versus applied voltage measured for (a) Al_2O_3, (b) HfO_2 and (c) Nanolaminate MOS capacitors on n-type silicon substrates. The different curves correspond to non-irradiated and 2 MeV electron-irradiated devices at different fluences and measured at various temperatures. Capacitor area is $1.44 \cdot 10^{-4}$ cm^2.

Figure 5: Current density versus applied voltage measured at -30ºC for Al_2O_3, HfO_2 and nanolaminate MOS capacitors of five different areas irradiated at a fluence of $1 \cdot 10^{16}$ e/cm^2.

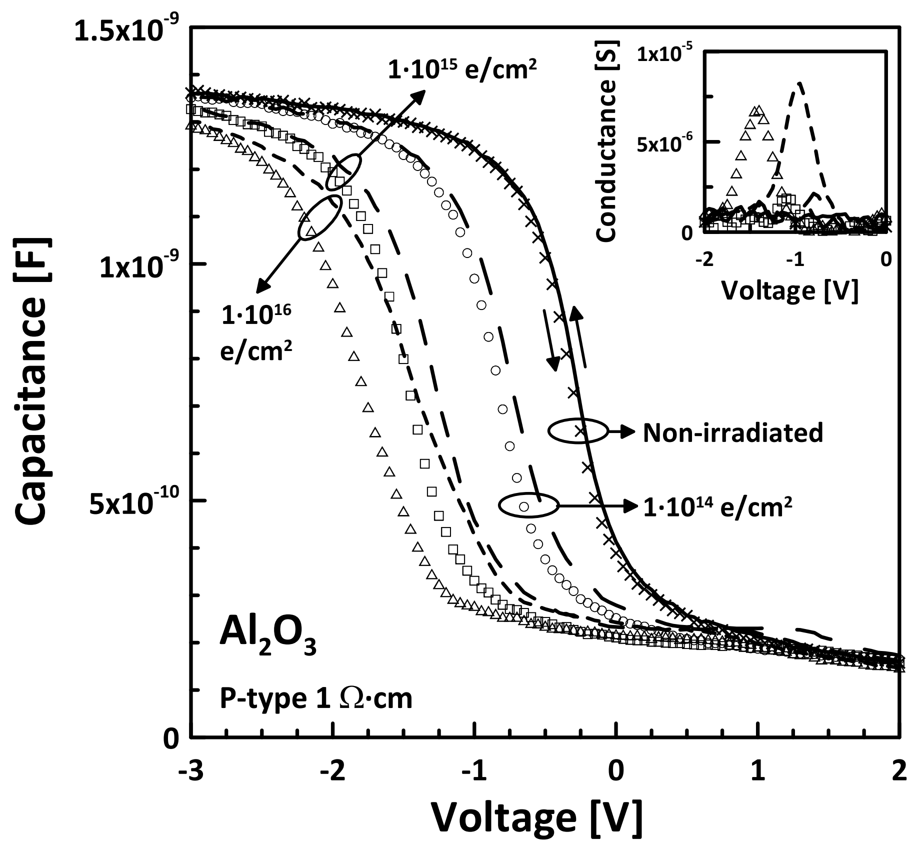
Figure 6: Absolute value of the electron irradiation-induced voltage shift of the current-voltage characteristics at a fixed current density level of $1 \cdot 10^{-5}$ A/cm^2 for Al_2O_2, HfO_2 and nanolaminate MOS capacitors on the different p-type and n-type silicon substrates studied.

Figure 7: Dependence between measured leakage current and electric field for non-irradiated HfO_2 MOS capacitors on p-type Si, fitting the Poole-Frenkel model at different temperatures (eq. (2), broken lines). The leakage current at an $E^{1/2}$ value of 1300 $(V/cm)^{1/2}$ is plotted against 1/T in the inset. Capacitor area is $1.44 \cdot 10^{-4}$ cm^2.

Figure 8: Dependence between measured leakage current at 20ºC and electric field for non-irradiated and 2 MeV electron irradiated Al_2O_3, HfO_2 and nanolaminate MOS capacitors on (a) p-type Si and (b) n-type Si, fitting the Poole-Frenkel model (eq. (2), broken lines). Capacitor area is $1.44 \cdot 10^{-4}$ cm^2.

Figure 9: Activation energies, derived from Poole-Frenkel plots corresponding to different measurement temperatures, as a function of square root of the electric field for (a) p-type and (b) n-type Si. (c) Extracted Poole-Frenkel barrier height or trap level energy (ϕ_B in eq. (2), intercept with energy axis corresponding to $E^{1/2} = 0$) for non-irradiated and irradiated Al_2O_3, HfO_2 and nanolaminate MOS capacitors on p-type and n-type silicon substrates.

Figure 10: Dielectric breakdown voltages (V_{bd}) for Al_2O_3, HfO_2 and nanolaminate MOS capacitors on p-type and n-type silicon substrates as a function of electron irradiation fluence for three different measurement temperatures (-30ºC, 20ºC and 100ºC). Capacitor area is $1.44 \cdot 10^{-4}$ cm^2.



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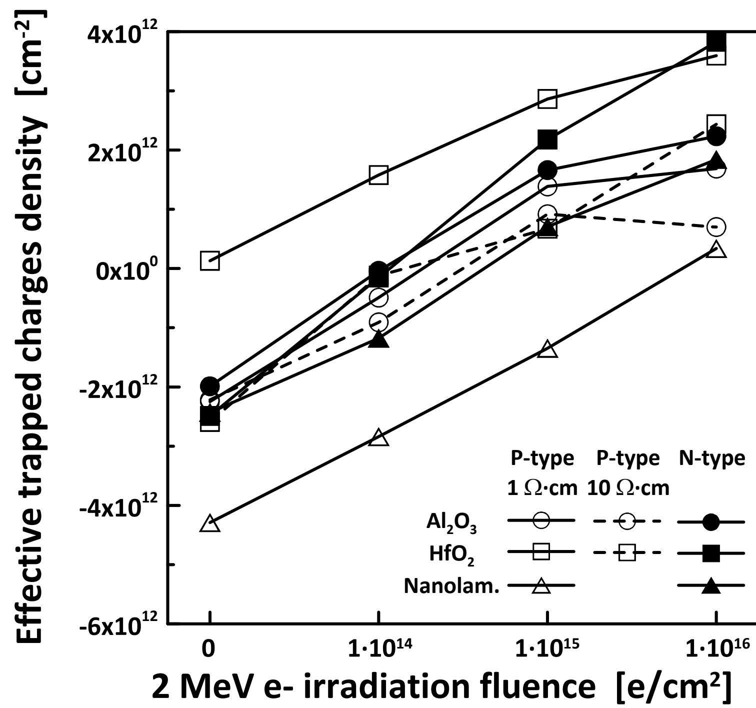

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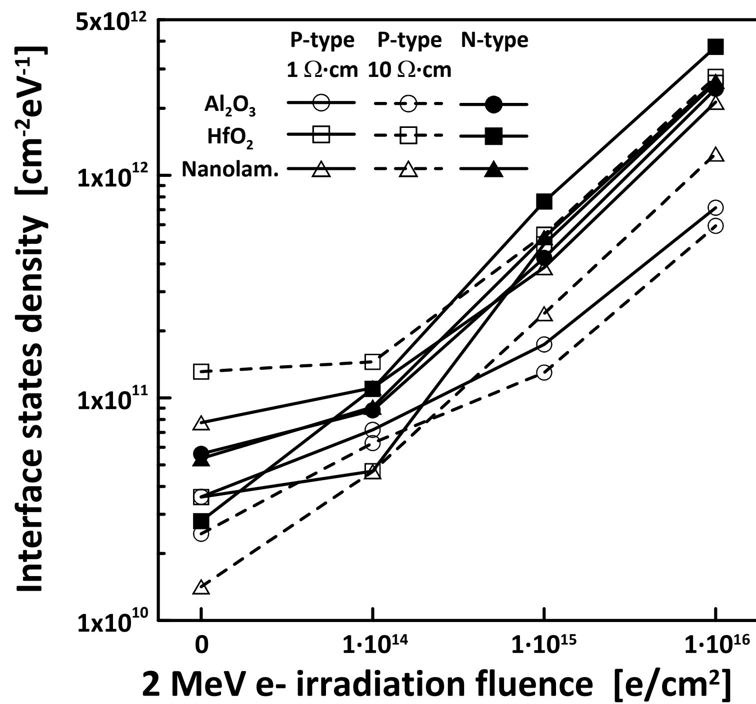

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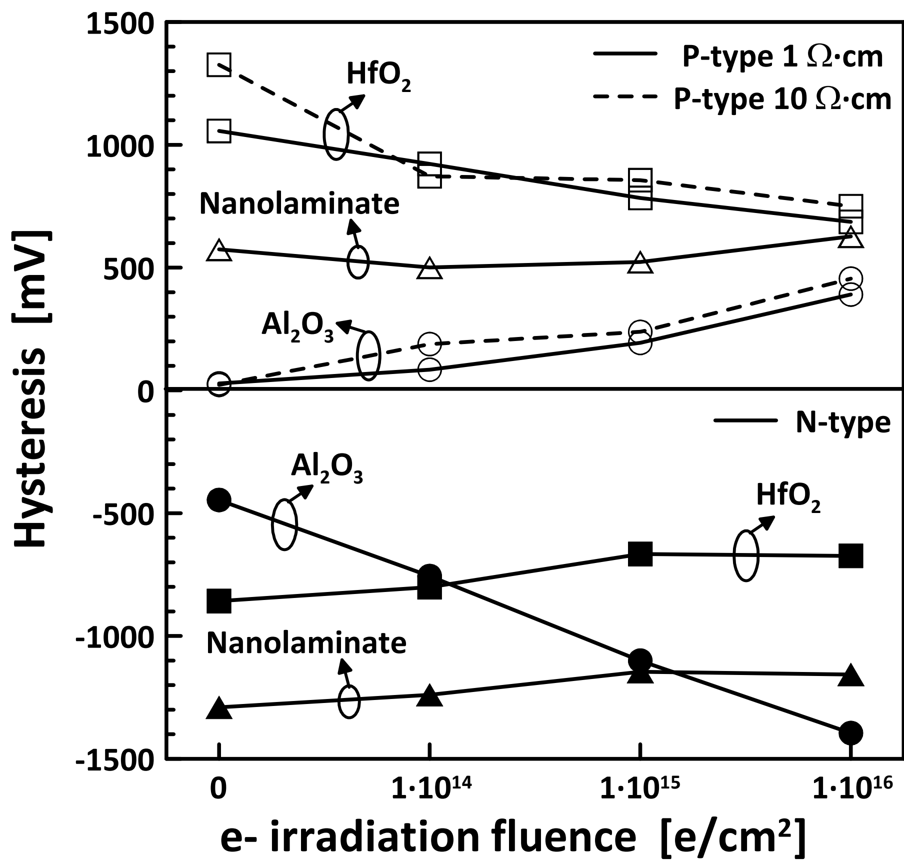

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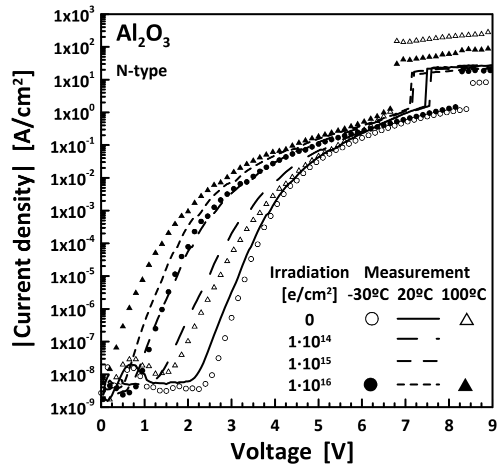


Figure 4(a)

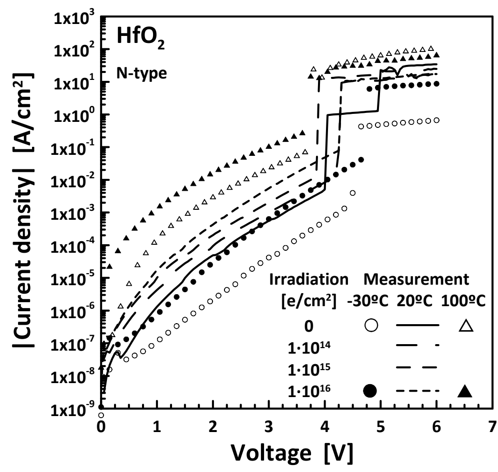
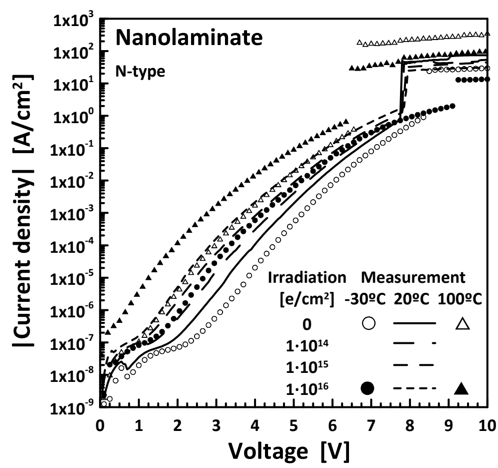


Figure 4(b)



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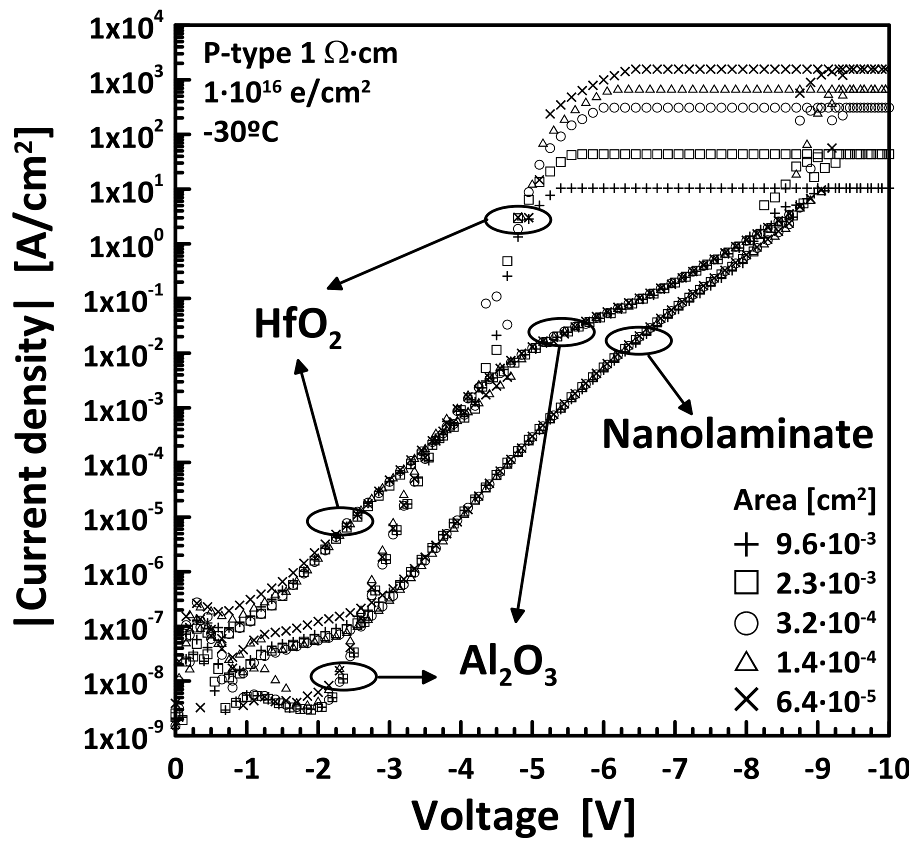
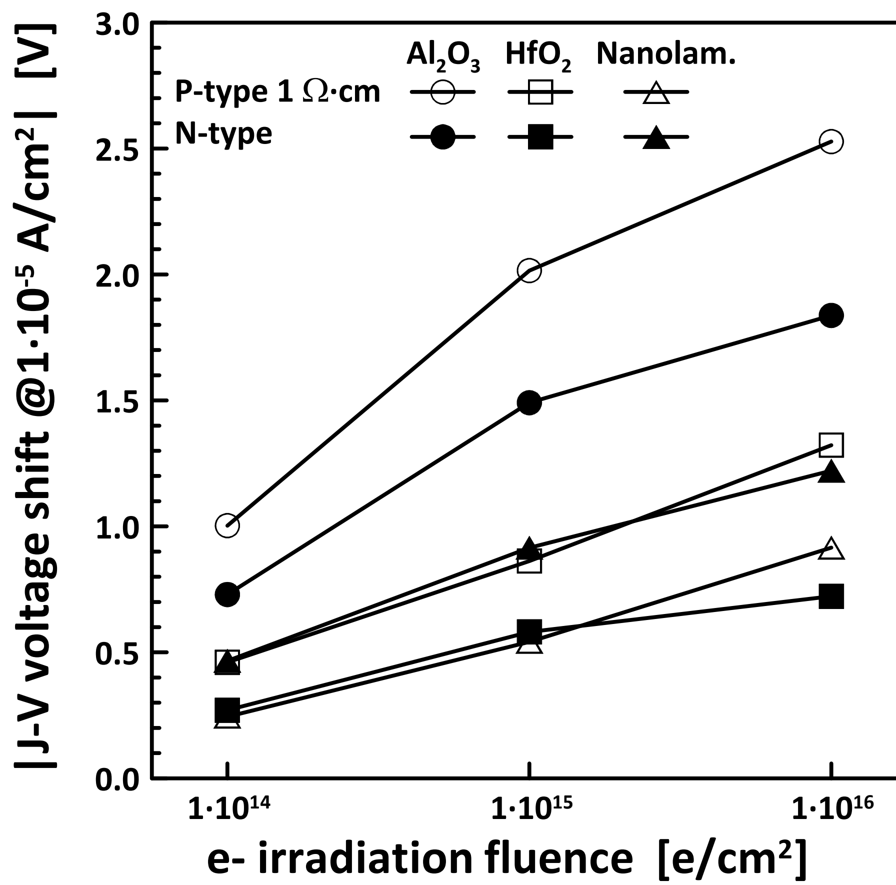


Figure 5



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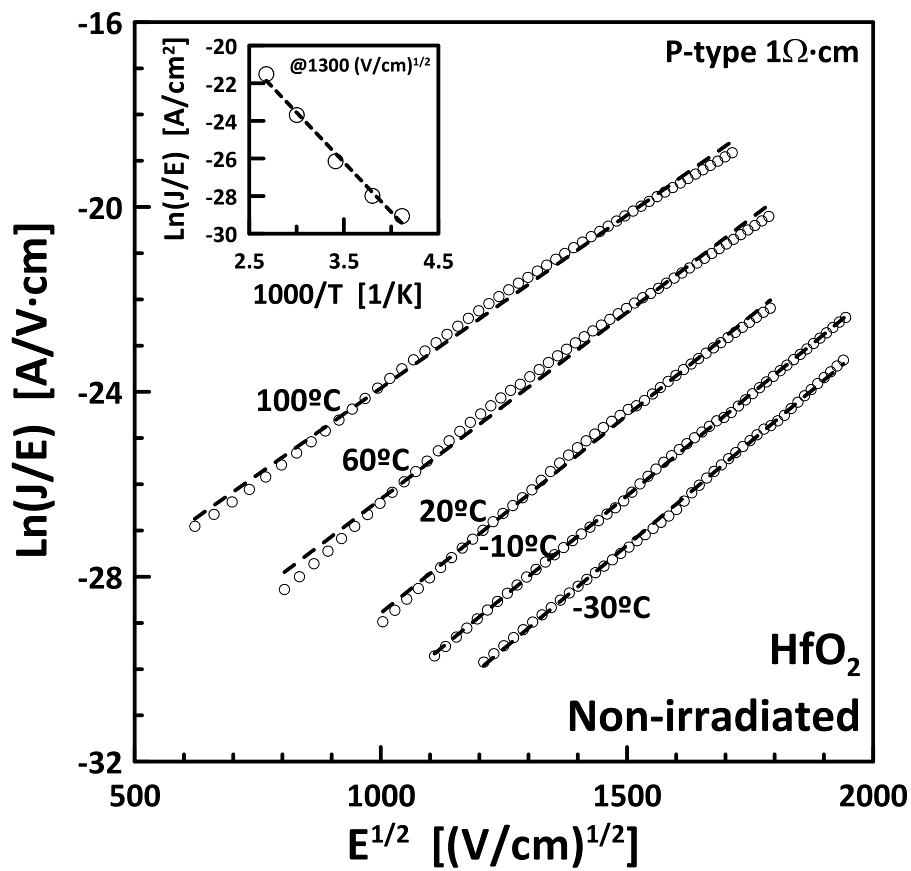


Figure 7

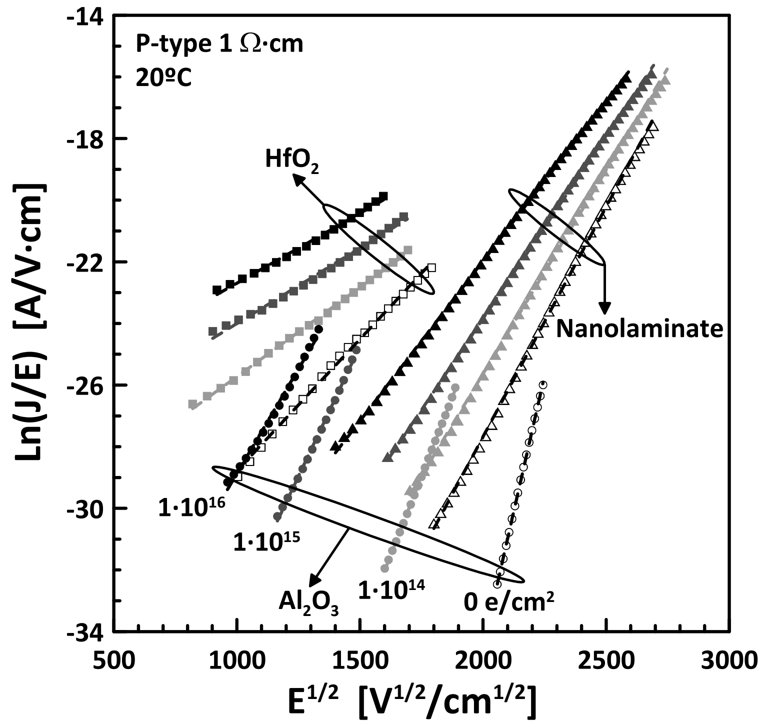


Figure 8(a)

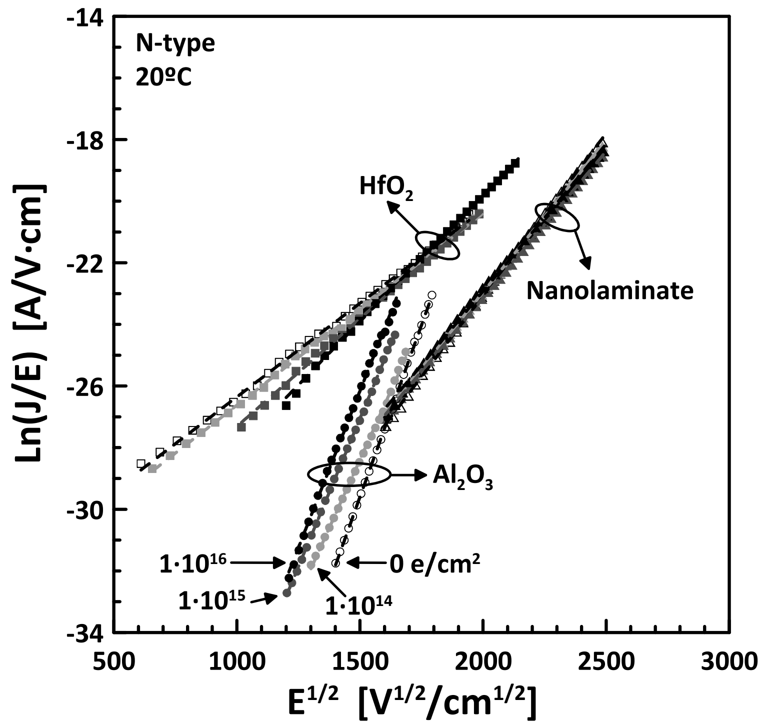


Figure 8(b)

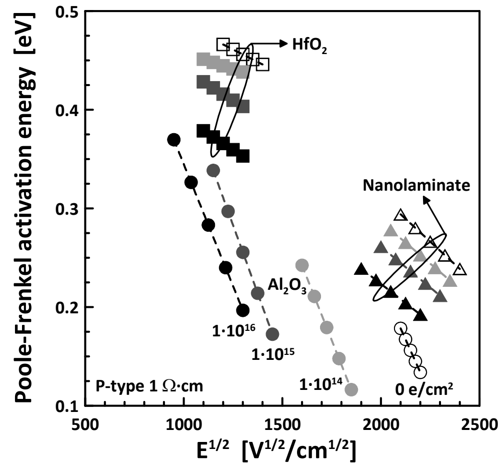
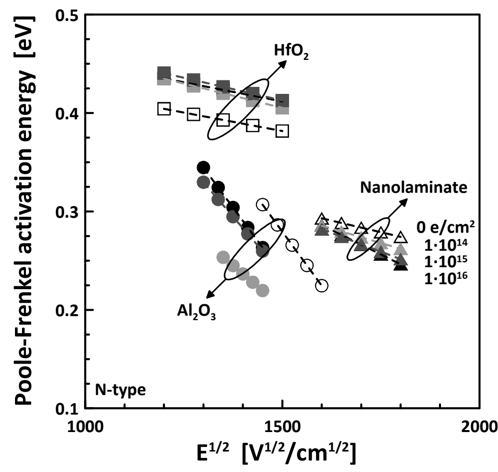


Figure 9(a)



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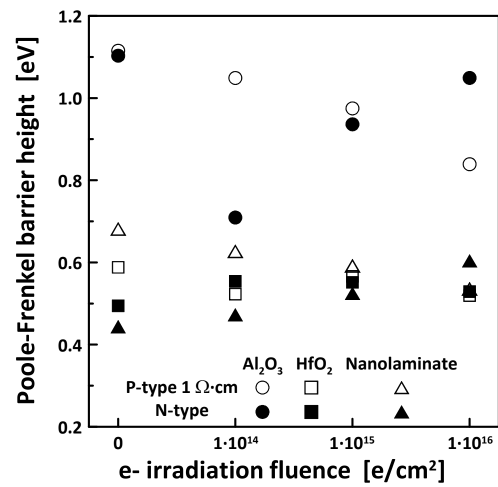

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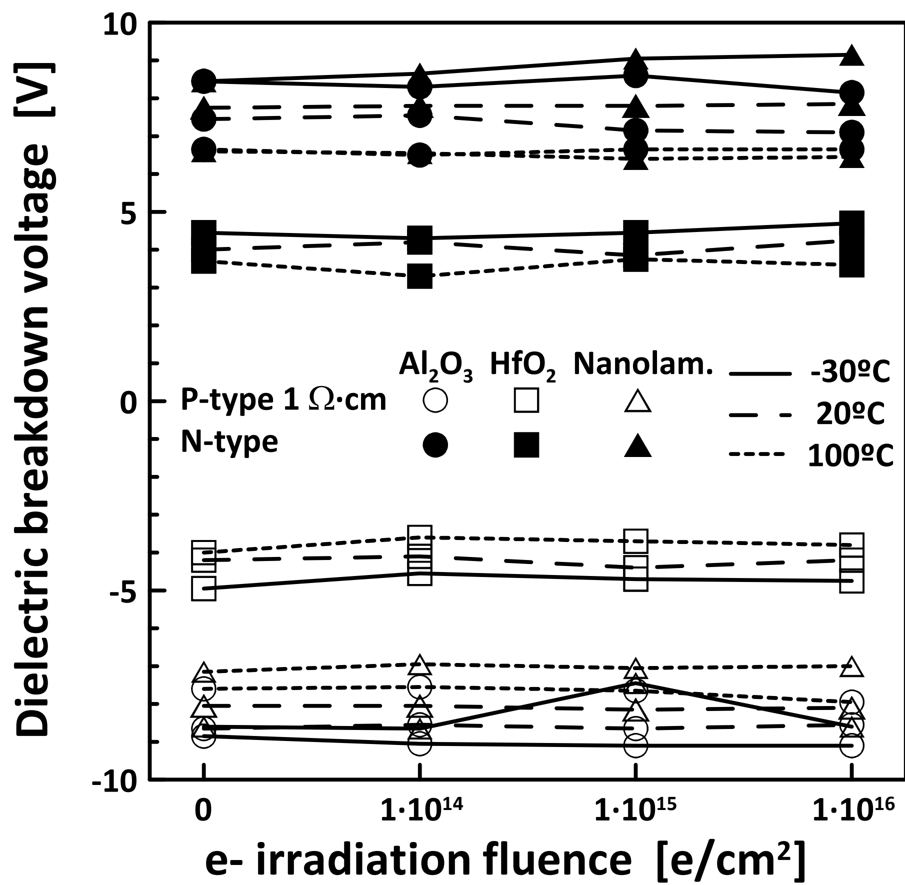

Figure 10