

Memory-in-pixel circuit with low temperature poly-Si and oxide TFTs

Jongbin Kim<sup>1</sup>, Hoon-Ju Chung<sup>2</sup>, Seung-Woo Lee<sup>1</sup>

<sup>1</sup>Dept. of Information Display, Kyung Hee University, Seoul, South Korea

<sup>2</sup>School of Electronic Engineering, Kumoh National Institute of Technology, Gumi, Gyeongbuk, South Korea

1. Introduction

Memory-in-pixel (MIP) circuit has been studied for years to reduce power consumption of display products. Displays with MIP circuit can reduce power consumption because of their much lower frame rate than that of conventional displays using memory characteristics. Meanwhile, commercial display products have begun to introduce display circuits using low temperature poly-silicon and oxide (LTPO) TFTs to improve the performance and to use an advantage of extremely low leakage current of oxide TFTs. In this paper, we propose a new MIP circuit to achieve low power consumption as well as high reliability using LTPO TFTs.

2. Proposed Pixel Circuit

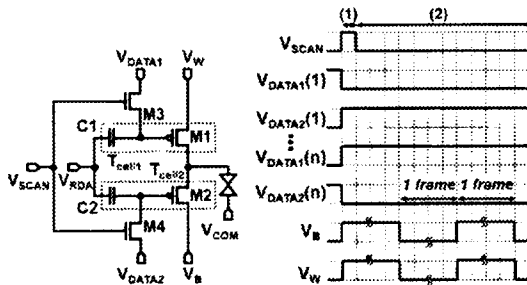


Figure 1: Proposed circuit and its driving signals

Figure 1 shows the proposed MIP circuit. M1 and M2 are driving TFTs using p-type LTPS TFTs, which drive the pixel with black ( $V_B$ ) and white voltage ( $V_W$ ), respectively. M3 and M4 are switching TFTs to program voltages to the gate nodes of M1 and M2, respectively. They are n-type oxide TFTs.  $T_{cell1}$  comprises M1 and C1.  $T_{cell2}$  is composed of M2 and C2. Each one acts like a memory cell. During (1),  $V_{DATA1}$  and  $V_{DATA2}$  can be applied to the gate nodes of the driving TFTs when  $V_{SCAN}$  turns on the oxide TFTs, M3 and M4. During (2), the oxide TFTs maintain the gate voltages of M1 and M2 until next program time.

3. Result and Discussion

Figure 2 shows transfer characteristics of a p-type low temperature poly-silicon (LTPS) TFT and an n-type oxide TFT. The proposed MIP circuit was verified with Spice simulation by using the fabricated LTPO TFTs as shown in Figure 3. At the 1st program,  $V_{DATA1}$  and  $V_{DATA2}$  were -10 V and 6 V, respectively. Thus, threshold voltage ( $V_{TH}$ ) of  $T_{cell1}$  was shifted in the positive direction. On the contrary,  $V_{TH}$  of  $T_{cell2}$  was negatively shifted. We could observe that the pixel voltage reached  $V_W$  (5 V) at the 1st program and

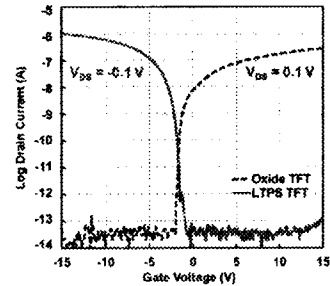


Figure 2: Transfer characteristics of LTPO TFTs

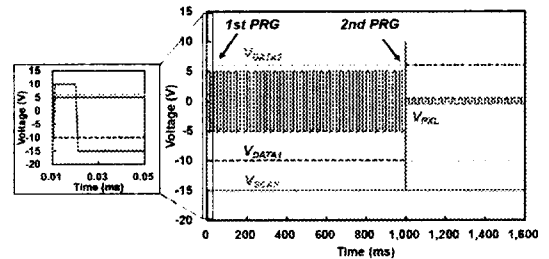


Figure 3: Simulation results of the MIP circuit

the polarity inversion was performed until the 2nd program. The oxide TFTs can maintain the programmed voltages for a long time due to extremely low leakage current. Thus, the frame rate can be quite reduced than that of conventional displays. As shown in Figure 3, we have successfully verified the operation at the low frame rate of 1 Hz. Furthermore, the driving TFTs use LTPS TFTs showing high reliability. They are stable under high voltages for a long period of time. Therefore, we expect that our proposed MIP circuits will contribute to high performance displays featuring low power consumption as well as good reliability. We will present the measurement results later.

4. Acknowledgements

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5. References

- [1] S.-H. Lee, B.-C. Yu, H.-J. Chung, and S.-W. Lee, "Memory-In-Pixel Circuit for Low-Power LCDs Comprising Oxide TFTs," IEEE EDL, Vol. 11, No. 11, pp. 1551-1554, 2017.
- [2] S. Kim, S.-H. Lee, H.-J. Chung, and S.-W. Lee, "Multi-Level Memory Comprising Only Amorphous Oxide TFTs," IEEE J-EDS, Vol. 7, pp. 575-580, 2019.