Metallization of Vias in Silicon Wafers to Produce Three-Dimensional Microstructures

A. I. Vorobjova
V. A. Labunov
E. A. Outkina,
D. V. Grapov

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Belarusian State University of Informatics and Radioelectronics

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Abstract: The processes of electrochemical deposition into a matrix of vertical vias of different diameters (500–2000 nm) in Si/SiO_2 substrates with a TiN barrier layer at the bottom of the holes are studied. Morphological studies of the metal in the holes show that the structure of copper clusters is rather uniform and is formed from crystallites of ~30 to 50 nm. Repeatability and stability with a homogeneous structure and with holes filled 100% by Cu determine the prospect of using the $Si/SiO_2/Cu$ system as a basic element for creating three-dimensional micro- and nanostructures, as well as for the 3D assembly of IC crystals.

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