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Prospects and Challenges of 4H-SiC Thyristors in Protection of HB-MMC-VSC-HVDC Converters

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ABSTRACT Pole-to-pole DC faults on HB-MMC-VSC-HVDC schemes impose significant risk of cascade failure on IGBT/diode pairs. Other novel topologies with fault blocking capability, i.e. AAC converters, and DC circuit breakers are not yet fully matured. Therefore, silicon thyristors are used to bypass the DC faults until AC breakers activate. However, silicon thyristors are also at risk of failure due to the capacitor voltage collapse at high junction temperatures caused due to imbalanced reverse recovery current conduction. Hence, the recovery cycles are included as part of IEC standard 62 501 HVDC type-test program. Emergence of commercial Silicon Carbide (SiC) thyristors has the potential to tackle this risk. This paper investigates such opportunities and challenges by accurately modeling the performance of thyristors at fault. It was seen that SiC thyristors with acceptable surge current and reverse blocking capability can eliminate the failure mode of silicon thyristors due to minimal recovery stored charge, resulting in an equal share of reverse voltage on all thyristors.

INDEX TERMS HVDC, power semiconductor devices, silicon carbide, thyristor, VSC.

I. INTRODUCTION

THYRISTORS are arguably the most rugged power semiconductor devices. They are capable of conducting currents as high as tens of kiloamperes while blocking voltages as high as several kilovolts. These robust characteristics makes them an attractive choice in grid-level applications where such high-voltage high-current features are vital. Although they became commercially available in 1950 s by GE, it was not until 1970 s that they were first used in a line-commutated high voltage direct current converter (LCC-HVDC) in Canada to replace thyratron valves [1]. In addition to improved efficiency, a key feature which makes them attractive for HVDC is the excellent robustness under high surge currents. The devices used in LCC-HVDC applications typically utilize the entire width of a silicon wafer with diameters up to 6-inch [2]. Nevertheless, there are recent applications, such as grid connection of offshore wind farms, where LCC-HVDC systems cannot be used due to limitations such as inability to operate at weak AC systems. Development of voltage source converters (VSC-HVDC) with hundreds of self-commutated insulated gate bipolar transistors (IGBTs) and capacitors connected in series in early 2000 s provided an alternative choice [3]. It is now anticipated that up to fifty percent of future HVDC projects will be developed by the VSC technology. However, despite all the advantages of VSC-HVDC, the use of IGBTs instead of thyristors subjects the converter to higher risk of cascaded failure in case of over-current transients. Therefore, it is vital to ensure that adequate protection is implemented to avoid catastrophic consequences. To this end, alternative topologies are developed to tackle this shortcoming while DC circuit breakers are also proposed to isolate DC fault [4].

In short, none of these solutions are presently adequately mature. So, parallel thyristors, including press-pack silicon thyristors [5] are currently required to bypass the surge

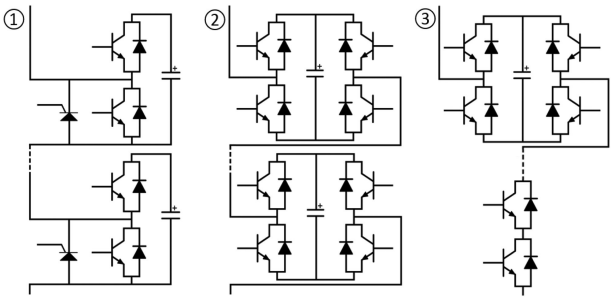

FIGURE 1. 1. HB with protective bypass thyristor, 2. FB without the need for a bypass thyristor and 3. Hybrid AAC.

transients from the IGBT/diode pairs, i.e. in the event of a pole-to-pole DC fault on the DC cables. This is currently the most practical protection method despite the additional costs imposed by hundreds of additional thyristors. Operation of silicon thyristors may also result in excessive electro-thermal stress with potential risk of widespread thyristor failures [6].

Recent commercialization of Silicon Carbide (SiC) thyristors has raised speculations on whether using SiC thyristors as a bypass switch has the potential to address the shortcomings of silicon thyristors in protection of VSC units, given the favourable characteristics of SiC thyristors such as low recovery charge and higher junction temperature.

This paper aims to investigate the industrial challenge of unbalanced reverse recovery charge across series-connected silicon thyristors immediately after fault bypass and the possibility of cascaded failure of the thyristors. It will evaluate the characteristics of SiC thyristors under the same scenario and provides a comparative analysis. Section II discusses the characteristics of DC faults; section III discusses the features of state-of-the-art SiC thyristors; section IV discusses the opportunities and challenges of implementation of SiC thyristors in VSC units; section V provides analysis of performance of silicon and SiC thyristors at faults while section VI concludes the paper.

II. MMC-VSC-HVDC CONVERTERS AT DC FAULTS

The initial VSC-HVDC converters had two-level and three-level structures. These were simpler to control, however had many challenges as hundreds of series-connected devices had to be switched simultaneously [3]. They also had poor harmonics, requiring large filters similar to LCC converters. These led to the development of modular multi-level converters (MMC) with isolated voltage-sourced units creating sinusoidal voltages with little, if any, filtering requirement.

The half-bridge (HB) units are shown in Fig. 1.1 are fundamental building blocks of converters. Hundreds of series-connected units with ratings of a few kV each are necessary to support a typical line-to-line voltage of ±320 kV. As seen, each bottom diode has a parallel protective thyristor [1]–[4], [6] to bypass the fault current due to the lower on-resistance of thyristors compared with diodes. The full bridge unit is shown in Fig. 1.2 with four IGBT modules. This enables them to have

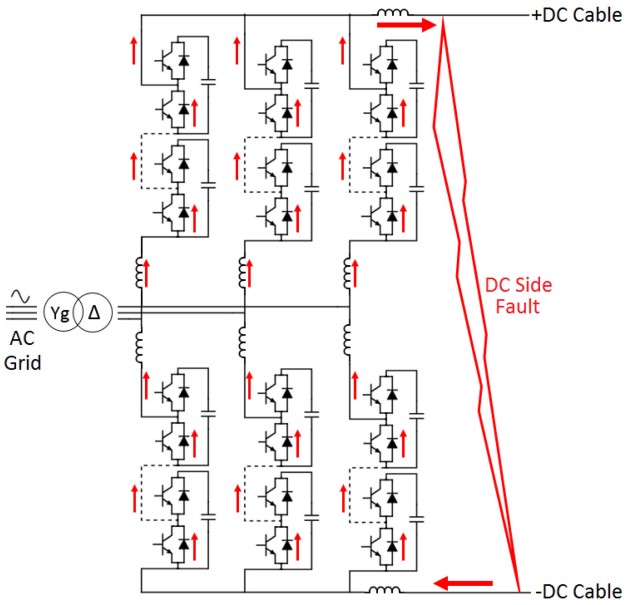

FIGURE 2. The pathways for DC fault current in absence of protective bypass thyristors.

a bipolar output by reversing the polarity of capacitor voltage and consequently suppress the DC fault by imposing the significant impedance of charged capacitors in its path. The disadvantages of this topology are higher capital cost and higher losses due to duplicated number of IGBTs. To tackle these shortcomings whilst maintaining the fault blocking capability, a hybrid structure shown in Fig. 1.3, called Alternate Arm Converter (AAC is proposed [7]. Full-bridge voltage units in this structure conduct only in half of each period controlled by the director switch which constitute series-connection of many individual IGBTs. Therefore, the number of required full-bridge voltage units is halved, so the conduction losses are comparable to that of HB-MMC topology while fault blocking capability is restored. Nonetheless, control of AAC converter is a challenge, in addition to potential DC output ripples when alternating conduction arm. Other topologies are proposed too, most of which are complex. Examples are clamped double cell (CDC), cross connected cell (CCC), and mixed topologies [8].

Fig. 2 shows the HB-MMC-VSC-HVDC converter structure with 6 valves in the 3 phases. The AC breakers promptly interrupt AC side faults while the DC pole-to-ground faults are also manageable by AC breakers due to the significant ground connection impedance. However, a pole-to-pole DC fault, as shown in Fig. 2, imposes a significant risk. Such DC cable fault is rare, however it becomes more likely when overhead lines are used such as in Ultranet project in Germany [9]. The bottom anti-parallel diode provides a low resistance path for the DC fault current to circulate across all bottom IGBT/diode modules. This could result in cascaded failure of devices, especially as the devices initially fail short-circuit as in Fig. 3. Only when the surge current raises further the wire-bonds are destroyed and the short-circuit turns into an open-circuit.

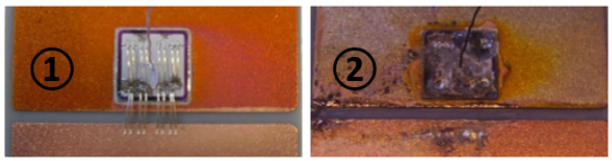

FIGURE 3. 1. Short-circuit failure vs. 2. Open-circuit failure of power module wire-bonds [10].

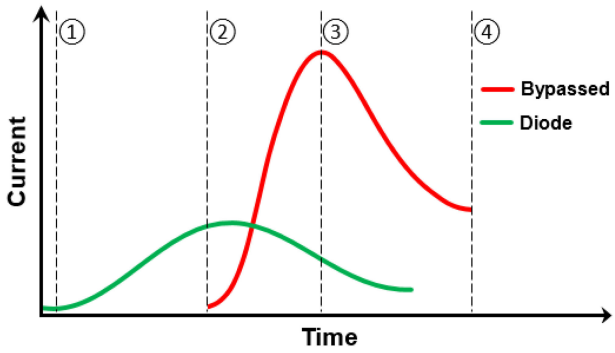

FIGURE 4. Fault current bypassed into the protection thyristor.

As seen in Fig. 2, there are two types of inductors in the path of the fault current. The first is the arm inductor normally in range of 50 to 100 mH, and the second is the DC line inductor normally in range of 10 s of mH. The total inductance in fault current's path limits its rate of raise (dI_F/dt) and provide time for current transducers to detect the fault [11], [12]. To interrupt the current, two methods are considered in literature. First, a DC circuit breaker could be initiated [9]. Second, using alternative topologies such as a Full-Bridge (FB)-MMC topology or a hybrid topology like AAC, that reverses the polarity of capacitance voltage in the fault current path. Presently, the DC circuit breakers are still in development, i.e. ABB's first commercial HVDC breaker was introduced in 2012 that required a reaction time of 5 ms [3] while since June 2020, ±500 kV MMC-HVDC grid with HVDC breakers has been in service in China. These breakers are expensive due to their requirement for series connection of hundred of high voltage devices. Ensuring simultaneous switching of all devices can be complex. In addition, the use of FB-MMC also imposes direct and indirect cost on the design of converter.

Unlike the above-mentioned solutions, a bypass thyristor does not mitigate the fault current but provides a safe bypass path. As indicated in Fig. 4, as soon as the current in each arm reaches a pre-defined value, the thyristors will be fired, and the current is diverted. This transpires in four steps as described as indicated in Fig. 4:

1) DC fault occurs and current starts to rise in the diode.
2) Current reaches pre-defined value and thyristors fire.
3) Fault increases while mostly bypassed in thyristors.
4) AC breakers disconnect and converter turns-off.

Thyristors are bipolar devices with some stored charge in space-charge region, especially in silicon devices due to the high carrier lifetime in wider regions. This recovery imposes additional stress on the thyristors. Fig. 5 describes the sequence of events following a fault:

1) Initially, all capacitors in the HB-MMC are charged. Some contribute to the overall voltage through the upper IGBTs whilst others are bypassed by bottom diode.
2) At instigation of fault, current in the converter arm rises which is fed back to the controllers using current transducers.
3) Once the current reaches a pre-defined value, IGBTs turn-off and all thyristors are fired simultaneously. The current flowing through the bottom diodes result in a voltage that forward bias the thyristors. Therefore, the forward blocking capability of thyristors only need to be a few volts while its reverse capability is in the range of few kilovolts. The on-state resistance of thyristors is typically in an order of magnitude that is lower than diodes. The trigger value is set as per the safe operating areas (SOA). The rate of rise of current, turn-on pace of thyristors and communication delays are also considered in the total delay.
4) Once the fault is over with AC breakers open, the current in the thyristors drops to turn-off. At this point, the junction temperature of the thyristors is very high due to the surge transient. All bipolar devices start reverse recovery in opposite polarity.
5) The diodes have smaller die areas, so their stored charge recovers faster than thyristors which utilize the entire width of a silicon wafer. Therefore, the reverse recovery current continues to conduct only through the thyristors.
6) Due to the variations in outputs of production line, there are slight differences in the recovery charge stored in each individual thyristor. Therefore, some thyristors complete the reverse recovery transient while others are still recovering. At this time, the remaining reverse recovery current flows in the upper diode and through the charged capacitor. The forward bias of the upper diode means that the entire voltage of the capacitor (which up to the moment of fault was at its nominal value) collapses on the thyristor in the reverse polarity, while the thyristor still suffers from a very high junction temperature. This is risky since the thermally-excited carriers have higher mobility and could skip the narrow bandgap of silicon, which could possibly initiate an avalanche breakdown and a potential failure by high electro-thermal stress. This is the rationale of the IEC standard 62 501 that requires the recovery voltage between cycles of fault current, including commutation overshoot, to be implemented in protection type-tests. SiC has very low minority carrier lifetime, so SiC thyristors may eliminate this recovery phase altogether.

III. STATE OF THE ART OF SIC THYRISTORS

Challenges in application of silicon thyristors in protection of HB-MMC-VSC-HVDC converters and recent emergence of commercial SiC thyristors have initiated a debate on whether these devices could provide a better alternative to

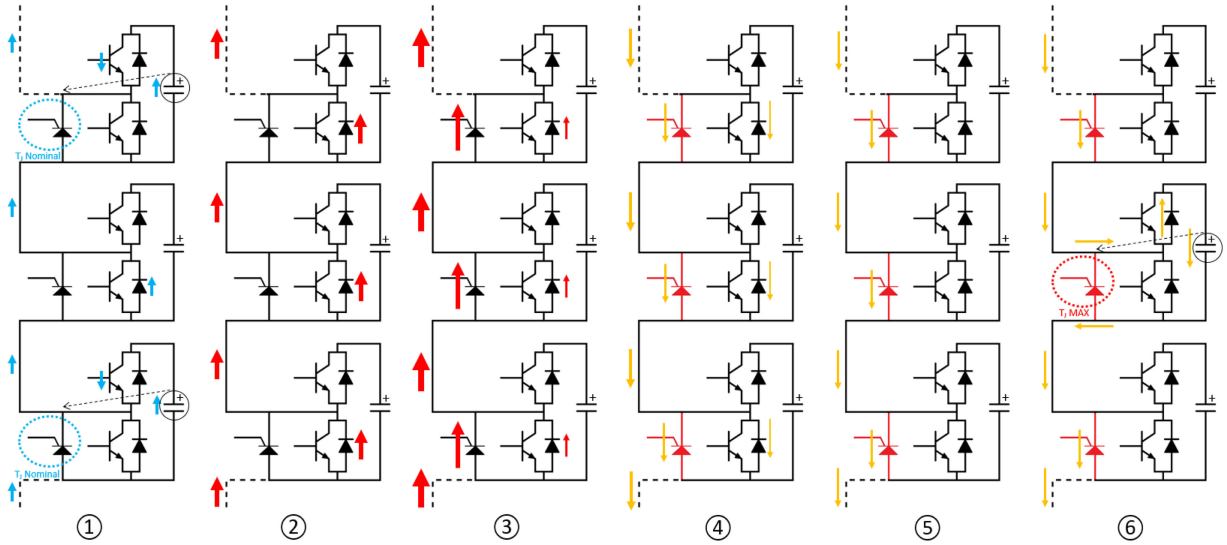

FIGURE 5. **1. Normal operation, 2. Instigation of Fault, 3. Thyristors Fired, 4. Fault removed, and devices recover (yellow arrows), 5. All diodes recovered, and Thyristors continue to recover, 6. Some thyristors recovered while others are still recovering.**

conventional thyristors. The principals that make SiC an attractive choice in fabrication of power devices is extensively discussed [13]–[16]. Many standard and gate turn-off (GTO) SiC thyristors have been developed in recent years. In 2001, 3 kV & 12 A PNPN asymmetric SiC super gate turn-off thyristors (SGTO) were introduced [17], [18]. This was followed by development of 4.5 kV SiC SGTO [19], [20], 9 kV SiC SGTO in 2009 [21] and 12 kV SiC thyristor in 2012 [22]. Since then, even higher ratings are demonstrated in laboratories worldwide, i.e. 10 kV 4H-SiC GTO [23], 12.7 kV 4H-SiC commutated gate turn-off thyristor (SICGT) [24], 13 kV SiC emitter turn-off thyristor (ETO) [25], 15 kV SiC ETO [26], 18 kV 4H-SiC thyristor [27], and a 22 kV SiC ETO [28]. Designs for 30 kV SiC thyristors [29], SiC anode switched thyristor (AST) [30]. 4H-SiC field-controlled thyristors (FCT) [31] are also available, while 6.5 kV SiC thyristors such as GeneSiC's GA080TH65 are already available in commercial market. The high critical electric field and wide bandgap in SiC are crucial advantages for grid-level heavy-duty power electronics. However, SiC material challenges impact rapid fabrication of devices. The low diffusion length of P-type acceptors has led to absence of thick ($\sim$1.5 mm) acceptor diffused substrates by ion implantation while the phase vapour transport (PVT) method is currently being used for doping of 4H-SiC substrates. This technique has better yield for the N-type 4H-SiC substrates but it is still problematic for fabrication of the P-type substrates [32]–[38]. Therefore, SiC bipolar devices especially thyristors are made on N-type substrates to avoid excessive substrate resistance. The P-type drift region of devices is not ideal due to the lower mobility of holes compared with electrons resulting in slower transients and higher on-resistance. Recent development of 4H-SiC with lower crystal defect density (compared with 6H-SiC) has made it the preferred polytype, especially when cut at 8 degrees off axis [39]. Higher isotropic mobility of electrons in 4H-SiC ($>$200%) and higher holes mobility ($>$20%) are also beneficial. Therefore, commercial SiC thyristors are 4H-SiC NPNP, many of which are ETOs driving the GTO with low voltage MOSFETs, enhancing RBSOA merits. Fig. 6 shows the common structures of silicon and SiC thyristors.

The first type of thyristors in Fig. 6 has a symmetric PNPN structure with similar forward and reverse voltage blocking capability which is a common structure in AC power conversion, i.e. LCC-HVDC. The cathode shortings seen in Fig. 6.1 is a feature to increase the forward blocking capability as it delays the avalanche regeneration by reducing the gain of the NPN BJT which has an adverse impact on the base current necessary to maintain the regenerative process especially at higher current levels. Fig. 6.2 shows an NPNP structure with a highly doped thin (a few μm) P-type drift layer to minimize the on-state resistance and avoid a reach-through turn-on. This converts the shape of electric field from triangular into trapezoidal, enabling blocking of higher forward voltage with smaller on-resistance. This structure, however, is unable to withstand any significant reverse voltage as both junctions between the P-anode and N-base and the P-buffer and N-substrate are highly doped and the electric field at the junction rapidly approaches the critical electric field. Fig. 6.3 shows an asymmetric PNPN GTO with anode shortings (transparent emitter). The GTO's highly doped P^+ gate regions assist 'stealing' of the anode current at turn-off. Therefore, applying a reverse polarity voltage on the gate turns off the device. The anode-shorts enable fast turn-off with minimized recovery charge, though eliminating the reverse blocking capability. Finally, Fig. 6.4 shows an asymmetric NPNP GTO with buffer layer as a common 4H-SiC structure with the least on-state resistance and excellent turn-off capability at the price of lack of reverse blocking capability.

Fig. 7 shows typical silicon and SiC thyristors. Silicon thyristors normally utilize the entire width of a wafer, i.e. 2

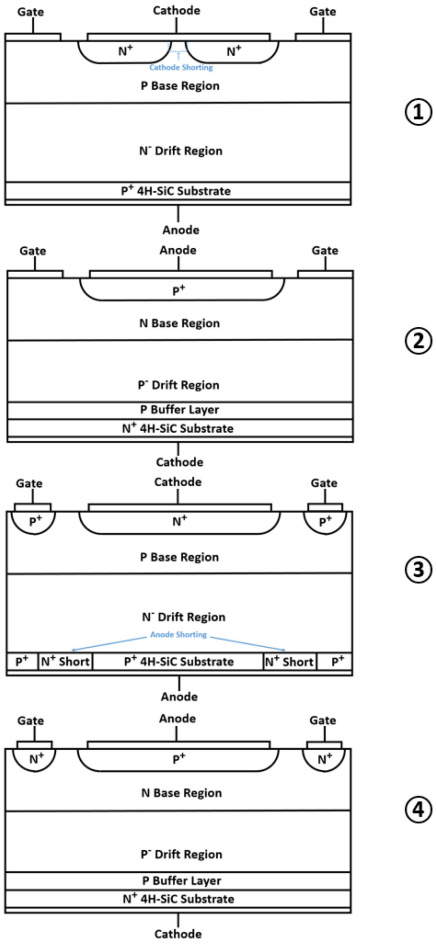

FIGURE 6. 1. Symmetric PNPN thyristor with cathode shorting, 2. Asymmetric NPNP thyristor via buffer layer, 3. Asymmetric PNPN SICGT via anode shorting, 4. Asymmetric NPNP GTO via buffer layer.

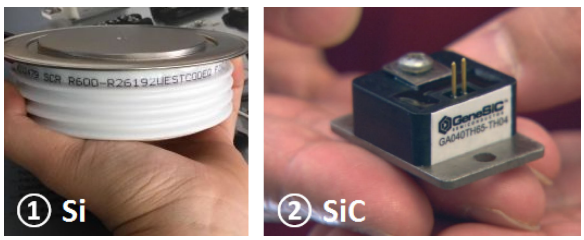

FIGURE 7. 1. Typical ø4″ 6.5 kV Silicon thyristor disk, 2. 6.5 kV Silicon Carbide thyristor in SOT-227 package with 8.2 × 8.2 mm die area cut from a ø3″ 4H-SiC wafer [40].

to 6 inches. In comparison, SiC thyristors, such as GeneSiC Semiconductor's GA080TH65, have lower current ratings with smaller die area due to the difficulties in fabrication of large-area defect-free SiC wafers. The parameters of closely rated Si/SiC thyristors are shown in Table I.

Commonly SiC thyristors are SiC p-ETO by connecting P-type SiC GTO to driving MOSFETs. This provides a unity gain turn-off by redirecting the anode current to the gate, rapidly turning it off. It also enables paralleling SiC GTOs for protection of VSCs due to the positive temperature-slope of driving MOSFETs. SiC ETO also has a lower back-porch

TABLE I Features of Two Closely-Rated Silicon and SiC Thyristors

	4H-SiC	Si
Model	GA080TH65	T201N
Manufacturer	GeneSiC	Infineon
Die Size *(mm)*	8.2×8.2 of ⌀3″ disc	⌀2″ disc
Forward Voltage *(V)*	6500	6500
Reverse Voltage *(V)*	50	6500
RMS Current *(A)*	139	385
Leakage Current (μA)	50	100000
Reverse Stored Charge (μC)	4	3500
Peak Recovery Current *(A)*	20	130
Typical Turn-off dI/dt $(A/\mu s)$	430	30
Turn-off Time (μs)	10	600
Delay Time *(ns)*	50	2000
Maximum Temperature *(°C)*	150	125
On-state Forward Voltage *(V)*	3.7	3.4
A-K Slope Resistance $(m\Omega)$	6.33	4.22
A-K Threshold Voltage *(V)*	3	1.29
J-C Thermal Resistance *(°C/W)*	0.08	0.04

current requirement compared with silicon GTOs. Several failure modes in thyristors are mitigated by the use of SiC ASTs as:

1) Turn-on *dI/dt:* A key failure mode is the rapid increase of current by a high *dI/dt* before the entire width of the wafer or chip conducts. This is less common in silicon GTOs as multiple chips are connected. Commonly, a turn-on reactor limits the *dI/dt*, however this is not useful in protection of HB units as more current flows into the diode. SiC AST with an involute gate ensures no thyristor failures occurs in absence of this reactor as a result of high turn-on *dI/dt* at DC pole-to-pole faults.
2) Turn-off *dV/dt:* As a thyristor turns-off at end of a fault, the capacitor voltage drops on the device as in Fig. 5. Such *dV/dt* may result in an unwanted turn-on, leading to failure. This can also happen when a thyristor in forward blocking mode rapidly shifts into reverse blocking, resulting in a substantial displacement current and space-charge shift. A turn-off *dV/dt* snubber is typically needed. This however, is not required for SiC AST.
3) Dynamic Avalanche: At very high-power limits, a dynamic avalanche may take place, resulting in thermal runaway and failure. The power limits in silicon devices is relatively lower, typically about 200-300 kW/cm^2 [25]. This limit for SiC is so high that other factors, such as packaging temperature limits, will define the SOA.
4) Reverse recovery voltage failure on gate-cathode: High reverse recovery coupled with stray inductance causes breakdown by voltage overshoots on the gate-cathode junction. A low recovery charge in SiC eliminates this.

IV. SIC THYRISTORS AS HB-MMC PROTECTION

To this end, the opportunities and challenges for state-of-the-art commercially available SiC thyristors as protection units of HB-MMC-VSC-HVDC converters are:

A. OPPORTUNITIES

1) REVERSE RECOVERY CHARGE

The main benefit of application of SiC thyristors is to avoid the failure shown in Fig. 5 by means of enabling simultaneous recovery of all thyristors through negligible stored charge and small recovery current. Silicon GTOs are made of many parallel cells to accelerate the turn-off transient, while SiC single-dies inherently has a low carrier lifetime and rapid recombination of minority carriers. Additionally, its high critical electric field means shorter drift region (i.e. 60 μm for a 10 kV SiC GTO [41] and 160 μm thick for a 22 kV device [42]). This means less carriers over a shorter distance, resulting in a faster recovery. As indicated in Table I, the recovery charge of a silicon thyristor is in range of 3500 μC which is very high in comparison to a 4H-SiC thyristor with just 4 μC. Combining this with the peak recovery current (130 A vs. 20 A) and turn-off time (600 μs vs. 10 μs) means that recovery of SiC thyristors is almost instantaneous. Such short turn-off time also enables it to safely withstand repetitive peaks and zero-crossing of faults.

2) JUNCTION TEMPERATURE

SiC devices are able to operate at higher junction temperatures, as it can maintain its semiconductor properties up to 900° C with melting point of 2700° C. In comparison, narrow bandgap of silicon devices limit junction temperature to 125° C with a melting point of 1400° C, although these are largely restricted by the limitations on the interface joints between the die and package. Therefore, the maximum junction temperature of silicon thyristor as listed in Table I is 125° C while for SiC thyristors it is 150° C that provides some extra room for operation. Given the wide-bandgap of SiC, high junction temperatures will not impact its blocking capability. The blocking voltage of a typical silicon thyristor at 300° C reduces by a factor of 90% [43] while this reduction for a SiC thyristor is only 4% [44]. Therefore, the likelihood of failure described in Fig. 5 is lower in SiC.

3) SHORT TURN-ON DELAY TIME

The SiC device has shorter delay time in forming the charge required in the N and P regions during turn-on transient due to smaller device area despite same forward voltage blocking. As seen in Table I, the delay time in silicon thyristor is 2000 ns versus 50 ns for the SiC device. However, the impact of this advantage of SiC over silicon may not be significant on the overall reaction time to DC faults when considering the detection and opening times by the ancillary.

4) LEAKAGE CURRENT

Protection thyristors are permanently connected to the output of HB-MMC voltage units in reverse polarity, so some leakage current is expected. The reverse voltage across the devices in normal conditions is in the range of a few kilovolts. Therefore, the leakage losses of the thyristor must be considered when the total losses of the converter station are calculated, which is in-line with IEC standard 62 751. SiC thyristors outperform silicon devices due to the higher energy required by the carriers to reach conduction band. Looking at Table I, in order of magnitude the leakage current of SiC device is three times smaller than that of the silicon devices. Additionally, spurious turn-on due to high junction temperature and reduction of PN junction built-in voltage will not happen in SiC thyristors. The cosmic ray failures in SiC is also 10 times less than that of silicon devices [45]. Although this can be improved in silicon thyristors at the cost of thicker drift regions, it would increase the on-state drop, resulting in higher share of fault current in diode.

B. CHALLENGES

1) DEVICE STRUCTURE FOR REVERSE BLOCKING

A key issue in commercial SiC thyristors is its asymmetric structure as in Fig. 6. Although low carrier lifetime in SiC leads to low recovery charge, this impedes adequate conductivity modulation in the drift region in on-state, contributing to additional on-resistance. To enable ample conductivity modulation while maintaining the recovery charge as little as possible, SiC thyristors are designed asymmetrically. Enhancing the carrier lifetime results in a lower forward voltage enabling a better protection of diodes by diverting more current into the thyristor. This will also result in higher reverse recovery charge at turn-off with consequences described in Fig. 5.6. However, HVDC applications need a reverse blocking capability without the reach-though effect, and therefore require a symmetric structure without cathode shortings and with wide epitaxial drift region, such as the one shown in Fig. 6.1. Thyristors used for the protection of HB-MMC are only required to block a few volts in forward direction (as the forward voltage drop of diode is only needed to forward bias the thyristor into turn-on) while the reverse voltage is in range of a few kilovolts. This is opposite of standard commercial devices. The additional on-resistance as a result of a symmetric structure has no adverse impact on protection of HB-MMC-VSC-HVDC, as the device only turns-on at point of fault. The additional losses is a trade-off for the higher margin in junction temperature of SiC device.

2) LOW CURRENT HANDLING CAPABILITY

Another significant limitation in the existing commercial SiC thyristors is the low surge current capability. This is mainly due to the high density of micropipe defects in SiC wafers, impeding fabrication of large defect-free SiC discs. Recently, Wolfspeed as a leader in manufacturing of SiC devices, has made substantial progress in reduction of defects and increasing the yield, however the surge current requirements still need purer wafers. This is not a technical limitation, rather a production challenge, and therefore it is deemed that high quality 'kiloamp rated' wafers will become available in foreseeable future. This will also assist overcoming the aforementioned challenge in fabrication of symmetric devices with reverse blocking capability as less defects means less recombination traps and higher carrier lifetime, which would subsequently enable fabrication of thinner symmetric devices.

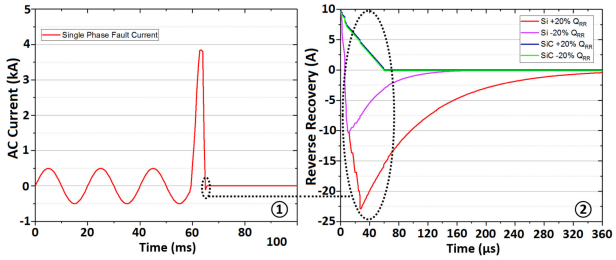

FIGURE 8. 1. Synthesized fault current, 2. Reverse recovery current in silicon and SiC thyristor at +20% and −20% charge profiles.

3) HIGHER THERMAL RESISTANCE

The junction-to-case thermal resistance of the SiC device is twice that of silicon, as shown in Table I. This is due to inferior heat transfer capability of the SOT-227 packaging of SiC thyristor compared to silicon disc enclosure which are be pressure-connected on one or both sides to heatsink. The higher maximum junction temperature of SiC provides some flexibility in managing this until thyristors with full-scale SiC wafers become available.

V. PERFORMANCE ANALYSIS OF THYRISTORS AT DC FAULTS

To understand the complete scope of improvements offered by 4H-SiC thyristors as fault bypass switches in HB-MMC voltage units, accurate modelings have been performed. Symmetrical voltage blocking was considered based on the principal data indicated in Table I. This was undertaken in the MATLAB blockset of PLECS by PLEXIM, a professional power electronics design tool. Five voltage units are connected in series with each other with a current source acting as the source of fault. Each capacitor in the model is 5 mF and charged with 3 kV. The capacitor voltages are used in the VSC converter to build the full line-to-line DC voltage. At the point of fault, due to the short-circuit on the DC cable, the line-to-line DC voltage drops and is assumed to reach half of the normal operation voltage. Therefore, at point of fault the five voltage units block only 7.5 kV instead of 15 kV. The characteristics of the IGBT and diodes are similar to typical rated commercial devices and are the same in these simulations. Fig. 8.1 shows the peak of fault current on the AC supply side. The peak of fault current is 4 kA while the dI_F/dt at turn-off is 20 A/μs. Fault currents may have even more onerous characteristics depending on the fault impedance, with peaks in range of tens of kA with durations as high as hundreds of milliseconds. Fig. 8.2 shows a comparison of the reverse recovery current of the thyristors upon turn-off. As indicated, the SiC thyristor shows almost no reverse recovery while the silicon thyristor shows a significant revere recovery current as indicated by variation of stored charge by 20%. This variation in charge can become a potential source of failure.

Fig. 9 illustrates the impact of charge variation in the five thyristors by means of imposed reverse voltage on the devices. The variations are in steps of 0.1%, 1% and 10% for both

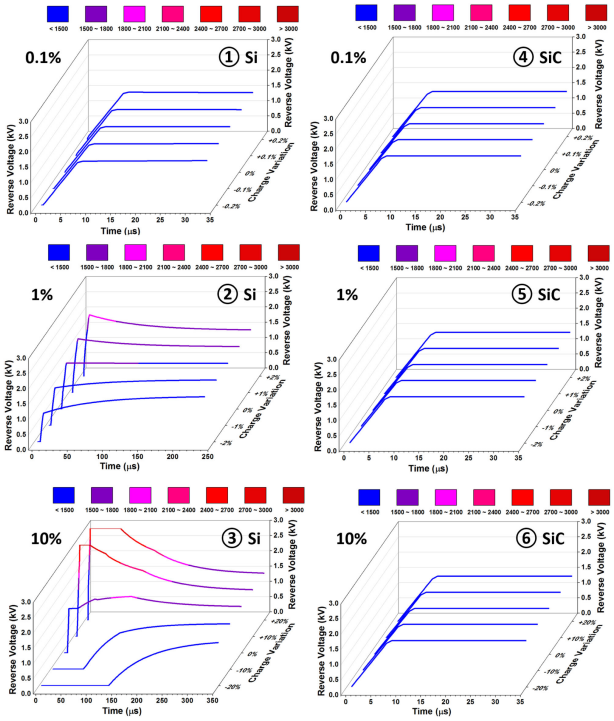

FIGURE 9. The reverse voltage depending on recovery charge variations for 1–3. silicon thyristors and 4-6. SiC thyristors.

the silicon and SiC devices. Fig. 9.1 shows that the reverse voltage on the silicon thyristors with 0.1% charge variation is constant and all five thyristors share nearly identical reverse voltages of 1.5 kV to block the full converter voltage of 7.5 kV. However, as the variation between the stored charges increase, the reverse voltages also start to vary. The thyristors that have recovered earlier will endure higher voltages compared to those that are still recovering. This reverse voltage is capped at the capacitor voltage; therefore, no thyristor has to endure more than the 3 kV on the capacitor. This is clear in Fig. 9.3 where the reverse voltage on the two thyristors with −10% and −20% charge is clamped at 3 kV. The recovery charge in SiC thyristors is almost negligible, so the variations do not have any impact on the reverse recovery current and therefore the reverse voltage on the thyristors is stable at 1.5 kV in all cases. During normal operation, the thyristors will also be subject to capacitor voltage in the reverse direction. However, this reverse voltage immediately after conduction of fault current occurs at very high junction temperatures and with significant *dI/dt* and *dV/dt* which could result in the thyristor failure. This is not the case for SiC thyristor as the reverse voltage at point of reverse recovery is independent of capacitor voltage and solely depends on share of the line-to-line DC voltage which has dropped due to the short-circuit between the DC cables.

In addition to the peak, the time duration that thyristors suffer the reverse voltage should also be considered when selecting the SOA capability. For example, charge variation of 20% results in higher stress compared to 10%, as the duration of the 3 kV reverse voltage is prolonged. This is illustrated in

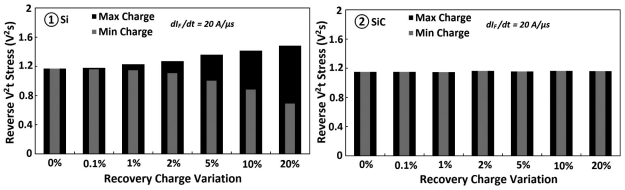

FIGURE 10. The V^2t stress on 1. Silicon and 2. SiC device.

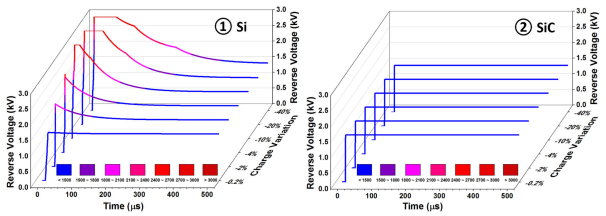

FIGURE 11. The worst-case reverse voltage depending on variations of stored recovery charge for 1. silicon thyristors and 2. SiC thyristors.

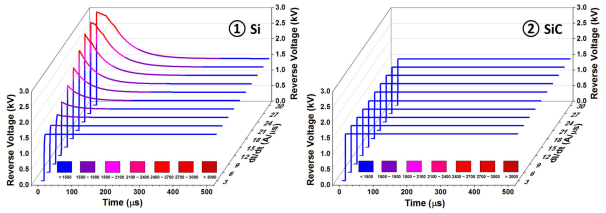

FIGURE 12. The worst-case reverse voltage depending on the dI_F/dt rate for 1. silicon thyristors and 2. SiC thyristors.

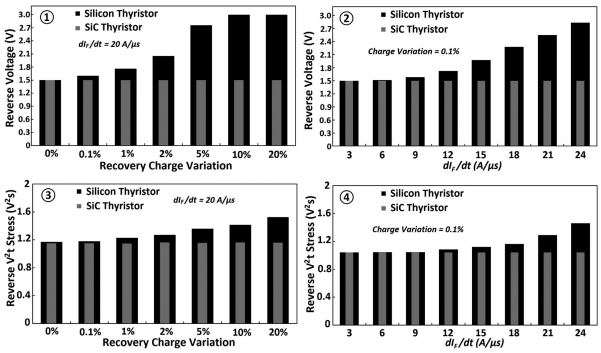

FIGURE 13. The worst-case thyristor reverse voltage and V^2t stress indicated by 1 & 3: recovery charge variations and 2 & 4: dI_F/dt.

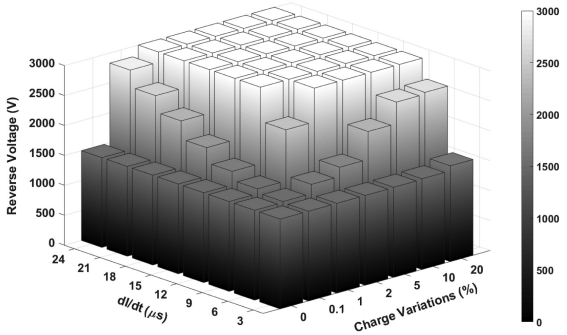

FIGURE 14. 3D plot of the worst-case reverse voltage depending on recovery charge variations and fault dI_F/dt of silicon device. N.B., the SiC thyristor reverse voltage is constant at 1.5 kV.

Fig. 10 in terms of the V^2t stress of reverse voltage on each device. It is illustrated that by increasing the variation, the stress on the silicon devices also increase, while it remains constant for the SiC device.

Fig. 11 shows the worst-case reverse voltage on the silicon and SiC thyristors with least recovery charge depending on its stored charge. Fig. 11.1 shows that as the recovery charge variation increases, the peak reverse voltage on the thyristors also increase until it is clamped to the DC capacitor's voltage. It is also seen that with further variation of recovery charge the thyristor has to endure the reverse voltage for a longer period, whilst at highest junction temperature. In comparison, SiC thyristors block the same share of DC line voltage, irrespective of capacitor voltage and charge variations, as shown in Fig. 11.2.

Fig. 12.1 shows similar trends of worst-case reverse voltage for a range of different dI_F/dt. It is shown that similar to the variations in the recovery charge, dI_F/dt also result in different recovery voltages on the thyristors. A similar trend is not seen in the SiC thyristor, due to the fact that the recovery charge indicated by the manufacturer is obtained at the peak turn-off *dI/dt* capability of the device. Therefore, any lower *dI/dt* will only result in less recovery charge which further reduces variations in reverse voltage.

A comparison of the impact of peak reverse voltage and dI_F/dt for both Silicon and SiC thyristors was undertaken, under identical conditions. As shown in Fig. 13.1, the peak reverse voltage on the silicon device varies from 1.5 kV to 3 kV over the 0–20% charge variation, while this value remains stable for the SiC thyristor. Fig. 13.2 also shows the significant impact of dI_F/dt on the imposed reverse voltage on the silicon thyristor whilst remaining mostly negligible on the SiC thyristor. Fig. 13.3 and Fig. 13.4 show the electro-thermal stress as a function of V^2t. It is demonstrated that with an increase in the charge variation and dI_F/dt, the electro-thermal stress rises for the silicon device as both the peak reverse voltage and its duration increase. In comparison there is virtually no impact on the SiC device, that suggests a smaller failure-in-time (FIT) rate.

Fig. 14 shows the 3D plot of modeling results for the silicon device. An increase of both dI_F/dt and charge difference rapidly results in additional reverse blocking requirement on the fast-recovered silicon thyristors. In comparison, the reverse voltage for SiC device consistently remains at its share of DC line-to-line voltage, irrespective of capacitor voltage, charge variation or dI_F/dt.

VI. CONCLUSION

SiC thyristors can alleviate the electro-thermal stress on the silicon thyristors following bypass of a DC fault current. The ability of SiC thyristors to tackle this stress is predicated upon the low stored recovery charge in the drift region of the device

which enables a fast reverse recovery transient. Consequently, the reverse voltage on all thyristors is kept at its minimum, especially when the thyristors suffer from a high junction temperature due to bypassing a significant proportion of surge current. To date majority of SiC thyristors are designed with asymmetrical blocking capability in favour of forward voltage blocking to minimize the on-state voltage drop. In contrast, the reverse blocking capability is the key parameter when used in protection of HB-MMC-VSC-HVDC. Therefore, device structures which are designed in favour of reverse blocking capability are sought. The surge current of the SiC thyristors also need to increase, which would depend on production of defect-free substrates. These are expected to be available in foreseeable future. Therefore, it can be argued that production of high current SiC thyristors with considerable reverse blocking capability will eliminate the main failure risk associated with the use of silicon thyristors and can displace the silicon thyristors and other complex fault management techniques in protection of HB-MMC-VSC-HVDC converters at DC faults.

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