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Analysis of the 1st and 3rd Quadrant Transients of Symmetrical and Asymmetrical Double-Trench SiC Power MOSFETs

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ABSTRACT In this paper, performance at 1st and 3rd quadrant operation of Silicon and Silicon Carbide (SiC) symmetrical and asymmetrical double-trench, superjunction and planar power MOSFETs is analysed through a wide range of experimental measurements using compact modeling. The devices are evaluated on a high voltage clamped inductive switching test rig and switched at a range of switching rates at elevated junction temperatures. It is shown, experimentally, that in the 1st quadrant, CoolSiC (SiC asymmetrical double-trench) MOSFET and SiC symmetrical double-trench MOSFET demonstrate more stable temperature coefficients. Silicon Superjunction MOSFETs exhibits the lowest turn-off switching rates due to the large input capacitance. The evaluated SiC Planar MOSFET also performs sub-optimally at turn-on switching due to its higher input capacitance and shows more temperature sensitivity due to its lower threshold voltage. In the 3rd quadrant, the relatively larger reverse recovery charge of Silicon Superjunction MOSFET negatively impacts the turn-OFF transients compared with the SiC MOSFETs. It is also seen that among the SiC MOSFETs, the two double-trench MOSFET structures outperform the selected SiC planar MOSFET in terms of reverse recovery.

INDEX TERMS Silicon carbide, trench, double-trench, MOSFET, temperature.

NOMENCLATURE

V_{GS}	MOSFET Gate-Source Voltage (V)
V_{TH}	MOSFET Threshold Voltage (V)
V_{DS}	MOSFET Drain-Source Voltage (V)
V_{FB}	Flat-band Voltage (V)
V_{GP_ON}	Miller Plateau at Turn-ON (V)
V_{GP_OFF}	Miller Plateau at Turn-OFF (V)
V_{DC}	DC Power Supply Voltage (V)
V_{GG_+}	Positive Gate Supply Bias (V)
V_{GG_-}	Negative Gate Supply Bias (V)
I_L	Load Current (A)
I_F	Diode Forward Current (A)
I_{DS}	MOSFET Drain-Source Current (A)
I_{CH_ON}	Channel Current at Turn-ON (A)
I_{CH_OFF}	Channel Current at Turn-OFF (A)
I_{G_OFF}	Gate Current at Turn-OFF (A)
I_{G_ON}	Gate Current at Turn-ON (A)
C_{iss}	MOSFET Input Capacitance (F)
C_{oss}	MOSFET Output Capacitance (F)
C_{GD}	MOSFET Gate-drain Capacitance (F)
C_{FWD}	Freewheeling Diode capacitance (F)
C_{OX}	Oxide Specific Capacitance (F/m^2)
R_G	Total Gate Resistance (Ω)
N_A	Acceptor Doping Concentration (cm^{-3})
L_{CH}	MOSFET Channel Length (m)
Z_{CH}	MOSFET Channel Width (m)
Q_{rr}	Reverse Recovery Charge (C)
k	Boltzmann Constant (J/K)
β	MOSFET Gain Factor (A/V^2)
D_{it}	Interface Trap Density ($cm^{-2}eV^{-1}$)

E_i	Midgap Energy Level (eV)
n_i	Intrinsic Carrier Concentration (cm^{-3})
ϵ_s	Permittivity of Semiconductor (F/m)
g_m	MOSFET transconductance (A/V)
μ_n	Electron Mobility (m^2/Vs)
τ	High-level Minority Carrier Lifetime (s)
t_Q	Pulse Width Period (s)
t	Time (s)
T	Temperature ($^\circ C$)

I. INTRODUCTION

Wide-bandgap devices are now considered established devices in power electronics. The wide-bandgap property of SiC enables high breakdown voltage, while its good thermal conductivity allows the devices to operate at higher temperatures. It also benefits from high carrier saturation velocity, making the devices capable of high frequency operation with literature reporting high conversion efficiency [1], [2]. With the increasing requirement on operating temperature, studies have been done on the dynamic performance of 2nd generation 1.2 kV SiC planar power MOSFETs compared with Silicon IGBTs which has demonstrated its superiority [3], [4]. Power MOSFETs have an intrinsic P-i-N diode, as a bipolar device, which may conduct in hard switching converters. The MOSFET body diode conducts current before turn-off [5], and the stored charge in its drift region leads to current overshoot in the switching transistor during its reverse recovery. This recovery current is temperature-variant due to the temperature-dependency of minority carriers lifetime. The built-in voltage in SiC is high due to its wide-bandgap which leads to increased conduction losses. Therefore, a SiC Schottky barrier diode (SBD) is commonly connected in anti-parallel to the MOSFET to avoid excessive losses. Addition of an external SBD increases the cost while its junction capacitance enhances the switching losses. As an step improvement, the SiC MOSFETs body diodes are shown to have similar reverse recovery performance to SiC Schottky diode in synchronous rectification [6] with higher surge current capability [7]. The SiC MOSFET body diode reverse recovery is shown to be worse than SiC SBD but superior to Silicon power MOSFET body diode [8].

The aforementioned studies have mainly covered planar SiC MOSFET structures. The planar structure has a JFET region, yielding an optimum JFET dimension beyond which the on state resistance increases. This limits the scaling down of unit cells, and the gate oxide is exposed to high electric field strength which leads to reliability concerns [9]. The double-trench power MOSFETs take advantage of deep P pillars within source/body cells to protect the trench gate, and reshape the E-field distribution so the stress on the gate oxide layer is alleviated [10]. The more compact structure achieves low on-state resistance with increasing cell density, but increases the junction capacitances. The deep P pillars may reintroduce the JFET effect and limit the current spreading into the drain drift region, hindering unit cell scaling down. The asymmetric double-trench structure implemented in CoolSiC MOSFET by Infineon overcomes this JFET limitation, and allows theoretical unlimited scaling down of the cells without affecting the avalanche ruggedness [10]. The higher density of cells further reduces the on-state resistance, and the P pillars induce low gate-drain capacitance enabling high frequency operation with low switching loss while effectively suppressing the parasitic BJT as well.

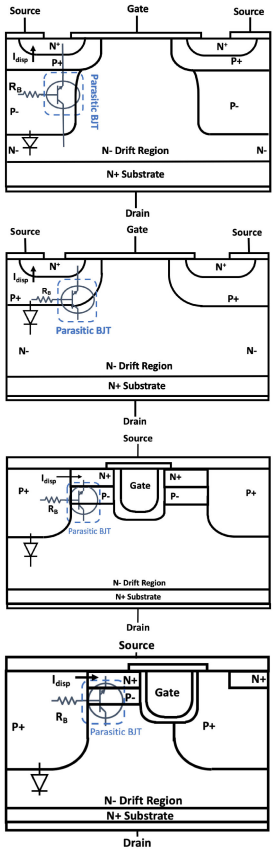

FIGURE 1. Cross-section schematics of the four MOSFET structures: Silicon Superjunction MOSFET, SiC Planar MOSFET, SiC Symmetrical Double-Trench MOSFET & CoolSiC Asymmetrical Trench MOSFET.

Fig. 1 shows the cross-section of the four devices under test in this paper, with structures listed as symmetrical Silicon superjunction MOSFET, symmetrical SiC Planar MOSFET, symmetrical SiC Double-Trench MOSFET & asymmetrical CoolSiC MOSFET. The P pillars enable a higher voltage ratings with thinner drift regions, enabling lower on-state resistance, but with significant reverse recovery charge in the conduction of Silicon superjunction device.

In this paper, the 1st and 3rd quadrant performance of symmetrical and asymmetrical trench and double-trench SiC MOSFETs are measured at 8 A and 800 V followed by accurate modelings with a range of switching rates at temperatures ranging from 25 °C to 175 °C. Section II discusses the theoretical models of the transients, Section III provides the experimental set-up and properties, Section IV provides the results of experimental measurements of 1st quadrant transients of

the four devices (DUTs) along with the demonstration of the modeling outputs, Section V discusses the 3rd quadrant performances while Section VI concludes the paper.

II. MODELING OF 1ST QUADRANT TRANSIENTS

To be able to understand the difference between switching behaviour of the four types of MOSFETs, first the transient models of power MOSFETs must be evaluated, and its accuracy in predicting the switching rates must be validated. The models will be subsequently used for estimation of the switching rates, and their validity for all four device structures in Silicon and SiC will be verified and the error quantified.

A. TURN-ON

At turn-ON transient of power MOSFETs, the current rise happens when voltage increases from threshold value to Miller plateau and then the current is transferred from free-wheeling diode to MOSFET. This voltage rise is defined by:

$$V_{GS} = V_{GG_+} \cdot (1 - e^{\frac{-t}{C_{iss} \cdot R_G}}) \tag{1}$$

and its transient rate is:

$$\left.\frac{dV_{GS}}{dt}\right|_{ON} = \frac{V_{GG_+}}{C_{iss} \cdot R_G} \cdot e^{\frac{-t}{C_{iss} \cdot R_G}} \tag{2}$$

The MOSFET current is flowing in the channel and can be defined by:

$$I_{DS} = I_{CH} = g_m \cdot (V_{GS} - V_{TH}) \tag{3}$$

where MOSFET transconductance is defined by

$$g_m = \frac{Z_{CH} \cdot C_{OX} \cdot \mu_n \cdot (V_{GS} - V_{TH})}{2 \cdot L_{CH}} = \frac{\beta}{2} \cdot (V_{GS} - V_{TH}) \tag{4}$$

where gain factor is defined as:

$$\beta = \frac{Z_{CH} \mu_n C_{OX}}{L_{CH}} \tag{5}$$

Therefore, the current turn-ON rate is [4]:

$$\left.\frac{dI_{DS}}{dt}\right|_{ON} = \beta \left(V_{GG_+}(1 - e^{\frac{-t}{C_{iss}R_G}}) - V_{TH} \right) \frac{V_{GG_+}}{C_{iss}R_G} e^{\frac{-t}{C_{iss}R_G}} \tag{6}$$

while the threshold voltage is given by [11]:

$$V_{TH} = V_{FB} + 2\phi_B + \frac{\sqrt{4\epsilon_{si} K T N_A \ln\left(\frac{N_A}{n_i}\right)}}{C_{OX}} + \frac{q \int_{E_i}^{E_i + \phi_B} D_{it}(E) dE}{C_{OX}} \tag{7}$$

where ϕ_B is given by

$$\phi_B = \frac{KT}{q} \ln\left(\frac{N_A}{n_i}\right) \tag{8}$$

The Miller plateau voltage can also be defined by:

$$V_{GP}|_{ON} = V_{TH} + \frac{I_L}{g_m} \tag{9}$$

where I_L equals to the channel current I_{CH_ON}. The MOSFET gain factor can then be given as [12]:

$$\beta = \frac{2 \cdot I_{CH}}{(V_{GP\_ON} - V_{TH})^2} \tag{10}$$

where channel current in this case is equal to the full load current in addition to any possible current overshoot caused by drain-source capacitance and freewheeling SBD capacitance. The MOSFET drain-source voltage transition happens when the gate voltage is maintained at plateau. The voltage transition speed can be represented by:

$$\left.\frac{dV_{DS}}{dt}\right|_{ON} = \frac{I_{G\_ON}}{C_{GD} = \frac{V_{GG_+} - V_{GP\_ON}}{C_{GD} \cdot R_G}} \tag{11}$$

which is essentially the charging rate of gate-drain capacitance by gate current as follows:

$$I_{G\_ON} = \frac{V_{GG_+} - V_{GP\_ON}}{R_G} \tag{12}$$

B. TURN-OFF

At turn-OFF transient, voltage transition happens when V_{GS} falls to Miller plateau. Considering the current transfer from MOSFET channel to FWD capacitance and MOSFET output capacitance when there is voltage variation, channel current can be derived as:

$$I_{CH}|_{OFF} = I_L - \left.\frac{dV_{DS}}{dt}\right|_{OFF} \cdot (C_{oss} + C_{FWD}) \tag{13}$$

Therefore, the Miller plateau at turn-OFF is given by:

$$V_{GP}|_{OFF} = V_{TH} + \frac{I_L - \left.\frac{dV_{DS}}{dt}\right|_{OFF} (C_{oss} + C_{FWD})}{g_m} \tag{14}$$

The turn-OFF process for the voltage transient is an reversion of voltage turn-ON process with gate current now flowing out from gate terminal at Miller plateau. This can also be described by:

$$\left.\frac{dV_{DS}}{dt}\right|_{OFF} = -\frac{I_{G\_OFF}}{C_{GD}} = -\frac{V_{GP\_OFF} - V_{GG\_}}{C_{GD} \cdot R_G} \tag{15}$$

which is essentially the discharging rate of gate-drain capacitance by gate current as follows:

$$I_G|_{OFF} = \frac{V_{GP\_OFF} - V_{GG\_}}{R_G} \tag{16}$$

The current turn-OFF transient is comprised of two phases. The first phase is the time taken to charge the free-wheeling SiC SBD diode capacitance which is also the time taken for the voltage to rise across the diode. Assuming that the dV/dt across the diode is linear, the time taken is given by:

$$\Delta t = \frac{V_{DC}}{\left.\frac{dV_{DS}}{dt}\right|_{OFF}} \tag{17}$$

As per [13], this charging current of diode is:

$$\Delta I = \left.\frac{dV_{DS}}{dt}\right|_{OFF} \cdot C_{FWD} \tag{18}$$

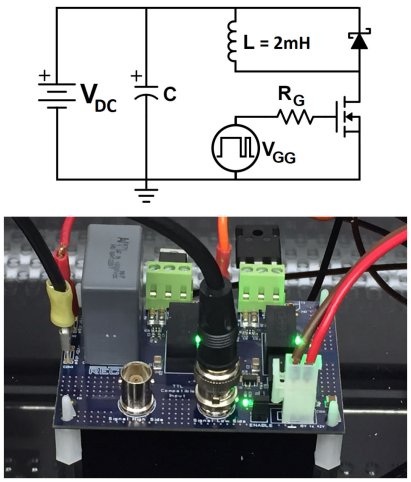

FIGURE 2. The clamped inductive switching test board.

therefore, the switching current rate can be written as:

$$\frac{dI}{dt} = \frac{\Delta I}{\Delta t} = \frac{\left(\frac{dV_{DS}}{dt}\Big|_{OFF}\right)^2 \cdot C_{FWD}}{V_{DC}} \tag{19}$$

Once voltage transition completes, it enters the second phase, the rest of MOSFET current follows the decay of V_{GS} from V_{GP_OFF}, given by:

$$I_{DS}|_{OFF} = g_m(V_{GS}|_{OFF} - V_{TH}) \tag{20}$$

in which

$$V_{GS}|_{OFF} = V_{GP\_OFF} \cdot e^{\frac{-t}{C_{iss}R_G}} \tag{21}$$

while the rate of change of current can be described as:

$$\begin{aligned}\frac{dI_{DS}}{dt}\Big|_{OFF} &= \frac{Z_{CH}\mu_n C_{OX}(V_{GS} - V_{TH})}{L_{CH}} \cdot \frac{dV_{GS}}{dt} \\ &= -\frac{Z_{CH}\mu_n C_{OX}(V_{GS} - V_{TH})}{L_{CH}} \\ &\quad \times \frac{V_{GP\_OFF}}{C_{iss}R_G} \cdot e^{\frac{-t}{C_{iss}R_G}}\end{aligned} \tag{22}$$

The models described above will be validated by device parameters for the four device structures in Silicon and SiC, and its result will be compared with the results of experimental measurements that will follow in the next section.

III. EXPERIMENTAL SET-UP FOR THE DUTS

Experiments are performed on Infineon's Silicon Superjunction MOSFET, Rohm's SiC Planar MOSFET, Rohm's SiC Symmetrical Double-trench MOSFET and Infineon's Asymmetrical Double-Trench CoolSiC MOSFET. The measurements are done on a clamped inductive switching test board shown in Fig. 2 with the freewheeling diode being Wolfspeed's SiC Schottky Barrier Diode (C4D08120 A) which is later replaced by MOSFETs body diode to test the 3rd quadrant transients. The MOSFET is driven by a gate driver that provides +15 V/−5 V output. The current is measured with CWT Ultra-mini Rogowski coil (CWT1) and voltage is measured with GW-Instek GDP-100 100 MHz voltage probe on a Keysight MSO7104 A 1-GHz 4GSa/s oscilloscope. The DUT measurement span is 90% to 10% of transients at 800 V & 8 A for temperature ranging from 25 °C to 175 °C.

TABLE 1 Measurement Board Components

Parameter	Symbol	Value
DC Capacitor	C_{DC}	1 μF
De-Coupling Capacitor	C_{HF}	100 nF
Load Inductor	L	2 mH
Voltage	V	800 V
Current	I	8 A
Charging Pulse Length	t_{Q1}	20 μs
Switching Pulse Length	t_{Q2}	5 μs
Gap between Pulses	t_{Qnil}	5 μs
Temperature Range	T	25-175°C
Gate Resistance Range	R_G	10-100 Ω

TABLE 2 Gate Driver ZXGD3006E6TA Parameters

Parameter	Symbol	Value
Driver Input Supply Voltage	V_{CC}	18 V
Input Peak Driver Current	I_{IN}	100 mA
Output Peak Gate Current	$I_{G,switch}$	10 A
Propagation Delay	t_{PD}	40 ns
Output Gate Voltage Rise Time	t_{rise}	8 ns
Output Gate Voltage Fall Time	t_{fall}	16 ns
Power Dissipation	P_D	1.1 W

Table 1 indicates the values of the key parameters for the measurement board and the conditions of the measurements. The length of the charging pulse for the 1st quadrant measurements have been fixed to deliver 8 A at 800 V while it has been dynamically changing for the 3rd quadrant measurements. Table 2 details the key parameters for the driving chip that impact the drive while Table 3 has listed the key parameters of the four devices under test (DUTs) to be used in calculations of Section IV to compare the model outputs with experimental measurements to verify the models' validity for the emerging device structures.

IV. MEASUREMENTS OF 1ST QUADRANT OPERATION

A. TURN-ON

There are two key factors that impact temperature dependency of MOSFET current turn-ON [14]: threshold voltage and carrier mobility. The threshold voltage of all four devices is measured at a wide range of temperatures, from 25 °C to 175 °C in steps of 25 °C, under the conditions of $V_{GS} = V_{DS}$ & $I_D = 4$ mA, with values measured at room temperature listed in Table 3. Intrinsic carrier density and interface traps are both responsible for decrease of the threshold voltage

TABLE 3 Key Device Parameters of the Four DUTs

	4H-SiC	4H-SiC	4H-SiC	Si
Model	SCT2160	SCT3160	IMW120R140M1H	IPW90R340C3
Make	Rohm	Rohm	Infineon	Infineon
Structure	Planar	Sym-DT	Asym-DT	SJ
Volt. (V)	1200	1200	1200	900
Amp. (A)	22	17	19	15
$R_{DS\text{-}ON}$ (Ω)	160	160	140	340
Q_G (C)	62	42	13	94
V_{GP} (V)	12.65	11.1	10.4	6.44
V_{TH} (V)	3.23	4.13	4.23	3.06
g_m (S)	2.4	2.5	3	6
C_{iss} (pF)	1200	398	454	2400
C_{oss} (pF)	45	41	25	120
C_{rss} (pF)	7	18	3	10
Q_{rr} (nC)	39	26	125	11000
$R_{G\text{-}int}$ (Ω)	13.7	18	14	1.3
$R_{th(jc)}$ (K/W)	0.7	1.12	1.2	0.6

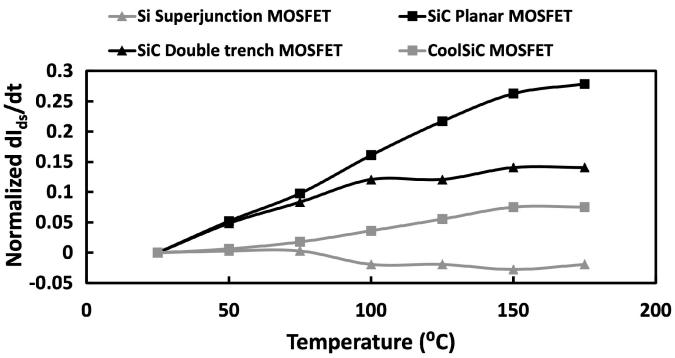

FIGURE 3. Normalized current turn-ON rate to temperature with 10 Ω external gate resistance for the four DUTs.

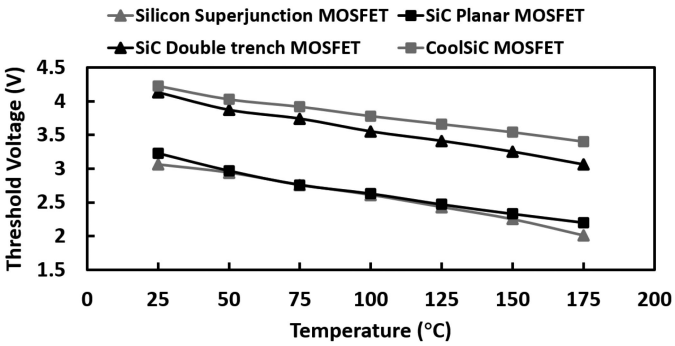

FIGURE 4. Threshold voltage to temperature for the four DUTs (measured at $V_{GS} = V_{DS}$ & $I_D = 4$ mA).

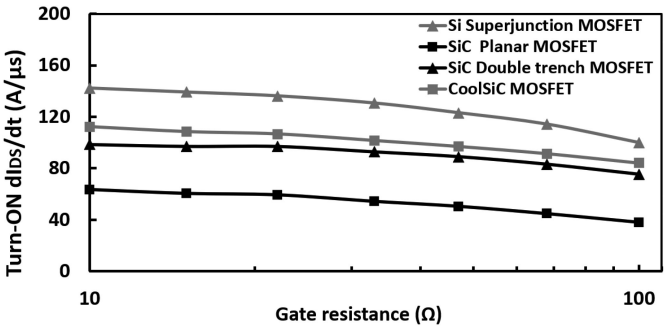

FIGURE 5. Current turn-ON rate with external gate resistance at 25 °C for the four DUTs.

as temperature rises [15] and enable MOSFET to turn-ON faster. To identify which factor is the main contributor, further measurements are required on the interface traps density of DUTs. Silicon has negative temperature coefficient in carrier mobility due to more significant scattering [14], [16], [17]. However, carrier mobility in SiC MOSFET is reported to have a positive temperature coefficient below around 200 °C and then decrease with further increase of the temperature due to the participation of electrons released from oxide interface traps [18]. The impact of temperature dependency of channel mobility on turn-on transients is also influenced by the crystal face in 4H-SiC in the MOS channel. The technology and quality of annealing will also impact the channel mobility [19]. Fig. 3 shows normalized current turn-ON rate with respect to temperature for the four DUTs. Slightly negative trend with temperature is observed on Silicon superjunction MOSFET which means that the two factors almost balance each other, though the effect from negative temperature coefficient of carrier mobility is slightly more pronounced. Three SiC MOSFETs show faster current switching speed as temperature rises with SiC planar MOSFET being the most temperature sensitive. This is due to the noticeable threshold voltage drop on SiC planar MOSFET, as shown in Fig. 4. Although SiC double trench MOSFET, CoolSiC MOSFET and SiC planar MOSFET all have around 1 V drop across the temperature span, the lower threshold value of SiC planar MOSFET makes the impact of temperature on switching rate more significantly at this SiC device.

Fig. 5 plots the current turn-ON rate variation with the gate resistance and shows that the Silicon superjunction MOSFET, SiC double trench MOSFET and CoolSiC MOSFET have close transition rates while the SiC planar MOSFET remains the slowest one.

The threshold voltage of the four DUTs at 25 °C was shown in Table 3. In addition the value of the plateau voltage will be required to be calculated. The method to extract Miller plateau is demonstrated in Fig. 6 where the Miller plateau period (t_{GP}) is defined by drain-source voltage transition while gate-source voltage is averaged over the same period. Given the same full load current in the testing circuit and ignore the impact of additional current generated by drain-source capacitance and freewheeling SBD capacitance, the difference between V_{GP_ON} and V_{TH} of Silicon superjunction MOSFET is significantly smaller than the three SiC devices, suggesting that

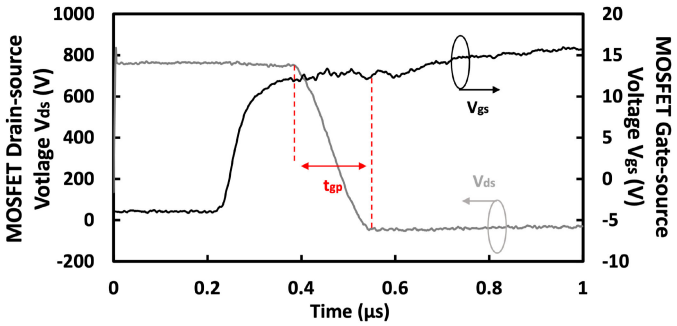

FIGURE 6. Extraction of Miller plateau from drain-source voltage and gate-source voltage waveform.

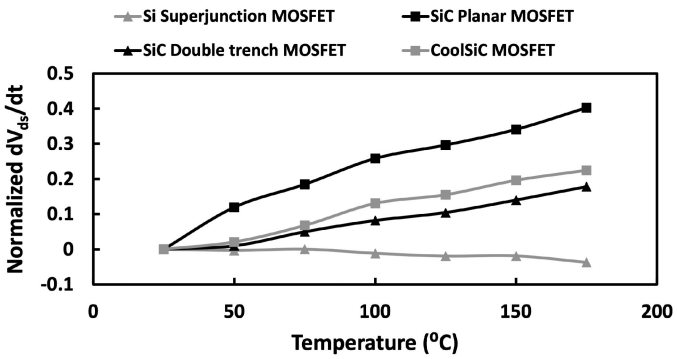

FIGURE 7. Normalized voltage turn-ON rate to temperature with 10 Ω external gate resistance for four DUTs.

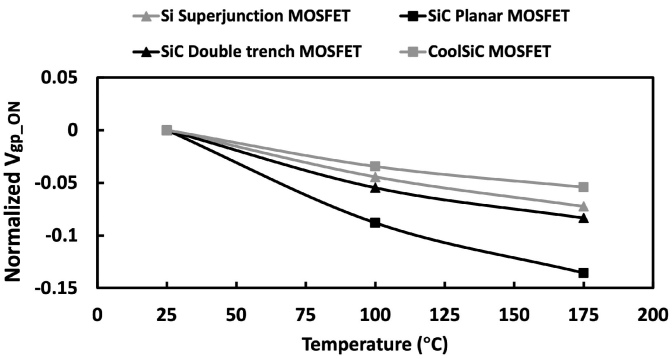

FIGURE 8. Normalized Miller plateau voltage at turn-ON to temperature with 10 Ω external gate resistance for four DUTs.

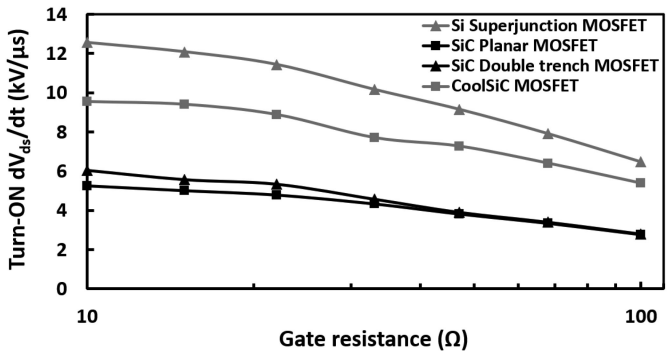

FIGURE 9. Voltage turn-ON rate with gate resistance at 25 °C with external gate resistance for four MOSFETs.

it has a large β while SiC planar has the smallest. Large input capacitance, threshold voltage and gate resistance slow down current switching while large gain factor accelerates current switching. One common disadvantage for Silicon MOSFET is large input capacitance compared with SiC MOSFET arisen from its large die size which is confirmed by its datasheet. The key criteria which makes the Silicon superjunction MOSFET to outstand of the other devices is its large transconductance when compared with threshold voltage and Miller plateau at turn-ON.

Fig. 7 also shows normalized voltage turn-ON rate with 10 Ω external gate resistance to temperature for the four DUTs. Negative temperature coefficient of threshold voltage [15] and positive coefficient of electron mobility [17] in SiC MOSFETs would accelerate voltage transition by decreasing Miller plateau (V_{GP_ON}) [20]. Negative temperature coefficient of electron mobility in Silicon MOSFET [18], on the other hand, hinders voltage transition by increasing the Miller plateau [20], despite the reduced threshold voltage. The normalized value of Miller plateau voltage at turn-ON is calculated by averaging the gate-source voltage over drain-source voltage transition and is plotted on Fig. 8 against temperature. In Fig. 8, the large drop of Miller plateau at turn-ON of SiC planar MOSFET leads to a noticeable increase in drain-source voltage turn-ON rate as in Fig. 7. This is while the SiC double-trench MOSFET and the CoolSiC MOSFET exhibit medium temperature sensitivity. It should also be noticed that as Miller plateau at turn-ON is closer to gate driver output voltage (V_{GG_+}), its temperature sensitivity has higher significance to that of the MOSFET's drain-source voltage turn-ON rate. Hence, with turn-ON Miller plateau of 12.65 V as the largest value amongst the four DUTs, a 15% drop of Miller plateau at turn-ON V_{GP_ON} in the SiC planar MOSFET results in a 40% rise of voltage turn-ON rate.

Fig. 9 shows the voltage turn-ON rate at 25 °C for the four DUTs. SiC double-trench MOSFET and SiC planar MOSFET have similar rate while CoolSiC MOSFET and Silicon superjunction MOSFET show close switching rate over the entire range of gate resistances. The high gain factor (β) results in low Miller plateau voltage, thus high gate current feeds into the gate-drain capacitance which ramps up the voltage dropping rate. The structure of the CoolSiC MOSFET have P-doped pillars partially wrapping the gate trench to reduce C_{GD} which achieves comparable drain-source voltage turn-ON rate as Silicon superjunction MOSFET with smaller gate current. The structure in SiC double-trench MOSFET has the drawback of large gate-drain capacitance [21] which slows down the voltage transient. SiC planar MOSFET as opposite to Silicon superjunction MOSFET, mainly takes the drawback of small transconductance, thus high Miller plateau voltage, which slows down the voltage transient by reducing the gate current. During voltage turn-ON, the freewheeling

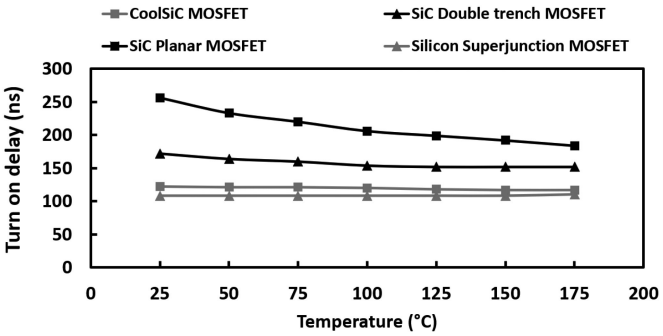

FIGURE 10. Turn-ON delay of DUTs with gate resistance 10 Ω with temperature.

SBD capacitance is releasing charge in response to the voltage transition. The charge flows into DUT and induces current overshoot [13]. Therefore, the current overshoot in CoolSiC MOSFET and Silicon superjunction MOSFET is more severe than the other two DUTs, which can be a potential reliability risk.

Fig. 10 shows the turn-ON delay variation with temperature with an external gate resistance of 10 Ω. The turn-ON delay on SiC planar MOSFET shows the least stable trend and has a clear decrease as a consequence of both highly temperature sensitive current turn-ON rate and voltage turn-ON rate. Its small transconductance is a major contributor to the longest turn-ON delay by slowing down both current and voltage turn-ON. For the same reason, the large transconductance enables Silicon superjunction MOSFET to excel at turn-ON transient, even exceeding the performance of the SiC double-trench MOSFET and CoolSiC MOSFET.

Fig. 11 shows the turn-ON models for the drain-source current of the four device structures when compared with results of the experimental measurements. It can be seen that the models strongly hold true for the novel structures including symmetrical and asymmetrical double-trench SiC MOSFETs, indicating that the transient models are still well applicable.

B. TURN-OFF

The results of normalized voltage turn-OFF rate with 10 Ω external gate resistance with respect to temperature for the four DUTs is shown in Fig. 12. The Miller plateau at turn-OFF (V_{GP_OFF}) is extracted by averaging the gate-source voltage during drain-source voltage turn-OFF. Its normalized value is plotted in Fig. 13 against temperature. The decreasing Miller plateau, previously enabling fast switching at turn-OFF, now impedes at turn-OFF according to (15). Although different varying degree of Miller plateau at turn-OFF is observed on DUTs, as shown in Fig. 12, the Miller plateau at turn-OFF is lowered due to the channel current transfer to drain-source capacitance and freewheeling SBD as represented in (13). The negative output voltage from bipolar gate drivers ($V_{GG\_}$) is able to damp the temperature dependency of voltage turn-OFF rate to a similar extent.

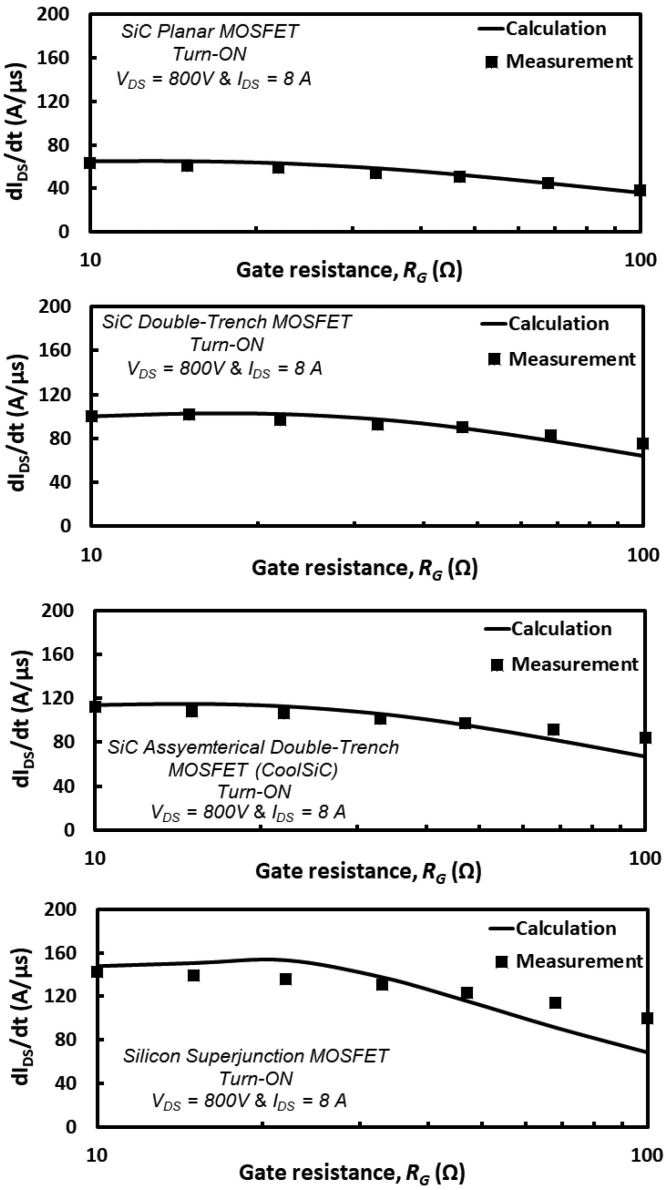

FIGURE 11. Turn-ON models for the drain-source current of the four device structures when compared with results of the experimental measurements show a good accuracy over a wide range of temperatures.

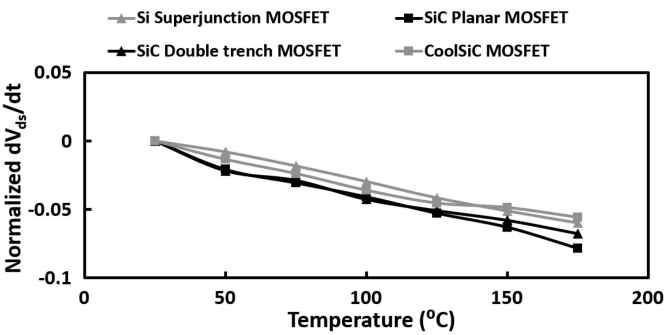

FIGURE 12. Normalized voltage turn-OFF rate to temperature with 10 Ω external gate resistance for four DUTs.

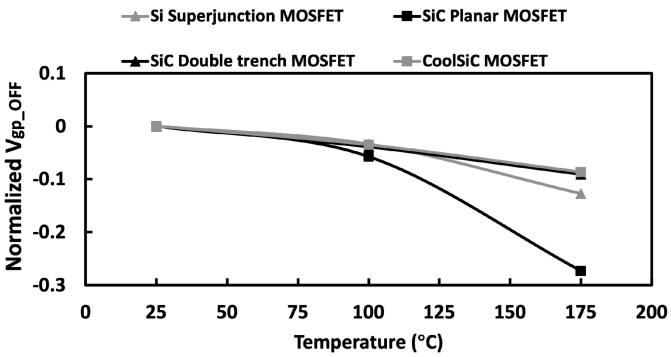

FIGURE 13. Normalized Miller plateau voltage at turn-OFF to temperature with 10 Ω external gate resistance for four DUTs.

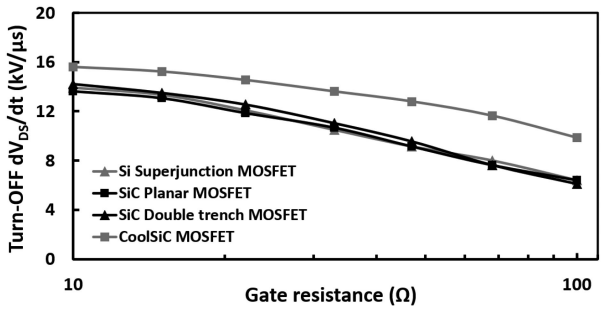

FIGURE 14. Voltage turn-OFF rate of DUTs to external gate resistance at 25 °C.

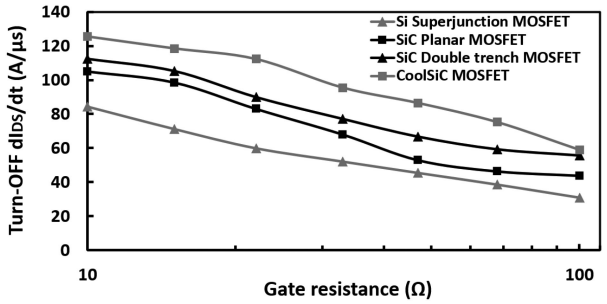

FIGURE 15. Current turn-OFF rate for four MOSFETs to external gate resistance at 25 °C.

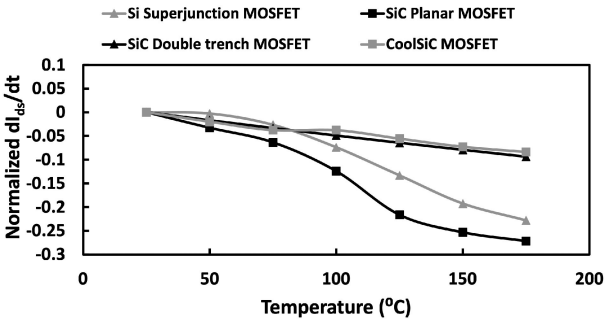

FIGURE 16. Normalized current turn-OFF rate to temperature with 10 Ω external gate resistance.

The voltage turn-OFF rate of the four devices is shown in Fig. 14 at 25 °C. It can be seen that the CoolSiC MOSFET exhibits the fastest voltage transition for its particularly low gate-drain capacitance as a feature of its asymmetric double-trench structure [22]. The other three DUTs have close switching rate and the reason is the similar gate current due to similar Miller plateau at turn-OFF (V_{GP_OFF}). During the voltage turn-OFF transient, freewheeling SBD and MOSFET drain-source capacitance draw current from MOSFET channel in response to voltage transition so that the reduced channel current lowers the Miller plateau. The difference in Miller plateau induced by transconductance is minimized. Therefore, the voltage turn-OFF rate is approaching to close to each other except for the CoolSiC MOSFET with particularly low C_{GD}.

The results of the current turn-off rate for the four DUTs against the gate resistance at room temperature is provided in Fig. 15 while the normalized current turn-OFF rate with external gate resistance of 10 Ω is plotted in Fig. 16 against temperature. In-line with expectations of (19), the current turn-OFF rate for this period follows the temperature dependency of drain-source voltage V_{DS} turn-OFF rate which is decreasing with temperature rise. The subsequent current drop once the voltage transition is completed is decay a with the gate voltage and it is determined by the Miller plateau at turn-OFF and input capacitance. The largest drop of current's turn-OFF rate is around 30% in SiC planar MOSFET which comes from its large drop of Miller plateau at turn-OFF over the experiment temperature range, as shown in Fig. 13. Silicon superjunction MOSFET has only 10% drop on Miller plateau at turn-OFF while there is 20% drop on current turn-OFF rate which is due to the significant impact of temperature on its input capacitance that further slows down the transient.

According to (18) and Fig. 14, there is minor distinction for current turn-OFF while voltage turns-OFF. The reason for the slowest current transition in Silicon superjunction MOSFET is its large input capacitance, since the distinction of Miller plateau at turn-OFF is minimized according to (14), thus similar gate current discharging input capacitance. With SiC double-trench MOSFET and CoolSiC MOSFET representing the fastest current turn-OFF rates, it could be demonstrated that these two double-trench structures (albeit one symmetrical and one asymmetrical) achieve an effective reduction on MOSFET input capacitance. Since one disadvantage for double-trench structures is that high unit cell density causes a linear increase in MOSFET input capacitance [10], the fast current turn-OFF rate observed reaffirms that double-trench structure allows a smaller die size than planar structure at the same rating which compensates the drawback by its high unit cell density.

Fig. 17 shows the turn-OFF delay variation with temperature with an external gate resistance of 10 Ω. The delay of Silicon Superjunction MOSFET is significantly larger than other SiC DUTs which is explained by the long time taken at begin the turn-OFF by decay of the gate voltage from

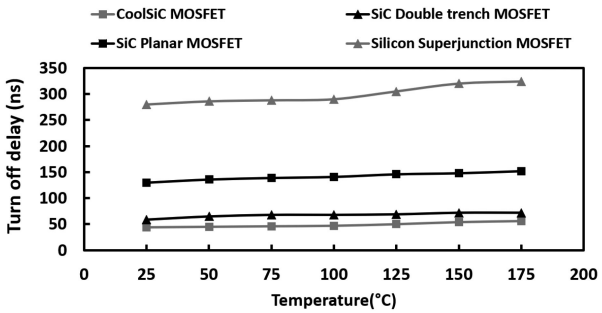

FIGURE 17. Turn-OFF delay for four MOSFETs with external gate resistance 10 Ω to temperature.

positive gate driver output voltage (V_{GG_+}) to Miller plateau at turn-OFF (V_{GP_OFF}), rendered by its large input capacitance C_{iss}. CoolSiC MOSFET and SiC double-trench MOSFET show the shortest turn-OFF delay which illustrates better high frequency operation capability compared with the planar MOSFETs.

Similar to the turn-ON case, Fig. 18 shows the turn-OFF models for the drain-source current of the four device structures when compared with results of the experimental measurements. It can again be seen that the models hold true with good accuracy and follows the same trend in both case of the established devices and the novel structures including symmetrical and asymmetrical double-trench SiC MOSFETs. This reaffirms that the transient models are well applicable to all device structures, including the emerging SiC ones.

V. MEASUREMENTS OF 3RD QUADRANT OPERATION

Measurement have also been done to understand the 3rd quadrant performance of the four device structures through the intrinsic body PiN diode. For a typical PiN diode, the reverse recovery charge increases with temperature because of the increase of the carrier lifetime in the body diode drift region. This charge can be approximated by:

$$Q_{rr} = I_F \cdot \tau \tag{23}$$

Measurements have indicated that Silicon superjunction MOSFET has a very large stored charge during conduction. In addition to the higher minority carrier lifetime in Silicon, the charge storage mechanism in the superjunction structure significantly contributes to this. The structure is effectively a $P^+N^-N^+$ diode in parallel with a $P^+P^-N^+$ diode at 3rd quadrant operation, so both the electrons and holes act as stored charge while the body diode is conducting. SiC MOSFET body diodes show very small reverse recovery current as a result of the short carrier lifetime in SiC. In fact, at room temperature, the three SiC MOSFETs have negligible reverse recovery current. SiC, as wide-bandgap semiconductor, has significantly lower intrinsic carrier density than Silicon, so it is harder to forward bias the SiC body diode at 3rd quadrant operation. Additionally, stronger body effect appears in SiC MOSFET as a result of the higher forward voltage drop on its intrinsic diode [23]. A unipolar current flow in the channel region with electrons, so no conductivity modulation occurs and there will be little stored charge to initiate the reverse recovery. With temperature increase, intrinsic carrier density rises by thermal generation, and the knee voltage of the body diode drops. In addition, the channel resistance rises due to the increased scattering, thus applying a higher voltage over the body diode junction. Therefore, the likelihood of forward biasing of the body diode at higher temperatures increases.

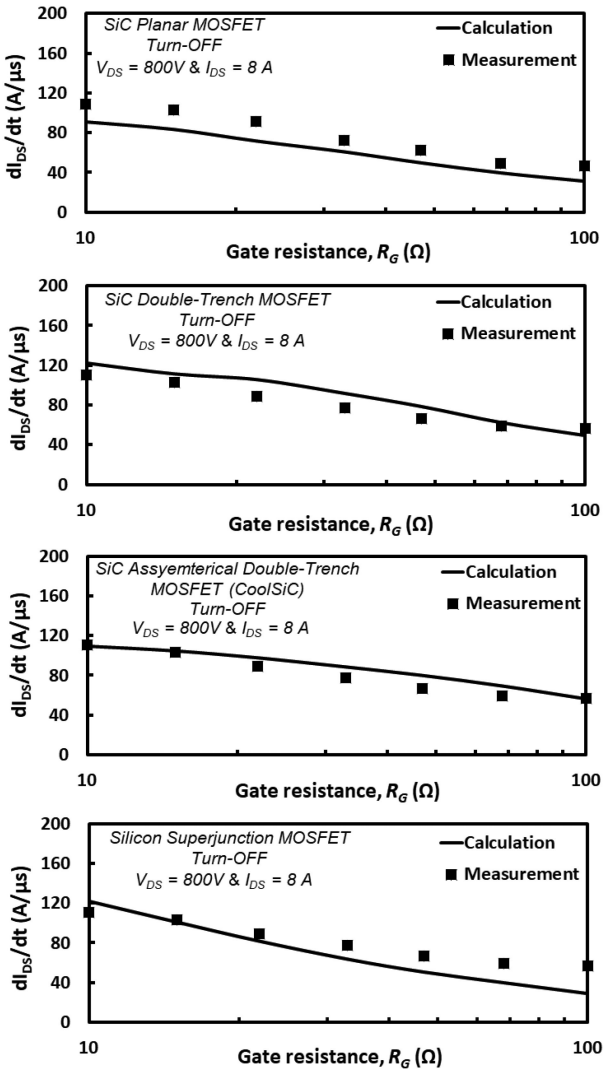

FIGURE 18. Turn-OFF models for the drain-source current of the four device structures when compared with results of the experimental measurements also show a good accuracy over a wide range of temperatures.

The temperature has negligible impact on the switching rates at 3rd quadrant operation of SiC devices. However, in case of the Silicon superjunction MOSFET, the high temperature significantly reduces the voltage turn-OFF rate as in Fig. 19. This is due to the fact that the voltage transition on body diode happens while the reverse recovery current is approaching zero. This means the drain current through the

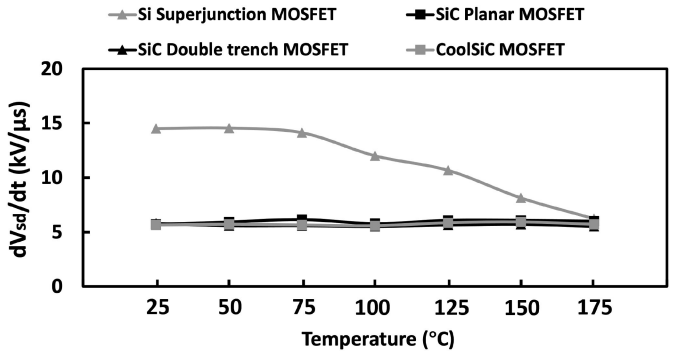

FIGURE 19. Voltage turn-OFF rate to temperature of DUTs at 3rd operation.

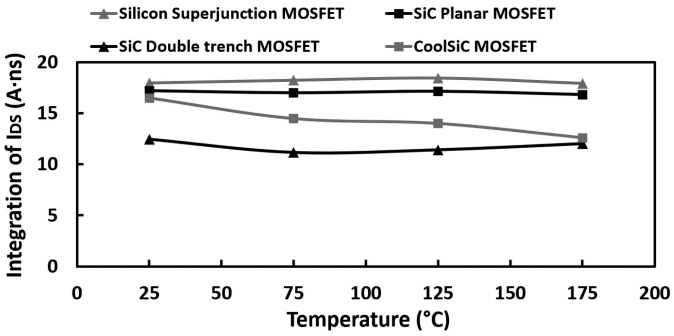

FIGURE 20. Integral of I_{SD} at voltage transition to temperature with 10 Ω gate resistance at turn-ON.

bottom-side MOSFET is declining. As the parasitic source inductance increases the effective gate-source voltage under a decreasing drain current, the bottom MOSFET switches at a higher rate. With temperature increase, the peak reverse recovery increases for Silicon superjunction MOSFET body diode which ramps up the removal of the stored charge. Therefore, the voltage transition occurs while the reverse recovery current is still increasing. This means the drain current on the bottom MOSFET is increasing. The parasitic source inductance reduces the effective gate-source voltage, yielding low switching rate. Once the reverse recovery current reaches the peak value, the voltage transient rate rises.

At turn-ON, The switching energy is mainly determined by the rate of switching of the transistors. At the third quadrant, CoolSiC MOSFET has a small decreasing trend in its switching energy as temperature increases. This is because parasitic capacitances are more sensitive to temperature in CoolSiC asymmetrical double-trench structure. Since the variation is small, the current is integrated over the voltage transition period to amplify the impact of temperature, as shown in Fig. 20. At turn-OFF, the key factor that affects the switching energy is the reverse recovery current. There is a increasing trend in all devices with temperature due to the increased reverse recovery current at high temperature.

The reverse recovery becomes more significant in Silicon superjunction MOSFET with forward current, in terms of

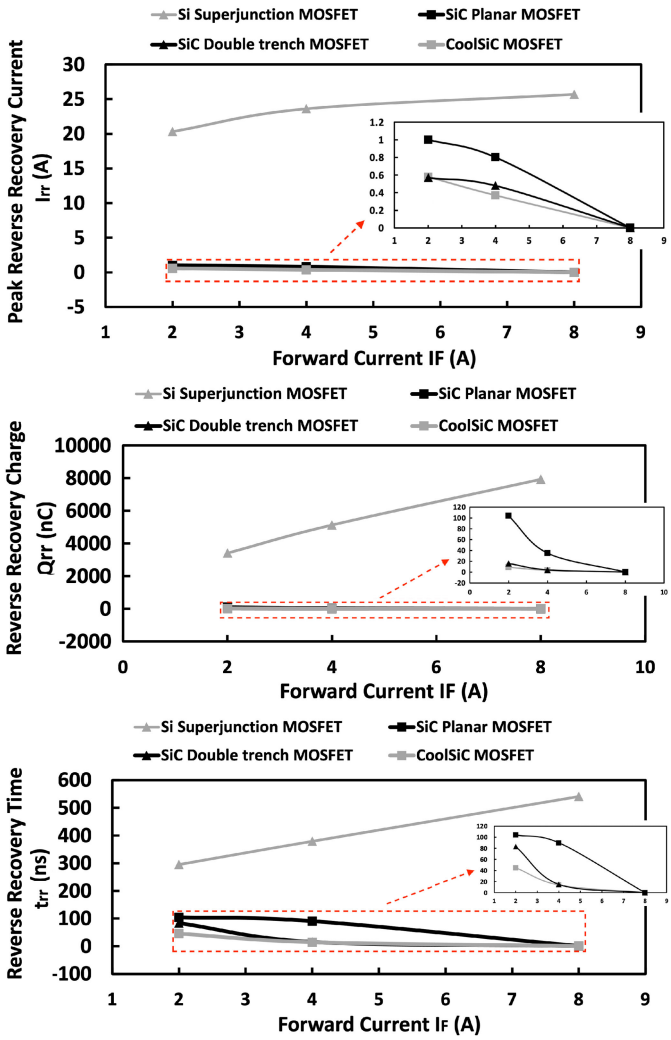

FIGURE 21. The peak reverse recovery current, reverse recovery charge, and recovery time to forward current level at 25 °C with 10 Ω gate resistance.

the peak reverse recovery current, reverse recovery time and reverse recovery charge as shown in Fig. 21. This means more charge is stored in the device during conductivity modulation, so these charge will take longer to recombine when the MOSFET body diode is turned-OFF. As for the other three SiC MOSFETs, this trend is slightly opposite. The reason is the extended switching time. Although higher current accumulates more charge, the longer switching time means more charge would recombine in switching and yields a net decrease in the residual charge when the reverse recovery takes place.

VI. CONCLUSION

The switching performance of Silicon Superjunction MOSFET, SiC Planar MOSFET, SiC Symmetrical Double-Trench MOSFET and CoolSiC Asymmetrical Double-Trench MOSFET are compared experimentally along with their 3rd quadrant operation. Silicon Superjunction MOSFETs exhibit more

than two times higher voltage and current switching rates at turn-ON compared with the slowest SiC planar MOSFET, due to large transconductance in spite of the large input capacitance. Its 3rd quadrant operation has largest switching energy as a result of the reverse recovery charge which increases temperature due to increased minority carrier lifetime thus reduces voltage turn-OFF rate. The selected SiC Planar MOSFET exhibits relatively reduced switching rate at turn-ON as a consequence of its small transconductance which generates relatively high switching energy. In the 3rd quadrant operation, its reverse recovery charge results in more switching energy, which increases with temperature. SiC Double-trench MOSFET and CoolSiC MOSFET maintain relatively optimal switching performance at all temperatures due to the reduced input capacitance resulting from their double-trench structure. When operated at 3rd quadrant, SiC double-trench MOSFET and CoolSiC MOSFET demonstrate reduced switching loss due to the minimal stored charges as well as reduced temperature sensitivity compared with the SiC Planar MOSFET. Models of the switching transients have been validated by extensive experimental measurements for all four device structures and are shown to be as accurate for the emerging device structures as the established ones.

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