New High Step-Up Coupled Dual Winding Quadratic Enhanced SEPIC DC-DC Converter

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***Abstract*—This paper introduces a non-isolated high step-up dc-dc converter originated from single-ended primary-inductor converter (SEPIC). The suggested dual winding quadratic enhanced SEPIC converter (DWQ-ESC) employs a voltage-boosting module to attain superior boost ability. A unique coupled inductor is exploited to regulate the boost factor by tuning the transformer's turns ratio along with the switching duty cycle. Additionally, very high boost factor is achieved at low transformer's turns ratio (limited around 1.0). As a result, low winding turns ratio is required for very high gain applications. Also, a clamping circuit is considered to eliminate the leakage inductance effects of the coupled inductor across the power switch. A single switch with a full control range of duty cycle (0 < D < 1) is utilized in the proposed DWQ-ESC that results in low conducting losses and high efficiency. The introduced DWQ-ESC drains a smooth current from the input dc source that makes it appropriate for renewable energy sources (RES) such as photovoltaic (PV) and wind sources. Theoretical analysis and simulation results are presented in the paper to demonstrate that the introduced topology can obtain high boost factor with a reduced duty ratio in comparison with existing similar quadratic dc-dc converters.**

Keywords—*dc-dc converter, Enhanced SEPIC converter, dual winding converter, non-isolated converter.*

I. INTRODUCTION

Recently, renewable energy sources (RES) including fuel cell, photovoltaic (PV), and wind energy have become more substantial than conventional fossil fuels because of their environmental impacts. However, these alternative energy resources suffer from finite voltage with intermittent characteristic. Power electronics converters play an essential role in the energy conversion of RES when they can provide constant and required voltage levels for high voltage purposes such as ac appliances and dc home utilities. For instance, the voltage at the maximum power of photovoltaic modules is low and intermittent (12-45 V) which does not provide an adequate voltage of 200 to 800 V for dc micro-grids and grid-connected inverters [1-2]. Likewise, another application of high step-up dc-dc converters is in electric vehicles (EV) that require the voltage level of 400 V to 800 V [3]. Accordingly, high gain dc-dc converters have been exploited in RES to supply the demanded voltage. Traditional dc-dc converters like Boost, SEPIC, CUK, and ZETA converters have narrow voltage gain ranges. Aiming to attain high boost ability, a high duty ratio is applied which is not feasible in practice, because it leads to operation malfunction, high switching losses, and efficiency reduction. Therefore, output voltage gain in conventional converters is at most 4-5 in practice [4].

In order to solve the aforementioned problems, several techniques such as switched capacitor, and switched inductor cells, multi-stages, multi cells and magnetic devices (coupled-inductor and transformer) have been exploited to attain a high voltage boost factor with an effective switching duty ratio [5]. However, the aforementioned techniques require additional elements to obtain the desirable output voltage level that raises the cost, size and circuit complexity of the converters. Recently, dc-dc converters based on coupled inductors have been suggested to provide high output voltage with a reduced number of components [6-10]. Generally, in most coupled inductor based dc-dc converters, the voltage boost ability can be raised by adding the turns ratio of the transformer, that can result in higher volume and cost [11].

Recently, impedance source networks based on coupled inductors like Y-source [12], Γ-source [13], and asymmetrical Γ-source [14] were designed to offer high voltage boost ability with a low duty cycle. However, they suffer from the voltage spikes across the power switch and narrow duty cycle control range [15]. In order to solve the voltage spikes problem, some absorbing circuits have been exploited in their impedance networks [16]. However, their narrow duty cycle control range is still considered a major drawback. Modified SEPIC converters based on coupled inductors with the full duty cycle control have been introduced in [17-18] to solve the mentioned drawbacks. These converters can raise the voltage boost factor by decreasing the transformer's turns ratio. However, decreasing the turns ratio must be done regularly to avoid generating distortions which applies limits for very high voltage applications.

This study presents a new high gain dual winding enhanced SEPIC converter which inherits all privileges of the presented topology in [17]. Besides, it attains a high boost factor with a smaller duty cycle in comparison with the proposed converter in [17] and [19]. The introduced converter combines the voltage boosting module and coupled inductor techniques to obtain desired voltage boost capability [20-22] with a small duty cycle for high voltage applications and low voltage distribution networks [23-24]. The circuit description of the proposed DWQ-ESC is given and comprehensive analysis and validation of the converter's performance will be presented in this paper.

This article is organized as follows; circuit analysis, operation basis, leakage inductance effect of coupled inductors, voltage gain analysis, voltage stress across the semiconductors are presented in section II. Section III presents a thorough comparison of proposed converter with existing similar topologies. Simulation results are given in section IV to verify the mathematical and theoretical results. The article is concluded in Section V.

II. Proposed Coupled Dual Winding Quadratic Enhanced SEPIC DC-DC Converter

A. Circuits Description

Fig. 1 illustrates the configuration of the suggested DWQ-ESC. Like the conventional SEPIC converter, the introduced topology has one middle capacitor (C_2), a single switch (S), one input inductor (L_1), one output diode (D_o), and one output capacitor (C_o). A coupled dual winding transformer is replaced instead of the middle inductor in a conventional SEPIC converter where its turn ratio is $n = N_1/N_2$. Also, the input inductor and the power switch are connected by a voltage-boosting module. The boosting module contains two diodes (D_1, D_2), one capacitor (C_1), and one inductor (L_2). To attain high voltage gain, one capacitor (C_3) and one diode (D_3) have been combined in the central section of the circuit. It is found that the input and output sides of the topology have been linked by an impedance source network. From Fig. 1, it is obviously seen that the suggested converter has some similarity with the quadratic topologies in configuration. This topology possesses plenty of absorbing privileges which are summarized as: 1) reduced switching losses; 2) smooth input current; 3) a full range of duty ratio control ($0 < D < 1$); 4) simple control process; 5) very high voltage boost capability; 6) utilizing reduced transformer's turns ratio; 7) using single power switch; 8) non-isolated structure; 9) utilizing clamping circuit for voltage spikes elimination and 10) removing leakage inductance effects of coupled-inductor without using snubber circuit.

B. Operating Principle of the Proposed DWQ-ESC

To abbreviate the converter's operating principle following assumptions are considered: all of the components are ideal; the inductors' and capacitors' resistance are insignificant; ON resistance of the S, the diodes' voltage drop, and parasitic capacitance is negligible. In Continuous Current Mode (CCM) and over one switching period, there are three operation modes as follows:

1) State I - interval [t_0 to t_1]

Fig 2. (a) illustrates the circuit of the DWQ-ESC in state I. In this state, diode D_2 and switch S are conducting. D_1, D_3, and Do are not conducting and reversed biased by capacitors C_1, C_3, and C_o respectively. Inductor L_1 is energized by the input source (V_{dc}) with the current path of V_{dc}-L_1-D_2-S-V_{dc}. The inductor L_2 is charged by capacitor C_1 with the current path of C_1-L_2-S-C_1. Windings N_1 and N_2 are magnetized through the current path as N_2-N_1-C_2-S-C_3-N_2. The resistive load is powered through output capacitor Co that is isolated from the dc source. The characteristic current waveforms of inductors, diodes and power switch are illustrated in Fig. 3. From t_0 to t_1, the current of L_1 and L_M and L_2 are increasing.

2) State II - interval [t_1 to t_2]

Fig. 2 (b) shows the operating mode *II* when diode D_2 is reversed biased by capacitor C_2 and the power switch S is switched OFF. L_1 releases its saved energy into C_1 through V_{dc}-L_1-D_1-C_1-V_{dc}. Capacitor C_2 is energized by L_2 with the current path of C_1-L_2-C_2-D_o-C_o-C_1. The saved energy in the coupled-inductors is released to the capacitor C_3 and load through the path of C_3-N_2-N_1-V_o-C_3. From t_1 to t_2, current of L_1 and L_M and L_2 are decreasing which can be seen in Fig. 3.

3) State III- interval [t_2 to t_3]

To apply steady-state analysis, the transformer is assumed ideal. Nonetheless, the effects of the leakage inductance of the transformer must be considered in practice. As a result because of the leakage inductance effect, D_o is revered biased before the end of the switching period while the power switch is still OFF. This state is illustrated in the Fig. 2 (c) as mode *III*. By applying the proper magnetizing inductance, low leakage inductance and high coupling coefficient, the effect of the turning OFF the diode D_o can be neglected in CCM voltage gain analysis and converter's operation.

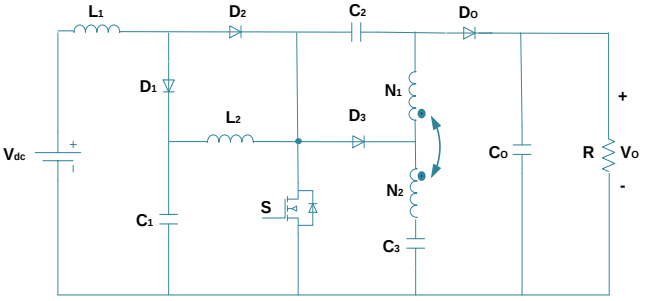

Fig. 1. Proposed coupled dual winding enhanced SEPIC dc-dc converter.

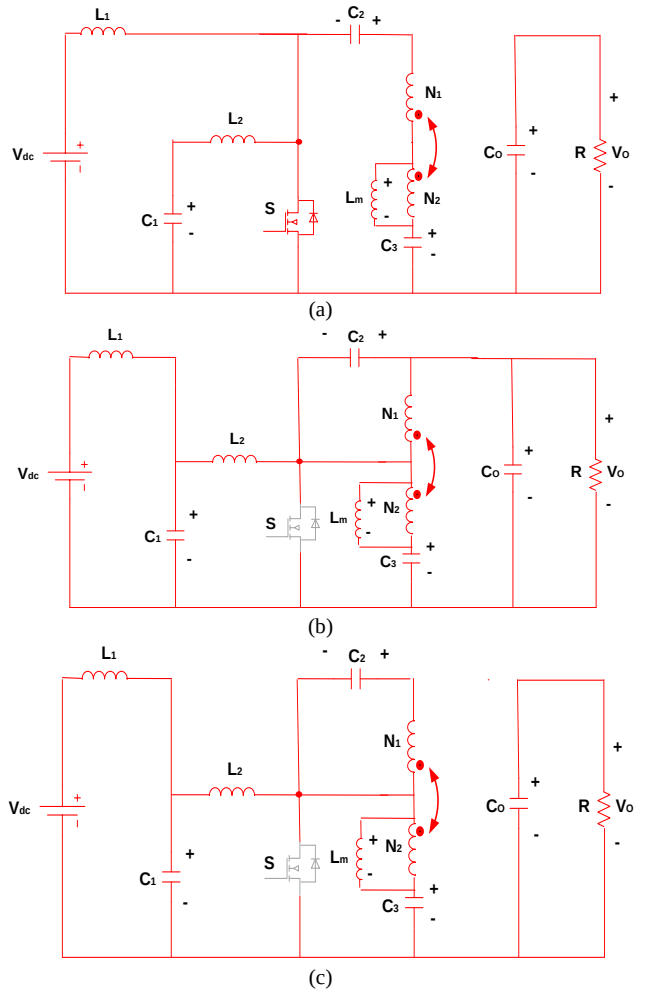

Fig. 2. Circuits of the the suggested DWQ-ESC in, *(a). state I, (b). state II and (c). state III.*

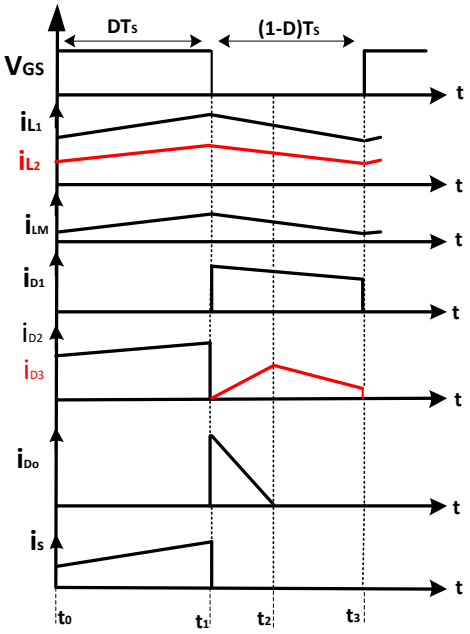

Fig. 3. Proposed Characteristics waveforms of DWQ-ESC in CCM.

C. *Clamping Circuit of the Power Switch*

As it was mentioned in the previous section, the leakage inductance of the coupled inductors cannot be considered zero in practice. Due to the existence of the parasitic capacitor in the power switch and by considering the resonance with the leakage inductance of the coupled inductors, voltage spikes can be produced on the power switch. In state II, when the power switch is switched OFF, it is clamped to $-V_{C2}+V_{Co}$ that is demonstrated by Fig. 2 (b). Accordingly, the leakage inductance of the transformer cannot cause voltage spikes across the power switch. Moreover, capacitors C_2 and C_3 absorb the stored energy in leakage inductance to avoid producing huge voltage spikes on the power switch. Hence, the snubber circuit is not required in the proposed topology which causes cost and size reducing.

D. *Voltage Gain Analysis in Ideal Condition*

In the ideal state, the losses of the source, inductors, diodes and the power switch are ignored. Furthermore, the capacitors' voltage ripples are neglectable. Also, the voltage relation between windings N_1 and N_2 is defined as:

$$n = \frac{V_{N1}}{V_{N2}} \tag{1}$$

Hence, according to Fig. 2 (a) and by applying Kirchhoffs Voltage Law (KVL), the voltage equations of the inductors and magnetizing Lm in state I can be written as:

$$V_{L1} = V_{dc} \tag{2}$$
$$V_{L2} = V_{C1} \tag{3}$$
$$V_{Lm} = \frac{V_{C3} - V_{C2}}{n-1} \tag{4}$$

From Fig. 2 (b) and by applying KVL, the voltage expressions of the inductors and magnetizing L_m in the mode II are derived as:

$$V_{L1} = V_{dc} - V_{C1} \tag{5}$$
$$V_{L2} = V_{C1} + V_{C2} - V_o \tag{6}$$
$$V_{Lm} = \frac{-V_{C2}}{n} \tag{7}$$
$$V_{L2} = \frac{V_{C2}}{n} - V_{C3} + V_{C1} \tag{8}$$

By using the volt-second balance law for the inductors and magnetizing L_m, we have:

$$\int_0^{DTs} V_{L1}\,dt + \int_{DTs}^{Ts} V_{L1}\,dt = 0 \tag{9}$$
$$\int_0^{DTs} V_{L2}\,dt + \int_{DTs}^{Ts} V_{L2}\,dt = 0 \tag{10}$$
$$\int_0^{DTs} V_{Lm}\,dt + \int_{DTs}^{Ts} V_{Lm}\,dt = 0 \tag{11}$$

Where D and T_s represent duty cycle and switching period of the proposed converter. From (1) - (11), the voltage across capacitors C_1, C_2, and C_3 are achieved:

$$V_{C1} = \frac{1}{1-D}\,V_{dc} \tag{12}$$
$$V_{C2} = \frac{nD}{(1-D)^2\,(n-1)}\,V_{dc} \tag{13}$$
$$V_{C3} = \frac{n-1+D}{(1-D)^2\,(n-1)}\,V_{dc} \tag{14}$$

Also, the output dc voltage is obtained as:

$$V_o = \frac{n-1+nD}{(1-D)^2\,(n-1)}\,V_{dc} \tag{15}$$

As a result the voltage gain expression is rewritten:

$$G = \frac{V_o}{V_{dc}} \frac{n-1+nD}{(1-D)^2\,(n-1)} \tag{16}$$

According to (16) and Fig. 4, it is clearly found that the suggested converter provides high voltage boost ability by lowering the transformer's turns ratio. This fact results in lower cost and volume of the suggested topology implementation.

E. *Voltage Stress on the Semiconductors*

From Fig. 2 (b), it is obvious that the voltage stress across the power switch S is equal to the difference of the voltage on capacitor C_2 and output voltage.

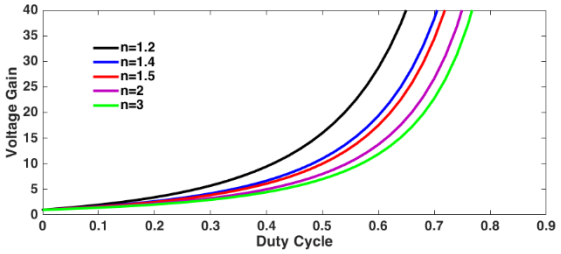

Fig. 4. Duty cycle versus voltage conversion ratio of the DWQ-ESC various *n*.

Accordingly, the voltage across on the power switch S is achieved from (17):

$$V_S = V_o - V_{C2} = \frac{(n-1)V_o}{n-1+nD} \quad (17)$$

The voltage stress across the diode D_1 can be obtained from Fig. 2 (a) as follows:

$$V_{D1} = V_{C1} = \frac{(1-D)(n-1)V_o}{(n-1+nD)} \quad (18)$$

From Fig. 2 (b), the voltage stress across the diode D_2 is obtained as:

$$V_{D2} = V_o - V_{C1} - V_{C2} = \frac{D(n-1)V_o}{n-1+nD} \quad (19)$$

From Fig. 2 (a), the voltage stress across the diode D_3 is achieved as follows:

$$V_{D3} = \frac{V_{C3} - V_{C2}}{n-1} + V_{C3} = \frac{nV_o}{n-1+nD} \quad (20)$$

Finally, the voltage stress across the output diode D_o is obtained from Fig. 2 (a) and (21):

$$V_{Do} = V_o - V_{C2} = \frac{(n-1)V_o}{n-1+nD} \quad (21)$$

III. Comparing Proposed DWQ-ESC with Similar Topologies

In order to show the merits of the presented circuit, a comparison with existing quadratic non-isolated step-up topologies is provided, as it is possible to observe in Table I. For a fair comparison with addressed transformer based quadratic structures the transformer's turns ratio of the suggested topology is assumed $N = 1/n = N_2/N_1$. Fig. 5 depicts the voltage conversion ratio versus the switching duty ratio of the introduced topology and addressed converters in Table I with N= 0.8. It can be found that the proposed topology provides higher voltage gain compared with other converters at the duty cycle range $D > 0.35$. Also, the normalized maximum voltage stress across the power switch and the maximum peak reverse voltage on the output diode of the referenced converters in Table I are presented in Fig. 6 and Fig. 7, respectively.

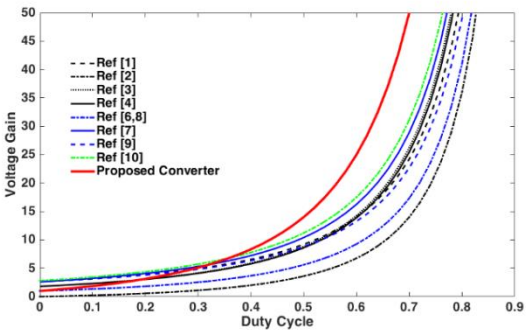

Fig. 5. Comparison of the voltage conversion ratio versus duty cycle in DWQ-ESC and existing quadratic topologies with N=0.8.

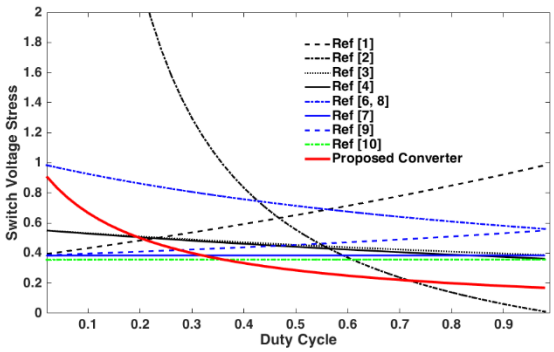

Fig. 6. Comparison of the normalized voltage stress on the power switch in DWQ-ESC and existing quadratic topologies with N=0.8.

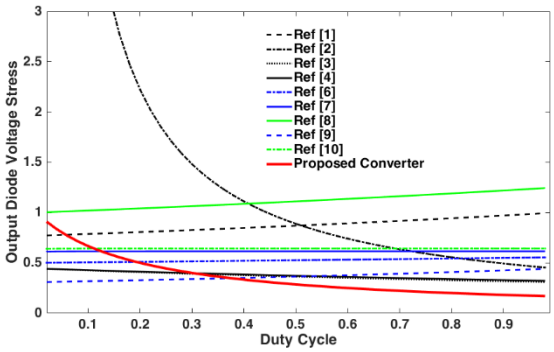

Fig. 7. Comparison of the normalized voltage stress on the output diode in DWQ-ESC and existing quadratic topologies with N=0.8.

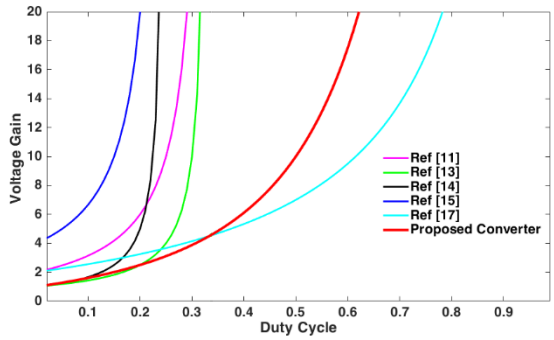

Fig. 8. Comparison of the voltage gain and control range of duty cycle in DWQ-ESC and existing trans inverse converters with n=1.5.

According to these results, the presented topology offers the lowest value of voltage stress in comparison to the other converters. This leads to circuit design with semiconductor components including MOSFET and diodes with the smaller resistance of drain-source. In comparison with transformer types of impedance source dc-dc converters, the proposed topology provides a wider control range of the duty cycle. Fig. 8 demonstrates that Γ-source [13] and asymmetrical Γ-source [14] networks where the proposed trans-inverse converters in [11] and [15] suffer from narrow switching duty ratio control range. Additionally, the suggested DWQ-ESC offers a higher voltage gain compared with the new trans-inverse semi SEPIC converter which provides a higher voltage conversion ratio in the smaller switching duty cycle.

TABLE I. COMPARISON OF THE HIGH VOLTAGE NON-ISOLATED QUADRATIC CONVERTERS

Converter Topology	No. of Components					Voltage Gain	Voltage Stress on Switches	Voltage Stress on Output Diodes
	s	d	c	CI+L	T			
[1]	2	4	4	1+1	12	$\frac{1+D+2N(1-D)}{(1-D)^2}$	$\frac{V_o(1+D)}{1+D+2N(1-D)}$	$\frac{2V_o}{1+D+2N(1-D)}$
[2]	2	3	3	1+1	10	$\frac{(1+N)D}{(1-D)^2}$	$\frac{(1-D)V_o}{(1+N)D}$	$\frac{NV_o}{(1+N)D}$
[3]	1	6	5	1+1	14	$\frac{1+N+ND}{(1-D)^2}$	$\frac{V_o}{1+N+ND}$	$\frac{NV_o}{1+N+ND}$
[4]	1	6	5	1+1	14	$\frac{N(3D+2)+(2-D)}{2(1-D)^2}$	$\frac{(2+D(N-1))V_o}{N(3D+2)+(2-D)}$	$\frac{2NV_o}{N(3D+2)+(2-D)}$
[6]	1	6	4	1+2	14	$\frac{1+ND}{(1-D)^2}$	$\frac{V_o}{1+ND}$	$\frac{(2+D(N-1))V_o}{1+ND}$
[7]	2	6	6	1+1	16	$\frac{1+2N}{(1-D)^2}$	$\frac{V_o}{1+2N}$	$\frac{NV_o}{1+2N}, \frac{NV_o}{1+2N}$
[8]	1	5	3	1+2	12	$\frac{1+ND}{(1-D)^2}$	$\frac{V_o}{1+ND}$	$\frac{(1+D(N-1))V_o}{1+ND}$
[9]	1	6	5	1+1	14	$\frac{1+N(2-D)}{(1-D)^2}$	$\frac{V_o}{1+N(2-D)}$	$\frac{NV_o}{1+N(2-D)}$
[10]	1	5	4	1+1	12	$\frac{2+N}{(1-D)^2}$	$\frac{V_o}{2+N}$	$\frac{(1+N)V_o}{2+N}$
Proposed DWQ-ESC	1	4	4	1+2	12	$\frac{1+D-N}{(1-N)(1-D)^2}$	$\frac{(1-N)V_o}{1+D-N}$	$\frac{(1-N)V_o}{1+D-N}$

s=switch, **d**=diode, **c**=capacitor, **CI** =coupled-inductor, **L**=inductor, **T**=Total Device Count.

IV. SIMULATION RESULTS

Simulation results of the proposed DWQ-ESC in Matlab/Simulink software are provided to verify the mathematical expressions and theoretical principles. The circuit parameters of the suggested DWQ-ESC are supposed as follows; inductance of the inductors are L_1=L_2=200 μH, the capacitance of the capacitors are C_1=C_2=C_3=C_o=100 μF, and the switching frequency of the single switch S is f_s=50 kHz. The input voltage is considered 24 V which is related to RES such as PV panel or fuel cell. The output voltage is considered more than 400 V that is suitable for high voltage dc micro grid applications and EV systems. For this purpose, the duty cycle is supposed as a practical value of about D = 0.5. Also, using the low number of transformer's turns ratio as $n = N_1/N_2$ = 120/100 = 1.2, the introduced topology offers a high voltage boost ability by low input dc voltage source and small switching duty ratio. Fig. 9 (a) verifies the characteristics waveforms of DWQ-ESC in CCM which has been presented in Fig. 3. Furthermore, from the current waveform of the input inductor L_1, it is obvious that the introduced topology draws a continuous input current from the dc-source that makes it appropriate for RES like PV and fuel cell systems. Fig. 9 (b) demonstrates the voltage and current stress across the diodes and the power switch which verify the mathematical equations of the (17) – (20). As seen from the simulation results, the voltage stress on the power switch is about 100 V when the output voltage is around 400 V. Also the voltage stress on D_1, D_2, D_3 and D_o are approximately 50 V, 50 V, 600 V and 100 V which verify the theoretical analysis by simulation results. The voltage and current stress waveforms on the output diode which verify the equation (21) are demonstrated in Fig. 9 (c). According to simulation results, it is obvious that the voltages stress on the power switch and the output diode are lower than the output voltage. Finally, the voltage equations of the capacitors and the output voltage which have been obtained from (12) to (15) are verified by Fig. 9 (d). The voltage stress on the capacitors C_1, C_2 and C_3 are about 48 V, 288 V and 336 V, respectively. Furthermore, the suggested topology operates under the output voltage of about 400 V, an efficiency of 95.6% and the output power of 400 W which are suitable for dc micro grids.

V. CONCLUSION

This study introduces a novel high voltage dc-dc converter applicable in renewable energy sources applications. Presented topology utilizes a single semiconductor power switch which simplifies the control scheme. It benefits from a combination of the voltage boosting module and coupled inductors to obtain high output voltage suitable for dc- micro grid and high voltage applications such as EV charging systems. Due to the unique structure of the coupled inductors, the suggested topology obtains a high voltage conversion factor in the practical duty cycle by lowering the transformer's turns ratio. Unlike the impedance source topologies and most of the other high voltage gain dc-dc topologies, the suggested DWQ-ESC offers a wide control range of switching duty ratio instead of the narrow range. The introduced topology not only inherits the advantages of the non-isolated transformer types of quadratic and SEPIC converters but also provides a higher voltage conversion ratio with low normalized voltage stress across its semiconductors that has been demonstrated in the comparison section. Also, a clamping circuit is considered for the effect of leakage inductance of the coupled inductor to avoid producing voltage spikes on the power switch. Simulation results were presented to validate the proposed converter's performance.

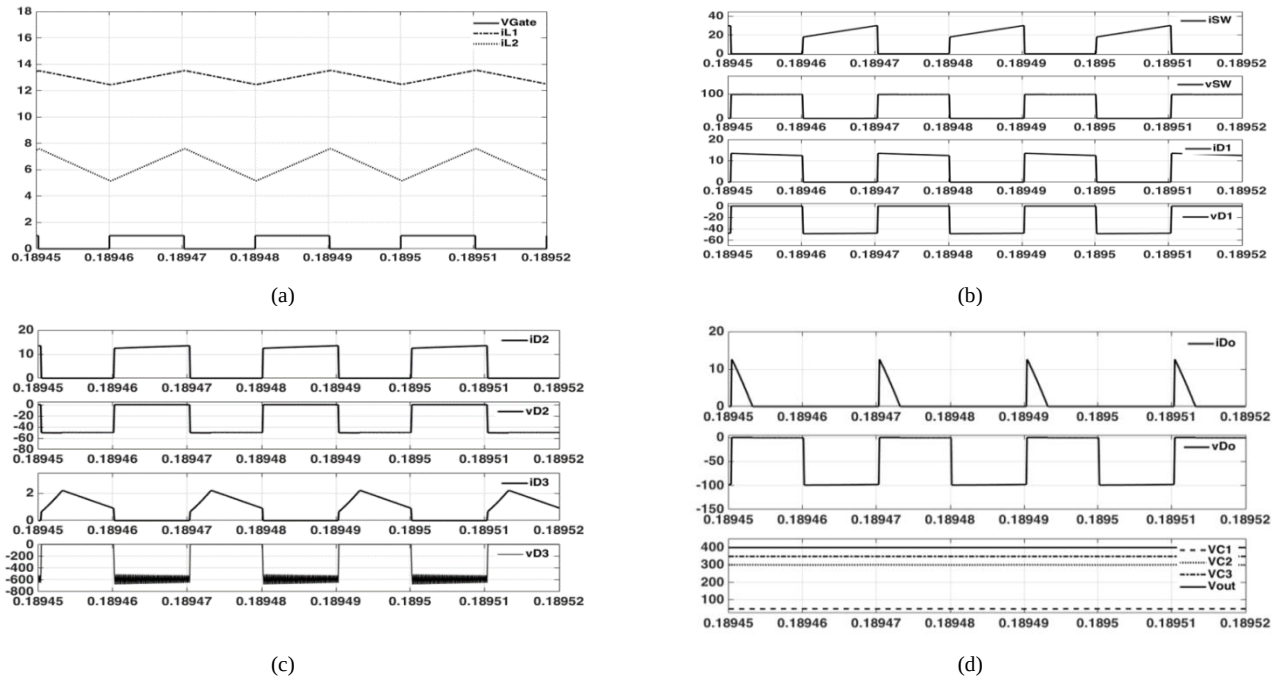

Fig. 9. Simulation results of the proposed DWQ-ESC, *(a). i_{L1} and i_{L2}, (b). i_{sw}, v_{sw}, i_{D1}, and v_{D1}, (c). i_{D2}, v_{D2}, i_{D3}, and v_{D3}, (d). i_{Do}, v_{Do}, V_{C1}, V_{C2}, V_{C3} and v_{out}.*

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