Tampereen yliopisto

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LOW VOLTAGE THIN-FILM TRANSISTORS WITH ATOMIC LAYER DEPOSITED HIGH-K DIELECTRIC

Master's Thesis
Engineering and Natural Sciences
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April 2021

ABSTRACT

Aleksi Ruhanen: Low Voltage Thin-Film Transistors with Atomic Layer Deposited High-κ Dielectric
Master's thesis
Tampere University
Degree Programme in Science and Engineering
April 2021

Atomic layer deposition (ALD) is a thin film deposition technique investigated as a method to solventlessly deposit gate insulators with thin-film transistors. Low temperature (<300 °C) ALD combined with solution-processed semiconductor deposition would enable transistor fabrication on flexible substrates, which cannot withstand temperatures used in conventional silicon gate oxide processes. In this thesis, aluminum oxide and hafnium oxide dielectrics along with an indium oxide semiconductor solution are deposited on silicon wafers and glass slides to fabricate candidate thin-film transistors, and to fabricate metal-insulator-semiconductor capacitor test structures.

Dielectric thicknesses of 10-30 nm were deposited at 120-300 °C and the In_2O_3 was baked at 300 °C. Dielectric thickness was measured through ellipsometry and roughness by atomic force microscopy (AFM). The 10 nm thick Al_2O_3 and HfO_2 dielectrics proved highly leaky, with current densities of ~1 mA/cm^2 even under mild voltage bias. Thicker insulators, up to 30 nm, reduced leakage currents to ~1 μA/cm^2. General transistor performance proved poor, with common on-off ratios of less than 10^2, with the best device achieving a ratio of 10^4. Saturation electron mobilities were measured at around 1-10 cm^2 V^{-1}s^{-1}, similar to what has been achieved in previous reports with the same semiconductor recipe. Density of interface traps in MOS-capacitors on n-type silicon were around 10^{12} – 10^{13} for both HfO_2 and Al_2O_3 dielectrics. Leakage current mechanisms in capacitor structures was investigated with graphical methods, but no conclusive results were determined at this time.

ALD deposited gate dielectrics proved usable in thin-film transistors, but, owing to the poor performance, further research is required, with special focus on the semiconductor-insulator interface. If the process is improved without increasing the thermal budget, there should be no major barriers in fabricating transistors on flexible substrates such as polyimide and polyurethane.

Keywords: Atomic Layer Deposition, Thin-film Transistor, Metal-Oxide-Silicon Capacitor, Oxide Semiconductors, Flexible Electronics,

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TIIVISTELMÄ

Aleksi Ruhanen: Matalajännitteinen ohutkalvotransistori atomikerroskasvatetulla hilaeristeellä
Diplomityö
Tampereen yliopisto
Teknis-luonnontieteellinen DI-tutkinto-ohjelma
Huhtikuu 2021

Atomikerroskasvatus (ALD) on menetelmä ohuiden pinnoitteiden kasvatukseen, jonka käyttöä tutkittiin ohutkalvotransistorien hilaeristeiden valmistuksessa. Matalan lämpötilan (<300 °C) atomikerroskasvatusprosessi yhdistettynä liuospohjaiseen indiumoksidipuolijohteeseen mahdollistaa transistorien valmistamisen prosessilämpötiloissa, jotka soveltuvat joustaville pohjamateriaaleille. Tässä työssä valmistettiin ohutkalvotransistoreja piikiekkojen ja lasilevyjen päälle alumiinioksidi sekä hafniumoksidi hilaeristeillä, sekä metalli-eriste-puolijohdekondensaattoreita piikiekoille.

Eristeitä kasvatettiin 10–30 nm paksuiksi 120–300 °C lämpötiloissa ja indiumoksidiliuos kovetettiin 300 °C lämpötilassa. Eristepintojen sileys todettiin atomivoimamikroskoopilla ja paksuus mitattiin ellipsometrillä. 10 nm Al_2O_3 ja HfO_2 hilaeristeet osoittautuivat riittämättömiksi ja vuotovirta oli yli 1 mA/cm^2 miedollakin jännitteellä. Paksummilla eristeillä saatiin ~1µA/cm^2 vuotovirtoja. Transistorien yleinen suorituskyky oli heikko, useimpien transistorien on-off virtojen suhde oli alle 10^2, paras mitattu on-off suhde oli 10^4. Elektronimobiliteetti oli välillä 1-10 cm^2 V^{-1}s^{-1} joka vastasi hyvin aikaisempia tutkimustuloksia samalla puolijohdemateriaalilla. Kondensaattorirakenteilla tutkittiin pii-eriste pinnan pintatilatiheyttä, joka oli 10^{12} – 10^{13} sekä Al_2O_3 että HfO_2 eristeillä. Kondensaattorirakenteiden vuotovirtamekanismia tutkittiin graafisin menetelmin, mutta yksiselitteistä syytä virralle ei löydetty.

ALD:llä kasvatetut hilaeristeet osoittautuivat toimiviksi, mutta hyödyllisten transistorien valmistus vaatii jatkotutkimusta. Etenkin puolijohde-eriste rajapinnan ominaisuuksia on syytä pyrkiä parantamaan. Mikäli prosessia onnistutaan kehittämään nostamatta käytettyjä lämpötiloja, voidaan ohutkalvotransistoreja valmistaa mm. polyimidi- ja polyuretaanikalvoille.

Tämän julkaisun alkuperäisyys on tarkastettu Turnitin OriginalityCheck –ohjelmalla.

PREFACE

This thesis was done in Tampere University Laboratory for Future Electronics as a part of a group effort to create flexible transistors for use in high-speed, low power circuits. I wish to thank the entire LFE group, especially my supervisors Prof. Paul Berger and Dr. Serges Zambou, as well as Prof. Donald Lupo for their advice. Additionally, I wish to thank Matin Forouzmehr and Miao Li for their vital help in the experimental work, especially with the special global circumstances this work was made in.

I would like to thank Dr. Kimmo Lahtonen for the XPS analysis and Dr. Mari Honkanen for SEM analysis, and Maimouna Niang for her collaboration with the device simulation.

Tampere, 27.4.2021

Aleksi Ruhanen

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LIST OF SYMBOLS AND ABBREVIATIONS

AFM	Atomic Force Microscope
ALD	Atomic Layer Deposition
CMOS	Complementary Metal-Oxide-Silicon
C-V	Capacitance-Voltage
FN	Fowler-Nordheim
IGFET	Insulated-Gate Field-Effect-Transistor
IGZO	Indium-Gallium-Zinc-Oxide
MOS	Metal-Oxide-Silicon
MOSCAP	Metal-Oxide-Silicon Capacitor
MOSFET	Metal-Oxide-Silicon Field-Effect-Transistor
PE-ALD	Plasma-Enhanced Atomic Layer Deposition
PECVD	Plasma-Enhanced Chemical Vapor Deposition
PF	Poole-Frenkel
T-ALD	Thermal Atomic Layer Deposition
TCAD	Technology Computer Aided Design
TDMAH	Tetrakis(dimethylamido)hafnium
TFT	Thin-Film Transistor
TMA	Trimethylaluminum
XPS	X-ray Photoemission Spectroscopy

κ	Dielectric constant
μ	Saturation electron mobility
C_{ox}	Oxide capacitance
D_{it}	Interface trap density
I_d	Drain current
I_g	Gate current
SS	Subthreshold swing
V_{ds}	Drain-source voltage
V_{fb}	Flatband voltage
V_g	Gate voltage
V_t	Threshold voltage

.

1. INTRODUCTION

New usages for flexible electronics demand transistor fabrication on flexible substrates, which are limited by the fabrication thermal budget and the processes used herein. Silicon wafers are inflexible, and typical silicon processes reach temperatures which would evaporate common flexible substrates such as polyimide film, making conventional Si MOSFETs impractical. An alternative is found in thin-film transistors (TFT) where the semiconductor and dielectric are deposited through lower temperature vacuum processes, or by solution processing directly atop flexible substrates.

Thin-film transistors differ from MOSFETs by using only a thin layer of semiconductor atop an inert, non-conducting substrate as opposed to atop a bulk crystalline silicon wafer. While similar in operation, the underlying physics of the devices are different as the thin-film does not have the long-range order of monocrystalline silicon, leading to lower mobilities and allowed trap states inside the forbidden energy bandgap, heavily influencing device behavior. The semiconductors of choice are usually either organic semiconductors or metal oxide semiconductors, with indium, gallium and zinc oxides and their combinations being used industrially, and ongoing research aims to improve performance by e.g., increasing electron mobility in the material, while dropping operational voltages.

Atomic layer deposition (ALD) is a technique used for conformal thin-film deposition of metal oxides and other materials. Precursors are pulsed into the reaction chamber in cycles enabling self-limiting controlled growth, roughly 1 Å per cycle. In this thesis, atomic layer deposition is used to deposit Al_2O_3 and HfO_2 high-κ dielectrics at different temperatures and different thicknesses to act as the gate insulator in a thin-film transistor and as the insulator in a metal-insulator-semiconductor capacitor test structure, with both thermal and plasma-assisted deposition being used.

Atomic layer deposition is combined with spin-coated indium oxide to create thin-film transistors at low process temperatures, along with certain test structures to investigate the compatibility and performance of the resulting devices. The goal is to fabricate devices with high on/off ratio and a low threshold voltage for use in flexible electronics with minimal power consumption, and the different devices are compared to each other by

their electrical performance and physical properties such as electron mobility and interface trap density.

2. THEORY

The Insulated-Gate Field-Effect Transistor (IGFET), and its most common implementation as the Metal-Oxide-Semiconductor Field-Effect-Transistor (MOSFET), are three-terminal (ignoring the bulk connection) electronic devices where a high impedance gate controls the conductivity between the source and the drain [1]. These devices are manufactured on silicon wafers by using high temperature processes to grow, or deposit, an oxide layer on the silicon, and then using photolithographic methods to expose some areas of the wafer at a time, allowing for selective doping to manufacture a desired device in a controlled, parallel process.

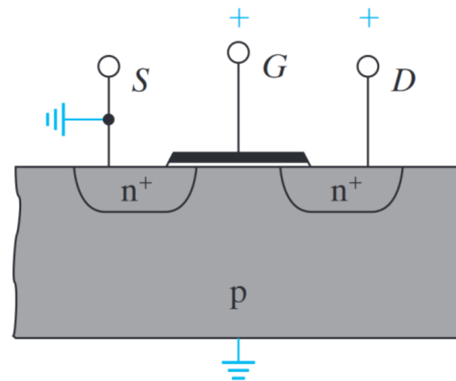

Figure 1. *Typical long channel planar n-channel MOSFET structure, from Ref. [2]*

Figure 1 depicts a typical long channel planar n-channel MOSFET. The channel has p-type doping and under zero-bias condition presents a potential barrier to the n-doped source and drain, no current flows and the device is off [1,3].

When the gate voltage, V_g, is swept from negative to positive with the semiconductor bulk grounded, the MOS structure goes from accumulation, to flatband, to depletion and finally to inversion. With a negative gate voltage, holes accumulate to the interface from the bulk semiconductor, increasing the energy of the conduction band near the interface. With increasing gate voltage, the device enters flatband state, where the conduction and valence band energies in the semiconductor do not bend near the insulator. This flatband voltage, V_{fb}, depends on the work function difference between the metal and the semiconductor with an added contribution by charges on the oxide-semiconductor interface [1].

With $V_g > V_{fb}$, the positive charge at the gate is enough to repel holes from the semiconductor-oxide boundary eventually depleting the surface of positive carriers, reducing the

surface band energy. When the voltage is increased far enough the intrinsic energy level of the semiconductor bends below the Fermi level at the interface, the majority carrier at the interface is now n-type, and the surface is inverted. The channel between the source and the drain is now conductive as the potential barrier is reduced. With low source-drain voltage V_{ds}, the current through the channel scales linearly with V_{ds} and the device operates in linear or triode region, but at a certain threshold the current becomes constant in respect to V_{ds} and the device is in saturation region [1].

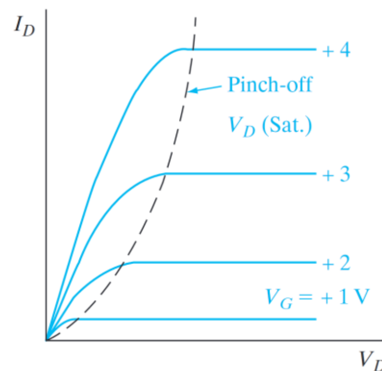

Figure 2. *Typical MOSFET I_d-V_d characteristics at various V_g, from source [1]*

The dashed line in Figure 2 separates the linear and saturation regimes of the device. The equation for saturation drain – source current in a MOSFET is approximated as [1]

$$I_d = \frac{W}{L}\mu C_{ox}\frac{\left(V_g - V_t\right)^2}{2}, \tag{1}$$

where *W* and *L* are the physical width and length of the channel, μ the mobility, C_{ox} oxide capacitance, V_g gate voltage and V_t the threshold voltage. In saturation, the drain current does not grow with increasing drain voltage. This effect is called *pinch off*, and is caused by the drain-source voltage narrowing the channel on the drain end [1,3].

In switching use, it is desirable to have a transistor with minimal drain current when the device is off, however devices still have some channel conductance when $V_g < V_t$, called subthreshold conduction [1]. The subthreshold performance of a transistor is characterized by its subthreshold slope, with values of 70 mV/decade having been achieved for high-performance devices [1]. This value is the change in gate voltage required for the drain current to change by an order of magnitude, with lower values resulting in less power consumption due to undesired off-state current.

In this idealized model, the gate leakage or current flow through the oxide is zero, and the source and drain semiconductor-metal connections are perfectly ohmic, achieved through a doping gradient. In real devices, gate leakage is always present and is a critical

factor in gate stack engineering. Real devices also contain impurities and defects as a result of the manufacturing process, metallic contamination of Fe or Cu at the oxide/semiconductor interface degrades oxide integrity [4], alkaline ion impurities create mobile charges in the oxide [4], and physical defects such as vacancies in the crystal lattice, often created by hot carrier effects, create generation-recombination sites. The allowed discrete energy levels created by defects are collectively called traps. Fabrication methods and methodologies seek to minimize the defects in devices and thus semiconductor work is commonly done in cleanrooms and cleaning processes such as the RCA clean are used.

In modern very large-scale integration semiconductor processes the complementary metal-oxide-semiconductor (CMOS) is the basis of the technology, where pairs of p- and n-type MOSFETs form realizations of logic circuits usable in high-speed logic. Increasing device performance requires ongoing miniaturization of the transistors [5], and the famous Moore's law posits that the number of transistors in integrated circuits doubles every two years, a prediction made in 1975 that has held well to this day [6]. This miniaturization is achieved through advances in lithography allowing smaller features to be created, e.g., shorter gate lengths, and was coupled with oxide thinning until recently [5]. At the so called 45nm process node, which was adopted around 2007, Intel began replacing silicon oxide with hafnium oxide, a high-κ dielectric, that allows for a physically thicker insulator layer with the performance of a thinner silicon oxide layer, avoiding overwhelming leakage issues due to electron tunneling through a thin oxide [7].

2.1 High-κ dielectric

The capacitance *C* for a parallel plate capacitor is [4]

$$C = \frac{\kappa \epsilon_0 A}{d}, \tag{2}$$

where ϵ_0 is vacuum permittivity, *A* the plate area and *d* the separation between the plates. κ is the dielectric constant of the dielectric. In a conventional MOSFET device the gate dielectric is thermally grown silicon dioxide, which has a dielectric constant of 3.9. Increasing gate capacitance increases device performance, and oxide thinning is a simple way to achieve this, but reducing the oxide thickness too far exponentially increases the tunneling current density through the dielectric. As an alternative, so called high-κ dielectrics are used which have a dielectric constant higher than that of SiO_2, allowing a higher physical thickness with the same capacitance [8].

There are several mechanisms for conduction through dielectric films, and they can be divided into electrode-limited and bulk-limited mechanisms [9]. In electrode-limited mechanisms the metal-dielectric interface and the barrier height are critical parameters. Electrode-limited mechanisms include Schottky-emission, where electrons gain enough thermal energy to cross the potential barrier, Fowler-Nordheim (FN) tunneling, and direct tunneling. In electron tunneling, the barrier is high enough to prevent thermionic emission, but the wavefunction of the electron penetrates through the thin barrier allowing them to pass through. The barrier height depends on the electrode and dielectric materials used, high-bandgap dielectrics presenting a higher barrier [8,9].

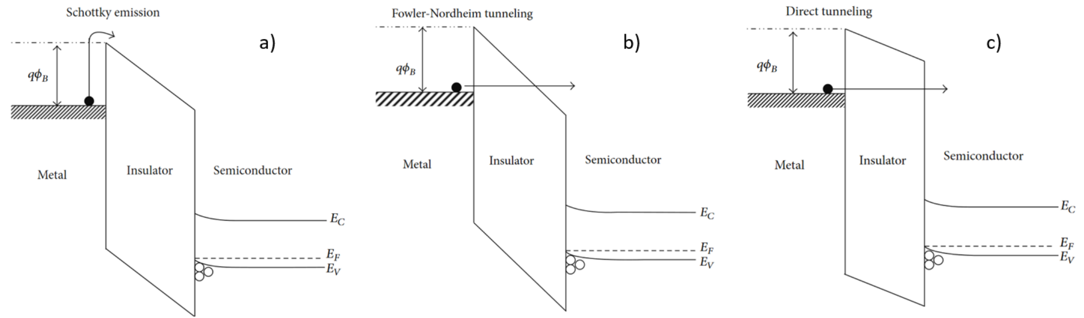

Figure 3. *Electrode-limited conduction mechanisms, modified from source [9]*

Figure 3 illustrates the different mechanisms. The equation for Schottky emission current is [9]

$$J = A^{*}T^{2}\exp\left(-\frac{q\left(\phi_{\mathrm{B}} - \sqrt{\frac{qE}{4\pi\epsilon_{r}\epsilon_{0}}}\right)}{kT}\right), \tag{3}$$

Where, A^* is the effective Richardson constant, *T* temperature, ϵ_0 and ϵ_r vacuum permittivity and optical dielectric constant, $q\phi_B$ Schottky barrier height and *E* the electric field across the film.

Fowler-Nordheim (FN) tunneling is the dominant leakage method for oxide thicknesses greater than 4 nm, below which direct tunneling dominates. The difference between the mechanisms is that in FN tunneling the penetration happens through a triangular potential barrier, which approximates the insulator barrier under an electric field. In direct tunneling the entire barrier is penetrated [9]. The FN current density is [4]

$$J_{FN} = AE_{ox}^{2}\exp\left(-\frac{B}{kE_{ox}}\right), \tag{4}$$

where *A* and *B* are constants and E_{ox} is the electric field through the dielectric. As the electric field is $E_{ox} = \frac{V_{ox}}{t_{ox}}$ [4] the current density scales heavily with oxide thickness. Below

4 nm dielectric thickness, direct tunneling becomes the dominant mechanism, effectively creating a hard limit to oxide thinning. Direct tunneling current through a 1.5 nm thick SiO_2 layer exceeds 1 A/cm^2 [8].

In bulk-limited mechanisms the structure of the dielectric determines the conductivity, with the trap states being the most important factor [9]. Bulk-limited mechanisms include Poole-Frenkel (PF) [10] emission, hopping conduction and ohmic conduction [9]. In P-F emission, electrons are thermally excited from traps into the conduction band, while in hopping conduction electrons tunnel through from one trap state to another. In ohmic conduction, electrons gain enough energy to be excited to the conduction band, electrons can also be excited to the conduction band from trap states. [9]

SiO_2 grown on a silicon wafer has a very high bandgap and can produce a very high-quality film, with which alternative dielectrics must compete. The conduction mechanisms can be experimentally identified to an extent in I-V characteristics by the way the current scales [11]. For example, Fowler-Nordheim tunneling current should be linear in a plot of log(I/V^2) vs. 1/V [12] and independent of temperature, while Schottky current scales with temperature [11].

2.2 MOS-Capacitor

An important structure related to the MOSFET is the MOS-Capacitor (MOS-C, MOS-CAP). It is the same structure as the MOSFET, except without the source and drain electrodes and doping regions, and thus just a linear structure of the gate metal – insulator – silicon wafer. While not important as a production device, the MOSCAP is a very useful test structure used to explain phenomena in semiconductors, and as a research structure, allows the investigation of a number of bulk and interface effects [4].

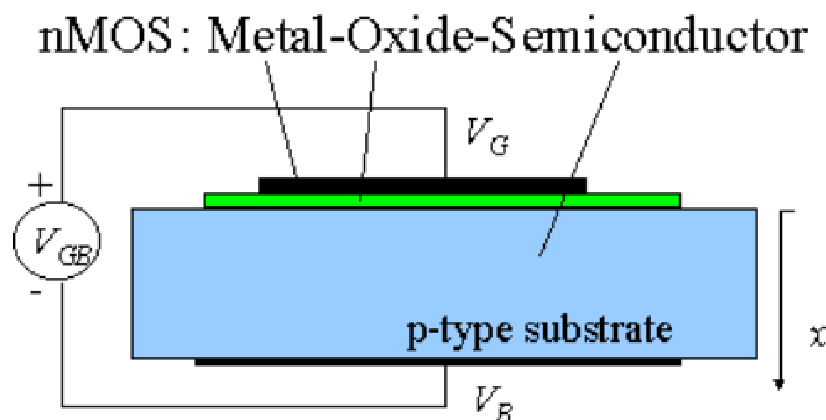

Figure 4. *nMOS Capacitor structure, from Ref. [13]*

Figure 4 depicts a typical nMOS MOSCAP structure. When the gate bias voltage is swept, the device goes through accumulation – depletion – inversion same as a MOSFET, and in these different regions the capacitance of the structure varies.

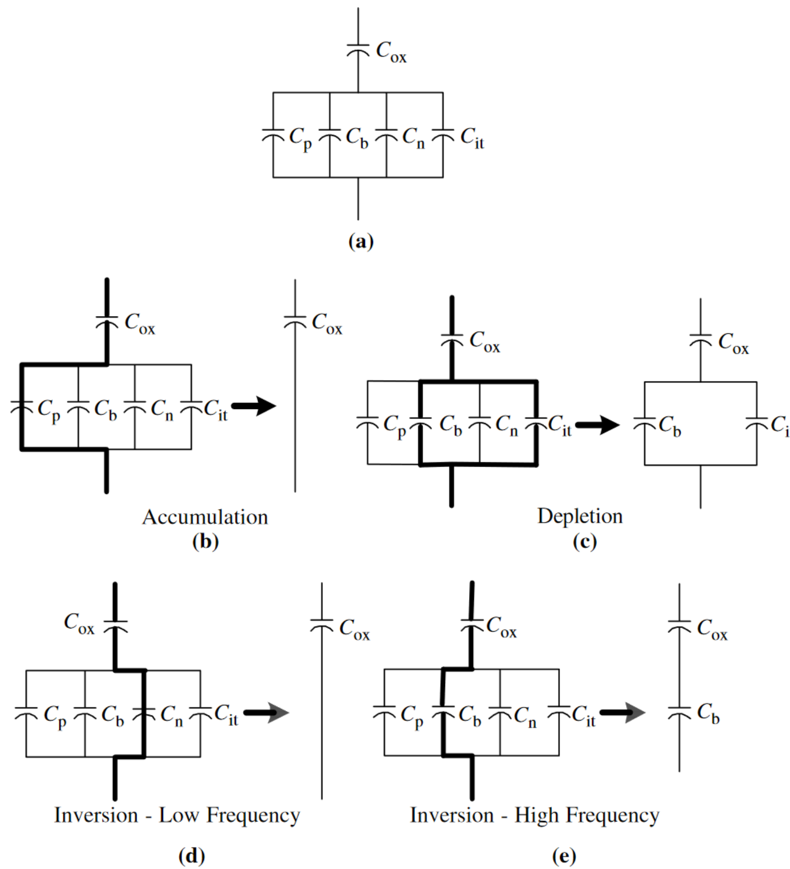

Figure 5. *p-type MOSCAP equivalent circuit in different biasing conditions, from source [4]*

As the biasing is varied, the capacitance is dominated by different charges in the device, with the equivalent circuits depicted in Figure 5. Oxide capacitance, C_{ox}, is always in series with the semiconductor, and in a p-type MOSCAP in accumulation, the positive charge dominates with the corresponding capacitance, C_p. C_p is very high so it is treated as a short circuit, leading to C_{ox} being the overall capacitance. In inversion, with negative charge and corresponding capacitance, C_n, the same effect is seen when the biasing voltage is kept at a low frequency, i.e., a capacitance measurement is performed by summing a small signal AC-component to the DC bias, and the frequency of the AC-signal is low. However, when a high frequency is used, the overall capacitance is reduced as the slow recombination/generation of carriers is unable to follow the fast signal, exposing the semiconductor bulk charge and its capacitance, C_b. In depletion, the space charge and interface trapped charge C_{it} become dominant in overall capacitance [4].

From this model, a clear experimental use for MOSCAP structures is measuring the oxide capacitance, which has been used to measure the thickness of the native oxide layer which has a known dielectric constant [4]. In the context of high-κ dielectrics, the thickness is measured independently and used with the capacitance measurement to find out the dielectric constant. Other defects such as oxide charges and interface charges can also be probed with a MOSCAP structure, and leakage current through the oxide can also be measured [4].

An important consideration in all MOS structures is the electrode contact [14]. The source and drain contacts should be ohmic and low resistance in a MOSFET, and so should the back electrode in a MOSCAP structure such as in Figure 4. The work function of the gate electrode is important as it causes band bending in the semiconductor and oxide [1], shifting the flatband voltage, and the metal-oxide barrier must be high enough to prevent current injection.

2.3 Thin-film transistor

Thin-film transistors (TFT) are distinct from MOSFETs by having a thin semiconductor layer as opposed to a thick wafer. The semiconductor is deposited as a uniform layer without the channel or source and drain regions having been formed by doping. The semiconductor is not grown as a monocrystal, instead having a polycrystalline or amorphous form depending on the deposition and annealing [15]. This fundamentally changes the channel formation mechanism in TFTs, as the lack of long-range structural order introduces allowed electron states inside the bandgap [3]. Hydrogenated amorphous silicon is a common semiconductor material in flat-panel display TFTs, and the material contains defects in the form of dangling bonds where a silicon atom has an unbounded electron due to strain in the Si-Si network. Some of these bonds are satisfied by bonding with the included nitrogen [3].

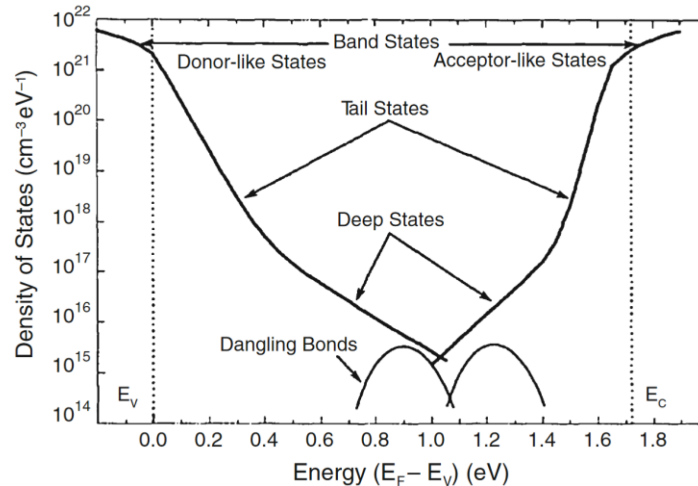

Figure 6. *Density of states distribution of a-Si:H, from [16]*

Figure 6 shows the density of states in undoped a-Si:H, with dangling bonds creating allowed states inside the bandgap.

Due to these allowed states inside the bandgap, TFTs operate in accumulation mode [15] as opposed to MOSFETs which operate in inversion [17]. The first thin film transistor [18] was demonstrated in 1962 using microcrystalline cadmium sulfide as the active layer, and evaporated silicon monoxide as the insulator on a glass substrate. TFTs have found extensive commercial use in display technology and show great potential in flexible and wearable electronics. TFT processes for flat panel display production traditionally use amorphous (a-Si) or polycrystalline silicon (poly-Si), with amorphous oxide semiconductors (AOS) [19] and organic semiconductors as more recent developments [3].

2.4 Device simulation

In electronic device simulation, the term technology computer-aided design (TCAD) means the simulation and modelling of electronic devices through the gamut of circuit simulation, semiconductor device modelling and semiconductor process simulation. Circuit simulators such as SPICE have broad usage from through-hole-technology circuit simulation on PCBs down to integrated circuits consisting of individual transistors fabricated on silicon. In contrast to this, a device simulator aims to simulate a single device.

A semiconductor device simulator is at minimum, a differential equation solver capable of solving Maxwell's equations and drift-diffusion equations in the context of a semiconductor. The simulator used in this thesis is Silvaco Atlas which uses finite element method on a 1D, 2D or 3D simulation grid, and device simulation begins with defining this grid. In Atlas, the physical properties of the device are then defined, the dimensions, material regions and material parameters. The simulator contains material properties for

common semiconductor and insulator materials along with a variety of empirical and analytical equations related to them, and from the device simulations common transistor properties such as transfer curves can be obtained [20].

Thin-film transistor simulation requires extraction of the density-of-states in the semiconductor layer, and in Atlas they are specified as coefficients of exponential tail states and gaussian deep states. The total density-of-states is specified as exponential valence and conduction bands with two deep level bands:

$$g(E) = NTA \exp\left(\frac{E - E_c}{WTA}\right) + NTD \exp\left(\frac{E_v - E}{WTD}\right) + NGA \exp\left(-\left(\frac{EGA - E}{WGA}\right)^2\right) + NGA \exp\left(-\left(\frac{E - EGD}{WGD}\right)^2\right), \quad (5)$$

where the three letter combinations are coefficients, E_c and E_v conduction and valence band, respectively, and E the energy. Hence, the density of states must be fitted to this equation using the coefficients [20].

Dielectric leakage mechanisms can also be simulated. While direct tunneling and Fowler-Nordheim tunneling can be described as statistical processes with certain coefficients similar to equation 3. Trap-assisted leakage mechanisms are more challenging to simulate as trap energies and other variables such as their density of states must be assumed [20].

3. METAL OXIDE SEMICONDUCTORS AND INSULATORS

Metal oxides are chemical compounds of a metal cation and at least one oxygen atom. Metal oxides are solid in room temperature and usually have high melting points and high resistance to solvents, while still being attacked by some acids [21]. Metal oxides have a crystalline or amorphous structure, which heavily influences their electrical properties. In the field of semiconductor devices, silicon oxide is the most important one, in the conventional CMOS process SiO_2 is thermally grown and selectively etched to pattern high density integrated circuits. Outside the electronics industry, common glass is a mixture of silicon dioxide and sodium or calcium oxides, and due to their refractory properties they are used in applications such as brake pads.

3.1 Metal oxide gate dielectric

As mentioned in the previous chapters, SiO_2 had been the most common gate insulator material in MOSFETs, but other, high-κ materials are desired to achieve higher gate capacitance. Metal oxides used as gate dielectrics include Al_2O_3, HfO_2, ZrO_2, Ta_2O_5 and TiO_2 [22].

Material	Dielectric constant	Bandgap (eV)
SiO_2	3.9	9.0
Al_2O_3	9	8.8
HfO_2	25	6.0
TiO_2	80	3.3
Ta_2O_5	26	4.5
ZrO_2	25	7.8

Table 1. *Material properties of high-κ dielectrics [23]*

Table 1. contains material properties of select dielectrics. To be useful as a gate insulator, the dielectric must be compatible with the semiconductor and gate electrode material and introduce minimal defects to the interface [22]. The dielectric must also present a sufficiently high barrier to electrons in the semiconductor to inhibit thermionic emission. An ideal material would have both a high dielectric constant and a large bandgap, but in practice few materials satisfy both conditions [24].

Metal oxide layers can be deposited by thermal growth, anodization [25--27], sputtering, solution processing [28] and atomic layer deposition. Different deposition methods effect

the stoichiometry and structure of the film. According to some [15] amorphous semiconductors are preferred as grain boundaries limit mobility, but on the other hand methods for low temperature crystallization to enhance mobility have been reported [29].

The materials used in this thesis are aluminum oxide and hafnium oxide deposited by ALD. Aluminum oxide has a hexagonal crystal lattice and appears in many crystalline phases, with α-Al_2O_3, also known as corundum, being the most thermodynamically stable one [30]. The gemstones ruby and sapphire are formations of aluminum oxide. In microelectronics, aluminum oxide is used as a gate insulator and as a passivation layer. Aluminum oxide can be deposited by anodization of aluminum metal or by ALD.

Atomic layer deposition of aluminum oxide is commonly done with trimethylaluminum (TMA) $(CH_3)_3Al$ precursor. In this process, TMA is pulsed sequentially with an oxidant, water in thermal-ALD and oxygen plasma in plasma-assisted ALD. The trimethylaluminum decomposes into free methyl groups and aluminum ions which attach to the oxygen bonds on the substrate. In the thermal-ALD process, the relationship between chamber temperature and growth per cycle was studied to tune the deposition process.

While structural analysis of the films was not performed, previous reports suggest the ALD deposited Al_2O_3 film is amorphous [31]. Plasma-assisted ALD was investigated as a method to deposit aluminum oxide film with higher quality than with a thermal process at the same process temperature, however, the benefit of plasma-assist in gate dielectrics may be negligible. PE-ALD is however useful for low temperature deposition of e.g., moisture barriers [32].

Hafnium oxide is a high-κ material that has found industrial usage, and it was also investigated as a gate insulator deposited by a thermal-ALD process. The as-deposited film did not perform very well, however.

3.2 Metal oxide semiconductors

In addition to their utility in dielectrics, some metal oxides can be used as the active layer in thin-film transistors. Oxides of indium, tin, zinc, gallium and binary or ternary compounds of them are a target of active research. The first oxide semiconductors reported in 2004 [33] had a field effect mobility of around 5 $cm^2\ V^{-1}s^{-1}$, while in 2020 up to 100 $cm^2\ V^{-1}s^{-1}$ has been reported [34]. The focal points of oxide semiconductor research are in improving the mobility and stability of the layer by studying new materials compositions, deposition methods and post-annealing methods, while attempting to move away from expensive rare-earth minerals such as indium [34].

As opposed to amorphous silicon where the band structure is influenced by the dangling Si bonds, in oxide semiconductors the ionic bonding between metal cations and oxide anions results in a Madelung potential separating the ion orbitals with the metal cation s-states forming the conduction band minimum and the oxygen anion p-states forming the valence band maximum [3]. In oxides of post transition metals, the s-state orbitals overlap in crystalline and amorphous lattices, allowing for high electron mobilities in these structures [3].

In the ternary In-Ga-Zn oxide system, the lattice structure, electron mobility and free carrier concentration can be controlled by adjusting the composition of the compound as well as the deposition conditions. In deposition by sputtering, the oxygen vacancies can also be controlled by adjusting the oxygen pressure in the chamber [19].

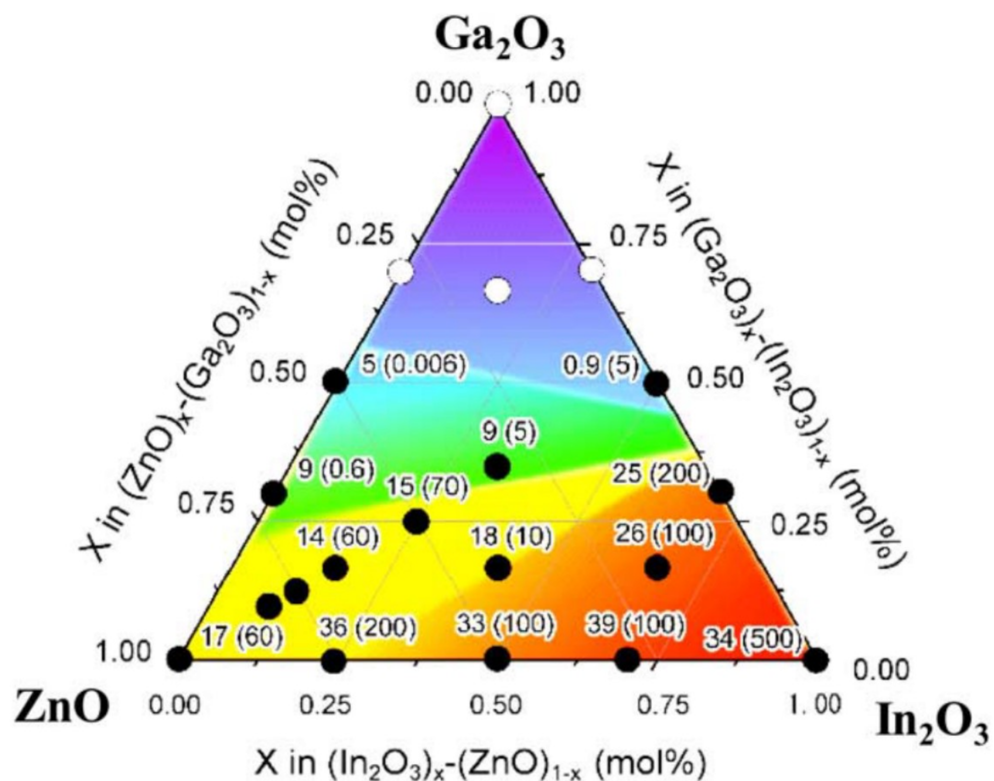

Figure 7. *Hall mobility and carrier density (in parenthesis) of In-Ga-Zn-O compound. From source [35]*

Figure 7 shows a composition triangle of RF-sputtered In-Ga-Zn-O (IGZO) semiconductor ternary compound. While the highest mobility is achieved with a very indium rich composition, common compositions usually incorporate zinc and gallium to improve the stability of the film and reduce free carrier concentration [19]. While adding gallium reduces the electron mobility, it reduces the amount of oxygen vacancies and thus the

amount of free carriers [19]. The semiconductor used in this thesis is indium oxide deposited through spin-coating, which, while not directly comparable to the RF-sputtered materials, should have the same structural considerations with the concerns about oxygen vacancies and free carrier concentration.

As TFTs operate in accumulation, the conductivity threshold is not as simple as in MOSFETs where the channel is inverted. The conduction threshold in IGZO TFTs was studied by Lee *et al*. [17] and they report that deep and tail trap states inside the bandgap determine the channel conductivity. The structural disorder in the semiconductor film creates allowed states inside the bandgap, and in IGZO TFTs, the conduction threshold is crossed as applied gate voltage shifts the Fermi level from deep to tail states [17]. The importance of trap states is reflected in device simulation, many methods for extracting the density of states in a TFT through electrical and optical measurements have been demonstrated followed by accurate device simulations [36--39].

3.3 Atomic layer deposition

Atomic layer deposition (ALD) is a self-limiting chemical vapor deposition technique where two precursor chemicals are introduced into the reaction chamber one after another. The precursors bond with the substrate surface and with one another, but do not react with themselves, and the surface becomes saturated where thin films can be grown one atomic layer at a time [40]. First introduced in 1974 as atomic layer epitaxy by Suntola *et al*. as a means to fabricate electroluminescent displays, ALD has since found use in a variety of industries as means to deposit highly conformal films [41].

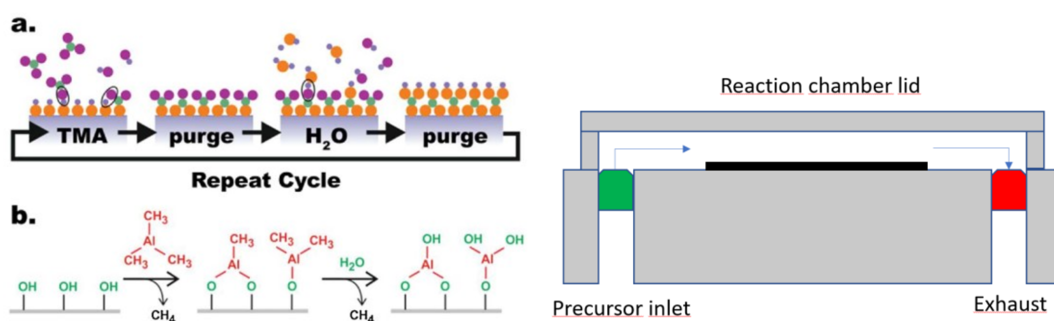

Figure 8. *TMA-H_2O ALD reaction schematic representation, from source [42], and cross-flow T-ALD chamber schematic*

By controlling the pulse and purge lengths, the complete saturation of the surface is achieved while making sure the precursor vapors are removed from the chamber prior to introducing the other precursor, excessive pulse and purge times increase the deposition time and waste the precursor chemicals. The chamber temperature is controlled as it effects the properties of the film being deposited. In the processes used in this

thesis, the precursors are an organometallic compound and an oxidizer. In so-called thermal-ALD (T-ALD), where the reaction energy is received from the chamber temperature alone, the oxidizer used is H_2O, which is pulsed into the vacuum chamber by its own vapor pressure. Figure 8 contains a schematic representation of a complete cycle of a thermal-ALD process.

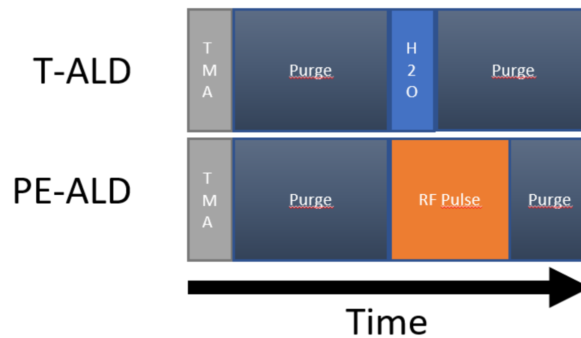

Figure 9. *T-ALD and PE-ALD cycle comparison*

In plasma enhanced ALD (PE-ALD) the oxidant is provided by a plasma "showerhead" mounted above the substrate. The showerhead contains a capacitively coupled plasma source, where a gas flows through the capacitor plates and gets excited into a plasma which is introduced into the reaction chamber. The gas is constantly flowing to prevent precursor flow back into the plasma equipment, but the reaction only happens during the RF pulse as pictured in Fig. 9. The gas used in this thesis is 80/20 N_2/O_2 mixture, the N_2 is used to reduce the corrosion in the equipment.

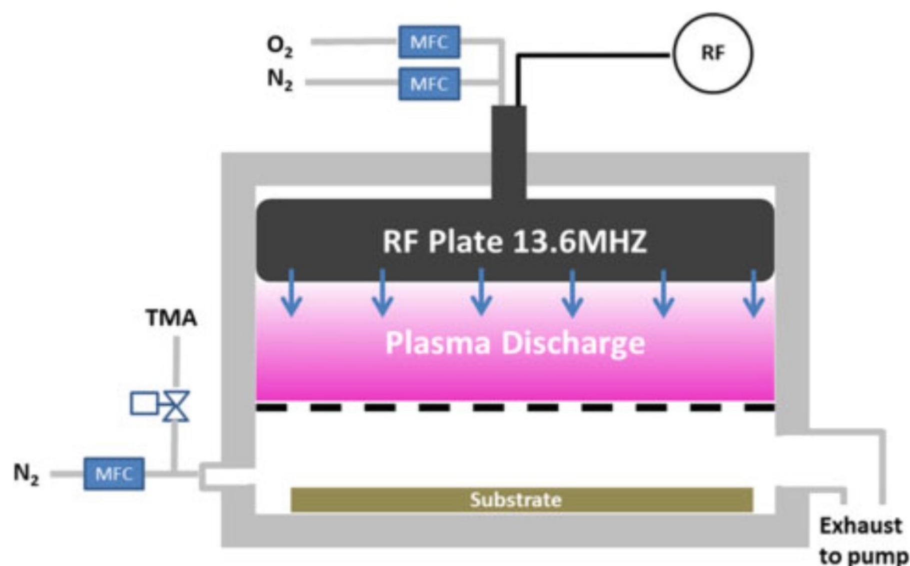

Figure 10. *Schematic representation of PE-ALD in a Beneq TFS-200, from source [32]*

Figure 10 depicts the PE-ALD setup in a Beneq TFS-200 similar to the one used in this thesis. The precursor trimethylaluminum (TMA) is also depicted in the figure, which is used to deposit aluminum oxide. The deposition of aluminum oxide is one of the most studied ALD processes [40], being used as a high-κ dielectric [43], moisture barrier [32] and a passivation layer. The primary dielectric used in this thesis is Al_2O_3 deposited with TMA precursor, using both a thermal and a plasma-assisted deposition. HfO_2 was deposited using TDMAH as a precursor.

4. DEVICE CHARACTERIZATION AND SIMULATION

Thin-film structures and transistors are characterized through electrical measurements as well as optical, electron and probe microscopy. The electrical measurements are DC drain current probing in response to drain and gate voltage and gate current vs. gate voltage. Gate-source/drain capacitance is probed by low and high frequency AC measurement. From these measurements, important characteristics such as threshold voltage, on-off ratio, oxide capacitance, electron mobility and subthreshold swing can be extracted. In addition, the density-of-states and interface trap density can be approximated and used in device modeling.

4.1 Threshold voltage

The threshold voltage V_t is the minimum gate-source voltage required to create a conducting channel between the drain and the source.

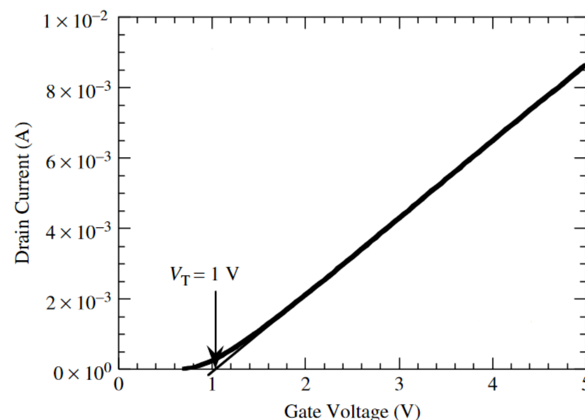

Figure 11. *Threshold voltage determination by extrapolation, modified from source [4]*

Figure 11 depicts a graphical method for determining the threshold voltage. A line is extrapolated from the maximum slope of the V_g-I_d curve to the x-axis intercept, which is the threshold voltage [4].

4.2 On-off ratio

The on-off ratio is the ratio of drain current when the device is in saturation vs. when the device is off, or $V_g < V_t$. On-off ratio is an important performance figure for transistors as suppression of off-state current directly leads to less power consumption.

4.3 Subthreshold slope

Subthreshold slope (SS) and its reciprocal, subthreshold swing, quantify the subthreshold conduction of the device. It is defined as the change in gate voltage required for the drain current to change by one decade, when $V_g < V_t$.

$$SS = \frac{dV_g}{dlog_{10}(I_{ds})}. \tag{6}$$

In conventional devices, subthreshold swing is ultimately limited by the thermionic limit, which at room temperature is 60mV/dec. Modern MOSFETs can achieve values as low as 70mV/dec [1].

4.4 Carrier mobility

Carrier mobility in saturation can be extracted from an I_d-V_g sweep combined with capacitance measurement of the gate oxide [4].

$$\mu_{sat} = \frac{\left(\frac{\partial\sqrt{I_D}}{\partial V_g}\right)^2}{\frac{1}{2}C_{ox}\frac{W}{L}}. \tag{7}$$

Higher carrier mobility leads to a larger saturation current as seen in Eq. (1). Electron mobility with the In_2O_3 solution recipe used has been in 3 to 8 $cm^2 V^{-1}s^{-1}$ range in previous reports [25,44].

4.5 Contact resistance

The semiconductor-metal interface has some resistance which is in series with the rest of the device. The total resistance R_T of a metal-semiconductor-metal MOSCAP structure is [4]

$$R_T = R_c + R_{sp} + R_{cb} + R_p, \tag{8}$$

where R_c, R_{sp}, R_{cb} and R_p are respectively the top contact resistance, spreading resistance, back interface resistance and probe/wire resistance. Neglecting the back interface and probe resistance, and approximating the spreading resistance as

$$R_{sp} = \frac{\rho}{2\pi r}\arctan\left(\frac{2t}{r}\right), \tag{9}$$

where ρ is the semiconductor bulk resistivity, t thickness and r the electrode diameter, the contact resistance can be solved as

$$R_c = R_T - R_{sp}. \tag{10}$$

By measuring the contact resistance of different sized electrodes and plotting contact resistance vs. electrode area, the contact resistivity is the slope of the plot [4]. Measuring the contact resistivity is important to establish the quality of the electrodes. In addition, I-V plots of the metal-semiconductor-metal structure shows whether the contacts are ohmic or nonlinear.

4.6 Capacitance-voltage measurements in MOSCAP structures

Capacitance-voltage (C-V) measurements are carried out by applying a DC bias to the circuit to which a small AC signal is superimposed. In capacitance measurements of a silicon MOSCAP the accumulation-depletion-inversion regions can be easily identified when sweeping the DC bias.

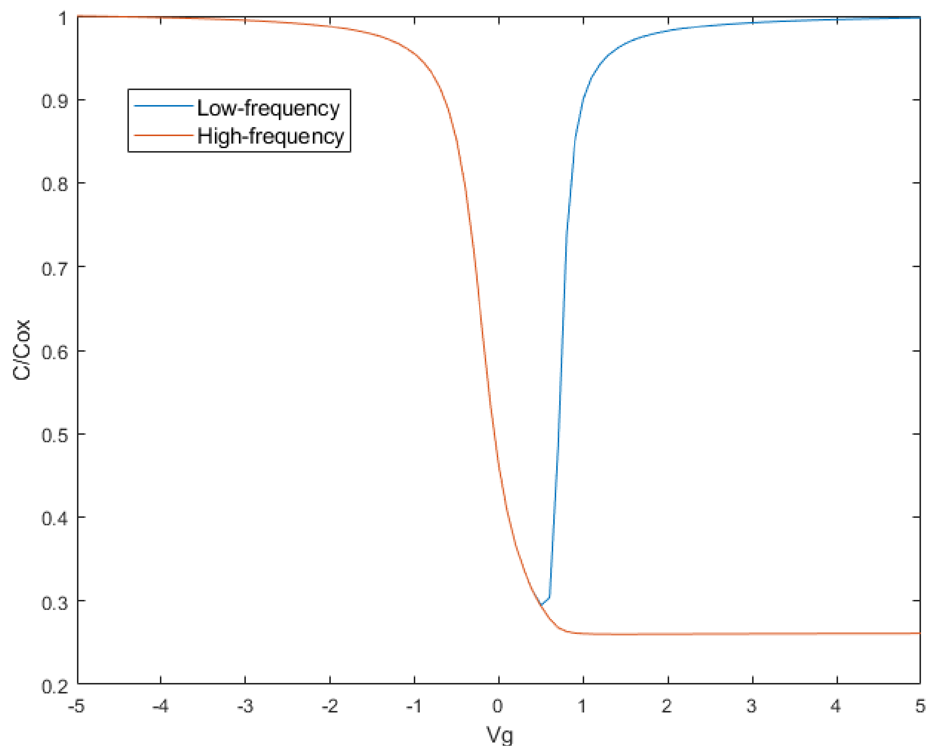

Figure 12. *Low- and high-frequency C-V nMOS characteristics, simulated device with 100 nm SiO2 on 10^{15} doped p-type Si*

Figure 12 shows a simulated capacitance-voltage profile of an ideal MOSCAP. In strong accumulation, the accumulation charge dominates the device capacitance, and the device behaves like a parallel-plate capacitor, hence oxide capacitance can be measured in accumulation [4]. In depletion, the space-charge capacitance in the semiconductor in parallel with the interface charge capacitance increase with the oxide capacitance in series, leading to a decrease in the measured capacitance [4]. In inversion, the high and

low frequency measurements separate, if the minority charges are able to follow the ac signal, the device will act like a parallel-plate capacitor again and approach oxide capacitance. In high frequency measurements however, the charges cannot respond fast enough and the space charge will dominate the measurement [4].

Flatband voltage can be determined by plotting gate voltage versus $(1/C_{hf})^2$, where the flatband voltage is at the knee of the curve, the knee can be identified by differentiating the curve and locating the peak [4].

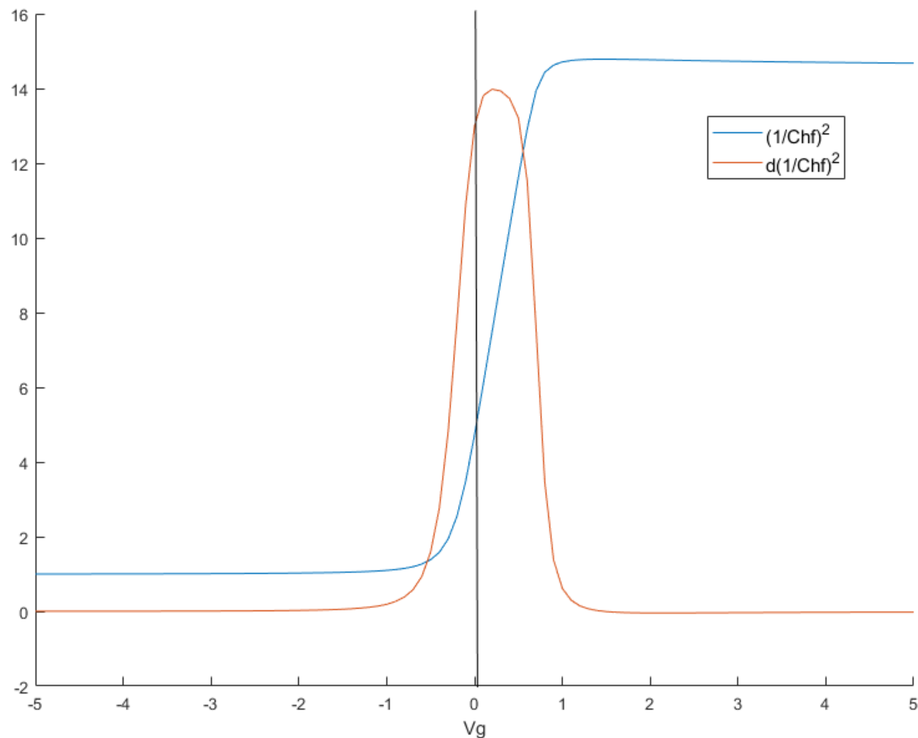

Figure 13. *Flatband voltage in a simulated MOSCAP*

Figure 13 shows an application of this method to a simulated MOSCAP. While the flatband voltage of the device is 0, the differentiated peak is slightly higher, displaying the difficulty in determining the curve.

Capacitance-voltage characteristics can be used to interrogate the fixed oxide charge and interface trap density, as well as be used in determining the density of states in a TFT. Fixed oxide charge is related to the flatband voltage as

$$Q_f = (\phi_{MS} - V_{FB})C_{ox}, \tag{11}$$

which allows the change in fixed oxide charge between similar devices to be quantified in the flatband voltage shift [4].

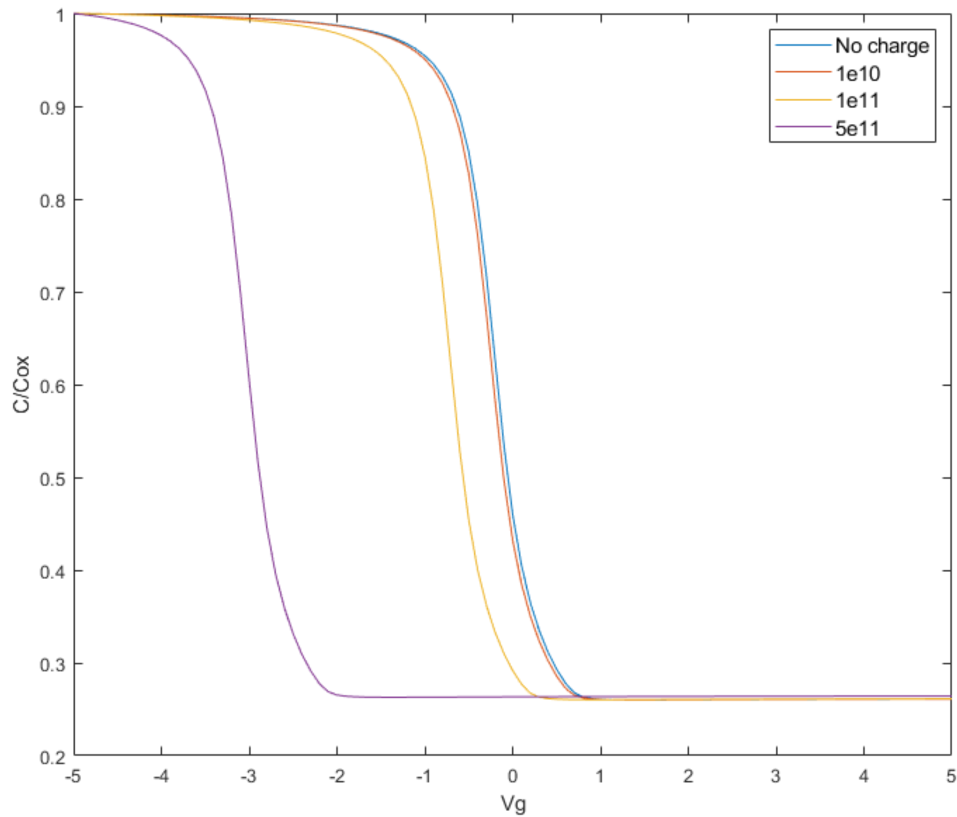

Figure 14. *Flatband voltage and fixed oxide charge in a simulated device*

As seen in figure 14, the flatband voltage shifts significantly as the amount of fixed charge is increased.

The interface trap density can be determined with the conductance method, where the equivalent parallel conductance of the structure is measured as a function of bias voltage and frequency [4]. Equivalent parallel conductance G_p at measurement frequency *f*, is given by

$$\frac{G_P}{2\pi f} = \frac{2\pi f G_m C_{ox}^2}{G_m^2 + (2\pi f)^2 (C_{ox} - C_m)^2}, \tag{12}$$

where G_m and C_m are the measured conductance and capacitance, and C_{ox} the oxide capacitance. The interface trap density D_{it} is approximated as

$$D_{it} \cong \frac{2.5}{q} \left(\frac{G_P}{2\pi f} \right)_{max}, \tag{13}$$

where the maximum conductance is found at a certain frequency. With this method the interface trap density can be examined at different bias voltages.

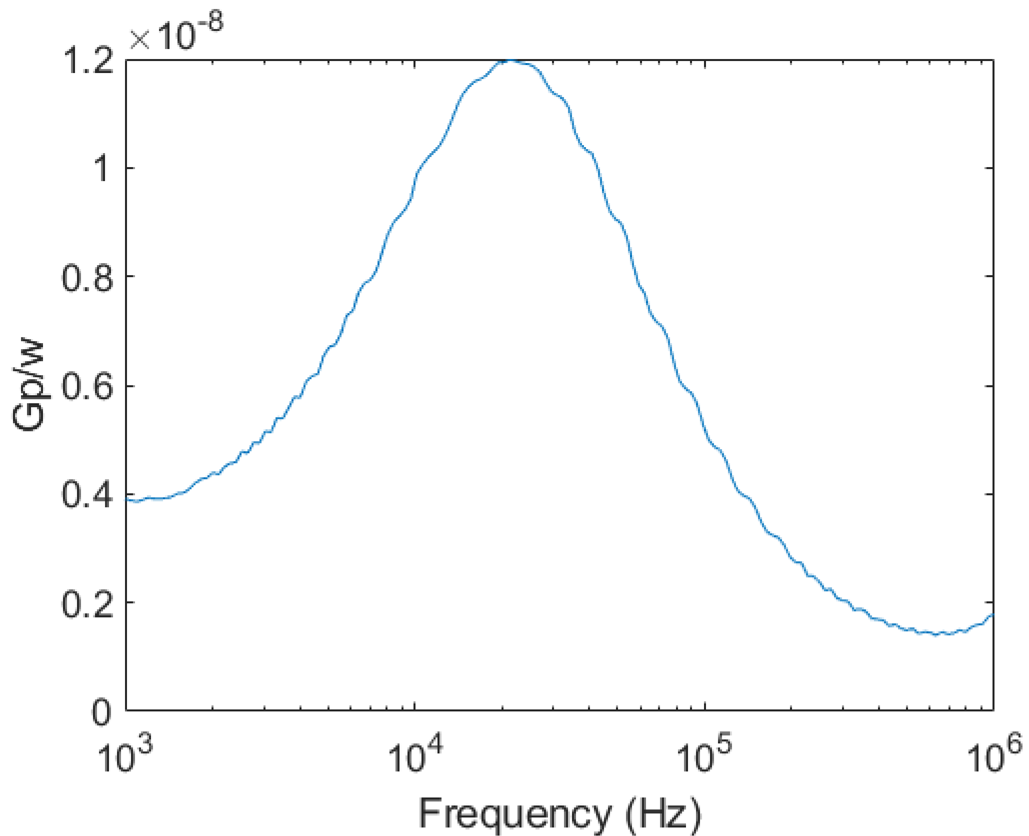

Figure 15. *Conductance plot example from 10nm HfO_2 MOSCAP*

Figure 15 shows the experimental conductance vs. frequency plot of a HfO_2 MOSCAP. The shape of the plot is due to the time-constant of the interface traps and their response to the measurement frequency [4].

4.7 Ellipsometry

Ellipsometry is an optical method used for measuring dielectric properties of a thin film. In the basic setup, a laser is polarized and pointing at the sample at a shallow angle, and a detector with a rotating polarizer is placed on the opposite side to receive the reflected light. The detector measures the amplitude and phase shift of the reflected light which can then be used to compute information about the film, such as its thickness and refractive index [4]. A downside of ellipsometry is that the measured parameters must be fitted to a model to make physical sense of the data [4], and heavily scattering samples cannot be measured. An advantage of ellipsometry is that it is non-destructive and can be used *in situ* to monitor the deposition in, for example, ALD or MBE reactors fitted for the apparatus. The ellipsometer used in this thesis is a Rudolph AutoEL III, with a single wavelength 632 nm He-Ne laser source. The machine automatically calculates the thickness and refractive index of the sample from known optical values for the substrate.

4.8 Atomic Force Microscopy

Atomic force microscopy (AFM) is a type of scanning probe microscopy where a vibrating cantilever is fitted with a microscopical tip that is then scanned across the sample surface [4]. The advantage of using a mechanical probe is that wave phenomena such as the diffraction limit and aberrations are eliminated, allowing the examination of features smaller than what can be achieved on optical microscopes, on the order of 1nm. The AFM imaging done in this thesis is done using the so-called tapping mode, where the cantilever is driven at a certain frequency to “tap” the surface, the system measures the force acting on the tip, which, along with information from the servomotors, is used to determine the surface height [4]. AFM is a relative measurement, offering information on the relative height of surface features without measuring the absolute thickness of the film.

Using a mechanical probe has the disadvantage that the quality of the probe tip is critical for measurement accuracy and resolution. A sharper tip can resolve smaller features than a round one, and if the tip is damaged by, e.g., picking up debris from a sample, artifacts will show up in the measurement [4]. Another error is bowing of the measured surface, caused by errors in the position measurement of the servomotors, this can be corrected in software, however. AFM is used in this thesis to measure the roughness of the dielectric surfaces; excessive roughness would indicate trouble with the deposition process.

5. EXPERIMENTAL WORK AND RESULTS

Samples were fabricated on n-doped silicon wafers and glass microscope slides. Highly doped silicon was used for TFTs and medium doped silicon for MOSCAPs. The manufacturer's (Siegert Wafer) specification for these was 0.003 Ω·cm resistivity for highly doped silicon and 1-10 Ω·cm for medium doped silicon. Sample fabrication began with substrate cleaning. Silicon wafers were cleaned with the RCA cleaning procedure, oxide strip omitted, inside a cleanroom. Glass slides were cleaned in an acetone bath inside an ultrasonic cleaner, followed by an isopropanol bath in an ultrasonic cleaner. Medium-doped silicon was additionally immersed after cleaning in 2% hydrofluoric acid for a few minutes to strip the native oxide layer to reduce the series resistance from a poor back interface contact. The cleaned substrates were transferred to a nitrogen glovebox and aluminum was evaporated on the back surface of the silicon, and a gate pattern was evaporated on glass slides by taping a physical mask on the glass piece.

Dielectric was deposited on the substrates with a Beneq TFS-200 ALD. Aluminum oxide was deposited using trimethylaluminum (TMA) as the metal precursor, and water and O_2/N_2 gas mixture as the oxidant in thermal and plasma-assisted processes, respectively. HfO_2 was deposited using tetrakis(dimethylamido)hafnium (TDMAH) as the metal precursor and water as the oxidant. TDMAH is solid at room temperature so it was used in a heated source, the vapors were carried to the chamber with nitrogen that was bubbled through the source. H_2O and TMA sources were maintained at room temperature and delivered to the chamber through their own vapor pressure. Due to the open-loop deposition control of the ALD, the film thickness was routinely measured by ellipsometry afterwards and some variation exists in films with the same amount of ALD cycles.

The next step for TFTs is deposition of the semiconductor. A 0.2 M indium oxide solution was prepared with a method reported by Leppäniemi *et al*. [44], consisting of dissolving indium nitrate hydrate in 2-methoxyethanol. 100 µl of the solution was spin-coated on the substrate at 8000 RPM followed by a 15-minute cure in 90 °C and 30-minute cure in 300 °C, both in air inside a cleanroom. For some TFT samples an additional 30-minute bake at 150 °C, in air, was performed after electrode deposition. The semiconductor film thickness was not measured due to difficulties in measuring a binary film by ellipsometry, but the presence of the film was visible by a purplish tint on the surface after the spin-coating. The film thickness was measured by transmission electron microscopy in a paper using the same methodology and anodized aluminum oxide dielectric to be around 10 nm [25].

Electrodes were deposited by evaporation. Aluminum was deposited on the back of silicon wafers to improve their contact to the probe station chuck, gate electrode was deposited on top of glass substrates with a shadow mask prior to dielectric deposition. MOSCAP electrodes and source/drain electrodes were also deposited using shadow masks.

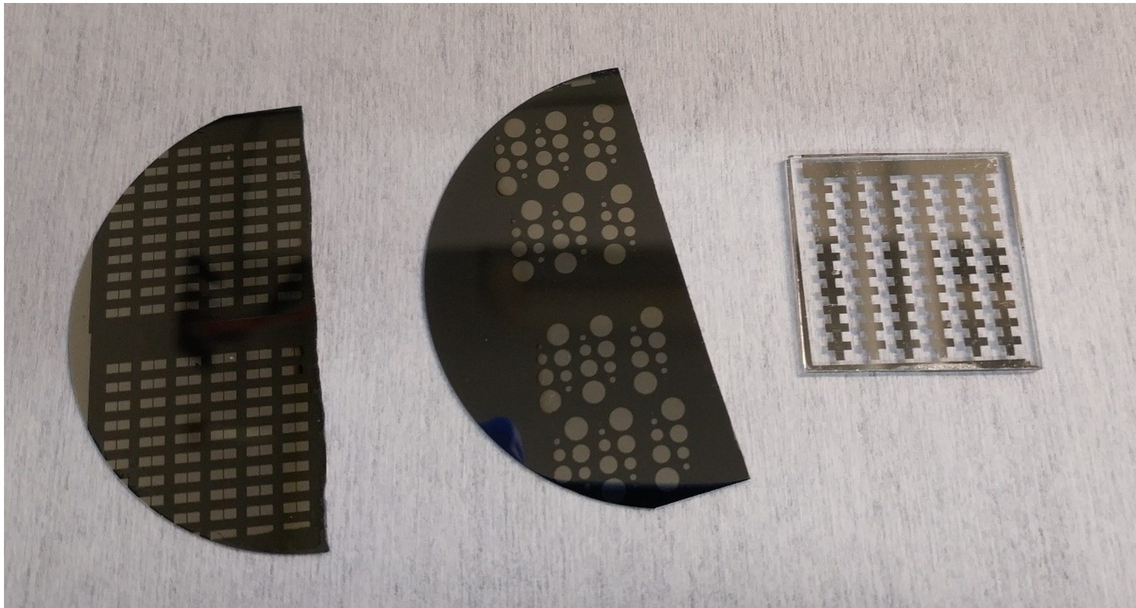

Figure 16. *Left to right, examples of TFT on Si wafer, MOSCAP on Si wafer, TFT on glass microscope slide*

Figure 16 shows typical fabricated samples. In TFTs fabricated on doped silicon, the wafer's only functional purpose is to act as a metallic-like gate, i.e., a conductor. Using a silicon wafer as the gate has some advantages in early prototyping, silicon has a slightly higher work function than aluminum, which should inhibit emission from the gate to the dielectric, and probing and ellipsometry are more practical with a device on silicon. The ellipsometer can be used to measure a spot anywhere on the wafer, while on glass the ellipsometer must be pointed at the gate metal. Probing a device fabricated on glass involves piercing the dielectric layer with the probe tip to contact the underlying gate, while with silicon the probe simply has to touch the probe station chuck on which the wafer is resting. On the other hand, the silicon wafer provides 100% gate overlap, the gate fully overlaps the source and drain electrodes, while on glass the overlap is less. Gate overlap is generally undesirable and increases gate leakage current due to the higher area involved, as well as raises gate capacitance, thereby reducing speed.

In MOSCAP structures, the silicon plays a critical functional role in the metal-insulator-semiconductor structure, the methods based on capacitance measurements introduced in Chapter 4 are specifically for structures on silicon.

5.1 Thermal-ALD Al_2O_3

Aluminum oxide deposited through thermal-ALD was seen as a good baseline dielectric, devices with aluminum oxide dielectric and solution processed indium oxide semiconductor had been reported on in [44] and thus comparisons were readily available. In addition, the T-ALD Al_2O_3 process is a well-studied one and thus the confidence in the process was high. Both TFTs and MOSCAPs were fabricated to study the process both in a device and as just an insulating layer.

	100 °C	250 °C	Anodized
Al:O Ratio	0.567	0.733	0.765

Table 2. *Al:O Ratio of T-ALD Al_2O_3 deposited at 100 °C and 250 °C, and anodized Al_2O_3*

X-ray photoelectron spectroscopy (XPS) was used to measure the Al:O ratio in certain temperatures, and a clear increase in the aluminum fraction is seen when going from 100 °C to 250 °C, with a slightly higher ratio in anodized Al_2O_3.

A set of devices with a 10 nm oxide thickness target was fabricated at ALD chamber temperatures of 120, 200 and 300 degrees Celsius.

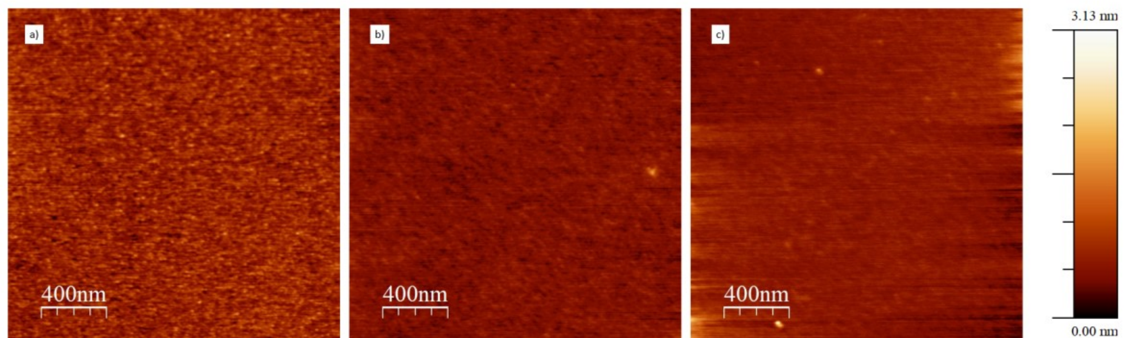

Figure 17. *AFM images of T-ALD Al_2O_3 films deposited at a) 120 °C, b) 200 °C, c) 300 °C*

Deposition temperature	Thickness (nm)	Refractive index	Growth per cycle (Å/cyc)	RMS roughness (nm)
120 °C	8.92	1.72	0.890	0.201
200 °C	10.35	1.67	1.035	0.109
300 °C	9.86	1.72	0.986	0.151

Table 3. *Physical properties of T-ALD Al_2O_3 film*

Table 3 shows that the growth per cycle of aluminum oxide increases when going from 120 °C to 200 °C but is reduced when going back to 300 °C. Refractive index behaves the opposite, being the lowest at 200 °C deposition temperature, this might hint that the film is less dense than with the other temperatures, but further density analysis was not performed. The AFM images in Fig. 17 show no particular surface features.

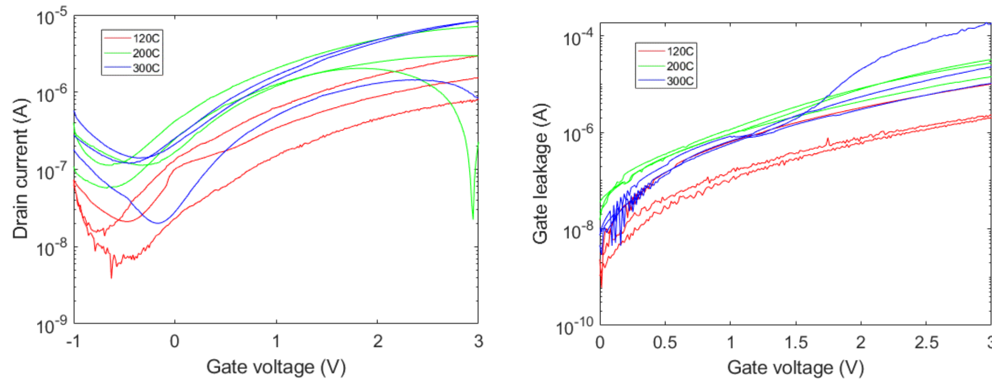

Figure 18. *I_d-V_g and I_g-V_g characteristics of device with 10 nm Al_2O_3 dielectric.*

Figure 18 shows some of the transfer characteristics of devices with 10 nm gate insulator. The TFTs did function as transistors and a quite decent drain current was obtained, but all the devices are fundamentally flawed due to the high gate leakage. I-V characterization of the MOSCAP structures also showed high leakage, suggesting the film might be too thin. C-V characterization was omitted due to difficulties caused by heavy leakage current.

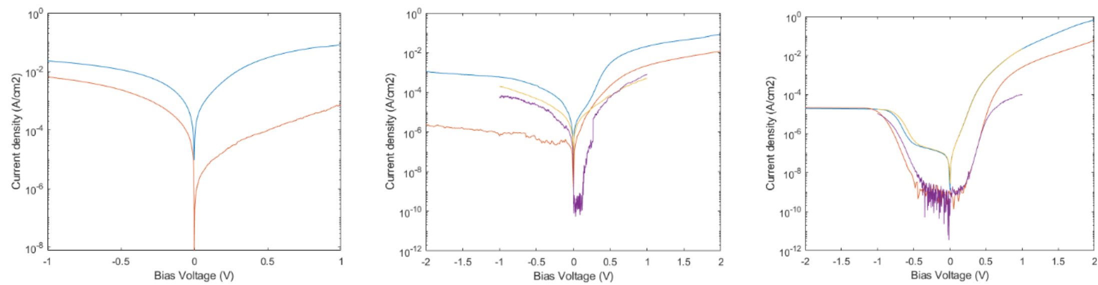

Figure 19. *10 nm Al_2O_3 MOSCAP I-V Characteristics, a) 120 °C, b) 200 °C, c) 300 °C deposition temperature*

As seen in Figure 19, the leakage current density is unacceptable high. Additionally, when going from 200 °C to 300 °C the shape of the plot changes and symmetry is lost between positive and negative bias.

Deposition temperature	**Sub-threshold swing (mV/dec)**	**Threshold voltage (V)**	**On/off ratio**	**Mobility ($cm^2 V^{-1}s^{-1}$)**
120 °C	1750 ± 548	0.78±0.06	~100	~2
200 °C	1090 ± 83	0.70±0.08	~100	~5
300 °C	917 ± 196	0.71±0.13	~100	~4

Table 4. *Electrical properties of 10 nm Al_2O_3 TFTs*

Devices with nominal 20 nm gate oxide showed reduced gate leakage, but a negative threshold voltage shift and worse on-off ratio.

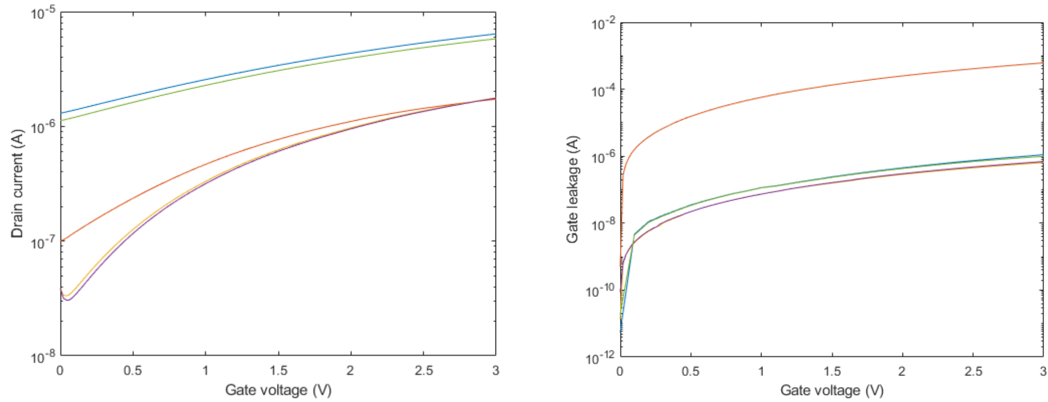

Figure 20. *I_d-V_g and gate leakage plots of TFT with 20 nm Al_2O_3 dielectric*

As seen in Fig. 20 the gate leakage is significantly reduced, but still high compared to the drain current.

Deposition temperature	Sub-threshold swing (mV/dec)	Threshold voltage (V)	On/off ratio	Mobility ($cm^2 V^{-1}s^{-1}$)
200 °C	1381	0	50	~2

Table 5. *Electrical properties of TFT with 20 nm Al_2O_3 dielectric*

A set of devices were made with thermal-ALD Al_2O_3 dielectric and varied spin-coating RPM for the In_2O_3 solution deposition, combined with a 15-minute surface UV treatment in air, to investigate the effect of the thickness of the semiconductor. While the thickness of the In_2O_3 layer was not measured, the thickness of a spin-coated layer increases with reduced RPM.

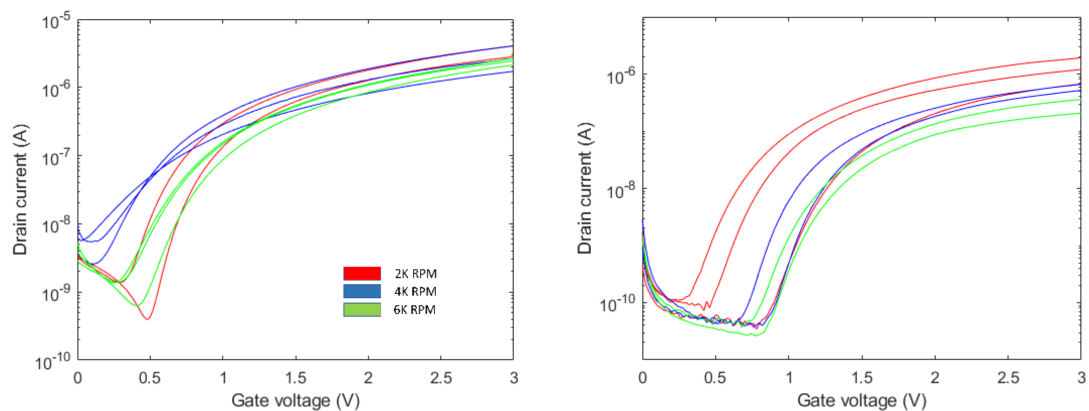

Figure 21. *Id-Vg Characteristics of 20 nm 200 °C Al_2O_3 devices with In_2O_3 spin-coating RPM varied from 2-6K RPM. a) glass substrate, b) silicon substrate*

From the Id-Vg characteristics in Fig. 21 some differences are apparent with the different RPMs. On glass, 4K RPM has the worst on-off ratio and a negative threshold voltage shift from the other RPMs. Mobility seems similar across the devices as the on-state drain current has little variation. With silicon however, 2K RPM has the smallest threshold

voltage and very little difference exists between 4 and 6K RPM. A possible trend in devices on silicon is in the drain current, which is reduced with increasing RPM. Owing to the small sample size however, individual device variation may skew the results.

Substrate and spin-coat RPM	Sub-threshold swing (mV/dec)	Threshold voltage (V)	On/off ratio	Mobility ($cm^2 V^{-1}s^{-1}$)
Si 2K	190 ± 40	1.45 ± 0.12	10^4	N/A
Si 4K	174 ± 64	1.57 ± 0.05	10^4	N/A
Si 6K	200 ± 26	1.9 ± 0.66	10^3	N/A
Glass 2K	193 ± 53	1.26 ± 0.70	10^3	~0.3
Glass 4K	519 ± 104	1.52 ± 0.20	10^3	~0.3
Glass 6K	253 ± 48	1.49 ± 0.07	10^3	~0.4

Table 6. *Electrical properties of TFTs with varied spin-coating RPM*

The most interesting result seen in Table 6 is the significantly improved on/off ratio in contrast to the previous devices. This could be explained by the thicker semiconductor layer being less damaged by the aluminum electrode evaporation, aluminum acts as a p-type dopant and creates oxygen vacancies, and the implantation of aluminum near the semiconductor-dielectric interface could increase the carrier concentration and thus the off-state current.

5.2 Plasma-enhanced-ALD Al_2O_3

Plasma-enhanced ALD with Al_2O_3 was hoped to produce a high-quality dielectric with reduced chamber temperature, as reducing the overall process temperature is desirable to allow a larger variety of substrates to be used. In practice, the devices with PE-ALD Al_2O_3 gate insulator performed worse than ones deposited with a thermal process, and the indium oxide spin-coating failed completely on PE-ALD samples with 200 and 300 °C chamber temperatures. It must however be said that the PE-ALD recipe was not tuned at all, and the default recipe provided by the ALD manufacturer was used, which may or may not be optimal for use in gate dielectrics.

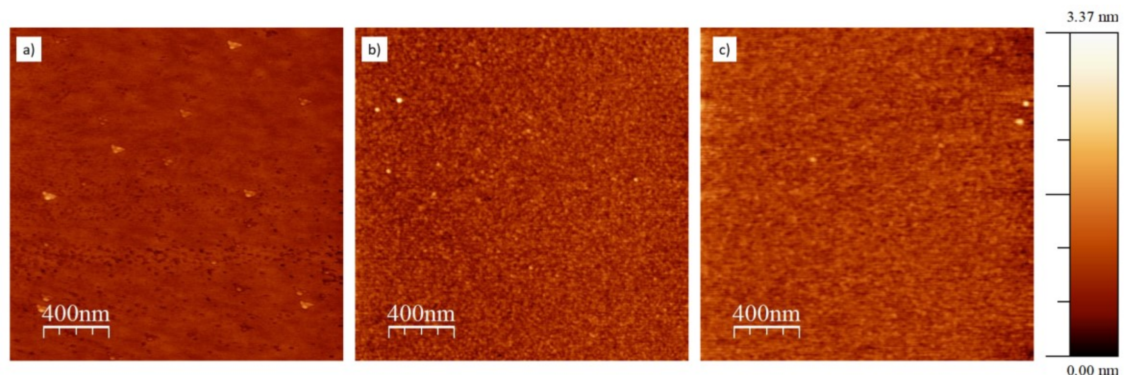

Figure 22. *AFM images of PE-ALD Al_2O_3 films deposited at a) 150 °C, b) 200 °C, c) 300 °C, figure a) contains artefacts*

A 30 nm Al_2O_3 layer was targeted, but due to miscalculated initial growth per cycle all films were around 15 nm. AFM images in Fig. 22 show a smooth film.

Deposition temperature	Thickness (nm)	Refractive index	Growth per cycle (Å/cyc)	RMS roughness (nm)
150 °C	16.6	1.686	1.38	0.1087
200 °C	15.1	1.661	1.26	0.1959
300 °C	15.5	1.629	1.29	0.1893

Table 7. *Physical properties of PE-ALD Al_2O_3 films*

150 °C deposition was the only one that produced usable TFTs due to the spin-coating failure with other deposition temperatures.

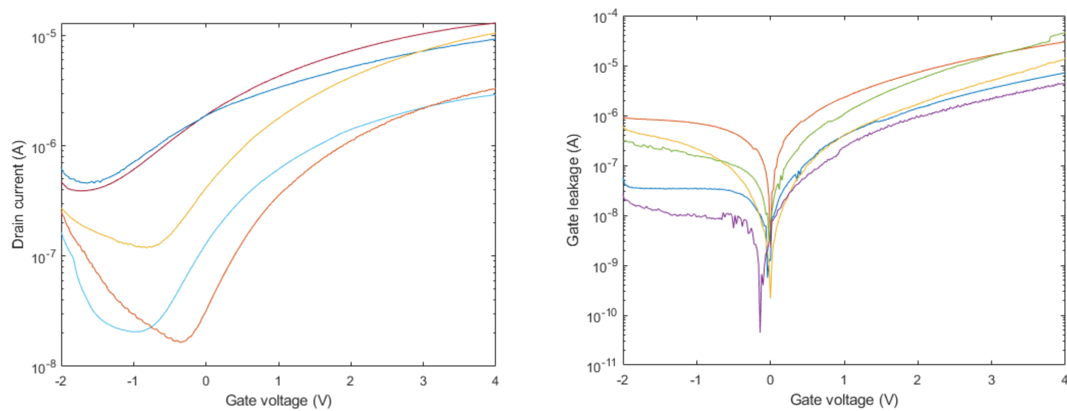

Figure 23. *Id-Vg and gate leakage plots of TFTs with 150 °C PE-ALD Al_2O_3 dielectric*

Deposition temperature	Subthreshold swing (mV/dec)	Threshold voltage (V)	On/off ratio	Mobility ($cm^2 V^{-1}s^{-1}$)
150 °C	1920 ± 1020	-0.67 ± 0.23	~100	~1

Table 8. *Electrical properties of 150 °C PE-ALD Al_2O_3 TFT*

Table 8 and Figure 23 contain electrical properties of the TFT with 150C PE-ALD Al_2O_3, most significant change compared to T-ALD Al_2O_3 is seen in the negative threshold voltage. While TFT fabrication failed with Al_2O_3 deposition temperatures other than 150 °C, MOSCAPs were successfully manufactured, interface trap density and flatband voltage was extracted by C-V measurements.

	-1V ($1/cm^2$)	0V ($1/cm^2$)	1V ($1/cm^2$)
150 °C #1	$1.49 \cdot 10^{12}$	$4.41 \cdot 10^{11}$	$1.89 \cdot 10^{12}$
150 °C #2	$9.47 \cdot 10^{11}$	$6.35 \cdot 10^{11}$	$1.7 \cdot 10^{12}$
200 °C #1	$1.55 \cdot 10^{12}$	$1.48 \cdot 10^{12}$	$1.58 \cdot 10^{12}$
300 °C #1	$3.36 \cdot 10^{12}$	$5.53 \cdot 10^{11}$	$1.02 \cdot 10^{12}$
300 °C #2	$4.27 \cdot 10^{12}$	$1.31 \cdot 10^{12}$	$4.39 \cdot 10^{12}$

Table 9. *Interface trap density of PE-ALD Al_2O_3 MOSCAPs*

	Flatband voltage (V)	Vfb hysteresis (V)
150 °C #1	-0.22	0.22
150 °C #2	-0.16	0.12
200 °C #1	-0.22	0.08
300 °C #1	0.22	0.02
300 °C #2	0.4	0.06

Table 10. *Flatband voltage + hysteresis in PE-ALD Al_2O_3 MOSCAPs*

In Tables 9 and 10, no significant trends appear in flatband voltage hysteresis nor in interface trap density between the deposition temperatures.

5.3 Pseudo-CVD Al_2O_3

In the first attempts at making PE-ALD Al_2O_3 films, the RF power generator for the plasma device was misconfigured, leading to constant RF power and hence constant plasma generation in the device. This left the ALD reactor operating in a mode where the oxidant is always present in the chamber during deposition, meaning there was no layered deposition.

Figure 24. *PECVD pulsing schematic*

During the TMA pulse the precursor started immediately reacting with the plasma which resulted in a quite high growth per “cycle” and very uneven film growth. The film growth near the gas inlet was almost twice that of the growth near the gas exhaust as the TMA was being immediately consumed instead of evenly coating the substrate. Despite this, a working device was eventually fabricated with this setup. The error went unnoticed for a while which led to RF “pulse” length and RF power testing in order to optimize the films. As seen in Figure 24, there is no real RF pulsing, and the increased pulse length instead acts as an increased interval between the TMA pulses, e.g., 5 s pulse vs. 7 s pulse has two additional seconds between the TMA pulses. This mode of operation is referred to in this thesis as “plasma-enhanced chemical vapor deposition” (PECVD), but it must be emphasized that this is not proper use of this reactor.

The initial testing was done with a short 5 s pulse and 70 W power at 150 °C deposition temperature, and the device had no gate modulation and relatively low resistivity between the source and drain electrodes leading to suspicion of high carrier concentration in the film, possibly caused oxygen vacancies at the dielectric-semiconductor interface.

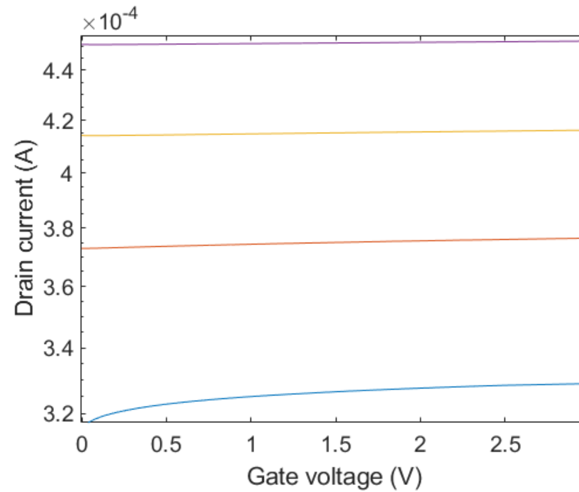

Figure 25. *I_d-V_g characteristics of a device with PECVD Al_2O_3 film deposited with 70 W, 5 s RF pulse. Drain voltage swept from 0.5 V – 2 V*

Figure 25 shows the I_d-V_g characteristics of a device which has seemingly no gate modulation, and thus not a transistor. The semiconductor just acts as a resistive film between the electrodes. Highest film density at 100 °C deposition temperature with similar equipment had been reported to be had at 100 W power and 7 s pulse length [32], so an experiment was carried out where the pulse length and power were changed independently and then together with 150 °C chamber temperature.

Pulse length and power	**Thickness (nm)**	**Refractive index**	**Growth per cycle (Å/cyc)**
5 s 70 W	12.23	1.69	0.687
7 s 70 W	33.87	1.61	1.902
5 s 100 W	39.2	1.62	2.202
7 s 100 W	37.3	1.61	2.094
5 s 150 W	14.26*	1.61	2.852
9 s 70 W	9.1*	1.71	1.816

Table 11. *Growth properties of PECVD Al_2O_3 on silicon with different plasma parameters, (*)5 s 150 W and 9 s 70 W 50 cycles, others 178 cycles*

Table 11 shows the growth per cycle of the Al_2O_3 film with different plasma parameters, the increasing growth per cycle was taken as an indication that the original film's oxygen ratio was substoichiometric, which might affect the TFT qualities, and device performance did improve with higher pulse length and power.

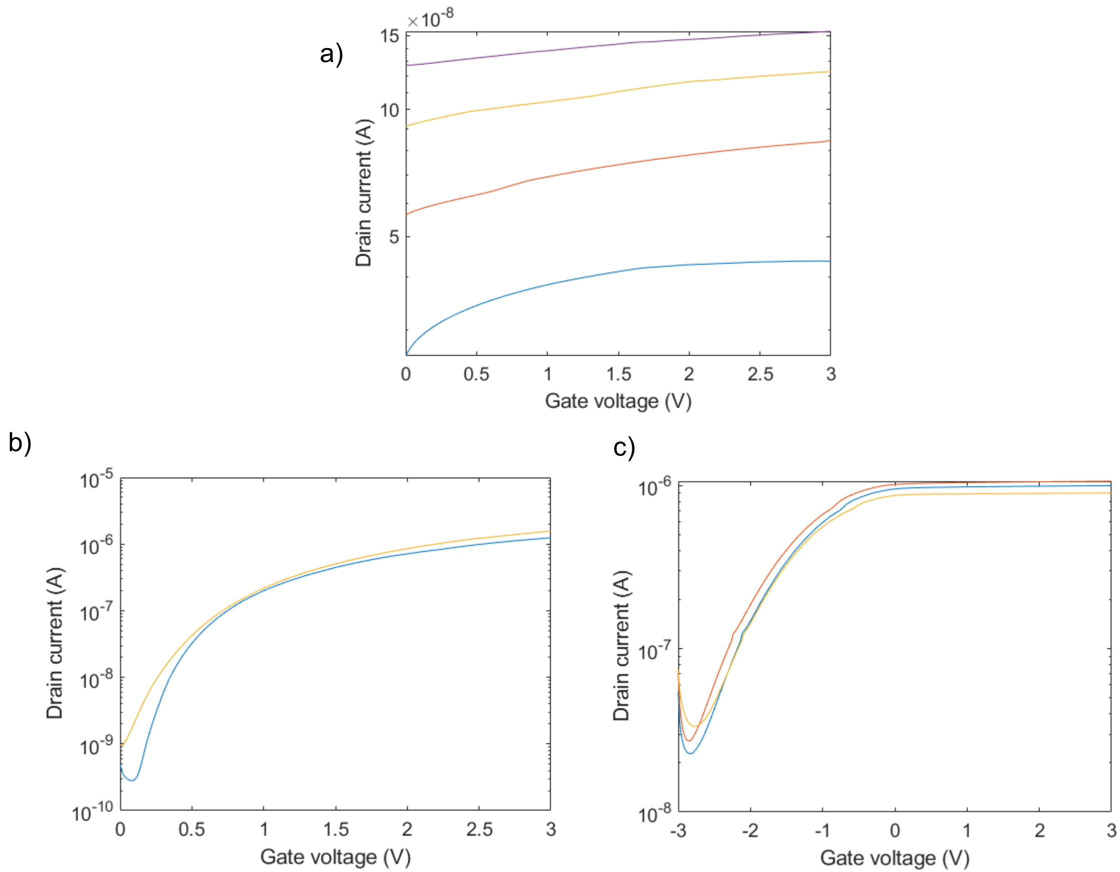

Figure 26. *I_d-V_g characteristics of PECVD Al_2O_3 devices, a) 7 s 70 W, V_d swept 0.5 – 2 V, b) 5 s 100 W two devices, c) 7 s 100 W three devices*

Figure 26 a) with 7 s 70 W pulsing has minimal transconductance and does not turn off much like devices 5 s 70 W pulse, but the drain current is reduced by some orders of magnitude, suggesting reduced carrier concentration. Increasing the power to 100 W provided significant improvement with both 5 s and 7 s pulse timing, with clear on- and off-states in both types of devices.

	Subthreshold swing (mV/dec)	**Threshold voltage (V)**	**On/off ratio**	**Mobility (cm^2 $V^{-1}s^{-1}$)**
5 s 100 W	285±67	-0.07±0.13	~1e3	~1
7 s 100 W	1140±100	-3.15±0.07	~1e2	~1

Table 12. *Electrical properties of PECVD TFTs*

A significant negative shift in threshold voltage is seen with the increased pulse length.

5.4 Thermal-ALD HfO_2

Performance wise, hafnium oxide should make a better gate dielectric than aluminum oxide owing to its higher dielectric constant, but the much lower bandgap is problematic. The ALD manufacturer does not directly support the use of TDMAH precursor in their

machine, and thus the recipe used has presumably not been optimized by the manufacturer.

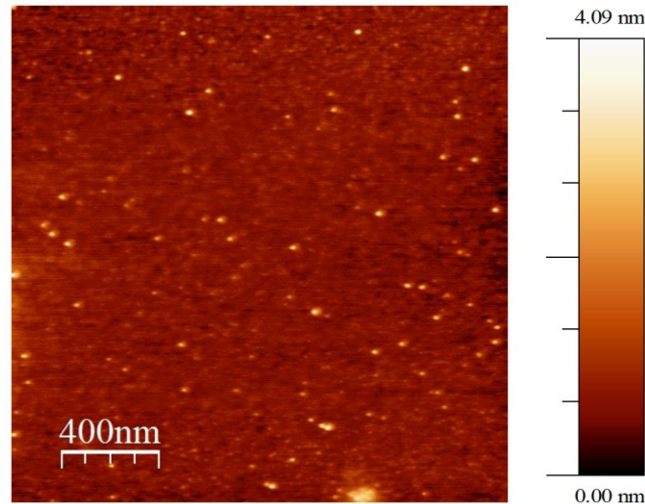

Figure 27. *AFM image of T-ALD HfO_2 layer deposited at 200 °C*

Deposition temperature	Thickness (nm)	Refractive index	Growth per cycle (Å/cyc)	RMS roughness (nm)
200 °C	10.9	2.01	1.36	0.2136

Table 13. *Growth properties of HfO_2*

The AFM image in Fig. 27 contains multiple high spots, which may be due to artefacting or an actual surface feature. The roughness of the surface is not significantly higher than with Al_2O_3 processes.

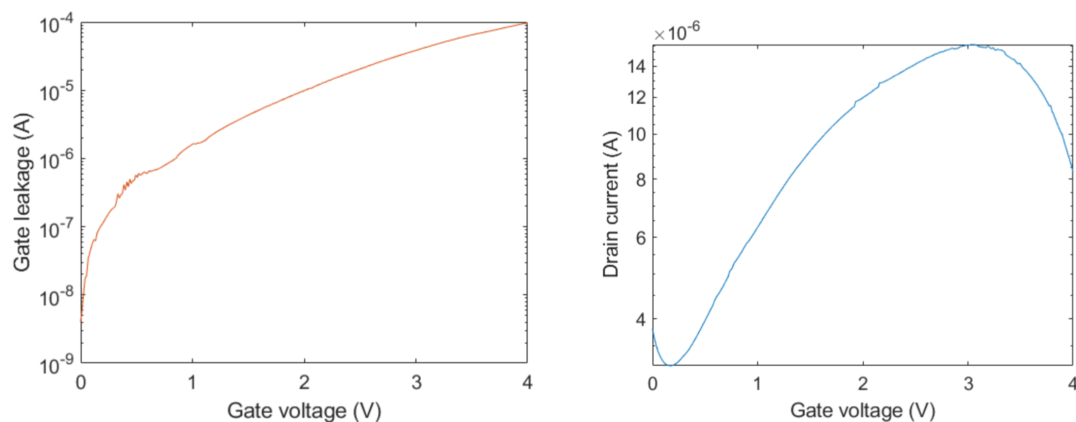

Figure 28. *I_d-V_g and gate leakage plots of TFT with HfO_2 dielectric*

TFTs produced with 10nm nominal HfO_2 gate dielectric did not function immediately, but after a post-electrode deposition annealing at 150 °C for 30 minutes they started performing as transistors. While the saturation current is quite high in Fig. 28, the on-off ratio is very low and gate leakage is very high.

Deposition temperature	Subthreshold swing (mV/dec)	Threshold voltage (V)	On/off ratio	Mobility ($cm^2 V^{-1}s^{-1}$)
200 °C	4219	0.28	~10	10^{-2}

Table 14. *Electrical properties of HfO_2 TFT*

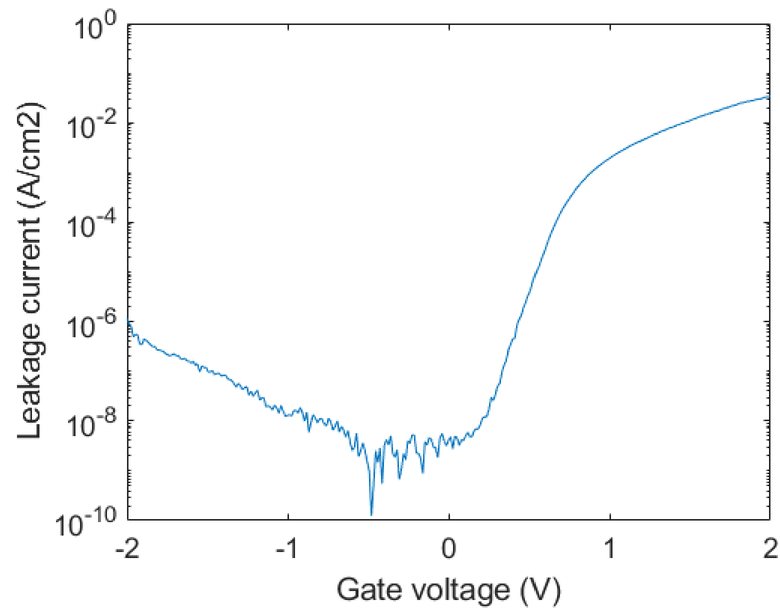

Figure 29. *Leakage current density in 10 nm HfO_2 MOSCAP*

As seen in Figure 29, the MOSCAP structure seems to rectify the current instead of having symmetrical leakage. The leakage current density is very high in forward bias which is problematic for transistor use.

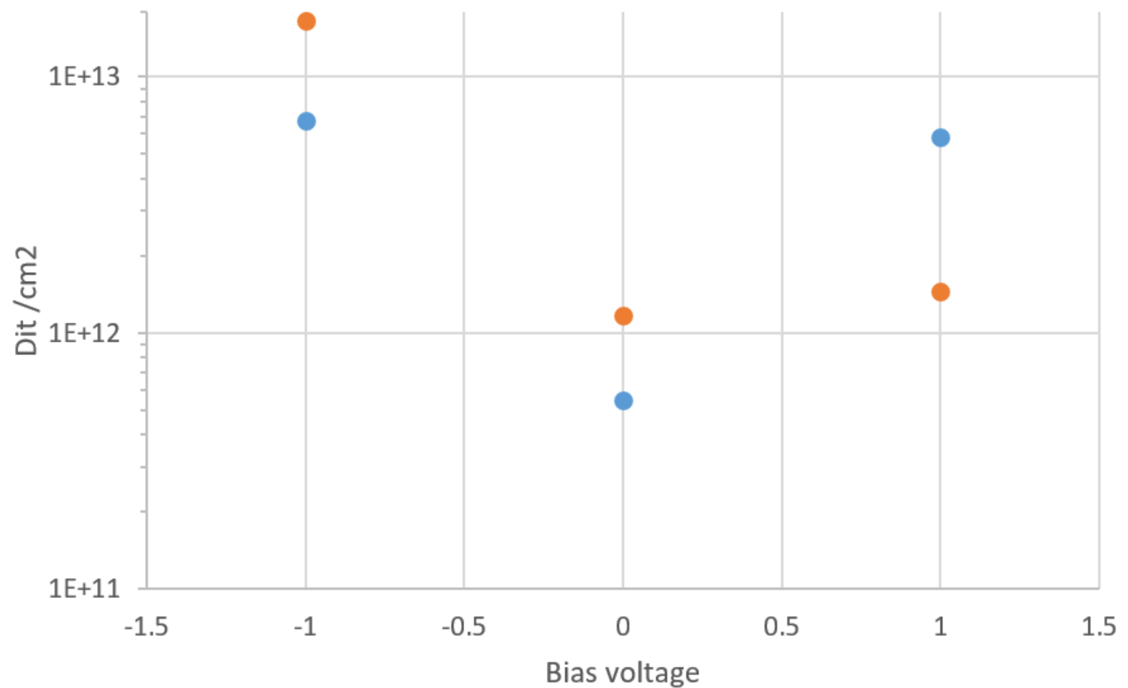

Figure 30. *Interface trap density in two HfO_2 MOSCAPs*

	Flatband voltage (V)	Vfb hysteresis (V)
#1	0.24	0.10
#2	0.34	0.14

Table 15. *Flatband voltage in HfO_2 MOSCAPs*

Interface trap density as plotted in Figure 30 is slightly higher than in Al_2O_3 capacitors.

5.5 Contact resistance

To evaluate the quality of the electrodes a contact resistance structure was fabricated by back evaporating aluminum to a silicon wafer followed by MOSCAP mask aluminum electrode evaporation on top, without any prior dielectric deposition. I-V plots of these devices should be linear with V/I slope being the total resistance, with the procedure described in Section 4.6 applied to find out the contact resistivity.

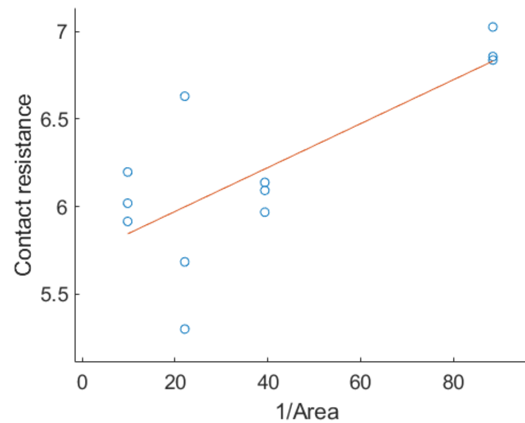

Figure 31. *Highly-doped silicon contact resistance plot*

Figure 31 shows the contact resistance plot for highly doped silicon with a fitted line with slope 0.0125 $\Omega \cdot cm^2$. This indicates acceptable electrode quality for highly doped silicon, but the precision of the value is dubious seeing the high spread in the measurements, and Schroeder mentions that this entire method is questionable [4].

The same procedure was not performed on medium-doped silicon, as the contacts turned out to be rectifying.

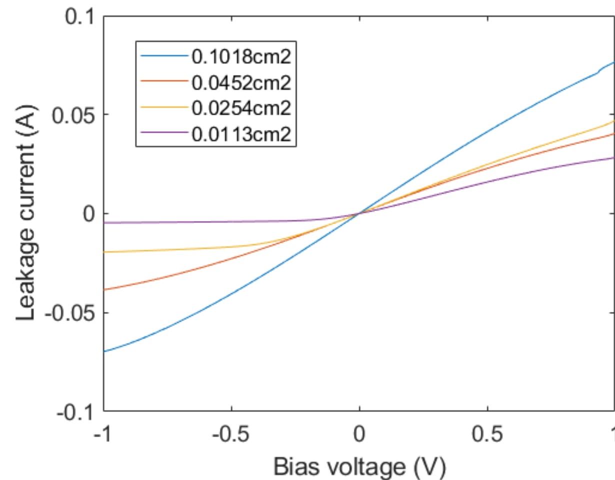

Figure 32. *I-V plot of contact resistance structure on medium-doped Si*

With the four different sized electrodes used, rectifying behavior was measured in two of the smallest electrodes as seen in Figure 32. This was unexpected as the structure is symmetric with Al-Si-Al cross-section.

5.6 Fabrication error analysis

Sample fabrication consists of cleaning the substrate, depositing the dielectric by ALD, depositing indium oxide by spin-coating and depositing electrodes by evaporation. Each of these steps is liable to introduce variation into the final devices, and some qualitative analysis is performed in this section.

Solvent cleaning glass substrates is straightforward and an unlikely source of errors, barring any mishandling of the samples by e.g., getting fingerprints on them after cleaning. Likewise, RCA cleaning of silicon wafers should have a consistent result and the manufacturing tolerances should not be a concern either. The thickness and resistivity of the wafers has an effect on the contact resistance calculation but owing to the general inaccuracy of the method used, higher tolerances would be unlikely to grant more accurate results. The ALD reactor used should create highly uniform films, and nothing to the contrary was observed. Layer thickness slightly varies between depositions done with the same number of cycles but with different temperatures, which reduces the direct comparability between samples.

Spin-coating and electrode deposition on the other hand had visible flaws. The indium oxide spin-coating leaves a visible layer on the substrate and voids in the coating are visible in a microscope. The film thickness was not measured, and the uniformity is uncertain, the process should produce a uniform film, however. Electrode deposition

through evaporation introduces errors in the form of shadowing and roughness. Shadowing is caused by the mask itself. As the mask has some thickness, the edges of the mask will block line-of-sight from the evaporation source to the target when the two are not perpendicular to each other. The mask may also be slightly lifted from the target causing deposition under the mask in areas that have line-of-sight. This manifests in MOSCAPs as electrodes that are out of round with a smaller or greater area than the nominal mask dimension.

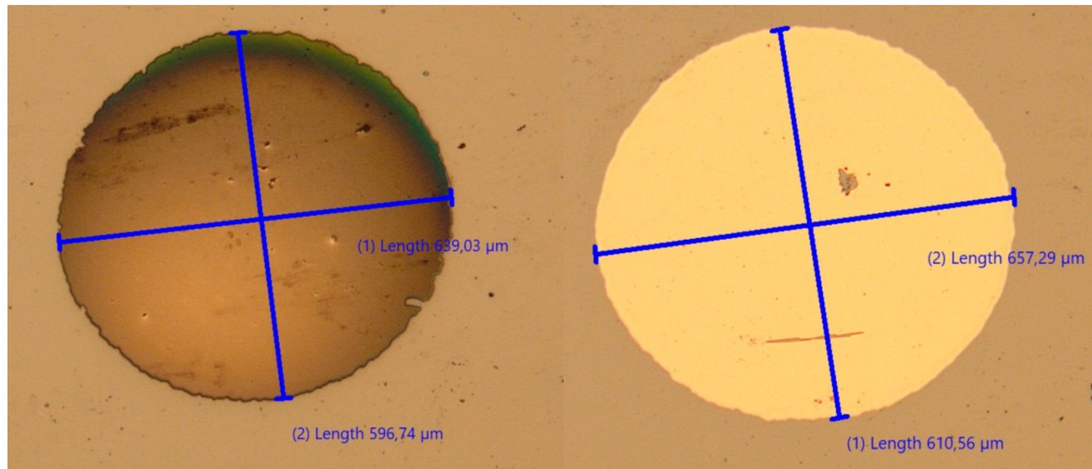

Figure 33. *Microscope picture of MOSCAP aluminum electrodes with 0.0113 cm² nominal area*

Figure 33 shows two electrodes with nominal area 0.0113 cm², however approximating them as ellipses gives them areas of 0.0120 cm² and 0.0126 cm², meaning 6% and 10% difference from nominal. This error propagates linearly to methods involving the electrode area.

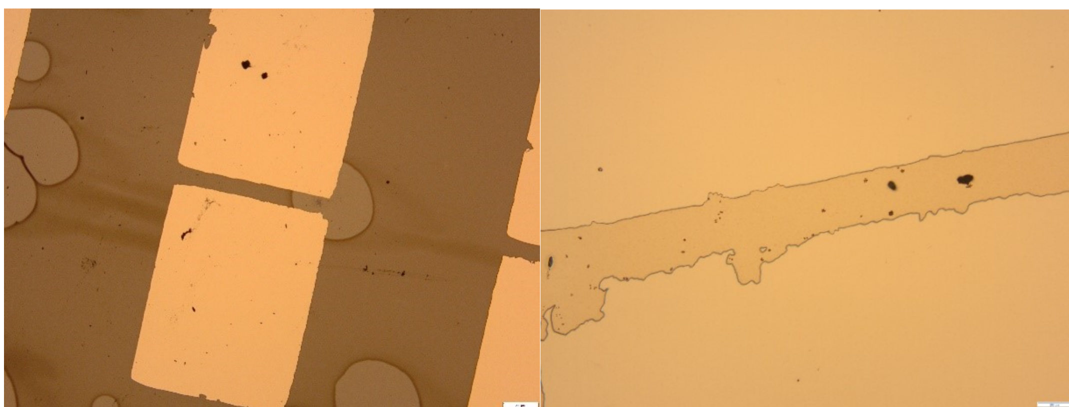

Figure 34. *Microscope pictures of a void in indium oxide layer in the transistor channel, electrode roughness in the channel. Scale bars 200 µm and 50 µm*

Roughness on the transistor channel as in Fig. 34 causes a slightly variable channel length along the width of the channel, and shadowing may cause the channel length to vary from the nominal 70 µm. While undesirable, linear error propagation from these

faults would not be enough to explain the at worst order-of-magnitude differences in some of the devices demonstrated. Excessively rough electrodes and large voids in the indium oxide layer left by the spin-coating process were visible through the microscope in the probe station, and these faulty looking devices were ignored.

6. DISCUSSION AND SIMULATIONS

Leakage currents for 10 nm thick dielectrics were excessive with both Al_2O_3 and HfO_2. All of the depositions were very smooth, with RMS roughness below 0.2 nm in each case. With thermal-ALD Al_2O_3, a plateau in growth per cycle is reached quickly, as 200 °C deposition temperature provided the highest value. The increased temperature of the deposition only seemed to have an effect on the subthreshold swing in TFTs, but in MOSCAPs a change is seen in current under reverse bias, which is significantly reduced in 300 °C deposition.

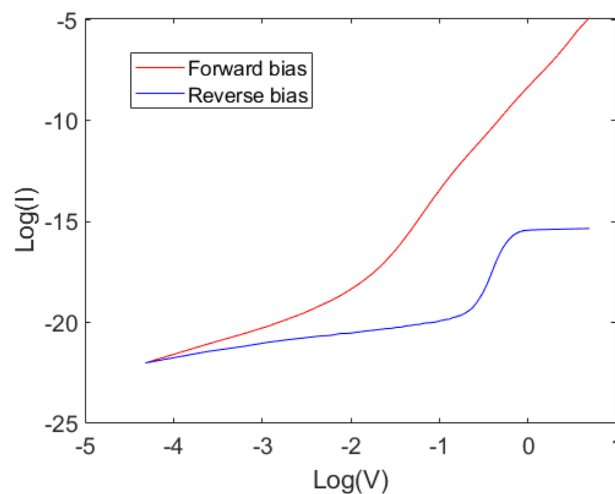

Figure 35. *10 nm 300 °C Al_2O_3 MOSCAP I-V log-log plot*

A log-log plot of the I-V measurements in Fig. 35, as demonstrated in Ref. [9], reveals space-charge limited current in reverse bias in 300 °C 10 nm Al_2O_3 MOSCAPs explaining the rectification, the step in the graph is due to the device reaching the traps-filled limit [9]. An attempt was made at interpreting the current under forward bias, but no conclusive results were obtained. Such a clear plot was not obtained with other devices, leaving the conduction mechanisms ambiguous. Some rectification is visible in HfO_2 and PE-ALD gate leakage, but not to the extent as in the 300 °C 10 nm Al_2O_3 MOSCAP.

Increasing In_2O_3 film thickness by decreasing the RPM improved on/off ratio by an order of magnitude but mobility was reduced. The experiment with the different RPMs was carried out due to concerns that the aluminum may spike through the thin semiconductor layer, and aluminum does create oxygen vacancies, which would increase the number of free carriers in the film.

An interesting result is seen in the threshold voltage shift between T-ALD Al_2O_3 and PE-ALD and PECVD Al_2O_3. Plasma enhanced deposition resulted in a noticeably negative shift, and in PECVD RF parameter testing the semiconducting layer was initially just a resistive film, but with increased power and pulse length the devices started performing like transistors, and with a further increase the threshold voltage shifted further into the negative. This suggests that the dielectric deposition method heavily effects the dielectric-semiconductor interface, with heavy consequences to the device behavior.

A device simulation of the 20 nm T-ALD Al_2O_3 TFT was attempted, and a basic model was produced.

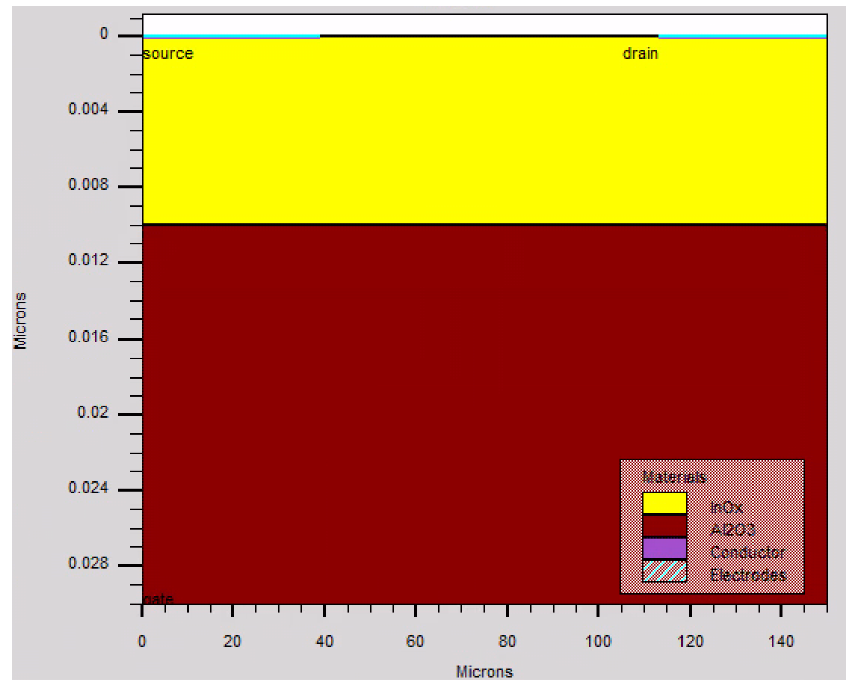

Figure 36. *Cross-section of TFT simulation model*

A 2D model with the cross-section shown in Figure 36 was used. IGZO was used as a stand-in material for In_2O_3 which is not available in the materials library. The density of states was extracted with a method introduced by Chen *et al* [39]. Only the donor tail-states were used, with NTD = 1.126×10^{19} and WTD = 5.

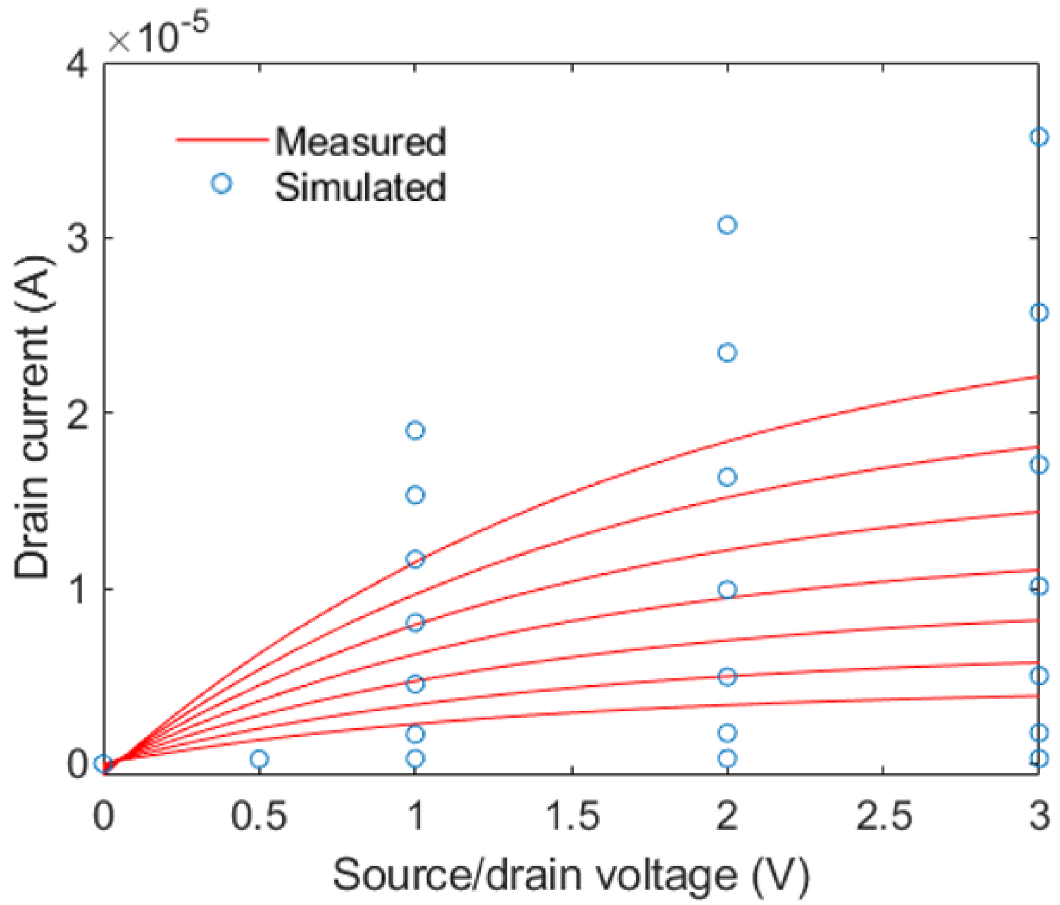

Figure 37. *Measured and simulated I_d-V_g plot of 20 nm Al_2O_3 device, gate voltage swept 0-3 V in 0.5 V increments*

The simulation does not match the real device due to a number of reasons. Certain simplifications were made in the density-of-states extraction, and some material properties are incorrect. Interface traps and gate leakage models were also not implemented. Despite these shortcomings, the model provides a basis for more sophisticated future simulations. An accurate device model would enable e.g., the creation of a SPICE model of the devices, allowing circuit simulation with the fabricated TFTs.

7. CONCLUSIONS

Low temperature atomic layer deposition is suitable for gate dielectric deposition, but the deposition parameters must be carefully considered. Establishing the best deposition temperature or optimal thickness with the dataset in this thesis is not feasible, but as a generality the 10 nm films had unacceptably high leakage, which is somewhat improved by thicker films. High off-state current is a very persistent issue, which might be attributed to oxygen vacancies in the semiconductor or at the semiconductor-dielectric interface. Improving the films without high temperature annealing would be ideal, and some possibilities are in UV ozone treatment, photonic annealing, and in *in situ* ALD plasma treatment.

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