The Digital Signal Processing Platform for the Low Frequency Aperture Array: Preliminary Results on the Data Acquisition Unit

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A signal processing hardware platform has been developed for the Low Frequency Aperture Array component of the Square Kilometre Array. The processing board, called an Analog Digital Unit (ADU), is able to acquire and digitize broadband (up to 500MHz bandwidth) radio-frequency streams from 16 dual polarized antennas, channel the data streams and then combine them flexibly as part of a larger beamforming system. It is envisaged that there will be more than eight thousand of these signal processing platforms in the first phase of the Square Kilometre Array, so particular attention has been devoted to ensuring the design is low-cost and low-power. This paper describes the main features of the data acquisition unit of such a platform and presents preliminary results characterising its performance.

Keywords: SKA, FPGA-based System, Digital Receiver, Data Acquisition.

1. Introduction

The Square Kilometre Array (SKA) will be the largest and most sensitive radio telescope ever built (Dewdney *et al.*, 2009). It will be constructed in two phases (SKA1 and SKA2), over two sites, South Africa and Western Australia, and at the end of the second phase, it will provide about a million square meters of collecting area through many thousands of connected radio telescopes. An update of the Baseline Design document issued in 2013 for the first phase is provided in (Dewdney, 2015).

The first phase of the Low Frequency Aperture Array (LFAA) component of the Square Kilometre Array (SKA) will consist of 2^{17} log-periodic dipole antennas (Faulkner & Bij de Vaate, 2013). The current architecture, shown in Fig. 1, features the transport of the Radio-Frequency (RF) bandwidth of 300 MHz over fiber to a Central Processing Facility (CPF). Once inside the building these antenna signals are digitized, channelized and beamformed together to form logical stations which are an aggregation of 256 antennas. The LFAA is currently designed to produce 512 of these logical stations which can be flexibly configured by programming the signal processing platform to send its traffic across a highly configurable network.

The antennas are grouped in tiles of 16 antennas each. Each tile is processed in a Tile Processing Module (TPM), and 16 TPMs are connected together in a flexible way to form a station, using a general purpose high speed Ethernet interconnect. Development proposals for the LFAA were initially discussed and an architecture for the TPM was sketched together with the main design choices adopted (Faulkner & Bij de Vaate, 2013).

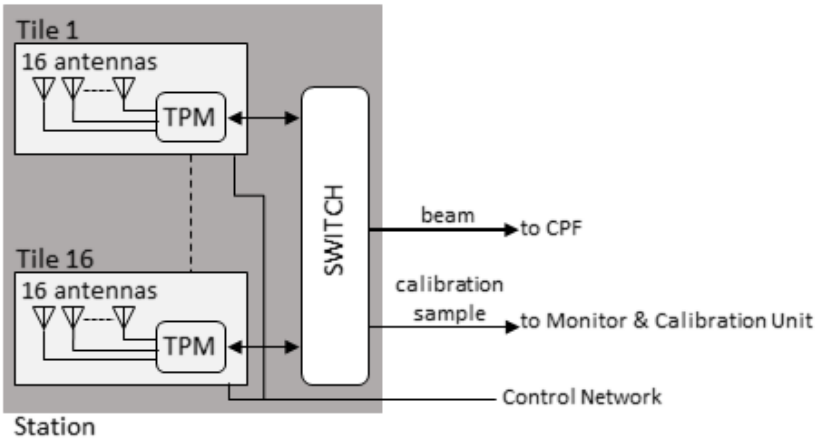

Fig. 1 The proposed layout for SKA1-low. 16 antennas form a tile, and 16 tiles form a station producing a station beam for the Central Signal Processor.

The present paper concerns a step forward with respect the ideas presented in that paper and describes the main characteristics of a novel digital hardware platform for the TPM, able to digitize and process signals from 16 dual polarized antennas of an LFAA station.

The TPM consists of two units. The first, called Analog Digital Unit (ADU) includes an analog part, performing high frequency acquisition and conversion of the antennas' RF signals, and a digital part, accomplishing high performance filtering and pre-processing of the acquired data. The second unit, called Pre-ADU board, performs optical-electrical conversion, filtering, amplification and equalization of analog signals. A Pre-ADU board manages 8 analog signals. A TPM is, thus, an assembly of one ADU and two Pre-ADU boards. A picture of the TPM assembly is shown in Fig. 2.

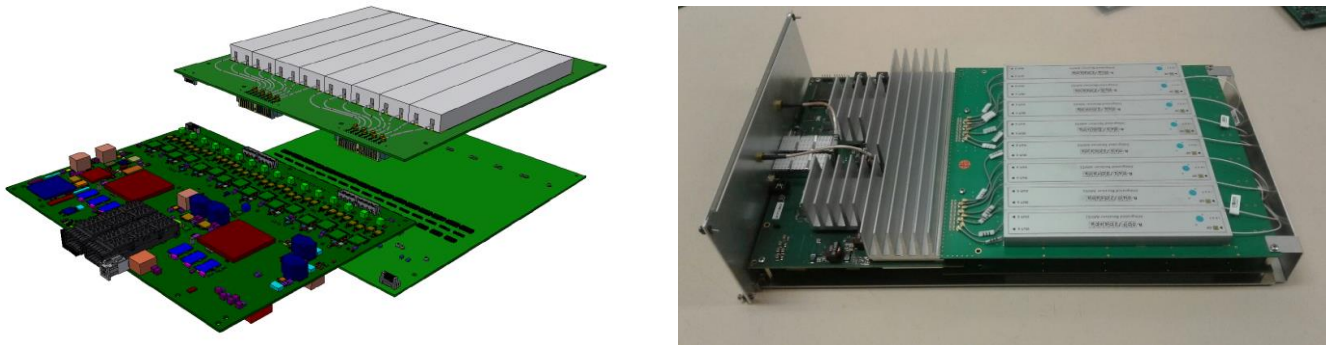

Fig. 2. TPM assembly showing two Pre-ADU(s) and one ADU: the exploded view drawing obtained from 3D CAD (left) and a picture of the realized hardware (right).

The ADU project has been developed within the context of the activities of the Aperture Array Design and Construction Consortium (AADC) of the SKA LFAA. The project is led by the University of Oxford in collaboration with the Italian Institute of Astrophysics (INAF), Sanitas EG, Malta University and Science and Technology Facility Council (STFC). The project started in 2013 and various prototypes have been realized since then. The first release of the complete design and assembly of ADU and Pre-ADU boards will be used for the

Aperture Array Verification System (AAVS) demonstrator, which will include the deployment of 400 antennas at the Murchison Radio-astronomy Observatory in 2017.

The details of the firmware implementing the signal processing algorithms for the ADU board are illustrated in (Comoretto *et al.*, 2017), while this paper describes the main features of the ADU board and presents a few preliminary results concerning the characterization and performance evaluation of its data acquisition unit.

The main features of the ADU and Pre-ADU boards are illustrated in Section 2 and Section 3, respectively. The performance parameters and the hardware test setup for the performance valuation of the data acquisition unit are described in Section 4, while the software programs are presented in Section 5. Results are discussed in Section 6. Conclusions are drawn in Section 7.

2. ADU Board Architecture

2.1. *Overview*

The scientific challenges that SKA has to face are mainly due to the number of telescopes to be managed in remote locations with limited power available. Indeed, the LFAA antennas that will be installed in South Africa and Australia at the end of the construction of the first phase will be about 131,000, spread on a wide desert land. On-line processing of large amounts of data, as well as their storage and distribution in locations with limited resources constitute the major challenge.

The main functions of the board are as follow:

- To acquire 32 analog inputs (16 antennas in double polarization), 50–350 MHz low frequency range.
- To convert optical signal to electrical signals, with conversion sampling up to 1 Gsample/s.
- To process massive amounts of digital data.
- To possibly transfer data internally, whenever required by the algorithm, through a high speed bus for high performance data processing, 400 MHz.
- To communicate output data on high speed digital channels (80 Gbit/s).

The board (Fig. 3) is a modular element of a system and is envisaged there will be more than eight thousand of these signal processing platforms in the first phase of the Square Kilometre Array. So power consumption and cost become fundamental elements of the design.

Fig. 3. Analog Digital Unit (ADU) Board includes an analog part, performing high frequency acquisition and conversion of the antennas' RF signals, and a digital part, accomplishing high performance filtering and pre-processing of the acquired data.

When the ADU project started in 2013, no commercial solutions able to satisfy the processing requirements for the SKA LFAA antennas were available on the market. Existing hardware platforms, for instance the well-known Uniboard architecture (Szomoru *et al*., 2011), turned out not to be suitable to the purpose. Indeed, the Uniboard did not have the required interfaces and was conceived to provide much more functionalities than those effectively requested by LFAA. Similarly, no hardware from the CASPER collaboration was suitable (Hickish *et al*., 2016).

The ADU is the main hardware component of the TPM signal processing platform. Its development moved from the design outlined in Faulkner & Bij de Vaate (2013). It is a 6U board containing sixteen dual-inputs Analog to Digital Converters (ADC) and two Field Programmable Gate Array (FPGA) devices, capable of digitizing 32 RF-paths and processing digitized input signals respectively. In particular, the following devices have been selected: Xilinx Kintex UltraScale XCKU040 for the FPGA (Xilinx, 2015), and AD9680 for the ADC (Analog Devices Inc., 2014a). Device choice has been driven by multiple factors. For FPGAs, they have been the following:

- Access to the latest, not yet available on the market, high performance and low power devices.
- Resource occupancy of the beamforming algorithms; preliminary evaluations of the firmware implementation (Comoretto *et. al*, 2017) were accomplished as to choose the most suitable among available device sizes.
- Availability of high-speed transceivers to interface eight antennas for each device.
- Layout optimization. Placing two identical devices allows for an optimal and balanced clock routing from the center of the board.

Similarly, for ADCs the choice has been mainly due to the following:

- Sampling rate up to 1 GSPS of dual inputs.
- 2 GHz usable analog input full power bandwidth.
- High speed serial interface supporting JESD204B (JEDEC, 2011) data transmission protocol.
- Access to the latest devices.
- Roadmap to the development of low power devices.

The ADU board functional diagram is shown in Fig. 4.

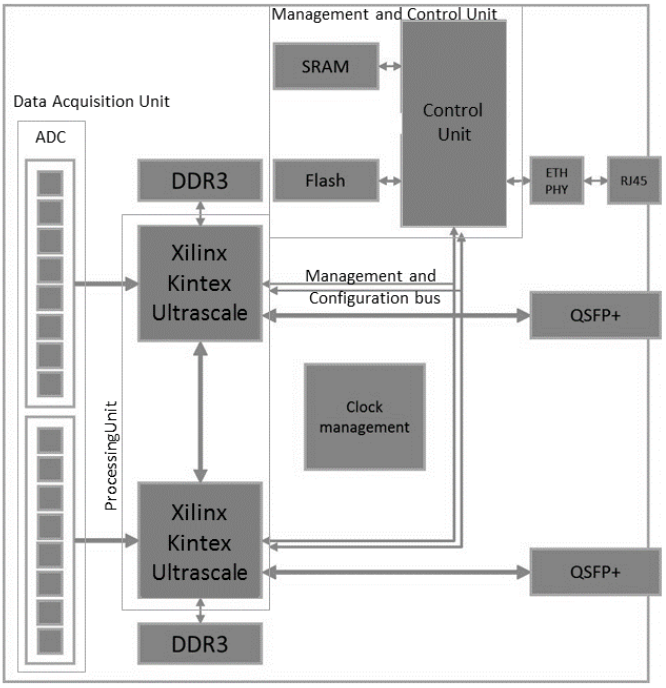

Fig. 4. ADU Board Functional Block Diagram.

For each channel a configurable RF-network including an Analog Devices ADA4961 low distortion amplifier (Analog Devices Inc., 2014b) provides filtering and conditioning of signals before Analog-to-Digital conversion.

Each ADC digitizes two RF signals and transmits the encoded digital data streams to two Xilinx Kintex UltraScale XCKU040 FPGAs (Xilinx, 2015) over two JESD204B data lanes.

Each FPGA handles 16 JESD204B lanes corresponding to 16 RF inputs. Each FPGA implements a 96-bit wide Double Data Rate type 3 (DDR3) interface that manages up to 6 DDR3 memory chips for a total capacity of 1 GByte of memory per each FPGA. Such a memory is used to store partial beams used by the beamforming algorithm as explained in Comoretto *et al*. (2017). A Quad Small Form-factor Pluggable (QSFP+) is connected to each FPGA enabling transmission of processed data over two 40 GbE link.

The management and control of the board is performed by a functional block, that also includes a Gigabit Ethernet link with RJ45 interface for transmission and reception of monitor and control data packets.

2.2. *Data Acquisition Unit*

In the ADU the 32 analog input signals coming from the Pre-ADU boards are converted from single ended to differential signals by baluns, then amplified by programmable Digital Gain Amplifier (DGA) chips and finally digitized by 14 bit dual-input ADCs, that send the eight most significant bits to the FPGAs via high speed links for processing. The reason for the selection of an ADC with such characteristics derives from Faulkner & Bij de Vaate (2013) and Comoretto (2016). In this case we can reach the target 7.5 ENOB with 8-bit samples into FPGA.

For the ADU release 1.0 prototype, two slightly different boards have been manufactured by using the same PCB, corresponding to either a passive or active circuit with the Analog Devices ADA4961 (DGA) chip before each ADC. This allows the amplifiers to be bypassed through a matching network.

The paper illustrates in Section 4 the results of a preliminary evaluation of the resulting performances of these two prototypal boards. The ADU integrates in a small sized 6U board a lot of electronics (> 4,000 devices), including 32 ADCs for a wide analog input data band (up to 500 MHz). The objective of this test is not the analysis of the goodness and quality of the selected ADC, which has been already accomplished by the manufacturer. Instead, the test aims at analyzing that the ADU behavior does not get compromised by the presence of 32 ADCs close to each other (e.g. "cross-talk" effect) and no performance degradation is observed. Also, we wanted to evaluate potential undesired effects (e.g. undesirable signals like spurs) generated by the proximity of PCB traces on a high density board, the proximity of clock signals and the presence of unshielded windings of wire coils of baluns.

Another goal of the preliminary tests described in this paper is the comparison of performances obtained with the two versions of ADU rel. 1.0. In fact, by having two prototypes, we were able to verify experimentally the best placement of the last gain stage.

2.2.1. *ADU 1.0 prototype: "ADA" vs. "no ADA" version*

The analog to digital conversion chain was developed in collaboration with Analog Devices Inc. A dual solution using ADC chip technologies ahead of commercial introduction (end of 2014) was evaluated: a passive matching network (without power amplifier before ADC) and an active matching network (with power amplifier before ADC).

The acronym ADA will be used in the paper to identify the Analog Devices ADA4961, which is a high performance BiCMOS RF DGA. The ADA has a very low Third Order Intermodulation and Harmonic Distortion products (IMD3 and HD3, respectively), which allows converters to achieve their optimum performance with minimal limitations of the driver amplifier. It is optimized for wideband, low distortion performance up to 2 GHz. It has a gain step size of 1 dB with maximum power gain of 18 dB (15 dB of voltage gain) programmable via the SPI bus.

2.2.2. *ADC*

The ADU board hosts 16 Analog Devices AD9680 Dual Input, 14 bits, 1GSPS, JESD204B ADCs. The device has an on-chip buffer and sample-and-hold circuit designed for low power, small size, and ease of use. The AD9680 is optimized for wide input bandwidth, high sampling rate, excellent linearity, and low power consumption in a small

package. The manufacturer's basic specifications for both AD9680 and ADA4961 are shown in Table 1 and Table 2 respectively.

The AD9680 supports JESD204B Subclass 0 and Subclass 1 operation modes. The ADU board implements the required hardware for SYSREF management, thus it supports the deterministic latency feature, as expected in JESD204B Subclass 1 operation mode.

The AD9680 supports up to 4 JESD204B lanes. When all 4 lanes are operating, it is possible to transfer a maximum of 4*10 Gbit/s of 8B10B encoded data. Since only two JESD204B lanes for each ADC are connected to the FPGA, the maximum data rate supported by the ADU is 20 Gbit/s per ADC; this allows the ADCs to work in dual channel mode, 8 bits per sample up to 1 GSPS.

The AD9680 supports an SPI configuration port that is controlled by the Management and Control Unit. The SPI port is used to control and monitor the ADC. The AD9680 also supports two Fast Detect signals that work as amplitude threshold detectors. These are connected directly to the FPGAs and provide fast feedback into the FPGA fabric.

Table 1. AD9680 Basic Specifications

Pin compatible family supporting sample rates up to 1.25 GSPS
JESD204B (Subclass 1) coded serial digital outputs
1.65 W total power per channel at 1 GSPS (default settings)
SFDR = 85 dBFS at 340 MHz, 80 dBFS at 1 GHz
SNR = 65.3 dBFS at 340 MHz (A_{IN} = −1.0 dBFS), 60.5 dBFS at 1 GHz (A_{IN} = -1.0 dBFS)
ENOB = 10.8 bits at 10 MHz
DNL = ±0.5 LSB
INL = ±2.5 LSB
Noise density = −154 dBFS/Hz at 1 GSPS
1.25 V, 2.5 V, and 3.3 V dc supply operation
No missing codes
Internal ADC voltage reference
Flexible input range
• AD9680-1000 and AD9680-820: 1.46 V p-p to 1.94 V p-p (1.70 V p-p nominal)
• AD9680-500: 1.46 V p-p to 2.06 V p-p (2.06 V p-p nominal)
Programmable termination impedance
• 400 Ω, 200 Ω, 100 Ω, and 50 Ω differential
2 GHz usable analog input full power bandwidth
95 dB channel isolation/crosstalk
Amplitude detect bits for efficient AGC implementation
2 integrated wideband digital processors per channel
• 12-bit NCO, up to 4 cascaded half-band filters
Differential clock input
Integer clock divide by 1, 2, 4, or 8
Flexible JESD204B lane configurations
Small signal dither

Table 2. ADA4961 Basic Specifications

High speed • −3 dB bandwidth: 3.2 GHz • −1 dB bandwidth: 1.8 GHz • Slew rate: 12,000 V/μs
Digitally adjustable gain • Voltage gain: −6 dB to +15 dB • Power gain: −3 dB to +18 dB • 5-bit parallel or SPI bus gain control with fast attack
Differential impedances: 100 Ω input, 50 Ω output
Low power mode operation, power-down control
• IMD3/HD3 (3rd-order Intermodulation/Harmonic) distortion, maximum gain, 5 V, high performance (HP) mode • IMD3/HD3 at 1 GHz: −90 dBc/−83 dBc • IMD3/HD3 at 1.5 GHz: −85 dBc/−75 dBc • IMD3/HD3 at 2 GHz: −70 dBc/−70 dBc
Low noise • Noise figure: 5.6 dB at AV = 15 dB
Single 3.3 V or 5 V supply operation
Available in 24-lead, 4 mm × 4 mm LFSCP

2.3. *Data Processing Unit*

The data processing unit consists of two Xilinx Kintex Ultrascale FPGAs and is responsible of performing polyphase filtering and beamforming of incoming signals (Comoretto *et al*, 2017). The ADU board hosts two Xilinx Kintex Ultrascale XCKU040-FFVA1156. Each FPGA provides the following interfaces:

- JESD204B interface for data reception from 8 ADCs (16 channels) using 16 high speed transceivers.
- DDR3 interface with 6 DDR3 memory chips supporting 1.5 GByte of memory and 96-bit wide memory bus. The maximum bitrate is 1600 Mbps.
- FPGA to FPGA fast link for transferring data from one FPGA to the other. It consists of 36 LVDS lanes supporting up to 1.6 Gbit/s per lane.
- 40 GbE QSFP+ using 4 high speed transceivers.
- Communication with the Management and Control Unit for monitor and control. This is a bidirectional parallel bus aimed to monitor and control the FPGAs. The bus is driven by the Management and Control Unit shared between the FPGAs.
- SelectMAP shared bus between the FPGAs, driven by the Management and Control Unit and used to upload the bitstream into the FPGAs.

2.4. *Management and Control Unit*

The ADU board implements a complex control plane performing the following functions:

- Board power on/off.
- 1 GbE interface for Monitor & Control communication over Ethernet.
- SPI programming of ADCs, PLL, Analog Amplifiers and Pre-ADU boards.
- System clock signals generation.
- Voltage and temperature monitoring.
- FPGA firmware storing.
- FPGA configuration, monitor and control.

The Management and Control Unit allows the remote control of on board functional units, including the one for firmware update.

2.5. *Power Supply*

The ADU board is powered by a single voltage in the range 12–32 V. It requires a specific power-up sequence to reduce in-rush current. The power system also provides power to the two Pre-ADU boards with a dedicated adjustable voltage of 3.5 V, maximum current of 4 A.

The power management system also allows the user to selectively switch on the main parts of the board (FPGA, data acquisition interface, Pre-ADU), to avoid an excessive in-rush current. It is also possible to monitor all the major internal voltages and the total current absorption of the board.

Table 3 shows the measured power consumption for the ADU board without ADA in various operating conditions up to the acquisition by the ADC. No beamforming firmware is considered in the measurement. This result complies with SKA LFAA requirement in Faulkner & Bij de Vaate (2013). In that paper, a preliminary power consumption estimate of 7 kW for a rack able to handle 1024 antennas is given. With respect to the current ADU design, 64 ADU board are necessary to manage that number of antennas. This results in an average power consumption of abut 110 W per ADU, greater than the value measured.

Table 3. Measured power consumption for the ADU board without ADA4961. Supply voltage is 24 V for all tests.

Measurements	Condition	POWER (W)
STATIC	all power supply on, all clocks stopped	39.6
ADC PLL	ADC and PLL configured and running @700 MHz, FPGAs not programmed	76.8
ADC PLL	ADC and PLL configured and running @800 MHz, FPGAs not programmed	79.8
ADC PLL FPGA	ADC and PLL configured and running @700 MHz, FPGAs acquire and transmit data	95.6
ADC PLL FPGA	ADC and PLL configured and running @800 MHz, FPGAs acquire and transmit data	99.7

2.6. *Clock and Synchronisation*

The ADU board accepts a 10 MHz reference clock through an MMCX (Micro-Miniature Coaxial) connector. This clock feeds an Analog Devices AD9528 JESD204B clock generator. The AD9528 component is specifically designed to meet JESD204B requirements and supports JESD204B Subclass 1 SYSREF signal generation. AD9528 integrates two PLLs and supports two clock inputs, selectable between a 10 MHz reference clock and a 10 MHz on-board oscillator. The selected clock input feeds the first PLL, which drives a 100 MHz VCXO, locking the VCXO frequency to the 10 MHz reference clock. It is then possible to synthesize a broad range of frequencies through a second PLL and an independent clock divider associated with each AD9528 output. The AD9528 supports the automatic switching of clock input sources and automatic failover. In the latter case the VCXO is free running.

The generated clocks and SYSREF signals are buffered by two Analog Devices ADCLK948 clock buffers and then distributed to the ADCs and FPGAs. The two FPGA-layout allows for an optimal routing of the clock lines, preventing additional noise in the analog part, caused by the digital hardware. The board hosts a 25 MHz oscillator connected to an Analog Devices AD9550 Integer-N clock translator. This is configured to generate two 156.25 MHz clock signals that are connected to the FPGA MGT reference clock inputs. Two 100 MHz oscillators, one per each FPGA, provide a suitable clock source for interfacing with DDR3 memories.

The ADU board supports one Pulse-Per-Second (PPS) input through a MMCX connector. The PPS input is first isolated through an optocoupler and then connected to both FPGAs.

2.7. *Implementation solutions*

In order to grant isolation between analog and digital domains that coexist in the board, we followed a twofold approach in the ADU design. Firstly, careful placement guarantees an effective separation of high efficiency DC-DC supply, digital electronics and the clock network from the analog acquisition interface. Secondly, a multilayer PCB has been implemented, in order to separate the input RF signals from supply/digital control interfaces. Ground planes and supply voltage planes have been placed in order to improve the separation and noise filtering.

3. Overview of the Pre-ADU Board

Pre-ADU board corresponds to the analog receiver in front of the ADU. Every Pre-ADU hosts 8 double channel analog receivers (i.e. 16 analog chains). The two chains in each double channel receiver correspond to the two antenna polarizations. Two Pre-ADU boards are needed to feed all the ADU inputs (16 antennas/32 polarizations=32 receiver chains) and to compose the so called TPM. The top view of the Pre-ADU board is visible in Fig. 5.

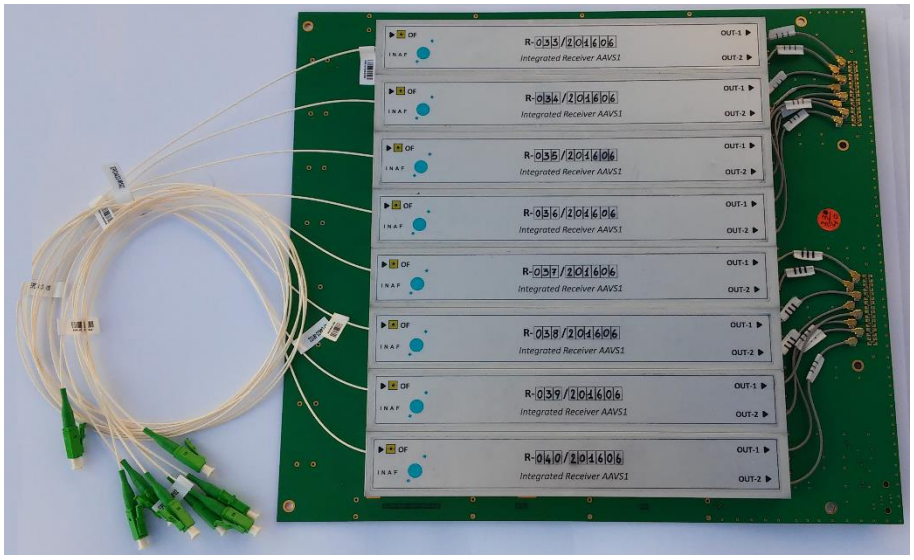

Fig. 5. Pre-ADU top view: 8 double channel analog receivers are hosted on the same board.

The first stage of any Pre-ADU channel is an optical receiver (ORX) which converts back to the RF domain the signal transmitted through an optical fiber from the remote antenna. The current Pre-ADU version adopts WDM (Wavelength Division Multiplex) optical receivers, which paired with WDM optical RFoF (RF over fiber) transmitters at the antennas, allow to use one single fiber for both antenna polarizations.

A standard direct RF receiver (i.e. without any frequency conversion) follows the ORX. Several functions are here included in order to adapt the signal for the digital conversion: amplification, level adjustment (by means of a digital step attenuator, 31 dB range/1 dB step), band selector with a filter bank (low band, 50–375MHz, or high band, 375–650MHz) and a RF switch to close the RF input of any receiver on a 50 Ohm load for debugging procedures. The digital step attenuator and the two RF switches (band selection and 50 Ohm load) are controlled by ADU board via the SPI bus. Fig. 6 shows the PCB of one double channel Pre-ADU receiver.

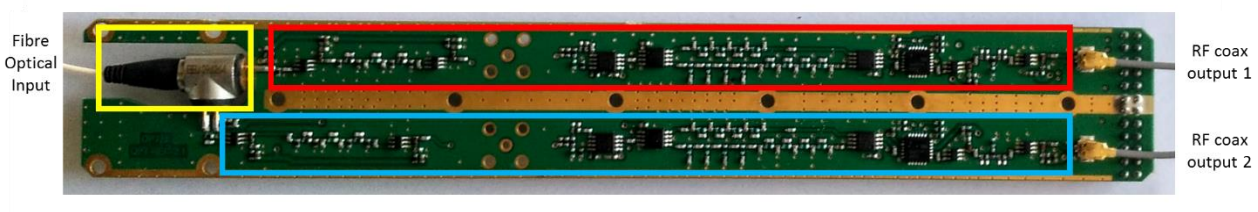

Fig. 6. Pre-ADU integrated WDM optical photodiode (yellow) and double channel RF receiver (red and blue) PCB.

4. Test set-up for ADU board performance evaluation

4.1. *Performance parameters*

Two ADU boards (with and without ADA) have been compared by measuring the performance parameters listed in Table 4. Except for the Gain Flatness, these are the typical parameters of dynamic (AC) tests used to characterize the A/D converters and are calculated with a standard Fast-Fourier Transform (FFT) analysis.

Tests are made with the analog signal at the rated frequency with a signal power of 1 dB below full scale (dBFS) at the inputs of the ADU.

More details about test procedures and the definition of dynamic performance parameters of ADC can be found in Analog Devices Inc. (2005), Arrants, Brannon & Reeder (2015) and Kester (2009).

Table 4. Performance parameters typically used to characterize the A/D converters. They are adopted to compare the two versions of ADU boards (with and without ADA).

Parameter	Definition
Gain Flatness [dBFS]	The level of the fundamental tone referenced to full scale.
Signal to Noise Ratio [dB]	The ratio of the RMS signal amplitude to the RMS value of the sum of all spectral components except the first six harmonics and dc.
Signal to Noise Ratio referenced to Full Scale [dBFS]	The ratio of the RMS full scale to the RMS value of the sum of all spectral components except the first six harmonics and dc.
Spurious Free Dynamic Range [dBc]	The ratio of the RMS value of the signal to the RMS value of the worst spurious signal (Harmonic Distortion (HD) or not) regardless of where it falls in the frequency spectrum.
Harmonic Distortion [dBc]	The level of the first six harmonics referenced to the carrier.
Worst Other Spur [dBc]	The level of the worst spurious component excluding the first six harmonically related components referenced to the carrier.
Total Harmonic Distortion [dBc]	The ratio of the RMS signal energy to the RMS value of the sum of the first six harmonics.
ENOB [bits]	Effective number of bits.
Cross-Talk [dBc]	The measure of any feedthrough coupling onto the quiet channel referenced to the carrier.
Second-Order Input Intercept Point [dBm] Third-Order Input Intercept Point [dBm]	$IIPn = P + \frac{\Delta P}{n-1},\ n = 2\ (IIP2),\ 3\ (IIP3)$ where P is the output power of the fundamental, and ΔP is the difference between P and the nth-order Intermodulation Distortion (IMD) product.

4.1.1. *FFT analysis*

Performance parameters are evaluated with an FFT analysis of the data captured by the board. This analysis, executed by offline data analysis software (see section 5.2), is divided into: single-tone and two-tone FFT analysis depending on whether only one tone or two tones are injected into ADC input.

It is recommended that frequencies of the input signal are chosen according to the following relation:

$$M * F_i = J * F_s \tag{1}$$

where M is the number of samples in the data record, F_i is the frequency of the input signal, J is an integer prime number of cycles of the input waveform in the data record, and F_s is the sampling frequency. Additionally, both the signal generator and the clock source used to trigger the sampling of the ADC should be phase-locked with a stable reference signal. These two conditions ensure coherent sampling that provides the best results to accurately measure the noise and distortion spectral components in the FFT. In these tests we satisfy the second condition using a common and stable reference signal (it was provided by Hydrogen Maser available in our laboratory). But equation

(1) is not completely respected since the frequency increments of the signal generator do not allow the required precision to be reached.

Coherent sampling cannot be achieved, hence a window weighting function (see section 5.2) is applied to the time record to minimize spectral leakage. Windowing (Harris, 1978) consists of multiplying the data in the time domain by a suitable window function with low-side lobes to resolve the noise and harmonic components in the frequency spectrum.

While the signal generator is connected to an ADU board input, all the other inputs are terminated to 50 Ohm.

Tests are repeated for all the ADU board inputs to evaluate the performances of each input chain and measure the cross-talk between them.

Except for IIP2 and IIP3 (two-tone analysis), the performances are measured in two frequency bands:

- 50–375 MHz ("low frequency band") sampling data at 800 MSPS (1st Nyquist zone);
- 375–650 MHz ("high frequency band") under-sampling data at 700 MSPS (2nd Nyquist zone)

with segmented frequency sweeps setting a step size of about 1M Hz. The second and third-order input intercept points are computed on just one point of the low band and one point of the high band. The adopted frequencies of the two tones (equalized at the exactly same level after filter attenuation) are: 184 and 187 MHz for low frequency band, and, 500 and 503 MHz for high frequency band.

4.2. *Hardware test set-up*

The basic setup (Fig. 7) for dynamic testing includes a signal generator, band-pass filter, RF power meter (or spectrum analyzer), low noise power supplies, a stable reference signal, an ADU Board under test and a PC/workstation for instrument control, data acquisition and data analysis.

Single-tone tests are performed as summarized here below (details will be given in next sections):

- A PC/workstation controls the signal generator and the power meter (or spectrum analyzer) via GPIB.
- For every frequency spanning the bandwidth, the PC/workstation sets a frequency and a nominal power level of the signal generator and then corrects it iteratively by reading the level with a RF power meter (or spectrum analyzer). This loop process ends when the ADU board input receives a signal with a level of about -1 dBFS within ± 0.08 dB of accepted tolerance between the expected and measured value (good trade-off between precision and convergence of the algorithm). So the input signal amplitude is constant across all frequency range.
- ADU board FPGA stores time domain data in a 2 MByte BRAM and sends UDP packets through 1Gbit Ethernet link.
- The PC/workstation gets UDP packets, checks for data integrity and saves files.
- Software routines (written in Matlab® code) process data and compute some parameters to evaluate the performance over the bandwidth (SNR, SFDR, SINAD, ENOB, etc…).

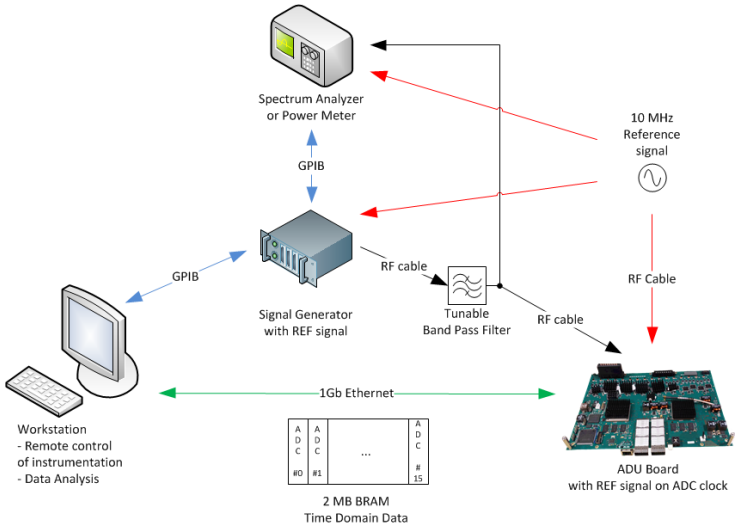

Fig. 7. Block diagram of hardware test set-up.

The goal of the test program is to measure the performances of the board including the harmonics and spurious signals generated by the device under test. Therefore, we have to ensure that the signal source is as "clean" as possible, not generating this kind of undesired signals; as such, it has to be properly filtered.

It is also necessary to verify that the test environment is not affected by RFI that could invalidate the measurements. For this reason, we performed a preliminary RFI monitoring campaign in the laboratory before starting the tests of ADU boards. Only negligible RFI signals were detected.

Gain flatness measurement of the ADU board should not be subject to the filter response and the stability of the signal generator RF output level across the frequency range. So the system must be controlled in closed loop to guarantee a constant level of the signal at the ADU board input, usually set to -1 dBFS, both for single-tone and two-tone analysis (see Section 5.2).

The signal generator is locked to a stable frequency reference (10 MHz). This is important to achieve a high level of spectral purity and to reduce the phase noise. The same reference signal is used to lock the PLL that generates the ADC clock of the ADU board, improving the precision of ADC sampling. Without this precaution the spectrum could be affected by phase noise and spurious signals thus corrupting the measurements.

In the case when a spectrum analyzer is present in the chain, the reference signal should be connected to it as well.

The test bench prepared for ADU board measurements is visible in Fig. 8 and includes the instruments listed in Table 5.

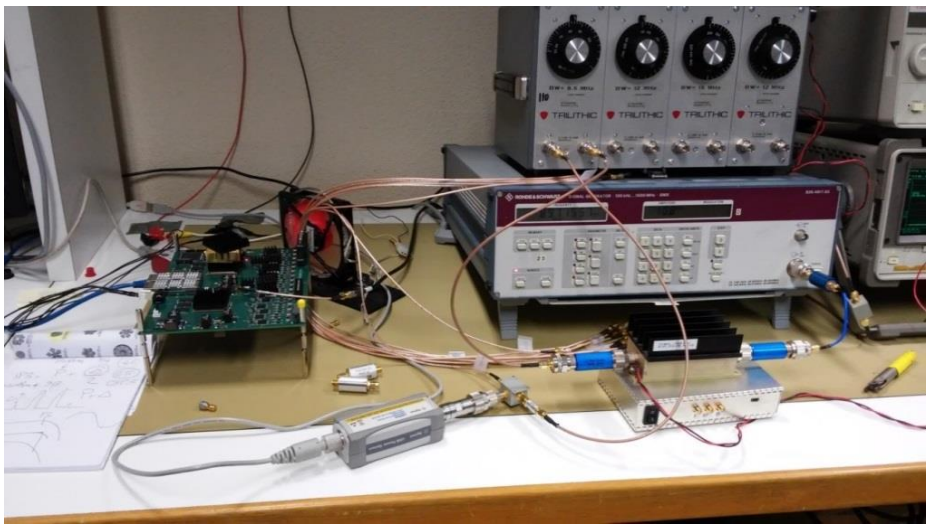

Fig. 8. Test bench for ADU board measurements.

Table 5. Instruments of the test bench used for ADU board measurements

Instrument	Model
Signal generator	Rohde&Schwarz SMX
Tunable band pass filter	Trilithic VF-40000
Low pass filters	Minicircuits SLP-100, SLP-250, SLP-450, SLP-550, SLP-1000
High pass filters	Minicircuits SHP-100, SHP-200, SHP-500
LNA	Minicircuits ZHL-2-8-N
Power meter	Agilent U2004A
Directional coupler	Minicircuits ZEDC-15-2B

5. Firmware and software

5.1. *Firmware*

The Xilinx UltraScale FPGAs are two identical devices that provide suitable and efficient resources to implement the main board data processing. The two FPGAs have an identical pinout and can share the same configuration firmware. In fact, each of the two FPGAs can manage 16 data links to receive data from eight ADCs and provide the required processing.

Firmware for the ADU board release 1.0 was developed as a very preliminary and limited version without too many IP cores (e.g. to address external DDR memories, interface with high speed QSFP+ links).

The planned tests require both time domain and frequency domain analysis on data sampled by ADCs. For convenience, these analysis algorithms have been developed in software rather than through dedicated firmware. So the FPGAs are used only to acquire ADC samples (via JESD204B lanes), buffer them into 2 MB Block RAM logic and subsequently send the time domain data in UDP packets through the 1 Gbit Ethernet interface. Once the buffer is completely filled, the memory is accessed for reading and data are sent in multiple UDP packets tagged with a very short header (sequence counters and flags). The firmware is flexible, allowing the user to select how many (from 1 to 16) and which ADC input streams are written into 2 MB internal memory.

5.2. *Instruments management*

As previously mentioned, the power level of the signal injected into ADU board must be equal to a constant value of -1 dBFS for every input frequency spanning the bandwidth of the test signal. There are some factors that affect this level like the non-stability of the signal generator RF output and the insertion loss of the filters that is variable with frequency.

Therefore, a control procedure that measures the level of the signal and corrects it to a constant target value is needed. This measurement is performed by the USB power sensor connected to a directional coupler. This power sensor can be easily controlled with python libraries (PyVisa) which instantiate a GPIB object over USB and provide the methods to change attributes (e.g. the timeout of instrument response) and read the power level (dBm).

When using a directional coupler, it is necessary to take into account both the coupling loss and the insertion loss of the device. Both depend on frequency and have to be considered during the correction procedure. Basically, the power read by the power sensor P_{read} has to be properly corrected using the following equation:

$$P_{corr}\,[dBm] = P_{read}\,[dBm] + Corr\_Factor\,[dB] \tag{2}$$

where P_{corr} is the corrected power and the correction factor is the difference between the insertion loss and the coupling loss.

The algorithm is very simple and can be described with the following steps (see also the block diagram of Fig. 9):

(i) the frequency of the signal generator is set taking the value from a predetermined subset and the amplitude value is set to an arbitrary fixed level.

(ii) The power sensor measures the signal level at the coupled port of the directional coupler and this value is corrected with the correction factor (see equation (2)) that depends on frequency.

(iii) If the difference between the value of the corrected measurement (P_{corr}) and the value of the target level (P_{target}, -1 dBFS) is not less than ±0.08 dBm then this difference is applied to the previous value of the signal generator. This operation is repeated until the condition is true.

(iv) When the previous condition is satisfied, UDP packets containing time domain data for this frequency are acquired and saved into files. This operation is repeated 10 times in order to let FFT spectrum be averaged to reduce noise in the analysis phase.

(v) Points from (i) to (iv) are repeated until the set of frequencies is finished.

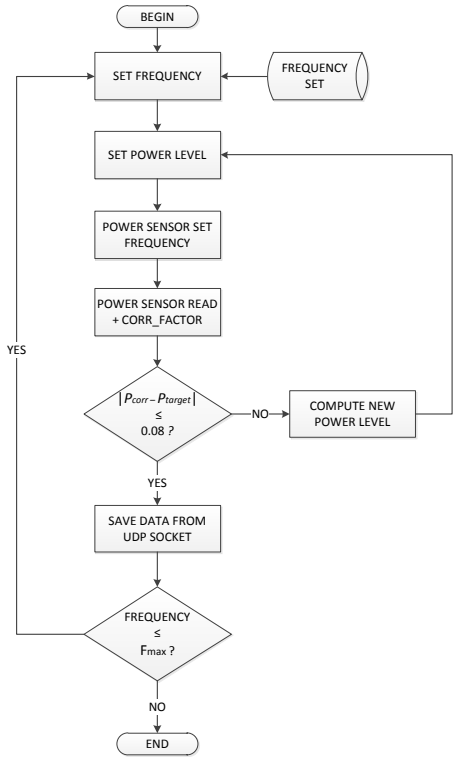

Fig. 9. Block diagram describing the state machine of the test.

Software functions in MATLAB® were specifically developed to calculate the performance parameters described in section 4.1. After data collection for every analog input and for every frequency of the bandwidth is complete, this software can be executed. The main steps are summarized in Fig. 10. First of all, some software parameters have to be set (see Table 6).

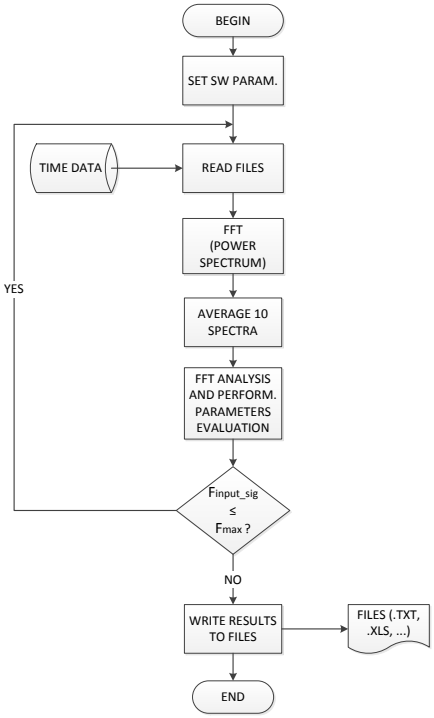

Fig. 10. Flowchart of data analysis software.

Table 6. List of software parameters that need to be set up at the beginning of software execution.

SW parameter	
F_s	Sampling Frequency (default 800 MSPS)
Nyquist Zone	1 for sampling in the first Nyquist Zone 2 for sampling in the second Nyquist Zone
N. Inputs	Number of inputs that are acquired (default 16)
Input Signal	What input is feeded with signal generator
Dir	Path where files can be read
N. Input Tones	1 for single-tone FFT analysis 2 for two-tone FFT analysis
HD Order	Number of Harmonic Distortion Products to be considered (default 6)

Starting from the first analog input under test and from the first frequency of the range, data files are read and copied into local memory. Then a real Fast Fourier Transform with a Blackman-Harris window is applied to time domain data. Once all the power spectra (10) have been calculated, they are averaged. The averaged power spectrum is the basis for calculating all the performance parameters described in section 4.1. The sequence of operations from reading data onwards is repeated for all the frequency set of the two bandwidths (50–375 MHz and 375–650 MHz). Finally, all the results are written in an output file.

The procedure described above provides the characterization of only one ADU Board input, such that all these steps have to be repeated for all inputs to fully test the board.

6. Results

6.1. *Cross-talk analysis*

Cross-talk analysis is important to determine the interference (or mutual coupling due to electromagnetic interaction) between adjacent traces and/or components on the board. For this kind of characterization, we drove the ADU board with the signal generator connected to one input and we measured the power level, relative to the frequency bin of the injected signal, from all the other inputs.

Consider the numbering of the ADU board inputs as indicated in Fig. 11, where the green boxes are the baluns, placed alternately on the top and the bottom of the board. The PCB traces that result more subject to cross-talk effects are the ones relative to inputs on top of the board (even numbers) and on the right hand side (the first 4 and in particular the n. #4 and #2). Fig. 12 provides an indication of the strongest interactions.

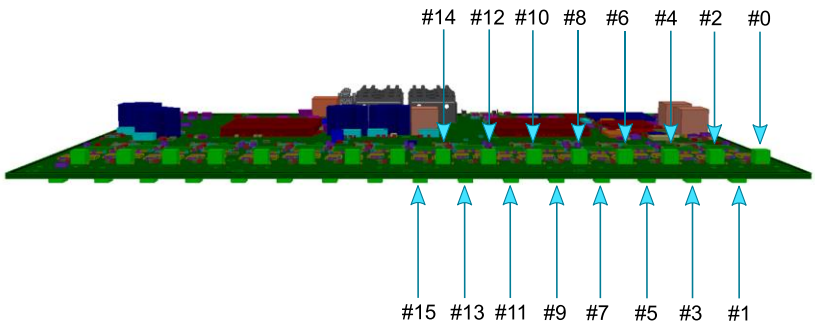

Fig. 11. Numbering of the ADU board inputs adopted for cross-talk analysis.

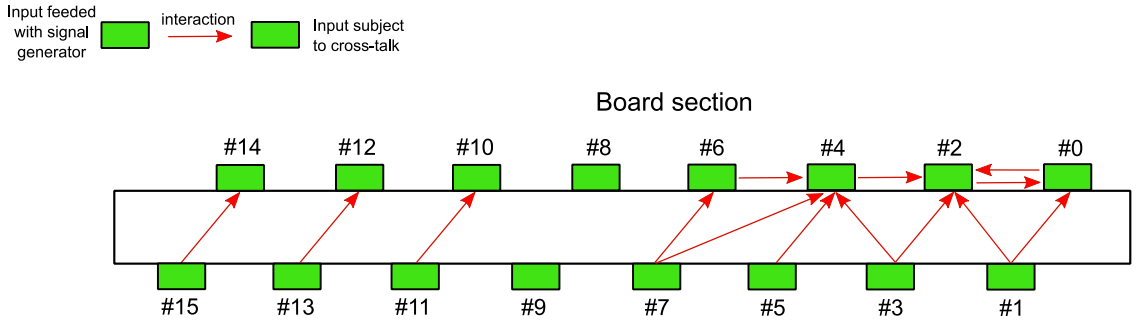

Fig. 12. The strongest interactions between the traces of the board due to cross-talk effect.

In Fig. 13 it can be observed that the worst case scenario for the two ADU boards occurs in the low frequency band: i.e. cross-talk "seen" by input #4 when the signal generator drives the other inputs. For both ADU boards the highest values are due to inputs #3, #5 and #6. This is very likely caused by the proximity of the traces in the PCB layout.

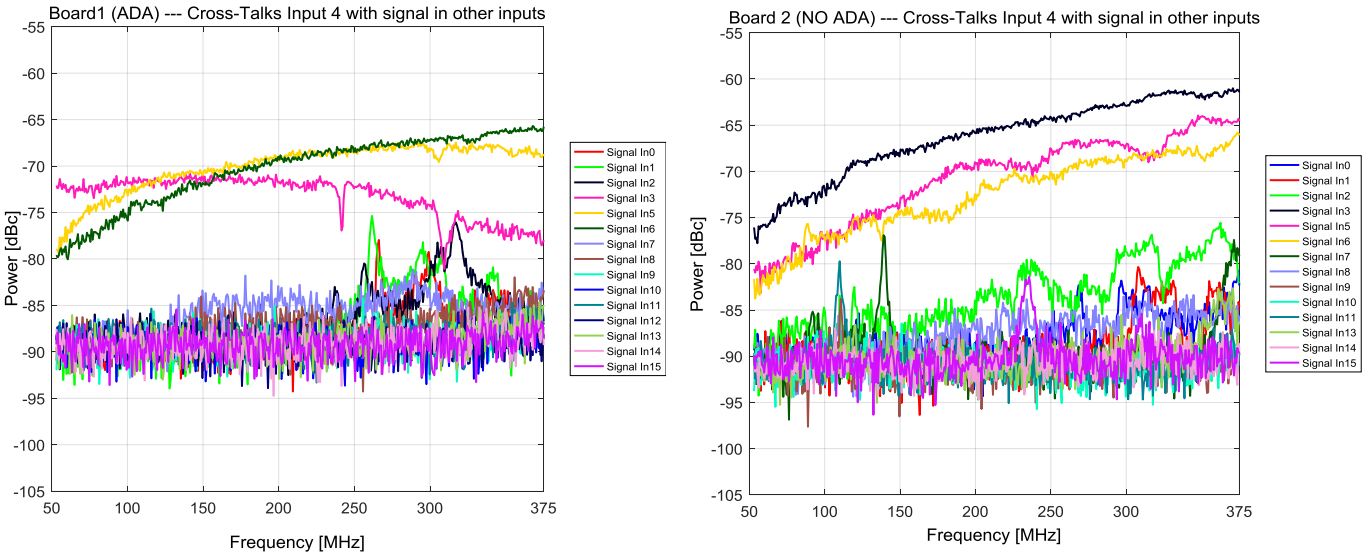

Fig. 13. Worst case of cross-talk level in low frequency band.

6.2. *Two-Tone analysis*

Intermodulation distortion (IMD) products may occur due to ADC nonlinearities when sampling a signal composed of two or more sine waves or narrowband signal groups. Two-tone testing in an ADC is a means of specifying these nonlinearities. The test signal consists of the sum of two independent, pure sine waves with frequencies, f_1 and f_2, at values that are an odd number of FFT bins away from $f_s/2$, with $f_1 > f_2$, where f_s is the sampling frequency.

When two tones at nearby frequencies are input to the ADC, we expect to find IMD products in the spectrum, in particular those of second and third-order.

Two tone IMD was measured using PNA-X Agilent 5249 A as source of the aforementioned two spectrally pure and independent sine waves (CW mode). We set the two tones at 184.7 MHz and 187.5 MHz for low frequency band, and, 500.1 and 503.2 MHz for high frequency band following equation (1) with power level close to full scale without clipping (-7 dBFS). Fig. 14 shows the spectra obtained with both boards.

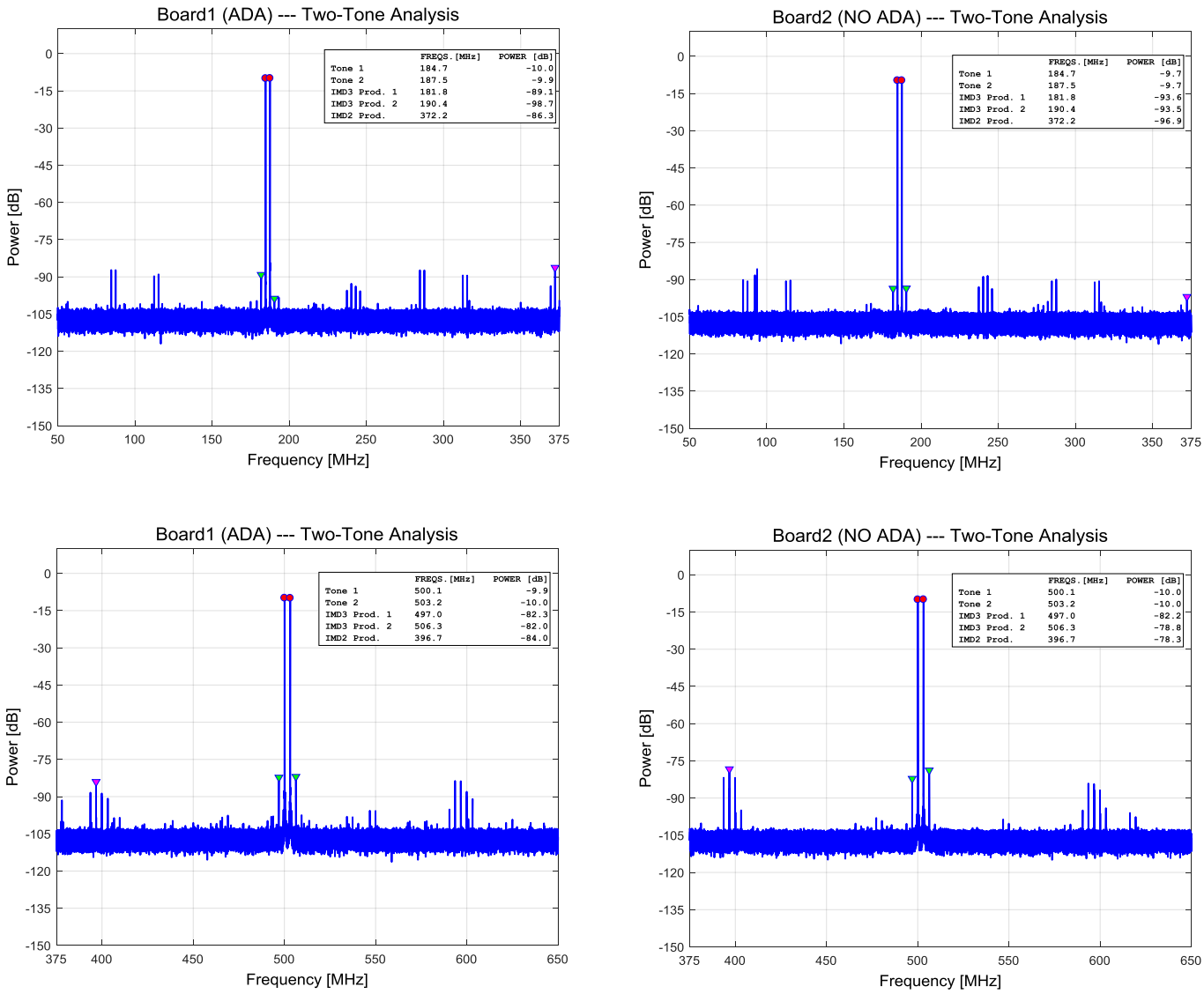

Fig. 14. Power Spectra with two tones injected to ADU boards for the measurement of IMD in both low and high frequency bands.

We have marked the fundamental tones, 2nd-order IMD product ($f_1 + f_2$) and 3rd-order IMD products ($2f_1 - f_2$, $2f_2 - f_1$) with different colors. Note that other spectral components are visible above noise level: they are relative to IMD products $2f_1 + f_2$ and $2f_2 + f_1$, 2nd and 3rd-order HD products of the fundamental tones and other spurious signals generated by clock signals inside the board (mostly 100 and 300 MHz).

After this two tone analysis, we also made some preliminary tests on TPM assembly connecting the ADU with one Pre-ADU board (Fig. 15). We properly set the acquisition chain to inject a white noise source with a power level approximately equivalent to the sky noise at that frequencies (-2.5 dBm). We then verified that the system was working correctly (Fig. 16): the RMS of the signal in terms of ADC units was as expected (19.8).

Moreover, with the same noise source in input, we added also the two tone signal (as in the previous test), and the result we obtained is reported in Fig. 17. It is possible to note that all the IMD products are no more observable since they are dominated by the noise level.

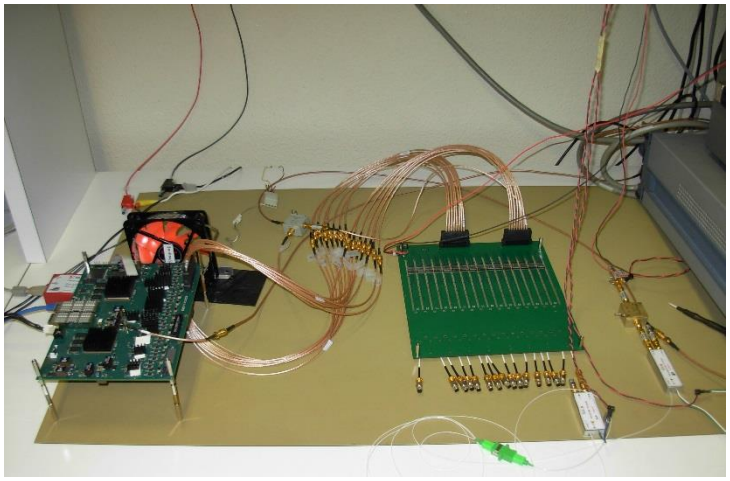

Fig. 15. Connection of Pre-ADU and ADU boards with white noise as input signal.

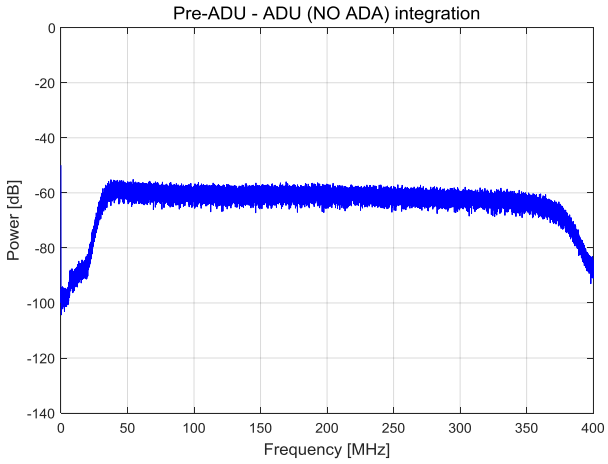

Fig. 16. Power spectrum obtained with the integration of Pre-ADU and ADU boards with white noise source.

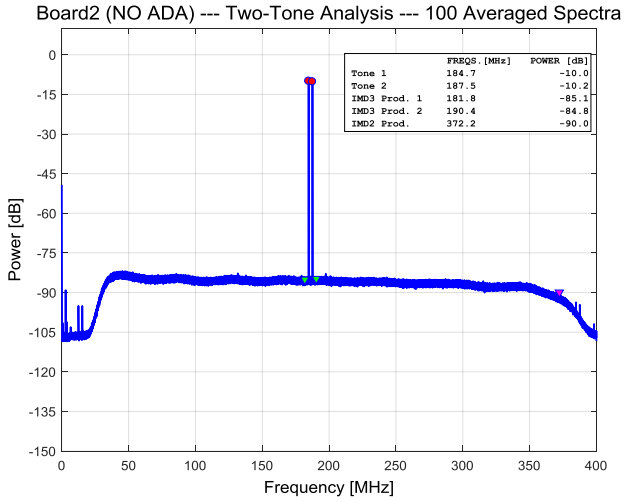

Fig. 17. Power spectrum obtained with the integration of Pre-ADU and ADU boards with white noise and two tones as input signal.

Table 7 and Table 8 summarize all the results obtained with the measurements performed on the two ADU boards over the two frequency bands respectively.

Table 7. Comparison of the two ADU Boards in terms of performance parameters in low frequency band (50-375 MHz)

Performance parameters	ADU Board#1 (with ADA) BW: 50 ÷ 375 MHz	ADU Board#2 (without ADA) BW: 50 ÷ 375 MHz
Single tone analysis		
Signal to Noise Ratio referenced to Full Scale [dBFS]	≥ 49.2	**≥ 49.3**
Gain Flatness [dBFS]	≤ ±0.4	**≤ ±0.3**
2nd-order Harmonic Distortion [dBc]	≤ -67.2	**≤ -67.7**
3rd-order Harmonic Distortion [dBc]	≤ -66.5	**≤ -68.6**
Worst Other Spur [dBc]	**≤ -67.0**	≤ -66.8
Spurious Free Dynamic Range [dBc]	≥ 66.5	**≥ 66.8**
ENOB [bits]	≥ 7.9	**≥ 7.9**
Cross-Talk [dBc]	**≤ -65.7**	≤ -61.0
Two Tone analysis		
Spurious Free Dynamic Range [dBc]	**≥ 76.3**	≥ 76.0
Worst Other Spur [dBc]	**≤ -77.2**	≤ -76.0
IP3 [dB] (F1=184.7 MHz; F2=187.5 MHz)	29.6	**32.2**
IP2 [dB] (F1=184.7 MHz; F2=187.5 MHz)	66.3	**77.5**

Table 8. Comparison of the two ADU Boards in terms of performance parameters in high frequency band (375-650 MHz)

Performance parameters	ADU Board#1 (with ADA) BW: 375 ÷ 650 MHz	ADU Board#2 (without ADA) BW: 375 ÷ 650 MHz
Single tone analysis		
Signal to Noise Ratio referenced to Full Scale [dBFS]	≥ 48.9	**≥ 49.3**
Gain Flatness [dBFS]	**≤ ±0.6**	≤ ±1.4
2nd-order Harmonic Distortion [dBc]	**≤ -65.8**	≤ -59.9
3rd-order Harmonic Distortion [dBc]	≤ -60.8	**≤ -65.6**
Worst Other Spur [dBc]	**≤ -64.2**	≤ -63.2
Spurious Free Dynamic Range [dBc]	**≥ 60.8**	≥ 59.9
ENOB [bits]	≥ 7.8	**≥ 7.9**
Cross-Talk [dBc]	**≤ -70.6**	≤ -70.4
Two tone analysis		
Spurious Free Dynamic Range [dBc]	**≥ 72.0**	≥ 68.3
Worst Other Spur [dBc]	≤ -80.8	**≤ -84.1**
IP3 [dB] (F1=184.7 MHz; F2=187.5 MHz)	**26.2**	24.4
IP2 [dB] (F1=184.7 MHz; F2=187.5 MHz)	**64.2**	58.3

Note that the values reported on the tables are relative to the worst case: that is the worst value considering all ADU inputs and all frequencies for that particular measurement. Also we have highlighted with bold type the best value between the two board versions. As can be noticed, the two versions present similar performances. This could be explained considering that at low frequencies (maximum operative frequency is 650MHz) the losses and parasitic effects of the passive components have a negligible impact. The benefits of the active solution probably would be more evident for operative frequency above 1 GHz.

We can see from the results that ENOB is very high (> 7.8) in all the considered cases and it complies with the requirements (Comoretto, 2016). Also Cross-talk parameter is abundantly within specification (≤ 30 dB), that derives from internal SKA engineering specification document.

7. Conclusions

In this paper we have presented a new signal processing hardware platform (ADU) for the SKA LFAA. With respect to existing architectures, it constitutes the best choice in terms of functionalities and modularity that fits the LFAA layout. This board is capable to digitize 32 signal streams up to 1 GSPS and provides the suitable DSP resources to implement the frequency domain beamformer, and the first stage of a high resolution spectroscopic channelizer of an LFAA station.

We have described preliminary tests aimed at a first evaluation of the ADU board, mainly for cross-talk and intermodulation distortion analysis and ENOB verification. The measurements have shown no undesired effects in a so densely populated board due to ADCs and PCB traces proximity, clock distribution circuit, baluns, etc... Moreover, we have demonstrated that ENOB parameter is in compliance with specification.

No significant performance differences arose from the comparison between two realizations of the same board (with and without ADA). On the other hand, the presence of the ADA causes an extra power consumption of about 16 W with respect to the values reported in Table 3 (without ADA). Considering the tight requirement for the power consumption mentioned in Section 2.5, the outcome of these measurements allowed to prefer the ADU version without DGA.

After the prototype described so far, a slightly different board (ver. 1.2) has been realized and is currently under test. It was needed in order to fix some minor bugs, especially to increase the power absorption capability and to equalize the traces of the ADC clock network. This version of ADU will be used for the already mentioned AAVS demonstrator in the LFAA site, in 2017. Furthermore, it will be part of the back-end of the Sardinia Array Demonstrator (SAD) telescope, at the Sardinia Radio Telescope (SRT) site near Cagliari (Italy). SAD will be a system composed of 128 dual polarization Vivaldi antennas operating between 270 and 420 MHz.

For the future, a new release of the board is planned to be produced: this will mount a new generation of ADC with a substantive power saving, the latest generation of FPGA device, in addition to other small modifications for board optimization.

Acknowledgments

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