Real-time Experimental Demonstration of Timestamped Digitised Radio over Switched Optical Ethernet Fronthaul

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Abstract: This paper experimentally demonstrates a novel digitised RF service transmission with data compression over switched 10Gbps optical Ethernet fronthaul showing low latency (<2.4μs), high transmission efficiency (~1/3 that of CPRI) and wide dynamic range (40dB). ©2020 The Author(s)

1. Introduction

Radio over Ethernet (RoE) offers a cost-effectiveness solution for last-mile wireless coverage by using existing Ethernet equipment and infrastructure for the provision of cellular services such as 5G. In the meantime, the packet-switched operation allows the realisation of traffic management and statistical multiplexing with virtualised functionalities. However, the stringent timing and capacity requirements are the bottlenecks for practical implementation. To solve these issues, a new Ethernet type fronthaul with timestamps [1] and functional splits allowing lower transmission data rate [2] has been defined. Although this approach can effectively improve the feasibility of real-life deployment, the flexibility of the open standards that enable network convergence is reduced as customised Ethernet equipment and vendor/operator-specific information are required.

In this paper, we demonstrate a novel flexible RoE approach by packetizing compressed digitised RF data into Ethernet frames with additional timestamps for packet reordering and synchronisation. The system shows robustness in terms of low latency, link efficiency, as well as wide RF dynamic range.

2. System Architecture and Frame Structure

The system architecture of the RoE system is illustrated in Fig.1. In a central unit (CU), RF services are firstly down-converted to an intermediate frequency (IF) located in the first Nyquist zone for a given digitiser. The data is then digitised by an analogue to digital converter (ADC) which is followed by a field programmed gate array (FPGA) where the data is digitally down-converted (DDC) to baseband. The resultant I/Q bits are compressed to 8-bit wide words, based on the algorithm described in [3][4], then packetized into an Ethernet frame, illustrated in Fig.2, using the FPGA. A 4-Byte timestamp allowing a resolution of 2^{-32} seconds for timing operations is added along with the I/Q payload. The packets carrying radio information are then fed to a commercially-available off-the-shelf (COTS) 10Gbps small form pluggable plus (SFP+) module with integrated 1550nm distributed feedback (DFB) laser for transmission over the optical 10G Ethernet channel. At the remote unit (RU), received frames are reordered and synchronised before recovering back to digital IF which is subsequently converted back to analogue format using an analogue to digital converter (DAC) and upconverted to the RF carrier for radio transmission.

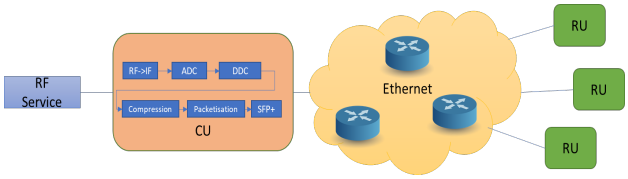

Fig.1 RoE Architecture

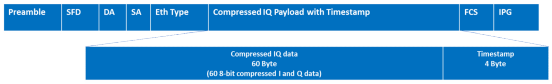

Fig.2 Frame Structure

3. Experimental Setup and Results

The experimental setup is shown in Fig.3. A 64 quadrature amplitude modulation (64-QAM) downlink LTE signal (test model 3.1) with an IF of 37.5MHz is generated from a vector signal generator (VSG). The signal is then digitised by a 16-bit ADC (TI ADC16DX370) in-turn connected to a master NetFPGA development platform incorporating a Xilinx Virtex 7 FPGA for data processing [5]. The digital data is compressed via a two-stage compression mechanism including sample rate reduction and non-linear resolution suppression [4]. The resultant I/Q data rate per 20MHz-bandwidth LTE service is 400Mbps (~1/3 that of common public radio interface or CPRI). In this setup, the compressed IQ information is replicated 10 times for a 64-byte payload and 20 times for a 512-byte payload for 10Gbps onward transmission over optical fibre, allowing extra room for the Ethernet overhead (i.e. 20×20MHz = 400MHz band to be transmitted over a single 10G network). The optical signal produced by the SFP+ module on the NetFPGA (master) board is sent through an optical fibre patch cord connecting to an Ethernet switch

which is emulated by a NetFPGA-based Ethernet learning switch, thus forwarding packets based on their MAC addresses and associated port previously learned [5]. In the NetFPGA (Slave), the data is recovered to the digital IF before being converted back to analogue format by a DAC (TI DAC38J84).

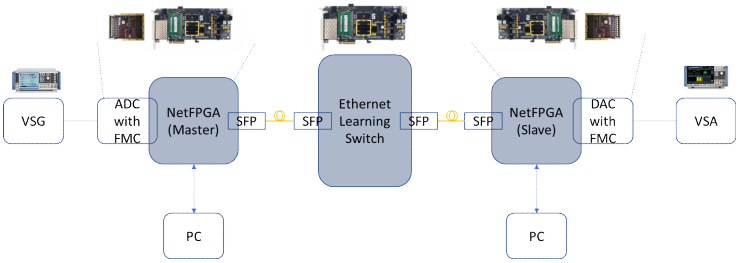

Fig.3. Experimental Setup for the RoE Demonstration

The error vector magnitude (EVM) of the signal, a measure of the modulation accuracy, is measured by a vector signal analyser (VSA). The maximum input power to the ADC is kept below 0dBm to avoid over ranging and the input bandwidth is varied from 10MHz to 20MHz. As shown in Fig.4, an input power dynamic range of over 40dB at less than the 8% EVM limit specified by 3GPP for a 64QAM signal is observed with a minimum value of around 2%.

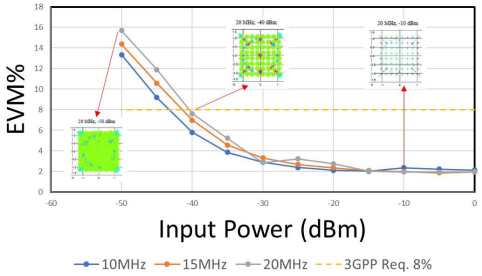

Fig.4. EVM Results and Constellation Diagrams

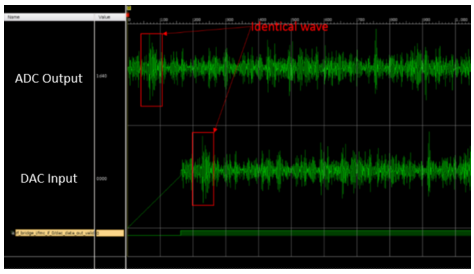

Fig. 5. Waveform Analysis in Vivado ILA

To measure the overall system latency, the signal is looped back to the master NetFPGA, permitting measurement of the delay offset between the identical data patterns at the ADC output and the DAC input. The waveforms are displayed by Xilinx Vivado integrated logic analyser (ILA) tool as shown in Fig.5. Different loopback measurements are compared in table 1. A single FPGA internal loopback gives 364ns and 513ns delay for 64 byte and 512-byte payload sizes respectively. Adding Ethernet and optical transmission will introduce extra latency. In this work transmission via an Ethernet switch, each switching stage adds approximately 800ns extra delay. Hence a limit on the number of switch stages must be imposed to meet the latency budget. For the 5µs budget as specified by CPRI, there is a maximum of two switch stages for a 512-byte payload size.

Table 1. Latency Analysis Results

Payload Size	Internal Loopback	10G SFP+ loopback	Switch Loopback
64B	364 (±7) ns	1026 (±7) ns	1846 (±7) ns
512B	513 (±7) ns	1253(±7) ns	2368 (±7) ns

5. Conclusion

This paper demonstrates a new compressive RoE optical fronthaul scheme allowing high-efficiency, low-latency, and multi-service interoperable transmission over Ethernet infrastructure. The results have shown over 40dB RF dynamic range for less than 8% EVM and approximately 2.4µs delay over single-stage Ethernet switch for a 512-byte payload. A 5G compatibility test is planned.

4. References

[1] IEEE Standard for Radio Over Ethernet Encapsulations and Mappings, Standard 1914.3-2008, Sep. 2018

[2] “Technical Specification Group Radio Access Network; Study on New Radio Access Technology; Radio Access Architecture and Interfaces,” 3GPP TR 38.801 V2.0.0, Tech. Rep., 2017.

[3] T. Li, R. V. Penty, and I. H. White, "Novel digital radio over fibre for 4G-LTE," IEEE Int. Conf. Commun. Work. ICCW 312–317 (2015).

[4] W. Li, A. Chen, T. Li, R. V. Penty, I. H. White and X. Wang, “Novel Digital Radio Over Fiber (DRoF) System With Data Compression for Neutral-Host Fronthaul Applications”, in IEEE Access, vol. 8, pp. 40680-40691, 2020

[5] Zilberman, N. et al. (2014). NetFPGA SUME: Toward 100 Gbps as research commodity. Micro, IEEE. 34. 32-41. 10.1109/MM.2014.61.