Modelling and Design Optimisations of CMOS MEMS Single Membrane Thermopile Detector Arrays

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Declaration

I hereby declare that the contents of this dissertation are the result of my own work and contains nothing which is the outcome of work done in collaboration with others, except as specified in the text and Acknowledgements. I further state that except where specific reference is made to the work of others, the contents of this dissertation are original and no substantial part of it has already been submitted, or, is being concurrently submitted for any such degree, diploma or other qualification at the University of Cambridge or any other University or similar institution. This dissertation does not exceed the prescribed word limit for the Engineering Degree Committee.

Ying Dai

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Abstract

Thermal imaging devices based on Complementary Metal-Oxide-Semiconductor (CMOS) and Micro-Electro-Mechanical System (MEMS) technology are widely used across consumer and industrial applications. The combination of CMOS and MEMS technologies allows for the production of devices with high performance, good reliability and consistent reproducibility. Additionally, these technologies allow devices to be manufactured at low cost and a high volume.

There are several types of thermal sensing technologies, however, this thesis mainly focuses on 8×8 thermopile based Focal Plane Arrays (FPAs). The core principles governing the function of thermopiles are based on the Seebeck effect. In this thesis, the structure and fabrication process of thermopile FPAs are described and discussed. The thesis describes the functionality of the array chip and introduces a new experimental technique, called the bi-directional electrical biasing method, which was applied to obtain the device's responsivity and crosstalk measurements. Compared to traditional measurement approaches using laser sources, this novel method significantly reduces the complexity of the experimental setup, as no external laser source is required. The crosstalk of the 8×8 array is ~2.69% and the responsivity is ~73.1 V/W. A detecting system using a larger array chip was designed, created and successfully applied in a series of experiments that involved gesture recognition and people counting.

In order to enhance the performance of the current array device, a 3D simulation model based on the Finite Element Method (FEM) was built using the COMSOL Multiphysics simulation tool. The numerical model was validated by comparing the model's simulated values for responsivity, crosstalk and temperature distribution with experimental results. The difference between the simulations and experimental results was <5%. With the aim of optimising various trade-offs, modifications in heatsinking

track widths/materials, additional air gaps between pixels, different packaging and different pixel sizes were assessed using numerical models. A design with copper heatsinking tracks and air gaps showed the best results, achieving an increase in responsivity by 6.4% while simultaneously reducing crosstalk by 65%. In addition, the vacuum packaging can reduce the crosstalk to less than 0.7% (only 0.2% in the model with copper tracks) and increase the responsivity to > 90 V/W in the model with tungsten tracks. A 32×32 array design demonstrates the smallest pixel size that can be achieved based on this thermopile array design. The 32×32 array design increased responsivity to ~77.18 V/W and crosstalk remained <4%. Crosstalk rose sharply to >6% when the pixel size was reduced further in a 64×64 array design, at this level of crosstalk, image quality is likely to be significantly affected.

Future work may focus on the implementation of carbon nanotubes or novel 3D thermopile designs. Carbon nanotubes, when deposited over the array chip, could enhance the absorption of IR radiation. While new thermopiles employing a 3D design could dramatically reduce array size and potentially achieve a fill factor of 100%.

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List of abbreviations

3D	*Three-Dimensional*
α	*Seebeck coefficient*
τ	*Response time*
ADC	*Analogue to Digital Converter*
AFE	*Analogue-Front-End*
CAGR	*Compound Annual Growth Rate*
CMOS	*Complementary Metal Oxide Semiconductor*
CNT	*Carbon Nanotube*
COVID-19	*Coronavirus 2019*
DRIE	*Deep Reactive-Ion Etching*
FEM	*Finite Element Method*
FIR	*Far-Infrared Radiation*
FPA	*Focal Plane Array*
FTIR	*Fourier-Transform InfraRed*
GND	*Ground*
IC	*Integrated circuit*
TCAD	*Technology Computer Aided Design*
IoT	*Internet of Things*
IR	*Infra Red*

LWIR	*Long-Wavelength InfraRed Radiation*
MCU	*Microcontroller*
MEMS	*Micro Electro Mechanical System*
MOSFET	*Metal-Oxide-Semiconductor Field-Effect Transistor*
MWIR	*Mid-Wavelength InfraRed Radiation*
NIR	*Near-InfraRed Radiation*
NEP	*Noise Equivalent Power*
NETD	*Noise Equivalent Temperature Difference*
PGA	*Programmable Gain Amplifier*
PVC	*PolyVinyl Chloride*
PZT	*Lead Zirconate Titanate*
R_v	*Voltage Responsivity*
SEM	*Scanning Electron Microscopy*
SiC	*Silicon Carbide*
SOI	*Silicon On Insulator*
SWIR	*Short-Wavelength InfraRed Radiation*
UV	*UltraViolet*
V_J	*Johnson noise voltage*

List of publications

[1] Y. Dai, S. Z. Ali, R. Hopper, C. Falco, P. Pandey, C. Oxley, D. Popa, and F. Udrea, "Crosstalk Analysis of a CMOS Single Membrane Thermopile Detector Array," *Sensors*, vol. 20, no. 9, 2020, doi: 10.3390/s20092573.

[2] Y. Dai, S. Z. Ali, R. Hopper, C. Falco, D. Popa, and F. Udrea, "Light-Free Cross-Talk Analysis of a CMOS Infrared Detector Array," in *4th International Conference nanoFIS*, Dec. 2020, doi: 10.3390/proceedings2020056010.

[3] Y. Dai et al., "Study of EM & Thermal Design in 1.2kV/600A IGBT module," in *19th EuroSimE*, 2018, pp. 1-4, doi: 10.1109/EuroSimE.2018.8369859.

[4] D. Popa, S. Z. Ali, R. Hopper, Y. Dai, and F. Udrea, "Smart CMOS mid-infrared sensor array," *Optics Letters*, vol. 44, pp. 4111-4114, 2019, doi: 10.1364/OL.44.004111.

[5] R. Hopper, S. Z. Ali, S. Boual, A. D. Luca, Y. Dai, D. Popa, and F. Udrea, "A CMOS-Based Thermopile Array Fabricated on a Single SiO2 Membrane," in *Proc. EUROSENSORS 2018*, Sep. 2018, doi: 10.3390/proceedings2130878.

[6] Y. Dai, S. Z. Ali, R. Hopper, D. Popa, and F. Udrea, "Modelling of CMOS Single Membrane Thermopile Detector Arrays," *accepted in IEEE Sensors.*

Chapter 1

Introduction

1.1 Overview

In recent decades, Complementary Metal-Oxide-Semiconductor (CMOS) Micro-Electro-Mechanical System (MEMS) technology has been utilized across a wide range of fields that require sensors, from flow sensors, gas sensors and pressure sensors to thermal sensors [1]. The majority of thermal infrared (IR) focal plane arrays (FPAs) in thermal sensors are based on CMOS MEMS technology as they offer the benefits of low-cost and low-power consumption. Thermal sensors are increasingly used in various fields [2–5], such as Internet of Things (IoT) environments [6], consumer electronics [7], activity recognition for care services [8], presence detection for security [9], in addition to applications which require high volume device manufacturability and battery-powered operation [7].

Despite the established use of thermal sensors, it is anticipated that the market for these products will further expand in the near future. The global thermal imaging market in 2020 was about $3.4 billion and is predicted to reach around $4.6 billion by 2025, with a compound annual growth rate (CAGR) of 6.2% [10]. The growth of this market is mainly driven by the increasing demand from end-use applications, like the automotive

industry, military and defence, manufacturing, healthcare and life science [11]. Moreover, since the end of 2019, IR thermometry has played a crucial role in the severe coronavirus (COVID-19) pandemic. The pandemic resulted in an exponential increase in demand of thermometers and thermal imagers in both the healthcare and transportation industries [12]. Non-contact IR temperature measurement devices greatly improve the efficiency of temperature detection, so that medical staff can quickly identify people with an abnormal body temperature and minimise the spread of the virus. Due to this new use case, IR thermometers and IR imaging devices are widely employed in daily life; they can be found in airports, train/bus stations, hospitals and even at the entrance to shopping malls.

The process technology that can produce integrated mechanical or electrical devices or systems in size range from a few micrometres to millimetres, is known as MEMS [58]. MEMS devices borrowed the processing techniques and materials from integrated circuit (IC) and developed additional techniques like plating, moulding, wet and dry etching for fabrication [58, 59]. Though MEMS devices are on the micro scale, they are capable of sensing, controlling and actuating the required signals and have an impact on the macro scale [58].

CMOS MEMS technology allows for interface circuitry to be monolithically integrated or co-packaged with sensing elements. The close proximity of the circuitry and sensors reduces the noise while benefitting from all the advantages of the CMOS process (i.e., high-volume manufacturing, high-performance and low cost) [13]. In this thesis, the aim is to characterise CMOS based thermal FPAs fabricated on a single membrane, employing standard CMOS tungsten (W) layers for heatsinking; a design that simplifies chip processing. Based on experimental data obtained from measurements of the thermopile-based array chips, accurate and fast simulation models have been constructed, which not only gave an insight into the device physics of the thermopile-based array but were essential in the optimisation process and led to several novel ideas about how best to maximise performance without resorting to exotic materials or

complex electronics.

1.2 State of the art IR cameras

There is currently great interest in the development of IR cameras and their underlying technologies [14]. Recent advances have focused on miniaturized, low-cost IR cameras suitable for mobile devices [15, 16]. At the simplest level, an IR camera is made up of an array of multiple sensors, which can generate thermal images and detect the movement and temperature of people or other near room temperature objects.

In order to produce a thermal image, the sensors in the thermal camera convert their absorbed thermal energy into an outputted electrical signal. The output signal is then amplified and converted from an analogue to a digital form. Subsequently, the signal is sent to a microprocessor via a read-out interface. The microprocessor interprets the signals and maps the temperature from every single pixel (individual detector picture elements) to create a thermal representation with the aid of a screen. An example of a thermal image is shown in Figure 1.

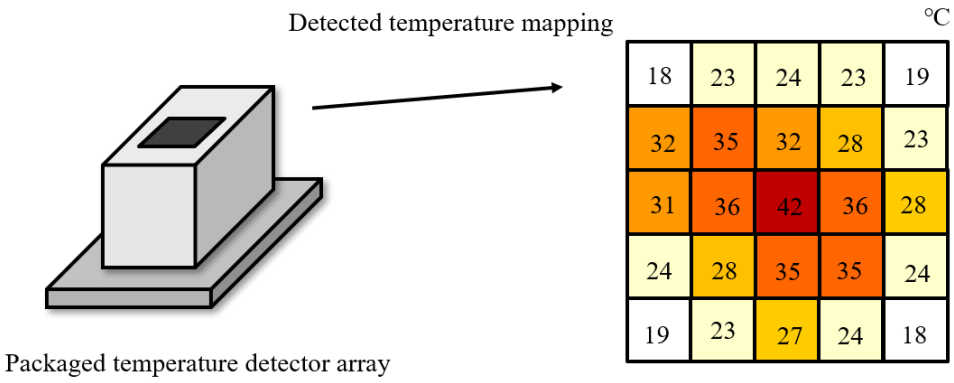

Figure 1: Thermal image example showing the map of temperature information in thermal representation view.

Generally, the performance of a thermal camera is assessed by the following parameters:

resolution, target temperature range, accuracy, responsivity and NETD (noise equivalent temperature difference, also known as the sensitivity of a thermal camera). The quality of a thermal image is determined by its resolution (the number of pixels used to form the image). Accuracy is the parameter used to assess the ability of a thermal camera to detect the correct temperature, normally expressed as ±2°C or 2% of the temperature reading, this gives the range of the errors that might be added to the detected temperature value. The responsivity can be defined as the change in voltage response per incident optical power [17]. The NETD is used to estimate a camera's ability to distinguish between noise and small temperature differences [17].

Other important aspects in evaluating the performance of a camera include the response time, spectral range, and crosstalk. The spectral range of a thermal camera is the range of IR wavelength which a thermal camera can detect. The response time of a thermal camera is defined as the time taken by the device to respond when the IR radiation is absorbed.

Crosstalk describes the effect which occurs when an IR source is focused on only one pixel, the signal output from the irradiated pixel may then induce parasitic signal outputs to adjacent pixels [18], see Figure 2.

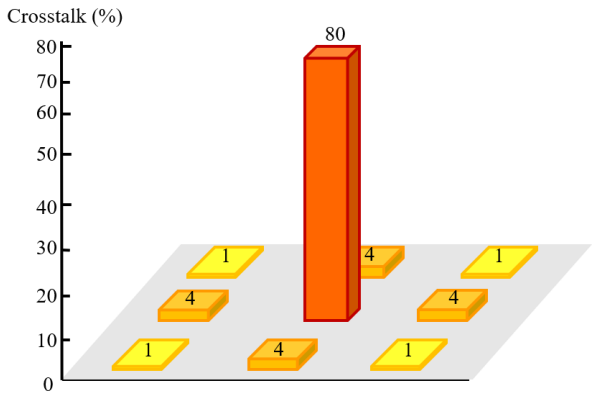

Figure 2: An example of crosstalk, an IR source is only applied to the centre orange pixel, but its adjacent pixels (yellow and light orange pixels) also show a response.

Figure 2 shows an example of the crosstalk effect in an array of pixels. Crosstalk rate (C) can be calculated by dividing the signal produced from the irradiated pixel (S_1) with the signal from its adjacent pixel (S_2), $C = S_2/S_1$.

In addition, the parasitic capacitance effect should be considered when designing electronic devices. Parasitic capacitance occurs when a pair of electric conductors are close to each other; the potential difference between them leads to the storage of an electric charge.

Current state-of-the-art IR cameras include handheld thermal cameras and smartphone applicable thermal cameras, the FLIR E96 [19] is currently considered to be one of the most accurate handheld IR thermal cameras for industrial use. Its dimensions are 278.4 mm × 116.1 mm × 113.1 mm (without the lens) with an IR resolution of 640×480 pixels based on microbolometers. The E96 can measure temperatures ranging from -20°C to 1500°C with an accuracy of ±2°C, and the NETD is less than 30 mK at 30°C. However, this camera costs more than $10,000, and it is not suitable for integration with consumer electronics, which is an area of anticipated high growth.

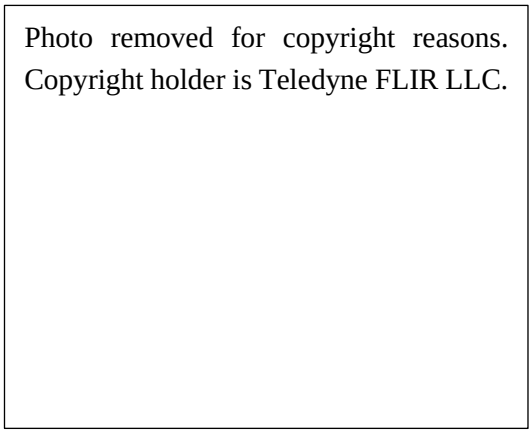

Figure 3: Smartphone thermal camera example [20].

Another example of a state-of-the-art thermal camera is the FLIR ONE Pro, which can be attached to a smartphone (Figure 3) [20]. This mobile camera has a size of 68 mm × 34 mm × 14 mm and can detect temperatures ranging from -20°C to 400°C with a 70 mK thermal sensitivity and ±3°C accuracy. Compared to the E96, the FLIR ONE Pro

has a reduced thermal resolution of 160 × 120 pixels. Despite its reduced performance, its significantly smaller size allows the possible integration in mobile phones. There are also commercially available FPAs based on thermopiles, e.g., the HTPA 120 × 84d series from HEIMANN Sensor, whose thermopile FPAs and has a resolution up to 120 × 84 pixels and can detect object temperature from -20℃ to more than 1000 ℃ [21].

In the past few years, there are various types of FPAs technologies have been studied and reported in the literature. In the case of IR FPA based on photodetectors, the first long-wavelength (more details about mid/long-wavelength IR in Chapter 2) IR InAs/GaSb superlattice FPA grown by metalorganic chemical vapour deposition (MOCVD) was presented by [22] with a clear image, this FPA has 320×256 pixels and achieved a peak detectivity (a parameter used to characterize the performance of an IR detector, more details in section 2.5.3) of 2.3×10^{10} cm·$Hz^{1/2}$/W at 80 Kelvin (K). By using the MOCVD, which is the leading epitaxy technology, the devices can be fabricated with high throughput production, easy maintenance process, and flexible reactor configuration [22]. To increase the operation temperature of the FPA based on photodetectors while keeping reduce the size, weight, and power (SWaP), Deng et al. reported a 640×512 middle-format pBn mid-wavelength IR photodetectors FPA involving short-period InAs/InAsSb T2SLs for being used as an efficient absorber to achieve devices at high temperature [23]. This FPA can be operated at a temperature up to 185 K and reach a specific detectivity of 4.43×10^{11} cm·$Hz^{1/2}$/W.

For FPAs based on thermal detectors, an ultra-small pixel (100 μm × 100 μm) IR sensing thermopile array (4 × 4 pixels) fabricated with a post-CMOS compatible process was introduced by [24]. This small array has a double layer structure (absorber and thermopiles in different layers) and achieved a normalized detectivity of 2.1×10^7 cm·$Hz^{1/2}$/W with a voltage responsivity of 52 V/W in air. A 160 × 120 long-wavelength IR CMOS microbolometer FPA was reported by Tankut et al. [25]. Compared to the traditional VOx bolometer-based arrays which usually require a special deposition and etching process, the post-CMOS process used in this paper only needs one mask

lithography process and a simple subtractive etching process to form the bolometer pixels. This FPA has a NETD of less than 90 mK at 4 frames per second (fps) [25].

To meet the requirements of high sensitivity, large dynamic range, large pixel count and fast data rate, Lincoln Laboratory developed a digital-pixel FPA (DFPA) technology [26] which is capable of 16-bit full dynamic range, analogue to digital conversion and real-time digital image processing (e.g., a 256 × 256 pixel image can be read out at a frame rate of 7 kHz.). This DFPA is a combination of the traditional detector array with a digital-pixel readout IC designed by their group. The integrated IC provides a low-power analogue to digital converter in each pixel and thus allows the rapid processing of digital data and enables real-time imaging [26].

Research on graphene has also been applied to IR FPAs technology. A graphene-based mid wavelength IR room temperature thermal detector has been published by Sassi et al. This paper introduced a thermal detector based on pyroelectric materials with a single layer graphene (SLG) amplifier integrated [27]. Due to the resistance of this two-terminal device changing proportionally with temperature, this detector can be considered as a bolometric resistor [27] and the temperature coefficient of resistance (TCR, the percentage of resistance changes per K, more details in section 2.3.2.2) can be measured. A floating metallic structure was included in this device and this structure used an integrated SLG field-effect transistor (GFET) to concentrate the charges produced from the pyroelectric substrate [27]. In this case, this detector can respond to DC signal without a chopper as the charge is unable to escape from the floating structure. They called this detector a “graphene-based pyroelectric bolometer” and shows a TCR up to 900 $\%K^{-1}$ (normally ~2 – 4 $\%K^{-1}$ for state-of-the-art materials) with a device area of ~ 300 × 300 μm^2 [27]. This new detector technology could be employed in future mid-wavelength IR uncooled FPA applications.

1.3 Thesis outline

This section provides a brief outline of the following seven chapters contained in this thesis.

This chapter, Chapter 1, outlines the main applications and markets for CMOS MEMS technology and introduces the aims of the thesis.

Chapter 2 describes the fundamentals of IR detection, including the IR spectrum, photon detectors and the different types of thermal IR detectors. The theories and working principles of the four main types of thermal IR detectors (thermopiles, bolometers, pyroelectric detectors and diodes) are presented with a comparison of their central properties. The IR focal plane arrays based on thermopiles and bolometers are introduced and compared. In addition, an overview of the MEMS technology fabrication process is presented.

Chapter 3 details the finite element method (FEM) for simulation. The basic working process of FEM is introduced and three types of elements (1D, 2D and 3D) are discussed and compared. Different FEM simulation software packages are compared, and the physics related to the simulation model developed in this project are depicted alongside a simple model of a thermocouple as a proof of concept.

Chapter 4 introduces the basic experimental setup, design and methodologies used in this project to measure responsivity and crosstalk. This includes a detailed explanation of a novel thermoelectric signal measurement method, the bi-directional electrical biasing approach. A detector array system design is also presented in this chapter that has been successfully used in gesture recognition and people counting.

Chapter 5 introduces an accurate numerical model of a thermopile array design. The model has been validated through experimental results and is used as a tool for optimisation of the process in addition to helping generate novel ideas. The signal responsivity and crosstalk are the main properties that demonstrate the design's performance. Model simplifications when compared to the real devices are explained and the comparison of the model to a current source and power source are presented.

Chapter 6 deals with further improvements to the array design based on the optimisation of the existing array and the introduction of novel approaches. Different heatsinking metals and different packaging are employed in the simulation model to enhance various performance parameters. Air gaps are placed between the pixels to improve the signal responsivity. The numerical model of the design with the combination of new heatsinking metal layers and air gaps are built for design optimisation. In addition, arrays with different pixel sizes are simulated and the possible smallest pixel size based on the current thermopile design is proposed.

Chapter 7 presents the conclusions of the thesis and proposes the future plans for this project. New designs for further improving signal responsivity and crosstalk performance are briefly discussed. A design implementing carbon nanotubes could be pursued as a future refinement of our design, as theoretically IR absorption could be increased to almost 100%. Additionally, novel 3D structures could be a creative choice for increasing the fill factor of the detector without impacting performance, or perhaps even improving performance.

Chapter 2

Fundamentals of IR detection and MEMS

2.1 Introduction

In this chapter, the fundamental theories behind the IR detection technology are introduced. The IR spectrum is depicted and the IR wavelengths of interest, along with their applications, are presented with examples. The basic concept of IR detectors is explained, introducing the two main categories of IR detectors, photon detectors and thermal detectors. Thermal detectors are often preferred as they are simpler and more cost-efficient. The main types of thermal detectors are thermopiles, bolometers, pyroelectric detectors, and diodes. The physics and properties of these four different thermal detectors are introduced and compared. The basic theory and working principles of the FPA and its main figure of merits are presented. Finally, the basic theory and key processes regarding MEMS fabrication are illustrated.

2.2 IR spectrum

IR radiation is a type of electromagnetic radiation with wavelengths longer than those of visible light and shorter than millimetre-waves (~0.76 µm to 1 mm) [17] as seen in Figure 4. Just like visible light, IR radiation also has optical properties like reflection, refraction, and the formation of interference patterns [28].

All objects above 0 K (> −270.15 °C) emit IR radiation and the temperature of the object determines the intensity and spectrum of the radiation [28]. This relationship between IR radiation and temperature allows IR detection technologies to be central in the development of temperature detection tools.

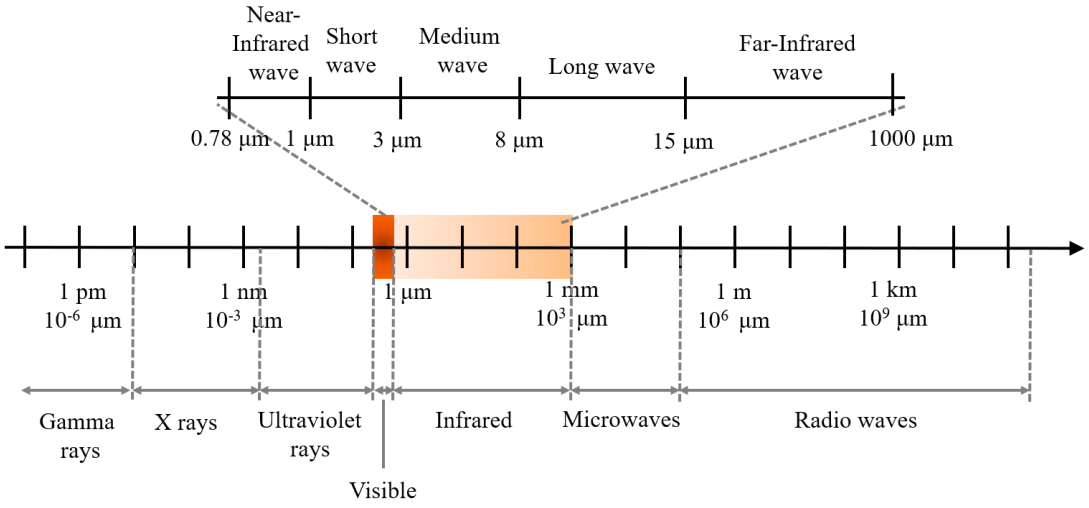

Figure 4: Electromagnetic spectrum with IR spectrum range enlarged.

IR radiation can be sub-divided into five main regions based on wavelength [17]. The first is the Near-IR radiation (NIR) region, with wavelengths ranging from 0.78 to 1 µm. This is followed by Short-wavelength IR radiation (SWIR) in the 1 ~ 3 µm region. The Mid-wavelength IR radiation (MWIR) region is from 3 to 8 µm. From 8 ~ 15 µm there is the Long-wavelength IR radiation (LWIR) region and finally, the Far-IR radiation (FIR) region ranges from 15 to 1000 µm. Thermal IR is an alternative name for MWIR and LWIR. LWIR is of particular interest to IR sensor technology and has

been widely used in industrial and even military applications, as it includes the IR radiation wavelengths emitted by the human body (8 ~ 14 μm).

2.2.1 Wavelengths of interest and their applications

Currently, IR based sensing technology is being developed for a large number of applications. These include detecting people presence for security purposes [29], military applications (such as night vision devices and IR tracking) [17], gas detection for environmental issues [30, 31] and medical applications [16, 17]. These devices allow people to 'see' objects which would be impossible with the naked eye. For instance, firefighters can use IR cameras to look for survivors through the smoke, additionally IR imagers can detect invisible gas leakages from pipes which may present further hazards in an emergency.

Figures 5, 6 and 7 illustrate some examples of the real-life applications of IR detection. Figure 5 shows a typical comparison of what is visible through the fog by visible light compared to IR light. This particular image displays a runway covered in dense fog, on which an aircraft is attempting to land.

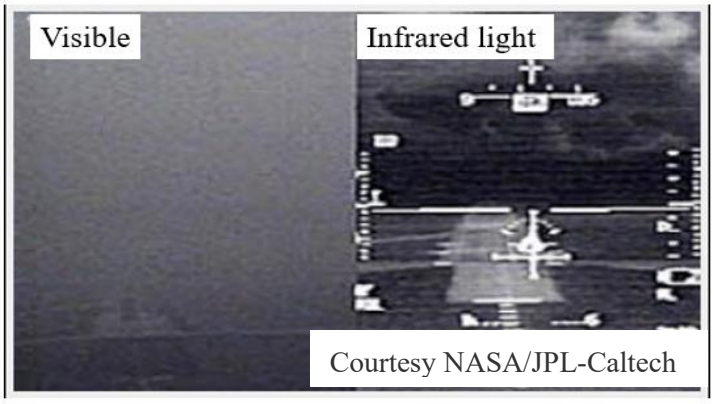

Figure 5: Comparison of visible and IR imaging in fog [32].

This application of IR detection technology can also be utilized in rescue activities as

previously mentioned, aiding rescue workers to identify civilians in thick smoke or fog and highly increasing the likelihood of saving lives in extreme situations.

IR cameras are also widely used for astronomy investigation (using wavelengths ranging from 1 to 300 μm). Figure 6 depicts the birth of new stars in space. The stars are surrounded and obscured by dust and gas; therefore, they are almost impossible to observe by detecting visible light alone (Figure 7a). By employing an IR camera (Figure 6b), the stars can be easily identified and observed through thick dust.

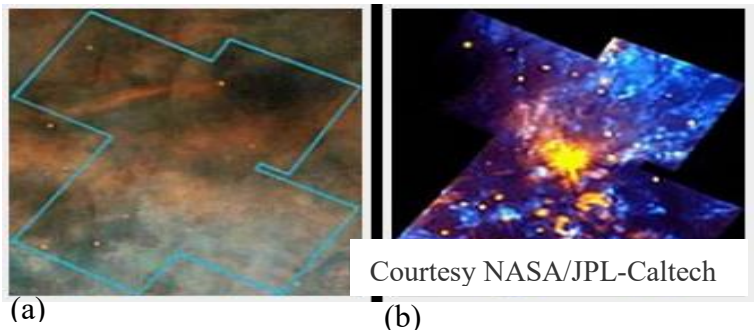

Figure 6: IR technology in astronomy, image under normal visible light camera (a) and IR camera (b) [32].

The research in this thesis aims to study a FPA which could be integrated into thermal imaging devices at room temperature (~25°C). The FPA will target the LWIR region between 8 to 15 μm. Figure 7 shows a comparison between a thermal image and a normal image with a hand covered by a plastic bag.

Figure 7: The comparison of human hand covered by plastic bag under normal camera (left) and IR camera (right) [32].

Thermal cameras have also been used in art research, for instance, NIR thermal cameras made up with indium gallium arsenide (InGaAs) are implemented in analysing the composition and underdrawings of the paintings, these cameras mainly detect the IR range from ~900 nm to 1700 nm [33]. Furthermore, a 384 × 288 pixels vanadium oxide (VO_x) uncooled bolometer camera module were designed by Arifin et al. to monitor the volcanic events and peat land fires in Indonesian [34].

In the normal camera, it is impossible to see through the plastic bag, however, the hand can be observed clearly with the IR camera. One can note that the temperature difference between the human body and the environment is easily detected and distinguished using a thermal camera [32]. The IR detector array devices investigated in this project are primarily aimed at detecting people presence. Further specific details are introduced and outlined in the following chapters.

2.3 IR detectors

Photon and thermal detectors are the two main categories of IR detectors [35]. This section explains the working principle and main properties of both detectors alongside the pros and cons of different IR detector technologies.

The voltage responsivity (R_v) is one of the main parameters to be considered in IR detectors. It is defined as the rate of the output signal (V_0) over the input radiation power (P_{in}) [36].

$$R_v = \frac{V_0}{P_{in}} \qquad (2.1)$$

In thermal detectors, the response time (τ) of the device can be calculated using equation (2.2) [35, 37]. This parameter measures the speed at which the detector reacts to the incident IR power.

$$\tau = \frac{C_{th}}{G_{th}} \qquad (2.2)$$

C_{th} represents thermal capacity (the ability of an object to store or release heat) and G_{th} represents the thermal conductivity (the ability of an object to conduct heat) of the detector.

Johnson RMS noise voltage (V_J) (equation (2.3)) [17], is one of the main types of noise to be considered in thermal detectors. It is defined as the noise generated by the thermal agitation of charge carriers inside the device [38].

$$V_J = (4KTR_{th}B)^{1/2} \qquad (2.3)$$

K is the Boltzmann constant, T the absolute temperature, R_{th} is the resistance, and B the noise bandwidth.

2.3.1 Photon detectors

This section introduces the basic concept concerning photon IR detectors. In this type of IR detector, the interaction between free electrons, lattice atoms, or impurities with IR radiation can lead to photoexcitation [38], which is the excitation process that converts photons into free carriers and result in the production of an output current.

Figure 8 shows the basic excitation process which occurs inside a semiconductor photon IR detector when it is heated. Section (a) of Figure 8 illustrates the intrinsic absorption, which occurs when the energy ($E = hv$, h: Planck's constant, v: photon frequency) from the absorbed photon is greater than the bandgap energy (E_g, the energy which allows an electron to move from valance band to conduction band) and thus

allows the transition of electron or hole (lack of electron in position) between the valence band and conduction band.

Figure 8 section (b) explains the extrinsic absorption, which occurs when the absorbed photon energy is smaller than the bandgap energy but larger than the energy of the impurities. This energy induces the transitions between acceptor (an atom tends to become negative by attracting electrons) with valence band or donor (an atom tends to become positive by attracting holes) with conduction band.

Figure 8 section (c) illustrates free carrier absorption, which usually occurs when the free carriers absorb photon energy in the conduction or valence band [39]. According to the categories of the interactions, photon detectors can be divided into the following types: intrinsic detectors (interband), extrinsic detectors (impurity to the band), quantum well detectors (to and/or from spatially quantised levels) and free-carrier detectors (intraband) [38]. Photon detectors usually require a cryogenic cooling system for detecting wavelengths above 3 μm.

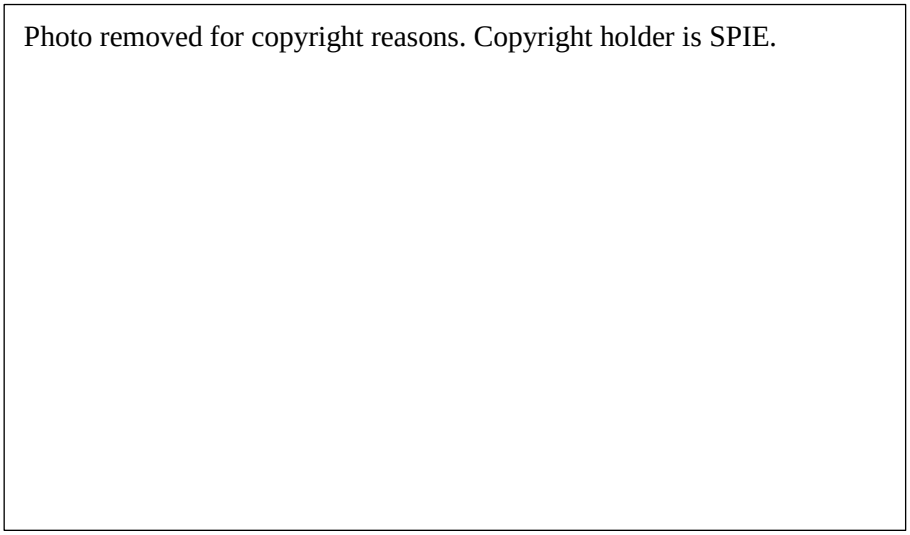

Figure 8: Photon detector excitations, adapted from [38].

In general, photon detectors have good sensitivity, low noise and short response time, but a cryogenic cooling system should be implemented to reduce the noise and detect wider range of IR wavelength. Some charge carriers are produced by the thermal energy

generated by atoms in the photon detector, and the photon energy induced by the radiation needed to compete with the thermal energy, thus without a cooling system, the detector becomes noisy [38]. The need for implementing a complex cryogenic cooling system for detecting IR wavelengths over 3 μm results in a great increase in device size, cost and manufacturing complexity [38] which makes photon detectors unsuitable for daily applications.

2.3.2 Thermal detectors

In thermal detectors, an electrical signal is generated as a result of changes in temperature-dependent physical properties when the detector's temperature varies due to the absorption of incident radiation (e.g., the thermoelectric voltage in thermocouples, resistance in bolometers, or pyroelectric voltage in pyroelectric detectors) [17]. Thermal detectors can be mainly classified into the following types: thermopiles, bolometers, pyroelectric detectors and diodes. The detailed properties and working principles of these detectors are discussed in the following subsections.

2.3.2.1 Thermopiles

A thermopile is an array of series-connected thermocouples (made up of two different conductors) which produces a voltage when there is a temperature gradient applied to the two junctions of the two electrical conductors [40, 41].

Figure 9 demonstrates a classic structure of an open circuit architecture for generating voltage in the open end (the cold end, where the two conductors are not connected). This structure is called a thermocouple. Leads a and b are made of materials with different Seebeck coefficients. According to Seebeck [40], the relationship between the

temperature difference of the two ends (ΔT (kelvin, k)) and the output voltage from the open end (V) is linearly proportional. This relationship can be expressed as in equation (2.4) below:

$$V = \alpha_r \Delta T \tag{2.4}$$

α_r (V/K) is the Seebeck coefficient, which is a constant parameter related to the material's temperature property. In the material, which is electrically isolated, V(V) is defined as the voltage generated by the thermocouple when its temperature changes with the value of ΔT(k).

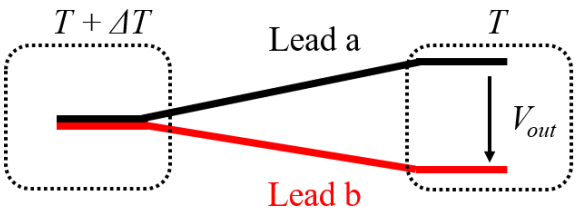

Figure 9: Thermocouple structure which comprises two different conductors (lead a and lead b) where one end is electrically joined. The joined end is the hot junction, and the open end is the cold junction [41].

α_a is the absolute Seebeck coefficient and is known as the differential relationship between the V and temperature T at temperature T_0 (the initial temperature) [42], see equation (2.5). The Seebeck coefficient of a thermocouple is the difference value of the absolute coefficients from the two conductors, thus equation (2.4) can be modified, as shown in equation (2.6), $\alpha_{a.a}$ and $\alpha_{a.b}$ are the absolute Seebeck coefficient of lead a and lead b, respectively.

$$\alpha_a = \left.\frac{dV_a}{dT}\right|_{T_0} \tag{2.5}$$

$$\Delta V = \alpha_r \Delta T = (\alpha_{a.a} - \alpha_{a.b}) \Delta T \tag{2.6}$$

However, the output voltage signal of a thermocouple is of the order of a few μV K^{-1}. In order to increase the voltage signal, a thermopile is used, which composes of a number of thermocouples connected in series [41], the basic structure is illustrated in Figure 10. The total output voltage signal is then *N* (number of thermocouples) times of the voltage from a single thermocouple, see equation (2.7).

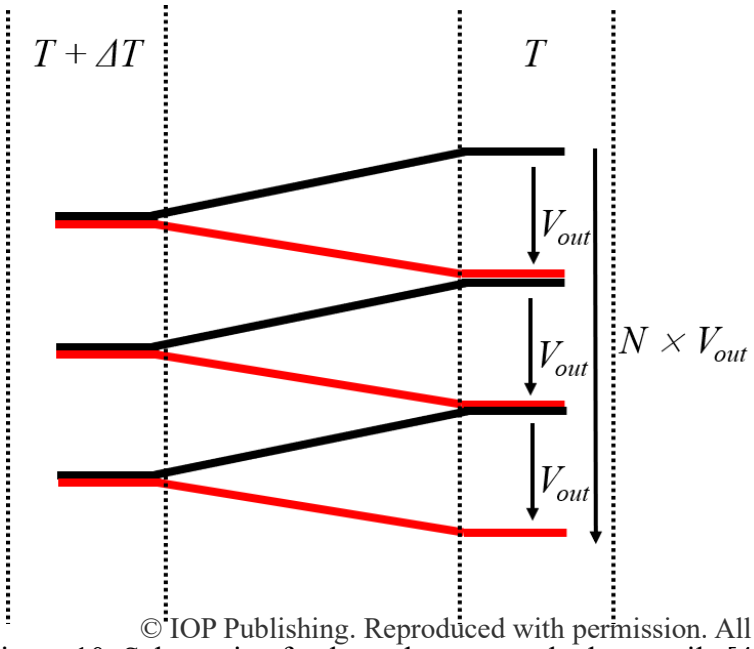

Figure 10: Schematic of a three-thermocouple thermopile [41].

$$V = N\alpha\Delta T \qquad (2.7)$$

As the output voltage from the thermopile is induced by incident radiation, a thermopile detector can be used without a chopper for detecting direct current (DC) radiation and have a reasonable DC response (e.g., 34 V/W in polysilicon thermopile ST150 [43]), this technology is low noise and low cost.

2.3.2.2 Bolometers

In bolometers, the resistance of the detector varies with changes in temperature [44]. A large difference in the resistance of bolometers would be induced when IR radiation is absorbed because this type of detector is usually made up of materials that contain a small thermal capacity with a large temperature coefficient [17]. Unlike thermopiles, bolometers are required to be biased by an external current source and then measuring the output voltage [17]. The relationship between the change in voltage and the change in temperature of a bolometer (which is constantly biased with a current, I) can be presented by equation (2.9) [17, 45] and the resistance temperature coefficient (TCR), α, can be calculated by equation (2.8).

$$\alpha = \frac{1}{R}\frac{dR}{dT} \tag{2.8}$$

$$\Delta V = I\Delta R = IR\alpha\Delta T \tag{2.9}$$

ΔV represents the change in voltage and ΔT shows the change in temperature. α is negative in semiconductors, while in metals, it is positive [36].

Figure 11 presents a simple schematic of a bolometer detector model. The bolometer connects with a heat sink through a thermal link. In the beginning, the bolometer and the heat sink are at the same temperature. The bolometer contains a sensing layer (normally a thin layer of semiconductor covered by a thin black layer to improve the radiation absorption) to absorb IR radiation, a germanium-based sensing layer is used in ref [36]. After absorbing the IR radiation, the temperature of the bolometer increases and thus leads to a change in the electrical resistance of the device [36].

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Figure 11: Simple thermal model of a Bolometer, which contains a thermometer with sensing layer, a thermal link, and a heat sink [36].

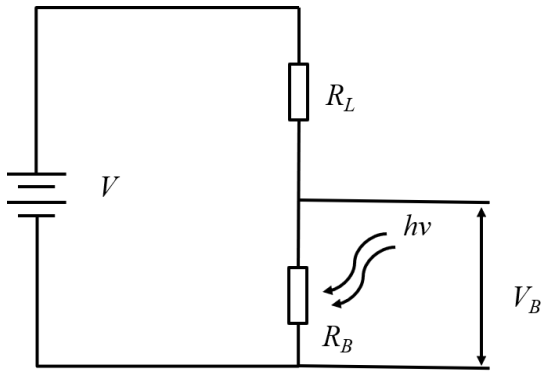

Figure 12: Bolometer biasing and readout circuit [46].

Figure 12 shows an example circuit used to measure the resistance of the bolometer. A biasing voltage V and load resistor R_L are connected to the bolometer (with resistance R_B) and the output voltage V_B of the bolometer can be measured [46]. Here the load resistance R_L needs to be much larger than the resistance of the bolometer to ensure the R_B has a negligible effect on the current through the bolometer [46] (a biasing circuit with a constant current source could be employed to avoid the use of additional load resistance). The bolometer resistance is Joule heated (which will lead to a temperature increase) when there is a current flow in the circuit. The temperature of the bolometer will change by ΔT when there is radiation falling on it, subsequently resulting in a resistance change in the bolometer [17]. After obtaining the resistance of the bolometer, the temperature change of the bolometer can be calculated.

In comparison to the thermopile, the bolometer's biasing circuit for temperature measurement, the external electric source and the additional load resistor used in the readout circuit increases the power consumption and response time of this detector.

2.3.2.3 Pyroelectric detectors

A pyroelectric detector exhibits spontaneous polarization, and this phenomenon is dependent on temperature. This property can be used in a pyroelectric detector to measure the temperature change induced by absorbing IR radiation [47].

Among the 32 known crystal classes, ten out of twenty-one noncentrosymmetric crystals exhibit temperature-related spontaneous polarization, in other words, the alignment of electric dipoles in the crystal domain [17, 48]. Electric dipole moment (electric dipole, a pair of equal and opposite charged charges, dipole moment $P = qd$, q is the magnitude of charge and d is the distance between the electric dipole) is produced along with a homogeneous change of the temperature in an insulating material, this property is called Pyroelectricity [47, 48].

Due to the internal depolarization field, free charges are neutralized when the crystal temperature remains unchanged and the existence of free charges compensate the electrical asymmetry [17, 47]. However, once the rate of free charges redistributes themselves slower than a rate of change in temperature applied to the materials, an electrical signal will be generated. For a pyroelectric detector, the relationship between the change in its output voltage ΔV and the change in irradiance ΔH can be described by the equation below [48].

$$\Delta V = \frac{R_T \Delta H A}{1 + j R_T \xi S_\omega A h} \; h\left[d(P_S/\varepsilon)/dT\right] \qquad (2.\ 10)$$

Where R_T is the thermal leakage to surroundings (W), A is the area (cm^2), ξ is the density (gm/cm^3), S is the specific heat (cal/gm°C), ω is the radian frequency (rad/s), h is the thickness (cm), P_s is the spontaneous polarization (C/cm^2), ε is the permittivity (F/m) and dT is the change in temperature (°C).

Compared to thermopiles and bolometers, pyroelectric detectors are alternating current (AC) devices as they only react to temperature changes instead of constant temperature levels [17, 38]. This property of pyroelectric detectors makes them less appropriate for low-frequency applications [17]. In addition, the charging rate of the input IR radiation should be similar to the electric time constant of the components for producing maximized output signal [17].

2.3.2.4 Diodes

A semiconductor diode is a device who's current can only flow in one direction with two electrodes. The anode (where the current enters a polarized electrical device) and the cathode (where current leaves a polarized electrical device) [49]. If the temperature of the diode increases, more charge carriers inside the device become free to move, which will decrease the bandgap energy and then reduce the forward voltage. If the voltage in the anode is larger than the voltage in the cathode, the diode is forward biased. Reverse bias occurs when the cathode voltage is higher than the anode voltage.

Diodes can be operated as a thermal detector because of their almost linear relationship between temperature (T) and forward voltage drop (V_F) when it is forward biased [50-52]. Equation (2.11) demonstrates this relationship.

$$\Delta T = K \times \Delta V_F + C \qquad (2.11)$$

K usually varies between 0.4 ℃/mV (for Schottky diodes) to 2 ℃/mV for semiconductor diodes. K and C are the constants determined by calibrating the diodes when it is driven by a constant current. ΔV_F represents the change of forward voltage. The slope of the V_F-T line determines the value of the factor K and can be calculated by

equation (2.11), according to the relationship shown in Figure 13. If the value of *K* is known for a diode, the temperature of the diode can be calculated.

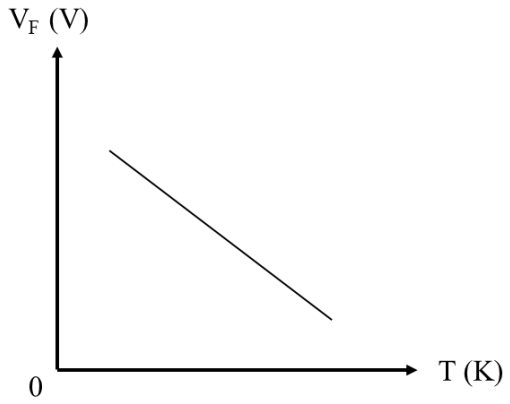

Figure 13: Ideal voltage temperature characteristic in forward bias region of a diode [53].

The advantages of using diodes as thermal detectors include a simple voltage temperature relationship, the ability of monolithic integration, very low cost of production and low complexity due to mature fabrication technology. Transistors, like a bipolar junction transistor (BJT), can also be used as thermal detectors due to the dependence of the base-emitter voltage V_{BE} to temperature (similar to the relationship between temperature and forward bias voltage from diodes) when the BJT is diode-connected (base and collector are shorted) [52, 54]. The issues involved in diode manufacturing, like the effect of material, geometric and process variations are removed when employing BJTs as on-chip temperature sensors [43]. In addition, a standalone diode might not be available in some CMOS design kits as they only apply the option of diode-connected BJTs [43].

2.3.3 Comparison of IR detector technologies

Compared to thermal IR detectors, photon detectors have better responsivity, lower

noise and a lower response time, but their limited spectral range and high cost make photon detectors unsuitable for many applications in daily life.

Thermopiles have reasonable responsivity, low noise, proper response time, good DC response and low cost. Compared to thermopiles, bolometers require external biasing current, while pyroelectric detectors suffer from poor DC response. In addition, bolometers are usually made up with non-CMOS compatible materials (like vanadium oxide, VO_x) which increases the cost as the requirement of special process for CMOS integration [17]. On the other hand, the low complexity and relatively good accuracy of diode thermal sensors make them one of the most popular temperature sensors to be employed in IC manufacture.

Table 1: Comparison of IR detector technologies

	Voltage Responsivity (V/W)	**Noise ($nVHz^{-1/2}$)**	**Response time (ms)**	**Spectral range (μm)**
Photonic [17]	–	–	$< 10^{-6}$	<3
Bolometers [55, 56]	>1000 *Depend on bias current	–	10	1 – 20
Pyrodetectors [34]	274 (25℃, 10Hz) *AC only	~12 (25℃, 10Hz)	150	1 – 20
Thermopiles [21]	58 (100℃, DC)	~38 (25℃)	~10	1 – 20
Diodes [57]	5.3 (500℃, 26Hz)	2 (500℃)	1.8	–

Overall, thermopile and diode thermal detectors can be considered to be the most cost-efficient uncooled IR detecting technologies.

2.4 Focal plane arrays

A FPA consists of an array (typically rectangular) of pixels located at the focal plane of an imaging system. It usually consists of one-dimensional ("linear") arrays and two-dimensional (2-D) arrays and is normally applied to the latter [17].

Thermal cameras can be built based on a thermopile array, which consists of multiple thermopile-based pixels for generating thermal images. Figure 14 gives an example structure of a pixel based on a thermopile. The cold junction is located at the substrate, which is used as a heat sink for heat dissipation and ensure the temperature of the cold junction remains unchanged. The hot junction is connected with an IR absorber, which heats up the hot junction when IR radiation is absorbed.

Figure 14: Example of the structure of a thermopile-based pixel [58].

Bolometers are also widely used in thermal cameras. Figure 15 shows a typical structure of a bolometer-based pixel [58]. The bolometer film is supported by two narrow legs.

The readout circuit is connected with the bolometer by the support legs. The IR reflector on the substrate and the IR absorber film on the bolometer form a resonant optical cavity (a set of optical ‘mirrors’ which allows the light to circulate in a closed loop) for IR absorption [58].

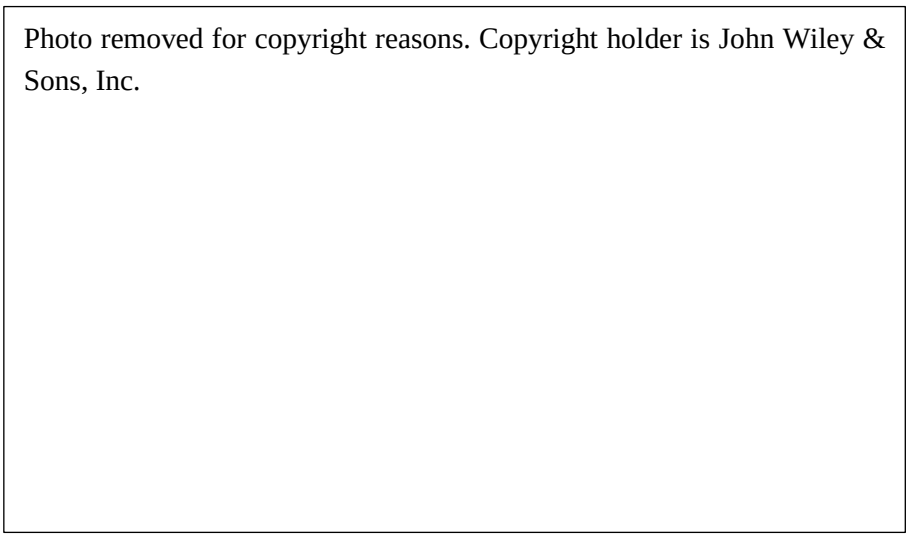

Figure 15: Example of the structure of a bolometer-based pixel [58].

Thermal cameras also can be considered detector array systems with an integrated readout circuit to process the signals generated from the pixel array. Figure 16 shows a typical circuit of a thermal camera (detector array). Each pixel comprises a thermal detector and a Metal-Oxide-Semiconductor Field-Effect Transistor (MOSFET), where the MOSFET is used as a switch to control each pixel’s access. The row multiplexer is implemented to select the row number of pixels. The integrator integrates the signal from the pixel and then transfers the signal to the row storage capacitors, then the signal can be selected and read from the output multiplexer.

To produce thermal images, thermal cameras employ IR detector arrays to convert thermal energy into electrical signal outputs. The electric signal is sent to a microprocessor by the sensor electronics and the output signal is subsequently amplified and converted from an analogue to a digital form. The microprocessor deals with the signals and maps the temperature from every single pixel into a thermal representation to produce the final thermal images [17].

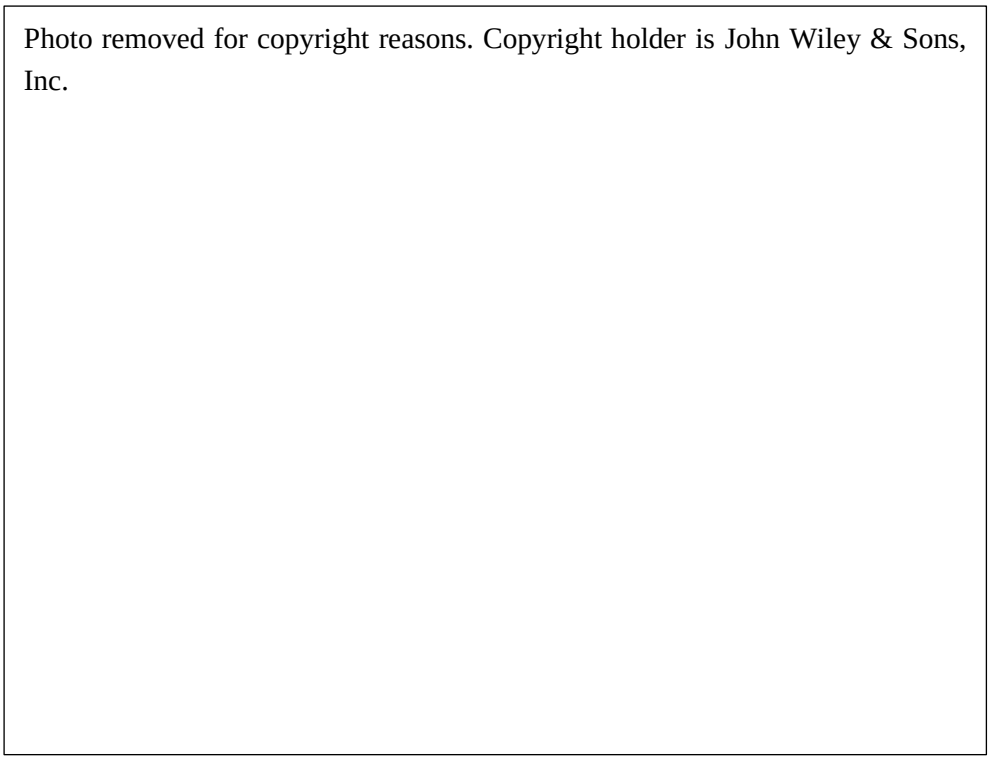

Figure 16: An example of the readout circuit for an IR detector array, adapted from [58].

Compared to state-of-the-art IR FPAs, our devices can be used in room temperature applications without cryogenic system equipped, e.g., FPAs based on photon detectors like [22] works well at an operating temperature of ~80 K and [23] works up to 185 K, both are much lower than room temperature (298K, 25℃) and require cooling system. In thermal detector FPA technologies, thermopile-based arrays respond to the temperature difference instead of an absolute temperature (the case in bolometers). Therefore, changes in substrate temperature have a minimal effect on device performance and thermopile IR FPAs can be implemented without stabilising the temperature of the device [58]. Moreover, thermopile-based arrays can operate without an optical chopper because it detects DC signals (pyroelectric detectors are AC devices) and there is no requirement for electric bias (the case in bolometer), effectively reducing noise and power consumption [17]. [24] introduced a ultra-small thermopile based array with pixel area of 100 μm × 100 μm, the pixel size is indeed smaller than our 8 × 8 FPA (pixel area of 150 μm × 150 μm, and for the 16 × 16 FPA is 75 μm × 75 μm), but their array only have 4 × 4 pixels and the voltage responsivity of 53 V/W is lower than our

devices (more than 70 V/W in the 8 × 8 FPA, introduced in details in section 4.3) and the pixel size of our arrays could be further scaled down (simulation results of smaller pixel size are presented in Chapter 6). [59] presented a thermopile-based array with 10 × 10 pixels with single pixel area of 250 μm × 250 μm and the crosstalk of this array was measured to be below 0.1%. However, this FPA use gold layers (CMOS-compatible W are used in our case) for heatsinking structures and gold is not fully CMOS-compatible which would require special process techniques and thus increase the cost and complexity of the fabrication.

2.5 Key characteristics of IR detector arrays

This section introduces the key aspects of IR detector arrays, which must be characterised when considering the performance of an IR detector array. As mentioned in Chapter 1, the performance of a thermal camera can be characterised by the following parameters: resolution, target temperature range, accuracy, spectral range, noise equivalent temperature difference (NETD), responsivity, and crosstalk. The following sections discuss responsivity, NETD, detectivity and crosstalk in detail.

2.5.1 Responsivity

In general, the responsivity of an IR thermal detector can be expressed in two ways: voltage responsivity and current responsivity [60].

The voltage responsivity (R_v) of a thermal detector can be defined as the change in voltage response (ΔV) due to the incident optical power (P_i) irradiated pixel, $R_v = \Delta V / P_i$ with the unit of volts per watt (V/W). Similarly, the current responsivity (R_i, which is usually applied to test the performance of pyroelectric detectors) is defined as the

generated current flow (ΔI) divided by the incident input radiation power (P_i), $R_i = \Delta I / P_i$, with the unit of amps per watt (A/W). The responsivity value used in this thesis is voltage responsivity.

2.5.2 Noise equivalent temperature difference

NETD is used to estimate the thermal sensitivity of a thermal camera i.e., the amount of temperature difference required to distinguish between noise and a small signal [17]. For instance, if the NETD of a thermal camera is 40 mK, this camera cannot resolve a useful thermal signal when the noise signal is equal to or lower than 40 mK. A camera with lower NETD can detect smaller temperature differences and generates images with higher quality. The NETD of a detector can be defined as the temperature changes in the device due to an incident IR radiation which is equal to the root mean square (rms) detector noise, see equation (2.13) [17].

$$NETD = \frac{V_n(\frac{dT}{dQ})}{(\frac{dV_s}{dQ})} = V_n \frac{\Delta T}{\Delta V_s} \qquad (2.13)$$

Where V_n is the rms noise, Q is the spectral photon flux density (photons/cm^3) incident on a focal plane array, and ΔV_s is the electric signal generated due to a change in temperature ΔT [17].

2.5.3 Detectivity

Before discussing detectivity, an important parameter of a thermal detector should be introduced, which is the noise equivalent power (*NEP*). The *NEP* is defined as the amount of incident power on the device which induces an output signal that is the same

as the rms noise output [17]. *NEP* is expressed as the ratio between the output electrical signal of the detector and the noise output, $NEP = V_{noise}/ R_V = I_{noise}/ R_I$, and the unit is watts.

The detectivity (D) is defined as the reciprocal of *NEP, D = 1/NEP.* It was discovered by Jones [61, 62] that the detectivity is proportional to the square root of the detector area (A_d) and electric bandwidth (Δf). Thus, a normalized detectivity D^* (or D-star) can be expressed as shown in equation (2.14):

$$D^* = D(A_d \Delta f)^{1/2} = \frac{(A_d \Delta f)^{1/2}}{NEP} \qquad (2.14)$$

D^* is treated as a key metric as it allows a comparison between the same type of thermal detectors with different areas [17].

2.5.4 Crosstalk

Another important characteristic of an FPA is the pixel-to-pixel crosstalk (C) (i.e., the unwanted transfer of signals between pixels [63]), which can affect the spatial resolution of the detector and thus complicate the reconstruction of the desired image [64].

For a thermopile array, C is defined as the ratio between the V_T signal generated by an optically irradiated pixel (V_{T1}) and that of an adjacent non-irradiated pixel (V_{T2}), i.e., $C = V_{T2}/V_{T1}$. In thermal FPAs, C is dependent on the inter-pixel heat diffusion [18] and is typically measured by optically irradiating (e.g., by a laser source [18]) a pixel and comparing its V_T signal to that of adjacent pixels [18,65]. However, imperfections in the laser focusing can lead to optical leakage from the laser spot, which can be challenging to control and/or quantify [18,65].

A different approach for C-measurement is to use an on-chip heater for thermal excitation [18]. However, this additional structure increases the fabrication complexity and may compromise the thermal performance of the device. In the later chapters of this thesis, a novel approach for measuring the crosstalk of a thermopile-based FPA without using a laser source, or an on-chip heater, will be introduced. This approach uses bi-directional electrical biasing of the thermopile elements themselves to obtain the thermoelectric voltages needed for crosstalk calculations.

2.6 MEMS technology

MEMS fabrication is a cost-effective technology and allows a significant reduction in device size. The development of MEMS technology also opens up the possibility of the integration of electronics with mechanical sensing elements on the same chip.

The integration of MEMS with CMOS on the same membrane (where devices are built in the chip) significantly reduces the size of devices (smaller packages and system), allows pre-amplification of the sensor signal, and reduces electrical connections between a mechanical device and its interface electronics (no connecting wires) [66, 67]. The connecting wire is one of the main sources of parasitic capacitance in chip fabrication, the existing parasitic components increase power consumption and influence signal quality [66]. Integration of sensors with electronics in the same chip significantly reduced the need for connecting wires. In this case, integration can reduce the noise from the interface circuit and cuts down the effect of parasitic capacitance [66]. Therefore, the quality of the signal is enhanced and signal to noise ratio is improved.

2.6.1 MEMS materials and processes

For MEMS devices, the properties of their thin-film materials are usually dramatically different from those materials in macro-form [67], this should be particularly considered when designing MEMS products. The difference is mainly owing to the diversity in the fabrication process of micro-scale and bulk materials [67]. The key parameters for characterizing a thin-film material for MEMS include density, Poisson's ratio, elastic modulus, electrical and thermal conductivity, fracture toughness, yield stress, and specific heat [67-70].

To integrate MEMS with ICs, three main conditions should be met [71]. Firstly, the materials and relevant processes should be compatible with the IC fabrication technology. Secondly, the MEMS materials should have desirable electrical and mechanical properties. Finally, the materials should always remain unchanged under any process (being freed or released), which means the process should always avoid building high-stress structures.

As the MEMS process also combines strengths from other microfabrication technologies, there are some fabrication processes and materials from MEMS that are unique when compared with conventional IC technologies [67]. Traditional CMOS materials include silicon, silicon nitride, silicon dioxide and aluminum. Its fabrication processes involve photolithography, dopant diffusion, thermal oxidation, chemical vapour deposition, evaporation, sputtering, wet etching, plasma etching and reactive ion etching [67]. In addition to these aspects of IC technology, MEMS includes materials such as Silicon carbide (SiC) and ceramics as high-temperature materials, lead zirconate titanate (PZT) as piezoelectric films, platinum, gold and plastics (e.g., Polyvinyl chloride (PVC)). MEMS also has additional fabrication processes such as deep reactive ion etching (DRIE), anisotropic wet etching, x-ray lithography and batch

micro assembly.

The same standard photolithography process is implemented in both MEMS and CMOS manufacturing, and it is one of the most crucial steps in fabrication as it allows for micro-scale and high-volume production [1, 67]. Figure 17 gives a schematic of a typical photolithographic process flow.

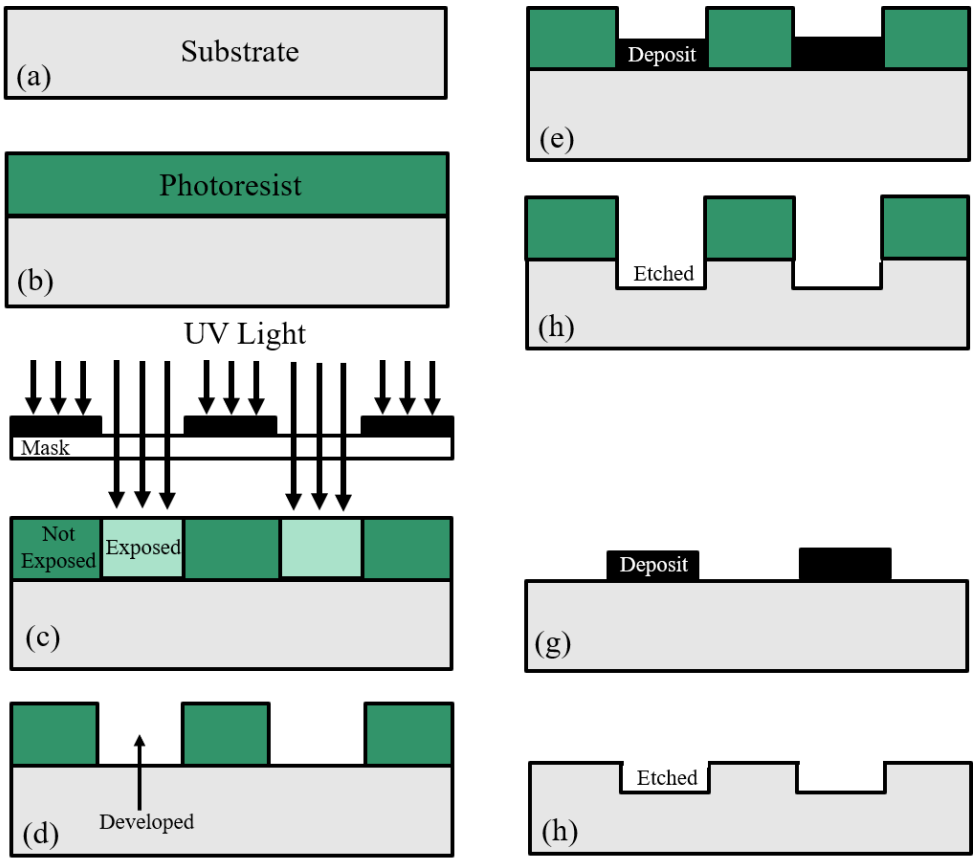

Figure 17: Schematic of the key steps in the photolithographic process [67]

Step (a) in Figure 17 shows the silicon substrate as the initial step. A photosensitive polymer (photoresist material) with a volume of a few ml^3 is placed on the surface of the silicon wafer. The polymer layer then becomes thinner by spinning the wafer at high speeds. Subsequently, the layer is baked and then forms a solid photoresist layer, as shown in step (b).

To produce the correct pattern to produce the required structure, a mask is designed.

The photoresist layer is selectively exposed to ultraviolet (UV) light through the mask. The characteristic of the polymer is changed by the UV light, which causes the exposed polymer to become dissolvable in dilute alkali (NaOH). This process is shown in steps (c) & (d). According to the different requirements in devices' structure, the silicon substrate is then deposited by materials such as silicon or ceramic (e) or etched (f). Finally, a solvent (e.g., acetone) is used to remove the photoresist layer and leads to a micromachined substrate, presented in (g) or (h) [67]. A detailed schematic illustrating the fabrication process of FPAs investigated here is presented in Chapter 4.

The bulk micromachining and surface micromachining illustrated in Figure 18 are the two main methods of producing MEMS systems [67, 69], and their detailed processes are outlined below.

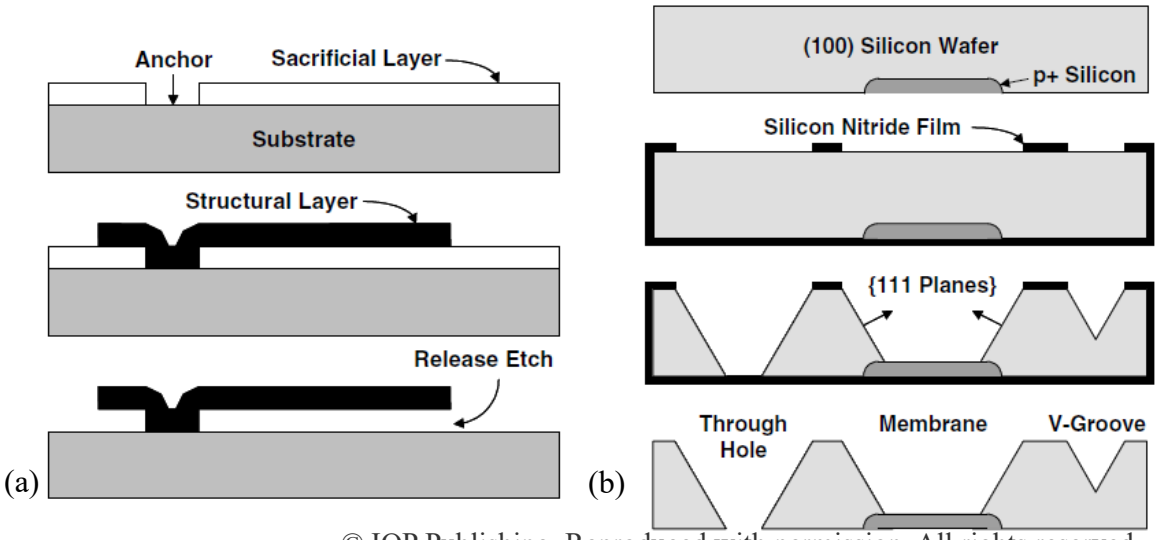

Figure 18: Main processes in (a) Surface micromachining and (b) Bulk micromachining [67].

The process of surface micromachining is shown in Figure 18a. In this process, consecutive thin films (silicon dioxide, polysilicon) are deposited, patterned and etched on the substrate, to form the structure of the devices [67]. In order to provide temporary support for the structure layer during device fabrication, a sacrificial layer (silicon oxynitride) is used. The sacrificial layer can be removed later by reactive ion etching

or wet chemical processes. The overlying layer on the sacrificial layer is called a structural layer, this is a layer of polysilicon and is deposited by chemical vapour at a temperature of about 200°C. To avoid the failure of device fabrication and to prevent the surface from cracking during micromachining, the mechanical properties of the sacrificial layer should have low-residual stresses and good adhesion among other characteristics [69]. In addition, to remove the sacrificial layer accurately without damaging the remaining structure, the etchants should have a great etch selectivity [69]. Surface micromachining has been used in a wide range of different applications and some devices are able to be fabricated commercially in large volumes (> 2 million parts per month) [67].

The fabrication flow shown in Figure 18b is the standard process of bulk micromachining. Compared to surface micromachining, which normally uses silicon substrates as a mechanical base with no technical function, the substrate of bulk micromachining usually implements single-crystal silicon. This substrate is patterned and shaped to be part of the technical structure of the final device [67]. In bulk micromachining, the region of the silicon substrate to be etched is defined by a thin film, normally silicon nitride. Compared to silicon, boron (P) doped silicon requires a 50× longer etch time, so it is always used as an etch stop. As shown in the flow graph, there are some regions in the substrate that are P+ (heavily P) doped, and the etch process will stop at this region. The etch stop can also be controlled by ‘timed stop’, which is defined as predicting the stop time for the etch process, but this method is not always accurate enough, especially for high-precision devices [72]. Wet etching and dry etching are the main techniques employed in bulk micromachining, and the type of etchants used will inform the choice. Wet etching mainly uses liquid etchants (mainly includes aqueous chemicals), and dry etching usually uses vapour and plasma etchants [69].

In bulk micromachining, many three-dimensional (3D) structures with high complexity and precision can be created, such as membranes, V-grooves, and vias [73, 74]. Figure

18b gives an example of a bulk micromachining based on a wet etching with an anisotropic etchant, this etching method is limited by the crystallographic directions [1, 67]. In our designs, a different etching approach is employed.

The array devices introduced in this thesis are fabricated on a Silicon-on-Insulator (SOI) CMOS process and followed by a DRIE to release the membrane. SOI devices are the fabrication of Si components separated to the Si substrate by an insulating oxide layer, which also acts as etch stop for etching techniques [75]. This technology allows the buried oxide layer to be employed as an effective thermal and electrical isolator between the silicon structures, thus significantly reducing interference from parasitic components [75]. The dry etch process, DRIE was invented by Robert Bosch Corp [76]. This etch method can be utilised in bulk micromachining for producing steep sides by vertical etching. In addition, the crystallographic orientation does not affect the result of DRIE. So, the practicality, feasibility and flexibility of bulk micromachining are significantly enhanced by using DRIE [67].

Currently, surface micromachining and bulk micromachining are both widely used in commercial device fabrication, such as sensors (thermal sensors, pressure sensors, gas sensors, etc.), and inkjet nozzles, as well as other devices [69]. However, the differences between these two techniques are narrowing. The invention of new etching approaches, such as DRIE, can take the advantage of both methods. This allows them to combine the optimal aspects of each technique, such as the comb structures from bulk micromachining and in-plane operation of surface micromachining [69].

2.7 Conclusions

In this chapter, the fundamental aspects of IR detection and MEMS technology are introduced. The IR spectrum with the relevant wavelengths of interests and their

applications were presented. Then the two types of IR detectors, photon detectors and thermal detectors were briefly discussed. Though the photon detectors show higher responsivity and faster response time, their high price and limits in spectral range make thermal detectors more suitable for daily life applications. Thermopiles, bolometers, pyroelectric detectors and diodes are the main categories of thermal detector. The physics and working principles of different thermal detectors are presented and thermopiles and diodes demonstrate advantages in lower power consumption and lower cost when compared to other thermal detectors. Furthermore, the fundamental physics and operation of FPAs were introduced and the main merits to be considered were explained.

For MEMS technology, the integration of CMOS and MEMS allows on-chip amplification, reduces chip size significantly and effectively enhances the quality of the signal. Although many materials and fabrication processes are commonly employed in both fields, MEMS requires additional materials and processes due to the requirements of devices. Therefore, the selection of materials and fabrication processes is always a challenge when designing a CMOS MEMS system. Photolithography is one of the key processes applied to both CMOS and MEMS production, which was discussed in detail. Surface micromachining and bulk micromachining are both widely used in commercial MEMS device fabrication. The basic processes of both approaches were introduced and compared. The creation of a new etching technique, DRIE, was able to take advantage of both methods and allows the combination of both methods when fabricating MEMS devices.

Chapter 3

The fundamentals of FEM simulations

3.1 Introduction

During the past few decades, the Finite Element Method (FEM) has widely become one of the most popular simulation technologies for solving engineering problems relating to fluid flow dynamics, heat transfer, electromagnetics, and structural mechanics, among others [77-79].

The established process of researching and developing complex engineering systems contains the following stages: design, modelling, simulation, analysis, prototyping, testing and, finally, fabrication (Figure 19) [77]. The development chart for complex engineering systems illustrated in Figure 19 demonstrates the many steps taken before the final production is commenced, the development process aims to ensure the feasibility of the engineering system and minimize the possibility of failure in the final products, while also reducing costs [77]. Processes are always iterative, meaning that some processes are repeated many times on the fundamental of the results from the current procedure, this allows for the design to be progressively tested and optimised to ensure the cost-effectiveness of the process [77]. Modelling and simulation techniques which allow for effective and accurate models to be produced are central to

the current research process, as an effective model can save time, materials and reduce the overall cost of the design and fabrication process. FEM is currently the main technique used to model products and systems [66]. Further details of FEM are discussed in the following sections.

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Figure 19: Process of the fabrication of an advanced engineering system, adapted from [77].

3.2 FEM simulations

FEM is a powerful tool that allows engineers to solve a multitude of problems. FEM can be applied to multiple types of engineering problems, supplying engineers with simulated distributions of key variables of interest, such as field variables for physical

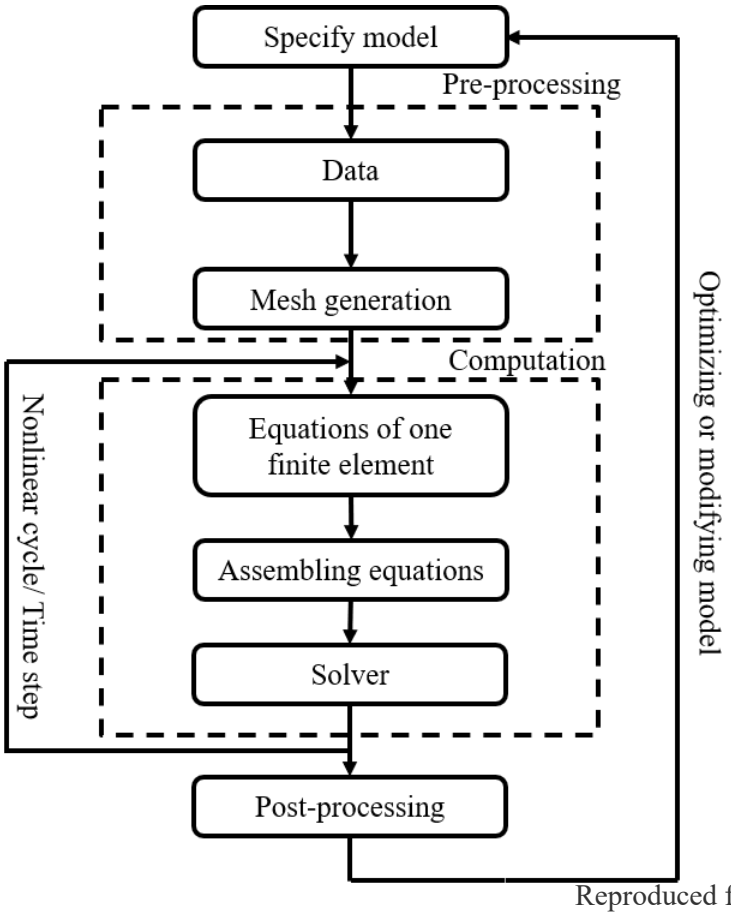
problem analysis, temperature or heat flow distributions for heat transfer analysis, electrical potential difference in electrical analysis, and flow velocity distribution in fluid dynamics problems [77].

FEM is a numerical technique that solves analytically difficult field variables by generating approximate solutions [77, 80]. In FEM, a continuous problem is divided into a finite number of smaller pieces (so-called elements). Elements are assigned by equations determined from required physical and mathematical principles [77, 78]. By doing this, difficult field variable problems can be transferred to a set of simple linear algebraic simultaneous equations to be solved for a complete geometry [77]. The solution of the complete domain is produced by assembling all of the elements following the same rules [77, 78].

The main process of FEM simulations are usually as follows (see Figure 20 for a flowchart of a basic FEM simulation process). The first part of the FEM process is pre-processing, in which the model is defined in accordance with the problem it is required to solve, pre-processing contains several steps: (1) The model needs to be modelled with geometry where unnecessarily complicated structures are simplified. As most physical structures are quite complex, geometry simplifications are crucial in simulation to reduce model complexity and computation time; (2) Decide on the materials to be used in the model according to the desired device; (3) Define the loads. This requires the definition of any external forces which may be placed on the device; (4) Define the boundary conditions. Boundary conditions are significant for accurate simulation. These conditions can be geometric properties such as points, lines, surfaces and solids, or some mesh properties like nodes and element edges; and finally, (5) Set up a mesh for model computation, this allows for the separation of the problem into a small finite number of elements for computation, the main concept behind the FEM technique. An appropriate mesh aids the accuracy and effectiveness of the computation [77, 80].

The second part of the FEM process is concerned with computation. To solve the problems, the FEM equations are assembled into a global system of algebraic equations (these are usually linear or nonlinear but linearized, decided by the medium to be considered) through the FEM mesh for the entire discrete domain and then subsequently solved by the solver [80]. Iteration would occur when the calculation includes nonlinear constitutive equations, which means the equation system is compiled in steps in order to reach convergence [80].

The final stage of FEM is post-processing. Once the solver gives the results, they are usually visualized as contour plots or graphs, which can be analysed by the user. The simulation results should then be validated with relevant literature or experimental data [77].



Reproduced from [80]

Figure 20: Flowchart of the FEM simulation process, adapted from [80].

Figure 21 shows an example of a mesh for an electronic component that is mounted on a circuit board by solder ball joints. It can be observed that different parts of the mesh are built using different mesh structures, and finer mesh is always established in the key structures while a simplified coarser mesh is built for the remaining structure, to save the computation time. Figure 22 shows an example of a visualized solution, demonstrating the temperature distribution in a heating circuit at a steady state. This model represents an electrically resistive structure placed on a glass plate. The white part of the image represents a higher temperature (compared to the temperature of the surrounding glass plate, which is mainly in red) which occurs when the circuit is Joule heated by an external voltage source. Through the strong contrast of the colours in the image, we can quickly and clearly obtain the temperature profile across the device and identify any potential problems and optimise the design. Figure 23 visualises streamlines which are coloured by the velocity magnitude of the flow through a pipe elbow. From the colour legend, we can easily identify how the velocity changes as fluid flows through the pipe structure. The highest velocity occurs around the corner bend and is represented in red. These model outputs (Figures 21, 22, and 23) demonstrate some basic and clear visualisations which can be produced using FEM software.

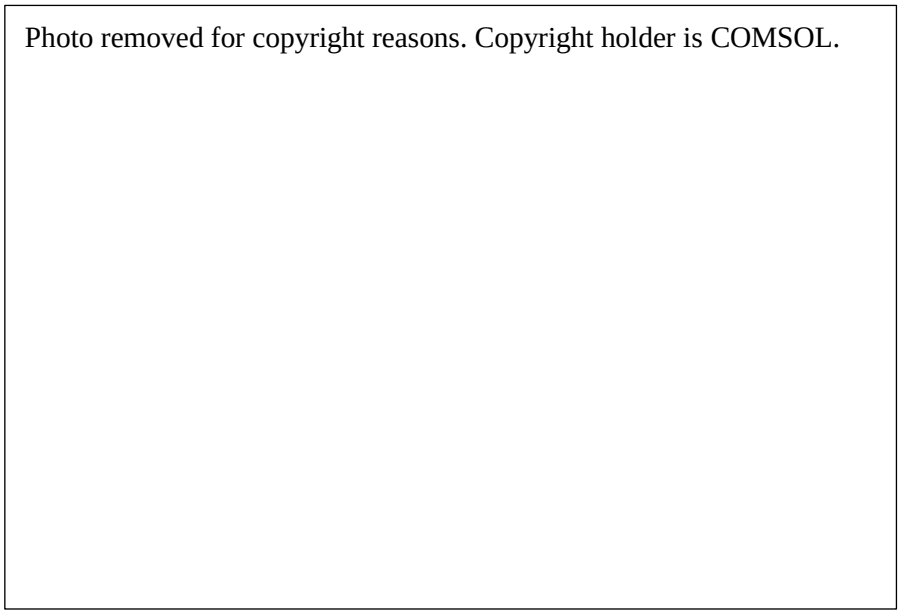


Figure 21: Mesh of an electronic component that is mounted on a circuit board by solder ball joints built by COMSOL, from COMSOL model examples [81].

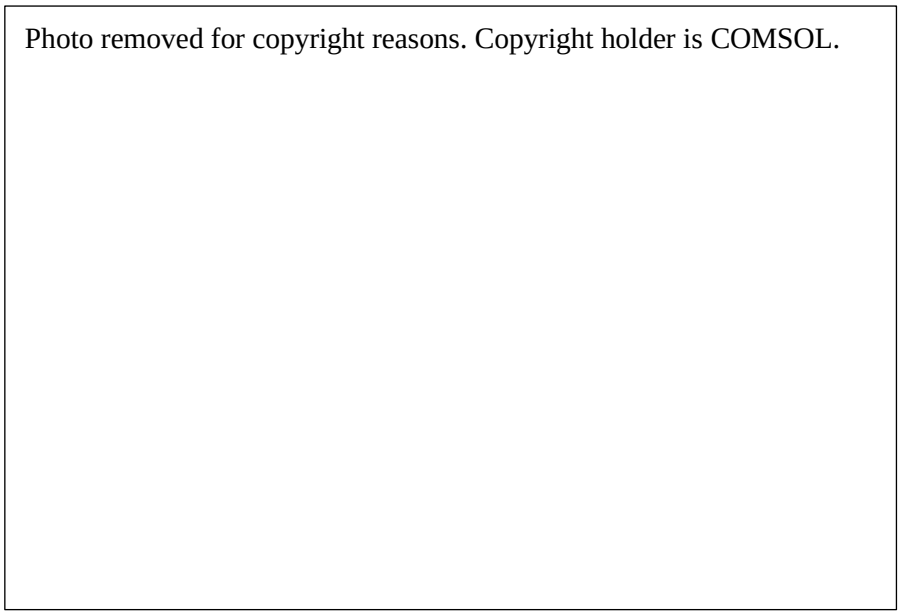


Figure 22: Temperature distribution in a heating circuit at steady state solved by COMSOL, from COMSOL model examples [81].

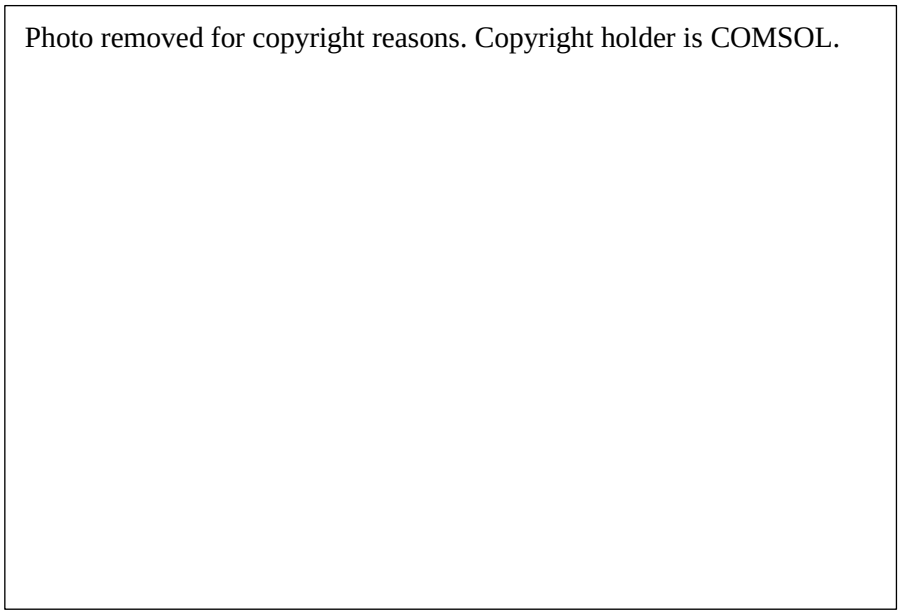


Figure 23: Streamlines coloured by the velocity magnitude of the flow through a pipe elbow, from COMSOL model examples [81].

3.3 1D, 2D and 3D solid elements simulation

One-dimensional (1D) elements, two-dimensional (2D) elements and three-dimensional (3D) elements are the main categories of the elements in FEM simulation. In this section, the main properties of three types of FEM solid elements are introduced and compared.

The shapes of 1D elements are normally straight or curved lines, they are the simplest of the elements. 2D solid elements are plane elements that can be formed with straight or curved edges. The shape of 2D elements can be triangular, rectangular or quadrilateral [77, 82]. Engineering related problems usually implement line elements with straight edges [77]. The 2D model is defined with the x-y plane, which means the displacement and any external forces of the model has components in x and y directions [77].

3D solid element simulations are defined in x, y and z directions, which includes all three physical components, therefore 3D elements are known as the most general element in modelling. In accordance with the real devices, 3D solids can be defined as having any shape, material property and boundary condition [77]. The shapes of 3D elements can be tetrahedrons or hexahedrons with flat or curved surfaces [77, 82].

Figure 24 illustrates several examples in 1D, 2D and 3D element geometries. Compared to 3D elements, the simulations built based on 1D or 2D elements require significantly less computation time and complexity [77]. 3D element modelling could be quite challenging for geometry set-up, meshing and computation, and it also requires hardware facilities of a greater specification. Therefore, generally, 2D or 1D elements are preferred when the structure is able to be simplified and established within a proper tolerance for numerical modelling [77].

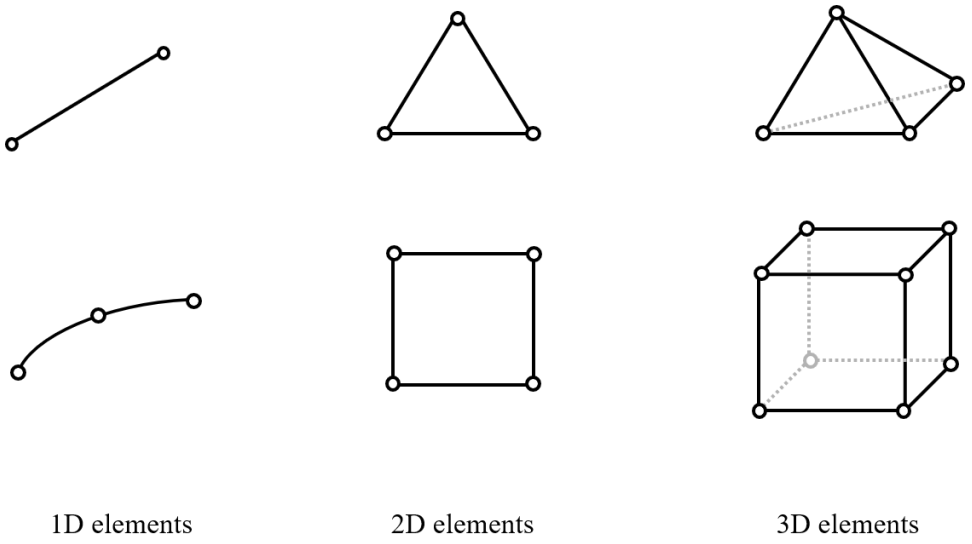


Figure 24: Examples of typical 1D, 2D and 3D elements geometry in FEM simulation.

Due to the asymmetry and complexity of the structure of the original chip design in this project, 1D and 2D modelling are not appropriate for accurate simulation of the devices introduced in this thesis. Although the simulation model built in this project uses 3D elements, several reasonable simplifications are implemented to the model geometry to reduce the meshing complexity and computation time.

Triangulation, i.e., the use of triangular elements, is the most efficient and mature method for building meshes, and this method can be completed almost automatically for establishing 2D and/or 3D meshes [77]. Because of this, triangulation can be found in most simulation tools. Moreover, the ability to fit triangle elements to almost any complex geometric shape and boundary gives them a further advantage over other 2D/3D. Triangle elements can be easily fitted to adapt into sharp corners of a required shape, whereas, attempting to implement quadrilateral elements to achieve the same result may seriously affect the shape of the element [77]. However, compared to results computed based on quadrilateral elements, the simulations using triangular elements show less accuracy [77].

3.4 Choices of software: Comsol Multiphysics vs Ansys

Comsol Multiphysics and Ansys are commercially available FEA simulation tools, and both are popular in academic and industrial research. For simulating the thermopile based FPA devices in this project, heat conduction and the Seebeck effect are the two main physics to be considered. In this case, those physics and their coupling physics need to be simulated accurately by the FEA tool.

Deepti et al., (2010) present a critical comparison of Comsol Multiphysics and Ansys [83]. The authors indicate that simulation results from the two software packages applied to the same problem show a good level of agreement (5-13% variation) and both tools have the proven ability to accurately simulate and solve Multiphysics problems [83].

Compared to Ansys, Comsol is more accurate in simulating Multiphysics problems and features, as it is more flexible in the model set up when coupling different physics, although it may require more hardware memory for computation. Whereas Ansys always needs to couple incompatible physical modules for load transfers between them [83]. In addition, Comsol gives high flexibility in user defined PDEs for solving specific problems whereas Ansys might be less flexible. Comsol Multiphysics was chosen to simulate the device in this thesis, as coupling Multiphysics was important for solving thermoelectric problems.

3.5 Physics and boundary conditions

To accurately simulate the physics involved in the FPAs investigated in this project, the electric currents module, heat transfer module and their coupling physics from COMSOL are used. More details about the model physics are introduced in the following sections.

3.5.1 Heat transfer

Joule heating (also known as ohmic or resistive heating) is one of the main physics to be considered here, as the device is heated by an external current source with power equation, $P = I^2R$, R is the resistance. Joule heating describes the process of the heat generated when an electric current passes through an electric conductor, see equation (3.1).

$$Q = \mathbf{J}\,(-\nabla V) \qquad (3.1)$$

In equation (3.1), Q represents Joule heating with unit W/m^3, J (A/m^3) is the current density and V is the electric potential.

To investigate the heat transfer in the device, heat conduction in solids is the main area of physics to be understood. There are three types of heat transfer: heat conduction, convection and radiation. Heat convection usually describes the process of heat escaping from the surface of an object via a fluid flow, such as the movement of air or water. Thermal radiation is the phenomenon that all objects with a temperature higher than absolute zero can generate electromagnetic waves, and this can happen without any additional medium [84]. Heat conduction is the process of thermal energy being transferred within a body due to the movement and collision of microscopic particles

[84, 85]. These microscopic particles could be molecules, electrons or atoms [85]. The kinematic and potential energy of microscopic particles is included in thermal energy [85]. Heat conduction follows Fourier's law (the heat transfer rate in a device is negatively proportional to the gradient of temperature along an axis), which is expressed in equation (3.2).

$$\mathbf{q} = -k\nabla T = -k\frac{\partial T}{\partial x} \tag{3.2}$$

Where **q** represents the energy flux, its unit is W/m^2, k is the thermal conductivity ($W/(m\cdot K)$) and T is the temperature. To consider a 3D simulation model, the Fourier's law can be expressed under a Cartesian coordinate system as follows in equation (3.3) [84],

$$\mathbf{q_x} = -k_x\frac{\partial T}{\partial x},\ \mathbf{q_y} = -k_y\frac{\partial T}{\partial y},\ \mathbf{q_z} = -k_z\frac{\partial T}{\partial z} \tag{3.3}$$

Where $\mathbf{q_x}$, $\mathbf{q_y}$, and $\mathbf{q_z}$ are the rate of heat transfer, k_x, k_y, and k_z are the thermal conductivity coefficient along x, y, z axis and $\frac{\partial T}{\partial x}$, $\frac{\partial T}{\partial y}$, and $\frac{\partial T}{\partial z}$ are the temperature gradients along the x, y, z axis of the Cartesian coordinate system [85].

3.5.2 Seebeck effect

The Seebeck effect was discovered by Thomas Johann Seebeck in 1821, it describes the phenomenon that a potential difference is generated when a temperature gradient is placed at the junctions of two dissimilar electric conduction materials [40].

Figure 25 illustrates the Seebeck effect that occurs in silicon, where the two conductors are p doped and n doped silicon, respectively. With the joint end of two conductors

placed in the hot region and the open end placed in the cold region, the electrons in the n doped silicon and holes in the p doped silicon diffuse from the hot end to the cold end, leading to the generation of a thermoelectric voltage at the open end. Figure 26 gives an example thermopile built based on the thermocouple shown in Figure 25

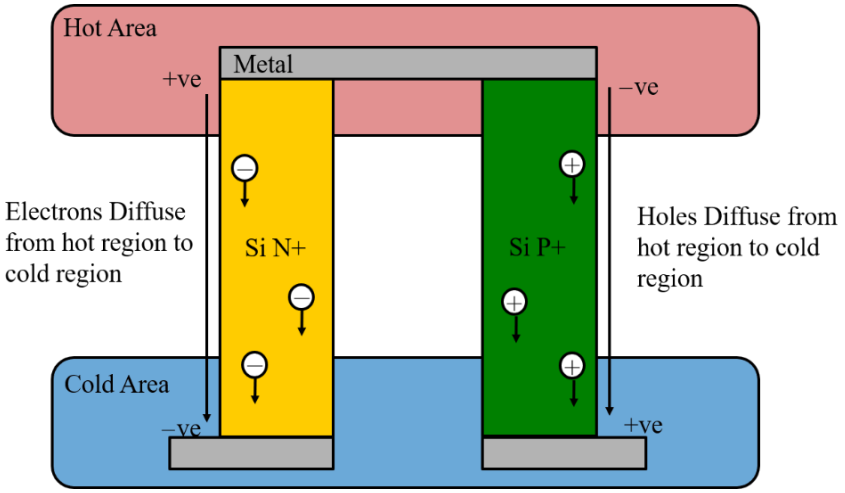


Figure 25: An example of the Seebeck effect in Silicon, this process also occurs in other materials.

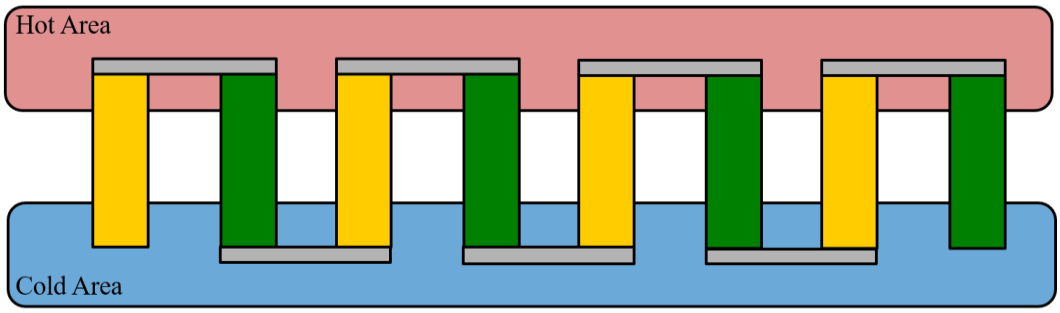


Figure 26: A simple schematic of a thermopile, it is composed of a series of thermocouples shown in Figure 25, which can increase the total voltage.

To implement the Seebeck effect in simulation, the physical module in Comsol, electric currents, is implemented. The equation regarding the Seebeck coefficient is introduced in Chapter 2 as $\Delta V = \alpha \Delta T$ (α is the Seebeck coefficient), and it works with Ohm's law as shown in equation (3.4). The final expression regarding current density is implemented in the boundary conditions, external current density, in x and y direction

(z-direction can be neglected to reduce the computation complexity as the thickness of the thermocouple leg is negligible when compared to the length and width).

$$\begin{cases} \Delta V = \alpha \Delta T \\ V = IR = I \cdot \rho \ \frac{l}{A} \\ I = JA, \rho = \frac{1}{\sigma} \end{cases} \quad (3.4)$$

Thus, the following expression about current density **J** can be obtained, here the unit length is considered, so the l is ignored in the final equation (3.5).

$$\mathbf{J} = -\alpha\sigma \nabla T \quad (3.5)$$

Where **J** is the current density (A/m^2) and σ is the electrical conductivity (S/m).

3.5.3 Single thermocouple simulation set-up and results

To verify the feasibility of the physics related to the thermoelectric effect introduced in the previous sections, a simple model for simulating a single thermocouple is established in COMSOL Multiphysics.

As shown in Figure 27, this simple thermocouple is composed of p doped and n doped silicon legs with tungsten (W) interconnections at the joint end of the device. The width of each single silicon leg is 5 μm, the total length is 600 μm and the thickness is 0.25 μm. The thickness is set to be the same across the whole device. The Seebeck coefficient of the p doped silicon (α_p) is 163.5 μV/K and the n doped silicon (α_n) is -117 μV/K. The temperature of the joint end (also known as the hot junction) is set to be 120°C and the open end (cold junction) is set to be 20°C, thus the temperature difference (ΔT) is 100°C.

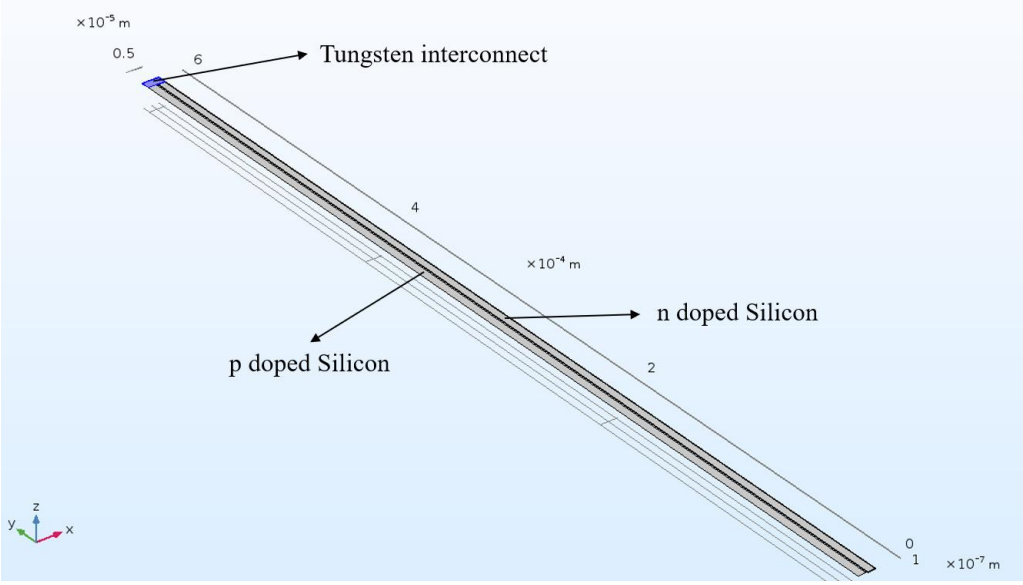


Figure 27: The structure of a simple thermocouple, formed by p doped and n doped Silicon, with W as the interconnection metal.

Figure 28 visualises the result of the temperature distribution across the thermocouple with white representing the hottest end and red representing the coldest end. It can be clearly observed that the temperature decreases gradually from the hot junction (more than 110℃) to the cold junction (about 20℃).

The inset in Figure 28 shows the mesh of the circled part of the device, as the structure of the thermocouple at this point is two identical strips (except material), the mesh can be considered as evenly distributed throughout the device.

Figure 29 presents the voltage difference generated due to the Seebeck effect in this thermocouple using a range of warm and cold colours, the warmer the colour the higher the voltage. The surface of the open end of the n doped Si leg is defined as the ground, thus its voltage is shown as 0 V in the figure (shown in blue). The voltage increases gradually from the ground to the surface of the open end of the p doped Si leg, here the colour in blue represents 0 V and red represents the highest voltage. By checking the voltage output from the surface of the highest end, the thermoelectric voltage generated

by this thermocouple, due to the applied temperature difference, can be obtained from this simulation model. The simulation results can be compared with the theoretical results.

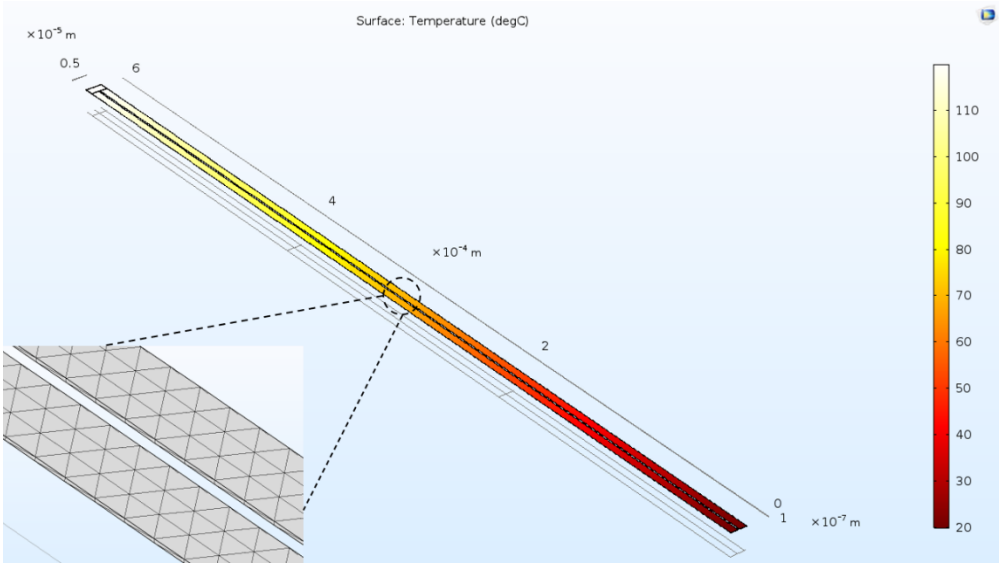


Figure 28: Temperature distribution of a single thermocouple with inset shows a part of the mesh built in this device.

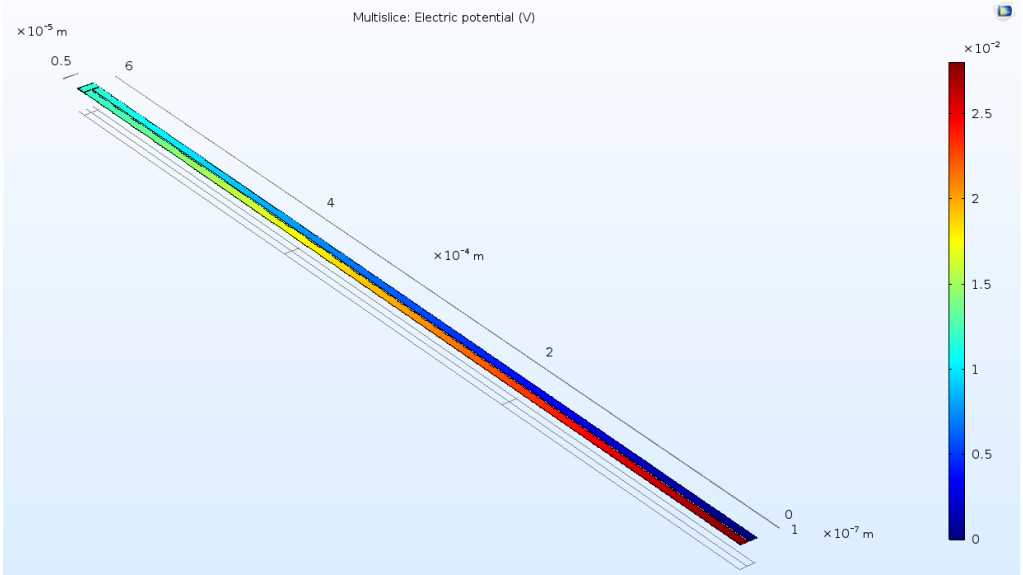


Figure 29: Electric potential distribution of a single thermocouple.

According to the provided parameters, the thermoelectric voltage of this model case can be calculated using the basic equation defining the Seebeck effect (equation (2.4)

from Chapter 2). Therefore, the thermoelectric voltage generated by this thermocouple under the temperature difference stated here due to the Seebeck effect should be 0.028 V. This is the same as the result obtained from the simulation model. In this case, the physics setting which models joule heating and the Seebeck effect can be assumed to be working correctly.

3.6 Conclusions

The fundamental theories of FEM simulation are introduced in this chapter. To further understand the physics and effectively improve the performance of our FPA design, FEM based simulation tools could be employed. FEM is a mature and popular simulation technique for solving engineering problems. The merits of utilizing 1D and 2D finite elements for modelling includes less computation complexity and time. These models can also be run without consuming too much device memory. However, 3D elements were chosen for the simulations in this thesis because the structure of the original chip design is asymmetric and complicated. Triangulations are the most common shape of elements when building meshes, either in 2D or 3D models. However, it usually generates simulation results that are less accurate than models using quadrilateral elements. The models presented in this thesis are established in Comsol Multiphysics. Heat transfer, electric current modules and coupling modules are implemented for simulating heat conduction and thermoelectric physics in the thermopile-based array device. To validate the conditions which are presented in the simulation, a simple model with a single thermocouple was built, and its thermoelectric voltage result was obtained. The thermoelectric voltage value given by the simulation shows a good agreement with the value derived from the fundamental theory.

Chapter 4

Thermopile arrays - Experimental Methods

4.1 Introduction

This chapter introduces the fabrication process for thermopile array chips, mainly focusing on the structure of the 8×8 and 16×16 array designs. To check the basic performance of the devices, the experimental set-up and a bi-directional electrical biasing approach for thermoelectric signal and crosstalk measurements are depicted. Finally, a thermopile array system that implements the 16×16 array chip is demonstrated for gesture recognition and people counting applications.

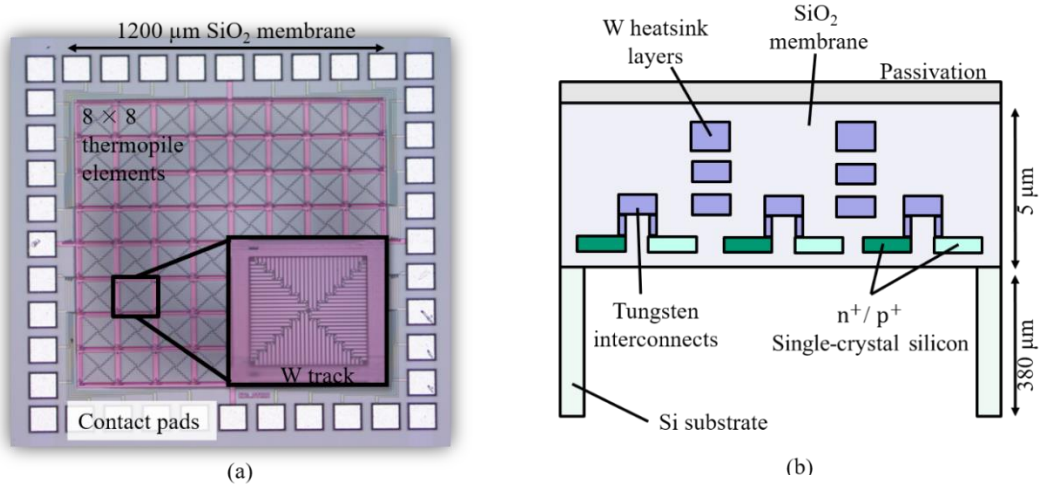
4.2 Thermopile arrays

4.2.1 Fabrication

This section introduces the main fabrication technologies used in the chips tested in this thesis. The chips used in this project were fabricated based on MEMS technology, and

electronic circuits were integrated with the same chip to control the thermal detectors (except the chip with an 8×8 array, which has no circuit included).

The chip size of the device is 1.76 mm × 1.76 mm (see Figure 30a for an optical top-down view of the chip, taken using a microscope). The enlarged section in Figure 30a gives a clearer view of the structure of a single pixel, with surrounded by W tracks. The layout design was carried out using the CADENCE Virtuoso design platform. The chips were fabricated on SOI wafers. The design of SOI wafers is based on a sandwiched structure, made up of a buried oxide (SiO_2) layer placed between a thin silicon layer and the silicon substrate.



Reproduced from [87]

Figure 30: (a) Optical image of the 8×8 thermopile array with a magnified image (colour-shifted) of an individual pixel. Chip size = 1.76 mm × 1.76 mm. (b) Cross-sectional view of the numerical model (not to scale) showing the single-crystal Si p^+/n^+ elements and W layers of the thermopile array.

This single membrane detector array was fabricated using a commercial 1 µm (SOI)-CMOS process on 6-inch SOI wafers. The pixels were formed using highly doped p^+ and n^+ single-crystal Si layers which formed within the SOI layer. The interconnects between the Si p^+ and n^+ elements, and the heatsinking tracks between the pixels are formed by three W layers, with track widths of 20 µm and a total thicknesses of ~ 1 µm.

W was chosen here as it can be implemented in a standard high-temperature CMOS process and has a much higher thermal conductivity (~80 W/mK) when compared to that of silicon dioxide (SiO_2, ~0.8 W/mK) which is the main material making up the chip membrane. In this case, layers made of W are highly suitable for effective heat dissipation.

The SiO_2 based membrane has an area of 1200 μm ×1200 μm (the area of a single pixel is 150 μm ×150 μm) and thickness of ~5 μm, see Figure 30b. The layers were grown on a 380 mm thick Si substrate which is back etched using DRIE to form the membrane, with the first SiO_2 layer acting as an etch stop. Devices with array sizes of 8×8 and 16×16 pixels were fabricated as a proof of concept. In the 8×8 array design, each individual pixel comprises 52 series-connected thermocouples with their cold junctions placed close to the surrounding heatsinking tracks (20 μm width), formed by the three W layers. For the 16 × 16 array design, it has the same membrane dimension and materials with 8 × 8 array, with the heatsinking track widths of 10μm and each pixel consists of a thermopile with 36 thermocouple pairs. The detailed fabrication process is outlined in Figure 31.

Figure 31: The schematic process flow outlining the fabrication process used for our device. The process starts with an SOI structure with a buried layer placed between a thin silicon layer and the silicon substrate. The top silicon layer is etched to form the required patterning. Then the silicon structure is implanted to form the p+/n+ structure and a silicon dioxide layer is deposited on top. With the formation of the contact metal and three layers of heatsinking metal tracks, a layer of passivation (Si_3N_4) covered the entire chip to protect the device from the environment. Finally, the chip is completed with the back-etch by DRIE to release the membrane.

4.2.2 Pin-out diagrams

In this section, diagrams of the chip layout with marked pins (Figure 32 and Figure 35) are outlined and described.

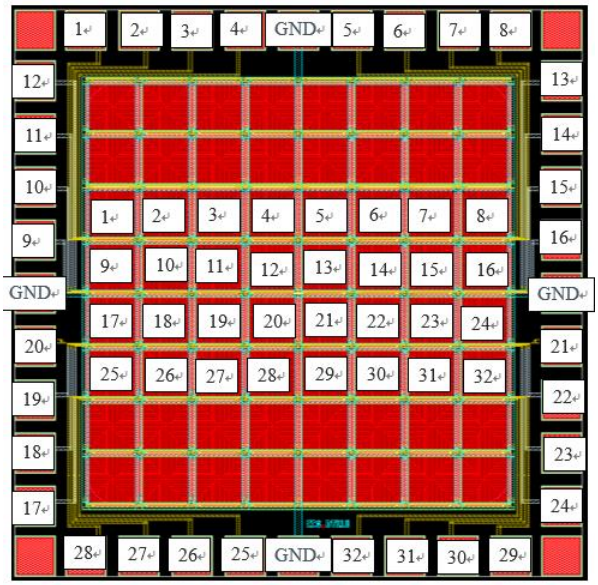


Figure 32: Chip CCS_DTA 18, numbers from 1-32 on the output pins are the Output (V) from the pixel (thermopile) with the same number, GND represents ground

The chip shown in Figure 32 is a CCS_DTA 18[1]. The name of the chip is derived from the abbreviation of "Cambridge CMOS Sensors Detector Thermopile Array", followed by the number of the chip. As there is no circuit built into CCS_DTA 18, only 8×4 pixels are readable.

There are in total 8×8 pixels of thermopiles designed in this chip, however, only 8×4 of the pixels are bonded out due to the limit in pads. Therefore, the thermal images obtained by this design only include 32 pixels. The numbers in the middle four lines of the chip (Figure 32) indicate the output-available thermopiles, and their output can be read from the pads labelled with the same number. The pin 'GND' (ground) needs to be

[1,2] Dr. S. Z. Ali from Flusso limited, Cambridge, designed these chips.

connected to the ground.

In order to produce thermal images with higher resolution, the Chip CCS_DTA 22[2] with 16×16 pixels was designed, where each pixel consists of 36 pairs of thermocouples. To enable all pixels, a new schematic with an electronic circuit integrated on the same chip was applied, which utilises MOSFETs and multiplexers. When the gate-source voltage of the MOSFET reaches 5 V, the MOSFET is turned on and its related thermopile can be enabled.

This design also features a differential output mode for reducing the noise level, as explained in Figure 33. In a differential signal mode, the input signal is converted into a pair of signals which have the same amplitude but opposite direction. The output signal is obtained from the subtraction of the pair of signals. In this case, if a noise is introduced to the signal, it will be added to both positive and negative signals and cancelled after the subtraction [86]. Figure 34 shows the differential circuit implemented in our chips. Figure 35 presents a pin-out diagram of an array with 16×16 pixels for the chip CCS_DTA 22.

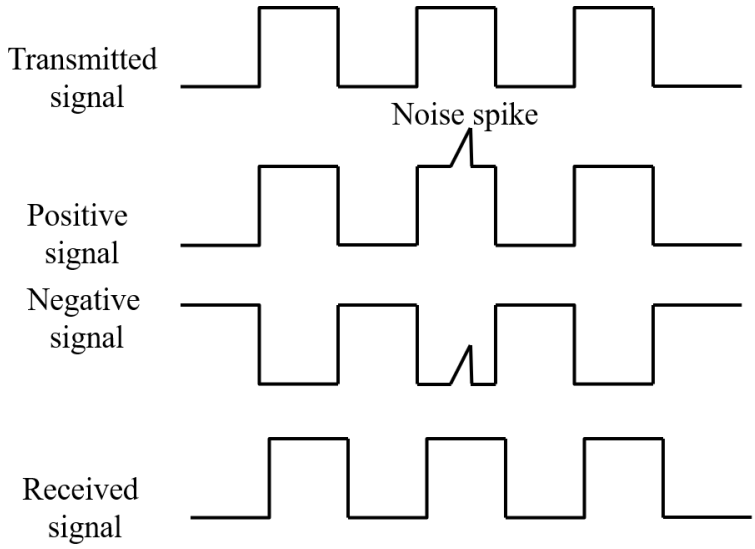


Figure 33: Differential signal mode, when a noise is introduced to a differential signal. circuit, it will be cancelled after the signal subtraction [86].

[1,2] Dr. S. Z. Ali from Flusso limited, Cambridge, designed these chips.

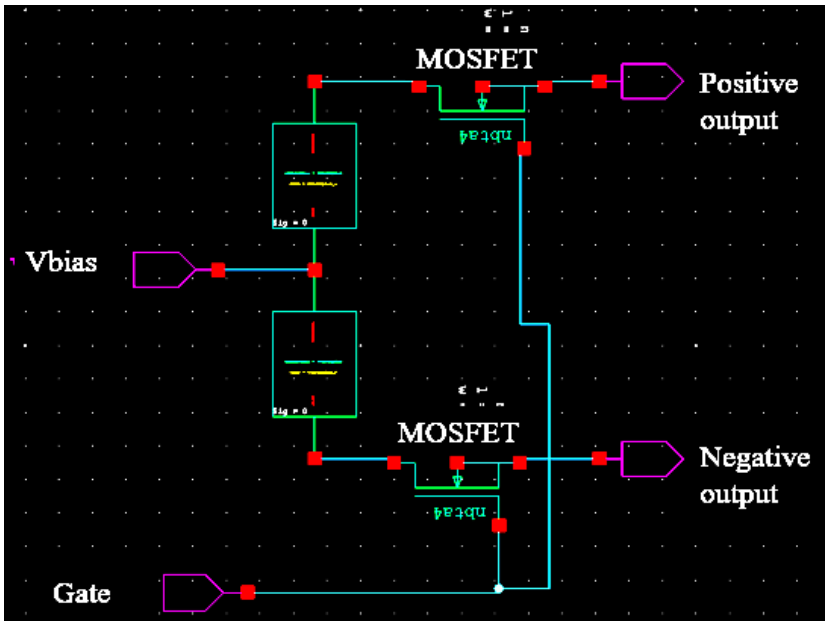


Figure 34: Circuit schematic for chips with differential output, shows the connection between thermopiles and MOSFETs for differential signal output. The positive and negative outputs along with the gate control of the MOSFET can be found on the circuit.

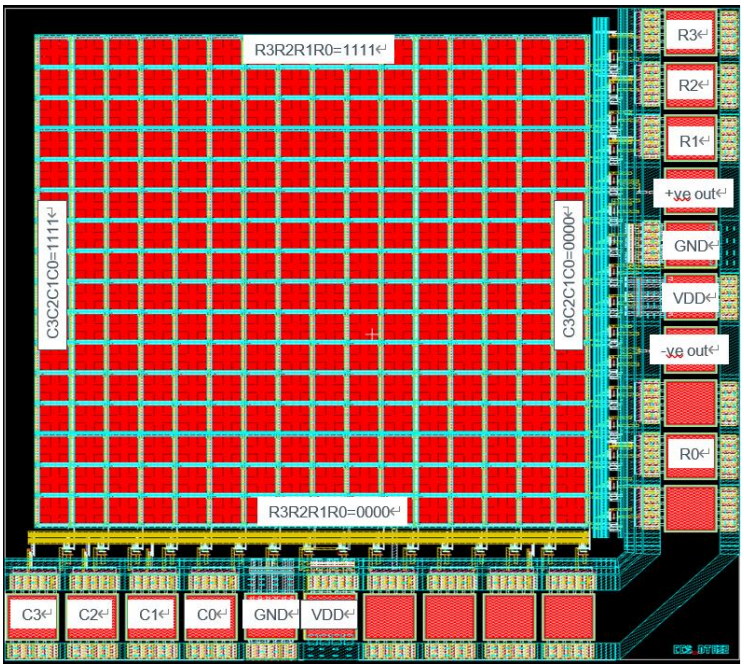


Figure 35: Chip CCS_DTA 22 with pin C3-C0 enable column 0000-1111 and pin R3-R0 enable row 0000-1111, pin VDD for ESD circuit and GND is ground, +ve Out is the positive thermopile output and -ve Out is the negative thermopile output.

[1,2] Dr. S. Z. Ali from Flusso limited, Cambridge, designed these chips.

Chip CCS_DTA 22 features 16×16 pixels of thermopiles, along with a 4:1 multiplexer to choose the specific column/row. In Figure 35, the pins on the bottom side of the chip 'C3 C2 C1 C0' were used to select the input of the column multiplexer. C3 is the most significant bit (MSB) while C0 is the least significant bit (LSB). For instance, the signal from the leftmost column is selected when the value of 'C3 C2 C1 C0' is set to 0000 and the rightmost column is selected when 'C3 C2 C1 C0' is 1111. The marked pins shown on the right side of the chip in Figure 35 are the inputs of the row multiplexer. Similarly, the labels of 'R3 R2 R1 R0' are implemented to select a row. R3 represents the MSB and R0 is the LSB. For example, the bottommost row can be selected to be read when the number of 'R3 R2 R1 R0' is set to 0000. The input pin 'C0' can be set to '1' by applying 5V to the pin.

As the output signal in the chip CCS_DTA 22 is in a differential mode, the '+ve out' in the diagram represents the positive output signal and the '-ve out' represents the negative output signal. Electrostatic discharge (ESD) pads were implemented in the pin pads of CCS_DTA 22 for preventing static charges, which could be fatal for the chip. For example, if the human bodies capacitance is 100pF with about 0.6μC charge stored in it, the resulting electrostatic voltage is $V = Q/C = 6kV$, which is much higher than the operating voltage (5V) and it will likely damage the chip.

Figure 36 shows a basic ESD circuit. The voltage drain (VDD) pin in the chip is the VDD in the circuit, which should be enabled by 5V. The two diodes are not conducting (reverse biased) when the input signal is not in excess of the thermopile operating voltage (5V). Once an electric signal larger than the operating voltage occurs at the ESD pad, the top diode will conduct (forward biased). Similarly, once the signal is lower than -5V, the bottom diode will conduct. In this case, the over-range signals can be effectively restricted by the ESD circuit.

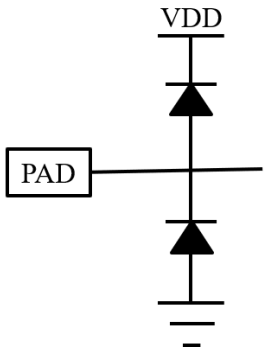


Figure 36: ESD protection circuit showing the basic components for reducing static charges, diodes are normally reverse biased.

4.2.3 Experimental set-up

Figure 37 presents the basic set-up of the experiments and a microscope view of the probe station when undertaking experiments with chip CCS_DTA 18. The voltage/current sources used to enable the chip and output voltage measurement is conducted by an electric measurement source meter, Keithley 2401, which can be used as both a power source and an electrical measurement device for V(voltage), I(current), P(power).

A schematic of the wire connection is shown in Figure 37a. Pixel no.21 (the heater pixel, inside the green square) is heated using a current source provided by SourceMeter 1, and its output voltage is also measured by SourceMeter 1. Simultaneously, the induced signal from pixel no.22 (the test pixel, inside the black square) is measured by SourceMeter 2 (with no current/voltage source connected). Here pixel no.21 is treated as the IR source and powered by an external current source. As shown in the graph, two pixels connect to separate ground pads, which can effectively reduce the influence of current leakage when using a common ground. Figure 37b gives an example set-up of the probe station with the microscope turned on and Figure 37c presents a microscope view of the device CCS_DTA 18 when there are three probes contacting the pads.

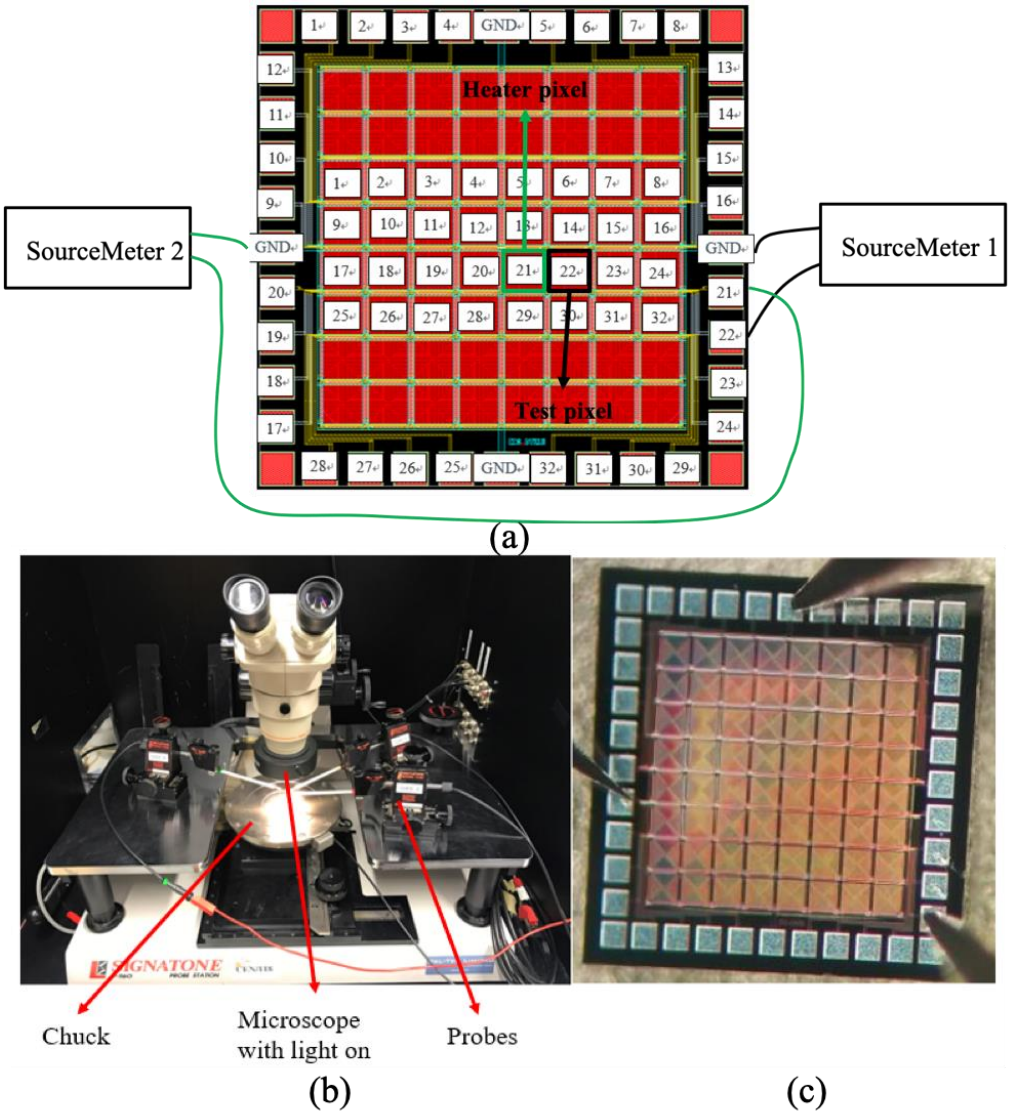


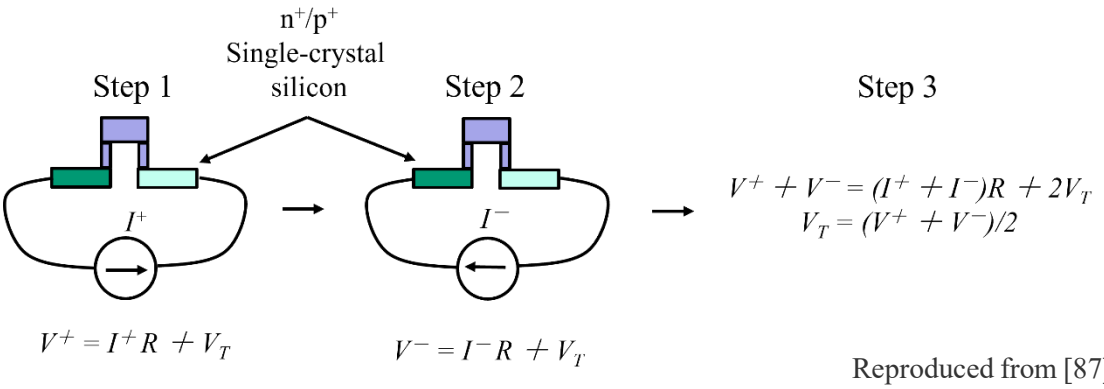
Figure 37: (a) Wire connection schematic for chip measurements (b) An example set-up of the probe station for taking measurements (c) A microscope view of chip CCS_DTA 18 with three probes contacting the pads.

4.3 Bi-directional electrical biasing approach

4.3.1 Method introduction

To evaluate crosstalk, a bi-directional electrical biasing method (originally published in

[87]) was applied to obtain the thermoelectric voltage V_T generated by a thermopile (pixel) under thermal stress, as shown in Figure 38. The pixel was thermally heated by Joule heating [88], i.e., by applying a range of biasing currents (in this case, from $I \sim$ 10 μA to 200 μA) to the thermopile elements, resulting in a heat load (RI^2) proportional to the thermocouple resistance (R). This gives rise to a ΔT across its thermocouple's junctions and thus a V_T. To extract V_T, a current in both negative and positive directions (I^+ and I^-) was applied, as shown in Figure 38. I^+ and I^- are the current that having the same absolute value with opposite sign. V^+ and V^- are the related output voltage signal when the thermopile is biased by I^+ and I^-, respectively.



Reproduced from [87]

Figure 38: Schematic diagram showing the bi-directional electrical biasing measurement method in three steps.

When the p+ and n+ Si elements of the pixel are I-biased, the total generated voltage will contain an Ohmic drop ($V = IR$) contribution, caused by the thermocouple track's R, added to V_T. The measured respective voltages, for the applied positive (I^+) and negative (I^-) electrical currents, will therefore be $V^+ = I^+R + V_T$ (step 1) and $V^- = I^-R + V_T$ (step 2), as shown in Figure 38. When added, the voltage caused by electrical resistance (created by the opposing current flows) cancels out, resulting in $V_T = (V^+ + V^-)/2$ (step 3). The V_T generated by an adjacent pixel is then directly measured and finally, the crosstalk can be calculated as the ratio between the two.

4.3.2 Responsivity measurements

In Figure 37a, the heater pixel inside the green frame is the pixel heated by an external current source. The bi-directional electrical biasing approach was applied to this pixel for calculating the thermoelectric signal generated. The adjacent test pixel, surrounded by the black frame, was the pixel to be measured. As there is no V/I source connected, the signal generated from the test pixel is purely induced by the IR radiation from the heater pixel.

A range of currents (from 10 μA to 200 μA) were applied through the probe station to the heater pixel (pixel no.21). At each current level, the voltage signals output from the heater pixel and test pixel were measured by two SourceMeters and recorded. Three different chips were tested to ensure the consistency of the experimental results.

4.3.2.1 Results and discussion

The results of the calculated responsivity, crosstalk and pixel resistivity are presented in Table 2. A plot of output signal versus power in the heater pixel is shown in Figure 39 as a line graph. In Figure 39, the three differently coloured lines, which represent the results from the three different chips (red line for chip 1, green line for chip 2 and blue line for chip 3) almost perfectly overlap each other. The responsivity can be extracted by the slope of the linear line. Chip 1 has a responsivity of about 73.35 V/W, chip 2 is around 73.66 V/W and chip 3 has a slightly lower value, 72.31 V/W (the average responsivity is ~73.1 V/W). As the difference between the three chips was less than 3%, the results can be considered to show good consistency. A comparison between the performance of crosstalk and pixel resistance of different chips, also shown in Table 2, is discussed in the following sections.

Table 2: Experiments results of responsivity, crosstalk and pixel resistivity in three chips

Devices	Responsivity (V/W)	Crosstalk (%)	Pixel Resistance (kΩ)
Chip 1	73.35	2.70	76.75
Chip 2	73.66	2.68	76.13
Chip 3	72.31	2.71	75.20

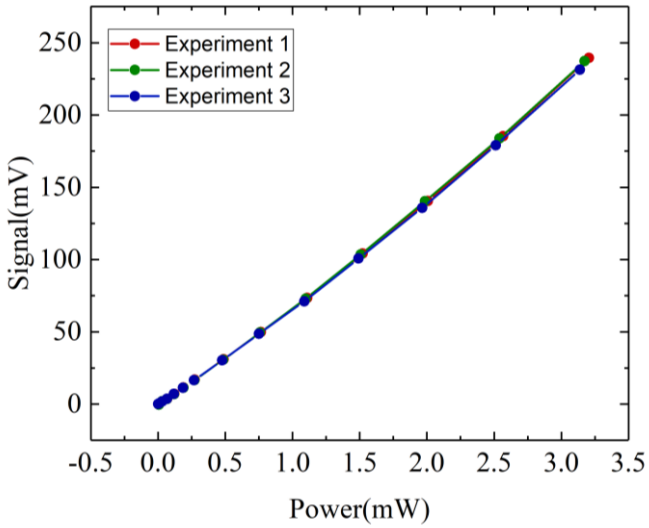


Figure 39: Experimental results of thermoelectric signal versus the power of the heater pixel in three chips.

4.3.3 Crosstalk measurements

By obtaining the thermoelectric signal from the heater pixel with the bi-directional electrical approach, using a separate Sourcemeter to measure the signal from the test pixel, crosstalk can be quantified by calculating the ratio between the signal from the heater pixel and the text pixel. To reduce error, the final crosstalk is given as the average value of the crosstalk obtained at each current level (10 μA ~200 μA).

4.3.3.1 Results and discussion

As shown in Table 2 above, the crosstalk of the three devices were quite similar. Chip 1 is 2.7%, chip 2 is 2.68% and chip 3 is 2.71%, giving an average crosstalk of ~2.69%. These values are comparable to current state-of-the-art thermopile FPAs [59, 89], with this novel method being significantly simpler to apply. The resistance of a single pixel was also obtained, the resistance of a pixel in chip 1 was 76.75 kΩ, 76.13 kΩ in chip 2 and 75.2 kΩ in chip 3. The difference between the crosstalk and the resistivity values are both less than 3% and are therefore at acceptable levels.

4.4 A thermopile array system for gesture recognition and people counting applications

4.4.1 Design

In order to obtain thermal images, these chips should be integrated with a suitable amplifier for larger signals. The printed circuit board (PCB) named 'LMP93601 Evaluation Board' from Texas Instruments was chosen for testing our chip, see Figure 40. This PCB is an Analog-Front-End (AFE) board, which has three differential channels, a low noise analogue to digital converter (ADC), a programmable gain amplifier (PGA) with low offset voltage (0.7 μVrms), low input bias current (–1.3 nA), and a programmable gain of up to 128x (the total gain of this device can be up to 4096x with the digital programmable gain from the ADC) [90, 91]. Overall, this AFE is characterised as high gain (up to 4096x), low noise (up to 2.331 μV_{rms}), ultra-low shutdown current (0.1 μA) and it is designed for thermopile array with pixels up to 16×16 [90]. The experimental configuration of the smart IR detector array is shown in

Figure 41 and the results of this test have been presented in [92].

Photo removed for copyright reasons. Copyright holder is Texas Instruments Incorporated.

Figure 40: Functional block diagram of LMP93601 Evaluation Board [90].

Photo removed for copyright reasons. Copyright holder is Optica Publishing Group.

Figure 41: Thermopile array system diagram. Each pixel is accessed by selecting the corresponding XY address via internal on-chip decoder circuits. An output frame consists of X by Y differential signals, each floating on a reference voltage (V_{ref}) provided by the AFE. Each frame is transferred to the AFE via positive and negative output pins of the sensor in serial format, where it is amplified, digitized, and subsequently, processed by the microcontroller (MCU). The thermal image and processing of a hand posture are shown, the red dots represent the number of fingers which is computed by an algorithm, more details in section 4.4.3.

The 16×16 thermopile array chip (chip CCS_DTA 22) was mounted and bonded to a 16 pin TO-8 type chip package, which was placed on a PCB, connected to the board LMP93601, and interfaced to a microcontroller (MCU, MSP430). This 16×16 array is fabricated based on the same materials and process as the 8×8 array (CCS_DTA 18), which has been introduced in section 4.2. The output from the active pixel elements was read by selecting the corresponding XY address of the internal decoder circuits. An output frame (one sample from each of the pixels) consists of differential signals from the X by Y array which were amplified and digitized by the AFE.

4.4.2 Test

The thermopile detector shows high optical absorption in the 8–14 μm waveband (measured at room *T* using a Fourier-transform IR (FTIR) spectrometer), due to the properties of the SiO_2 membrane [93]. With an absorption peak of ~90% at 8.5 μm (see Figure 42a), it makes it suitable for people presence detection [94]. For responsivity (R_V) tests, a blackbody source (Fluke 4180) was placed at a 50mm distance away from the device and the source was set at a constant temperature of 100°C. In the tests, the total emitted power from the blackbody was used for R_V calculations, which was extracted from the measured V_T. R_V varies with the wavelength [17] and is expected to be at its highest value in the 8 to 10 μm range (see Figure 42a, depicted by the wavelength range between the dashed green lines), which is the relevant IR absorption range for detecting human bodies and contribute most to the thermopile outputs.

The response uniformity to IR illumination per pixel for the 16 × 16 pixels array is shown in Figure 42b. The pixel elements in the centre of the membrane show a drop of up to 20% in signal level due to the lower efficiency of the thermopile cold junction heatsinking (see Figure 42b). At the edge of the membrane, the substrate with bulk silicon acts as a more efficient heatsink, maximizing the temperature difference

between the hot and cold junctions, thereby creating a higher V_T. The 16 × 16 array shows low thermal crosstalk (~2%), demonstrating the efficiency of the thermal isolation between pixels.

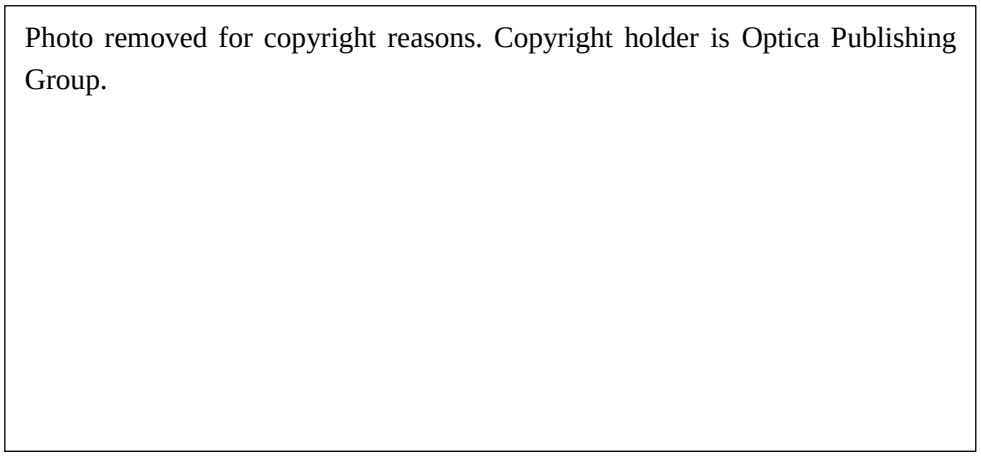


Figure 42: (a) IR absorption spectrum of the 16 × 16 pixel array measured using FTIR spectroscopy, and (b) its pixel optical response uniformity.

When considering the practical application of this thermopile array, a relevant metric to characterise is the noise equivalent power (*NEP*), which represents the lowest detectable power per square root bandwidth (f, typically normalized to 1 Hz) [17]. In a thermopile detector, the noise level is dominated by the thermal Johnson–Nyquist contribution, $V_n = \sqrt{4KTR}$ [17], where k is the Boltzmann constant, and R is the detector resistance. The *NEP* is obtained by dividing this value by R_V. The 16 × 16 pixel array has an R_V of 34 V/W, translating to a NEP ~1.6 nW/$\sqrt{\text{Hz}}$. This gives a specific detectivity $D^* = \sqrt{A}/NEP$ [11] of 7 × 10^5 cm$\sqrt{\text{Hz}}$/W, where A is the membrane area. The values calculated for these thermopile arrays are comparable to current state-of-the-art thermopile sensor arrays [96,96].

4.4.3 Signal processing

To test the array in a real-world situation, it was used to detect and recognise thermal images of hand gestures. The system consisted of the IR array and a Umicore IR lens (focal length = 6.8 mm) with ~97% transmission in the 8–12 μm range, to form the images. The eight timing signals (X and Y), required by the thermopile array to output the pixel data, regenerated by the MCU, with data being transmitted from the array one pixel at a time.

The system was driven at a speed of 10 fps, corresponding to a ~300 μs pixel sampling time. To compensate for R_V non-uniformity, 100 consecutive frames were averaged to form a reference frame which was then subtracted from the normal frame to create a corrected frame. The reference frame subtraction removes pixel-to-pixel offsets present in the thermopile array, and the image of any warm objects that are stationary in the sensor's field of view (FOV). The reference frame is taken after an initial ~10 min warm-up time, and then periodically retaken to compensate for changes in ambient *T*. Thermal images of five different hand postures are presented in Figures 43a-e.

To detect a hand posture, a low-complexity image processing algorithm based on an open-source computer vision and machine learning software library [97] was used. The algorithm uses the corrected frame to track the heat characteristics of the hand in the target area and predicts its posture. In this case, manually setting the threshold determines the temperature below which data are not considered, thereby effectively setting the image background. The algorithm ignores any pixels with a value that is lower than the threshold and only captures pixels with a value that is higher than the threshold value.

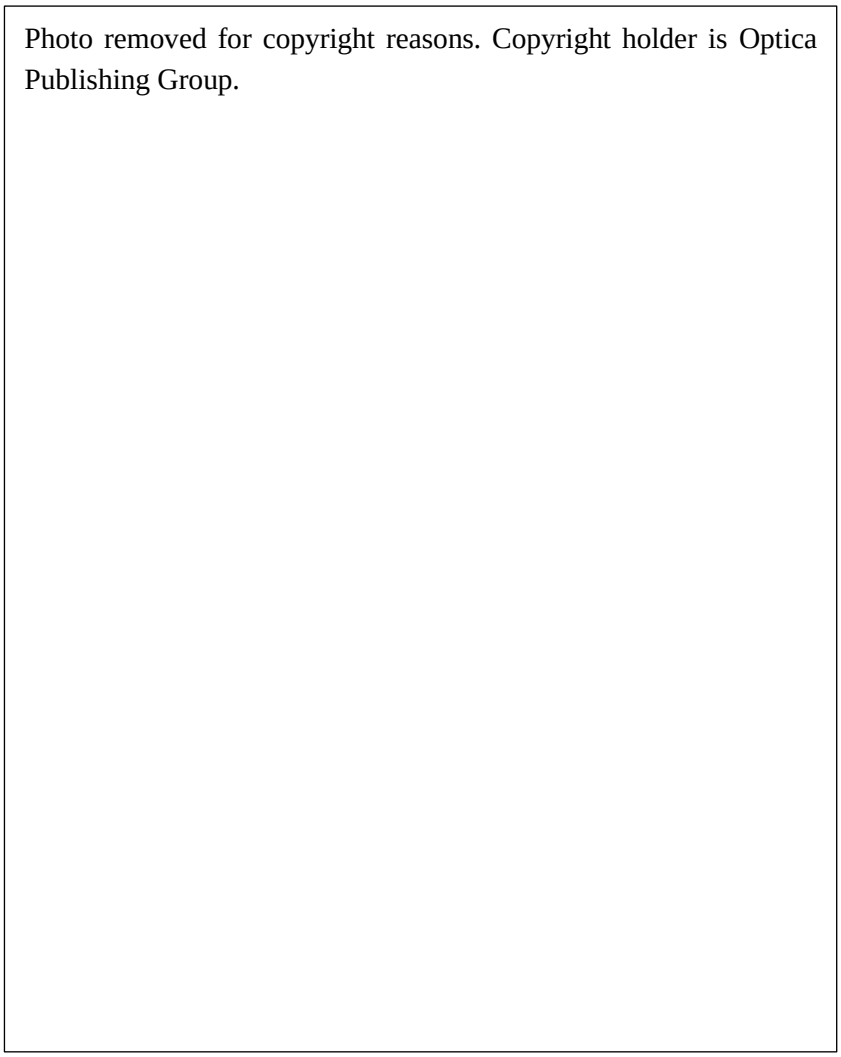


Figure 43: Hand posture thermal images showing (a) one, (b) two, (c) three, (d) four, and (e) five fingers. Frame (f) demonstrates the image processing of frame (e). The background is subtracted by manually setting a pixel threshold. Pixels below the threshold are not considered. An algorithm computes the extreme points (shown in red) of the thresholded posture, which is then used to estimate the number of fingers, being five in this case.

Figure 43f illustrates the process of image processing, where the background of Figure 43e has been removed. The algorithm then discovers the contour of the thresholded hand pose (convex hull [97]) and calculates its extreme points (shown in red in Figure 43f), which is finally used to obtain the number of fingers in a posture. For more

information on image processing, see [97]. The system shows good performance not only for tracking a moving object but also for detecting its posture.

The system was also tested for its ability to count the number of people in a room. For operational testing, the system was placed on the ceiling (in front of the door) and operated continuously for a few days, while periodically being connected to a host computer to control the new reference frames. The number of people entering and leaving the room was counted with 100% accuracy. This test demonstrates that the device has surpassed its proof-of-concept stage and can already be used in real-world applications and environments for posture detection and counting.

4.5 Conclusions

In this chapter, the structure, operation and fabrication process of the SOI CMOS MEMS detector array chips were introduced. The basic experimental set-up was presented and a novel bi-directional biasing method for measuring the signal and crosstalk of the thermopile detector array was introduced and applied in experiments. This method treats a pixel as a micro-heater, reducing the design complexity of an on-chip heater and effectively simplifying the experimental set-up compared to methods utilising external laser sources (with this special resolution). The crosstalk of the 8×8 array is ~2.69% and responsivity is ~73.1 V/W. Three 8×8 chips were measured with a difference of less than 3%, ensuring and emphasising the consistency of the chip performance. For the thermopile array system design, the 16×16 thermopile array was successfully employed for thermal gesture detection and people-counting applications.

Chapter 5

Thermopile array - numerical modelling

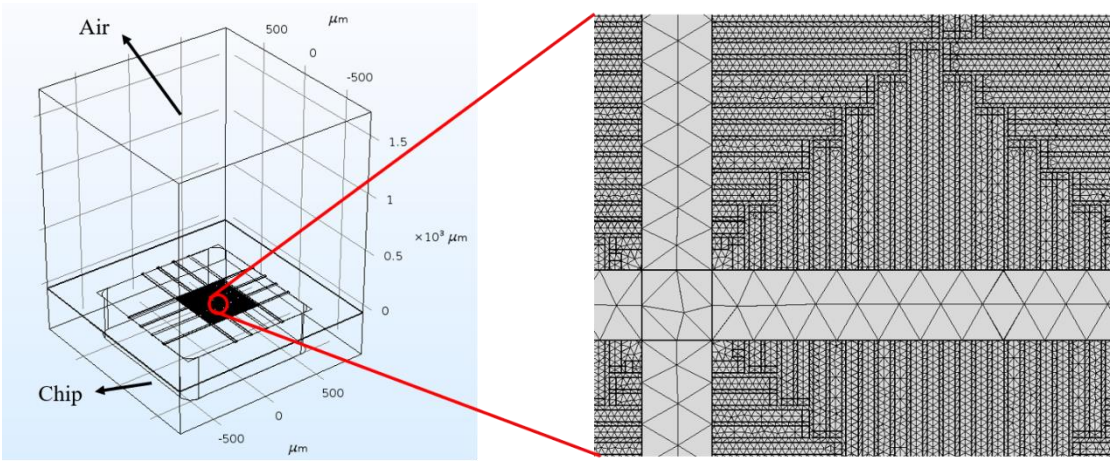
5.1 Introduction

In order to analyse and optimise the array design, numerical simulations based on a FEM model have been carried out. For a comprehensive depiction of the thermopile's behaviour, the electric current module, the heat transfer module and their coupling physics from the commercial software package COMSOL Multiphysics [89] was implemented. These two modules were coupled with equations to implement the Seebeck effect (where equation (3.5) was implemented for the electric current module and equation (5.1) was implemented for the heater transfer module). These equations were investigated in detail in [85, 98], which simulated the thermoelectric phenomena with a combination of Joule heating and input thermoelectric properties.

$$Q = J_x \alpha \frac{dT}{dx} + J_y \alpha \frac{dT}{dy} + J_z \alpha \frac{dT}{dz} \tag{5.1}$$

Where J is current density, α is the Seebeck coefficient, σ is electric conductivity and Q is the heat.

The 3-dimensional (3D) view of the model (Figure 44a) shows an air cube placed on top of the chip to account for heat loss in the air. The length of the air (1.76 mm) is the same as the chip length. An example of part of the mesh built in this model is shown in Figure 44b, where it illustrates the mesh of the circled area in Figure 44a, including a corner of a pixel with surrounded metal tracks. Moreover, as the heat conduction of the air should be accurately simulated here, the mesh built in the air cube is much finer than the mesh built in the thick Si substrate.



(a) (b)

Figure 44: (a) 3D view of the numerical model with air block above. (b) Top view of the mesh built for the circled part in (a), which includes a corner of the pixel and surrounded metal tracks.

5.2 Advantages compared to state-of-the-art devices

There is an extensive literature concerning the numerical modelling of a single thermopile detector [99] or a linear array of thermopiles [65, 100]. A high-performance MEMS IR thermopile detector (equipped with a double-ended beam and a dual-layer thermocouple structure to improve the responsivity, which achieved 1151.14 V/W and

measured response time at 14.46 ms) is introduced in [99] and it built a model to obtain the temperature distribution across the device. The characterization of thermal crosstalk in a linear MEMS thermopile detector array (building thermal quadrupole models to obtain the crosstalk performance) is introduced in [65] and a 3D model to compute the temperature distribution across a linear array with 256 pixels is presented in [100]. In contrast, there have been very few studies dealing with the numerical simulation or modelling of 2D thermopile arrays. Multiphysics modelling (including the Joule heating, heat transfer and Seebeck effect) of four thermopiles (made up of different CMOS materials, placed on the same membrane with a heater in the centre) is implemented in [101] to improve the accuracy of the Seebeck coefficient in different CMOS materials. A simple thermopile array model is introduced in [102]. The array is based on 2×8 pixels and shaped like an "X", which makes this kind of structure inapplicable for accurate thermal imaging. A CMOS integrated MEMS detector array with 10×10 pixels based on thermopiles is presented in [59]. This paper depicts a model which only simulates one complete pixel (with gold grid surrounded) to obtain a comparison of temperature distributions when heated by IR absorption or by an integrated electric heater. This design implements gold layers for heatsinking, which can lead to non-standard processes and is less cost-efficient as gold is not fully CMOS compatible.

Furthermore, there are no analyses that compare designs with different interconnecting metals or air gaps through the membrane (an area focused upon in Chapter 6). The work introduced here is based on a newly developed 3D numerical model for a 2D structure thermopile-based detector array (based on the CCS_DTA 18 chip introduced in Chapter 4), this model was published in [87]. Compared to existing literature, the work in this chapter presents a numerical model based on a fully CMOS compatible thermopile array and the relevant 3D model includes 9 fully working pixels in the centre of the array with Multiphysics modelling (Joule heating, heat transfer, Seebeck effect and their coupling physics) to obtain the accurate temperature profile and the thermoelectric

voltage output from the thermopiles. The model can be used to investigate different approaches for achieving thermal isolation between thermopile elements, including the use of heatsinking tracks and air gaps in the membrane. By comparing the simulation results for different designs, an optimized design can be selected based on the performance and fabrication complexity.

5.3 Numerical model

5.3.1 Design simplifications

Compared to the real device, the complexity of the numerical model was reduced by making the following simplifications to reduce computation time (an optical image of the actual chip is compared with the model in Figure 45). Firstly, the metal pin pads around the membrane were removed, considering their likely negligible effect on both the electrical and thermal behaviour of the chip [101]. Secondly, only the nine pixels at the centre of the membrane were included in the simulation, however, the metal tracks surrounding them remained (Figure 45b). Considering the device contains 64 identical thermopiles (a lower mesh count significantly reduces mesh elements and computation time). Thirdly, the W interconnections within the thermopiles were defined to have the same thickness as the silicon layer (Figure 46b). The thickness of the W interconnection was ~0.5μm thicker than the silicon layer in the real chip and they are defined to be placed at the same height. As the Seebeck effect in the Si thermocouples legs was the main process to be considered, as the Seebeck coefficient in Si is hundreds of times greater than that in W, slightly decreasing the thickness of W interconnections should have negligible impacts on the simulation results. By taking these steps, the complexity of the mesh is significantly reduced and requires a significantly shorter computation time. The 3D view of the model shows that there is an air cube placed on top of the chip

to account for heat losses to the air (Figure 46a).

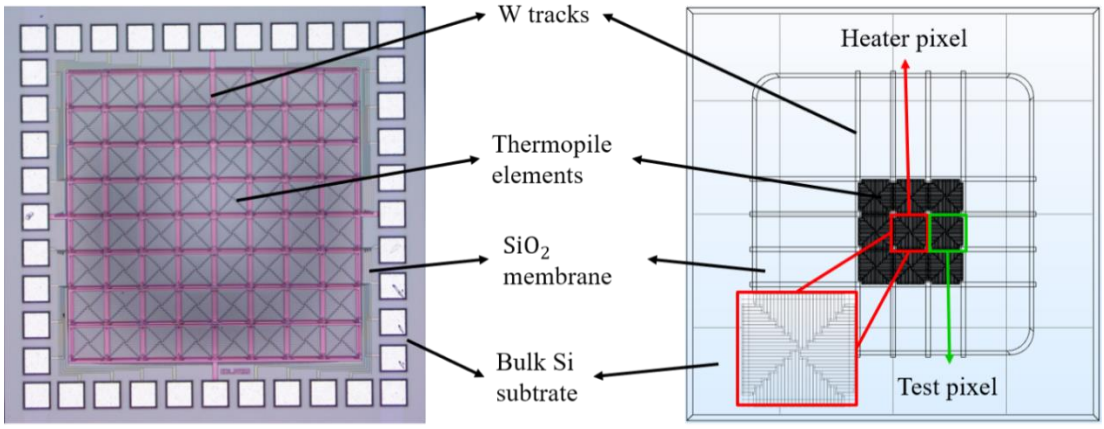


Figure 45: (a) Optical image of the thermopile array (b) Top view of the numerical model.

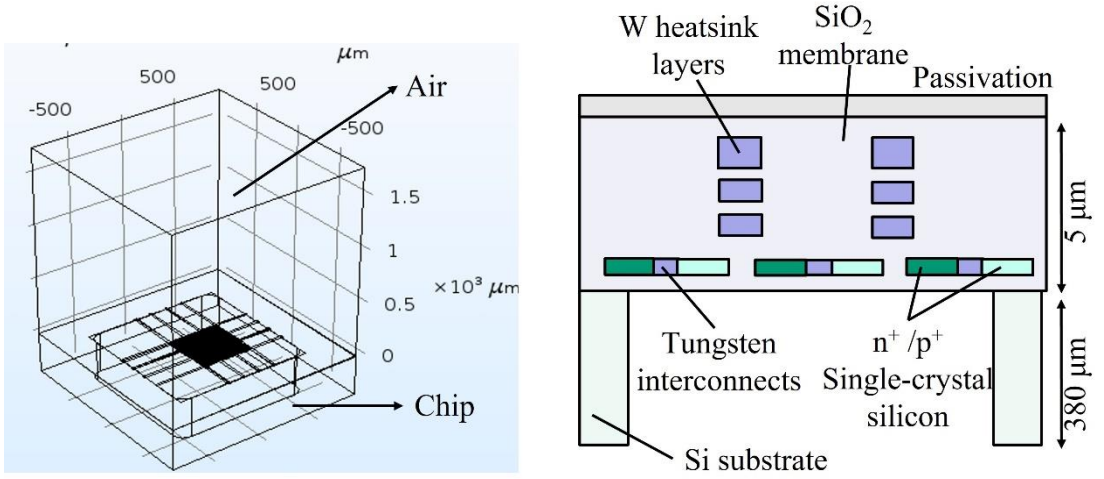


Figure 46: (a) 3D view of the numerical model with the air cube above the chip (b) Cross-sectional view of the numerical model (not to scale) showing the single-crystal Si p+/n+ elements and W layers of the thermopile array.

The length of the air cube is the same as the chip's length, which means the air cube is very small (<5.5mm^3) but allows for capturing critical thermal processes, which were mainly the heat conduction in the air (the model assumes there is only stationary air

above the device, fluid dynamics were not considered here). The successful implementation of a small air volume was enabled through the use of a software built-in boundary condition, *open boundary*, which allows the free conduction of the air and heat exchange between the inner and outer sides of the defined boundary. Due to this boundary condition, the size of the above air cube and mesh count in the model can be dramatically decreased and simplified while still allowing accurate computation of heat conduction and reducing computation time. Moreover, the use of a smaller air volume avoids potential influences on the temperature profile across the chip which might be caused by the implementation of a large air block.

5.3.2 Validation with experiment results

To match the performance between the models and real devices, key parameters of the materials (like the thermal conductivity and electrical resistivity) are obtained from the foundry. For the thermopiles, the thermal conductivity is 60 W/mK in the highly doped p^+ and n^+ Si, while the electrical resistivity is 16.25×10^{-6} Ωm in p^+ Si and 1×10^{-5} Ωm in n^+ Si. W used here has a thermal conductivity of 80 W/mK and electrical conductivity of 12×10^{-9} Ωm. The thermal conductivity for SiO_2 (the membrane) and silicon nitride (the top passivation layer) is 0.8W/mK and 2.2 W/mK, respectively, their electrical conductivity is not considered here as passivation and membrane layers do not participate in the Joule heating process. To obtain the Seebeck coefficient of the FPA here, the thermoelectric voltage was calculated using the bi-directional biasing approach introduced in Figure 38 and the relevant temperature difference was obtained from an IR thermal microscope (more details in Figure 48a). In this case, the relative Seebeck coefficient of the thermocouples in this FPA (α_r from equation 2.6) was calculated to be ~700 μV/K. The agreement between simulation and experimental results shown in Figure 47 proves the workability of these parameters used in the simulation models.

The comparison of the simulation and experimental results are presented in Figure 47 and show good agreement for thermoelectric signal (V_T) generated by a pixel as a function of input power. The corresponding average error value is ~5% (the responsivity is 73.1 V/W in experiments and 72.76 V/W in simulation), which is acceptable. The crosstalks in the simulations and experiments are 2.7% and 2.69%, respectively, with an error of less than 1%.

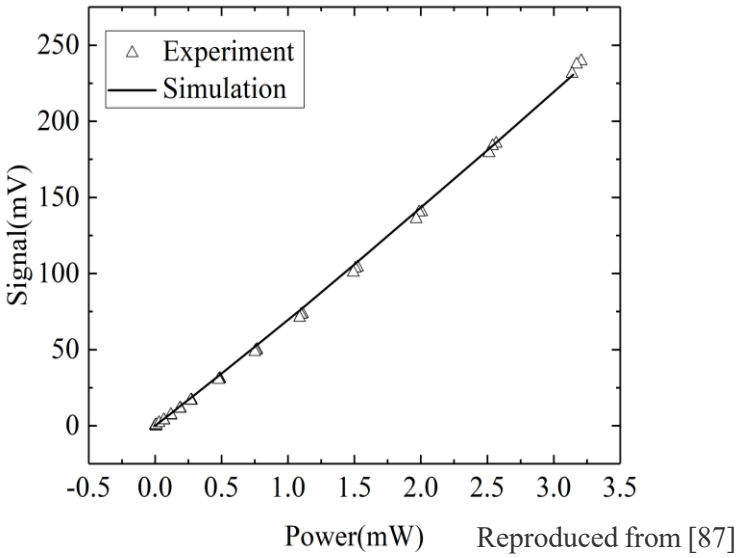


Figure 47: Comparison between simulated and experimentally generated thermoelectric voltages, by a heated pixel at different electrical power levels, ranging from 0 to 3.5 mW.

To identify the possible reasons for the small difference in the thermoelectric signal from experiments and simulations, the electric conductivity of the elements was modified. To simulate extra resistance in the device, the electric conductivity of the n doped Si was decreased by 20%. In this case, the responsivity reaches ~73.1 V/W which matches perfectly with the experimental data. On the other side, the differences noted in responsivity between the simulations and experimental data could be caused by the existence of additional resistance, which may affect the measurement results. The extra resistance from the experiments could be caused by the metal pads used to read the

pixel signals and/or the detecting probes from the measurement equipment. Alternatively, the value of the electric conductivity of the doped silicon may vary between batches, which may also lead to a small difference between the results from simulation and physical measurements.

To further analyse the influence of the environment on device performance, the thermal conductivity of the air block was changed slightly in the simulation model. The responsivity is consistent with the measured results when the thermal conductivity of the air block is decreased by 3%. Therefore, the actual temperature of the experimental environment might be slightly lower than 25 °C (which was the ambient temperature defined in the simulation model). In this case, the reduced air temperature may affect the air's thermal conductivity which could explain the small difference between the simulation and the experimental results.

The temperature distribution across the simulated chip surface was also compared to that measured using an IR thermal microscope with a real chip, both obtained with a heating current of ~200 μA (Figure 48).

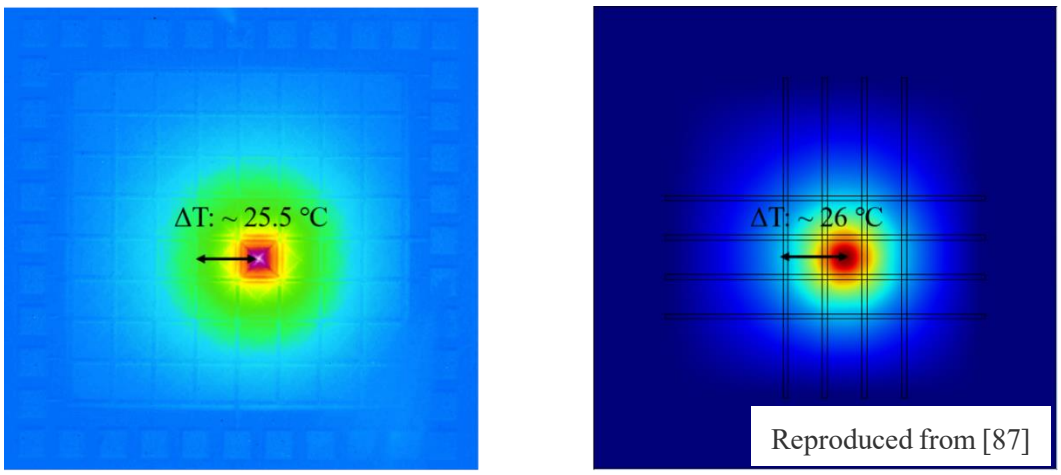


Figure 48: (a) IR image of the thermopile detector array chip measured using an IR thermal microscope. (b) Temperature distribution across the chip obtained from the simulations.

As can be seen from Figure 48, the colour distributions in both images are quite similar, with the hottest reading in the centre of the heated pixel and then gradually decreasing until reaching the edge of the chip. The temperature difference from the hottest point (the centre of the heater pixel) to the edge of the left adjacent pixel was measured. The numerical model estimates a difference of ~26 °C, the thermal microscope confirms this estimate with a recording of ~25.5 °C. It is expected that temperature-induced changes in the thermal properties of the materials, which may cause any distortion [17], would be limited here as temperature changes due to electrical heating are limited.

Figure 49 indicates the temperature distribution across the chip when the heater pixel is heated at a power of 3.2 mW.

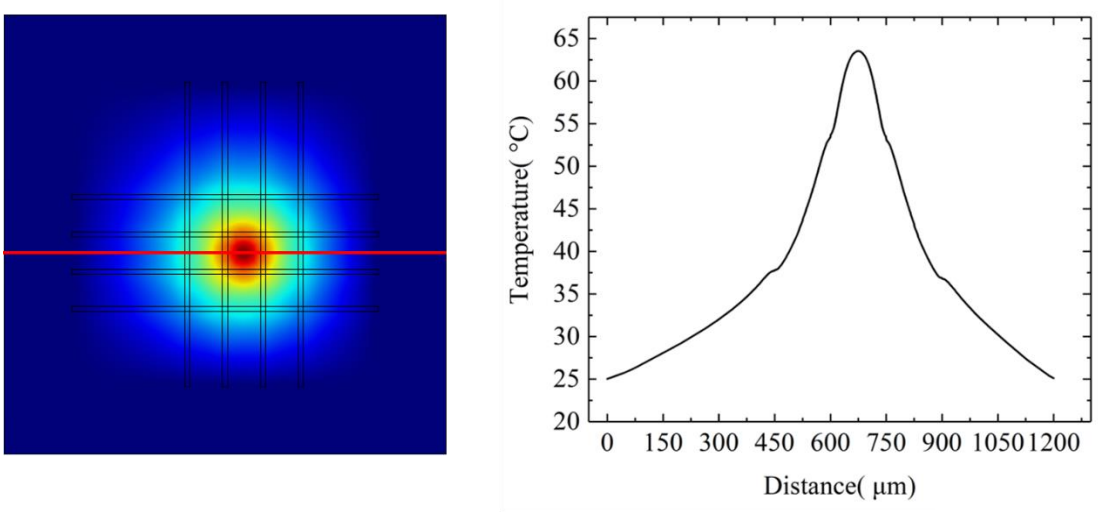
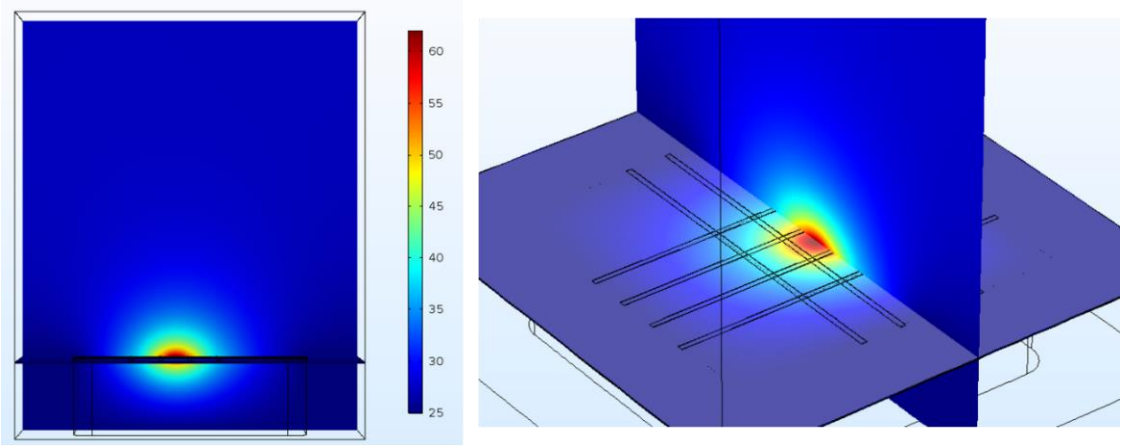


Figure 49: Simulated temperature distribution across the chip membrane when the heater pixel is powered at 3.2 mW. (a) Indicates the resulting temperature distribution across the nine simulated pixels with a cutline (red) placed through the centre of the nine pixels. (b) The simulated temperature along the cutline shown in (a), moving from the left to the right-hand side of the chip.

A cutline on the chip surface is defined across the middle of the heater pixel (placed on the surface of the chip), shown as the red line in Figure 49a. The temperature versus

distance along the cutline is shown in Figure 49b, which emphasises that temperature decreases when getting closer to the edge of the chip. Due to the position of the heater pixel, being slightly closer to the right-hand side of the membrane edge, the temperature decrease from the heat centre to the right side of the chip is quicker than the temperature drops on the left-hand side of the chip (can be observed by the line slope from each side).

Figure 50a illustrates the temperature distribution across the cross-section of the model, how heat conduction from the device to the air occurs is presented clearly in this image. Figure 50b shows the combination of the cross-section temperature distribution and the temperature across the chip surface.



(a) (b)

Figure 50: (a) Temperature distribution through the cross-section of the model showing the heat conduction from the heated area to the surrounding air. (b) Combined images of temperature distribution across the cross-section and across the chip surface.

Figure 51 gives the voltage profile across the surface of the nine simulated pixels when the centre pixel is connected to a positive 200 μA current, the voltage scale is given on the right side of Figure 51a. Each pixel contains a GND (in the same position as marked in Figure 51b) and the current is only applied to the biasing pixel (also marked in Figure 51b). The colour spectrum applied in Figure 51 clearly identifies the position of the

highest and lowest voltage, with the deepest blue end of the spectrum (see Figure 51b) representing GND at 0V, as the voltage increases through the connected thermocouples, it eventually reaches the deepest red end of the spectrum, demonstrating where the thermopile is biased.

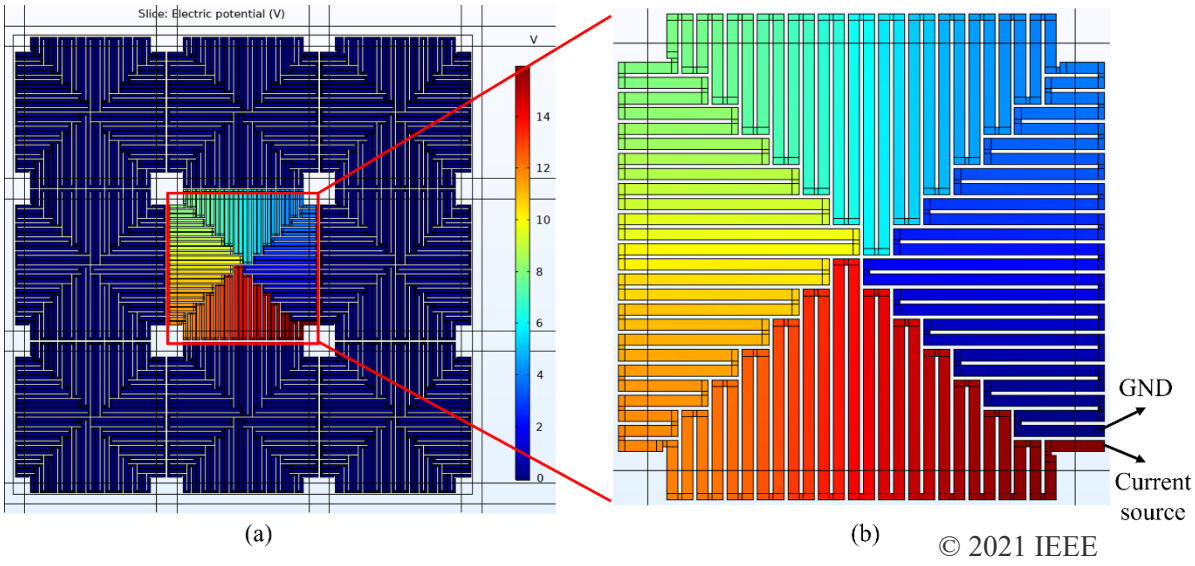


Figure 51: (a) Voltage profile across the simulated nine pixels when the heater pixel (highlighted by the red square) is biased by a 200 μA current (b) enlarged voltage profile of the heater pixel, the ports of GND and current source are marked on the image.

5.3.3 Simulations computed with different mesh quality

To understand the influence of the mesh quality on the accuracy of the simulation results, models with coarser (about twice of the mesh size) and finer mesh (about half of the mesh size) were created for key components (pixels and heatsinking tracks), see Table 3 for relevant boundary and edge mesh elements numbers. Compared to the original mesh presented in Figure 44b, where at least two elements were built along with the width of metal tracks and thermocouple legs, the coarser mesh shown in Figure 52a only includes a single element along the width. Figure 52b illustrates a finer mesh model, where more than twice the number of elements were built along the tracks and

thermocouple legs. The simulation results of models computed with different meshes are displayed in Table 3, with the experimental results included for comparison.

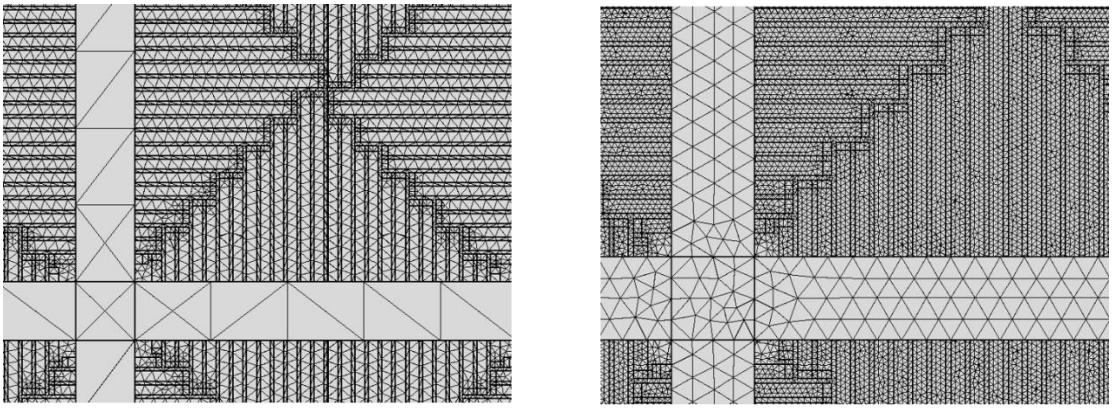


Figure 52: Top view of the mesh built for the highlighted part of Figure 44a, which includes a corner of the pixel and the surrounding metal tracks in (a) Model built with a coarser mesh and (b) model built with a finer mesh.

Table 3: Comparison of experiment results with simulation results for models built with different mesh qualities.

Results	Crosstalk (%)	Responsivity (V/W)	Boundary mesh elements of pixels & tracks	Edge mesh elements of pixels & tracks
Measurements with current source	2.69	73.10	-	-
Simulations with original mesh	2.70	72.76	92306	52369
Simulations with coarser mesh	2.78	72.69	37431	34336
Simulations with finer mesh	2.73	72.95	193116	73978

As can be seen from the data, simulation results with a coarser mesh show a larger error,

with more than 3% difference in crosstalk when compared with physical measurements, and more than a 5% difference in responsivity. For the models with the original mesh and finer mesh, the crosstalk difference is maintained at ~1% and the errors in responsivity compared to experimental results were ~4% and ~2% in the original mesh and finer mesh, respectively. Although the responsivity calculated by the model with the finer mesh shows the best agreement with experimental measurements, the computation time is almost twice that of the model with the original mesh. The error in the model with the original mesh is deemed as acceptable, as it is less than 5%. In this case, simulation design with the original mesh set-up is accurate enough, with the advantages of being more time-efficient and less computationally complex.

The temperature distribution along the cutline (defined in Figure 49) in the three models at ~3.2mW is plotted in Figure 53. The black line is the original model, the yellow line shows the model with a coarse mesh and the blue line gives the results for the finer mesh model.

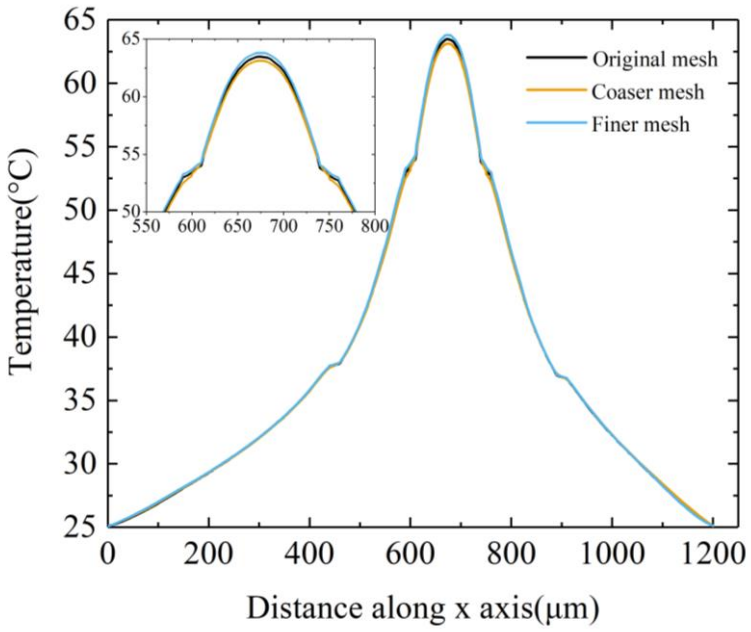
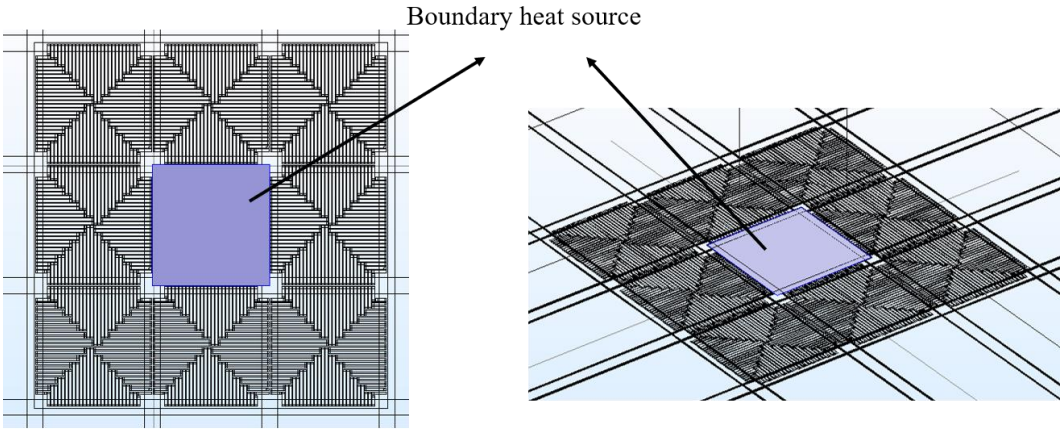


Figure 53: The temperature versus the distance along the cutline (defined in Figure 49a) when the heater pixel is heated by a power of 3.2 mW in models with different mesh quality.

The temperature distribution along the cutline in all three models is quite similar. The inset in Figure 53 gives an enlarged representation of the temperature distribution across the heater pixel. According to the inset, the temperature drops slightly in the model with fewer mesh elements (see the yellow line). However, the difference between the performance across the three models presented in Figure 53 is almost negligible, further illustrating the suitability and accuracy of the original model.

5.3.4 Comparisons with the power source model

In order to compare the bi-directional electrical approach with the traditional method using a laser source, the effect of a uniform heat source across the pixel was considered, as shown in Figure 54.



Reproduced from [87]

Figure 54: (a) Top view of the boundary heat source area. (b) 3D view of the boundary heat source area, the heat source area is highlighted in blue.

The current biasing was replaced with a boundary heat source, across the pixel, to define a constant power dissipation per unit area (a scenario mimicking a laser source illuminating a single pixel). In this case, the pixel is solely heated by the uniform

boundary heat source (no current being applied); with the heating power being equivalent to that for the Joule heating scenario.

5.3.4.1 Results and discussion

Table 4 shows a comparison of simulated crosstalk values obtained for both heating approaches. The pixel's responsivity is also included. The results of the experiments are the average values from across three chips, in order to reduce the error. The resistance of a single pixel measured by experiments was 76.03 kΩ, which is slightly lower than that from the simulations (76.21 kΩ for both the current source model and the boundary heat source model).

Table 4: Comparison between experimental and simulation results. Numerical simulations were implemented using both a current source and a uniform heat source across the thermopile elements.

Results	**Pixel resistance (kΩ)**	**Crosstalk (%)**	**Responsivity(V/W)**
Measurements with current source	76.03	2.69	73.10
Simulations with current source	76.21	2.70	72.76
Simulations with uniform power source	76.21	3.02	63.05

Reproduced from [87]

Regarding the simulations with different sources, the crosstalk simulated with the uniform heat source (3.02%) is slightly higher than that simulated with Joule heating (2.7%), while the responsivity shows an opposite trend, i.e., 13% lower. This is

expected, as a non-uniform heat distribution across the pixel in the model with current source enhances the temperature difference, while inter-pixel heat diffusion is limited by the localized thermopile tracks.

5.4 Conclusions

In this chapter, a 3D numerical model of the 8×8 thermopile array chip was introduced. The simulation was based on the FEM method, using Comsol Multiphysics. This model was able to simulate the physics involved in the array devices: Joule heating, heat transfer and the Seebeck effect with the software built-in physics modules. The numerical model was validated by matching the simulation outputs with experimental results, with a difference of less than 5%. The key parameters are obtained from the foundry and the relative Seebeck coefficient was calculated from the measureed thermoelectric voltage and relevant temperature difference. Models with different mesh quality were shown to prove the feasibility of the original mesh. To compare the bi-directional method to the traditional laser source method, a model with a uniform power source was created. There was a ~10% difference (in both crosstalk and responsivity) between the power source model when compared to the current source model. The difference is mainly caused by the non-uniform heat distribution across the pixel in the current source model, which enhances the temperature difference when compared to the uniform heat boundary source model. This model can therefore be further investigated for design optimisation which is explored in Chapter 6.

Chapter 6

Thermopile array design optimisations and new devices

6.1 Introduction

To improve the performance of our devices, modifications to the structure and materials were required. However, any physical changes to the materials used in the device or modifications to the device structure would require a significant redesign. In addition to the time and cost of redesigning, a new batch of detector arrays would have to be physically produced at the foundry, and further time and costs would be incurred during iterative loops for device optimisation. An alternative solution is the application of advanced numerical modelling. By checking the performance of modified detector array designs with relevant simulation models, accurate results can be obtained efficiently without the added cost, and time, of iterative experimental loops.

To improve the performance of this detector array design, responsivity and crosstalk were the main parameters considered. In this chapter, the modifications to heatsinking tracks and the application of air gaps were the main approaches employed for design improvement. The size of the pixel was also considered, scaling down to identify a

possible smallest pixel size based on the current pixel design.

6.2 Design modifications

6.2.1 Tracks in different widths (10 μm, 20 μm, 30 μm)

The first attempt of design modification was to adapt the width of the heatsinking metal tracks. Here the performance of the model with track widths of 10 μm, 20 μm and 30 μm is shown. The material used for the interconnect tracks is the same as for the original model, i.e., W. Figure 55 depicts the temperature distribution across the surface of the technology computer aided design (TCAD) models (only the centre nine pixels were simulated) with track widths of 10 μm (Figure 55a), 20 μm (Figure 55b) and 30 μm (Figure 55c). A heating current of 200 μA was applied to the heater pixel in the centre, and those images are plotted with a temperature range from ~25°C to ~75°C.

According to the images, the temperature difference between the hottest point and the pixel edge decreases when the width of the metal tracks increases, as the wider heatsinking tracks between pixels allows for more heat to dissipate and thus reduces the temperature of the heating pixel.

The responsivity and crosstalk of designs with different W heatsinking track widths (10 μm, 20 μm, 30 μm) are shown in Table 5. The responsivity of a single pixel increases with decreasing metal track width, increasing from 60.45 V/W (with 30 μm tracks) to 84.54 V/W (with 10 μm tracks). However, the thermal crosstalk shows the opposite trend, decreasing from ~3.7% (with 10 μm tracks) to ~2.5% (with 30 μm tracks).

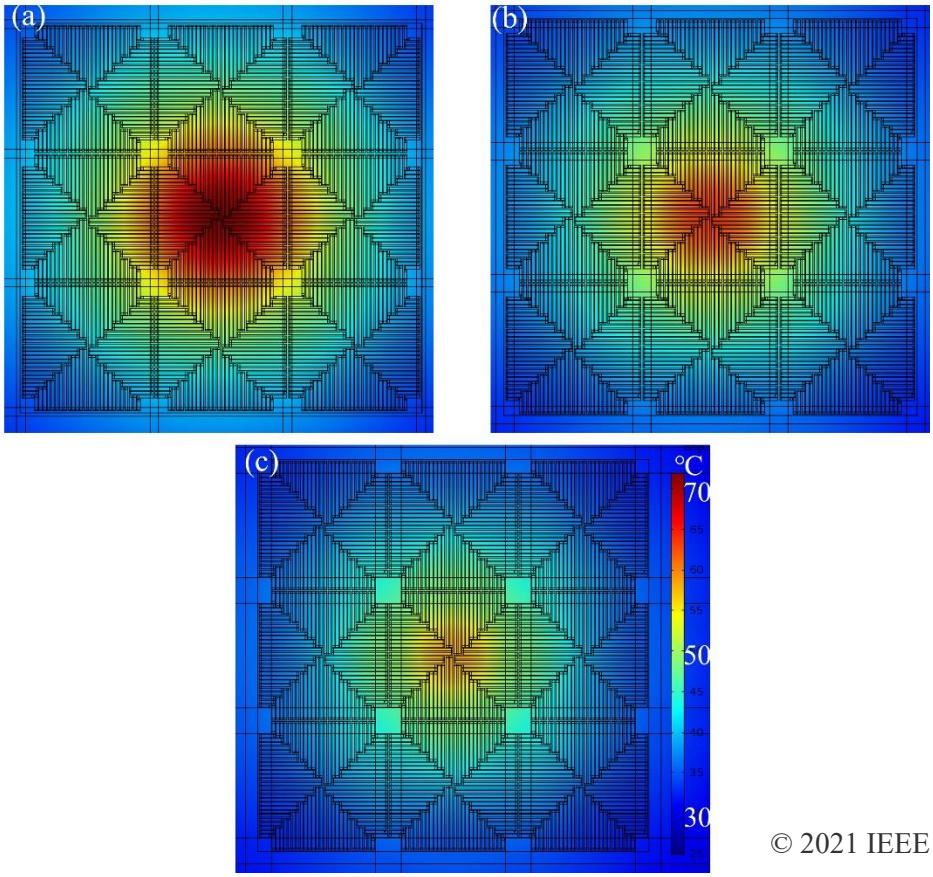


Figure 55: Temperature distribution across the nine modeled pixels for (a) 10 µm-wide W tracks. (b) 20 µm-wide W tracks. (c) 30 µm-wide W tracks. The temperature scale in the three models is the same (from ~25°C to ~75°C).

Table 5: Comparison of models with W heatsinking tracks in different widths

W track width (µm)	Responsivity (V/W)	Crosstalk (%)
10	84.54	3.73
20	72.76	2.70
30	60.45	2.53

The results shown here can be explained by considering the area between the W tracks and the pixels. Wider metal tracks act as a more efficient heat sink, redirecting heat flow away from adjacent pixels, thereby reducing thermal crosstalk. At the same time, more efficient heat sinking lowers the thermal resistance of the pixels, reducing their ability to generate a temperature gradient for a given optical power. The electrical signal

created by the temperature gradient (due to the Seebeck effect) therefore diminishes and the responsivity becomes weaker.

By comparing the performance of the three models, the model with a track width of 20 μm was taken forwards to the next stage of design optimisation. Although the responsivity of the model with a 20 μm track is ~14% lower than that of the model with a 10 μm track, the crosstalk decreases almost 28% when the track width becomes 20 μm. The model with 30 μm track has the lowest responsivity (28% lower than 10 μm model and 17% lower than 20 μm model) while its crosstalk remains similar to the design with 20 μm track (only about 6% lower than that of 20 μm width model).

6.2.2 Tracks in different metals (Tungsten, Aluminum, Copper)

To find an approach of reducing the crosstalk between pixels without affecting the working area of the pixels, metals with a higher thermal conductivity could be employed for heatsinking tracks. Two metals, aluminum (Al) and copper (Cu), were utilized as alternative materials for heatsinking tracks in simulations.

A comparison of the performance between Al, Cu and W is displayed in Table 6. The results show that as the thermal conductivity of the material increases (80 W/mK for W, 238 W/mK for Al and 400 W/mK for Cu), the crosstalk decreases (2.7% for W, 1.55% for Al and only 1.09% for Cu). However, the responsivity shows the opposite trend, (72.76 V/W for W, 68.78 V/W for Al and 67.29 V/W for Cu). This is because more heat is extracted from the pixels through metal tracks with higher thermal conductivity which lowers the temperature and reduces the temperature difference between the centre of the heating pixel and the edge of the chip membrane.

The temperature distribution of the simulated nine pixels in models equipped with different heatsinking metals when heated a power of ~3.2mW is displayed in the Figure 56.

As can be seen from the colour distribution from the plots in Figure 56, the implementation of Al and Cu greatly helps to improve the thermal isolation from the centre pixel to its adjacent thermopiles. According to the results from three models, with the changes in thermal conductivity across the different metal types, more heat is dissipated through the heatsinking tracks and thus leads to a lower temperature in the centre pixel and lower crosstalk between pixels.

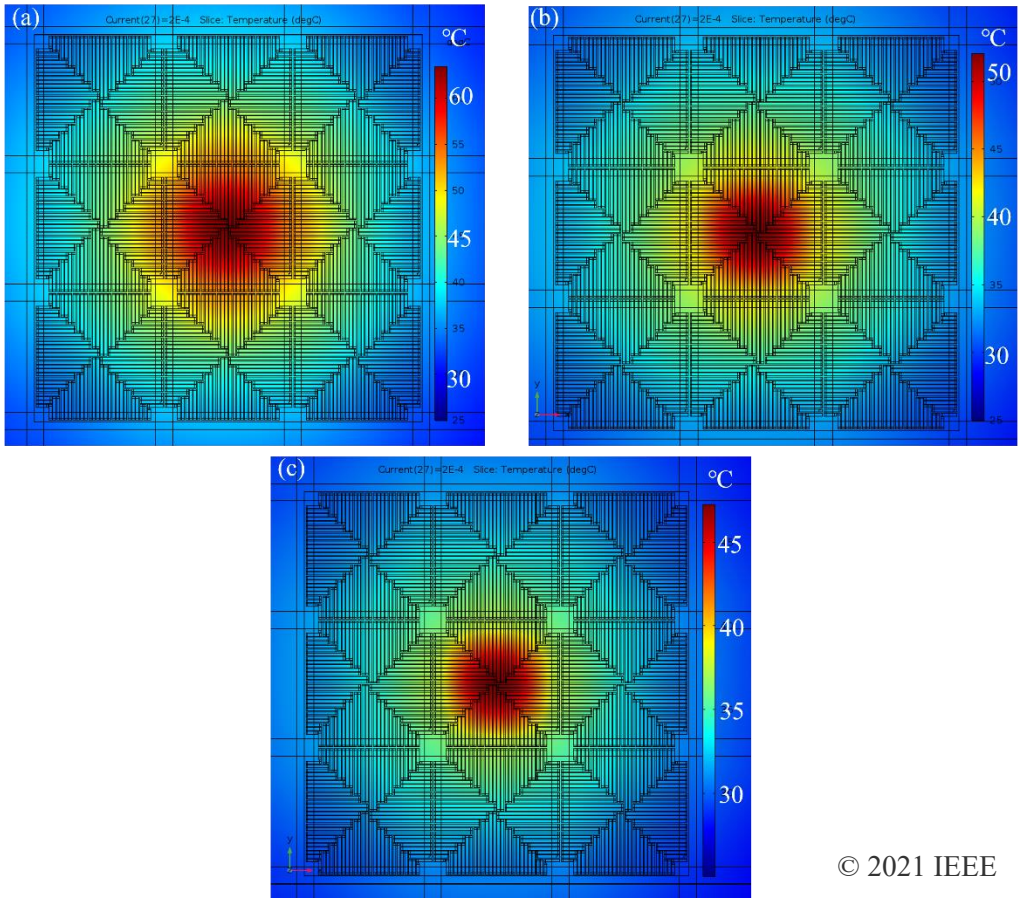


Figure 56: Temperature distribution across the modelled nine pixels in (a) W tracks, (b) Al tracks, (c) Cu tracks, the relevant temperature scale is shown on the right side of each figure.

Table 6: Comparison of performance between models with heatsinking tracks comprised of different metals

Heatsinking metal type	Responsivity (V/W)	Crosstalk (%)
W	72.76	2.70
Al	68.78	1.55
Cu	67.29	1.09

Although crosstalk drops ~60% in the model with Cu tracks compared to the W tracks design, the responsivity of Cu tracks also decreases by ~7.5%. Therefore, a potential solution that may simultaneously keep the responsivity constant and reduce thermal crosstalk was the next aim of the optimization process.

6.2.3 Air gaps

To find a solution of maintaining the responsivity, a new array structure that implements air gaps is explored in this section. As air has a much smaller thermal conductivity (~0.025 W/mK at room temperature) when compared to silicon and metals, air gaps were cut through the membrane and placed around pixels to improve the thermal isolation between pixels. Designs with and without air gaps are shown in Figure 57 and the comparison of results from different models is presented in Table 7. The thin strips circled by the red frames illustrate the air gaps. The metal tracks are highlighted in blue, in this case, W is used.

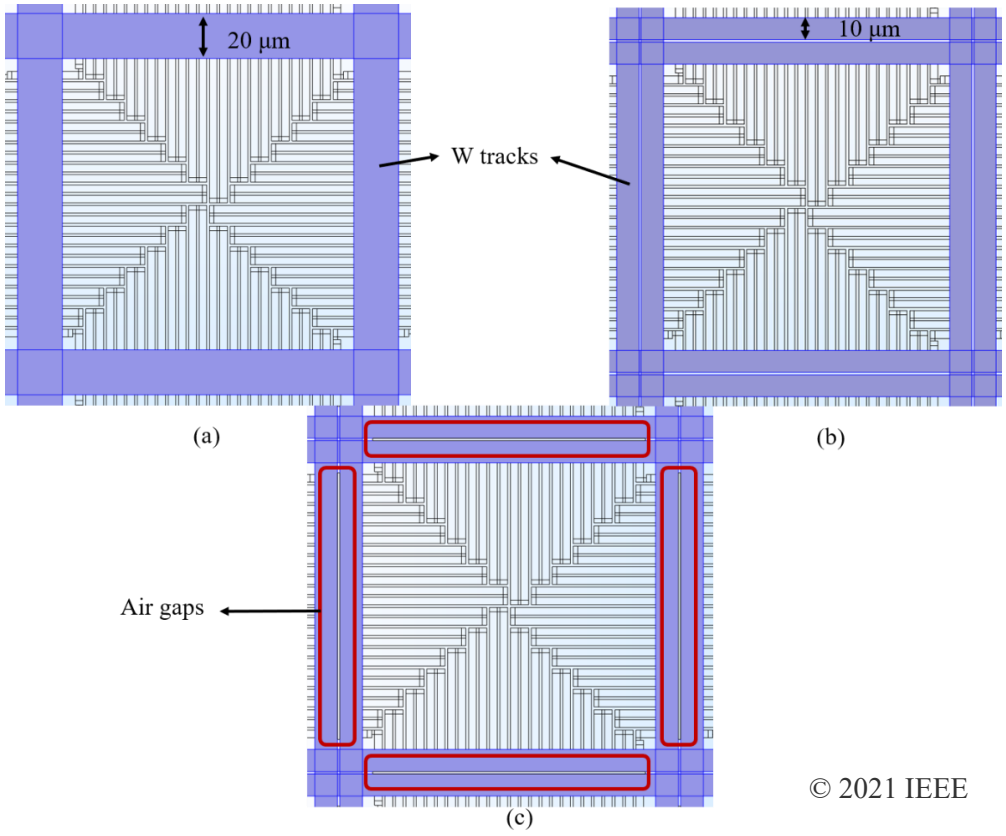


Figure 57: (a) A single pixel surrounded by W tracks without air gaps (b) A single pixel surrounded by split W tracks without air gaps (c) A single pixel surrounded by split W tracks with air gaps (circled by red rectangles) cut through the membrane.

Table 7: Comparison of performance between models with W heatsinking tracks, split W tracks and models with a combination of W tracks and air gaps

Heatsinking metal	Responsivity (V/W)	Crosstalk (%)
W	72.76	2.70
W (split)	72.55	2.83
W with air gaps	77.10	2.70

According to the data from table 8, the responsivity of the model with air gaps (77.1 V/W) increases about 6% compared to that of the original model (72.76 V/W). At the same time, the crosstalk almost remains the same, with 2.7% in both the model with original design and the model with air gaps.

Combined with the results from the previous section 6.2, a new design could feasibly employ air gaps to improve responsivity and a suitable metal to reduce crosstalk.

6.2.4 Different packaging

In order to identify more possibilities for design improvements, Table 8 lists the results of models when different packaging was applied to replace the air above and below the chips, see those blue blocks highlighted in Figure 58. As can be seen from the table, the crosstalk value drops ~26% to 2% when the packaging uses argon instead of air. At the same time, the responsivity shows a slight increase (~5%).

Another model is a simulation with vacuum packaging. Though there is no thermal conduction in perfect vacuum, the vacuum packaging for chips might still allow some heat conduction. So, to simulate the vacuum packaging, the thermal conductivity of the gas cubes is defined to be 0.005 W/mK (~0.023 W/mK in air). In this case, the crosstalk shows a huge drop to 0.68%, and the responsivity increases ~14.7% when compared to the model with an air packaging. Furthermore, the results of a W model with combination of vacuum packaging and air gaps between pixels are shown. With the combined modifications, the crosstalk reduced to 0.63% and the responsivity effectively grows up to more than 90 V/W, and it is almost 27% higher than the original design.

Table 9 demonstrates that different packages of this array design will effectively affect chip performance, and gases with lower thermal conductivity, like argon or vacuum packaging, may be a favourable choice when compared to air. However, the use of specialised gases like argon or using vacuum packaging would significantly increase costs and the maintenance of the vacuum packaging could also increase the cost.

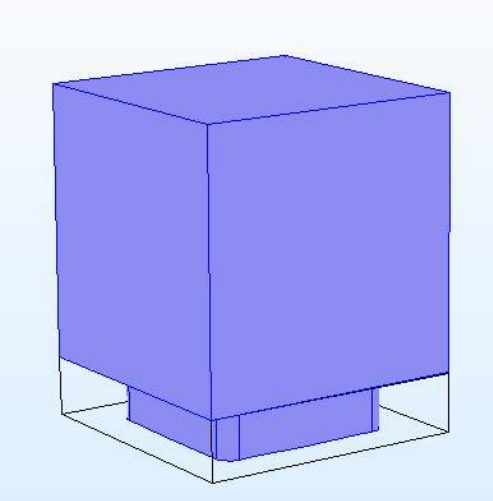


Figure 58: Simulation model with gas blocks highlighted.

Table 8: Comparison of simulation results for models with different packaging, as opposed to air.

Simulation results (W model)	Crosstalk (%)	Responsivity (V/W)
Air (original)	2.70	72.76
Argon	2	76.37
Vacuum	0.68	83.45
Vacuum & air gaps	0.63	92.15

6.3 Optimised design with a combination of modifications

Figure 59 illustrates the temperature versus distance along the cutline (which is defined in Figure 49) in simulations with different heatsinking metals and air gaps. The graph can be considered as a combination of three groups of lines where the different groups are distinguished by metal type. Designs with W tracks show the highest temperature, followed by Al tracks. As the thermal conductivity in W is the lowest of the three metals,

less heat can be extracted by W tracks and thus leads to the highest temperature distribution. Compared to the original design, the models with air gaps inserted between pixels experience a sharp temperature drop in the gap region, this could result from the large difference between the thermal conductivity of metal and air. Figure 60 gives the temperature distribution across models with all three metal tracks (W, Al and Cu) when air gaps are inserted between heatsinking tracks.

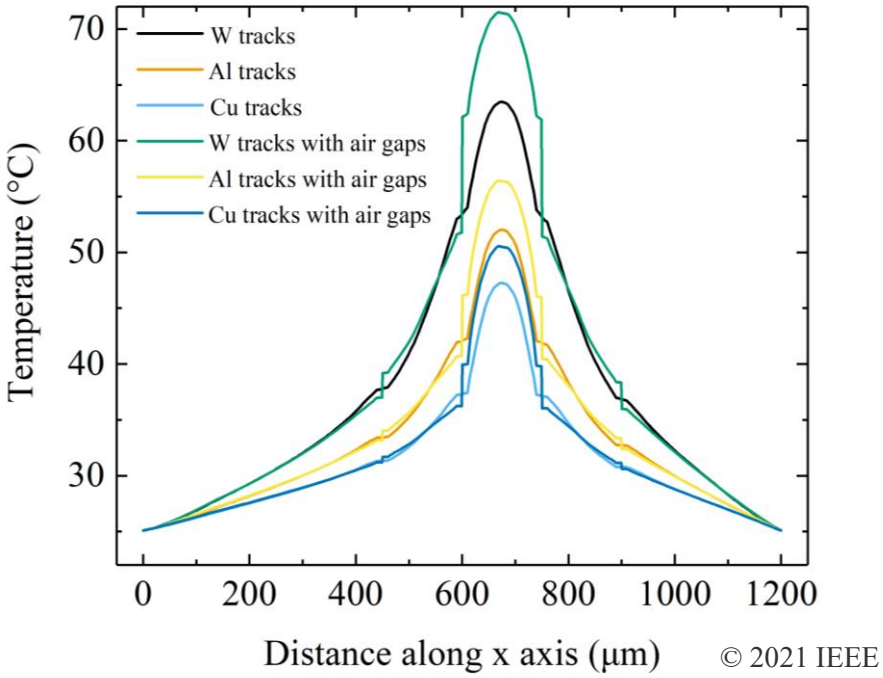


Figure 59: Temperature versus the distance along the cutline, as defined in Figure 49a, when the pixel is heated by power at 3.2 mW in array models with W, Al and Cu heatsinking tracks and their corresponding models with air gaps inserted.

Table 9 lists the data of responsivity and crosstalk from models with a combination of new heatsinking metals and air gaps. Different metal tracks were explored in the previous section to reduce the crosstalk. The crosstalk and responsivity for each are summarized in Table 10, where it also shows the values achieved using different combinations of different metal tracks and air gaps to help either maintain or improve responsivity levels while significantly reducing crosstalk. The results from the model

using W have already been shown in Section 6.3.1.

Table 9: Comparison of performance between models with heatsinking tracks in different metals and their corresponding models with air gaps inserted

Heatsinking metal type	Responsivity (V/W)	Crosstalk (%)
W	72.76	2.70
Al	68.78	1.55
Cu	67.29	1.09
W with air gaps	77.10	2.70
Al with air gaps	77.53	1.44
Cu with air gaps	77.44	0.95
Cu with air gaps & vacuum packaging	85.84	0.20

For the model using Al as a heatsinking metal, the responsivity increases by ~13% with the air gaps inserted (from 68.78 V/W to 77.53 V/W), while its crosstalk is reduced by ~7% (from 1.55% to 1.44%) when compared to the Al model without gaps. For the model with Cu heatsinking tracks, responsivity increases by ~15% (from 67.29 V/W to 77.44 V/W) while the crosstalk drops by ~13% (from 1.09% to 0.95%) when compared with the Cu model without gaps. The responsivity from the Cu model with air gaps is ~6.4% higher than that of the original W model (without any air gaps), and the crosstalk drops by almost 65% in the Cu model with gaps (compared to the original W design). The last row of this table includes the simulation results of a model which combines Cu heatsinking tracks, air gaps and vacuum packaging. In this case, the crosstalk dramatically decreases to ~0.2% and the responsivity grows to more than 85V/W. Based on these results, a combination of Cu heatsinking tracks and air gaps should be used in future designs. In addition, though the cost will be increased, vacuum packaging could also be considered in future design as it effectively improves the performance in responsivity and crosstalk.

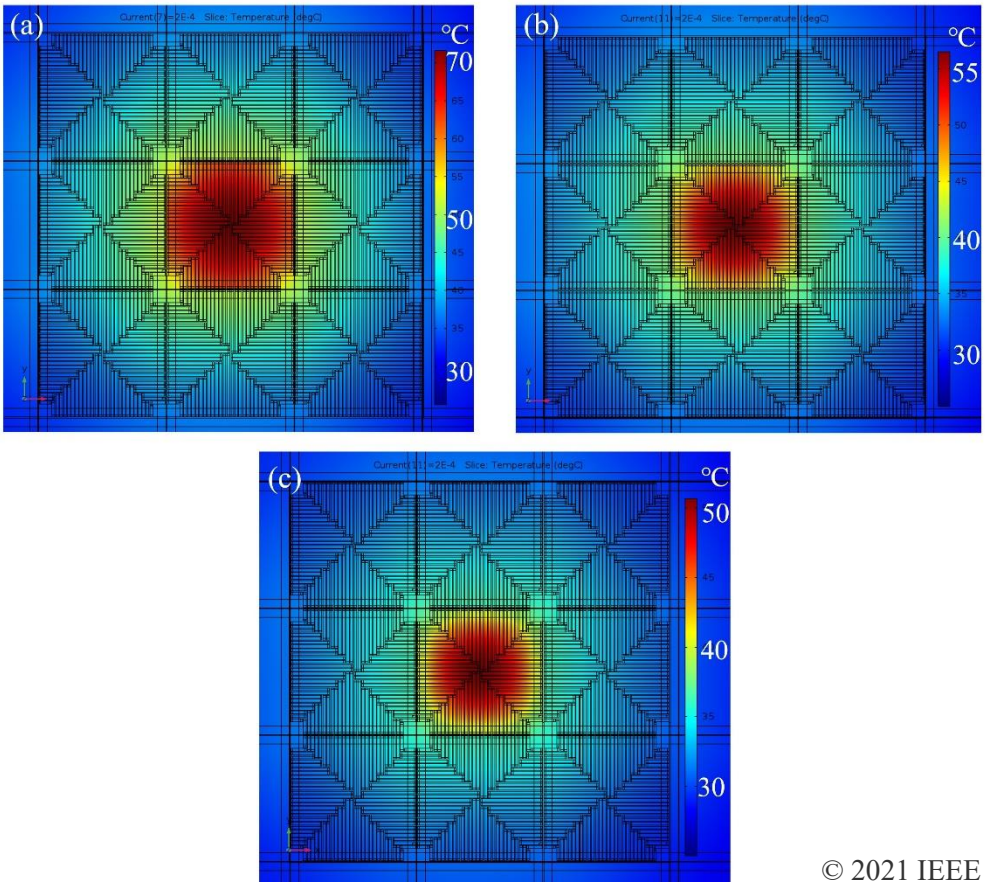


Figure 60: Temperature distributions across the modelled nine pixels with air gaps cut through in (a) W tracks, (b) Al tracks, (c) Cu tracks, the relevant temperature scale is shown on the right side of each figure.

6.4 Smaller pixel size

To investigate the effect of pixel size on the chip performance, the key parameters of simulation models with different array sizes were compared. The materials and dimensions of the FPA chips remain the same as those implemented in the model introduced in the previous sections (e.g., membrane area is 1.2 mm ×1.2 mm, the thermocouple is formed by n doped and p doped Si and the linking metal is W). A comparison presented in Figure 61 gives the top view of the models with different pixel size.

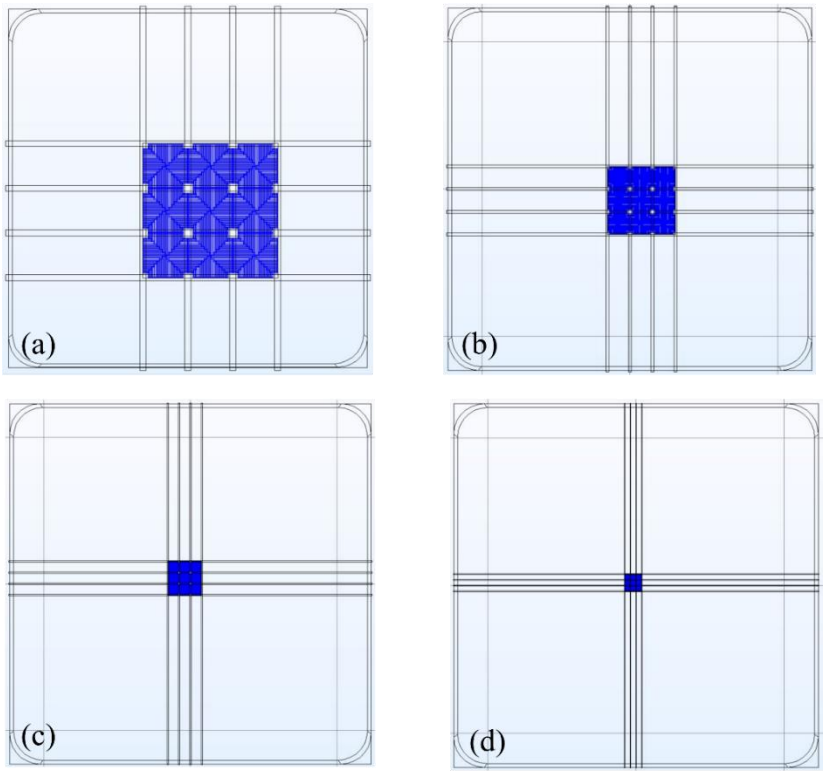


Figure 61: The comparison between the membranes from models with different size of pixels, (a) 8×8 array, (b) 16×16 array, (c) 32×32 array, (d) 64×64.

The number of thermocouples in each pixel is the same (52 thermocouples per pixel) and the only difference is the number of pixels (arrays with 8×8, 16×16, 32×32 and 64×64 number of pixels) and their relevant heatsinking track width is scaled down relatively, according to the pixel size. For instance, the area of a pixel in an 8×8 array is 150 μm × 150 μm and the heatsinking track width is 20 μm, so for the 16×16 model, the area of a pixel is scaled down to 75 μm × 75 μm and the heatsinking track width is 10 μm. One thing to note is that the thickness of the thermopiles remains the same in every array design. Table 10 shows the pixel resistance, responsivity, and crosstalk of each numerical model. The bar graphs regarding pixel resistance, responsivity and crosstalk versus pixel area are shown in Figure 62.

It can be seen from the data that pixel resistance increases only slightly with reduced pixel size. This was expected as resistance scales inverse proportionally to the area, and

proportional to the length ($R = \rho l/A$), therefore the length and width of the thermocouples reduce at the same time and almost cancel out the effect of resistance (as the thickness of thermocouples remains the same). Pixel resistance in an 8×8 array is 76.21 kΩ and increases slightly to 76.81 kΩ in 16×16 array, followed by an increase to around 77.38 kΩ in a 32×32 array and finally reaches 78.14 kΩ in a 64×64 array model.

Table 10: Comparison of performance between simulation models with arrays size in 8×8, 16×16, 32×32 and 64×64 number of pixels

Array size	Pixel width (µm)	Track width (µm)	Pixel resistance (kΩ)	Responsivity (V/W)	Crosstalk (%)
8×8	150	20	76.21	72.76	2.70
16×16	75	10	76.81	72.52	2.76
32×32	37.5	5	77.38	77.18	3.79
64×64	18.75	2.5	78.14	101.59	6.33

The crosstalk between two pixels is similar in the 16×16 array model (2.76%) and the 8×8 array model (2.7%). The crosstalk then rises to 3.79% in the 32×32 array, followed by a sharp increase to 6.33% in the 64×64 array model. According to the results shown in Figure 61b, the responsivity is almost identical in arrays with 8×8 and 16×16 pixels, with a value of just over 72 V/W in both cases. The responsivity increases to around 77.18 V/W in the 32×32 pixels array model, followed by its highest value at 101.59 V/W in a 64×64 pixel array. As the pixel size and the width of heatsinking tracks are scaling down without changing the number of thermocouples in pixels, there is less heat that can be dissipated through the metal tracks to the substrate and the overall thermal loss from the pixels is reduced. In this case, the responsivity and the crosstalk effect are increasing with a greater number of pixels are equipped. Although the responsivity in 64×64 shows the highest value (about 40% higher than that in the model with 8×8 pixels), its crosstalk was also the highest, at over 6% (more than twice of that in the

array with 8×8 pixels) it is not at a level acceptable in commercial products, as high crosstalk may greatly affect image resolution. The performance of the array design with 32×32 pixels was more acceptable, where responsivity increased about 6% (compared to the 8×8 array) and maintained crosstalk at lower than 4%. In this case, the performance of the model with a 32×32 pixel array gives the smallest possible pixel size in a detector array on the fundamental of the current thermopile design.

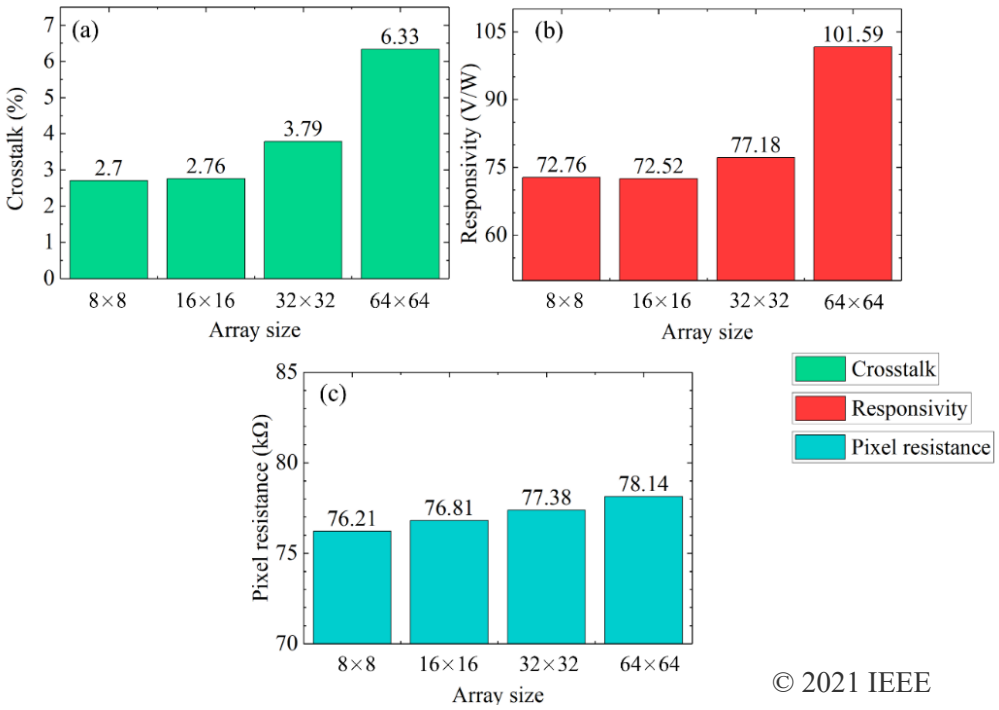


Figure 62: The performance of thermopile array versus pixel area, (a) Crosstalk, (b) Responsivity, (c) Pixel resistance.

The idea of decreasing the pixel size while remaining the membrane area was to find the possibility of increasing the resolution of our thermal FPAs based on current designs. With the pixels and their relevant metal tracks became small, there is less thermal isolation between pixels and lead to a higher crosstalk. Our next step could be looking for approaches to fix this problem, like using metals with higher thermal conductivity, implementing air gaps, vacuum packaging and increasing the distance between pixels.

6.5 Conclusions

This chapter presented novel techniques to increase or maintain responsivity while reducing crosstalk between adjacent pixels in a thermopile array. Special care has been taken for these techniques to be compatible with the current CMOS-MEMS process. These techniques have been validated through extensive numerical TCAD simulations using previously calibrated models. The challenge was to alter the width of the heatsinking metal tracks between pixels in an attempt to reduce crosstalk. However, the simulations showed that while crosstalk decreased by ~6% when the track width was increased to 30μm from 20μm, the responsivity dropped by ~17%.

To find an approach for reducing crosstalk more efficiently, heatsinking tracks comprising metal layers with higher thermal conductivity (Al and Cu) were employed. Here, the model with Cu tracks showed the best performance in terms of crosstalk, which was ~1.09% (60% lower than the crosstalk of equivalent structure with W tracks), but its responsivity decreased to 67.29 V/W (72.76 V/W in model with W tracks). As heatsinking tracks with higher thermal conductivity enhances the heat isolation between pixels, it would also increase the overall heat loss and decreasing the responsivity. In this case, air gaps inserted between split heatsinking tracks were employed to maintain the responsivity level. The design with Cu heatsinking tracks and air gaps showed the potential to increase responsivity by 6.4% while dramatically reducing crosstalk by 65% (compared with the structure using W tracks only). So, it is desirable to implement Cu as heatsinking tracks with air gaps inserted in our next FPA design based on the current thermopile structure. In addition, models with different packaging were simulated, and the vacuum packaging has the potential to be implemented in the future design as it effectively decreases the crosstalk to less than 0.7% (only 0.2% in the Cu model) and increase the responsivity to more than 90 V/W in the model with W tracks. However, the chip cost and size will increase if implementing vacuum packaging and the

maintenance of the vacuum condition could also be a challenge.

Models with smaller pixels sizes (array size in 8×8, 16×16, 32×32 and 64×64) were built and their performance in pixel resistance, responsivity and crosstalk were compared. The reduction on pixel size and width of the relevant heatsinking tracks lead to a decrease of the heat isolation between pixels and thus increase the crosstalk effect. The array with 32×32 pixels gives the smallest possible pixel size based on the current thermopile design, with responsivity reaching ~77.18 V/W and crosstalk remaining <4%. Although the array model with 64×64 pixels showed the highest responsivity (101.59 V/W), its crosstalk was >6% and may have significant effects on the resolution of the final thermal image. To further decrease the pixel size in the FPAs design, new heatsinking designs (e.g., use of metal with higher thermal conductivity, like Cu, and air gaps between pixels) should be employed to reduce thermal crosstalk to an acceptable range. To further increase the absorption/responsivity, carbon nanotubes could be grown or deposited on top of the thermopile, this application is briefly discussed in Chapter 7.

Chapter 7

Conclusion and avenues for future work

7.1 Summary

The wide range of applications and promising emerging markets for thermal imaging technologies was briefly discussed in Chapter 1. Over the last two years, the onset of the COVID-19 pandemic has massively increased the demand for IR thermometers and thermal imagers for non-contact temperature monitoring. The technology and principles behind different IR detectors, as well as the basic theory and properties of IR radiation, were discussed in Chapter 2. IR sensors can be mainly divided into two categories: photon detectors and thermal detectors. Thermal detectors (thermopiles, bolometers, pyroelectric detectors and diodes) are more highly favoured than photon detectors for daily life applications such as human presence detection due to their wider spectral range when operating at room temperature and their lower cost. IR FPAs based on thermal detectors have been presented together with their relevant working principles and main parameters in Chapter 2.

FEM simulation methods of IR detectors were described in Chapter 3. Comparisons between different types of mesh elements and different programming cores were also demonstrated. A model of a single thermocouple was built to validate the simulation

concept. The theory and fabrication flow of MEMS technology were also presented. Chapter 4 introduced the experimental methods for measuring the responsivity and crosstalk of a thermopile based SOI CMOS MEMS array chip. The novel method introduced in this thesis is named the bi-directional biasing method. This method uses a pixel as a self-micro-heater which greatly reduces the design complexity of the on-chip heater and simplifies the experimental characterisation and setup compared to traditional methods with laser sources. The structure, working principle and fabrication flow of the array chip were introduced in Chapter 4. The crosstalk of the 8×8 array was assessed to be ~2.69% with a responsivity of around 73.1 V/W. For the array system design and the requirement for higher resolution, a 16×16 thermopile array was fabricated using the same process as the 8×8 array. This array successfully demonstrated its ability in use cases such as thermal gesture detection and for people-counting applications.

To further analyse the thermopile array design and improve its performance, a 3D numerical model of the 8×8 thermopile array chip was presented in Chapter 5. To match the performance between the numerical model and experimental results, parameters like electrical conductivity and thermal conductivity, were obtained from the foundry. The relative Seebeck coefficient of out thermopile design was calculated by the measured thermoelectric signal and relevant temperature differences. As the difference between the results from simulated and experimental results was less than 5%, the numerical model was proved to be accurate. A novel bi-directional biasing approach was introduced for measuring crosstalk of thermopile based FPAs without implementing complex laser source set-up or on-chip heater. To draw comparisons between the bi-directional method and the traditional laser source method, a model with a uniform power source (mimicking a laser source illuminating a single pixel) over a single pixel was built. The responsivity of the power source model was ~10% lower than the current biasing model while the crosstalk showed the opposite trend. This result was acceptable as the non-uniform heat distribution across the pixel in the current

source model enhanced the temperature difference when compared to the uniform heat source model.

To optimise the array design, several modifications were applied and demonstrated numerically in Chapter 6, these include different heatsinking widths; different metal layers (W, Al and Cu); different packaging and the incorporation of additional air gaps between pixels. Though implementing metals with higher thermal conductivity in heatsinking tracks could effectively decrease the crosstalk, the increased heat loss would also result in a reduced responsivity. The combination of air gaps and heatsinking tracks with metals in higher conductivity works well in decreasing the crosstalk without compromising the responsivity. Overall, the design with Cu heatsinking tracks and air gaps showed the best results: its responsivity showed an increase of 6.4% while dramatically reducing crosstalk by 65% (compared with the structure using W tracks only). Because of the negligible thermal conductivity, vacuum packaging could also be considered in the future design as it can effectively decrease the heat conducted through the air. The W model with air gaps and vacuum packaging shows a crosstalk of lower than 0.7% and responsivity of 92.15 V/W. Models with smaller pixels sizes (array size in 8×8, 16×16, 32×32 and 64×64) were also tested and the 32×32 array shows the smallest possible pixel size based on the current thermopile design, with responsivity reaching ~77.18V/W and crosstalk remaining <4%.

According to the simulation results from the modifications based on the current FPAs designs, the combination of Cu heatsinking tracks and air gaps could be employed in our future FPAs. On the other hand, though the cost will be higher, vacuum packaging could also be equipped if available. To further scale down the pixel size (increase the number of pixels) while maintaining the current chip size, techniques like using heatsinking tracks with metals in higher conductivity, increasing the space between pixels, insertion of air gaps between pixels and using vacuum packaging could be applied to decrease the undesired crosstalk effect.

7.2 Future work

7.2.1 Further optimisations based on current results

On the basis of the simulation results presented in the previous chapters, the material of the metal tracks could be changed from W to Al or Cu, as metals with better heat dissipation performance should be used. Air gaps could also be considered. Although the crosstalk effect shown in these chips is already reasonably small (less than 4%), the performance could be further enhanced by modifying the pixel arrangement. For instance, the distance between the pixels might be increased, or again the metal tracks might be redesigned for better heat isolation between pixels.

Alternatively, as shown in results from the experiments in the 16x16 array chip system (see Figure 42b), the signal variation along a column of pixels can be up to 20%, which would not be acceptable in commercial products. As the signal produced from the centre pixel is always lower than the signal output from the edge pixels, the size of the pixels could be adjusted. For example, the pixel in the centre could be designed to have a larger size in comparison to the edge pixels, with the aim of ensuring a uniform signal over the whole chip. Alternatively, the metal tracks implemented in the chip design could be redesigned. For instance, the size or number of the metal tracks in the central region could be increased for greater heat dissipation, hence increasing the temperature difference which could lead to a larger signal. However, an increase in the size or in the number of metal tracks would result in a larger chip size. Therefore, this method still needs to be further optimised.

7.2.2 Carbon nanotubes

There are several approaches that could be applied to improve the absorption of the IR detector array, such as covering the surface with a high absorption coating, e.g., carbon nanotubes (CNT). A CNT can be considered as a cylinder that is fabricated using rolled-up graphene sheets [103]. CNTs have excellent optical emission [104] and absorption [105] and characteristics across the entire MIR range; thus, they could be employed to enhance the overall optical absorption of our devices. Below is discussed a successful example of increasing the effectiveness of the CNT layers to allow IR absorption enhancements.

In [96], the application of vertically aligned, multi-walled, CNTs as nano-engineered blackbody-like IR absorbing layers in a fully CMOS compatible MEMS thermopile IR detector was characterised. *In-situ* thermal chemical vapour deposition (T-CVD) was applied to grow the CNT layers with the use of an integrated micro-heater as a micro-reactor at 700°C for 10 min, all structures are fabricated in a commercial foundry using SOI (CMOS) technology [105]. The successful growth of the vertically aligned, multi-walled CNT layers was confirmed through Scanning electron microscopy (SEM), as shown in Figure 63a.

Figure 63: (a) SEM micrograph of the CNT-based IR radiation absorbing layer and (b) Mid-IR spectra of carbon nanotubes (CNT)-coated and uncoated devices [105].

Fourier transform IR (FTIR) spectroscopy was applied to compare the absorption between the coated and uncoated detectors, shown in Figure 63b, the spectral range from the wavelength between 3 - 15.5μm. The absorption ($A = 1-R-T$), where R is the reflection and T is the transmission. Compared to the performance of the detector without CNT layers, the absorption of the CNT-coated device was enhanced dramatically and reached almost 100%.

This technique could also be employed in an IR camera (as opposed to a single thermopile). The CNTs could be grown using integrated micro-heaters placed below each pixel or could be deposited post-CMOS and annealed, the latter being cheaper and possibly easier to implement.

7.2.3 Future 3D thermopile structure

In the future development of thermopile based FPAs, fill factor (the ratio of the area of radiation-sensitive pixels to the total area of the FPA) is one of the most significant considerations. The traditional design of thermopile arrays is usually comprised of series-connected two-dimensionally arranged thermocouples. Their advantages include high detectivity due to semiconductor conductors with large Seebeck coefficients, the lack of requirement to implement cryogenic cooling systems and present reasonable design complexity [106].

Compared to bolometer-based IR arrays, thermopile FPAs are passive devices with no requirement for an active sensing readout circuit [107]. Furthermore, thermopile-based FPAs present an opportunity for energy-harvesting, self-powering the readout circuit with the electrical power generated by itself [107]. However, the 2D nature of current thermopile devices results in significant space consumption. Therefore, current 2D thermopile structures may not be the first choice for future high-resolution microarray

sensors [106, 107].

Figure 64 illustrates a schematic structure of a 3D thermopile, of the kind designed and first introduced by Wick et al., (2015) in [106]. This free-standing design could be manufactured on a bulk silicon wafer with holes (diameter: 5 μm and length: 515 μm) cut through to act as a mold (released by photo-assisted electrochemical etching) with the length of the thermocouples decided by the length of the holes [107].

The simulated results of another 3D thermopile structure are introduced in [107] (patented by [108]). A sacrificial layer process (similar to the process presented in [109]) could be employed for fabricating the relevant 3D design (in [108]), while post-CMOS integration could be operated for building the readout circuit [107].

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Figure 64: An example of a three-dimensional thermopile structure from [106]. The absorber consists of n layers includes SiO_2, Si_3N_4, Al for insulating layers and metal connecting for thermocouples. The coaxial thermocouple is made up of m coaxially layers which include SiO_2 and Si_3N_4 for insulating and protection, and n/p doped Si for the thermocouple.

Compared to conventional 2D thermopile designs, this 3D design dramatically reduces

the chip size as all thermocouples can be vertically arranged under the absorber layer. In a 3D design, the readout circuit could be fully equipped within the space under the thermopile. The fill factor of a 3D thermocouple in this design can be almost 100% [106, 107]. In addition, the high aspect ratio of the geometry of this design shows improved electrical responsivity [106]. Simulation results indicate the length of the 3D thermocouple is the main parameter that affects electrical responsivity, specific detectivity and thermal time constant [106]. Thus, this 3D design has the potential to be implemented in future cost-effective, high-resolution microarray IR imagers, as it can meet different requirements by simple making modifications to the length of the thermocouples [106].

References

[1] G. Fedder, "MEMS Fabrication, " in *Proc. ITC International Test Conference*, 2003, pp. 691–698. doi:10.1109/TEST.2003.1270898.

[2] M. Kimata, "Uncooled infrared focal plane arrays," *IEEJ Trans. Electr. Electron. Eng*. 2017, vol. 13, pp. 4–12, doi:10.1002/tee.22563.

[3] A. Rogalski, "Progress in focal plane array technologies," *Progress in Quantum Electronics*, vol. 36, no. 2-3, pp. 342-473, 2012, doi: 10.1016/j.pquantelec.2012.07.001.

[4] D. Popa, F. Udrea, "Towards Integrated Mid-Infrared Gas Sensors," *Sensors*, no. 9, 2019, doi:10.3390/s19092076.

[5] A. Königs and D. Schulz, "Evaluation of thermal imaging for people detection in outdoor scenarios," in *2012 IEEE International Symposium on Safety, Security, and Rescue Robotics (SSRR)*, 2012, pp. 1-6, doi: 10.1109/SSRR.2012.6523883.

[6] D. Minoli, K. Sohraby and B. Occhiogrosso, "IoT Considerations, Requirements, and Architectures for Smart Buildings—Energy Optimization and Next-Generation Building Management Systems," *IEEE Internet of Things Journal*, vol. 4, no. 1, pp. 269-283, Feb. 2017, doi: 10.1109/JIOT.2017.2647881.

[7] G. Meijer, K. Makinwa, M. Pertijs, *Smart Sensor Systems: Emerging Technologies and Applications*, UK, Wiley: Chichester, 2014.

[8] Q. Liang, L. Yu, X. Zhai, Z. Wan and H. Nie, "Activity Recognition Based on Thermopile Imaging Array Sensor," in *2018 IEEE International Conference on Electro/Information Technology (EIT)*, 2018, pp. 0770-0773, doi: 10.1109/EIT.2018.8500177.

[9] V. John, S. Mita, Z. Liu and B. Qi, "Pedestrian detection in thermal images using adaptive fuzzy C-means clustering and convolutional neural networks," in *2015 14th IAPR International Conference on Machine Vision Applications (MVA)*, 2015, pp. 246-249, doi: 10.1109/MVA.2015.7153177.

[10] "Thermal Imaging Market by Technology. Wavelength, Product, Application, Vertical, Region - Global Forecast to 2025, " (2020). https://www.marketsandmarkets.com/Market-Reports/thermal-imaging-market-1300.html. (accessed: Jun.1, 2021).

[11] P. Wadhwani and S. Gankar. "Thermal Imaging Market Size, By Product, By Technology, By End-Use, By Application, Industry Analysis Report, Regional Outlook, Application Potential, Competitive Market Share & Forecast, 2020 – 2026," Global Market Insights, Inc., (2020). https://www.gminsights.com/industry-analysis/thermal-imaging-market. (accessed: Jun. 1, 2021).

[12] "Thermal Imaging Market Size, Share & COVID-19 Impact Analysis, By Type, By Technology, By Product, By Wavelength, By vertical, and Regional Forecast, 2020-2027," Fortunebusinessinsights.com. (2020). Available: https://www.fortunebusinessinsights.com/thermal-imaging-market-102588. (accessed: Jun.1, 2021).

[13] F. Udrea, "Smart sensors for environment monitoring," *ESSDERC Tutorial Leuven*, Sep. 2017.

[14] S. Eminoglu, M. Y. Tanrikulu and T. Akin, "A Low-Cost 128×128 Uncooled Infrared Detector Array in CMOS Process," *Journal of Microelectromechanical Systems*, vol. 17, no. 1, pp. 20-30, 2008, doi: 10.1109/JMEMS.2007.910235.

[15] B. Hunt, A. J. Ruiz, B. W. Pogue, "Smartphone-based imaging systems for medical applications: a critical review," *Journal of Biomedical Optics*, vol.26(4), 15 Apr. 2021, https://doi.org/10.1117/1.JBO.26.4.040902

[16] J. S. Teich, "Digital infrared imaging for medicine. Recent advances in I.R. focal plane array imaging technology," in *Proc. of 18th Annual International Conference of the IEEE Engineering in Medicine and Biology Society*, 1996, pp. 2079-2080, vol.5, doi: 10.1109/IEMBS.1996.646441.

[17] A. Rogalski, *Infrared Detectors 2nd*, Boca Raton, USA: CRC Press, 2011.

[18] A. Schaufelbuhl *et al.*, "Uncooled low-cost thermal imager based on micromachined CMOS integrated sensor array," *Journal of Microelectromechanical Systems*, vol. 10, no. 4, pp. 503-510, Dec. 2001, doi: 10.1109/84.967372.

[19] Teledyne FLIR LLC. "FLIR E96 Advanced Thermal Imaging Camera," Available online: https://www.flir.co.uk/, (Accessed: Aug. 2021)

[20] Teledyne FLIR LLC. "FLIR ONE Pro Thermal Imaging Camera for Smartphones," [online], Available: https://www.flir.co.uk/, (Accessed: Aug. 2021).

[21] Heimann Sensor GmbH, Thermopile sensors (HTS Series). https://www.heimannsensor.com/HTS-A-Series. (Accessed Aug. 2021).

[22] Y. Teng et al., "Demonstration of MOCVD-Grown Long-Wavelength Infrared InAs/GaSb Superlattice Focal Plane Array," *IEEE Access*, vol. 9, pp. 60689-60694, 2021, doi: 10.1109/ACCESS.2021.3072845.

[23] G. Deng, D. Chen, S. Yang, C. Yang, J. Yuan, W. Yang, and Y. Zhang, "High operating temperature pBn barrier mid-wavelength infrared photodetectors and focal plane array based on InAs/InAsSb strained layer superlattices," *Opt. Express*, vol. 28, pp. 17611-17619, 2020.

[24] W. Zhou, H. Zhang, D. Xue, W. Li, Z. Ni and X. Li, "Ultra-Small Pixel IR Sensing Array Fabricated with a Post-CMOS Compatible Process," in *2021 21st International Conference on Solid-State Sensors, Actuators and Microsystems (Transducers)*, pp. 589-592, 2021, doi: 10.1109/Transducers50396.2021.9495752.

[25] F. Tankut, M.H. Cologlu, H. Ozturk, G. Cilbir, O. S. Akar, T. Akin, "A 160x120 LWIR-band CMOS Infrared (CIR) microbolometer," in *Proc. SPIE 11002 Infrared Technology and Applications XLV,* no. 110021Q, 2019, doi: 10.1117/12.2521484.

[26] K. I. Schultz et al., "Digital-Pixel Focal Plane Array Technology," *Lincoln Laboratory Journal*, vol. 20, no. 2, 2014.

[27] U. Sassi et al. "Graphene-based mid-infrared room-temperature pyroelectric bolometers with ultrahigh temperature coefficient of resistance," *Nature Communications*, vol. 8, no. 14311, 2017, doi: 10.1038/ncomms14311.

[28] C. J. Donlon, P. J. Minnett, A. Jessup, I, Barton, W. Emery, S. Hook, W. Wimmer, T. J. Nightingale, and C. Zappa, "Chapter 3.2 - Ship-Borne Thermal Infrared Radiometer Systems," in *Experimental Methods in the Physical Sciences,* Academic

Press, 2014, vol. 47, pp. 305-404.

[29] V. John, S. Mita, Z. Liu, and B. Qi, "Pedestrian detection in thermal images using adaptive fuzzy C-means clustering and convolutional neural networks, " In *Proceedings of the 2015 14th IAPR International Conference on Machine Vision Applications (MVA)*, Tokyo, Japan, May 18–22, 2015, pp. 246–249.

[30] D. Holzman, "The Carbon Footprint of Biofuels: Can We Shrink It Down to Size in Time," *Environmental Health Perspectives*, vol. 116, no. 6, pp. A246-A252, 2008, doi: 10.1289/ehp.116-a246.

[31] T. Waterston and S. Lenton, "Public health: Sustainable development, human induced global climate change, and the health of children," *Archives of Disease in Childhood*, vol. 82, no. 2, pp. 95-97, 2000, doi: 10.1136/adc.82.2.95.

[32] “The Infrared Universe," Cool Cosmos, [online], Available: Coolcosmos.ipac.caltech.edu. (Accessed: Aug. 2018).

[33] J. K. Delaney, G. Trumpy, M. Didier, P. Ricciardi, and K.A. Dooley., "A high sensitivity, low noise and high spatial resolution multi-band infrared reflectography camera for the study of paintings and works on paper," *Heritage Science*, 2017, doi: 10.1186/s40494-017-0146-1.

[34] B. Arifin, A. M. Tahir and I. Priyanto, "LAPAN'S Mid Wavelength Infrared Camera Module," in *IGARSS 2020 - 2020 IEEE International Geoscience and Remote Sensing Symposium*, pp. 6401-6404, 2020, doi: 10.1109/IGARSS39084.2020.9323882.

[35] A. Rogalski, "Infrared detectors: status and trends," *Progress in Quantum Electronics*, vol. 27, no. 2-3, pp. 59-210, 2003, doi: 10.1016/s0079-6727(02)00024-1.

[36] G. Hyseni, N. Caka and K. Hyseni, "Infrared Thermal Detectors Parameters: Semiconductor Bolometers Versus Pyroelectrics," *WSEAS Transactions on Circuits and Systems*, vol. 9, no. 4, pp. 238-247, 2010, doi: abs/10.5555/1852282.1852287.

[37] F. Trager, *Springer handbook of lasers and optics*. Berlin: Springer, 2007, pp. 549-554.

[38] A. Rogalski, "Infrared thermal detectors versus photon detectors: I. Pixel

performance," in *Proc. Material Science and Material Properties for Infrared Optoelectronics*, 1997, doi: 10.1117/12.280417.

[39] D. Schroder, R. Thomas and J. Swartz, "Free carrier absorption in silicon," *IEEE Transactions on Electron Devices*, vol. 25, no. 2, pp. 254-261, 1978. doi: 10.1109/t-ed.1978.19066.

[40] T. Seebeck, "Ueber die magnetische Polarisation der Metalle und Erze durch Temperatur-Differenz," (in German), *Annalen der Physik*, vol. 82, no. 1, pp. 1-20, 1826. Available: 10.1002/andp.18260820102.

[41] A. Graf, M. Arndt, M. Sauer and G. Gerlach, "Review of micromachined thermopiles for infrared detection," *Measurement Science and Technology*, vol. 18, no. 7, pp. R59-R75, 2007, doi: 10.1088/0957-0233/18/7/r01.

[42] D. Rowe, *General principles and theoretical considerations CRC Handbook of Thermoelectrics* Boca Raton, FL: CRC Press. 1995, pp. 7-17.

[43] N. Neumann and V. Banta, "Comparison of Pyroelectric and Thermopile Detectors," in *AMA Conferences*, 2013, pp. 139-143.

[44] J. Nemarich, *Microbolometer Detectors for Passive Millimeter-Wave Imaging*. Ft. Belvoir: Defense Technical Information Center, 2005.

[45] R. Waynant and M. Ediger, *Electro-optics Handbook*, 2nd ed. New York: McGraw-Hill, 2000.

[46] G. Rieke, *Detection of Light – From the Ultraviolet to the Submillimetre*, 2nd ed. Cambridge: Cambridge University Press, 2003.

[47] A. Hossain and M. Rashid, "Pyroelectric detectors and their applications," *IEEE Transactions on Industry Applications*, vol. 27, no. 5, pp. 824-829, 1991, doi: 10.1109/28.90335.

[48] H. Beerman, "The pyroelectric detector of infrared radiation," *IEEE Transactions on Electron Devices*, vol. 16, no. 6, pp. 554-557, 1969, doi: 10.1109/t-ed.1969.16798.

[49] D. Crecraft, S. Gergely, "Diode and transistor circuits," in *Analog Electronics:*

Circuits, Systems and Signal Processing. Butterworth-Heinemann. Amsterdam: Butterworth-Heinemann, 2002, pp. 110.

[50] N. Sclar and D.B. Pollock, "On diode thermometers," *Solid-State Electronics*, vol. 15, no. 5, pp. 473-480, 1972, doi: 10.1016/0038-1101(72)90149-9.

[51] A. McNamara, "Semiconductor Diodes and Transistors as Electrical Thermometers," *Review of Scientific Instruments*, vol. 33, no. 3, pp. 330-333, 1961, doi: org/10.1063/1.1717834.

[52] M. Mansoor, I. Haneef, S. Akhtar, A. D. Luca, F. Udrea, "Silicon diode temperature sensors - A review of applications," *Sensors and Actuators A: Physical*, vol. 23, pp 63-74, 2015, doi: org/10.1016/j.sna.2015.04.022.

[53] B. Siegal, "An Introduction to Diode Thermal Measurements," Thermengr.net, (2009).https://thermengr.net/An_Introduction_to_Diode_Thermal_Measurements6.pdf. (Accessed: Aug. 2021).

[54] G.C.M.Meijer, "Thermal sensors based on transistors," *Sensers and Actuators*, vol. 10, pp. 103–125, 1986, doi: 10.1016/0250-6874(86)80037-3.

[55] H. O. Kang et al., "Fabrication and performance analysis of an amorphous silicon-based thermal IR detector," in *Proc. of 2010 IEEE 5th International Conference on Nano/Micro Engineered and Molecular Systems*, 2010, pp. 696-699, doi: 10.1109/NEMS.2010.5592504.

[56] W. S. Boyle and K. F. Rodgers, "Performance Characteristics of a New Low-Temperature Bolometer," *Journal of the Optical Society of America*, vol. 49, pp. 66-69, 1959, doi: org/10.1364/JOSA.49.000066.

[57] Y. P. Xu, R. S. Huang, and G.A. Rigby, "A silicon-diode-based infrared thermal detector array," *Sensors and Actuators A: Physical*, vol. 37-38, pp 226-230, 1993, doi: org/10.1016/0924-4247(93)80039-J.

[58] M. Kimata, "Uncooled infrared focal plane arrays," *IEEJ Transaction on Electrical and Electronic Engineering*, vol. 13, no. 1, pp. 4-12, 2017, doi: org/10.1002/tee.22563.

[59] A. Schaufelbuhl *et al.*, "Uncooled low-cost thermal imager based on

micromachined CMOS integrated sensor array," *Journal of Microelectromechanical Systems*, vol. 10, no. 4, pp. 503-510, Dec. 2001, doi: 10.1109/84.967372.

[60] A. Rogalski, M. Kopytko, and P. Martyniuk, "Infrared Detector Characterization," in *Atimonide-based Infrared Detectors: A New Perspective*, SPIE, 2018, doi: 10.1117/3.2278814.ch1.

[61] R. C. Jones, "Performance of Detectors for Visible and Infrared Radiation," in *Advances in Electronics and Electron Physics*, vol.5, New York, NY, USA, Academic Press, 1953, pp. 1-96, doi: 10.1016/S0065-2539(08)60683-6.

[62] R. C. Jones, "Phenomenological Description of the Response and Detecting Ability of Radiation Detectors," in *Proceedings of the IRE*, vol. 47, no. 9, Sep. 1959, pp. 1495-1502, doi: 10.1109/JRPROC.1959.287047.

[63] K. Hirakawa, "Cross-talk explained," In *Proceedings of the 2008 15th IEEE International Conference on Image Processing*, San Diego, CA, USA, Oct. 12-15, 2008, pp. 677-680.

[64] G. Agranov, V. Berezin and R. H. Tsai, "Crosstalk and microlens study in a color CMOS image sensor," *IEEE Transactions on Electron Devices*, vol. 50, no. 1, pp. 4-11, Jan. 2003, doi: 10.1109/TED.2002.806473.

[65] H. Wu, S. Grabarnik, A. Emadi, G. de Graaf, and R. F. Wolffenbuttel, "Characterization of thermal cross-talk in a MEMS-based thermopile detector array," *Journal of Micromechanics and Microengineering.* vol. 19, 2009, doi: 10.1088/0960-1317/19/7/074022.

[66] A. Witvrouw, "CMOS-MEMS integration today and tomorrow," *Scripta Materialia*, vol. 59, pp. 945-949, Nov. 2008, doi: 10.1016/j.scriptamat.2008.06.043.

[67] J. W. Judy, "Microelectromechanical systems (MEMS): fabrication, design and applications," *Smart Materials and Structures*, vol. 10, no. 6, pp. 1115-1134, Nov. 2001, doi: 10.1088/0964-1726/10/6/301/meta.

[68] Prime Faraday Partnership, *An Introduction to MEMS (Micro-electromechanical Systems)*, UK, PRIME Faraday Partnership, 2002, pp. 1-29.

[69] V. R. Mamilla and K. S. Chakradhar, "Micro Machining for Micro Electro Mechanical Systems (MEMS), " in *Procedia Materials Science,* vol. 6, 2014, pp. 1170-1177, doi: org/10.1016/j.mspro.2014.07.190.

[70] R. Pratap and A. Arunkumar, "Material selection for MEMS devices," *Indian Journal of Pure and Applied Physics*, vol. 45, pp. 358-367, 2007.

[71] N. C. MacDonald, L. Y. Chen, J. J. Yao, Z. L. Zhang, J.A. Mcmillan, and D. C. Thomas, "Selective chemical vapor deposition of tungsten for Microelectromechanical systems," *Sensors and Actuators*, vol. 20, no. 15, pp. 123-133, Nov. 1989, doi: 10.1016/0250-6874(89)87110-0.

[72] P. J. French and P. M. Sarro, "Surface versus bulk micromachining: the contest for suitable applications," *Journal of Micromechanics and Microengineering*, vol. 8, no. 2, pp. 45-53, 1998, doi: 10.1088/0960-1317/8/2/002/meta.

[73] G. Kovacs, *Micromachined Transducers Sourcebook*. Boston, Mass.: Mcgraw-Hill, 1998.

[74] K. E. Petersen, "Silicon as a mechanical material," in *Proceedings of the IEEE*, vol. 70, no. 5, May 1982, pp. 420-457, doi: 10.1109/PROC.1982.12331.

[75] A. De Luca, "SOI Smart Multi-Sensor Platform for Harsh Environment Applications," PhD, University of Cambridge, (2015).

[76] F. Laermer and A. Schilp, "Method of Anisotropically Etching Silicon, " German Patent DE4241045A, 1994.

[77] G. R. Liu, and S. S. Quek. *The Finite Element Method: a Practical Course*. Oxford, Boston: Butterworth-Heinemann, 2003.

[78] O. C. Zienkiewicz, R. L. Taylor, and J. Z. Zhu, *The Finite Element Method, Its Basis and Fundamentals*. (sixth ed.), Elsevier, Oxford, 2005.

[79] E. Barkanov, "Introduction to the Finite Element Method, " Institute of Materials and Structures - Faculty of Civil Engineering, Riga Technical University, 2001.

[80] M. Kuczmann, "Overview of the Finite Element Method," *Acta Technica*

Jaurinensis, 2015, doi: 8. 347. 10.14513/actatechjaur. v8.n4.393.

[81] COMSOL Multiphysics. "Application Gallery," (2021). Accessed Aug. 2021. [Online]. Available: https://uk.comsol.com/models.

[82] A. Rivai, O. Bapokutty, and C. Wai, "Modelling optimization involving different types of elements in finite element analysis," *IOP Conference Series: Materials Science and Engineering*. 2013, doi: 50. 10.1088/1757-899X/50/1/012036.

[83] S. Deepti, B. Dorin, J. Ortego, A. Giovanna, and S. Cristina, "Numerical modelling of continuous flow microwave heating: A critical Comparison of COMSOL and ANSYS," *Journal of microwave power and electromagnetic energy.* vol. 44. pp. 187-97, 2010. doi: 10.1080/08327823.2010.11689787.

[84] M. Feuchter, *Investigations on Joule heating applications by multiphysical continuum simulations in nanoscale systems.* Saint Philip Street Press, 2014.

[85] Z. Bi, "Chapter 9 – Heat Transfer Problem," *Finite Element Analysis Applications*, Academic Press, 2018, Pages 341-377.

[86] H. Austerlitz, *Data Acquisition Techniques Using PCs (Second Edition)*, Academic Press, Nov. 2003, pp.142-190.

[87] Y. Dai, S. Z. Ali, R. Hopper, C. Falco, P. Pandey, C. Oxley, D. Popa, and F. Udrea, "Crosstalk Analysis of a CMOS Single Membrane Thermopile Detector Array," *Sensors*, vol. 20, no. 9, 2020, doi: 10.3390/s20092573.

[88] F. J. DiSalvo, "Thermoelectric Cooling and Power Generation," *Science*, vol. 285, pp. 703-706, Jul. 1999, doi: 10.1126/science.285.5428.703.

[89] R. Hopper, S. Z. Ali, S. Boual, A. D. Luca, Y. Dai, D. Popa, and F. Udrea, "A CMOS-Based Thermopile Array Fabricated on a Single SiO2 Membrane," in *Proc. EUROSENSORS 2018*, Sep. 2018, doi: 10.3390/proceedings2130878.

[90] Texas Instruments. "LMP93601 Low-Noise, High Gain, 3-Channel AFE for Thermopile Sensors," (2014). Available: https://www.ti.com/product/LMP93601. Accessed: Aug. 2021.

[91] Texas Instruments. "LMP93601 EVM User Guide," (2014). Available: https://www.ti.com/product/LMP93601. Accessed: Aug. 2021.

[92] D. Popa, S. Z. Ali, R. Hopper, Y. Dai, and F. Udrea, "Smart CMOS mid-infrared sensor array," *Optics Letters*, vol. 44, pp. 4111-4114, 2019, doi: 10.1364/OL.44.004111.

[93] A. Graf, M. Arndt, M. Sauer and G. Gerlach, "Review of micromachined thermopiles for infrared detection," *Measurement Science and Technology*, vol. 18, no. 7, pp. R59-R75, May 2007.

[94] P. W. Kruse. *Uncooled Thermal Imaging: Arrays, Systems, and Applications,* WA, USA, SPIE Tutorial Texts, SPIE Press: Bellingham, 2001.

[95] A. D. Oliver and K. D. Wise, "A 1024-element bulk-micromachined thermopile infrared imaging array," *Sensors and Actuators A: Physical*, vol. 73, pp. 222-231, Jul. 1999, doi: 10.1016/S0924-4247(98)00276-3.

[96] A. Schaufelbuchl et al., "256-pixel CMOS-integrated thermoelectric infrared sensor array," in *Technical Digest. MEMS 14th IEEE International Conference on Micro Electro Mechanical Systems (Cat. No.01CH37090)*, Interlaken, Switzerland, 2001, pp. 200-203, doi: 10.1109/MEMSYS.2001.906513.

[97] G. Bradski and A. Kaehler, *Learning OpenCV 3 Computer Vision in C++ with the OpenCV Library*, O'Reilly Media, 2016.

[98] S. P. Yushanov, L. T. Gritter, J. S. Crompton and K. C. Koppenhoefer, "Multiphysics analysis of thermoelectric phenomena," In *Proceedings of the 2011 Comsol Conference*, Boston, MA, USA, 13–15 Oct. 2011.

[99] A. Bao, C. Lei, H. Mao, R. Li and Y. Guan, "Study on a high performance MEMS infrared thermopile detector," *Micromachines*, Dec. 2019, doi:10.3390/mi10120877

[100] E. Kessler, U. Dillner, V. Baier and J. Muller, "A 256 pixel linear thermopile array using materials with high thermoelectric efficiency," in *XVI ICT '97. Proceedings ICT'97. 16th International Conference on Thermoelectrics (Cat. No.97TH8291)*, Dresden, Germany, pp. 734-737, 1997, doi: 10.1109/ICT.1997.667634.

[101] C. Falco and F. Udrea, "On the application of a numerical model to improve the

accuracy of the seebeck coefficient in CMOS materials," in *2017 IEEE SENSORS*, Glasgow, 2017, pp. 1-3, doi: 10.1109/ICSENS.2017.8233900.

[102] Y. Li, H. Zhou, T. Li, Y. Wang, Y. Liu and Y. Wang, "CMOS-compatible 8×2 thermopile array, " *Sensors and Actuators A: Physical*, vol. 161, pp.120-126, 2010, doi: 10.1016/j.sna.2010.04.026.

[103] A. Eatemadi *et al.*, "Carbon nanotubes: properties, synthesis, purification, and medical applications,s" *Nanoscale Research Letters*, vol. 9, no. 393, 2014, doi: 10.1186/1556-276X-9-393.

[104] A. De Luca, M. T. Cole, A. Fasoli, S.Z. Ali, F. Udrea and W.I. Milne, "Enhanced infra-red emission from sub-millimeter microelectromechanical systems micro hotplates via inkjet deposited carbon nanoparticles and fullerenes," *Journal of Applied Physics*, vol. 113, no. 214907, Jun. 2013, doi: 10.1063/1.4809546.

[105] A. De Luca, M. T. Cole, R. H. Hopper, S. Boual and J. H.Warner, A.R. Robertson, S. Z. Ali, F. Udrea, J. W. Gardner, and W. I. Milne, "Enhanced spectroscopic gas sensors using in-situ grown carbon nanotubes," *Journal of Applied Physics*, vol. 106, no. 194101. May 2015, doi: 10.1063/1.4921170.

[106] M. Wick, H. Hedler, and H. Seidel, "Design and Analysis of Novel Micromachined Thermocouples with Vertical Free-Standing High-Aspect-Ratio Geometry," *Journal of Electronic Materials*, vol. 44, pp. 2146–2150, 2015, doi: 10.1007/s11664-015-3721-9.

[107] E. Verheyen, A. Erbslöh, R. Viga and H. Vogt, "Simulation Results of Prospective Next Generation 3-D Thermopile Sensor and Array Circuitry Options," *IEEE Sensors Letters*, vol. 2, no. 2, pp. 1-4, Jun. 2018, doi: 10.1109/LSENS.2018.2829265.

[108] E. Verheyen, T. Kleinfeld, D.Weiler, and H. Vogt, "Integrated thermoelectric structure, method for manufacturing an integrated thermoelectric structure, method for operating same as a detector, thermoelectric generator and thermoelectric peltier element," U.S. Patent 2017/0317260 A1, Nov. 2017.

[109] K. M. Muckensturm et al., "Measurement results of a 12 μm pixel size microbolometer array based on a novel thermally isolating structure using a 17 μm ROIC, " in *Proceedings of SPIE*, vol. 9819, 2016, doi: 10.1117/12.2223608.