

# A Design of a Low-Delay DPWM Control Circuit for DC-DC Converter

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**Abstract** - A proposed design of a low-cost digital pulse width modulation (DPWM) control circuit for non-isolated DC-DC converter without A/D converter is described. Also, proposed real-time PID control technique for DPWM is described. Some experimental results and simulation results are revealed the proposed circuit and scheme. The purpose of this research is striking a balance between minimizing cost increase by digitalizing of the control circuit of DC-DC converter and speeding up the control circuit.

## I. INTRODUCTION

Recently, power management has been introduced to improve the power efficiency of Micro Processing Unit (MPUs), Field Programmable Gate Array (FPGAs) and Digital Signal Processor (DSPs). The power management system includes a full operation mode, standby mode, and sleep mode. The clock frequency, core voltage and/or core current are changed in each mode accordingly. As a result, the output current of the point-of-load (POL) DC-DC converters is intermittent and has a high slew rate. A low output voltage, a large output current and a high speed response are required for the POL [1]. In such a condition for the control circuit, highly accurate and high-speed control demands that the tolerance of the output voltage becomes internally severe, advanced by speed-up and lowering of the voltage of the MPUs, FPGAs and DSPs [2,3]. A general control method is pulse width modulation (PWM) control with PID. Generally, such control circuits are composed with analog circuits and/or simple combination digital circuits.

In these days, robustness or flexible controls for versatile

conditions are demanded which cannot accomplished with analog control circuit. For the control purpose, DPWM control is a one of appropriate technique[4-6].

Digital control or DPWM can accomplish robust and flexible power control with soft-tuned parameters and will become popular control technique.

Although, there are some disadvantages in cost and speed, against analog control circuit.

Especially, A/D converter circuit, which doesn't need for analog control, is the one of the key circuits which effects on cost and speed. Generally, A/D converter is located in front of digital controller as shown in Fig. 1. Therefore, the transition speed of A/D converter directly effects on the response speed of the control circuit. And, the cost and speed are always trade off problem. This problem is especially serious in POL DC-DC converter which is required to design the control circuit in relatively low-cost and high speed control response. Moreover, generally, there is sample-hold circuit in front of A/D converter which degrades the response speed.

A delay in any feedback system degrades the stability and damping of the system [7]. Especially, in DPWM, if a total of the delays described in above become larger than on-term of one switching period, a factor of A/D converter becomes  $V_q/Z$  shown in Fig. 2 where  $V_q$  is a coefficient constant.

An objective of this paper is to design high speed and low cost voltage sensing circuit for DPWM control circuit for DC-DC converter. And, also real-time PID control method is proposed. In Sec. II, the details of proposed system are described. In Sec. III, the some characteristics of the system are confirmed with experimental results. Finally, in Sec. IV, the summary is described.

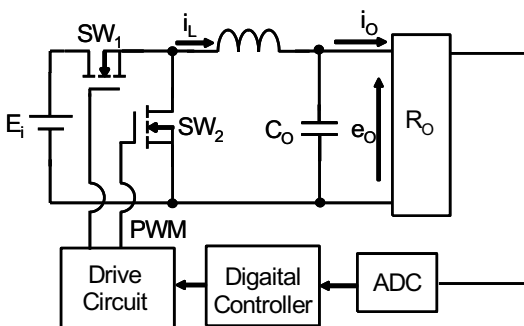


Fig. 1. Common digital control DC-DC converter.

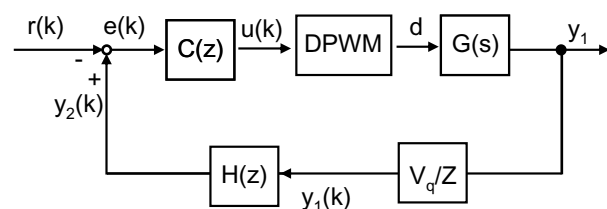


Fig. 2 Control System.

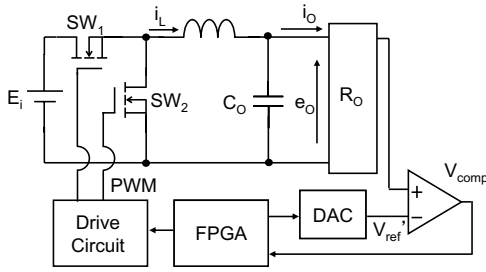


Fig. 3 Proposed Digital PWM Control DC-DC converter.

## II. PROPOSED SYSTEM

We propose a scheme of a digital control and DPWM circuit for DC-DC converter without A/D converter shown in Figs.3 and 4. In this proposed control circuit, most components are digital components. Analog components for the control circuit are essentially only D/A converter and analog comparator. Theoretical waveforms of each part are shown in Fig. 5.

The control circuit is composed of three major blocks.

### A. Analog-Timing Converter (ATC)

The first block is ATC block which detects the output voltage  $e_o$  and outputs the detected signal to latch register. The maximum output value of D/A converter DAC is set as a sum of the output reference voltage of DC-DC converter  $V_{ref}$  and margin  $\alpha(>0)$ . A digital staircase waveform data, pre-stored in memory Memory1, is output to DAC synchronized with a system clock, and converted analog staircase waveforms  $V_{ref}'$  is compared with  $e_o$ . As soon as  $V_{ref}' > e_o$ , the comparator out-

puts high.

### B. PID control with Look-up Table

$u(k)$  which is output from Memory2 is calculated by general PID digital control laws as

$$u(k) = u_{Ref} + K_P e(k) + K_I n_I(k) + K_D (e(k) - e(k-1)) \quad (1)$$

where  $u_{Ref}$  is a reference value of  $u(k)$ ,  $e(k)$  is an digitalized error value between  $r$  which is digitalized reference voltage  $V_{ref}$  in switching term  $k$ , and  $n_I(k) = n_I(k-1) + e(k)$ .  $K_P$ ,  $K_I$  and  $K_D$  are a proportional gain, an integral gain and an derivative gain, respectively.

Equation (1) can be transformed to

$$u(k) = u_{Ref} - (K_P + K_I)r + A\{y_2(k) + \frac{K_I}{A}n_I(k-1) - \frac{K_D}{A}y_2(k-1)\} \quad (2)$$

where  $A = K_P + K_I + K_D$  and  $y_2(k)$  is digitalized output voltage  $e_o$  in switching period  $k$ .

In Fig. 4,

$$a = \frac{K_I}{A}n_I(k-1) \quad (3)$$

$$b = \frac{K_D}{A}y_2(k-1) \quad (4)$$

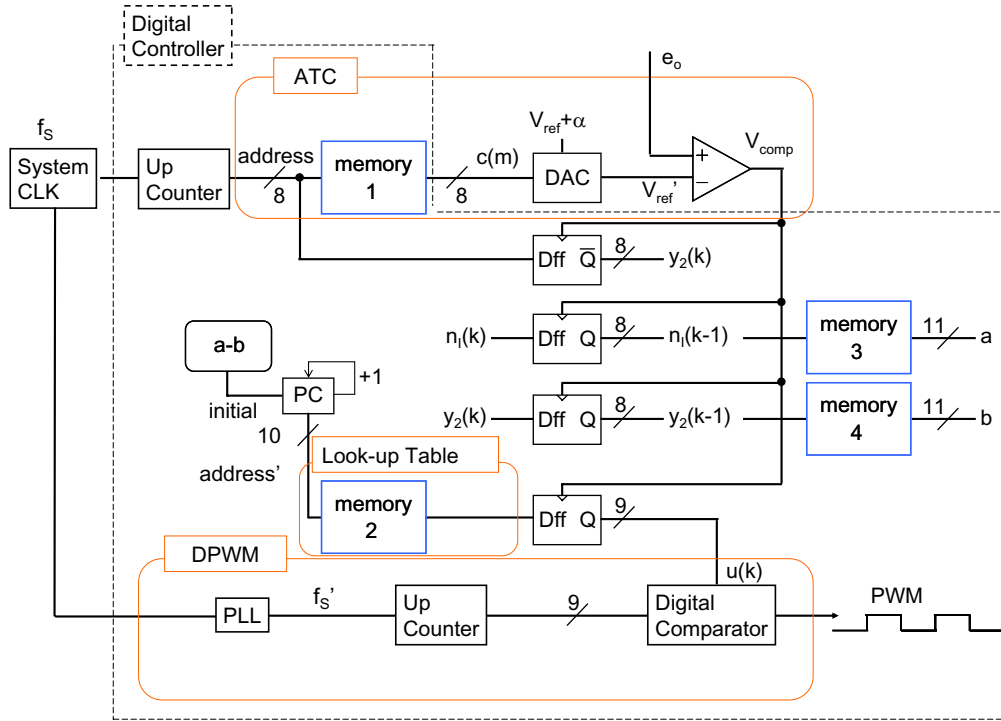


Fig.4. Proposed digital control circuit.

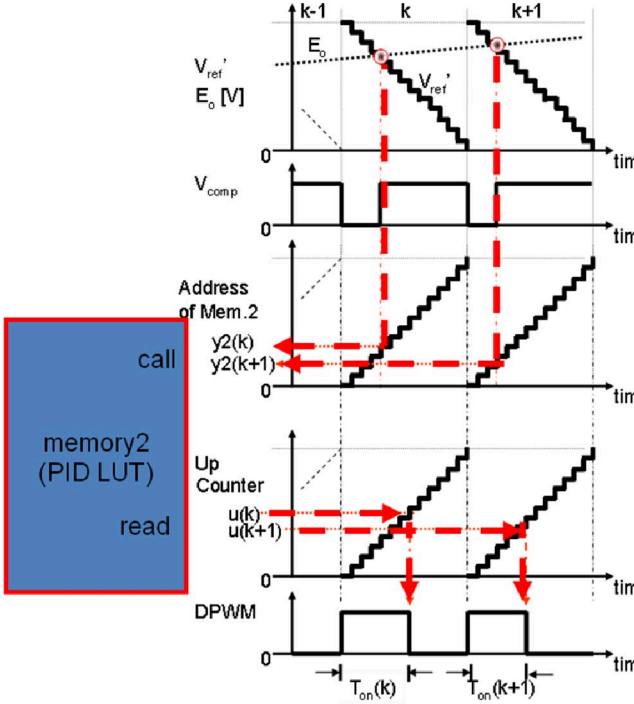


Fig.5. Theoretical waveforms.

Memory3 and Memory4 store  $a$  and  $b$ , respectively.

In (2),  $a-b$  in the term  $k$  is pre-calculated in the term  $k-1$  and the obtained value becomes the initial value of programmable counter PC of the term  $k$ . And,  $address'$  which indicates address of Memory2 is incremented with system clock and  $u(k)$  is called from Memory2, simultaneously.

$$address' = y_2(k) + a - b. \quad (5)$$

From (2) and (5),

$$u(k) = u_{Ref} - (K_P + K_I)r + A\{address'\} \quad (6)$$

Therefore,  $u(k)$  is determined as soon as  $y_2(k)$  is detected.

### C. DPWM

In this system, on-term  $T_{on}(k)$  of DPWM signal is decided by  $u(k)$ , which is normalized  $T_{on}(k)$ , and system clock frequency  $f_s$ 's

$$T_{on}(k) = u(k)/f_s' \quad (7)$$

$u(k)$  is decided by latched value of Memory2.

In parallel with the processing of ATC block, the  $u(k)$  is called with system clock and latched by ATC output as trigger.

## II. PROTOTYPE CIRCUIT EXPERIMENTS

### A. Experimental Conditions

Some experiments are performed to verify the scheme. The proposed controller with prototype circuit is shown in Fig. 6. The digital controller part is designed in FPGA Altera Stratix with Quartus II. 149 logic elements and 1 PLL block are used. All memory blocks, Memory1, Memory2, Memory3 and Memory4, are including in the logic elements. Intersil CA3338MZ is used as 8bit DAC. National Semiconductor LM360N is used as analog comparator.

The DC-DC converter topology is basically same as Fig. 2. The experimental conditions are shown in Table 1.

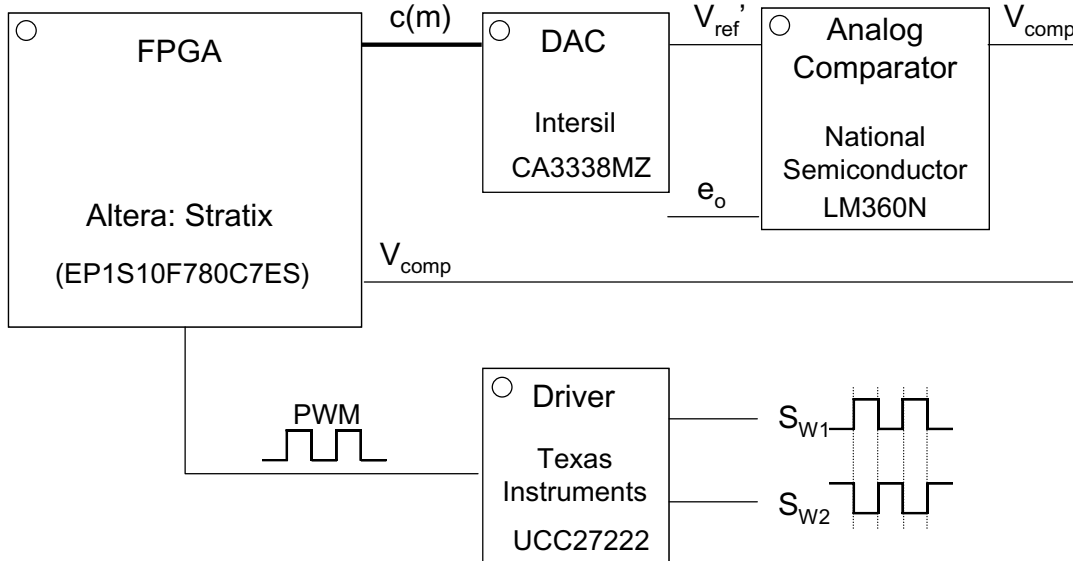


Fig. 6. Prototype proposed control circuit.

TABLE I  
EXPERIMENTAL CONDITIONS

Input voltage $E_i$	2-8V
Output voltage $E_o$	1.5V
Output current $I_o$	0-5A
Switching frequency $f_s$	120kHz
Choke inductor $L$	17 $\mu$ F
Output capacitor $C_o$	500 $\mu$ F
Proportional gain $K_p$	1-5
Derivative gain $K_D$	1,3,5
Integral gain $K_I$	0.1-0.5
$V_{ref} + \alpha$	1.7V
System CLK	33.3MHz

### B. Experimental Results

The experimental waveforms are shown in Fig. 7.

$i_o$ - $e_o$  characteristics are shown in Fig. 8.  $e_o$  is regulated in 5% between 0A to 5A of  $I_o$  at  $k_p=5$  and  $k_i=0.5$ .

$E_i$ - $e_o$  characteristics are shown in Fig. 9.  $e_o$  is regulated in 5% between 4V to 8V of rated  $E_i$  at  $k_p=5$  and  $k_i=0.5$ .

### C. Propagation Delay Reduction

D/A converter DAC and analog voltage comparator have a conversion time or propagation delay time  $T_d$  shown in Fig. 10(a). The delay makes decision error of  $y_2[k]$ . This degrades the stability and damping of the system. The one method of

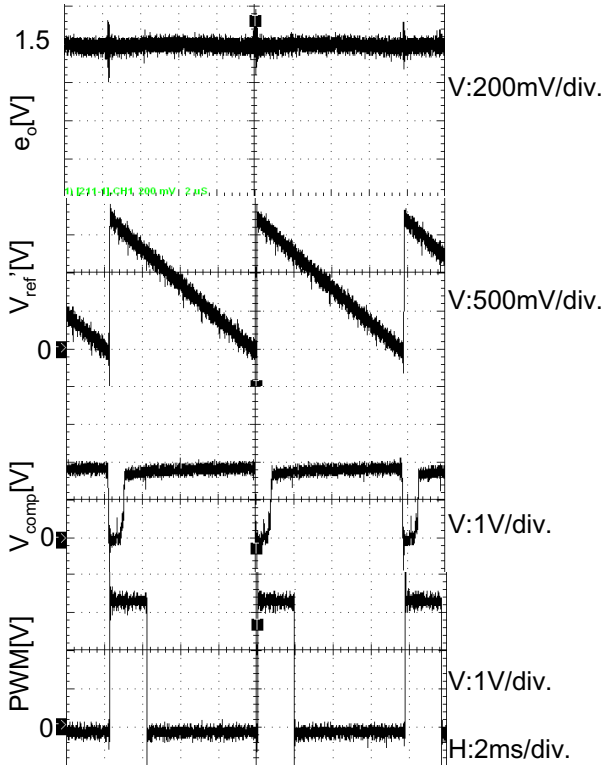


Fig. 7 Experimental waveforms.

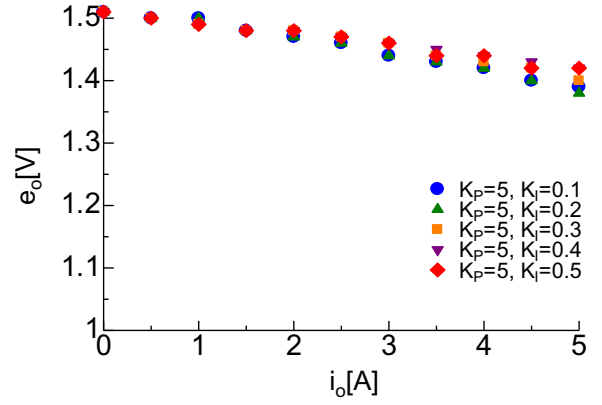


Fig. 8  $i_o$ - $e_o$ .

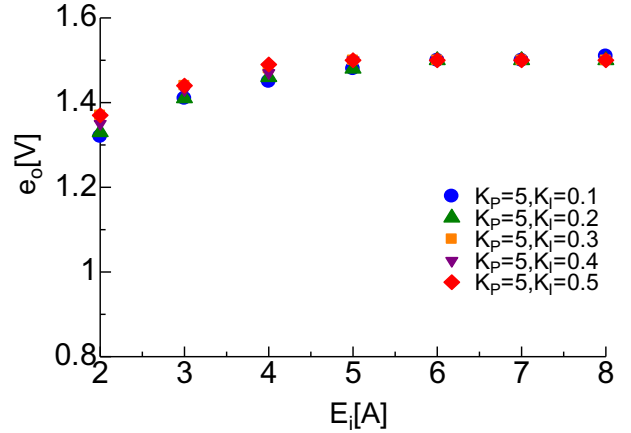


Fig. 9.  $E_i$ - $e_o$ .

suppressing influences of the delay, which is applied in this experiment, is shifting forward the stored digital staircase waveform data to appropriate quantities shown in Fig. 10(a). The shifting quantities is estimated by follow equation

$$(\text{Shifting quantity}) = T_d * f_s' \quad (8)$$

Figures 10(b) and (c) show the propagation delay from transition of  $C_m[0]$  to the transition of  $V_{comp}$ . From the results, it can be seen that the propagation delay time is reduced with the adjustment method. The shifting quantity was 4.

### D. The Output Voltage Detection Timing

The output voltage detection timing is variable in this system. To confirm an influence of the detection timing to static characteristic, the experiments are done with some detection timing parameters. The parameters are 0, 2, 5 and 10% shown Fig. 11.

The 0% means the detection timing is at the transition point from  $T_{off}$  to  $T_{on}$ . At this timing, the detection accuracy will be degenerated by the surge voltage.

Comparing with 0% and the others, there is 1% output voltage difference. The results show the availability to have the margin of detection timing which prevents one-sample time delay.

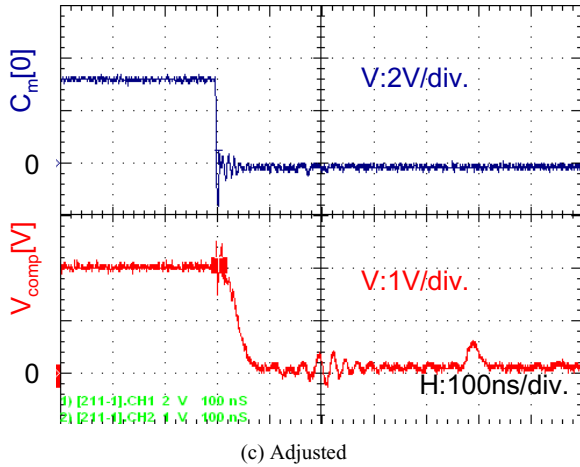
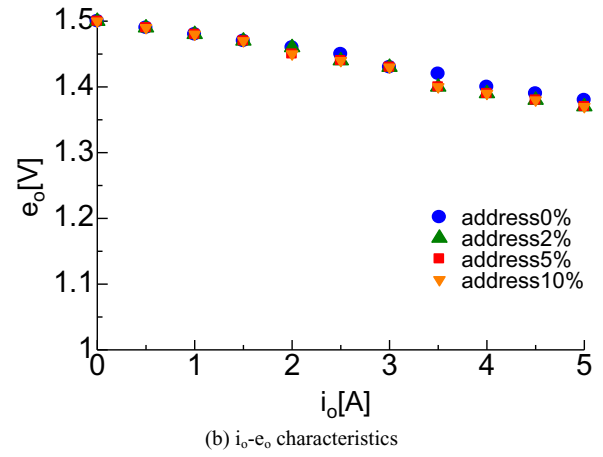
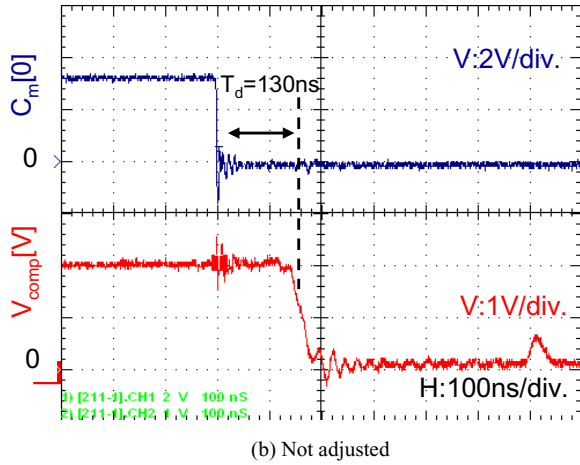
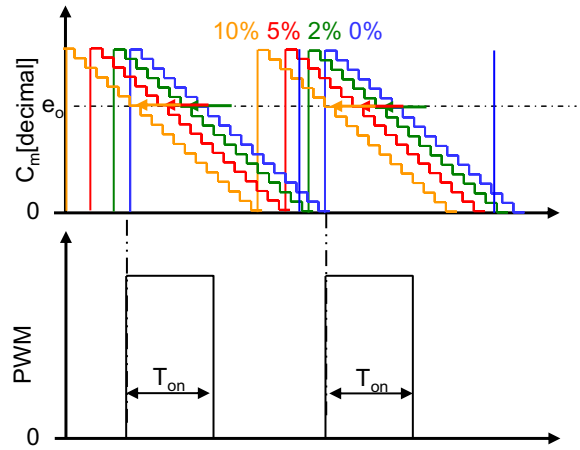
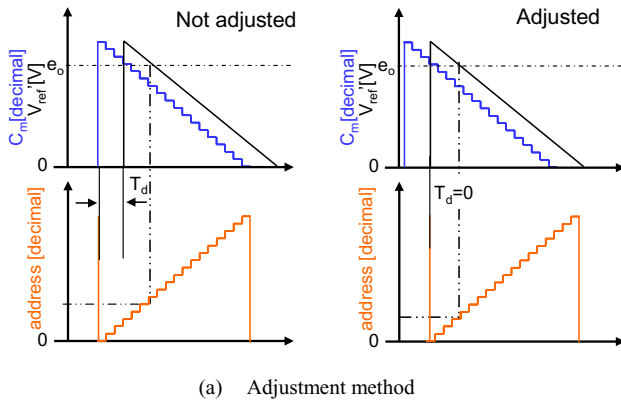


Fig. 10 Propagation delay reduction.

### E. Dynamic Characteristics

Figure 12 shows dynamic characteristic with load current  $i_o$  changing from 0.5A to 3A with 250mA/ $\mu$ sec. Fig. 12(a) The load current changing is evaluated with KIKUSUI PLZ164WA.

Fig. 11 The output voltage detection timing.

From Figs. 12(a), (b) and (c), the maximum voltage drop were 275mV, 168mV, 176mV and the settling time were 210 $\mu$ s, 88 $\mu$ s, 67 $\mu$ s, respectively.

## III. SUMMARY

In this paper, the effectiveness of the proposed digital PWM for DC-DC converter without A/D converter is described.

The circuit is composed with a simple design and digital components, and without A/D converter.

From the experimental results with prototype circuit, the total propagation delay time was suppressed to 30ns. And it was shown that the digital PID control was achieved within this time.

We are planning to design a custom digital LSI of the control circuit with an appropriate size and cost, and to apply to high speed switching control or multi-phase control.

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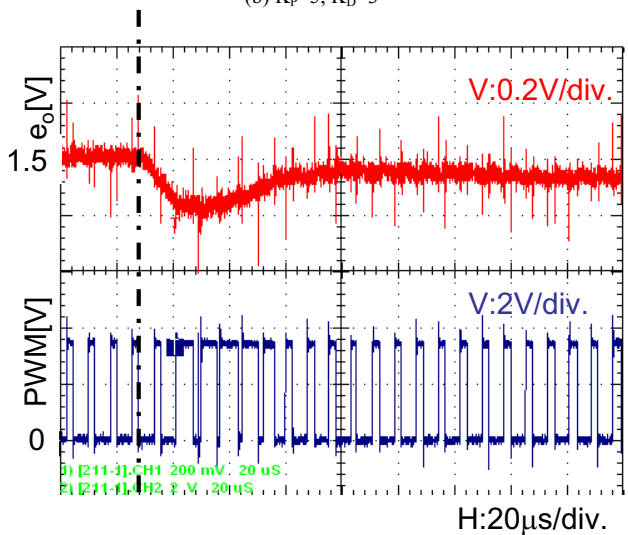
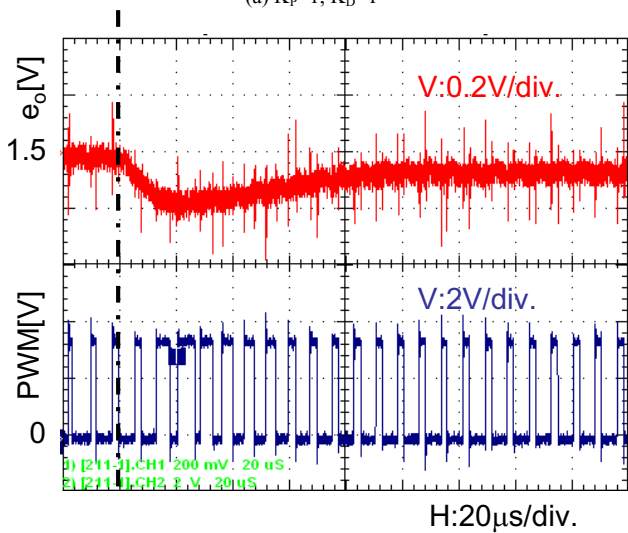
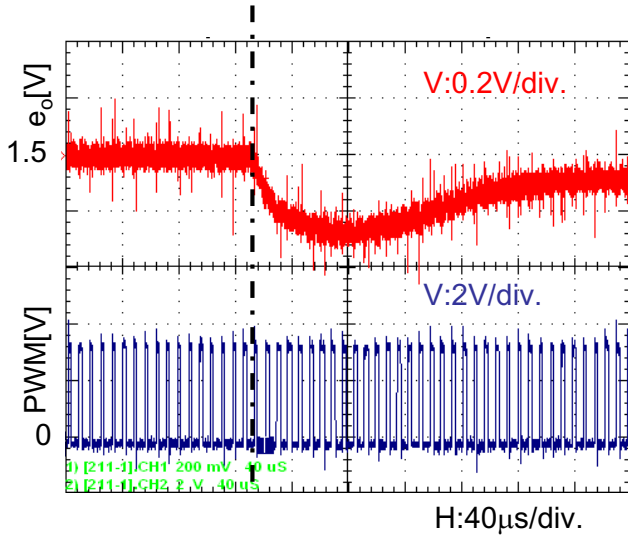


Figure 12 Dynamic characteristics.