

# A CMOS Analog LSI Design for 5GHz MIMO System

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**Abstract**—In this paper, we discuss linear power amplifier and RC polyphase filter design in 90nm CMOS process which dominate QoS in high throughput wireless communication system. From the theoretical analysis, we show that only class A operation can be a linear power amplifier and its maximum drain efficiency reaches 67[%] in CMOS process. We also propose an RC polyphase filter (PPF) design using frequency transformation from the prototype LPF and evaluate its parasitic effect. Both power amplifier and RC PPF are fabricated using TSMC 90nm process.

## I. INTRODUCTION

Recently, MIMO systems that can achieve transmission speed of several hundreds of Mbps and above have attracted interest due to the demand for high throughput data transmission in a wireless communication network[1]. In the case of wireless LAN, IEEE 802.11n and 802.11VHT provides methods to realize such a high throughput. Direct conversion architecture is often adopted for such application due to its possibility of 1-chip implementation in standard CMOS process.

In such transceiver system, power amplifier stage in transmitter section and polyphase filter (PPF) in local oscillator (LO) section dominate the overall throughput as shown in Fig.1. Less linearity of power amplifier causes higher order intermodulation and consequently destroys orthogonality between subcarriers in OFDM signals. Phase error in quadrature LO signal causes crosstalks between I and Q signals and results unavoidable demodulation errors. Therefore, high-linearity power amplifier and accurate quadrature LO signal are essential building blocks to realize high-speed wireless communication.

In this paper, we discuss linear power amplifier and RC PPF design in 90nm CMOS process.

At first, MOS power amplifier is analyzed theoretically and we find that only class-A amplifier can be used for linear amplification and its maximum drain efficiency exceeds 50[%]. It is also shown that the output saturation is caused by the transfer of transistor operation from saturation region to triode one and we derive maximum drive level. Up to 20.1[dBm] linear output is obtained from simulation results for a 5GHz PA with push-pull and series-combining transformer configuration.

For RC PPF, we discuss evaluation results on parasitic elements which appear in LSI implementation. Filter response

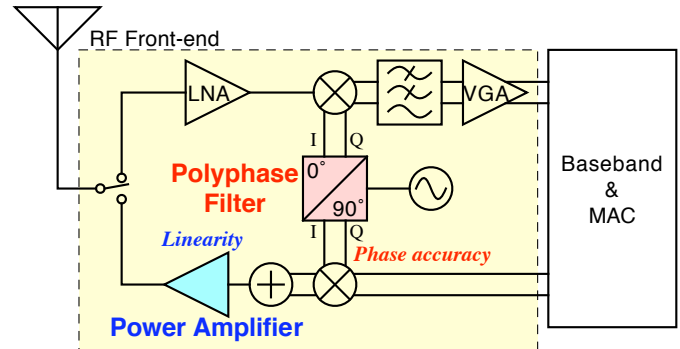


Fig. 1. System diagram of RF transceiver chip.

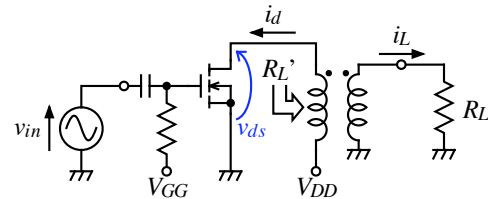


Fig. 2. Simple MOS power amplifier with transformer load.

and Packet Error Ratio (PER) are analyzed in terms of parasitic capacitance, and performance degradation due to parasitic resistors extracted from layout is also evaluated.

## II. MOS LINEAR POWER AMPLIFIERS

### A. Operating class

Let us consider a simple MOS power amplifier with transformer load as shown in Fig.2. In general, a MOS transistor which works in saturation region is characterized by the following equation:

$$I_D = \frac{\mu C_{ox}}{2} \frac{W}{L} (V_{GS} - V_{TH})^2, \quad (1)$$

where  $\mu$ ,  $C_{ox}$ ,  $W$ ,  $L$  and  $V_{TH}$  are electron mobility, gate oxide capacitance, channel width, channel length and threshold voltage, respectively. Drain current waveforms for a single sinusoid excitation under various operation classes are then shown in Fig.3.

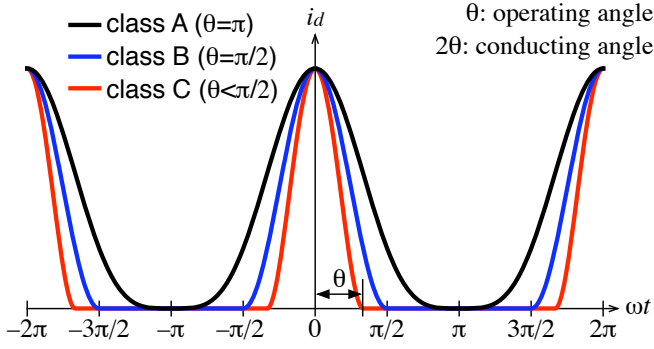


Fig. 3. Drain currents for three type of operation class.

By analyzing those current in Fourier series expansion, we have fundamental component as

$$a_1 = \frac{KV^2}{2\pi} \left( 3 \sin \theta + \frac{1}{3} \sin 3\theta \right) + \frac{2KV_bV}{\pi} \left( \theta + \frac{\sin 2\theta}{2} \right) + \frac{2KV_b^2V}{\pi} \sin \theta, \quad (2)$$

where  $K = \frac{\mu C_{ox}}{2} \frac{W}{L}$  is the transconductance parameter,  $V$ ,  $V_b$  and  $\theta$  are input amplitude, bias voltage and operating angle, respectively[2]. This means that only class A amplifier ( $\theta = \pi$ ) has capability of linear amplification: the other operation classes, even in the class AB, have the term proportional to the square of input amplitude in its output fundamental component.

### B. Drain current saturation

Increasing the input amplitude, increasing drain current and it decrease drain-source voltage  $v_{ds}$ , and finally the transistor operation goes into triode region. Therefore, there is a boundary voltage between saturation and triode region which is given by

$$V_{GS}' = \frac{-1 + \sqrt{1 + 4KR_L V_{DD}}}{2KR_L'} + V_{TH}, \quad (3)$$

where  $R_L'$  is drain load. Then the  $V_{GS}-I_d$  characteristics can be drawn as shown in Fig.4. From this figure, we can conclude that the output saturation is caused by operation mode transfer from saturation region to triode one.

Fig.4 also shows that the operating point of MOS class A amplifier should be set at the quarter of maximum drain current, not at the half of that. Many literatures[3], [4] follow traditional analysis in the era of vacuum tubes or bipolar transistor, where the plate or collector current waveform is based on sinusoid.

### C. Push-pull configuration and drain efficiency

From the discussion in previous subsections, only class A operation can be used as a linear amplifier. However, there exists 2nd order harmonic in the drain current. Therefore, we

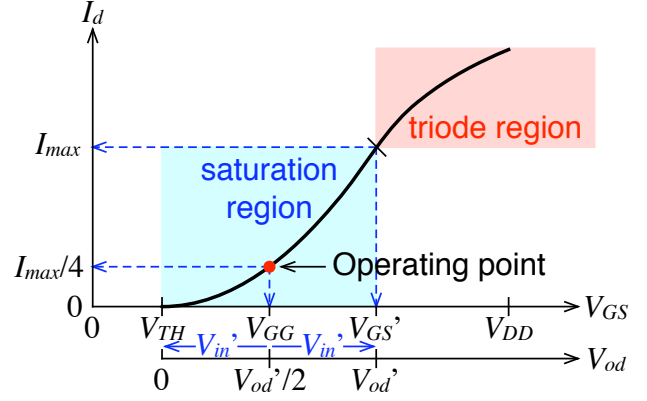


Fig. 4. The  $V_{GS}-I_d$  characteristics of transformer load MOS PA.

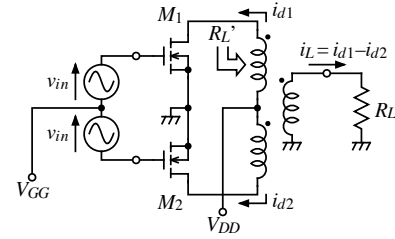


Fig. 5. Push-pull configuration.

adopt push-pull configuration shown in Fig.5 to cancel 2nd order harmonic.

Drain efficiency, defined as

$$\eta = \frac{P_{RF}}{P_{DC}} = \frac{P_{RF}}{V_{DD}(i_{d1} + i_{d2})}, \quad (4)$$

where  $P_{RF}$  and  $P_{DC}$  are output power and DC supply power, respectively, is a kind of figure of merit in power amplifier. Well known 50[%] efficiency value in class A amplifier seems incorrect in MOS transistor amplifier case as long as we assume its square-law characteristics, whereas the literatures[3], [4], [5] assume sinusoidal collector/drain current.

Drain supply current  $I_{DC}$  is given by

$$\begin{aligned} I_{DC} &= \overline{i_{d1} + i_{d2}} \\ &= \frac{K}{\pi} \int_{-\pi}^{\pi} V^2 \cos^2 \omega t + 2V_{GG}V \cos \omega t + V_{GG}^2 d\omega t \\ &= 3KV^2. \end{aligned} \quad (5)$$

Therefore, maximum drain efficiency of MOS push-pull power amplifier  $\eta_{max}$  is calculated as

$$\eta_{max} = \frac{\frac{1}{2}4KV^2V_{DD}}{3KV^2V_{DD}} = \frac{2}{3}. \quad (6)$$

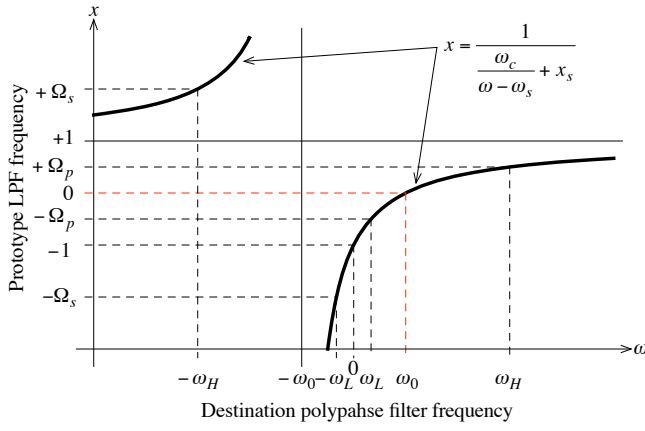


Fig. 6. BLLT for polyphase transfer function design.

### III. RC POLYPHASE FILTER WITH BUTTERWORTH CHARACTERISTICS

#### A. Transfer function design using BLLT

The bilinear LP-LP transformation (BLLT) is a complex filter design method from the lowpass prototype;

$$x = -\frac{1}{-\frac{\omega_c}{\omega - \omega_s} - x_s} \quad (7)$$

where  $x$  and  $\omega$  are frequencies of prototype and destination filters,  $x_s$  and  $\omega_s$  are the shifting parameters and  $\omega_c$  is the scaling parameter, respectively[6].

Let  $\omega_0$ ,  $\omega_L$  and  $\omega_H$  be the center, the lower passband edge and the upper passband edge frequencies of the destination polyphase filter, and these have following relationship:

$$\omega_0 = \sqrt{\omega_L \omega_H}. \quad (8)$$

Similarly, let  $\Omega_p$  and  $\Omega_s$  be the passband and the stopband edge frequencies of the prototype LPF, and these are normalized by the following:

$$\sqrt{\Omega_p \Omega_s} = 1. \quad (9)$$

By allocating the BLLT frequency mapping as shown in Fig.6, we have

$$\left\{ \begin{array}{l} 1 = \frac{1}{\frac{\omega_c}{\pm\infty - \omega_s} + x_s} \\ 0 = \frac{1}{\frac{\omega_c}{\omega_0 - \omega_s} + x_s} \\ -1 = \frac{1}{\frac{\omega_c}{0 - \omega_s} + x_s} \end{array} \right. \quad (10)$$

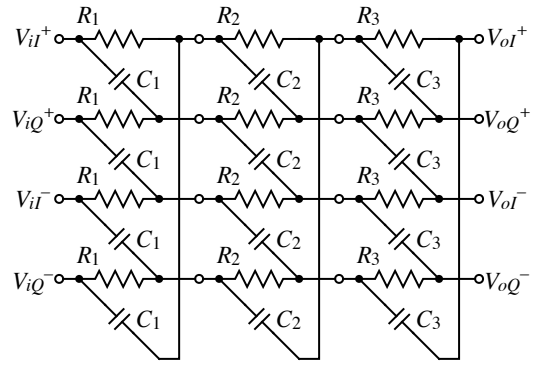


Fig. 7. 3rd order RC polyphase filter.

TABLE I  
COMPONENT VALUES FOR OUR DESIGN.

Stage	1	2	3
$R_i [\Omega]$	28.90	57.80	173.4
$C_i [\text{pF}]$	1.000	0.5000	0.1667

and it yields

$$\begin{cases} x_s = 1 \\ \omega_s = \omega_0 \\ \omega_c = 2\omega_0. \end{cases} \quad (11)$$

From eq.(11), we finally have a relationship between prototype and resultant polyphase frequency variables:

$$x = \frac{\omega - \omega_0}{\omega + \omega_0} \quad \text{or} \quad \frac{\omega}{\omega_0} = \frac{1+x}{1-x}. \quad (12)$$

By using this method, we transform polyphase filter specifications into the prototype LPF which design is well known and easy. Once the prototype LPF is determined, we transform back the pole and zero locations of the prototype into the complex filter domain to calculate polyphase transfer function[7].

#### B. 5GHz Polyphase Filter Design

Our design specifications are:

- Passband: 4.5 ~ 6.5[GHz]
- Attenuation: smaller than -55[dB] at -6.5 ~ -4.5[GHz]
- Maximally flat or Butterworth characteristics.

Since we assume Butterworth filter for its response, the derived polyphase transfer function can be implemented in RC polyphase filter[7] shown in Fig.7.

The transfer function of our design can be obtained by the method discussed in the previous subsection in terms of poles and zeros. Also,  $F$  matrix calculation for the RC polyphase filter structure shown in Fig.7 gives its transfer function. Therefore, element values can be calculated by coefficient matching between both transfer functions. Calculated component values for our design are shown in Table I. Note that element value ratio is integer (for resistor, 1:2:6) and this property comes from the peculiarity of pole locations of 3rd order Butterworth LPF.

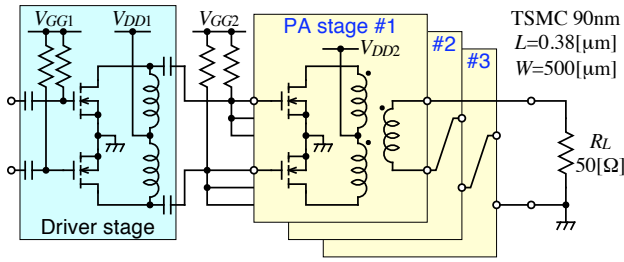


Fig. 8. Power amplifier schematic.

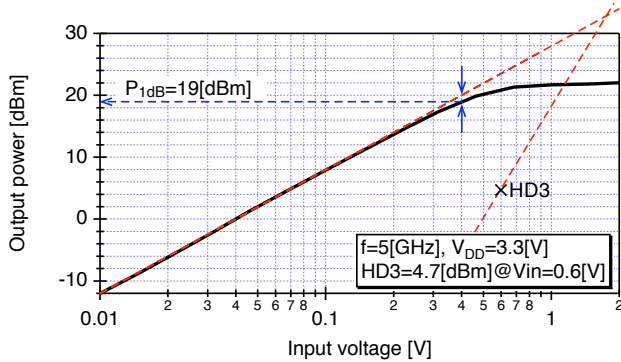


Fig. 9. Power amplifier response.

#### IV. TEST CHIP DESIGN IN 90NM PROCESS

##### A. Power amplifier design

Output power requirement for our design is 100[mW] at 5[GHz] band. We designed a push-pull amplifier with output transformer, however, simulated output is only 20[mW] due to insufficient transfer coefficient at the output transformer.

To overcome this drawback, we adopt series-combining transformer (SCT) technique[8], [9]. As shown in Fig.8, we connected 3 power amplifier sections in parallel and combined their output in series. Simulated output power (saturation) is greater than 100[mW] and 1[dB] compression output is 19[dBm].

Calculated drain efficiency is 24.7[%], however, it is better than conventional class A bias case (20.6[%]).

##### B. Polyphase filter design

The effect of parasitic resistance on polyphase filter response is shown in Fig.10. The figure shows that parasitic resistance of 10 $\Omega$  causes stopband attenuation degradation by 3.46[dB] below the specifications. In the case of 1 $\Omega$  and 5 $\Omega$ , design specifications are satisfied.

The effect of parasitic capacitance is shown in Fig.11. In terms of stopband attenuation, Fig.11 shows that the design specifications are satisfied in all cases of parasitic capacitance values. Note that the final stage of RC polyphase filter is most sensitive to parasitic capacitance due to its value.

We also investigate PER performance under the condition of 802.11n channel B environment with 600Mbps speed and 40MHz bandwidth shown in Table II. MATLAB simulation results are shown in Fig.12. In this figure, “Perfect” shows

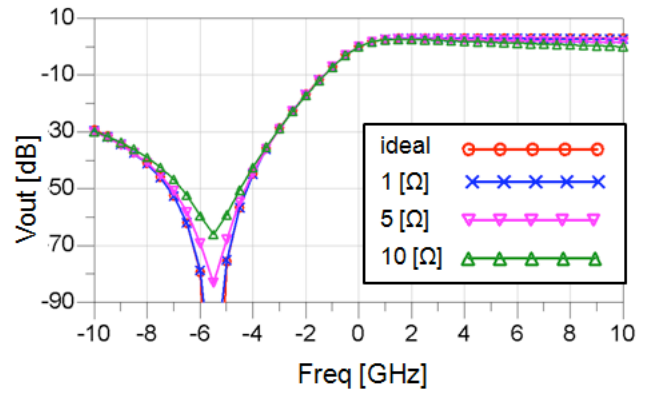


Fig. 10. Polyphase filter response with parasitic resistances.

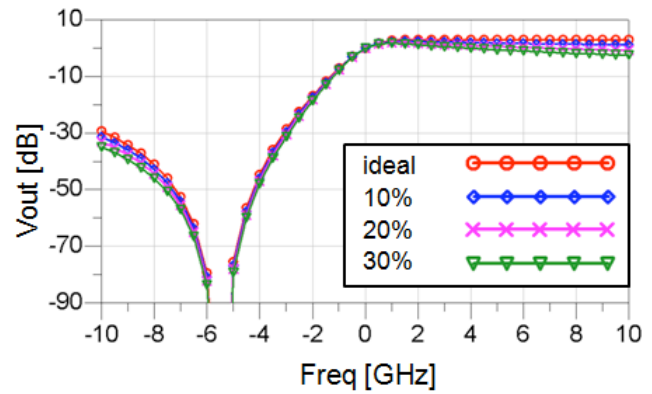


Fig. 11. Polyphase filter response with parasitic capacitances.

ideal I/O carrier case without phase error, “ideal” shows ideal (*i.e.* parasitic free) polyphase filter case and “30%” means polyphase filter with 30% parasitic capacitance case. The PER performance shows that the parasitic capacitors due to LSI implementation in the Butterworth RC polyphase filter does not affect 802.11n system performance[10].

##### C. Chip layout

Both power amplifier and polyphase filter are fabricated in TSMC 90nm process. For RC polyphase filter, bias resistors and output buffers are added to its schematic. Fig.13 shows microscope photograph of the test chip. Occupied areas are 1.2[mm<sup>2</sup>] for power amplifier and 0.36[mm<sup>2</sup>] for polyphase filter, respectively.

Spiral transformers and inductors consume most amount of the power amplifier area. Therefore, in actual 4  $\times$  4 MIMO

TABLE II  
SIMULATION CONDITIONS FOR PER ANALYSIS.

MIMO channel	B channel (indoor environment)
Channel width	40[MHz]
Data length	1000 [octets]
Data rate	600 [Mbps]
MCS	31

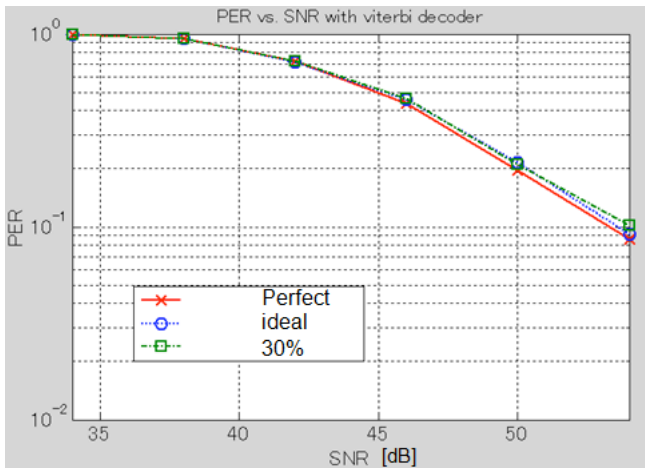


Fig. 12. Packet error ratio for 600Mbps MIMO channel.

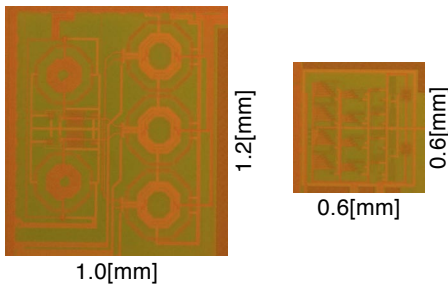


Fig. 13. Test chip view (left: PA, right: RC PPF).

RF chip design, we should consider separate power amplifier chip from other circuits.

Performance evaluation of the test chip is planned to carry out in this autumn.

## V. CONCLUSIONS

In this paper, we discuss linear power amplifier and RC polyphase filter design in 90nm CMOS process aimed for 5GHz  $4 \times 4$  MIMO transmission.

We analyze MOS power amplifier under square law condition. In such situation, only class-A amplifiers have capability of linear amplification and output saturation is caused by operation shift from saturation region to triode one. Test chip design results show that the output power of 100[mW] is obtained by using series-combining transformer technique.

For RC polyphase filter design, we develop a frequency transformation from the prototype LPF to design transfer function. Third order Butterworth RC polyphase filter for 5GHz band is evaluated and we found that parasitic capacitances does not affect 600Mbps MIMO system performance significantly.

Test chip evaluation will be made soon. Also, the entire transceiver chip design is further task. There are many theoretical subjects in RF circuit design as well as those concerning chip implementation. We hope those might be resolved in the near future.

## ACKNOWLEDGMENT

A part of this work is supported by Knowledge Cluster Initiative (The Second Stage), Ministry of Education, Culture, Sports, Science and Technology, Japan and cooperation of Agilent Technologies Japan, Ltd. through The VLSI Design and Education Center, University of Tokyo.

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