Accuracy Digital Control for Boost DC-DC Converter

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Abstract — This paper presents the accuracy digital control for the boost type dc-dc converter. The design of the A-D conversion timing and anti-aliasing filter's cut-off frequency is discussed to realize the accurate regulation characteristics and good dynamic characteristics.

I. INTRODUCTION

Recently, the concern with energy management in clean energy system has been growing. In this case, the boost converter is usually used in order to receive from the clean energy source, that is, solar cell, fuel cell and so forth because the input current of boost converter flows always continuously[1]-[4]. On the other hand, the high control-ability and monitoring function are required in these systems. So, the digitally controlled switching power supply is useful because it has the advantage of realizing both control and monitoring tasks. Furthermore, a key distinguishing feature of digital control circuit is easily able to communicate to the other component in the electronics system. However, there has been no study that tried to discuss the digitally controlled boost type dc-dc converter in detail.

Although the input reactor current of the boost converter is continuous, the output diode current is discontinuous in this converter. Therefore, since the ripple of the output voltage is relatively large, there is the problem that the detected output voltage is changed by the A-D conversion timing. To solve this problem, it is necessary to decrease the cutoff frequency of the anti-aliasing filter. However, it influences the dynamic response. So, it is important to clarify the relationship among the A-D conversion timing, the cutoff frequency and dynamic response.

The purpose of this paper is to present the most suitable cutoff frequency in digital control boost type dc-dc converter and to realize the accuracy output voltage control.

II. CIRCUIT CONFIGURATION AND OPERATION PRINCIPLE

Figure 1 shows the block diagram of the digitally controlled boost type dc-dc converter using DSP. E_i is the input voltage, and e_o is the output voltage. T_r is the main switch, D is the fly wheel diode, L is the energy storage reactor, C is the output smoothing capacitor and R is the load. The output voltage e_o is sent to the A-D converter through the anti-aliasing filter and is converted into digital amount N_n. The relationship between the input and output values of the A-D converter is given by Eq. (1) when it approximately shows the linear expression by considering the width of the quantization to be small.

$$N_n = G_{A-D} e_O \tag{1}$$

where n denotes an n-th switching cycle, and the digital amount N_n is a positive integer number. $G_{A\text{-}D}$ is a gain of the A-D converter and given by Eq. (2).

$$G_{A-D} = \frac{N_{n,\max}}{e_{o,AD\max}} \tag{2}$$

The digital amount N_n is sent to DSP. In the DSP, the numerical value N_{Ton} that corresponds to the on-time interval T_{on} is calculated.

The relationship between the on-time interval T_{on} and the numerical value N_{Ton} is shown as follows;

$$\frac{T_{on,n+1}}{T_s} = \frac{N_{Ton,n+1}}{N_{Ts}} \tag{3}$$

where N_{TS} is a numerical value corresponding to the switching period T_S (=1/f_S). N_{TS} is calculated in the PWM signal generation circuit which is composed of a-digital comparator or a counter. This case the PWM signal generation circuit is composed of a counter. Counter's frequency is f_{ck}, and relation between N_{TS} and f_{ck} is given by Eq. (4).

$$N_{Ts} = f_{CK} T_s \tag{4}$$

The relation between $T_{on,n+1}$ and $N_{Ton,n+1}$ is shown as follow by using Eq. (4);

$$\frac{T_{on,n+1}}{T_s} = \frac{N_{Ton,n+1}}{f_{CK} T_s} \tag{5}$$

According to the relation between the on-time interval T_{on} and the numerical value N_{Ton}, T_{on} is generated. This T_{on} regulates the output voltage e_o.

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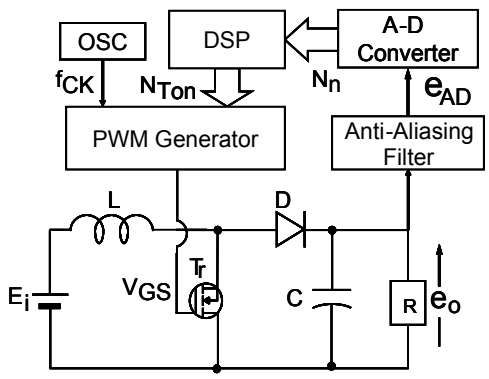


Fig. 1 Block diagram of digitally controlled boost type dc-dc converter using DSP.

The on-time interval N_{Ton} of the P control circuit is represented as follows [5], [6];

$$N_{Ton,n+1} = N_B - K_P\left(N_n - N_R\right) \quad (6)$$

where K_P is the proportional coefficients. N_B is the numerical bias value. N_R is the numerical proportional and values, these values are shown as follows;

$$N_B = N_{TS}\left(1 - \frac{E_i}{E_o^*}\right) \quad (7)$$

$$N_{INT} = G_{AD}e_o^* \quad (8)$$

III. Experimental Result

Figure 2 shows the A-D conversion timing to discuss the effect of the influence of the output voltage ripple and switching noise. The switching frequency is 100 kHz and the sampling frequency is also same. So, T_S is 10μs. When the switch is turn on, the time of the A-D conversion timing is 0. The four sampling points are t_{S1}=2.5μs, t_{S2}=4.5μs, t_{S3}=7.5μs and t_{S4}=9.5μs as shown in this figure. The input voltage E_i is 10V, the desired voltage E_O^* is 20V, the inductance L is 500μH, the output capacitance C is 1470μF and the number of bit of the A-D converter is 8bits.

The switching noise is generated when the switch is turn off or turn on. To guard the switching noise of output voltage ripple, the A-D conversion timing of output voltage is very important for digital controlled dc-dc converter shown in Fig. 1. Figure 3 shows the observed waveforms of input and output voltage of anti-aliasing filter. In this figure, the upper waveform is the input voltage $e_{af\text{-}in}$ of anti-aliasing filter and the under waveform is the output voltage $e_{af\text{-}out}$ of anti-aliasing filter. The anti-aliasing filter's cutoff frequency is 1kHz. As shown in this figure, the switching noise is not rejected completely by the anti-aliasing filter.

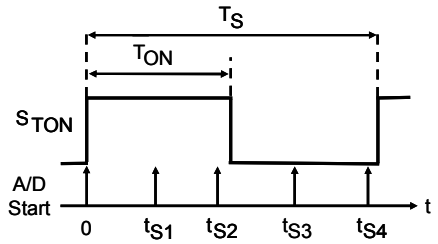


Fig. 2 A-D conversion timing.

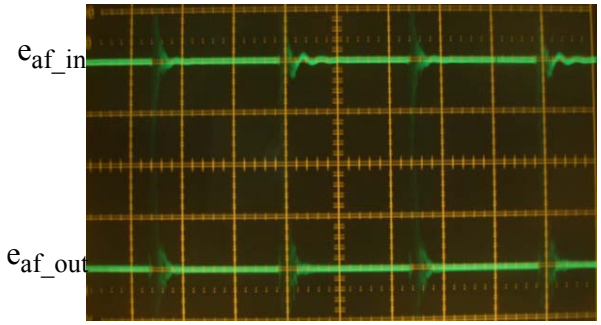


Fig. 3 Observed waveforms of input and output voltage of anti-aliasing filter.

A. Static Characteristics

Figure 4 shows the characteristic of cutoff frequency against ΔE_{omax}. ΔE_{omax} is the range of maximum unevenness of output voltage by the difference of A-D conversion timing. From this figure, it is seen that when proportional coefficient K_P is large, the ΔE_{omax} is large. However, when the cutoff frequency is decrease, ΔE_{omax} is also decrease. When the cutoff frequency is between 10 kHz and 50 kHz, ΔE_{omax} is becoming large. When the cutoff is between 1 kHz and 10 kHz, ΔE_{omax} changes few. Therefore, when the cutoff frequency is less than 10 kHz, the influence of the output voltage ripple and switching noise is reduced.

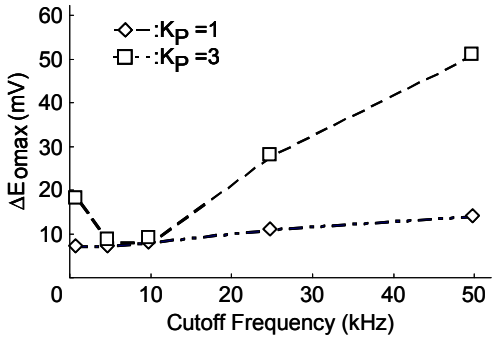


Fig.4 Characteristic of ΔE_{omax} against anti-aliasing cutoff frequency.

B. Dynamic Characteristics

Figures 5 through 7 show the bode diagram, taking the proportional coefficient Kp as a parameter. Figure 5 shows the bode diagram in case of Kp=1, Fig. 6 shows in case of Kp=3 and Fig. 7 shows in case of Kp=5. In these figures, when the proportional coefficient Kp is equal to 1 or 3, the output voltage is always stable. However, when Kp is equal to 5 and the cutoff frequency is 1kHz, the output voltage becomes unstable.

Figure 8 shows the characteristics of gain margin against anti-aliasing cutoff frequency. From this figure, when the proportional coefficient Kp is large, gain margin is low. When the anti-aliasing filter's cutoff frequency is from 50 kHz to 5 kHz, the gain margin is changed a few. Further, It is shown that there is no gain margin when Kp is equal to 5 and the cutoff frequency is 1kHz.

Figure 9 shows the characteristics of phase margin against anti-aliasing cutoff frequency. From this figure, when the proportional coefficient Kp is large, phase margin is also low. When the anti-aliasing filter's cutoff frequency is from 50 kHz to 5 kHz, the phase margin is almost constant.

The cutoff frequency which its gain margin and phase margin is equal to zero is 461Hz in Kp=3, and 1,156 Hz in Kp=5.

Figures 10 through 12 show the observed output voltage waveform of the experimental dynamic characteristics, taking the proportional coefficient Kp as a parameter. In these figures, the step change of the load R is from 200Ω to 20Ω and the A-D conversion timing is t_{S4} (=9.5μs).

Figure 10 shows the transient waveform of output voltage when the proportional coefficient Kp=1, Fig. 11 shows in case of Kp=3 and Fig. 12 shows in case of Kp=5, respectively. Moreover, each figure shows the observed waveforms, taking the cutoff frequency as a parameter.

From these waveforms, when the anti-aliasing filter's cutoff frequency becomes low, transient time becomes long and undershoot becomes also large. Furthermore, in this case, by changing the A-D conversion timing, the transient time and undershoot are no difference. Moreover, when Kp becomes large and the cutoff frequency becomes low, the output voltage becomes unstable as shown in Fig. 12(c). In this case, Kp is equal to five and the cutoff frequency is 1kHz, respectively.

Figure 13 shows the characteristic of undershoot against the anti-aliasing cutoff frequency. In this figure, when the proportional coefficient Kp is large, the undershoot is small. When the anti-aliasing filter's cutoff frequency is from 50 kHz to 5 kHz, the change of undershoot is almost constant.

Figure 14 shows the characteristic of transient time against anti-aliasing cutoff frequency. Similarly, when proportional coefficient Kp is large, the transient time becomes short, and when anti-aliasing filter's cutoff frequency is from 50 kHz to 5 kHz, the undershoot is also constant.

From these figures, it is revealed that the transient time is short and the undershoot is small when Kp is large. Moreover, it is seen that the transient time and undershoot is almost constant and small when the cutoff frequency is between 5 kHz and 50 kHz.

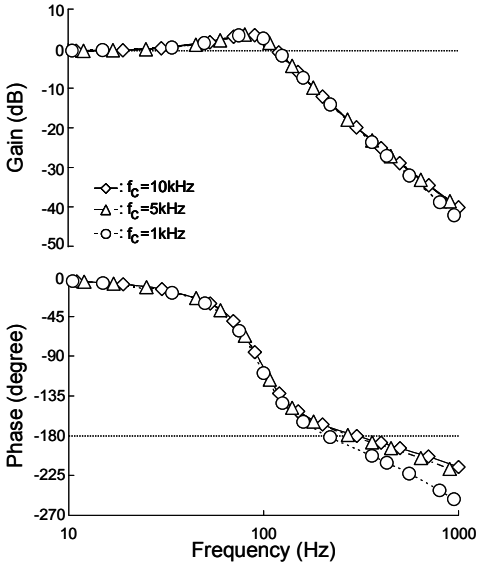


Fig. 5 Bode diagram in case of Kp=1.

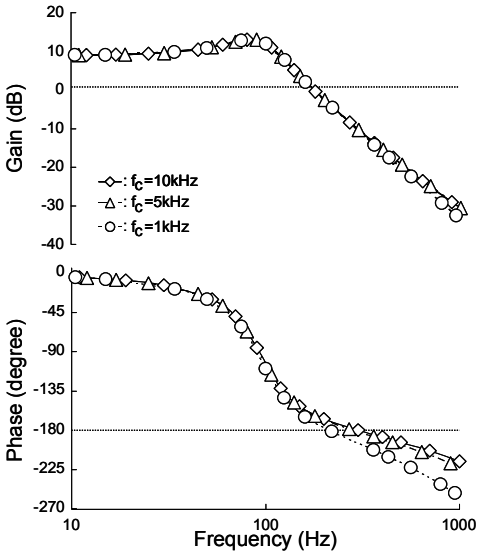


Fig. 6 Bode diagram in case of Kp=3.

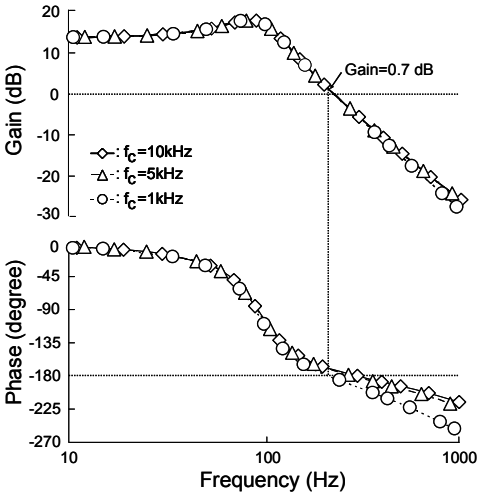


Fig. 7 Bode diagram in case of Kp=5.

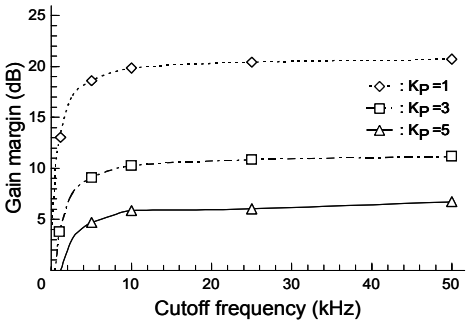


Fig. 8 Characteristics of gain margin against anti-aliasing cutoff frequency.

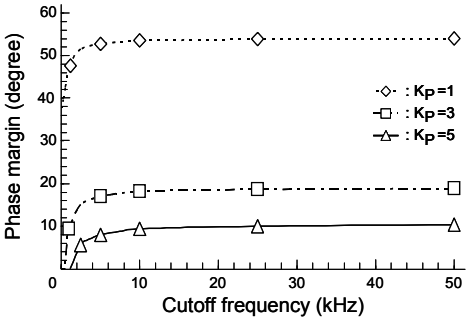
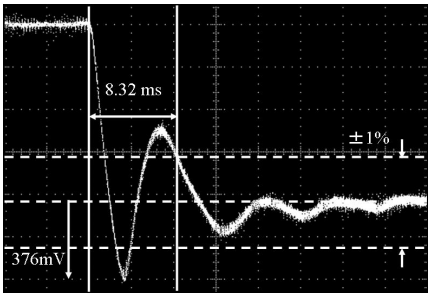
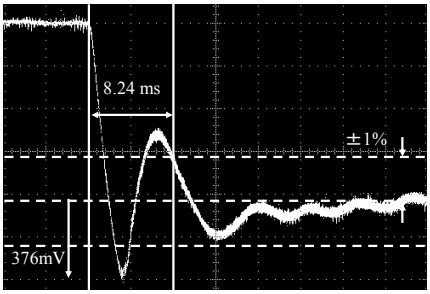


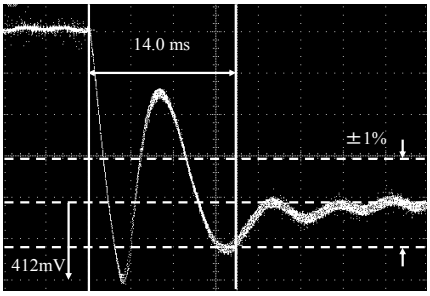
Fig. 9 Characteristics of phase margin against aliasing anti-cutoff frequency.



Vertical 200mV/div.
Horizontal: 4ms/div.
(a) f_c=10 kHz.

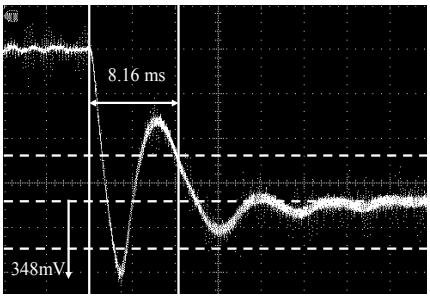


Vertical 200mV/div.
Horizontal: 4ms/div
(b) f_c=5 kHz.

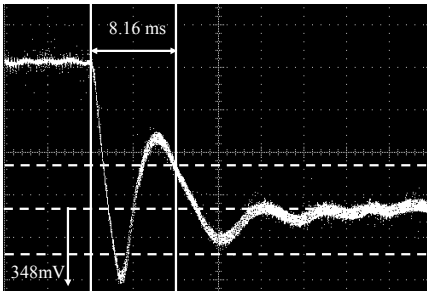


Vertical 200mV/div.
Horizontal: 4ms/div.
(c) f_c=1kHz

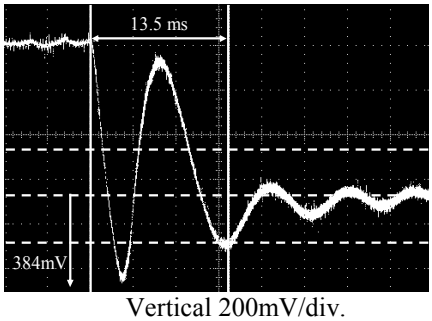
Fig.10 Indicial response of e_o in case of KP=1.



Vertical 200mV/div.
Horizontal: 4ms/div.
(a) fc=10kHz

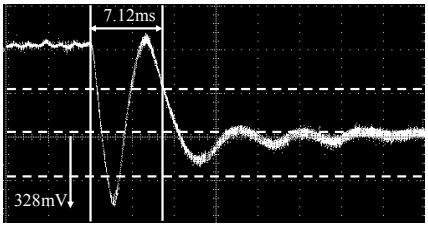


Vertical 200mV/div.
Horizontal: 4ms/div.
(b) f_c=5kHz

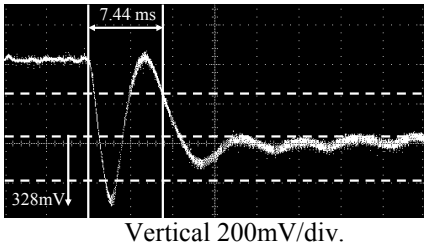


Vertical 200mV/div.
Horizontal: 4ms/div.
(c) f_c=1kHz

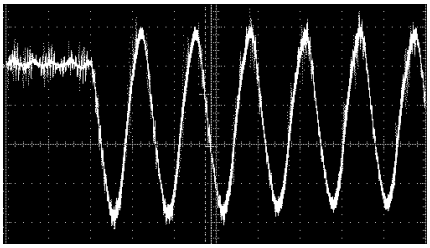
Fig. 11 Indicial response of e_o in case of KP=3



Vertical 200mV/div.
Horizontal: 4ms/div.
(a) f_c=10kHz



Vertical 200mV/div.
Horizontal: 4ms/div.
(b) f_c=5kHz



Vertical 200mV/div.
Horizontal: 4ms/div.
(c) f_c=1Hz

Fig.12 Indicial response of e_o in case of K_P=5.

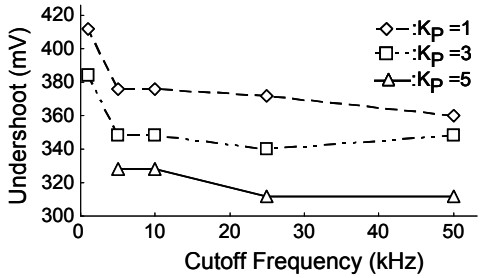


Fig. 13 Characteristic of undershoot against anti-aliasing cutoff frequency.

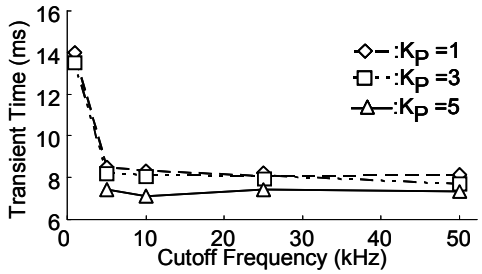


Fig. 14 Characteristic of transient time against anti-aliasing cutoff frequency.

IV. CONCLUSION

In the digital controlled boost type dc-dc converter using the DSP, it is discussed that the A-D conversion timing and anti-aliasing filter's cut-off frequency affect the dynamic characteristics.

From the above discussion, when anti-aliasing filter's cut-off frequency is low, the range of unevenness of output voltage by the difference of the A-D converter's timing is low in the regulation characteristics. In this paper, the influence of the output voltage ripple and switching noise is reduced when the cutoff frequency is less than 10 kHz.

From the bode diagram, it is verified that the output voltage becomes unstable when the cutoff frequency is too low and K_P is large.

In the dynamic characteristics, it is seen that the transient time is long when anti-aliasing filter's cut-off frequency is low. When proportional coefficient K_P is large, transient time becomes short and undershoot becomes also small. In this case, the digital controlled boost type dc-dc converter has no different characteristics by changing the A-D conversion timing. From the dynamic characteristic, it is revealed that the cutoff frequency is selected between 5 kHz and 50 kHz.

Therefore, from both the dynamic and static characteristics, the most suitable cutoff frequency is 5 kHz through 10 kHz. Under this condition, the accuracy digital control for the regulation of output voltage is performed in the boost dc-dc converter.

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