A Critical-Conduction-Mode Bridgeless Interleaved Boost Power Factor Correction

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Abstract — This paper explains about fundamental working principles, governing equations, implementation problems, and experimental results of a new power factor correction (PFC) topology. In this proposed topology, bridgeless technique is applied to a critical-conduction-mode (CRM) interleaved boost PFC in order to gain fundamental understanding towards high efficiency, high performance, low-cost, simple control scheme, and low conducted electromagnetic interference (EMI) circuit. This application is targeted for low to middle power applications that normally employs continuous or interleaved boost converter.

I. Introduction

The bridgeless boost PFC was born in order to maximize converter's efficiency. In that circuit, the number of semiconductor used in the line current path is reduced [1]. It lessens the energy loss that usually occurs inside bridged PFC circuit.

In other side, critical-conduction-mode (CRM) interleaved boost power-factor-correction (PFC) has started to gain widespread acceptance. This topology is characterized by simple control scheme, zero-current-switch (ZCS) during switch turn-on transition, and to some degree it also possible to have zero-voltage-switch (ZVS) turn-on transition. Moreover, the interleaved technique reduces the input current ripple. Therefore, its wave shape is quite similar to the infamous continuous-conduction-mode (CCM) boost converter [2].

Those ZCS, ZVS, and low-ripple input current of [2] not only make the converter efficiency increase but also reduces the conducted EMI. Other than that, those good characters can be achieved by smaller inductor, reasonable size capacitor, and less-ideal switches and diodes.

Therefore, it is reasonable to combine both technique – the bridgeless and the CRM interleaved boost PFC- to a new topology and expecting that those good characters be also inherited.

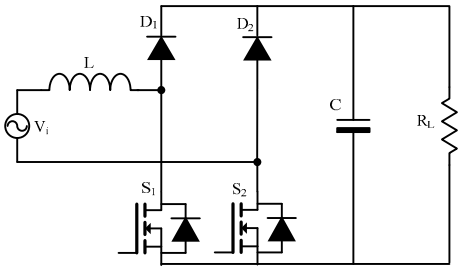

Fig. 1. Basic bridgeless PFC [3].

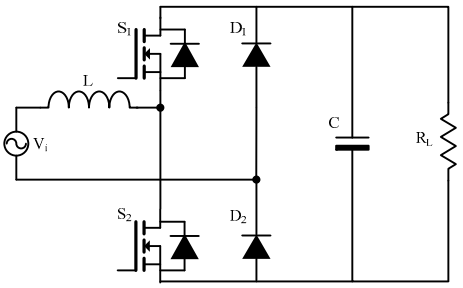

Fig. 2. Totem-pole dual-boost PFC rectifier [4].

II. Building Block

There are numerous topologies available to implement the bridgeless boost PFC. Fig. 1 shows the basic circuit of it [3]. According to [1], the referred circuit has larger common-mode conducted noise than conventional boost PFC. Therefore; the circuit is practically unacceptable to recent stringent regulation. Moreover, four switches and four diodes are required to implement an interleaved PFC based on this topology. Those are quite numerous numbers of switches.

An interesting topology is cited in [1] that is original work of [4]. The circuit is shown in Fig. 2 and is called totem-pole dual-boost PFC rectifier. It is stated in [1] that this topology is only suitable for DCM (discontinuous conduction mode) and CRM operation. This is because the switch body diode slow reverse recovery characteristics prohibited it to operate under CCM condition. Other advantage embed to this topology is that it does not suffer from the high common-mode noise problem [5] as occurs in circuit stated in [3].

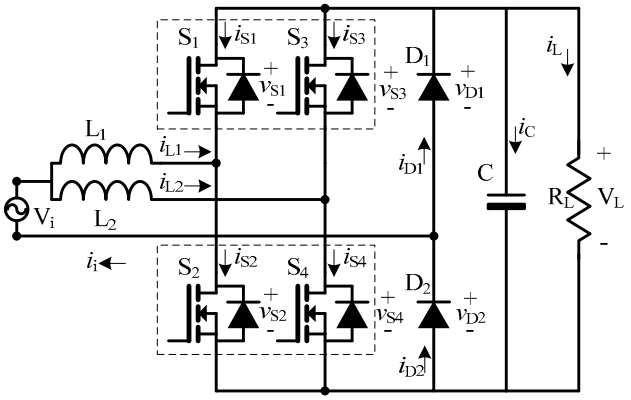

Fig. 3. The proposed CRM bridgeless interleaved boost PFC.

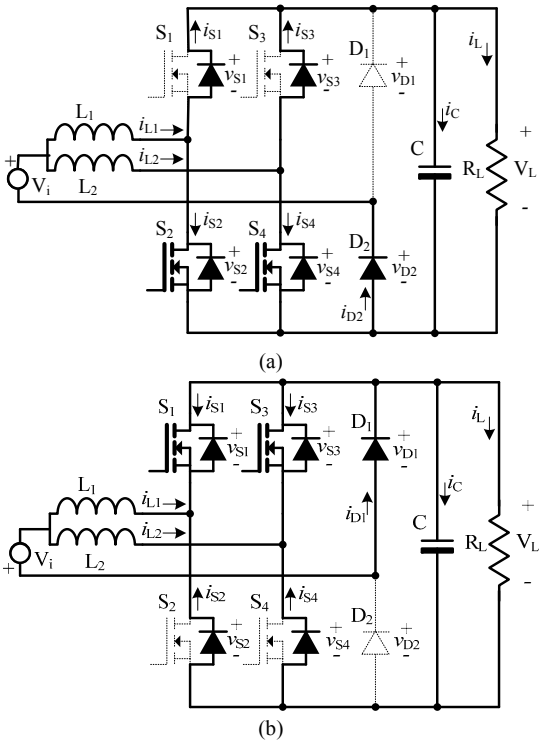

Fig. 4. Switch operation during (a) positive and (b) negative phase of V_i.

III. The Proposed Converter

Fig. 3 shows the proposed converter based on the circuit of Fig. 2. In the new circuit, additional inductor (L_2) and extra switch-leg (S_3 and S_4) are required. D_1 and D_2, like in its conventional version, are normal slow-recovery diodes. However, in this topology, they carry continuous current due to interleaved operation nature of the converter.

A. Basic operating principle

Switches on the Fig. 3 can be grouped into positive-phase group (S_2 and S_4) and negative-phase group (S_1 and S_3). The positive-phase group operates as boost-switches during positive phase of input voltage V_i. During this period, body-diodes of the negative-phase group act as the catch diode. In this phase, return current is delivered by D_2. The converter operation during this stage is illustrated by Fig. 4. (a).

When V_i is in its negative phase, the opposite condition occurs. Through out this time, negative-phase group operates as the boost switches and the positive-phase group body diodes work as the catch diode. Return current is handled by D_1. Fig. 4. (b) depict this condition.

It is known that the switch body diode normally exhibit relatively slow reverse recovery characteristic. This gives penalty to the converter efficiency when converter works under CCM. However, it do not affect too much to the efficiency of the proposed converter as it is intended to work under CRM. Instead, finite amount of diode reverse recovery current gives guaranty that the ZVS transition will always occurs every time the switches turned-on.

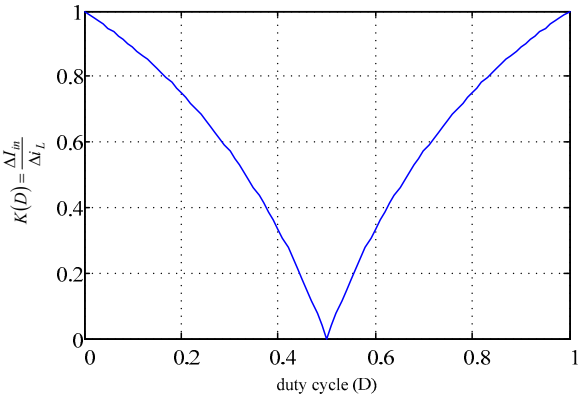

Fig. 5. Input current reduction capability of an interleaved boost PFC [2].

B. The interleave scheme

Those switches are also grouped as leg 1 (S_1 and S_2) and leg 2 (S_3 and S_4). Each leg forms a complete functional block of a boost converter. Control circuit orchestrated the operation of both legs to be 180 degrees out of phase. In other word, those boost converters are under interleaved operation.

As D_1 and D_2 carry the sum current of interleaved leg 1 and leg 2, it contains relatively small amount of ripple. While in conventional CRM boost PFC, the ripple current will be significant.

The ratio of diode ripple current to the inductor ripple current K(D) varies as a function of duty cycle D [2]. Equations to determine the current ratio are defined by [2] as follows:

$$K(D)=\frac{\Delta I_{in}}{\Delta i_L} \tag{1}$$

$$K(D)=\left.\frac{1-2D}{1-D}\right|_{D\le 0} \quad \text{or} \quad K(D)=\left.\frac{1-2D}{1-D}\right|_{D>0} \tag{2}$$

The above equations can be illustrated by Fig. 4. It is apparent that the minimum ripple can be achieved when D is 50%.

In PFC application, D always changes as $v_i(\theta)$ change in sinusoidal manner. It means, the ripple value resulted from the interleaved action will not always in its maximum point. However, from practical point of view, it can be considered low enough compared to the value of inductor applied to the circuit.

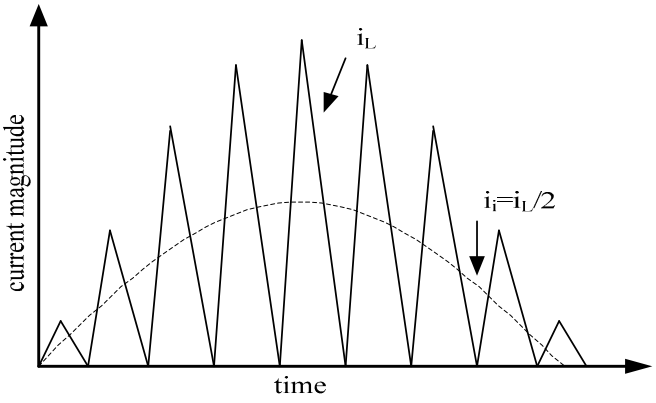

Fig. 6. Illustration of CRM boost PFC input current waveform.

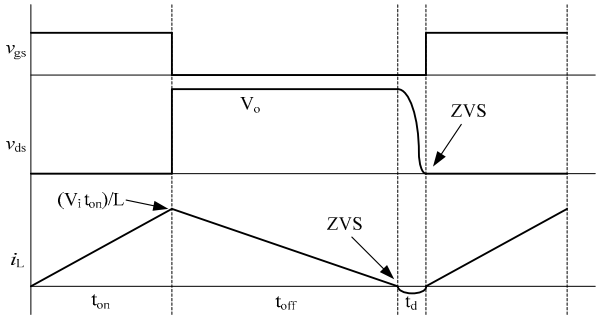

Fig. 7. Key-waveforms of a boost converter working under CRM.

C. *The critical conduction mode operation*

Fig. 6 illustrates the inductor current i_L condition related to the programmed input current i_i in a CRM boost PFC converter. The figure shows that i_L is switched very fast between zero to two times i_i in order to be proportional to V_i hence gives good power factor.

i_i can be calculated by (3). It is apparent from the equation that t_{on} should be kept constant at least for one cycle of V_i in order to make i_i proportional to V_i.

$$i_i = \frac{1}{2} \cdot \frac{V_i}{L} t_{on} \tag{3}$$

$$i_L = \frac{(V_i - V_o)}{L} \cdot t_{off} \tag{4}$$

t_{off} can be determined based on (4) when i_L equal to zero. t_{off} varies as a function of phase θ as its value is determined by V_i that is also a function of θ.

Equation (3) should be multiplied by two in order to determine the i_i for an interleaved boost PFC converter. That is because the referred converter consists of two inductors that carry the same amount of current with 180 degrees out of phase.

Fig. 7 describe an interesting phenomenon occurs in a CRM boost converter. Resonant condition between input inductor and the switch parasitic capacitance occurs during t_d. At certain time and conditions, this may discharge the parasitic capacitance of the switch. When considered properly, it is possible for the switch to turn-on under ZVS condition. This result in higher converter efficiency.

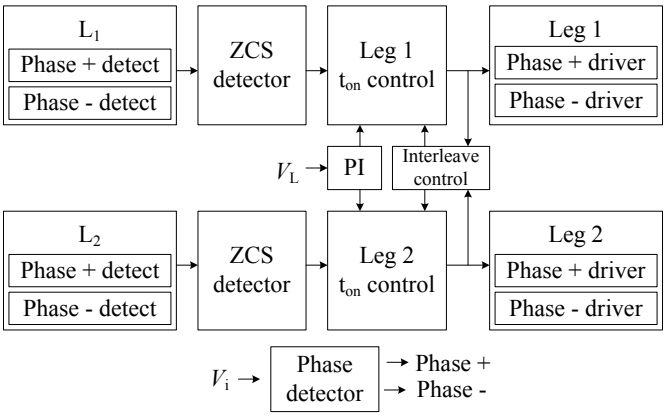

Fig. 8. Control scheme for the proposed converter.

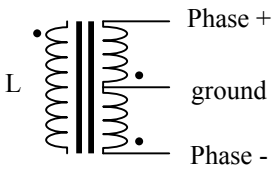

Fig. 9. The proposed zero-current winding detector.

IV. Control Scheme

The proposed converter control scheme can be seen in Fig. 8. Its main part is similar to a conventional interleaved CRM boost PFC. Therefore; commercially available controller for that converter can be used as the core controller.

CRM interleaved-boost PFC controller normally does not need any current sense for its control purpose [6]. It needs only to monitor V_L and the zero-current crossing instant to fulfill its basic function. The zero-current crossing detectors normally employ a secondary winding voltage sense attached to the inductor.

However, some adaptations should be made in order to accommodate the bridgeless nature of the proposed converter. In the modified control scheme, an input voltage detector is required.

The phase detection signal is used to direct PWM signals to the correct phase group switches, whether it is positive-phase group or negative-phase group. Moreover, this signal is also needed to direct the correct zero-current crossing signal source to its detector. The lather change is to accommodate a fact that the converter input inductors are now located in the ac side. It makes the zero-current crossing detection signals also alternate each time phase of V_i changes. To accommodate this, the zero-current detector winding is now modified as shown in Fig. 9.

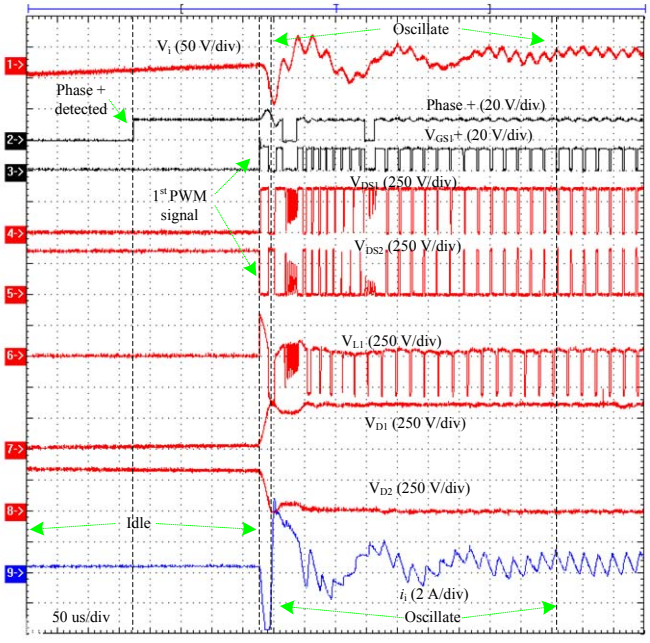

Fig. 10. The proposed topology key-waveforms during phase transition.

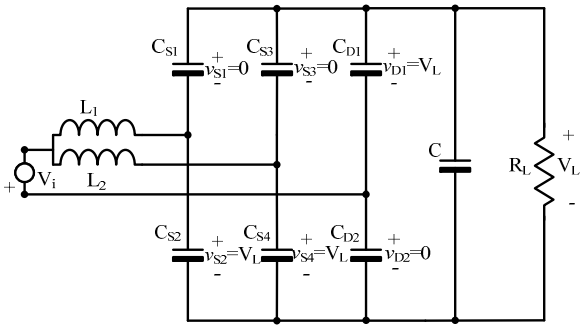

Fig. 11. The circuit configuration during phase transition from (+) to (-).

V. Practical Problem

Every time V_i crossing the zero point toward a new phase, the proposed converter enters an idle condition. Its waveforms during idle and some period after that is shown in Fig. 10. The circuit configuration at that time is shown in Fig. 11.

Fig. 11 illustrates the circuit condition during (+) to (-) phase transition. It is shown here that during idle time, parasitic capacitance of the switches and diodes dominate the converter state. Those capacitances are charged to certain value depend on the former operating condition whether positive or negative phase.

Careful attention should be made on the capacitances of the two diodes. During (+) to (-) phase transition, for example, the parasitic capacitance of diode 1 (C_{D1}) is charged up to V_L while voltages of C_{D2} is nearly zero. When the first PWM signal occurs, C_{D1} will be discharged through the input inductance and V_i . Here, discharging process is under resonant condition among the input inductance and the parallel-connected parasitic capacitance of diodes. It should be noted that at this moment, V_i is still very small and is in phase to the charge stored inside C_{D1}. This creates current pulse and excites quite disturbing voltage and current oscillation as shown in Fig. 10. The oscillating voltage and currents might result in several problems like:

1. momentarily wrong phase detection that result in shoot trough of the V_L to the V_i. It gives significant penalty to the converter efficiency,
2. increasing the cusp distortion around zero-crossing point that result in higher input current THD,
3. significantly, increase the converter's conducted EMI.

Those list figure out that the ringing should be addressed properly in order to achieve good performance of the proposed converter.

TABLE I
The Converters List of Parameters

Target power	300 W
Switches	MOSFET SPP11N60S5
Inductors	340 uH
Capacitors	200 uF
Output Voltages	390 V

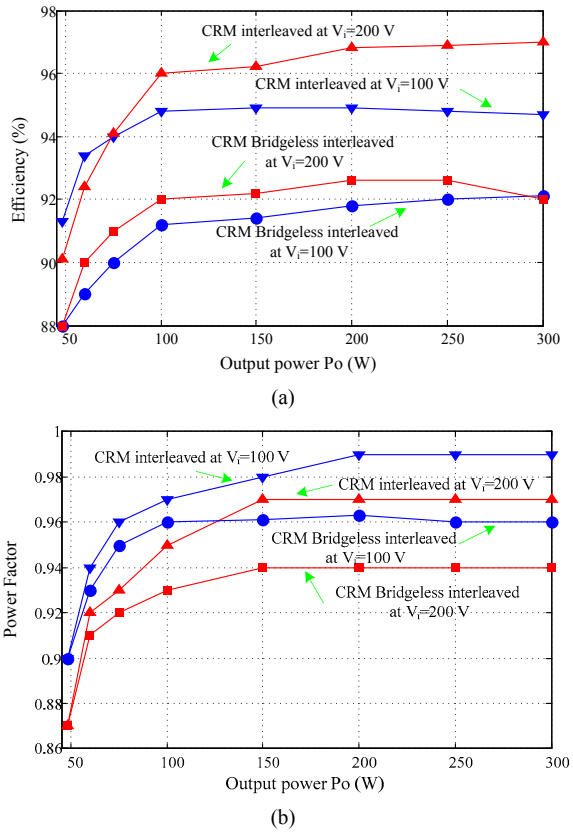

Fig. 12. (a) Efficiency and (b) power factor comparison among conventional and the bridgeless CRM interleaved boost converter.

VI. Experimental Result

A prototype of the proposed converter has been built. Its specification can be seen in Table 1. A conventional CRM interleaved boost PFC with similar specification also has been built for comparison purpose.

Efficiency and power factor comparison among conventional and bridgeless CRM interleaved boost converter can be seen in Fig. 12. (a) and (b) respectively. Depicted in those figure that due to the problem stated in part V, efficiency and PF performance of the proposed converter is still below the conventional CRM interleaved type. However, the overall performance is still good while considered that the result is taken by cheaper and smaller component compared to the conventional CCM boost PFC.

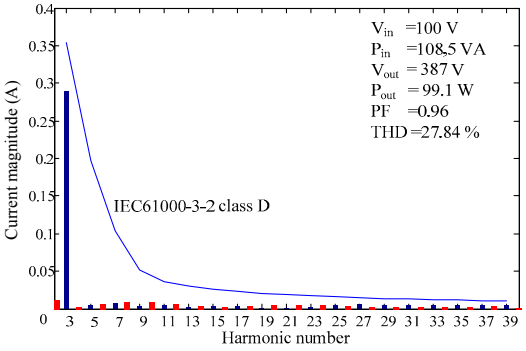

Fig. 13. i_i harmonic measurement during P_o= 99.1 W V_i = 100 V_{rms}.

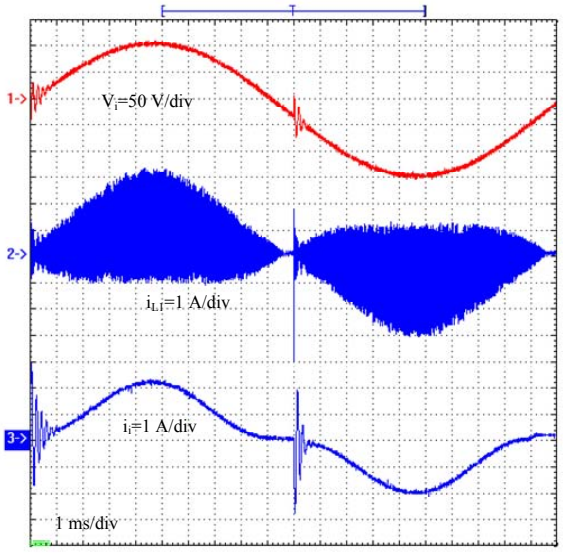

Fig. 14. Comparison of i_{L1} to the i_i that shown superior performance of interleaved technique.

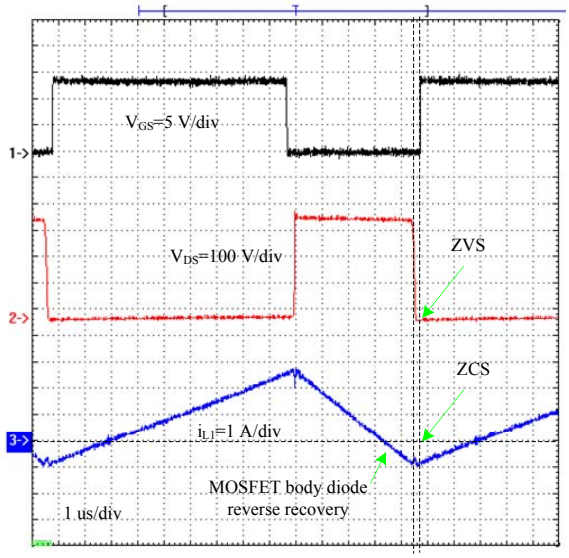

Fig. 15. Illustration of ZCS and ZCS switching condition occurs inside the proposed converter.

The harmonic content of the proposed converter, even though slightly high due to apparent cusp distortion around input voltage zero crossing, is still considered save for IEC31000-3-2 class D equipment. This evident can be seen in Fig. 13. It is also showed there that the proposed converter contain quite significant third harmonic current.

Fig. 14 describe about current condition inside i_{L1} and i_i. It is clear that even though i_{L1} contains fast change current signal, it becomes smoother while combined with the i_{L2} and results for i_i. This is the merit of an interleaved boost technique.

Evident of ZCS and ZVS switching condition can be found in Fig. 15. This occurrence makes the reverse recovery problem that normally gives significant impact to the converter performance become less evident.

VII. Conclusion

A CRM bridgeless interleaved PFC has been presented. Its basic principle, underlying equations, control scheme, problems, and experimental results have been shown thoroughly. It is evident that the new topology, at recent stage, be able to pass the IEC61000-3-2 class D standard while also performing reasonable efficiency even though some practical problems exist. Further developments towards better results are still widely open and promising. This new topology is a good candidate towards low to middle power PFC target.

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