A New Digital Control DC-DC Converter with Peak Current-Injected Control

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***Abstract* - This paper presents a new digital control circuit which is able to detect the peak switch current of the high frequency switching dc-dc converter. In this proposed digital control circuit, the peak current-injected control is realized using the combination of the simple dual pulse width modulation analog-to-digital signal converter and the programmed delay circuit. In 100kHz digitally controlled dc-dc converter, it is seen in simulation that the proposed method has no overshoot of the output voltage and the convergence time that the output voltage is settled to steady-state is only 30μs. The difference between the transient time of the proposed circuit and that of the conventional method is an order of magnitude. Furthermore, the ratio of resolution of the DPWM generator against the output voltage is 0.27% and is satisfied to apply the commercial power supply unit.**

Ⅰ. INTRODUCTION

Most of the telecommunications and data communications systems consist of digital ICs. Recently, in this area, the power supply system requires the high performance characteristics, the high energy management function, the high reliability and the small size more. Therefore, the digital control techniques have been growing to apply to these switching power supplies [1]-[7]. In this case, the current mode dc-dc converter is useful in order to perform the superior dynamic characteristics. However, these studies have focused on sensing the average value of the switch/reactor current because it is very difficult to sample the data of accurate peak point of switch/reactor current at the high switching frequency. Therefore, it has been reported that the peak point is estimated from the slope of reactor current, but there has been no study that tried to detect the peak value of reactor/switch current in the fast switching dc-dc converter [8]- [12].

This paper presents a new digital control circuit which is able to detect not only the average output voltage but also the peak switch current of the high frequency switching dc-dc converter. In this proposed digital control circuit, the peak current-injected control is realized using the combination of the simple dual pulse width modulation analog-to-digital signal converter and the programmed delay circuit.

At first, a comparison of the dynamic characteristics between the proposed digitally controlled dc-dc converter with the peak current-injected control and the conventional one is discussed. Next, the relationship between the steady-state error and control circuit parameter is examined.

Ⅱ. CIRCUIT CONFIGURATION AND OPERATION PRINCIPLE

Figure 1 shows the configuration of proposed digital power supply and monitoring system to increase the reliability of the telecommunications and data communications equipment in the communications building. In this system, all switching power supplies is controlled by the monitor station and the energy can be saved easily. Figures 2 and 3 show the circuit configurations of digitally controlled dc-dc converter and a new high performance digital control circuit, respectively. In Fig. 2, the output voltage and the switch current are detected and are sent to the digital control circuit. In Fig. 3, since the dual pulse code analog-to-digital (PC A-D) converter is used, the influence of

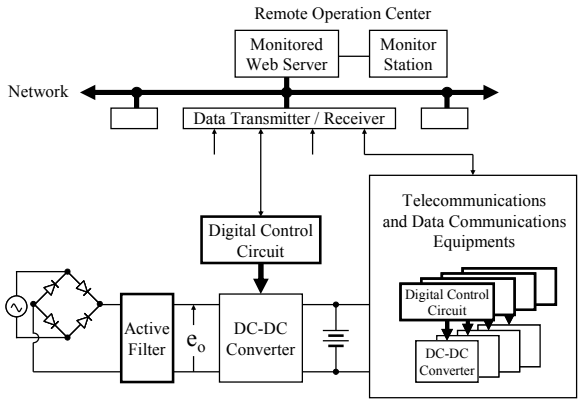

Fig. 1 Configuration of proposed digital control power supply and monitoring system.

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temperature, noise and so forth are rejected. In the dual PC A-D converter of the average voltage detector, the output voltage of dc-dc converter and the constant reference voltage E_o^* is converted into the signals S_1 and S_2, respectively, as shown in Fig. 4.

The CK is the clock pulse and S_{TS} is the start signal corresponding to the switching period. Furthermore, these pulses S_1 and S_2 are counted by the counters #1 and #2, respectively. The difference of these values is calculated by the subtracter. The output value S_{SUB} is sent to the digital filter circuit and this calculated result S_{SEL} decides the delay time T_D of programmable delay circuit as shown in Fig. 5. The moving average method [13] is performed in the digital filter. The delayed output signal S_D of the programmable delay circuit generates the start signal of the ramp voltage of PC A-D converter #4 during each divided short period T_{sD} of the switching period T_s as shown in Fig. 6. The ramp voltage is increased from this point of time and the pulse signal S_4 is generated when it reaches the threshold voltage as shown in Fig. 7. The ramp waveform is generated by the simple CR integrator and ramp voltage is corresponded to the constant voltage E_c in the PC A-D converter #4. In the PC A-D converter #3, the ramp voltage corresponding to the switch current iTr is increased during each divided period T_{sD} and S_3 is generated. In this case, the start time has no delay against the start signal S_{BTS}. When the switch current is larger than the threshold value corresponding to the output voltage, S_3 is generated at the early time against S_4 during some divided period T_{sD}. At the same instant, the signal S_{GS} of the digital PWM (DPWM) generator directs the main switch T_r to turn off and the on time interval T_{on} is decided.

As a consequence, the peak current-injected control is realized by the simple A-D converter and programmable delay circuit.

Next, the resolution against the output voltage of the DPWM generator will be discussed.

In Figs.3 and 7, the relationship between T_D and T_{DSEL} is represented as follows;

$$T_D = T_{DSEL} N_{RM} = T_{DSEL} \left\{ N_R + K_P \left(\frac{1}{M} \sum_{k=p}^{p+M-1} N_{eo} - N_{Eo*} \right) \right\} \quad (1)$$

where T_{DSEL} is the delay time of the delay buffer shown in Fig. 5 and M is the number of sample point of the moving average.

When the ramp voltage #4 reaches the threshold voltage V_{TH4}, the following relation is obtained.

$$t_{E_C} = t(E_c) = \tau_c \ln\left(\frac{Ec}{Ec - V_{TH3}} \right) \quad (2)$$

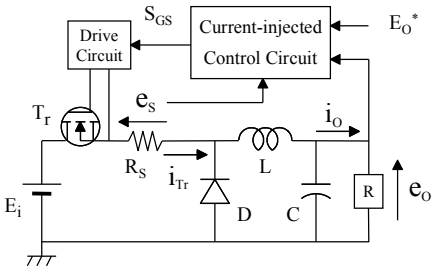

Fig. 2 Digitally controlled dc-dc converter.

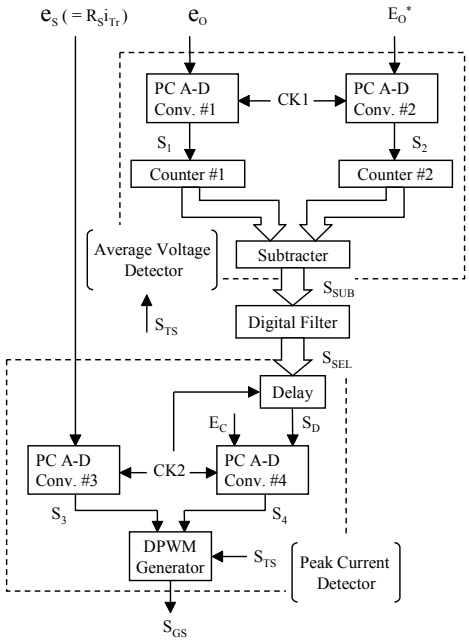

Fig. 3 A new control circuit.

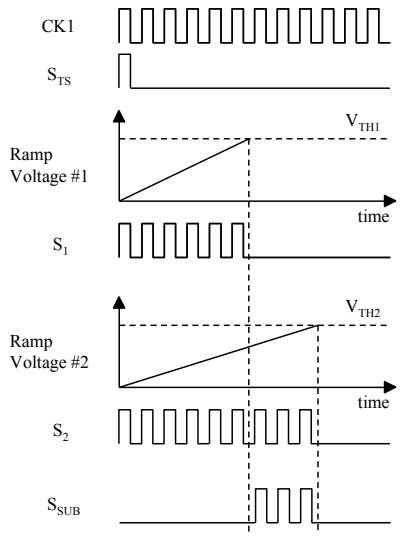

Fig. 4 Operation principle of dual PWM A-D converter in average voltage detector.

where V_{TH3} is equal to V_{TH4}. τ_C is the time constant of CR integrator.

Assuming that the small variation Δe_{pv} of the peak value e_p of ramp voltage #3 is caused at the voltage E_C, the following equation is obtained:

$$\Delta e_{pv} = -\left(\frac{E_c}{V_{TH3}} - 1\right)\frac{E_c T_{DSEL}}{\tau_c}\Delta N_R = -K_{DA}\Delta N_R \quad (3)$$

where

$$K_{DA} = \left(\frac{E_c}{V_{TH3}} - 1\right)\frac{E_c T_{DSEL}}{\tau_c} \quad (4)$$

In Fig. 6, the following relation is obtained because the peak value e_p of ramp voltage #3 is corresponding to e_S.

$$\frac{T_{on}}{T_s} = \frac{2f_s L}{A_{cc}R_s(E_i - E_o)}\left(e_p - A_{cc}R_s I_{Tr}\right) \quad (5)$$

where A_{cc} is the gain of amplifier of current detector and f_S is the switching frequency.

In the DC-DC converter in Fig. 2, assuming that the small variation ΔE_O in E_o and ΔT_{on} in T_{on} are caused by the small variation ΔI_O in I_o, the following equation is obtained:

$$\Delta E_o = \frac{\Delta T_{on}}{T_s}E_i - r\Delta I_o \quad (6)$$

where r is the internal loss of the dc-dc converter.

Considering equations (3), (5) and (6), the following equation is represented, the resolution of the DPWM generator against the output voltage is obtained as follows;

$$\left|\frac{\Delta E_o}{\Delta N_{RM}}\right| = \frac{2f_S L E_i}{\left(1+\frac{r}{R}\right)A_{cc}R_S(E_i - E_o^*) + 2f_S L E_i A_{cc}\frac{R_S}{R}}K_{DA} \quad (7)$$

Ⅲ. SIMULATED RESULTS

Figures 8(a) and (b) show the simulated output voltage and reactor current waveforms of transient response of the dc-dc converter using the proposed digital control circuit in step change of the load R from 10Ω to 5 Ω, taking M as parameter. In this figure, the simulator is PSIM, the digital filter control is performed by the moving average and the parameter M is the number of the sampling point of the moving average. The switching frequency is 100kHz, L is 188μH, C is 100μF and E_i is 20V. It is seen in these figures that there are no undershoot of the output voltage. Especially, no overshoot of reactor current is realized and the transient time until the complete steady-state is only 30μs as shown in Fig. 8(a). In this case, M is equal to 3.

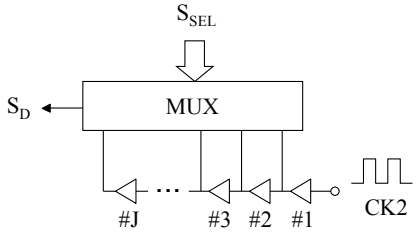

Fig. 5 Programmable delay circuit.

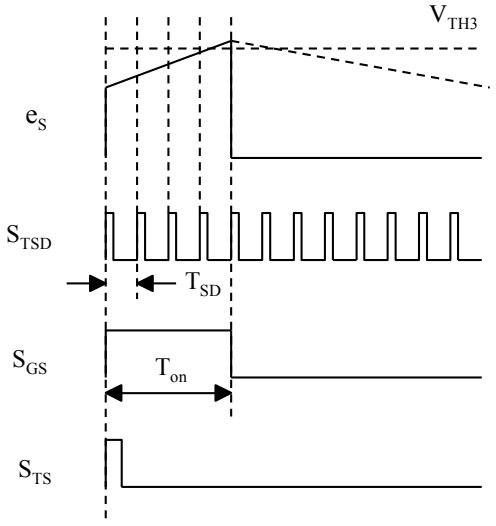

Fig. 6 Operation principle of peak current detector.

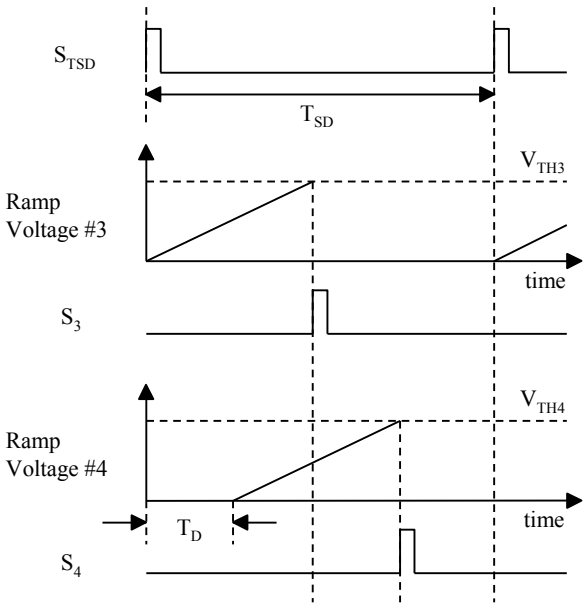

Fig. 7 Operation principle of dual PWM A-D converter in peak current detector.

In Fig. 8(b), the oscillation phenomenon is occurred because the M is large. When M is increased, the delay time also increases and the system performance becomes unstable.

Figure 9 shows the simulated output voltage and reactor current waveforms of transient response of the dc-dc converter using the conventional fundamental digital control circuit without the peak current detector in Fig.3. The circuit parameters are same as those of Fig. 8 except the circuit parameter of the peak current detector. M is equal to 3. This figure shows that the steady-state error is small, but the undershoot of the output voltage is approximately 7%, the overshoot of reactor current is 41% and the convergence time that the output voltage is settled within 1% is 1ms.

Therefore, it is seen that the difference between the transient time of the proposed circuit and that of the conventional method is an order of magnitude.

Figure 10 shows the relationship between the resolution of the DPWM generator and time-delay T_{DSEL} of delay buffer, taking the switching frequency f_S as parameter. The symbol of closed circle denotes the simulation results and the lines show the calculated results by Eq. (7). It is seen in this figure that the resolution of the DPWM generator is proportional to time-delay T_{DSEL} of delay buffer each switching frequency. Further, it is revealed that these simulated values agree well with the calculated ones.

In Fig. 8(a), the time delay of delay buffer in the proposed circuit is set at 0.10ns. The dc gain is 0.2 [1/V] and the steady-state error is approximately 0.1V. Therefore the resolution against the output voltage of the DPWM generator is 0.054 from Eq. (7) as shown in this figure. In this case, E_i=20V, E_o*=5V, r=0.17Ω, R=5 Ω, R_S=0.05 Ω, L=188μH and C=100μF. So, the ratio of resolution of the DPWM generator is 0.27% against the output voltage.

IV. CONCLUSION

A new digital control circuit for the dc-dc converter is presented in this paper. This proposed circuit has superior transient response. In 100kHz digitally controlled dc-dc converter, the proposed method has no undershoot of the output voltage and no overshoot of reactor current. Further, the convergence time that the output voltage is settled to steady-state is only 30μs. Furthermore, the ratio of resolution of the DPWM generator against the output voltage is 0.27% and is satisfied to apply the commercial power supply unit.

We confirm that these results are useful to realize the next generation model of the switching power supply.

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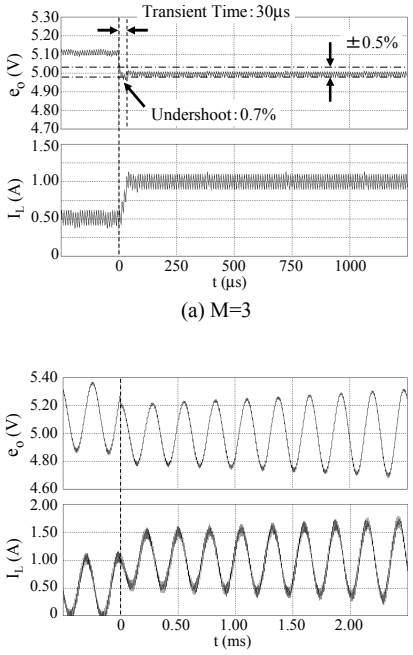

Fig. 8 Transient responses in step change of the load resistor R, taking M as a parameter.

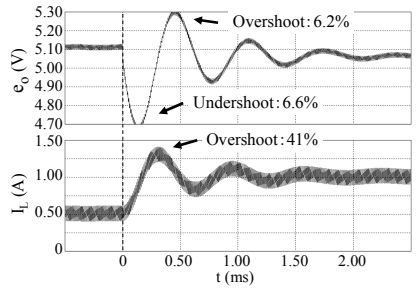

Fig. 9 Transient responses in step change of the load resistor R, in the conventional circuit.

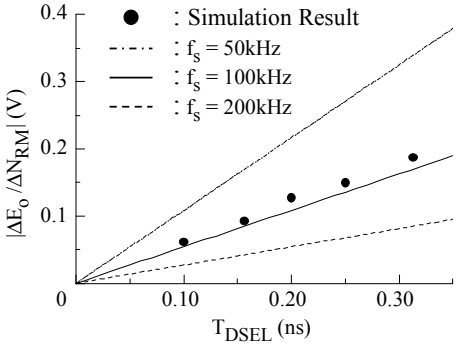

Fig. 10 Relationship between resolution of the DPWM generator and time delay T_{DSEL} of delay buffer.

REFERENCE

[1] W. E. Bury, D. Czarkowski, J. Dzieza, S. Lewis and S. Ramamurthy: "DSP H∞ controller for a variable output dc-dc converter: design and implementation", Proceedings of IEEE International Telecommunications and Energy Conference, pp. 415-420, Oct. 2002.

[2] F. Kurokawa and T. Nakashima: "A New Fast Response Digital Filter Control DC-DC Converter," Proceedings of the IEEE International Telecommunications Energy Conference 2007, Vol. 29, No. 1, pp.527-532, September 2007.

[3] H. Hu, V. Yousefzadeh and D. Maksimovic: "Nonlinear control for improved dynamic response of digitally controlled dc-dc converters," IEEE PESC '06 Record, pp.2584-2590, June 2006.

[4] V. Yousefzadeh, A. Babazadeh, B. Ramachandram and E. Alarcon: "Proximate time-optimal digital control for dc-dc converters," IEEE PESC '07 Record, pp.124-130, June 2007.

[5] Z. Lukic, C. Blake, S. C. Huerta and A. Prodic: "Universal and fault-tolerant multiphase digital PWM controller IC for high-frequency dc-dc converters", Proc. of IEEE APEC '07, pp. 42-47, Feb 2007.

[6] F. Kurokawa and W. Okamoto: "Improvement of Dynamic Characteristics of Digitally Controlled Switching Power Converter," Invited Paper, Proceedings of the IEEE & IEEJ Power Conversion Conference, Vol. 4, No. 1, pp. 1147-1153, April 2007.

[7] F. Kurokawa, T. Nakashima, K. Tanaka and W. Okamoto: "A New Fast Digitally Controlled DC-DC Converter," IEEE Power Electronics Specialists Conference Record, Vol. 38, No. 1, pp. 798-802, June 2007.

[8] H. Peng and D. Maksimovic´, "Digital current-mode controller for dc-dc converters," *IEEE APEC*, pp.899-905, Mar., 2005.

[9] S. chattopadhyay and S. Das, "A digital current-mode control technique for dc-dc converters," *IEEE Trans. On Power Electronics*, Vol. 21, No. 6, pp. 420–427, Nov., 2006

[10] J. A. A. Qahouq, L. Huang, D. Huard and A. Hallberg: "Novel Current sharing schemes for multiphase converters with digital controller implementation", Proc. of IEEE APEC '07, pp. 148-156, Feb 2007.

[11] I. Voss, S. Schroder and R. W. De Doncker: "Predictive digital current control using advanced average current sampling algorithm for multi-phase 2-quadrant dc/dc converters", Proc. of IEEE APEC '07, pp. 8-13, Feb 2007.

[12] O. Trescases, A. Parayandeh, A. Prodic and W. Tung Ng : "Sensorless digital peak current controller for low-power dc-dc SMPS based on a bi-directional delay line," IEEE PESC '07 Record, pp.1670-1676, June 2007.

[13] B. R. Bannister and D. G. Whitehead: "Fundamentals of modern digital systems," Second Edition, Macmillan Education