

# On Factors Affecting EMI-Performance of Conducted-Noise-Mitigating Digital Controllers in DC-DC Converters—An Experimental Investigation

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**Abstract**— This paper investigates several factors affecting EMI-performance of digital controllers targeted at conducted-noise reduction in dc-dc converters. Four factors have been studied: frequency modulation profile, randomization ratio percentage, clock frequency, and spread-spectrum scheme. The field-programmable gate arrays (FPGAs) have made substantial improvements in price and performance throughout the past few years. All investigations have been accomplished by using FPGA-based implementations. A breadboard circuit has been built-up for the experimental investigations. Furthermore, a comparative study has been carried-out to comprehensively understand the effect of such factors on conducted noise mitigation. A substantial part of the manufacturing cost of power converters involves designing filters to comply with the EMI limits. Considering these investigations when designing the dc-dc power converters significantly reduces the filter size.

**Index Terms**— DC-DC power conversion, Electromagnetic compatibility, Electromagnetic interference, Field programmable gate arrays, Frequency modulation, Random number generation.

## I. INTRODUCTION

Switching power converters generate considerable electromagnetic interference (EMI) noise [1]. EMI noise reduction is generally accomplished by three means: suppression of noise source, isolation of noise coupling path, and filter/shielding [2]. Common tools such as passive filters and shields will put increased pricing pressures on dc-dc converters [1].

The noise peaks of EMI spectrum are mainly concentrated on multiples of switching frequency. However, in the case of spread-spectrum techniques, the energy of harmonics is spread across a well defined frequency band; the peak of harmonics drastically decreases [2]-[32] (see Fig. 1). This paper investigates several factors affecting EMI-performance of the spread-spectrum techniques for conducted-noise reduction in dc-dc converters.

The field-programmable gate array (FPGA) is a flexible and attractive hardware design option, becoming lower cost, and applicable for power supply applications [29]-[31]. The implementation of the investigated factors has been accomplished by FPGA technology.

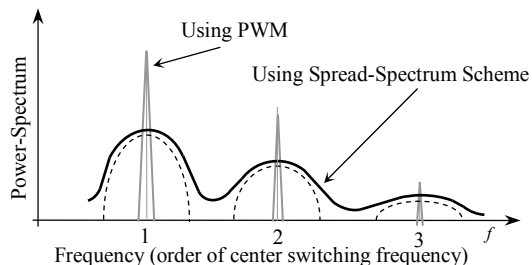


Fig. 1. Frequency spectrum comparison of two switching signals.

This paper is organized as follows. Section II describes the investigated factors. Section III presents details of the experimental test setup. Experimental results and discussions are presented in section IV. Finally, conclusions are addressed section V.

## II. INVESTIGATED FACTORS

### A. Frequency Modulation Profiles

The investigated profiles can be classified into two groups as follows:

Group I:

1. Sinusoidal modulation.
2. Triangular modulation.
3. Sawtooth modulation.
4. Exponential modulation.
5. Square modulation.
6. Zigzag modulation.

Group II:

7. Chaotic modulation.
8. Markov chain based random modulation.
9. Uniformly distributed random modulation.
10. Normally distributed random modulation.
11. M-sequence based random modulation.
12. Pseudorandom stream modulation.

All the investigated profiles fulfill the following considerations:

- Center switching frequency,  $f_{CSW} = 300$  kHz.
- Frequency deviation,  $\Delta f = \pm 25\%$ , and so:  
Lower switching frequency limit,  $f_L = 0.75 * 300 = 225$  kHz.
- Upper switching frequency limit,  $f_H = 1.25 * 300 = 375$  kHz.
- Number of the switching frequency points in the modulated sequence array,  $N_p = 256$  point.

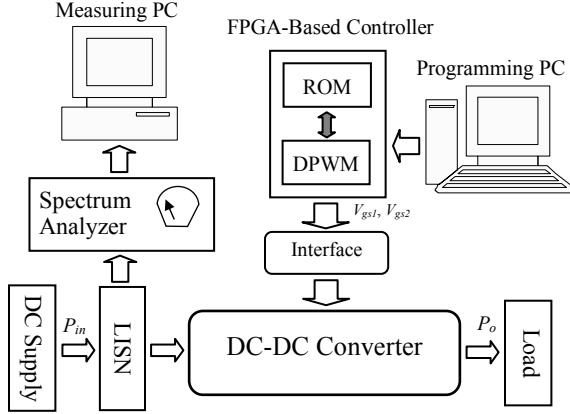


Fig. 2. Block diagram of the controlled dc-dc converter with the conducted-noise measurement system.

All the twelve switching frequency modulation profiles, stated above, have been investigated at the same considerations. Some of the modulation data have been prepared using MATLAB software, and others have been generated online. The implementation of the studied profiles has been accomplished by using an FPGA-based controller and experimentally investigated as shown in Fig. 2. As a sample, three profiles are described in this manuscript as follows:

#### A.I Sawtooth modulation

Figure 3.a shows the modulated switching frequency sequence with a sawtooth profile. In addition, Fig. 3.b presents the probability characteristics of this modulation sequence. The center frequency is swept from the lower frequency to the upper frequency. The presented probability mass level at the center frequency of the bandwidth is the sum of the discrete probability values at the frequencies that fall within the bandwidth.

In order to obtain a meaningful discussion that concisely implies the relation between the measured noise spectra and the investigated profiles, the resolution bandwidth (RBW) is taken as the same RBW of the spectrum analyzer (RBW = 9 kHz).

#### A.II Markov chain based random modulation

In this case, the modulated frequency is chosen according to the state of a Markov chain. The introduced example in [6] is applied here for comparing the EMI performances. Fig. 4 schematically shows a four state Markov chain, corresponding to the following policy.

The controller observes the last switching frequency and if it is  $F_1$ , then either of  $F_1$  with probability 0.25 or  $F_2$  with probability 0.75 is selected for the next cycle. If it is  $F_2$ , then either of  $F_3$  or  $F_4$  is selected for the next cycle with probability 0.5. If it is  $F_3$ , then either of  $F_2$  or  $F_1$  is selected for the next cycle with probability 0.5. If it is  $F_4$ , then either of  $F_4$  with probability 0.25 or  $F_3$  with probability 0.75 is selected for the next cycle.

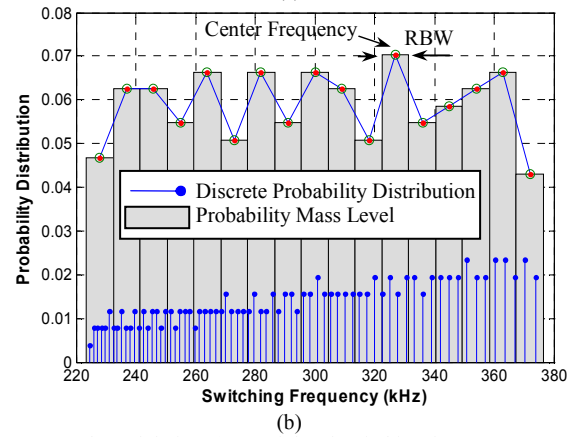
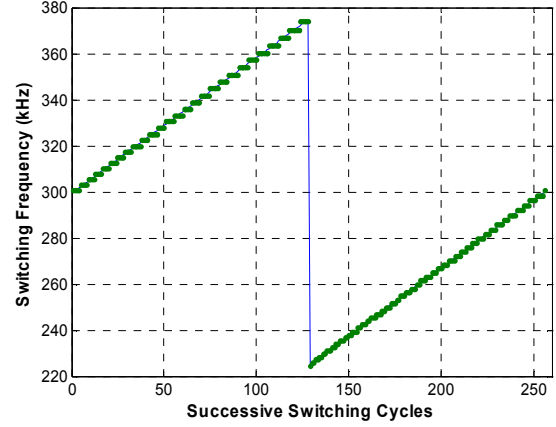


Fig. 3. Sawtooth modulation: (a) Modulated switching frequency sequence, (b) Discrete probability distribution and probability mass level.

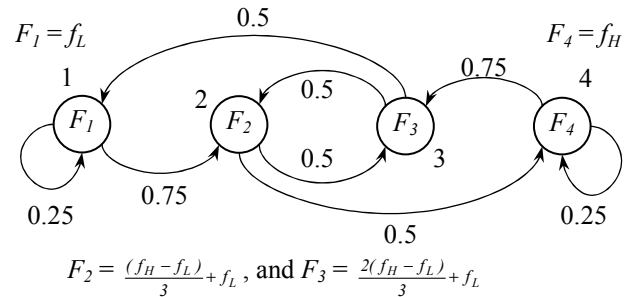


Fig. 4. Switching frequency modulation governed by Markov chain.

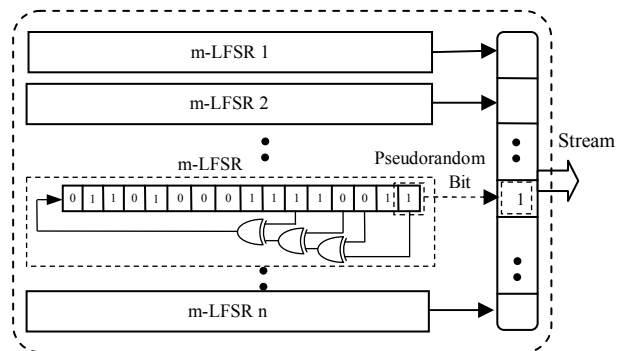


Fig. 5. Pseudorandom stream generator.

### A.III Pseudorandom stream modulation

A pseudorandom stream generator has been constructed using several maximum length linear feedback shift registers (m-LFSRs) in parallel, as shown in Fig. 5. For different m-LFSRs output bits, different initial contents of m-LFSRs (seeds) have been used. The taps are XOR'd sequentially with the output and then fed back into the leftmost bit.

The component m-LFSRs are clocked regularly. Only at the beginning of every switching cycle, the random output bits are converted into an integer number (PRN) and used in calculating the switching frequency for the started switching cycle.

### B. Randomization ratio percentage

The switching frequency is randomized using the pseudorandom stream, generated by the described above generator (see Fig. 6) at different randomization ratio percentages, (RRP), as follows:

$$f_{sw} = f_L + K \times PRN \quad (1)$$

then,

$$RRP = \frac{K * PRN}{2 * f_{csw}} * 100 \quad (2)$$

where;

- $f_{sw}$  : Switching frequency
- $f_L$  : Lower frequency limit
- $K$  : Constant for achieving the required randomized frequency range
- $f_{csw}$  : Center switching frequency
- $RRP$  : Randomization ratio percentage
- $PRN$  : Pseudorandom output stream converted into an integer number

### C. Clock Frequency

Any output signal of the FPGA is composed of number of clocks. Then, the frequency of this output signal can be calculated by the following equation:

$$F_{output\ signal} = \frac{1}{clocks\ No. * T_{clk}} = \frac{f_{clk}}{clocks\ No.} \quad (3)$$

where;

- $F_{output\ signal}$  : Frequency of the output signal
- $T_{clk}$  : Time period of each clock =  $1/f_{clk}$

From the above equation, for an output signal with a certain frequency randomization range, higher FPGA clock speed means higher resolution as illustrated in Fig. 5. On the other hand, the higher FPGA clock speed, the higher FPGA cost.

The conducted-noise characteristics of the dc-dc converter have been investigated at different FPGA clock speeds, (20 MHz, 40 MHz, and 66 MHz).

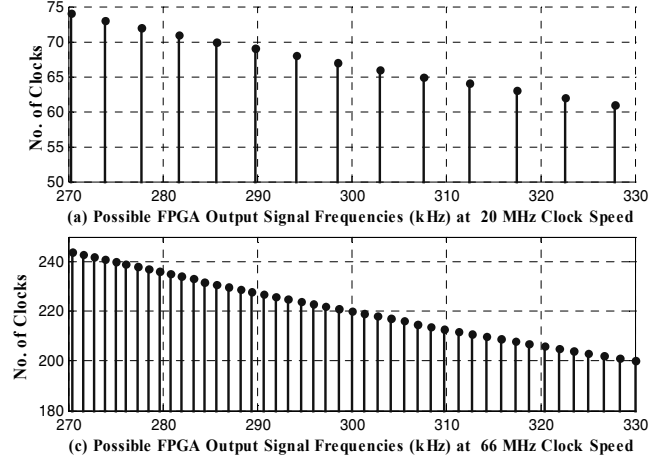


Fig. 6. The effect of increasing the FPGA clock speed on the resolution, (for output signal with frequency range 270~330 kHz).

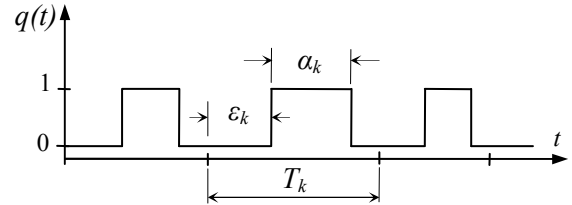


Fig. 7. Parameters in the switching signal.

TABLE I: THE RANDOMIZATION PARAMETERS FOR THE SCHEMES.

Case	Scheme	Randomization Parameters			$\alpha_k$	Remarks
		$F_k$	$d_k$	$\epsilon_k$		
(a)	PWM	Const.	Const.	Const.	Const.	Basic
(b)	RPPM	Const.	Const.	Rand.	Const.	Ad.*
(c)	RPWM	Const.	Rand.	Const.	Rand.	Ad.*
(d)	RDRPPMFCF	Const.	Rand.	Rand.	Rand.	New
(e)	RCFMFD	Rand.	Const.	Const.	Rand.; Synchron.	Ad.*
(f)	RCFRPPMFD	Rand.	Const.	Rand.	Rand.; Synchron.	New
(g)	RCFMVD	Rand.	Rand.	Const.	Rand.	Ad.*
(h)	RRRM	Rand.	Rand.	Rand.	Rand.	New

Ad.\*: Addressed previously in power electronics publications, [2]-[32].

### D. Spread-Spectrum Schemes

According to Fig. 7,  $T_k$  is the duration of the  $k$ th cycle,  $\alpha_k$  is the duration of the on-state within this cycle, and  $\epsilon_k$  is the delay from the starting of the switching cycle to the turn-on within the cycle. Note that the duty ratio is  $d_k = \alpha_k / T_k$  and the switching frequency  $F_k = 1/T_k$ .

The switching function  $q(t)$  consists of a series of such switching cycles. To spread the frequency spectrum of the switching noise,  $\{F_k, d_k, \text{ or } \epsilon_k\}$  can be randomized. Table I summarizes all the possible schemes that can be carried-out for this purpose.

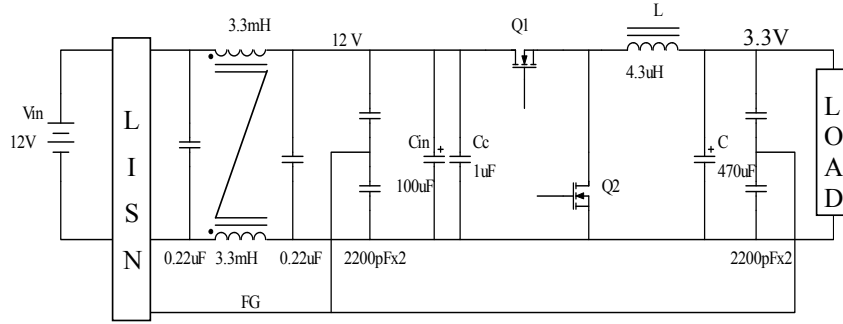


Fig. 8. Experimental converter circuit configuration.

Furthermore, another three different randomization schemes that have not been previously addressed due to hardware limitations and the complexity of the control circuit are presented in Table I.

Now, with the flexibility and programmability of FPGA technology, the above new schemes are designed, implemented, and addressed in this paper. Moreover, the other schemes, used previously in power electronics, are designed and implemented. Furthermore, all schemes are experimentally investigated, and the conducted-noise spectra are compared in the following sections.

### III. EXPERIMENTAL WORK AND DISCUSSION

The size of the output inductor and capacitor of the selected buck converter were chosen such that the converter operates in the continuous conduction mode. The investigated techniques were designed in VHDL (VHSIC hardware description language; VHSIC: very-high-speed integrated circuit). They were analyzed and synthesized using Quartus II web edition software. Then, they were implemented inside an Altera Cyclone EP1C6T144C8 FPGA.

Figure 2 shows a typical setup for conducted-noise measurement, which exactly follows the defined regulations for conducted EMI measurements in [1]. A line impedance stabilization network (LISN: ESH2-Z5 type) was used to standardize the input impedance seen from the input of the device under test (DUT), while ensuring a high degree of isolation over the spectral measurement range. The LISN sensed the conducted-noise. The EMI receiver (ESCI type) provided a  $50 \Omega$  termination for the LISN measurement port. This setup guaranteed a fixed or calibrated relationship between the conducted EMI current and the resulting voltage at the input of the measurement apparatus. Figure 8 presents the experimental converter circuit configuration.

Noise measurements were taken at  $V_{in} = 12 \text{ V}$ ,  $V_o = 3.3 \text{ V}$ , and  $I_o = 5 \text{ A}$  with a center switching frequency  $f_{csw} = 200 \text{ kHz}$  and a resolution band width of the spectrum analyzer  $\text{RBW} = 9 \text{ kHz}$ .

## IV. RESULTS AND DISCUSSION

### A. Frequency Modulation Profiles Effect

A sample of the measured conducted-noise frequency spectra are shown in Fig. 9 using different frequency modulation profiles. It is clear that the noise peaks are concentrated mainly in two regions: the first region in the low-frequency (LF) range (0.15–1 MHz) around the frequencies which have higher probability mass levels and the other region in the high-frequency (HF) range (1–30 MHz).

A comparison has been carried out by subtracting the conducted-noise peak of the PWM regime from that of the variable frequency modulation regime in the two regions. Table II summarizes the measured experimental results for the frequency modulation regimes with different profiles.

### B. Randomization ratio percentage Effect

The results, shown in Fig. 10, reveal that increasing the randomization ratio increases the noise level reduction until a certain ratio where the noise level reduction again decreases. The latter is due to the increased low-frequency noise and the overlaps between the successive frequency spectrum ranges in case of higher randomization ratios that can be clarified as follows:

Assuming a random pulse train with a uniform frequency distribution at a constant duty ratio, as shown in Fig. 11, the switching frequency changes uniformly from  $f_L$  up to  $f_H$  in the range of  $f_{csw} \pm \Delta f$ . As illustrated in Fig. 12a, at zero  $\Delta f$  i.e. fixed switching frequency PWM, the frequency spectrum of the pulse train will be concentrated at the switching frequency and its multiples.

Slightly increasing  $\Delta f$  as random PWM spreads the spectrum's peaks as in Fig. 12b. However, large values of  $\Delta f$  cause overlapping between the successive frequency spectrum ranges that increases the frequency spectrum envelope which in turn increases the low-frequency components. In addition, it also generates superposed peaks with higher values than those generated using a low  $\Delta f$ , as shown in Fig. 12c. To avoid such overlapping, the boundaries of the switching frequency variation should fulfill the following constraint.

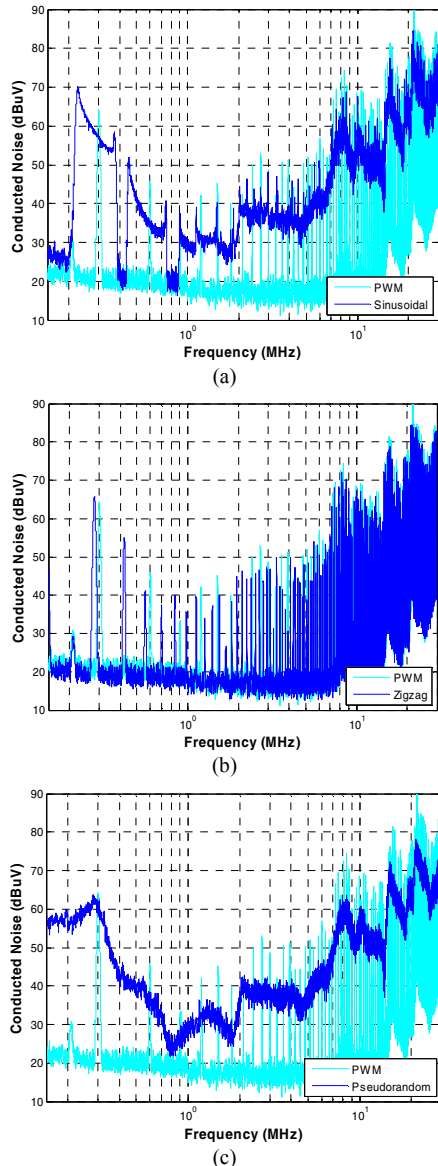


Fig. 9. Sample of the measured conducted-noise frequency spectra using different frequency modulation profiles.

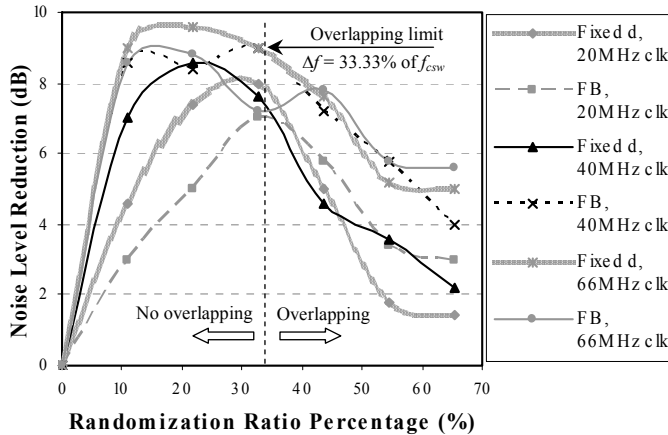


Fig. 10. The effect of randomization ratio percentage on the noise level reduction.

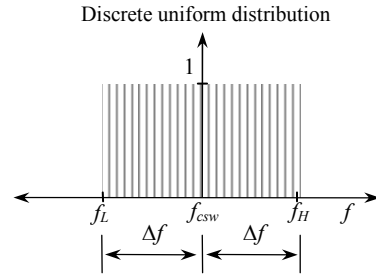


Fig. 11. Frequency variation's normalized probability mass function.

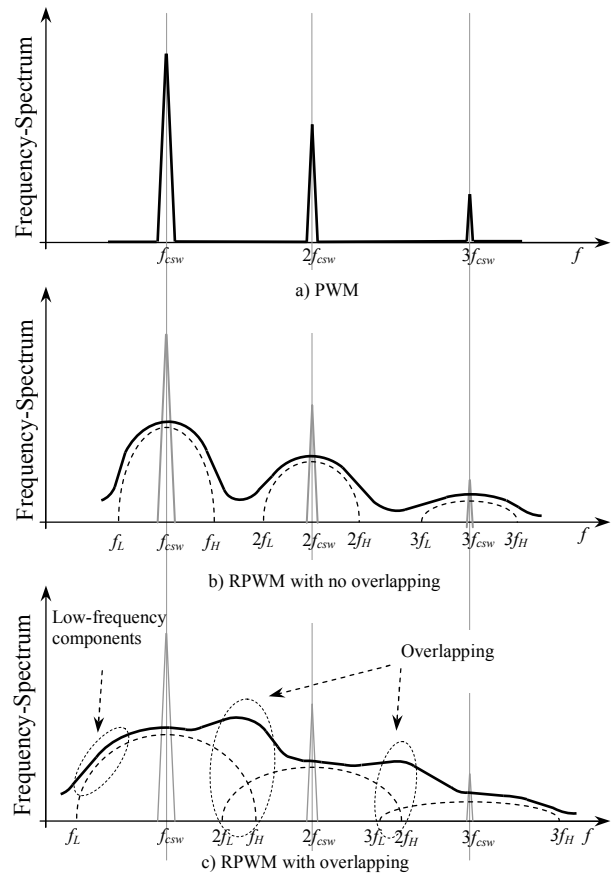


Fig. 12. Overlapping between the successive frequency spectrum ranges.

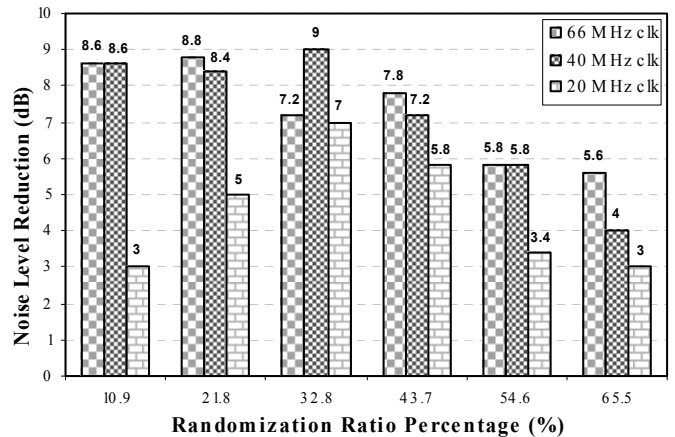


Fig. 13. The effect of FPGA clock speed on the noise level reduction.

TABLE II: SUMMARY OF THE EXPERIMENTAL RESULTS FOR THE FREQUENCY MODULATION REGIMES WITH DIFFERENT PROFILES.

Group	Series	Frequency modulation profile	Noise level reduction, dB		Percentage increase of ripple voltage with the reference of that at PWM	Acoustic noise
			LF	HF		
I	1	Sinusoidal modulation	-6.0	6.0	3.90625	No
	2	Triangular modulation	-5.1	11.2	2.734375	No
	3	Sawtooth modulation	-3.0	12.5	3.125	Small
	4	Exponential modulation	-2.2	11.0	0.78125	No
	5	Square modulation	-7.8	-0.2	3.90625	Large
	6	Zigzag modulation	-1.7	5.8	0	No
II	7	<b>Chaotic modulation</b>	<b>1.2</b>	<b>11.3</b>	<b>0.78125</b>	<b>Small</b>
	8	Markov chain based random modulation	0.5	8.8	1.5625	Large
	9	<b>Uniformly distributed random modulation</b>	<b>0.8</b>	<b>11.4</b>	<b>0</b>	<b>No</b>
	10	Normally distributed random modulation	-1.2	11.4	-0.390625	Small
	11	M-sequence based random modulation	-2.1	6.5	0.78125	Large
	12	<b>Pseudorandom stream modulation</b>	<b>0.5</b>	<b>12.3</b>	<b>0</b>	<b>No</b>

$$f_H \leq 2f_L \quad (4)$$

substitute with:

$$f_L = f_{csw} - \Delta f, \text{ and}$$

$$f_H = f_{csw} + \Delta f,$$

then,

$$f_{csw} + \Delta f \leq 2(f_{csw} - \Delta f)$$

$$3\Delta f \leq f_{csw}$$

thus,

$$\Delta f / f_{csw} \leq 1/3 \quad (5)$$

That means  $\Delta f \leq 33.33\%$  of  $f_{csw}$  which strongly agrees with the experimental results shown in Fig. 10.

### C. Clock Frequency Effect

As illustrated in Fig. 13, the noise level reduction increases with using higher FPGA clock speed, since the randomization resolution increases, as discussed in section II.C.

### D. Spread-Spectrum Scheme Effect

Figure 14 presents the effect of the spread-spectrum schemes on the conducted-noise peak reduction at both low- and high-frequency ranges. This comparison has been carried out by subtracting the conducted-noise peak of the PWM scheme from that of the spread-spectrum scheme in high- and low-frequencies.

It is clear that the RCFRPPMFD and RCFMVD schemes achieve a similar performance. The RPWM scheme gives the worst performance. It hardly improves the conducted-noise spectrum in the high-frequency range. Moreover, it increases the conducted-noise peak in the low-frequency range.

On the other hand, the RRRM scheme attains the best performance. It provides the highest conducted-noise peak

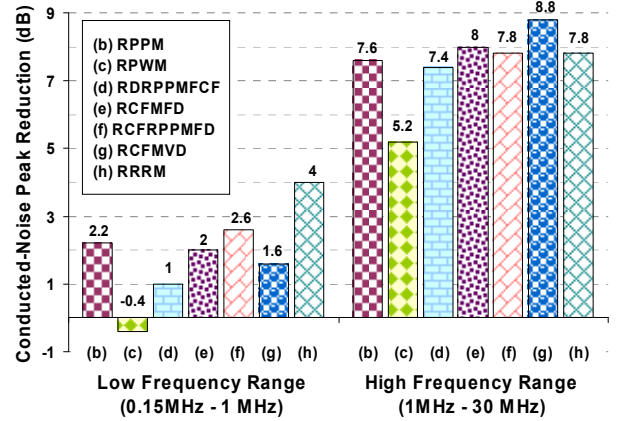


Fig. 14. The effect of the spread-spectrum schemes on the conducted-noise peak reduction.

reduction in the low-frequency range. Furthermore, it decreases the conducted-noise peak in the high-frequency range.

## V. CONCLUSION

Several factors affecting EMI-performance of digital controllers targeted at conducted-noise reduction in dc-dc converters have been investigated. It can be concluded that:

1. Both of frequency modulation sequence profile and its statistical characteristics should be considered when designing a programmed switching controller targeted conducted-noise reduction in dc-dc converters. Moreover, the chaotic modulation, uniformly distributed random modulation, and pseudorandom modulation

regimes attain good EMI performance. In addition they do not deteriorate the converter's normal operation.

2. Increasing the randomization ratio increases the noise reduction until a certain ratio where the noise reduction again decreases. The latter is due to the increased low-frequency noise and the overlaps between the successive frequency spectrum ranges. To avoid such overlapping, the randomization ratio shouldn't be taken more than  $\pm$  one third of the central switching frequency.
3. Increasing the FPGA clock speed improves the conducted-noise spectrum of the converter. On the other hand, the higher FPGA clock speed, the higher FPGA cost.
4. The switching frequency, as a randomization parameter, is more efficient in spreading the conducted-noise than the duty ratio or the pulse position parameters. The RRRM scheme attains the best EMI performance. It improves the conducted-noise characteristics, not only in the low-frequency range, but also in the high-frequency range.

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