

A Novel Digital PID Controlled DC-DC Converter

Fujio Kurokawa*, Yuki Maeda*, Yuichiro Shibata* and Hironori Maruta*

Tsukasa Takahashi**, Kouta Bansho**, Toru Tanaka** and Keiichi Hirose **

* Nagasaki University, 1-14 Bunkyo-machi, Nagasaki, 852-8521, (Japan)

** NTT Facilities, Inc., 3-4-1 Shibaura-ku, Tokyo, 108-0023, (Japan)

Abstract—This paper presents the relationship between the dynamic characteristics and sampling frequency of digitally controlled dc-dc converter with a novel control method. In the proposed method, the calculation process of P and I-D controls is parallel. The sampling interval and points for I-D control are same to the conventional method. However, the sampling point for P control is quickly. The A-D converter can sample the output voltage during the short interval because the calculation process of P control is very simple and to important for transient response. The only sample data near the turn-off timing of PWM pulse is used. The simulation and experiment results of the output voltage against the step change of the load and changing the P control sampling frequency are discussed. As a result, it is revealed experimentally that the good transient response is obtained.

Index Terms— DC-DC power conversion, Digital control, Sampling methods, Proportional control.

I. INTRODUCTION

In Japan, the national project is established to save the energy in the information and communication field and is called “NEDO (Japan New Energy and Industrial Technology Development Organization) Green IT Project.” In this project, it is very important to control the many dc-dc converters quickly and systematically in the data center because not only servers but also dc-dc converters operate the down and up conditions every moment to achieve the energy saving. In this case, the power supply system requires the high performance characteristics, the high energy management function and the high reliability more. So, the digitally controlled dc-dc converter is useful because it has the advantage of realizing the high performance control and monitoring tasks [1]-[5]. Furthermore, a key distinguishing feature of digital control circuit is easily able to communicate to the other component in the system. However, the digital control circuit for dc-dc converter has some problems. Especially, the central research target of digital control circuit is to improve the dynamic characteristics because the conversion time of the A-D converter and the processing time of digital controller exert a bad influence upon the dynamic characteristics.

This paper presents the relationship between the sampling frequency of proportional control and dynamic

characteristics of proposed digitally controlled dc-dc converter with a novel control method. In the proposed method, the sampling interval for I-D control is same to the conventional method. However, that of P control is oversampling [6].

II. OPERATION PRINCIPLE

Figure 1 shows the block diagram of the digitally controlled buck type dc-dc converter. E_i is the input voltage, and e_o is the output voltage. T_r is the main switch, D is the fly wheel diode, L is the energy storage reactor, C is the output smoothing capacitor and R is the load.

The digital control circuit is composed of the PID control calculator with DSP, A/D converter and Digital PWM Generator. The conventional digital control circuit has each only one device as show in Fig. 2(a). On the other hand, the proposed digital control circuit is divided to two calculation part as show in Fig. 2(b). There are P control calculation and ID control calculation. Each of control calculation have original A/D converter. Each A/D converter has respectively sampling frequency.

The output voltage e_o is sent to the digital converter through the A-D converter. In the conventional digital control method, the sampling rate is single in the A-D converter as shown in Fig. 3(a) and the calculation process of P-I-D control is series. On the other hand, in the proposed method, the sampling rate is multiple as shown in Fig. 3(b) and the calculation process of P and I-D controls is parallel. The sampling interval and points for I-D control are same to the conventional method. However, the sampling point for P control is oversampling [7]. The A-D converter can sample the output voltage during the short interval as shown in Fig. 3(b) because the calculation process of P control is very simple. The sample data for P control are received by the digital control circuit. In Fig. 3, T_s is the switching period of dc-dc converter, T_{on} is the on-interval, T_{off} is the off-interval and M is the number of sampling points in the switching period.

Therefore, the transfer functions of conventional and proposed methods are shown as follows;

Conventional:

$$H(s) = (H_P + \frac{H_I}{s} + sH_D) \left(\frac{1}{1+s\tau} \right) \quad (1)$$

Proposed:

$$H(s) = H_P \left(\frac{1}{1+s\tau_1} \right) + \left(\frac{H_I}{s} + sH_D \right) \left(\frac{1}{1+s\tau_2} \right) \quad (2)$$

This work is supported in part by the Grant-in-Aid for Green IT Project of NEDO (Japan New Energy and Industrial Technology Development Organization) and the Ministry of Economy, Trade and Industry of Japan.

where H_p is a proportional gain, H_D is a differential gain and H_I is a integral gain. These equations prove that the influence of delay-time of proposed method is a little.

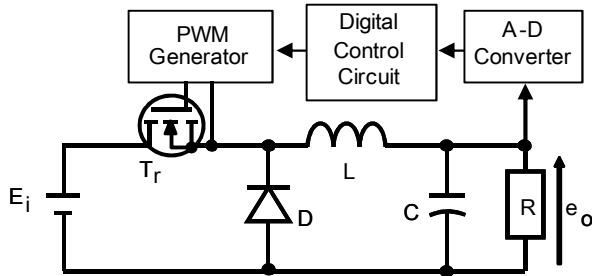
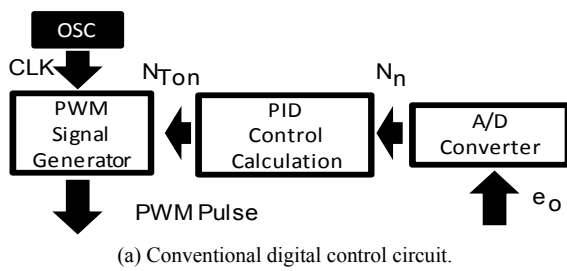
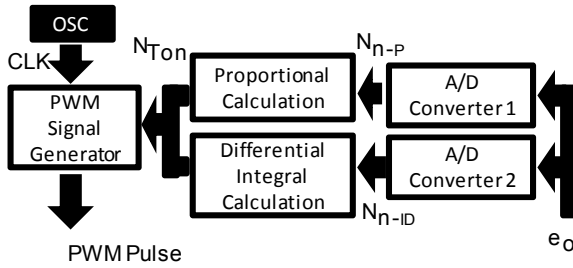


Fig. 1 Conventional Digital controlled dc-dc converter.

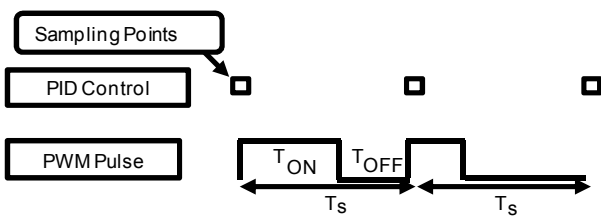


(a) Conventional digital control circuit.

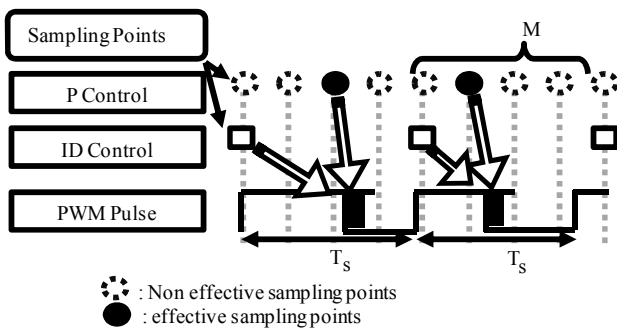


(b) Proposed digital control circuit.

Fig. 2 Digital control circuit.



(a) Conventional



○ : Non effective sampling points
● : effective sampling points

(b) Proposed

Fig. 3 Sampling method.

III. CHARACTERISTICS

Here, we will discuss the transient responses of the conventional digital and proposed digital in step change of the load resistor R from 20Ω to 10Ω . The simulator is PSIM. The switching frequency is 100kHz and then the switching period T_s is $10\mu\text{s}$. The circuit parameters are $E_i=20\text{V}$, $E_o=10\text{V}$, $L=513\mu\text{H}$, $C=95\mu\text{F}$, $H_p=0.2[1/\text{V}]$, $H_D=1[\text{msV}]$, $H_I=2.5[1/(\text{sV})]$, $\tau=T_s$, $\tau_1=T_s/M$, $\tau_2=T_s$. The number of bit of A-D converter is 11 bits.

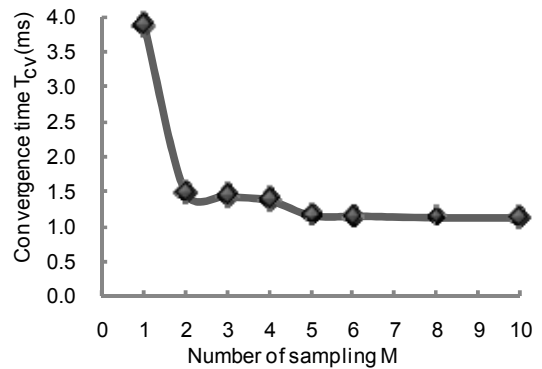


Fig. 4 T_{CV} against the number of sampling points M .

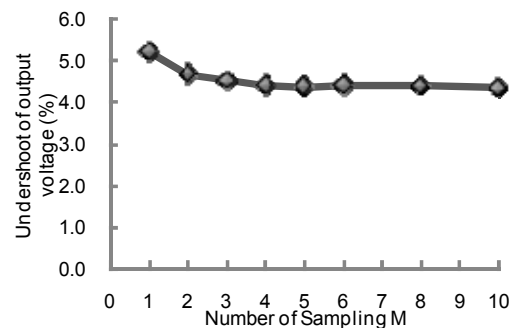


Fig. 5 Undershoot of output voltage against the number of sampling points M .

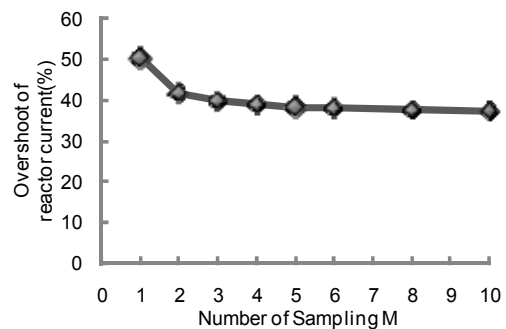
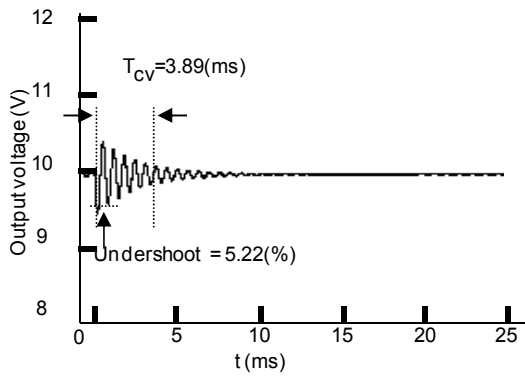
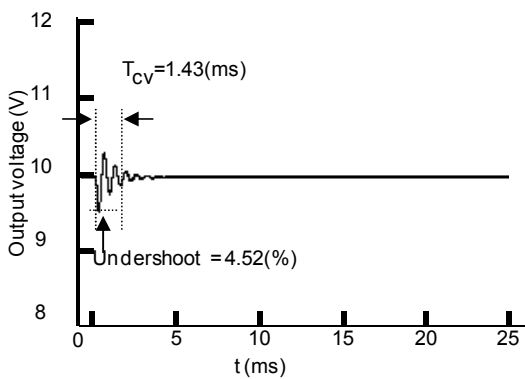


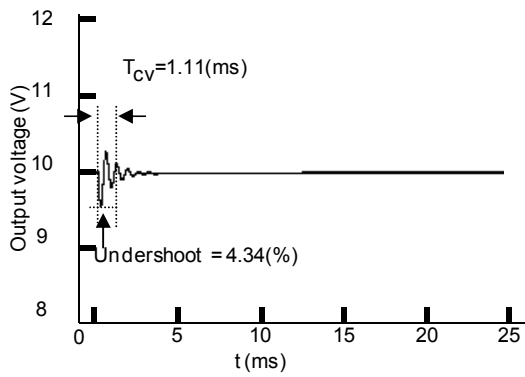
Fig. 6 Overshoot of reactor current against the number of sampling points M .



(a) $M=1$



(b) $M=3$



(c) $M=10$

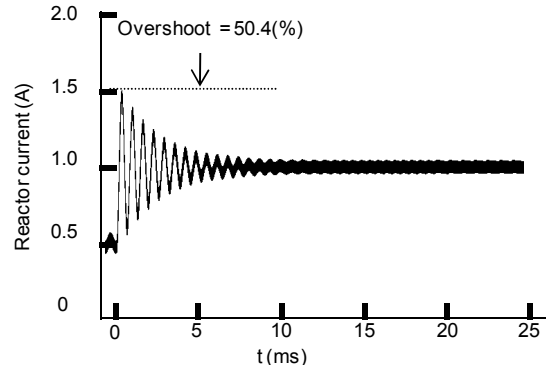
Fig. 7 Simulated transient response of output voltage e_o .

Figure 4 shows convergence time T_{CV} that the output voltage e_o is settled within 1% in the case of increased the number of sampling per period M . If M is change from 1 to 2, convergence time T_{CV} is decreased to as much as over 1/3. When M increased more 5, T_{CV} decrease more than $M=2$. In the result by this figure, it seen that increasing the number of sampling M improve

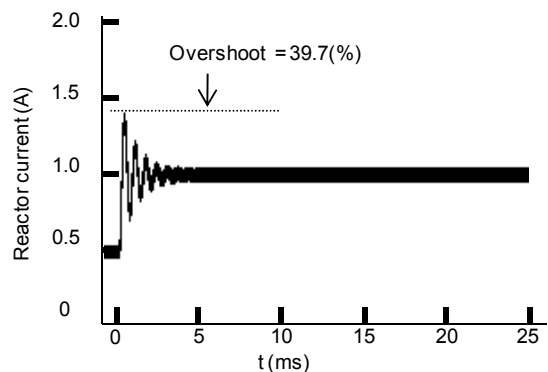
convergence time T_{CV} . Then M is 1 that means the conventional method..

Figure 5 shown the undershoot of output voltage e_o in the case of increased M . When the number of sampling M increase, the undershoot decrease slowly.

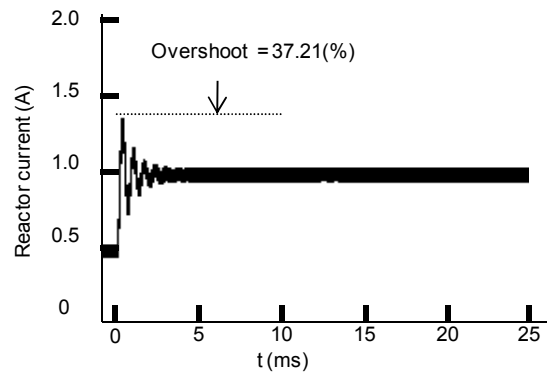
Figure 6 shows the overshoot of reactor current in the case of increasing M . In the result, Overshoot of reactor current is improved about 10%.



(a) $M=1$



(b) $M=3$



(c) $M=10$

Fig. 8 Simulated transient response of reactor current i_L .

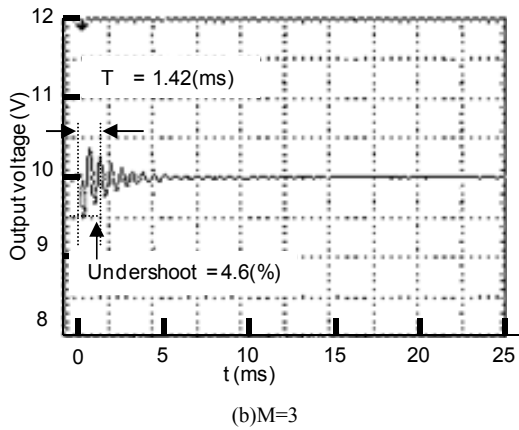
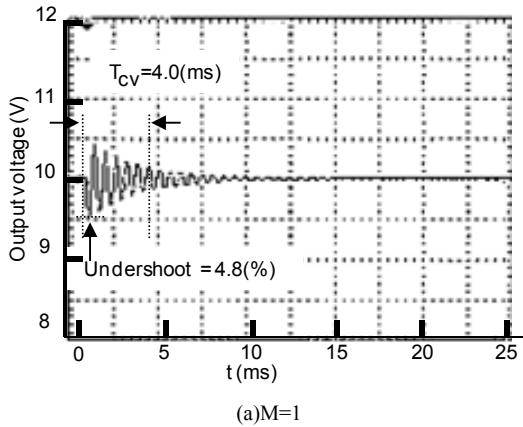


Fig. 9 Experimental transient response.

Figure 7 shows the transient response that the number of sampling M is 1, 3 and 10. Then the number of sampling M is 1 mean to equal conventional method. in conventional digitally controlled method, the undershoot of output voltage e_o is over about 2.8% as shown in Fig. 7(a). On the other hand, the convergence time of the output voltage is 1.43ms when the number of sampling M is 3. The undershoot is less than 4.52% as shown in Fig. 7(b). When the case of M is 10, undershoot and convergence time are less than 4.34% and 1.11ms as shown in Fig. 7(c). When the number of sampling is small and closed in the conventional method, it is seen that the transient response is deteriorated extremely.

Figure 8 shows the reactor current transient response. The overshoot of reactor current is over about 50.4% when conventional controlled as shown in Fig. 8(a). On the other hand, the overshoot reactor current in the proposed control $M=3$ are less than 39.7%, respectively, as shown in Fig. 8(b). When the number of sampling M is 10, there are less than 37.21% as shown in Fig. 8(c). It is

seen that the transient response is deteriorated extremely in the conventional method when the number of sampling is large.

Figures 9(a) and (b) show the experimental results of in case of conventional digital control and proposed digital control. The experimental result agrees well with the simulated one. It is revealed from these figures that the proposed method has superior transient response compared with the conventional digital control method, as increase the number of sampling M . The transient time becomes less than over half in the larger M .

Furthermore, the result of proposed method is almost equal to the ideal one.

IV. CONCLUSION

This paper presents a design criterion of proposed digitally controlled dc-dc converter and its dynamic characteristics. From the previous discussion, it is revealed that the proposed digital method has a superior transient response. The convergence time of output voltage is less than 1/3 of that of conventional one when the output capacitance is small and oversampling frequency is 3 times against the switching period.

Moreover, it is expected that the subject of Green IT Project can be achieved by this method.

References

- [1] J. Xiao, A. V. Peterchev, and S. R. Sanders: "Architecture and IC implementation of a digital VRM controller," in *IEEE PESC Record*, June 2001, pp. 38-47.
- [2] L. Guo, J. Y. Hung and R. M. Nelms: "PID controller modifications to improve steady state performance of digital controllers for buck and boost converters," in *Proc. Annual IEEE Applied Power Electronics Conference*, no.9.3, March 2002, pp. 381-388.
- [3] Q. M. Li: "A low-cost configurable PWM controller using programmable system-on-chip," in *IEEE PESC Record*, June 2003, pp. 1169-1174.
- [4] F. Kurokawa and W. Okamoto: "A consideration of digital control circuit for dc-dc converter," in *Proc. IAS International Conference on Electrical Machines and Systems*, vol.3, no. DS2E3-06, Nov. 2006, pp.1-5.
- [5] F. Kurokawa and W. Okamoto: "Improvement of dynamic characteristics of digitally controlled switching power converter," in *Proc. IEEE & IEEJ Power Conversion Conference*, vol. 4, no.1, April 2007, pp.1147-1153.
- [6] H. Fujimoto and Y. Hori: "Advanced digital motion control based on multirate sampling control," in *Proc. IFAC Triennial World Congress*, July 2002, pp. 1603-1608.
- [7] F. Kurokawa and Y. Maeda: "A new digital control circuit for green switching power supply," in *Proc. EVER Grimaldi Forum - Monaco*, March 2010 Ever10-331.
- [8] S. Efler, Z. Lukic and A. Prodic "Oversampled digital power controller with bumpless transition between sampling frequencies," *IEEE ECCE*, S9-2a-1 Sep. 2010, pp. 3306-3311.