Dynamic Characteristics of Digitally Controled Conveter with Pole-Zero-Cancellation Techique

Seiya Abe
ICSEAD
Kitakyushu, Japan
abe@icsead.or.jp

Mariko Ogawa & Masahito Shoyama
Kyushu University
Fukuoka, Japan
ogawa@ckt. & shoyama@ ees.kyushu-u.ac.jp

Toshiyuki Zaitsu & Satoshi Obata
Texas Instruments Japan Ltd.
Tokyo, Japan
t-zaitsu & oba @ti.com

Tamotsu Ninomiya
Nagasaki University
Nagasaki, Japan
ninomiya@nagasaki-u.ac.jp

***Abstract*— Recently, the performance of the DSP and FPGA is developed remarkably. So, fully digital control is enabled in switch mode power supplies. However, in many cases, the control system is built by very complicatedly and very difficult theories such as the adaptive control. Furthermore, in most popular PID control, its design method of the parameters is not clear, so derivation of the optimal parameters is very difficult. This paper proposes the interesting control technique which is cancelled the transfer function of the converter by using pole-zero-cancellation method. This technique is very simple and easy to stability design.**

Keywords-component; digital control; pole-zero-cancellation; stability; transient response

I. INTRODUCTION

Many types of electric equipments are digitized in recent years. However, the configuration of switch mode power supply is still only analog circuit because the analog circuit is held down to low cost. The digitized system is operated on the basis of a processor. When the switch mode power supply is treated as a part of the system, it is difficult that switch mode power supply inhabit alone in the system as the analog-circuit. Therefore, the digitization of the switch mode power supply is necessary to harmonize with other electronic circuits in the system. So far, various examinations have been discussed about digitally controlled switch mode power supplies[1-5]. However, important parameters such as the switching frequency were impractical because the performance of processor was not so good. Recently, due to the development of the semiconductor manufacture technology, the performance of processor such as DSP and FPGA is developed remarkably. Hence, the expectation of the practical realization in the digitally controlled switch mode power supply becomes higher.

So far, in many case on digitally controlled switch mode power supply, the control system is constructed by very complicated, difficult modern control theory (nonlinear control theory) such as adaptive control or predictive control.

Moreover, also in the most popular and easiest control method such as PID control, the design method is not so clear, and the optimal design is difficult[6, 7].

On the other hand, there are two methods of controller design. One is the digital direct design. The other is the digital redesign. The digital redesign method converts the analog compensator which is designed on s-region into digital compensator. The digital redesign method has some advantages. For example, the control system is designed from classical control theory (linear control theory). Therefore, many experiences and design techniques of the conventional analog compensator can be utilized. Moreover, from the practical stance, the digital redesign method is more realistic than digital direct design.

This paper investigates the digitally controlled switch mode power supply by means of classical control theory. Especially, the interesting control technique which is cancelled the transfer function of the converter by using pole-zero-cancellation technique is introduced. This technique is very simple and stability design of converter system is very easy. Furthermore, the arbitrary frequency characteristics can be created by introducing a new frequency characteristic. Here, the design method and system stability of the proposed control technique is examined by using buck converter as a simple example.

II. DYNAMIC CHARACTERISTICS OF BUCK CONVERTER

For the design of the control system, it is necessary to grasp correctly the characteristics of the converter in detail. The synchronous buck converter as the controlled objects is shown in Fig. 1. The dynamic characteristics of buck converter can be derived by applying the state space averaging method[8,9]. The dynamic characteristic of duty to output voltage of each converter is derived following equation;

$$G_{dv}(s)=\frac{\Delta V_o(s)}{\Delta D(s)}=\frac{G_{dvo}(s)}{P(s)} \quad (1)$$

where;

$$P(s)=\frac{s^2}{\omega_o^{\,2}}+s\frac{2\delta}{\omega_o}+1 \quad (2)$$

$$G_{dvo}(s)=\left(\frac{s}{\omega_{esr}}+1\right)\frac{R}{R+r_L}V_i \quad (3)$$

$$\omega_o=\sqrt{\frac{R+r_L}{LC(R+r_c)}} \quad (4)$$

$$\delta=\frac{L+C\{Rr_c+r_L(R+r_c)\}}{2\sqrt{LC(R+r_c)(R+r_L)}} \quad (5)$$

$$\omega_{esr}=\frac{1}{Cr_c} \quad (6)$$

Figure 2 shows the block diagram of analog system. From, Fig. 2, the loop gain of analog controlled converter can be derived following equation;

$$T(s)=\frac{\Delta V_o(s)}{\Delta V_o^{*}(s)}=\frac{G_{dvo}(s)}{P(s)}\cdot G_c(s)\cdot K\cdot K_s\cdot PWM \quad (7)$$

where;

Gc(s) : Transfer function of phase compensator

K : DC gain of error amp.

Ks : Sense gain of output voltage

PWM : transfer gain of voltage to duty

In order to evaluate the validity of the analytical result, the experimental circuit is implemented by means of the specifications and parameters shown in Table 1. Figure 3 shows the loop gain of the buck converter with p-control in analog control. As shown in Fig. 3, the analytical and experimental results are agreed well. However, as shown in Fig. 4, the big difference is shown in phase characteristics at high frequency side between analog control and digital control.

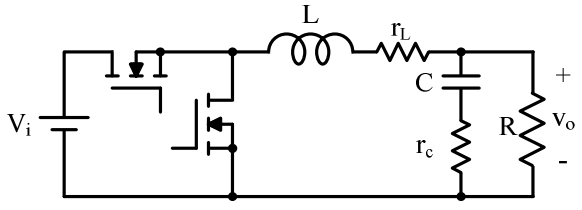

Figure 1. Synchronous buck converter.

In digital control system, the output voltage as a detected signal is converted to digital signal by AD converter, after that the converted signal is calculated by DSP. Next, the calculated signal decides the duty ratio of next switching period. Hence, the information of the output voltage as the detected signal at certain switching period is reflected into the duty ratio of the next switching period. Therefore, the dead time element He(s) is included into the control loop as shown in Fig. 5. From Fig. 5, the loop gain of digital controlled system can be derived following equation;

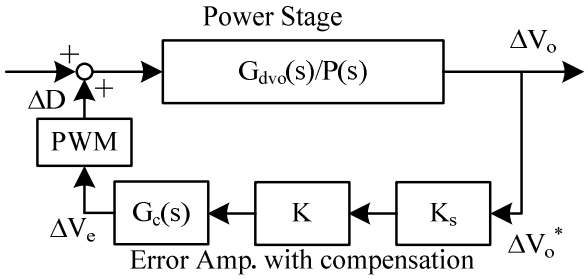

Figure 2. Block diagram of analog system.

TABLE I. CIRCUIT PARAMETERS AND SPECIFICATIONS

Symbol	Description	Value
Vi	Input Voltage	12V
Vo/Io	Load Condition	2.5V/5A
L	Filter Inductor	22μH
C	Filter Capacitor	470μF
r_L	DC Resistance of L	100mΩ
r_c	ESR of C	25mΩ
R	Load Resistance	1Ω
K_s	Sense Gain	0.25
K	Feedback DC Gain	5
PWM	PWM Gain	0.5
f_s	Switching Frequency	100kHz
T_{sample}	Sampling Period	10μs

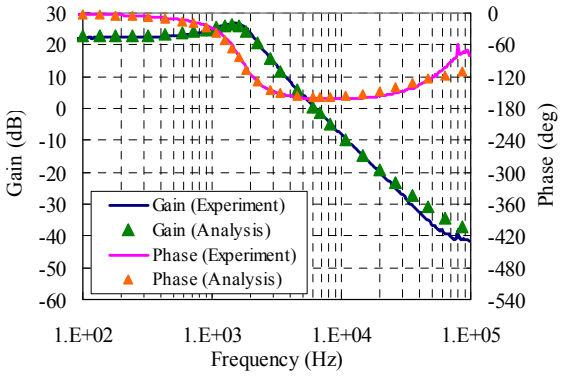

Figure 3. Frequency response of loop gain (analog control).

$$T(s)=\frac{\Delta V_o(s)}{\Delta V_o^*(s)}=\frac{G_{dvo}(s)}{P(s)}\cdot G_c(s)\cdot H_e(s)\cdot K\cdot K_s\cdot PWM \quad (8)$$

where;

$$H_e(s)=e^{-sT_{sample}} \quad (9)$$

Gc(s) : Transfer function of phase compensator

K : DC gain of error amp.

Ks : Sense gain of output voltage

DPWM : transfer gain of voltage to duty

He(s) : Dead time component of digital controller

Figure 6 shows the frequency response of dead time element He(s). As shown in Fig. 6, the gain characteristic does not depend on frequency and it is constant. On the other hand, phase characteristic depends on frequency. The phase is rotated around 180 degrees at Nyquist frequency (=f/2), and it is rotated around 360 degrees at switching frequency (sampling frequency). From these results, the phase is drastically rotated at high frequency side by the influence of dead time element He(s). In order to evaluate these discussions, the experimental circuit is implemented by means of the specifications and parameters shown in Table 1.

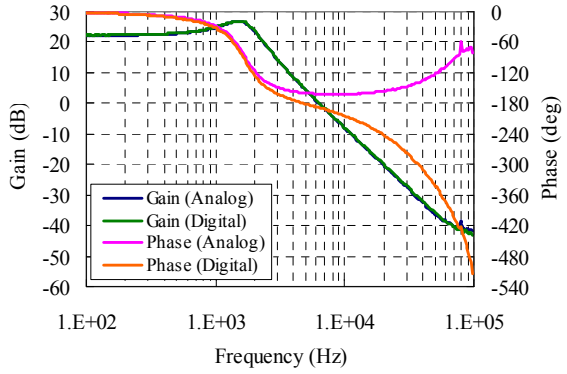

Figure 4. Frequency response comparison of analog control and digital control (Experiment).

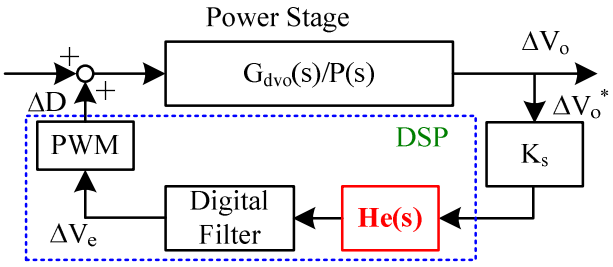

Figure 5. Block diagram of digital system.

Moreover, the experimental result is compared with analytical result. Figure 7 shows the loop gain of the buck converter with p-control in digital control. As shown in Fig. 7, the analytical and experimental results are agreed well. In analog control system, the phase characteristic of frequency response is improved at higher frequency side by the influence of ESR-Zero as shown in Fig. 4, and the system has stable operation.

On the other hand, in digital control system, the phase characteristic of frequency response is drastically rotated by the influence of the dead time element He(s) as shown in Fig. 7. As a result, the phase margin disappears, and the system becomes unstable.

In digital control system, the phase rotation is larger than analog control system by the influence of the dead time element He(s), so the phase compensation is necessary to keep the system stability.

III. Conventional Phase Compensation

The phase compensation is usually used to improve the system stability. There is various phase compensation. Here, the phase lead-lag compensation is used as the most popular compensation.

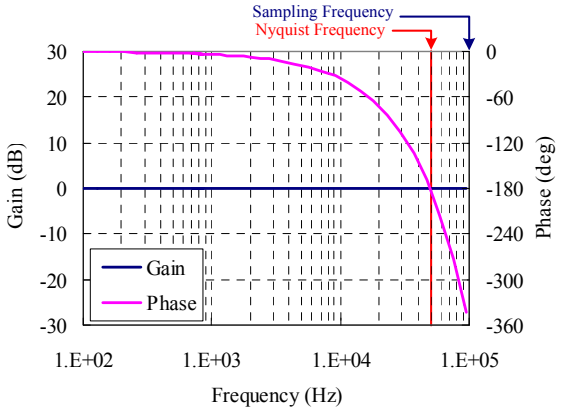

Figure 6. Frequency response of dead time element He(s).

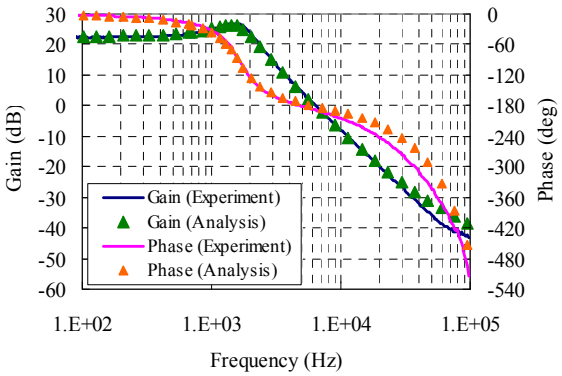

Figure 7. Frequency response of loop gain (digital control).

The digital filter is designed by digital redesign method. The transfer function of phase lead-lag compensation is given by following equation;

$$G_c(s)=\frac{\Delta v_e}{\Delta v_o^*}=\frac{K_c\left(\frac{s}{\omega_{z1}}+1\right)\left(\frac{s}{\omega_{z2}}+1\right)}{\left(\frac{s}{\omega_{p1}}+1\right)\left(\frac{s}{\omega_{p2}}+1\right)} \quad (10)$$

The digital filter can be realized by means of the bilinear transformation.

Figure 8 shows the analytical result of loop gain frequency response with phase lead-lag compensation. Where, Kc=10000, fp1=0.03Hz, fz1=1.3kHz, fp2=20kHz, fz2=1.5kHz. As shown in Fig. 8, this system has the stable operation, and then the bandwidth is around 5.5kHz, the phase margin is around 45 degrees. Figure 9 shows the experimental result of loop gain frequency response with phase lead-lag compensation. In this case, the bandwidth is around 5kHz, and the phase margin is around 45 degrees. Moreover, the analytical and experimental results are agreed well. Thus, the observation of control object frequency response is needed in classical control theory (linear control theory).

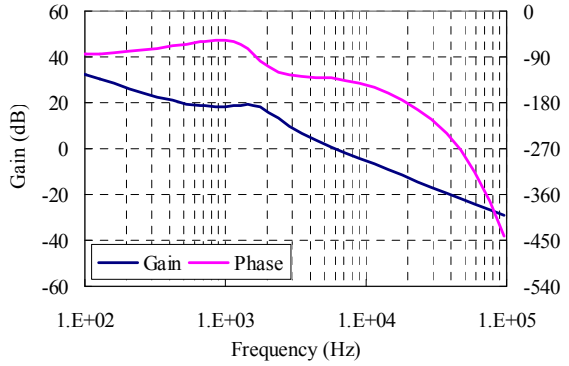

Figure 8. Frequency response of loop gain with phase lead-lag compensation (analytical result)

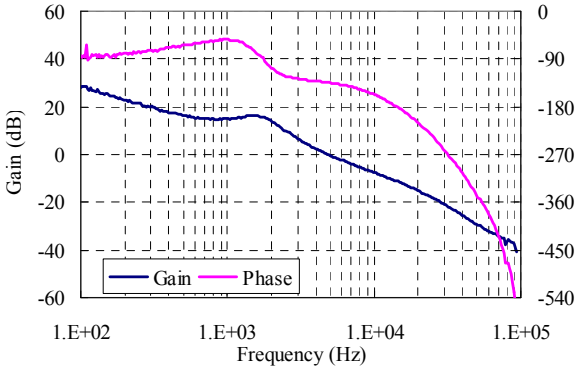

Figure 9. Frequency response of loop gain with phase lead-lag compensation (experimental result)

Moreover, much experience and knowledge are needed for controller design, because many parameters in compensator should be decided. Therefore, the design method is not so clear and depends on knowledge and experience, and the optimal design is difficult.

The controller design becomes very simple if the controller design is enabled without considering the frequency response of the converter as the control object.

IV. Dynamic Characteristic Improvement by Pole-Zero-Cancellation Technique

Reduction of the phase rotation is very important for system stability. Especially in the second order system, the phase is drastically rotated around 180 degrees at resonance peak. The stability of the system is improved remarkably if the phase rotation can be reduced.

This paper proposes the control technique which is cancelled the transfer function of the converter by means of pole-zero-cancellation method. The phase rotation and gain change can be suppressed by canceling the converter characteristics. Furthermore, new characteristic can be designed in the system as the arbitrary transfer function.

Figure 10 shows the block diagram of converter system including the pole-zero-cancellation technique. From Fig. 10, the transfer function of compensator part is given following equation;

$$G_c(s)=G_{new}(s)\cdot G_{pzc}(s) \quad (11)$$

The Gnew(s) is the arbitrary transfer function. This transfer function decides the frequency response of converter system. Here, the Gnew(s) is defined as simple low pass filter.

$$G_{new}(s)=\frac{K_c}{\frac{s}{\omega_c}+1} \quad (12)$$

In buck converter case, the resonance peak and ESR-Zero are cancelled. The phase rotation of 180 degree is reduced by cancelling resonance peak. The transfer function of the pole-zero-cancellation Gpzc(s) is given following equation;

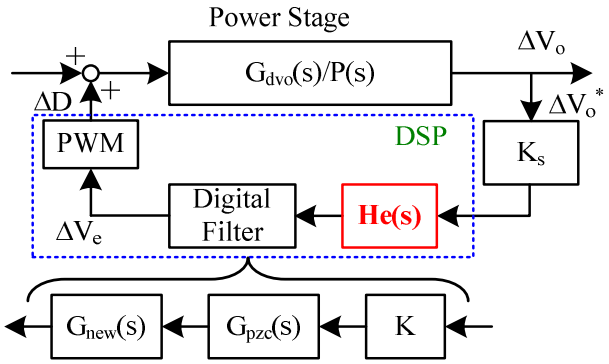

Figure 10. Block diagram of digital system with PZC contorl.

$$G_{pzc}(s) = \frac{\frac{s^2}{\omega_o^2} + s\frac{2\delta}{\omega_o} + 1}{\frac{s}{\omega_{esr}} + 1} \quad (13)$$

Moreover, the transfer function of the compensator is given following equation;

$$G_c(s) = K_c \frac{\frac{s^2}{\omega_o^2} + s\frac{2\delta}{\omega_o} + 1}{\left(\frac{s}{\omega_{esr}} + 1\right)\left(\frac{s}{\omega_c} + 1\right)} \quad (14)$$

The digital filter can be realized by means of the bilinear transformation.

Figure 11 shows the frequency response of PZC part Gpzc(s). As shown in Fig. 11, the ant resonance peak is appeared at the same frequency of power stage frequency response. Figure 12 shows the analytical result of the loop gain frequency response with PZC technique. Here, Kc=10000, fc=0.07Hz.

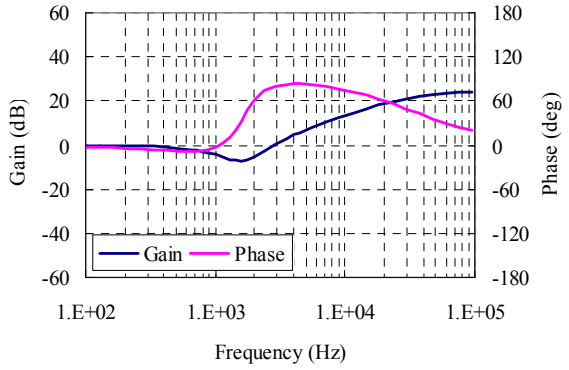

Figure 11. Frequency response of PZC part (analytical result)

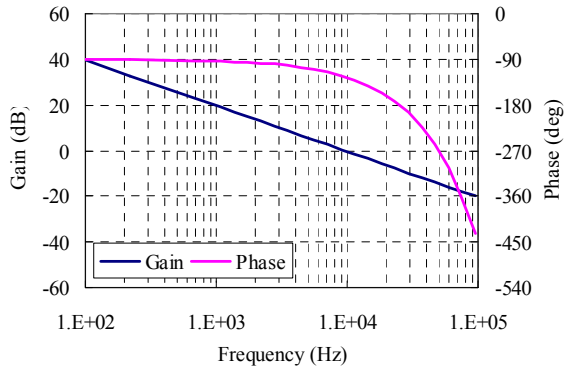

Figure 12. Frequency response of loop gain with PZC technique (analytical result)

As shown in Fig. 12, this system has the stable operation, and then the bandwidth is around 10kHz, the phase margin is around 50 degrees. Moreover, the resonance peak and ESR-Zero are completely cancelled, and this system becomes 1st order response. From these results, the converter frequency response is completely cancelled by the influence of PZC part, and the new characteristic is created (1st order characteristic).

Figure 13 shows the experimental result of loop gain frequency response with PZC technique. In this case, the bandwidth is around 10kHz, and the phase margin is around 50 degrees. Moreover, the analytical and experimental results are agreed well.

V. TRANSIENT RESPONSE

The transient response of the conventional phase lead-lag compensation and the PZC technique are measured using experimental circuit of 2.5V/5A during the step load transition from 1A to 4A (10A/ms). Figure 14 shows the transient response of the conventional phase lead-lag compensation. In this case, the output voltage drop is around 320mV and the transient time to the steady state is around 400µs. On the other hand, in the case with PZC technique, the output voltage drop is around 160mV and the transient time to the steady state is around 200µs as shown in Fig. 15, and the transient response is improved.

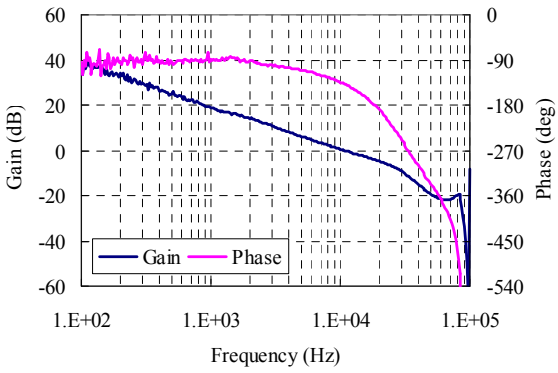

Figure 13. Frequency response of loop gain with PZC technique (experimental result)

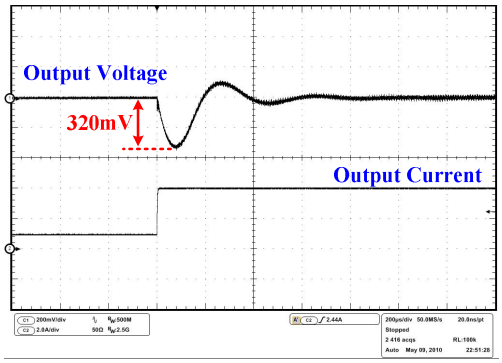

Figure 14. Transient response (Phase lead-lag compensation)

VI. CONCLUSIONS

This paper proposes the control technique which is cancelled the transfer function of the converter by means of pole-zero-cancellation technique. This technique is very simple and easy to stability design of converter system. Furthermore, the arbitrary frequency characteristics can be created by introducing a new frequency characteristic. Here, the design method and system stability of the proposed control technique is examined analytically and experimentally by using buck converter. As a result, the effectiveness of proposed control technique is confirmed. Moreover, it is confirmed that the characteristic cancellation of the converter can be realized very easy and can be set the arbitrary characteristic. Furthermore, the transient response is improved by means of pole-zero-cancellation technique.

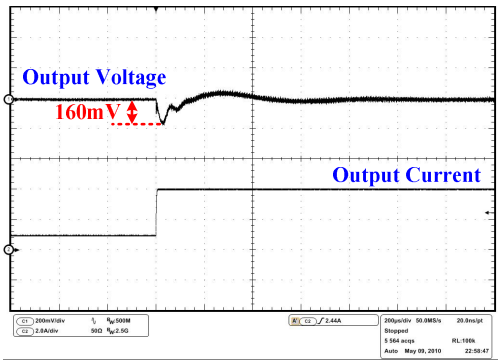

Figure 15. Transient reponse (PZC technique)

REFERENCES

[1] Philip T. Krein, "Digital Control Generations -- Digital Controls for Power Electronics through the Third Generation," IEEE PEDS'07, pp P-1-P5, 2007

[2] A. Kelly and K. Rinne, "Control of DC-DC Converters by Direct Pole Placement and Adaptive Feedforward Gain Adjustment," IEEE APEC'05, pp - , 2005.

[3] A. Kelly, K. Rinne,"A Self-Compensating Adaptive Digital Regulator for Switching Converters Based on Linear Prediction," IEEE APEC'06, pp 712-718, 2006.

[4] Y. Wen, S. Xiao, Y. Jin, I. Batarseh, "Adaptive Nonlinear Compensation for Asymmetrical Half Bridge DC-DC Converters," IEEE APEC'06, pp 731-736, 2006.

[5] L. Guo, J. Y. Hung, and R. M. Nelms, “Digital controller design for buck and boost converters using root locus,” IEEE IECON’03, pp. 1864-1869, 2003.

[6] H. Guo, Y. Shiroishi, and O. Ichinokura, “Digital PI controller for high frequency switching DC/DC converter based on FPGA,” IEEE INTELEC’03, pp-536-541, 2003.

[7] M. He, J. Xu, "Nonlinear PID in Digital Controlled Buck Converters," IEEE APEC'07, pp 1461-1465, 2007.

[8] R.D. Middlebrook, S. Cuk, “A General Unified Approach to Modeling Switching-Converter Power Stages,” IEEE Power Electronics Specialists Conference (PESC) 1976, pp. 18-34.

[9] T. Ninomiya, M. Nakahara, T. Higashi, K. Harada, “A Unified Analysis of Resonant Converters,” IEEE Transactions on Power Electronics Vol. 6. No. 2. April 1991, pp. 260-270.