5MHz PWM-Controlled Current-Mode Resonant DC-DC Converter Using GaN-FETs

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***Abstract*— In this paper, the method of the realization of a MHz level switching frequency DC-DC converter for high power-density is presented. For high power-density, Gallium Nitride field effect transistor (GaN-FET) and current-mode resonant DC-DC converter are adopted. In addition, the proposed pulse width modulation (PWM) control method which is suitable for the isolated current-mode resonant DC-DC converter operated at MHz level switching frequency, and the novel primary-side zero voltage switching (ZVS) turn on method for the proposed PWM control are presented.**

Some experiments have been done with 5MHz isolated DC-DC converter which has GaN-FET, and the total volume of the circuit is 16.14cm^3. With the proposed PWM control method, input voltage range is 36-44V, and maximum load current range is 8A at V_i = 44V. The primary-side ZVS turn on is confirmed, and the maximum power-efficiency is 89.4%.

***Keywords*— High Switching Frequency, PWM Control, Current-Mode Resonant DC-DC Converter, GaN-FET**

I. INTRODUCTION

Recently, high power-efficiency and high power-density DC-DC converters have been required in information and communication technology (ICT) equipment. Corresponding to the requirement of high power-density, the increase in the switching frequency of these converters has been considered to be one of key technologies. In particular, MHz level switching frequency contributes significantly to downsizing.

However, by adopting high switching frequency, power loss such as switching loss and gate driving loss increases. To solve this problem, the current-mode resonant DC-DC converter is effective because this converter can reduce switching loss. Also, GaN-FETs are suitable for high switching frequency operation as semiconductor switches because of low gate driving loss. Therefore, we have developed a 5MHz current-mode resonant DC-DC converter with GaN-FETs [1].

Current-mode resonant DC-DC converters are usually controlled by pulse frequency modulation (PFM). However, PFM control is hard to design to control the output voltage at MHz level switching frequency operation. The details are going to be described in the section III.

To solve the issue, this paper presents a novel PWM control method for the current-mode resonant DC-DC converter for MHz level switching frequency. This converter topology is same as the conventional current-mode resonant DC-DC converter with synchronous rectification. The feature of the converter is controlling the output voltage without any additional components. By using transformer's leakage inductance and secondary-side synchronously rectifying switches, the novel control method for boost conversion is realized.

In the previous researches, some PWM-controlled current-mode resonant DC-DC converters have been presented [2-4]. For example, the method of additional auxiliary circuits for regulating output voltage [2-3], and the method of controlling the duty ratio of primary-side switches [4] have been proposed. However, these methods need some additional components for regulating output voltage.

On the other hand, the advantages of the proposed method are controlling secondary-side switches and no additional components.

To accomplish the primary-side ZVS turn on, small magnetizing inductance L_m have been used in current-mode resonant DC-DC converter generally. However, small L_m leads to increase of primary-side current which is cause of reducing power-efficiency. Therefore, to accomplish the ZVS operation in the proposed method, phase-shift between primary and secondary-side switches which control resonant current is adopted. As a result, this proposed converter maintains primary-side ZVS turn on.

The targets of the study are to obtain the high performance which is the small volume, 36-75V or 42-53V of input voltage range, 10A of maximum load current range, the realization of primary-side ZVS turn on, and high power-efficiency.

In the section II, the approach of the realization of DC-DC converter operated at MHz level switching frequency is described. In the section III, the issue of the conventional PFM-controlled current-mode resonant DC-DC converter in MHz level operation is revealed. In the section IV, the proposed PWM-controlled current-mode resonant DC-DC converter is explained. In the section V, the experimental results are revealed.

II. The Approach of the Realization of DC-DC Converter Operated at MHz Level Switching Frequency

For miniaturization of the DC-DC converter, the increase in the switching frequency of these converters is considered to be one of key technologies. Therefore, this study challenges 5MHz of switching frequency at 120W of output power. Studies that satisfy both the frequency and the output power have not been challenged so far, as shown in Fig. 1. To suppress increasing core power loss with high switching frequency, NiZn ferrite core is used in the study because this core material is suitable for high frequency operation [5]. In addition, to decrease parasitic inductance, multilayer printed circuit board (PCB) and planar transformer like [6], [7] is adopted.

However, by adopting high switching frequency, power loss such as switching loss and gate driving loss increases dramatically. The switching loss P_{sw} is expressed by

$$P_{sw} = C_{oss} V_{DS}^{\ 2} f_s \qquad (1)$$

where C_{oss} is output capacitance of FET, V_{DS} is drain-to-source voltage of FET, and f_s is switching frequency. The gate driving loss P_d is expressed by

$$P_d = Q_G V_{GS} f_s \qquad (2)$$

where Q_G is gate charge, and V_{GS} is gate-to-source voltage of FET. From eqs. (1) and (2), these power losses are proportional to f_s.

For reducing gate driving loss, GaN-FET is adopted in the study because GaN-FET has low Q_G and be driven at low gate-source voltage. From these reasons, GaN-FET can realize low P_d. Also, another researches have been

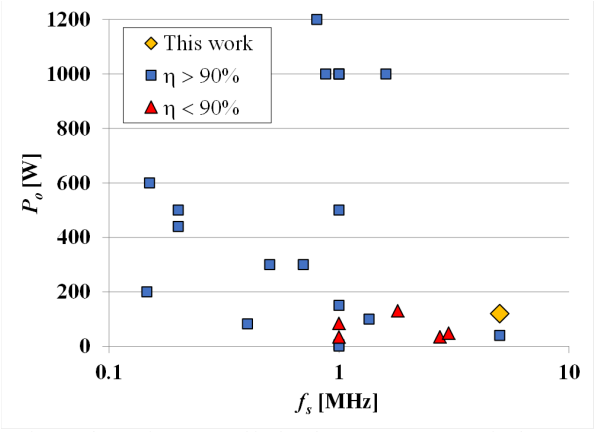


Fig. 1. The performance of isolated DC-DC converters in the previous papers.

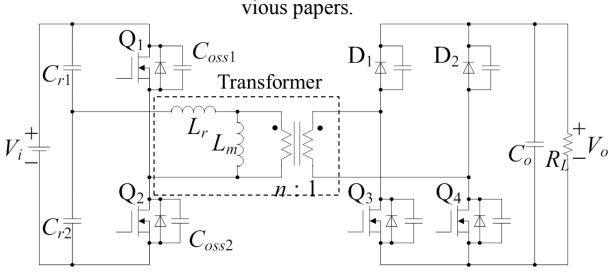


Fig 2. The circuit topology used in the paper.

proved utilizing GaN-FET for high switching frequency DC-DC converter is very practical [8-10]. Some literatures [11-13] prove that GaN devices are more effective than silicon devices.

However, because GaN-FETs have low gate-to-source threshold voltage V_{th}, low maximum gate-to-source voltage V_{GSS}, and high source-to-drain voltage V_{SD}, it is difficult to drive these FETs. Therefore, suitable drive circuit for GaN-FET is needed. Some literatures show that driver LM5113 is suitable for driving GaN-FETs [14], [15].

Furthermore, current-mode resonant DC-DC converter topology featuring primary-side ZVS turn on operation is adopted because switching loss can be suppressed. The circuit topology is shown in Fig. 2.

III. The Issue of The Conventional PFM-controlled Current-Mode Resonant DC-DC Converter in MHz Level Operation

To reduce the switching loss, the current-mode resonant DC-DC converter is widely used. Also, other researches have been proved using current-mode resonant DC-DC converter for high power-efficiency is very practical [16-19]. Generally, the current-mode resonant DC-DC converter is controlled by PFM control which varies switching frequency. PFM control has been valid for the control of the resonant DC-DC converters in kHz level switching operation so far.

To show the static characteristics, the definitions of the converter are

$$M = (2nV_o)/V_i \ , \qquad (3)$$

$$\kappa = L_m / L_r \ , \qquad (4)$$

$$F = f_s / f_0 \ , \qquad (5)$$

$$f_0 = 1/\left(2\pi\sqrt{L_r C_r}\right), \quad (6)$$

$$\omega_0 = 2\pi f_0, \quad (7)$$

$$Q = Z_0 / R_{ac}, \quad (8)$$

$$R_{ac} = \left(8n^2 R_L\right)/\pi^2 \quad (9)$$

and

$$Z_0 = \sqrt{L_r / C_r} \quad (10)$$

where turn ratio n, magnetizing inductance L_m, resonant inductance L_r, switching frequency f_s, resonant capacitance C_r and load resistance R_L.

From literatures, voltage conversion ratio M of PFM-controlled current-mode resonant DC-DC converter is written by

$$M = \frac{1}{\sqrt{\left(1+\frac{1}{\kappa}\left(1-\frac{1}{F^2}\right)\right)^2 + Q^2\left(F-\frac{1}{F}\right)^2}} \quad (11)$$

From eq. (11), the static characteristics of PFM controlled current-mode resonant DC-DC converter can be leaded. Two examples of the static characteristics are shown in Fig. 3. One is V_i = 48V, n = 2.2, L_m = 200nH, L_r = 100nH, C_r = 10nF, Z_0 = 3.16, f_0 = 5.04MHz and κ = 2. The other is V_i = 48V, n = 2.2, L_m = 200nH, L_r = 10nH, C_r = 80nF, Z_0 = 0.354, f_0 = 5.63MHz and κ = 20.

It is assumed that input voltage range is from 42 to 53V at R_L = 1.2Ω and V_o = 12V. In case of L_r = 100nH, for realization of the range, F is changed from 0.81 to 0.99 (f_s is changed from 4.06 to 4.99MHz). In contrast, in case of L_r = 10nH, for realization of the range, F is changed from 0.38 to 0.92 (f_s is changed from 2.16 to 5.17MHz).

The difference between two parameters can be confirmed. If switching frequency changes widely for controlling output voltage, the large noise filter will be needed. Therefore, the DC-DC converter is prevented from downsizing by large noise filter. If switching frequency changes narrow for controlling output voltage, the large resonant inductance is needed for controlling.

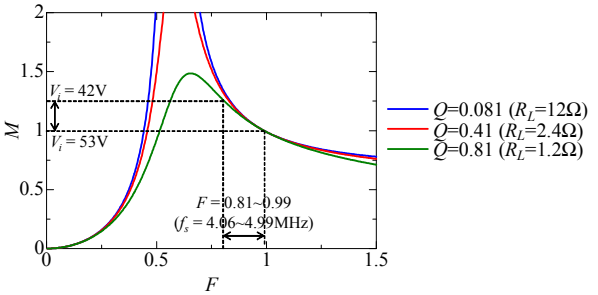
As a result, in MHz level operation for the miniaturization of the DC-DC converter, it is shown that PFM control is hard to be designed.

IV. The Proposed PWM-Controlled Current-Mode Resonant DC-DC Converter

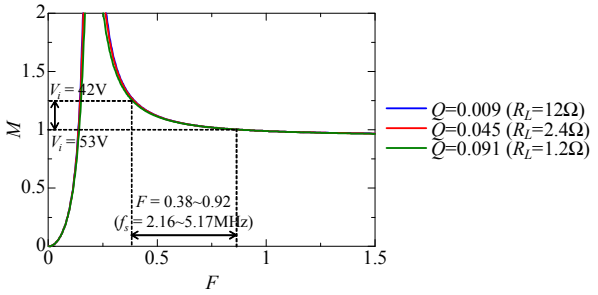
The proposed current-mode resonant DC-DC converter can be controlled at fixed switching frequency. In addition, for controlling output voltage, this method need not any additional components.

A. The Circuit Topology

The circuit topology is based on a half-bridge type current-mode resonant DC-DC converter as shown in Fig. 2. The primary-side is the half-bridge topology. Q_1 and Q_2 are driven in 50% duty ratio, alternatively. C_{oss1} and C_{oss2} are parasitic capacitance of primary-side switches



(a) L_r = 100nH, C_r = 10nF, Z_0 = 3.16.



(b) L_r = 10nH, C_r = 80nF, Z_0 = 0.354.

Fig 3. The static characteristics of LLC resonant DC-DC converter with the conventional PFM control method.

Q_1 and Q_2. C_{r1} and C_{r2} are the resonant capacitors which have same capacitances and also make averaged voltage of v_c to a half of the input. The inside of the broken line is the magnetic transformer which equivalently indicated that L_r is leakage inductance, and L_m is the transformer's magnetizing inductance. The turn ratio is n : 1. L_r is used as the resonant inductance. The secondary-side is the full-bridge topology composed with diodes D_1 and D_2 for high-side arm switches, and transistors Q_3 and Q_4 for low-side arm switches.

B. The Principle of the Proposed PWM Control Method

To simplify analysis of the circuit operation, the following assumptions are made:

- FETs are treated an ideal switch;
- The body diodes of the primary-side FET are neglected;
- The output capacitances of the primary-side FETs are constant during operation, satisfying $C_{oss1} = C_{oss2}$, $C_{oss} = C_{oss1} + C_{oss2}$;
- Resonant capacitances are satisfied $C_{r1} = C_{r2}$, $C_r = C_{r1} + C_{r2}$;
- The forward voltage drop and the parasitic capacitance of the secondary-side diodes are neglected;
- The output capacitance and the body diodes of the secondary-side FETs are neglected;
- The output voltage is constant;

The output voltage can be controlled with changing the duty ratio of Q_3 and Q_4, simultaneously. When the duty ratio is less than 0.5, the circuit is operated as well as conventional current resonance circuit. When the duty ratio is more than 0.5, the circuit is operated in the proposed operation.

The circuit can be separated into 5 states in the proposed operation with the switch combination as shown in TABLE I. The operational waveforms are shown in Fig. 4. The equivalent circuits for each state of a half switching term are shown in Fig. 5. In this figure, the switches drawn with weak colors represent OFF, and red line represents current flow. The definitions of the duty ratio D is followed as

$$D = T_{on}/T_S \ , \tag{12}$$

$$D = 1/2 + D_1 + D_4 + D_5 \ , \tag{13}$$

$$D_1 + D_2 + D_3 + D_4 + D_5 = 1/2 \tag{14}$$

and

$$\begin{cases} D \le 0.5 \cdots\cdots\cdots (\text{conventional operation}) \\ D > 0.5 \cdots\cdots\cdots (\text{proposed operation}) \end{cases} \tag{15}$$

where T_s is the switching period, and T_{on} is the on-term of Q_3 and Q_4. D_1~D_5 are the duty ratio of the each state. The definitions of the resonant are followed;

$$\omega_1 = 1/\sqrt{(L_r + L_m)C_r} \ , \tag{16}$$

$$Z_1 = \sqrt{(L_r + L_m)/C_r} \tag{17}$$

and

$$\omega_{oss} = 1/\sqrt{L_r C_{oss}} \tag{18}$$

The definitions of the initial value of the variable are followed;

$$v_{c1}(0) = V_i/2 - V_c \tag{19}$$

and

$$i_{r1}(0) = I_r \tag{20}$$

The description for each state is described below.

State 1 ($0 < t < D_1 T_s$):

In this state, t_1 is defined as $t_1 = t$. The primary-side switch Q_1 is turned ON. Also, the secondary-side switch-

TABLE I. CIRCUIT OPERATION STATES

State	FET				Diode	
	Q_1	Q_2	Q_3	Q_4	D_1	D_2
State 1	ON	OFF	ON	ON	OFF	OFF
State 2	ON	OFF	ON	OFF	OFF	ON
State 3	ON	OFF	ON	OFF	OFF	OFF
State 4	ON	OFF	ON	ON	OFF	OFF
State 5	OFF	OFF	ON	ON	OFF	OFF

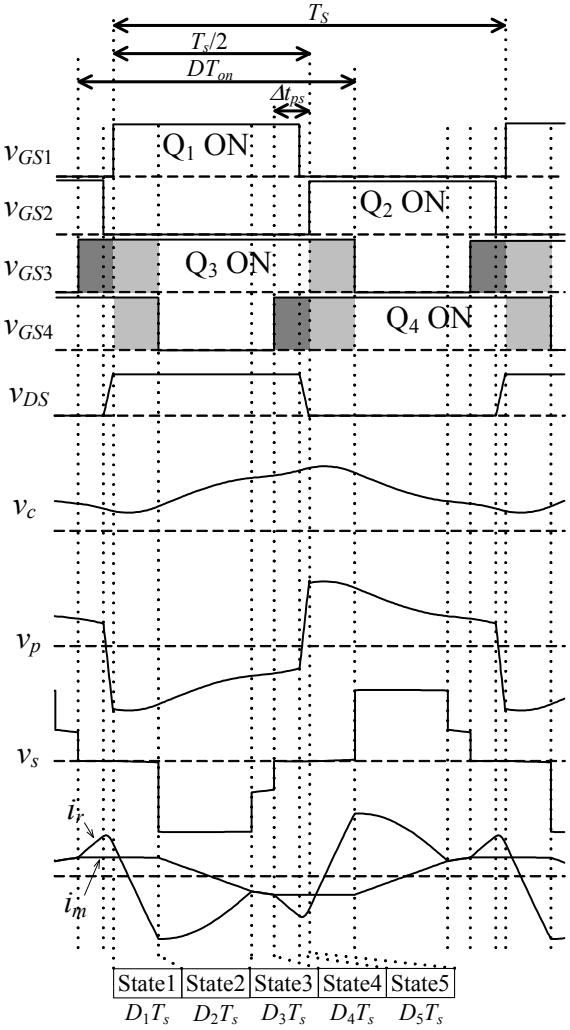
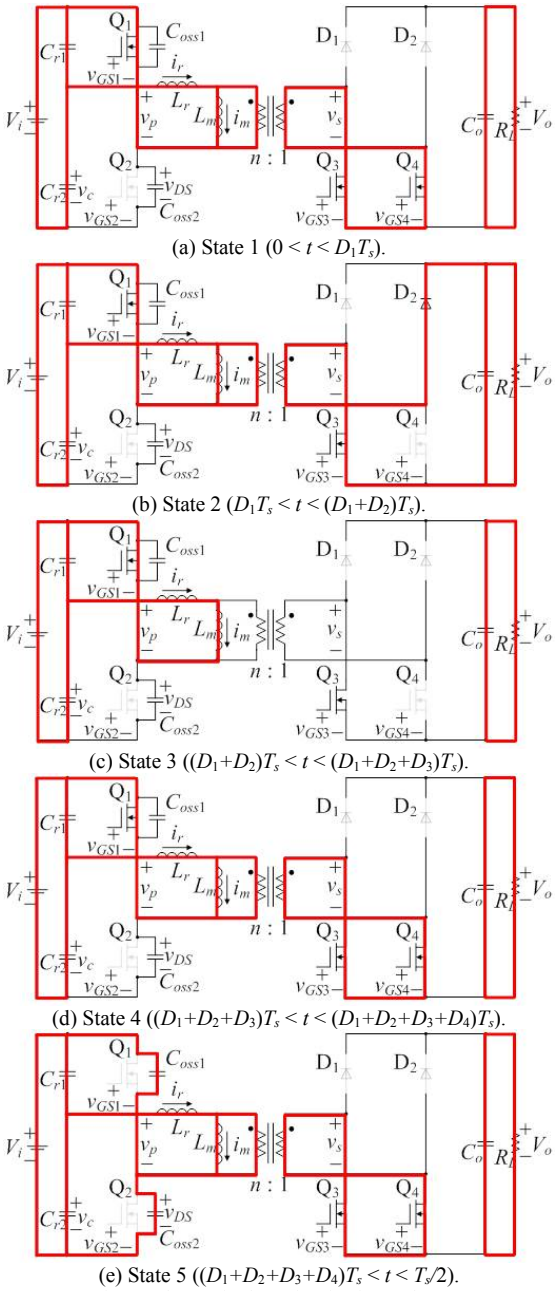


Fig. 4. The operational waveforms of the proposed PWM control.



(a) State 1 ($0 < t < D_1T_s$).

(b) State 2 ($D_1T_s < t < (D_1+D_2)T_s$).

(c) State 3 ($(D_1+D_2)T_s < t < (D_1+D_2+D_3)T_s$).

(d) State 4 ($(D_1+D_2+D_3)T_s < t < (D_1+D_2+D_3+D_4)T_s$).

(e) State 5 ($(D_1+D_2+D_3+D_4)T_s < t < T_s/2$).

Fig. 5. The equivalent circuits for each state of the proposed PWM method.

es both Q_3 and Q_4 are turned ON. Q_3 and Q_4 are overlapped as indicated with the light gray area in Fig. 4. The resonant inductance L_r is magnetized by i_r for boosting output voltage. From the figure, $v_{c1}(t_1)$ and $i_{r1}(t_1)$ are become

$$v_{c1}(t_1) = V_i - \{(V_i/2 + V_c)\cos(\omega_0 t_1) + Z_0 I_r \sin(\omega_0 t_1)\} \quad (21)$$

and

$$i_{r1}(t_1) = -1/Z_0 (V_i/2 + V_c)\sin(\omega_0 t_1) + I_r \cos(\omega_0 t_1). \quad (22)$$

The final values of the state 1 are

$$V_{c2} = v_{c1}(D_1 T_S) \quad (23)$$

and

$$I_{r2} = i_{r1}(D_1 T_S). \quad (24)$$

State 2 ($D_1 T_s < t < (D_1+D_2) T_s$):

In this state, t_2 is defined as $t_2 = t - D_1 T_s$. After Q_4 is turned OFF, the direction of the voltage applied to D_2 is inverted, and diode of D_2 becomes ON. The inductance current which is magnetized in state 1 flow through diode D_2 and switch Q_3, to the load. From the figure, $v_{c2}(t_2)$ and $i_{r2}(t_2)$ are become

$$v_{c2}(t_2) = V_i - nV_o + (V_{c2} - V_i + nV_o)\cos(\omega_0 t_2) - Z_0 I_{r2} \sin(\omega_0 t_2) \quad (25)$$

and

$$i_{r2}(t_2) = 1/Z_0 (V_{c2} - V_i + nV_o)\sin(\omega_0 t_2) + I_{r2} \cos(\omega_0 t_2). \quad (26)$$

The final values of the state 2 are

$$V_{c3} = v_{c2}(D_2 T_S) \quad (27)$$

and

$$I_{r3} = i_{r2}(D_2 T_S). \quad (28)$$

State 3 ($(D_1+D_2) T_s < t < (D_1+D_2+D_3) T_s$):

In this state, t_3 is defined as $t_3 = t - D_1 T_s - D_2 T_s$. The direction of the diode D_2 current is inverted, and diode of D_2 becomes OFF. In the state, resonant current i_r equal to magnetizing current i_m. From the figure, $v_{c3}(t_3)$ and $i_{r3}(t_3)$ are become

$$v_{c3}(t_3) = V_i + (V_{c3} - V_i)\cos(\omega_1 t_3) - Z_1 I_{r3} \sin(\omega_1 t_3) \quad (29)$$

and

$$i_{r3}(t_3) = 1/Z_1 (V_{c3} - V_i)\sin(\omega_1 t_3) + I_{r3} \cos(\omega_1 t_3). \quad (30)$$

The final values of the state 3 are

$$V_{c4} = v_{c3}(D_3 T_S) \quad (31)$$

and

$$I_{r4} = i_{r3}(D_3 T_S). \quad (32)$$

State 4 ($(D_1+D_2+D_3) T_s < t < (D_1+D_2+D_3+D_4) T_s$):

In this state, t_4 is defined as $t_4 = t - D_1 T_s - D_2 T_s - D_3 T_s$. This state is similar to state 1. In the state, the resonant inductance L_r is magnetized by i_r for primary-side ZVS turn on. Q_3 and Q_4 are overlapped as indicated with the dark gray area in Fig. 4. From the figure, $v_{c4}(t_4)$ and $i_{r4}(t_4)$ are become

$$v_{c4}(t_4) = V_i + (V_{c4} - V_i)\cos(\omega_0 t_4) - Z_0 I_{r4} \sin(\omega_0 t_4) \quad (33)$$

and

$$i_{r4}(t_4) = 1/Z_0 (V_{c4} - V_i)\sin(\omega_0 t_4) + I_{r4} \cos(\omega_0 t_4). \quad (34)$$

The final values of the state 4 are

$$V_{c5} = v_{c4}(D_4 T_S) \quad (35)$$

and

$$I_{r5} = i_{r4}(D_4 T_S). \quad (36)$$

State 5 ($(D_1+D_2+D_3+D_4) T_s < t < T_s/2$):

In this state, t_5 is defined as $t_5 = t - D_1 T_s - D_2 T_s - D_3 T_s - D_4 T_s$. The primary-side switch Q_1 is turned OFF. All primary-side switches are turned OFF, called dead-time. The parasitic capacitor C_{oss1} of Q_1 is discharged by a half of resonant inductance current i_r. Q_3 and Q_4 are overlapped as indicated with the dark gray area in Fig. 4. From the figure, $v_{c5}(t_5)$, $v_{DS5}(t_5)$ and $i_{r5}(t_5)$ are become

$$v_{c5}(t_5) = V_{c5} - \frac{\omega_0^2 (V_{c5} - V_i)}{\omega_0^2 + \omega_{oss}^2} + \frac{\omega_0^2 (V_{c5} - V_i)}{\omega_0^2 + \omega_{oss}^2} \cos\left(\sqrt{\omega_0^2 + \omega_{oss}^2} \cdot t_5\right) - \frac{I_{r5}}{C_r \sqrt{\omega_0^2 + \omega_{oss}^2}} \sin\left(\sqrt{\omega_0^2 + \omega_{oss}^2} \cdot t_5\right) \quad (37)$$

$$v_{DS5}(t_5) = \frac{\omega_{oss}^2 (V_{c5} - V_i)}{\omega_0^2 + \omega_{oss}^2} + V_i - \frac{\omega_{oss}^2 (V_{c5} - V_i)}{\omega_0^2 + \omega_{oss}^2} \cos\left(\sqrt{\omega_0^2 + \omega_{oss}^2} \cdot t_5\right) + \frac{I_{r5}}{C_{oss} \sqrt{\omega_0^2 + \omega_{oss}^2}} \sin\left(\sqrt{\omega_0^2 + \omega_{oss}^2} \cdot t_5\right) \quad (38)$$

and

$$i_{r5}(t_5) = \frac{V_{c5} - V_i}{L_r \sqrt{\omega_0^2 + \omega_{oss}^2}} \cdot \sin\left(\sqrt{\omega_0^2 + \omega_{oss}^2} \cdot t_5\right) + I_{r5} \cos\left(\sqrt{\omega_0^2 + \omega_{oss}^2} \cdot t_5\right). \quad (39)$$

C. The Method for Achieving Primary-side ZVS Turn On in the Proposed PWM Control

To accomplish the primary-side ZVS turn on, small magnetizing inductance L_m have been used generally. However, small L_m leads to increase of primary-side current which is cause of reducing power-efficiency. Therefore, to accomplish the ZVS operation in the proposed converter, phase-shift between primary and secondary-side switches which control resonant current is adopted. As shown in Fig. 4, the proposed operation has phase-

shift between primary and secondary-side switches. Δt_{ps} is the time length of the phase-shift. Without the phase-shift, Δt_{ps} = 0ns, the previous state of the dead-time becomes discontinuous current state. With this situation, initial current cannot be charged enough for ZVS because of secondary parasitic capacitance. Therefore, even with the long dead-time term, ZVS cannot be achieved. With the phase-shift, the problem of the initial current can be solved. From eqs. (34) and (36), the initial current of the dead-time, I_{r5} is

$$I_{r5} = 1/Z_0 \left(V_{c4} - V_i\right)\sin\left(\omega_0 D_4 T_S\right) + I_{r4}\cos\left(\omega_0 D_4 T_S\right). \quad (40)$$

The term of the phase-shift becomes

$$\Delta t_{ps} = D_4 T_S + D_5 T_S . \quad (41)$$

In eq. (41), as defined as the $D_5 T_s$ is fixed, the term of state 4 becomes larger with the increase of Δt_{ps}. I_{r5} is related to Δt_{ps} almost linearly. With the enough amount of I_{r5}, the amount of electrical charge q_{r5} which flows resonant inductance in dead-time becomes larger. For an example, in the conditions of C_{oss} = 900pF, V_i = 36V, R_L = 1.5ohm, $D_5 T_s$ = 5ns, the relation of Δt_{ps} and q_{r5} are shown in Fig. 6. The electrical charge q_{r5} can be calculated with

$$q_{r5} = \int_0^{D_5 T_S} i_{r5}(t)dt \quad (42)$$

For achieving ZVS, q_{r5} has to be larger than the amount of the electrical charge of the parasitic capacitance of the switch as

$$|q_{r5}| > q_{oss} \quad (43)$$

where $q_{oss} = C_{oss} V_i$ (44)

From the figure, it can be seen that the phase-shift Δt_{ps} between primary and secondary-side switches are valid for ZVS operation for the proposed PWM control.

D. *The Advantage of the Proposed Method at MHz Level Operation*

Similar to section III, two examples of the static characteristics of the proposed PWM controlled current-mode resonant DC-DC converter are shown in Fig. 7.

It is assumed that input voltage range is from 42 to 53V at R_L = 1.2Ω and V_o = 12V. In case of L_r = 100nH, for realization of the range, D is changed from 0.5 to 0.61. In contrast, in case of L_r = 10nH, for realization of the range, D is changed from 0.5 to 0.55. By comparing between two parameters, the case of L_r = 10nH can control in narrow duty ratio than the other one. Therefore, the proposed PWM control method is seem to be suitable for the miniaturization of the DC-DC converter because the output voltage can be controlled with small resonant inductance.

V. EXPERIMENTAL RESULTS

In this section, it can be confirmed the difference between the experimental results of the proposed method and the targets of the study.

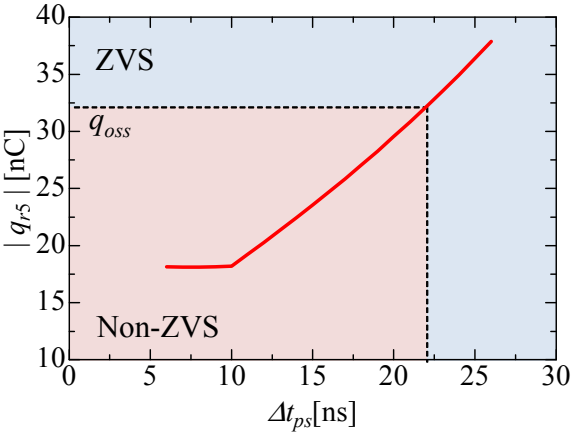
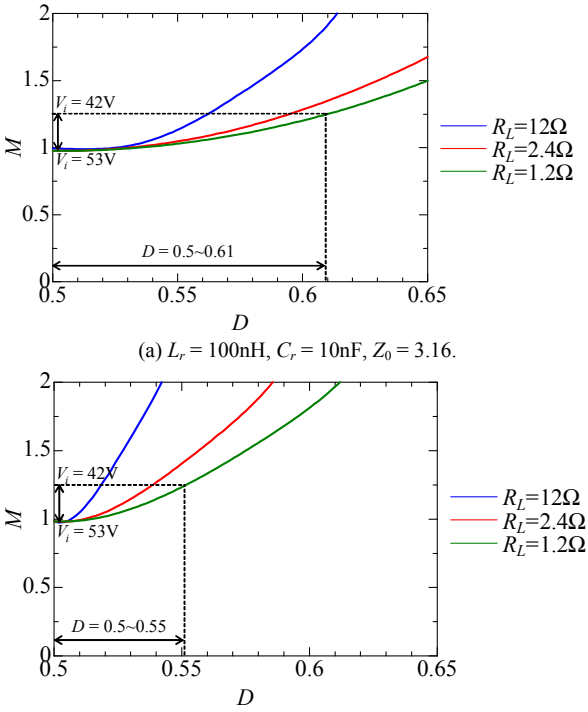


Fig 6. The effect of the phase-shift Δt_{ps} vs $|q_{r5}|$.



(a) L_r = 100nH, C_r = 10nF, Z_0 = 3.16.

(b) L_r = 10nH, C_r = 80nF, Z_0 = 0.354.

Fig 7. The static characteristics of resonant DC-DC converter with the proposed PWM control method.

TABLE II. EXPERIMENTAL PARAMETERS

Specifications	Value
Output reference voltage: V_o	12V
Transformer ratio n : 1	2 : 1
Switching frequency: f_s	5MHz
Resonant frequency: f_r	4.98MHz
Transformer leakage inductance: L_r	33nH
Transformer magnetizing inductance: L_m	200nH
Resonant capacitor: C_{r1},C_{r2}	15.5nF
Output capacitor: C_o	18.8μF

A. *The Experimental Conditions*

As a prototype digital controller, field programmable gate array (FPGA) Cyclone IV is used, which generates individual gate signal for each switch. The on-term of the gate signals are manually changed with software. The resolution of the gate signals is 1nano second.

Some experiments have been carried out with parameters as shown in TABLE II, and 12V of constant out-

put voltage with open loop control. Components used in the experiment are shown in TABLE III.

The main circuit of the proposed PWM-controlled 5MHz DC-DC converter with GaN-FETs is shown in Fig. 8. The total volume of the main circuit of the proposed 5MHz DC-DC converter is 16.14cm^3.

B. The Performance of the Proposed Method

The open loop static characteristics of the 5MHz PWM-controlled DC-DC converter are exhibited as shown in Fig. 9. From the figure, it can be seen that voltage transfer ratio M is controlled by duty ratio D, and input voltage range can be achieved 36-44V. The difference between the performance of the proposed method and the targets can be confirmed. The reason is that the ideal transformer turn ratio n is 2.2, however, the actual n is 2. Planar transformer cannot be changed n easily because the winding is incorporate into the substrate.

The waveforms of I_o = 0.89A and I_o = 6.3A with the phase-shift are shown in Fig. 10. The blue bar of dead-time shows achieving primary-side ZVS turn on and Δt_{ps} is effective for primary-side ZVS operation.

The power-efficiency of the DC-DC converter at V_o= 12V is shown in Fig. 11. The maximum power-efficiency is 89.4%, and maximum load current is 8A at V_i = 44V. Also, at low input voltage 44V or 36V, it can be seen that the power-efficiency is relatively low, and maximum load current is low. The reason is that large duty ratio is needed at low input voltage and large output current. The large duty ratio leads to large peak current which is cause of power dissipation. ZVS operation has been confirmed in the range of the experimental conditions.

The temperature distribution of the DC-DC converter as shown in Fig. 12, has been taken of the breadboard at V_i = 44V and I_o = 8A. From the results, the temperature of the secondary-side is still in high level. The reason is that large duty ratio leads to the hard-switching of secondary-side switches, and large conduction loss of diodes is happened. On the other hand, the primary-side temperature is relatively low because of achieving ZVS turn on. Therefore, in the future, the hard-switching of secondary-side switches will be improved.

TABLE III. EXPERIMENTAL COMPONENTS

Name	Manufacture	Part Name/ Material
Primary side GaN-FET	EPC	EPC2001
Secondary side GaN-FET	EPC	EPC2015
FET Driver	TEXAS INSTRUMENTS	LM5113
Diode	DIODES	PDS1040L
Transformer Core Material	TDK	NiZn Ferrite Core
Resonant Capacitor	TDK	C1608C0G1H392J
Input Capacitor	TDK	C3216X7R1H105K
Output Capacitor	TDK	C2012X7R1E475M
FPGA	Terasic (ALTERA)	DE0-nano (Cyclone IV)
Isolator	TEXAS INSTRUMENTS	ISO722

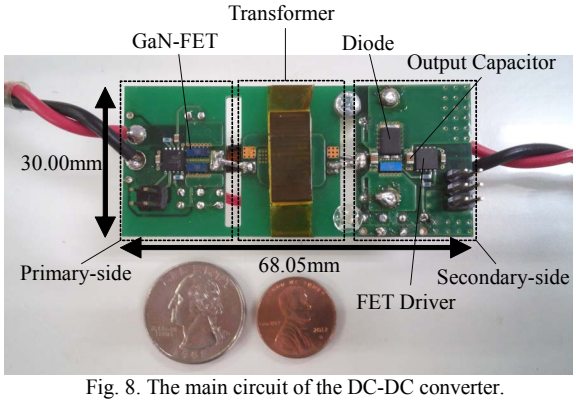


Fig. 8. The main circuit of the DC-DC converter.

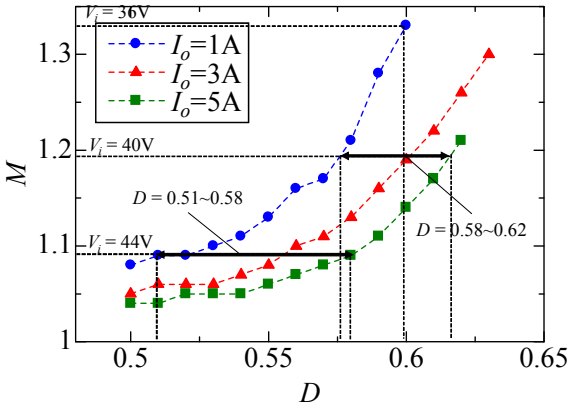
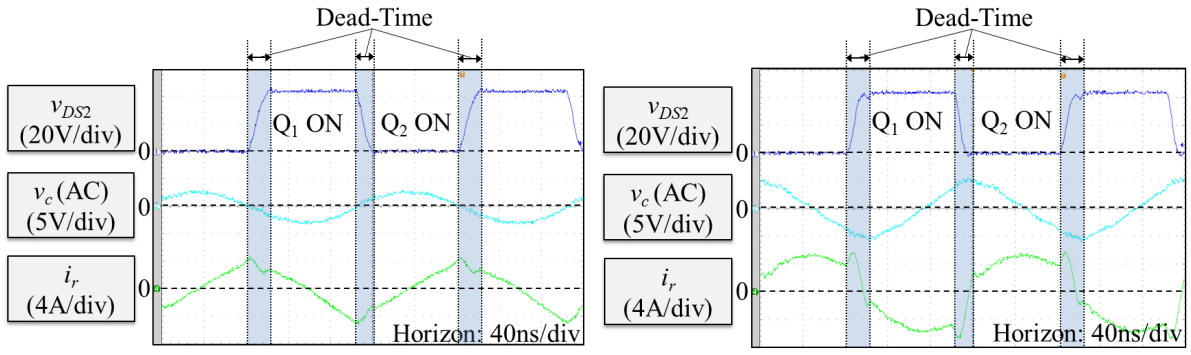


Fig. 9. The open loop static characteristics of resonant DC-DC converter with the proposed PWM control method.



(a) V_i = 44V, V_o = 12V, I_o = 0.89A, D = 0.53, Δt_{ps} = 3ns. (a) V_i = 44V, V_o = 12V, I_o = 6.3A, D = 0.6, Δt_{ps} = 13ns.

Fig. 10. Experimental waveforms of resonant DC-DC converter with the proposed PWM control method.

VI. CONCLUSIONS

In this paper, the method of the realization of a MHz level switching frequency DC-DC converter for high power-density is described. Furthermore, the novel PWM control method and achieving ZVS operation method for the current-mode resonant DC-DC converter in MHz level operation has been proposed.

The targets of the study is to obtain the high performance which is the small volume, 36-75V or 42-53V of input voltage range, 10A of maximum load current range, the realization of primary-side ZVS turn on, and high power-efficiency.

Some experiments have been done with 5MHz isolated DC-DC converter which has GaN-FET, and the total volume of the circuit is 16.14cm^3. With the proposed PWM control method, input voltage range is 36-44V, and maximum load current range is 8A at 44V. The primary-side ZVS turn on is confirmed, and the maximum power-efficiency is 89.4%.

As the future work, to accomplish the targets of the study, detailed analysis of the proposed method with phase-shift, realization of the wide control range and feedback control by digital controller are under considerations.

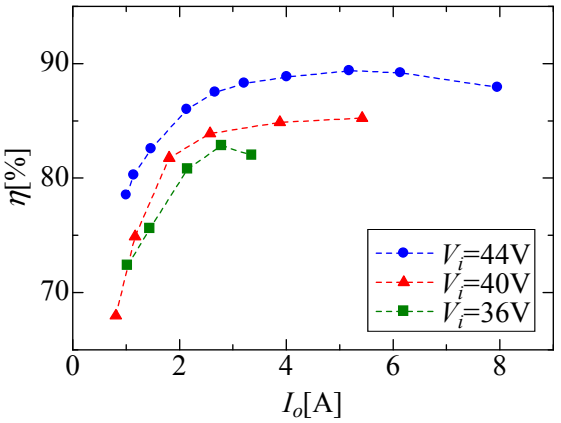


Fig. 11. The power-efficiency of resonant DC-DC converter with the proposed PWM control method at V_o = 12V.

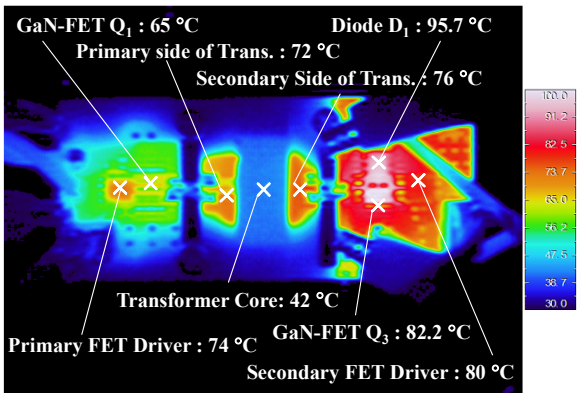


Fig. 12. The temperature distribution of resonant DC-DC converter with the proposed PWM control method at V_i = 44V, V_o = 12V, I_o = 8A.

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