A Static Characteristic Analysis of Proposed Bi-Directional Dual Active Bridge DC-DC Converter

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Abstract- **Recently, the power supply network with energy storage devices such as battery has been focused. This network topology uses bi-directional isolated DC-DC converter of low or medium capacity is required for the diversification of power supply network. The dual active bridge (DAB) DC-DC converter is one of the effective bi-directional isolated DC-DC converters. However, the circuit has some instinct problems such as degradation of power efficiency and the occurrence of the surge in light-load operation. In this paper, we have been done a static characteristic analysis and highly power-efficient technique for DAB DC-DC Converter at light load. Also the analysis results and the proposed technique are verified with some experimental results.**

I. INTRODUCTION

Recently, the bidirectional dc-dc converter has been focused on because of the huge demand for diversification of power supply network including battery. The DAB dc-dc converter is one of the most popular circuits for bidirectional applications because of its simple structure. Some examples are for UPS [1], for automotive [2]-[4] and for energy storage system [5]. The one of the feature is achieving zero volt switching (ZVS) in natural operation. However, hard switching and/or power efficiency at light load condition is the intrinsic problem [6]. Some research have been done to solve the problem, for instance, use of resonant type converter with snubber circuit [7], silicon carbide (SiC) power device and new magnetic materials [8], and Quasi-ZCS operation with LC filter [9]. Furthermore by applying switching modulation, DAB converter works in wide range of input voltage and load condition [10]-[12]. These objectives of switching modulation controls are to regulate voltage and satisfy load variation [10], to expand soft switching region [11], and minimize the total power losses [12]. However, the problem of switching surges reduction was not addressed. In [13], the novel switching surge reduction technique is proposed and confirmed with some analysis and experimental results. And also, the results of power efficiency improvement of the light load were described.

In this paper, the detailed analysis of the technique is described and confirmed with some experiments.

II. CONVENTIONAL OPERATION OF A DAB DC-DC CONVERTER

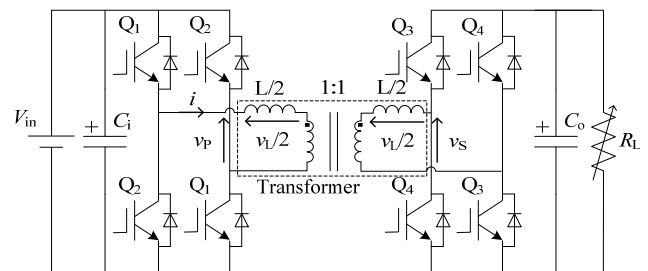Fig. 1 shows the circuit schematic of the basic DAB dc-dc

Fig. 1. The circuit schematic of DAB dc-dc converter.

(a) Light load   (b) Heavy load

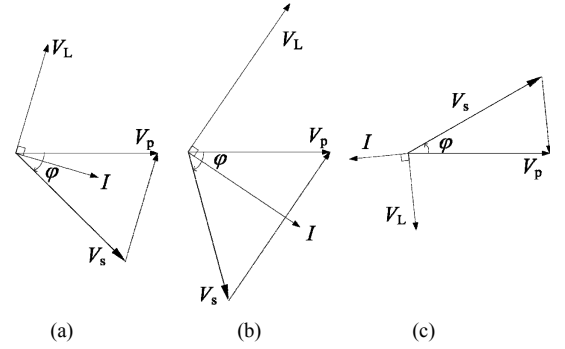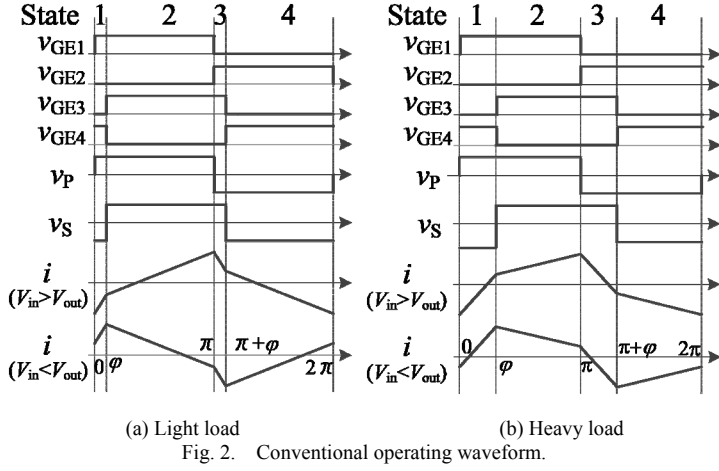Fig. 2.　Conventional operating waveform.

Fig. 3.　Phasor diagram [13]: (a) Forward power flow mode (light load); (b) Forward power flow mode (heavy load); (c) Reverse power flow mode.

converter. Fig. 2 shows the operating waveforms with the conventional operation [14]. In the conventional operation, the output power is operated by the phase-shift shown as φ between the primary voltage v_P and secondary voltage v_S of transformer. Fig. 3 shows the phasor diagram. V_P, V_S, V_L, and I are phasor symbols for v_P, v_S, v_L, i, respectively. When V_S is lagging V_P in forward power flow mode (Fig. 3 (a) and (b)), and when V_S is leading V_P, it is operated in reverse power flow mode (Fig. 3 (c)).

The output power P_o can be obtained as

$$P_o = \frac{V_{in}V_{out}}{\omega L} \varphi (1 - \frac{\varphi}{\pi}).$$ (1)

The output power can be controlled with the phase difference φ. The waveform of the current i is changed by the load condition. In this paper, current i crossed the zero line in the state 2 is defined as a light load, and current i crossed the zero line in the state 1 is defined as a heavy load as shown in Fig. 2.

III. INTRINSIC SURGES PROBLEM OF A DAB DC-DC CONVERTER

As mentioned in above, well known problem of a DAB DC-DC converter is hard switching in the light condition. However, previous researches haven't been addressed about the switching surges problem. It is caused by the reverse recovery effect of the diode. Fig. 4 shows φ - P_o. The switching surges occur at light load range of this figure.

Fig. 5 shows the generation mechanism of switching surges when $V_{in} > V_{out}$. The surges voltage occurs in the transition from State 1 (3) to State 2 (4), repeatedly. C_d is the parasitic capacitance of diode which is connected in parallel with the ideal diode, and L_{wire} is parasitic reactance. At the light load condition, the diodes D_4 is conducting in state 1. Then the switches Q_3 is turned on when state changes from State 1 to State 2. At this instantaneous moment, the diode D_4 is switched from a forward bias condition to a reverse bias condition, immediately. And the switching surges are
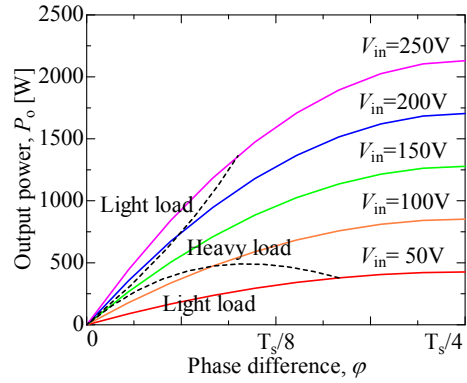

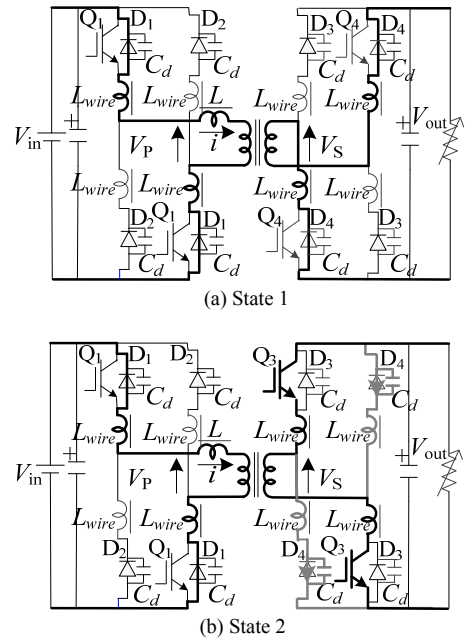Fig. 4.　φ - P_o (V_{in}=150V) [13].

(a) State 1

(b) State 2

Fig. 5.　The generation mechanism of switching surge ($V_{in} > V_{out}$).
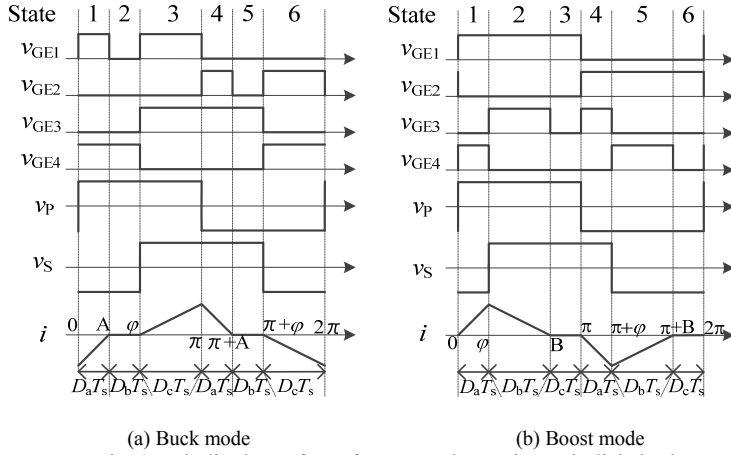
(a) Buck mode   (b) Boost mode

Fig. 6. Idealized waveforms for proposed operating at the light load.

occurred with the resonance of C_d and L_{wire} due to reverse recovery phenomenon. With the same reason, when $V_{in} < V_{out}$, the surges occurs in the transition from State 2 (4) to State 3 (1) on the primary side.

Commonly, to protect the switches from the switching surges, snubber circuit are applied. However, the power loss at the snubber circuit can't be ignored at the light load condition. The other way, the resonant converter type is also popular, but the additional components are needed [9].

IV. PROPOSED OPERATION METHOD

We have proposed the software-based compensation method for basic DAB dc-dc converter topology. It can be reduce the switching surges at the light load, without any of additional circuits such as the snubber circuits or resonant circuits [13]. Fig. 6 shows idealized waveform of the proposed operating method. When $V_{in} < V_{out}$, as it can be seen from the waveforms, the direction of primary side current of transformer i during each on-time of Q_1 and Q_2 is restricted to avoid the crossing the zero line. Due to the restriction, the zero-current-switching can be realized for Q_1 and Q_2, respectively. The ideal static analysis has been done as follows. This converter has six operational states in one switching period for each of the buck and boost mode operation, respectively. The each element is treated as ideal in equivalent circuit.

The detailed description of the ideal circuit is revealed in a previous paper [13]. Therefore, only the results are shown in this paper.
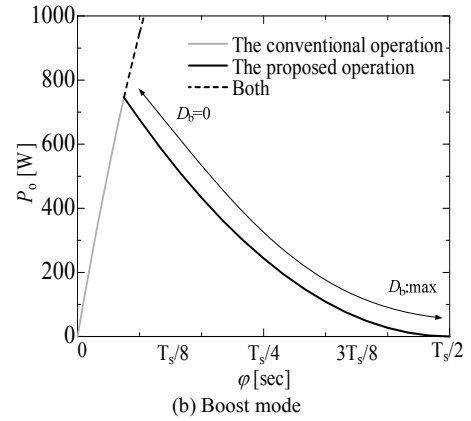
A. Buck Mode Operation in Light Load

In buck mode, the primary side switches Q_1 and Q_2 are turned-on twice in the period. Firstly, Q_1 and Q_2 are turn-on at $t = 0$ and $T_s/2$. Secondly, they are turn-off at $t = A$ and $T_s/2 + A$. Thirdly, they are turn-on at $t = \varphi$ and $T_s/2 + \varphi$. Fourthly, they are turn-off at $t = T_s/2$ and T_s.

A is calculated as

$$A = \frac{V_{in} - V_{out}}{V_{in} + V_{out}}(\frac{1}{2}T_s - \varphi). \qquad (2)$$
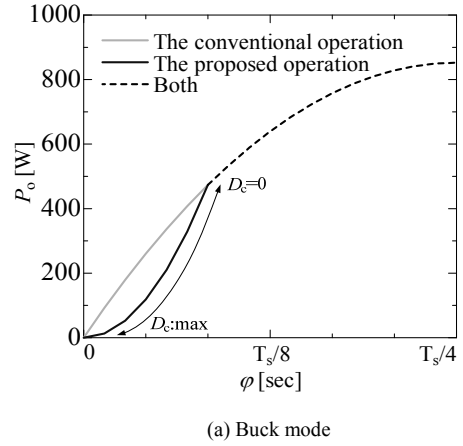
(a) Buck mode

(b) Boost mode

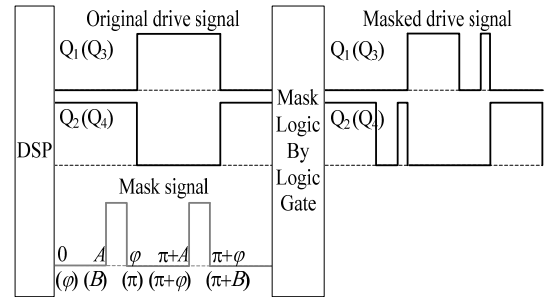Fig. 7. $\varphi - P_o$ (conventional operation and proposed operation).
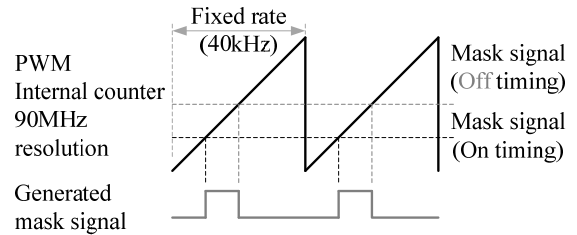

Fig.8. Masked drive signal generating mechanism.

Fig. 9. Mask signal generating mechanism of PWM in DSP.

B. Boost Mode Operation in Light Load

In boost mode, the secondary side switches Q_3 and Q_4 are turned-on twice in the period. Firstly, Q_3 and Q_4 are turn-on at $t = \varphi$ and $T_s/2 + \varphi$, respectively. Secondly, they are turn-off at $t = B$ and $T_s/2 + B$. Thirdly, they are turn-on at $t = T_s/2$ and 0. Fourthly, they are turn-off at $t = T_s/2 + \varphi$ and φ.

B is calculated as

$$B = \frac{2V_{out}}{V_{out} - V_{in}}\varphi. \tag{3}$$

C. Output Power Control in Light Load

The ideal analysis for both of buck and boost mode operation can be done for power. For the ideal analysis result, the output power P_o can be obtained as

$$P_o = \frac{2X^2}{T_s L} \cdot \left| \frac{V_{in} + V_{out}}{V_{in} - V_{out}} \right| \cdot V_{in}V_{out}. \tag{4}$$

In buck mode, $X = A$, and in boost mode, $X = \varphi$.

D. Output Power Control in Heavy Load

In the light load, with the output power increasing, the periods of which all switches turned OFF ($A \sim \varphi$, $\pi + A \sim \pi + \varphi$, $B \sim \pi$, $\pi + B \sim 2\pi$) becomes shorter. A equal to φ or B equal to π is the boundary between light load and heavy load. Therefore, in the heavy load condition, the only conventional phase-shift operation is active. From the results, it can be seen that it is possible to control the output power seamlessly despite of the load condition. Relationship φ and P_o of conventional and proposed operation is shown in Fig. 7.

E. Pulse Generating Method

Fig. 8 and Fig. 9 show the generating mechanism of proposed driving signal. As mentioned above, the gate signal is the combination of the phase shift signal and the masked signal. The mask width is calculated and controlled by (2) and (3), respectively.

V. LOSS INCLUDED ANALYSIS OF CONVENTIONAL OPERATION

Equation of the output power (1) was equation for the ideal state without consideration of the conduction loss of the body diode and switch and the parasitic resistance of the transformer. This chapter will be described analysis of static characteristics in consideration of these losses. In order to analyze and make some definitions, in the operation waveform of Figure 2, both of light load and heavy load can be divided into four states. Since the basic operation of two half cycles are symmetric, only the first half cycle is explained. To analyze the characteristics of the circuit, Extended State-Space Averaging Method [16] is applied.

In order to simplify the loss analysis, loss is defined as r_{loss}. Equivalent circuits corresponding to each state in buck mode operation are shown in Fig.9, where $\hat{v}_o$ is the low-frequency component of V_o.

For analysis, solving for i_L and i_c,

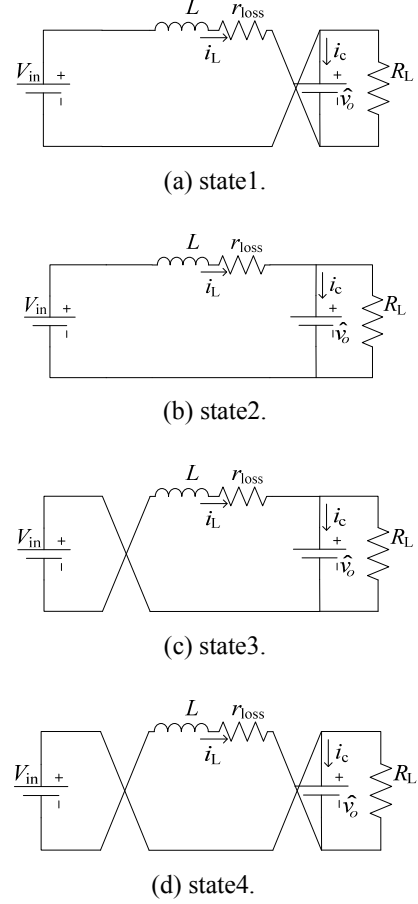
(a) state1.

(b) state2.

(c) state3.

(d) state4.

Figure 9. Equivalent circuit :
(a) state 1; (b) state 2; (c) state 3; (d) state 4;

for $0 \le t \le DT_s$ (state 1)

In Fig. 9(a), Voltage law of the circuit is

$$L \frac{di_{L1}(t)}{dt} = V_{in} + \hat{v}_{out} - i_{L1}(t)r_{loss} \cdot \tag{5}$$

Integration of eq.(5) is

$$L \cdot i_{L1}(t) = \int (V_i + v_o)dt - r_{loss}\int i_{L1}(t)dt + C . \tag{6}$$

Linear approximation of eq.(6) is

$$\int i_{L1}(t)dt = \frac{1}{2}\{i_{L1}(0) + i_{L1}(t)\}t . \tag{7}$$

Using eq.(5) and (6),

$$i_{L1}(t) \approx \frac{2(V_i + v_o)t}{2L + r_{loss}t} + \frac{2L - r_{loss}t}{2L + r_{loss}t} \cdot i_{L1}(0). \tag{8}$$

In addition, the current law is expressed as

$$i_{c1}(t) = -i_{L1}(t) - \frac{\hat{v}_{out}}{R_L} \cdot \tag{9}$$

for $DT_s \le t \le \pi$ (state 2)

Solving for current law and voltage law of circuit in the same way

$$i_{L2}(t) \approx \frac{2(V_i - v_o)(t - DT_s)}{2L + r_{loss}(t - DT_s)} \cdot$$
$$+ \frac{2L - r_{loss}(t - DT_s)}{2L + r_{loss}(t - DT_s)} \cdot \left\{ \frac{2(V_i + v_o)DT_s}{2L + r_{loss}DT_s} + \frac{2L - r_{loss}DT_s}{2L + r_{loss}DT_s} i_{L1}(0) \right\} \quad (10)$$

$$i_{c2}(t) = i_{L2}(t) - \frac{\hat{v}_{out}}{R_L} \cdot \quad (11)$$

In one cycle in the steady state, the current flowing through the leakage inductance is positive and negative symmetry operation. The operation of the state3 and State4 is equivalent to positive and negative symmetry to the operation of the state1 and state2 Therefore, the analysis was performed only for half cycle.

Since the conventional operation of two half cycles are symmetric,

$$i_{L1}(0) = -i_{L2}\left(\frac{1}{2}T_s\right) \cdot \quad (12)$$

It is possible to determine the initial value of the circuit using the eq. (12).

$$i_{L1}(0) \approx -\frac{2(V_i - v_o) \cdot (2L + r_{loss} \cdot DT_s)(1 - 2D)T_s + 2(V_i + v_o)\{4L - r_{loss} \cdot (1 - 2D)T_s\} \cdot DT_s}{\{4L + r_{loss} \cdot (1 - 2D)T_s\}(2L + r_{loss} \cdot DT_s) + \{4L - r_{loss} \cdot (1 - 2D)T_s\}(2L - r_{loss} \cdot DT_s)} \quad (13)$$

Next, deriving for the average current in the output capacitor of the state1 and state2.The average value of v in each state is calculated with

$$i_{c1\_ave} \approx -\frac{(V_i + v_o) \cdot D^2 T_s^2}{2L + r_{loss} \cdot DT_s} + \left(1 + \frac{2L - r_{loss} \cdot DT_s}{2L + r_{loss} \cdot DT_s}\right) \cdot$$
$$\frac{(V_i - v_o) \cdot (2L + r_{loss} \cdot DT_s)(1 - 2D)DT_s^2 + (V_i + v_o)\{4L - r_{loss} \cdot (1 - 2D)T_s\} \cdot D^2 T_s^2}{\{4L + r_{loss} \cdot (1 - 2D)T_s\}(2L + r_{loss} \cdot DT_s) + \{4L - r_{loss} \cdot (1 - 2D)T_s\}(2L - r_{loss} \cdot DT_s)}$$
$$-\frac{\hat{v}_o}{R_L} \cdot DT_s \quad (14)$$

$$i_{c2\_ave} \approx \frac{1}{2}\frac{(V_i - v_o)(1 - 2D)^2 T_s^2}{4L + r_{loss}(1 - 2D)T_s} + \frac{1}{2}\frac{(V_i + v_o) \cdot (1 - 2D)DT_s^2}{2L + r_{loss} \cdot DT_s}\left[1 + \frac{4L - r_{loss}(1 - 2D)T_s}{4L + r_{loss}(1 - 2D)T_s}\right]$$
$$-\frac{1}{2}\left[1 + \frac{4L - r_{loss}(1 - 2D)T_s}{4L + r_{loss}(1 - 2D)T_s}\right]\frac{2L - r_{loss} \cdot DT_s}{2L + r_{loss} \cdot DT_s} \cdot$$
$$\frac{(V_i - v_o) \cdot (2L + r_{loss} \cdot DT_s)(1 - 2D)^2 T_s^2 + (V_i + v_o)\{4L - r_{loss} \cdot (1 - 2D)T_s\} \cdot (1 - 2D)DT_s^2}{\{4L + r_{loss} \cdot (1 - 2D)T_s\}(2L + r_{loss} \cdot DT_s) + \{4L - r_{loss} \cdot (1 - 2D)T_s\}(2L - r_{loss} \cdot DT_s)} - \frac{\hat{v}_o}{R_L} \cdot \frac{1 - 2D}{2}T_s \quad (15)$$

while $\alpha = 2\omega L + r_{loss}\varphi$, $\beta = 2\omega L - r_{loss}\varphi$, $\gamma = 4\omega L + 2r_{loss}(\pi - \varphi)$ and $\lambda = 4\omega L - 2r_{loss}(\pi - \varphi) \cdot$

The results of static characteristics are obtained by letting $d\hat{v}_o / dt = 0$ (therefore $\overline{i_{c_o}} = C d\hat{v}_o / dt = 0$).

The output power Po is

$$P_o \approx V_i V_o \varphi \left(1 - \frac{\varphi}{\pi}\right) \left[\begin{array}{l} \frac{1}{\pi - \varphi}\left(1 + \frac{V_o}{V_i}\right)\left[\frac{\varphi\lambda}{\alpha\gamma + \beta\lambda} + \left(1 - \frac{\beta\lambda}{\alpha\gamma + \beta\lambda}\right)\left\{\frac{\lambda}{\alpha\gamma}(\pi - \varphi) + \frac{1}{\alpha}(\pi - 2\varphi)\right\}\right] \\ + \left(1 - \frac{V_o}{V_i}\right)\left[\frac{8\omega L}{\alpha\gamma + \beta\lambda} + \frac{2\pi}{\varphi}\left\{\frac{1}{\gamma}\left(1 - \frac{\beta\lambda}{\alpha\gamma + \beta\lambda}\right) - \frac{\beta}{\alpha\gamma + \beta\lambda}\right\}\left(1 - \frac{\varphi}{\pi}\right)\right] \end{array} \right] \cdot \quad (16)$$

When the $r_{loss} = 0$ in equation (16), is found to be obtained the same equation as the equation (1). Fig.10 shows the characteristics of changing the value of r_{loss}. We can see the effect of r_{loss} on the output power Po by Fig.10.

VI. LOSS INCLUDED ANALYSIS OF PROPOSED OPERATION

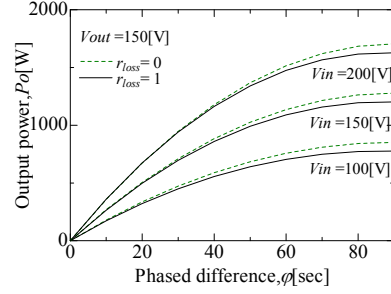To analyze the characteristics of the circuit, Extended

Figure 10. φ - Po
(conventional analysis and proposed analysis).
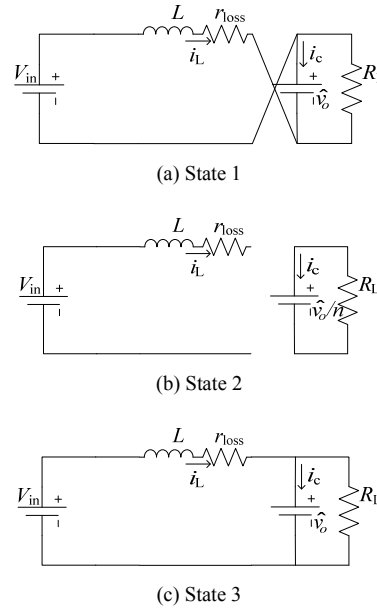

(a) State 1

(b) State 2

(c) State 3

Fig. 11. Equivalent circuit of buck mode operation.

State-Space Averaging Method [16] is applied again.

The analysis has been done for each of buck mode and boost mode operation, respectively. In order to simplify the loss analysis, loss is defined as r_{loss}.

A. Buck Mode Operation

Equivalent circuits corresponding to each state in buck mode operation are shown in Fig. 11, where $\hat{v}_o$ is the low-frequency component of V_o. $D_a = (A - 0)/T_s$, $D_b = (\varphi - A)/T_s$, $D_c = (\pi - \varphi)/T_s$ in Fig. 6 (a). For ease of analysis, the calculation has been performed in a half of the switching period because of the symmetric behavior of the circuit topology.

For analysis, solving for i_L and i_c,
for $0 \le t \le A$ (state 1)

$$i_L \approx \frac{2(V_{in} + \hat{v}_o)t}{2L + r_{loss}t} - \frac{2L - r_{loss}t}{2L + r_{loss}t}i_L(0) \quad (17)$$

$$i_{C_o} = -i_L - \frac{\hat{v}_o}{R_L} \tag{18}$$

for $A \leq t \leq \varphi$ (state 2)

$$i_L = 0 \tag{19}$$

$$i_{C_o} = -i_L - \frac{\hat{v}_o}{R_L} \tag{20}$$

for $\varphi \leq t \leq \pi$ (state 3)

$$i_L \approx \frac{2(V_{in} - \hat{v}_o)\{t - (D_a + D_b)T_s\}}{2L + r_{loss}\{t - (D_a + D_b)T_s\}} \tag{21}$$

$$i_{C_o} = i_L - \frac{\hat{v}_o}{R_L}. \tag{22}$$

From Fig. 6, it is clear that $D_a + D_b + D_c = 1/2$, $i_L(0) = -i_L(\pi)$ and $i_L(A) = 0$. Using the preceding relationships,

$$i_L(0) = -i_L(\pi) = -\frac{2(V_{in} + \hat{v}_o)D_aT_s}{2L - r_{loss}D_aT_s} \tag{23}$$

and

$$D_c = \frac{V_{in} + \hat{v}_o}{V_{in} - \hat{v}_o - 2D_aT_sV_{in}r_{loss}/L}D_a. \tag{24}$$

The average value of i in each state is calculated with

$$i_{c_o\_ave1} = -\frac{1}{2}\frac{2(V_{in} + \hat{v}_o)D_aT_s}{2L - r_{loss}D_aT_s} - \frac{\hat{v}_o}{R_L} \tag{25}$$

$$i_{c_o\_ave2} = -\frac{\hat{v}_o}{R_L} \tag{26}$$

$$i_{c_o\_ave3} = -\frac{1}{2}\frac{2(V_{in} + \hat{v}_o)D_aT_s}{2L - r_{loss}D_aT_s} - \frac{\hat{v}_o}{R_L}. \tag{27}$$

Hence,

$$\overline{i_{c_o}} = 2(i_{c_o\_ave1} \times D_a + i_{c_o\_ave2} \times D_b + i_{c_o\_ave3} \times D_c)$$
$$= \frac{2D_a^2T_s}{L} \cdot \frac{V_{in}\hat{v}_o(V_{in} + \hat{v}_o)}{V_{in} - \hat{v}_o - V_{in}D_aT_sr_{loss}/L} - \frac{\hat{v}_o}{R_L}. \tag{28}$$

The results of static characteristics are obtained by letting $d\hat{v}_o/dt = 0$. And using $D_aT_s = A$,

$$P_o = \frac{2A^2}{T_sL} \cdot \frac{V_{in}V_{out}(V_{in} + V_{out})}{V_{in} - V_{out} - V_{in}D_aT_sr_{loss}/L} \tag{31}$$

where

$$A = \frac{(V_{in} - V_{out})(T_s/2 - \varphi)}{V_{in} + V_{out} + V_{in}(T_s/2 - \varphi)r_{loss}/L}. \tag{32}$$
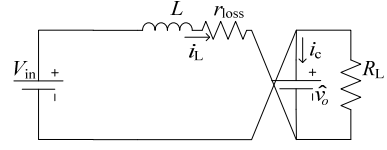
B. Boost Mode Operation

Equivalent circuits corresponding to each state in boost mode operation are shown in Fig. 12. For analysis, equation is formularized for each state. $D_a = (\varphi - 0)/T_s$, $D_b = (B - \varphi)/T_s$ and $D_c = (\varphi - B)/T_s$ in Fig. 6 (b).
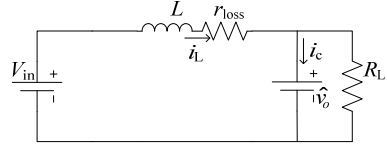
For $0 \leq t \leq \varphi$ (state 1)

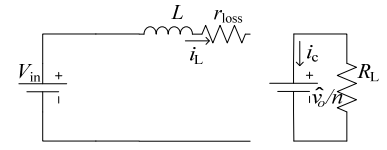$$i_L \approx \frac{2(V_{in} + \hat{v}_0)t}{2L + r_{loss}t} \tag{33}$$

$$i_{C_o} = -i_L - \frac{\hat{v}_o}{R_L} \tag{34}$$

(a) State 1

(b) State 2

(c) State 3

Fig. 12. Equivalent circuit of boost mode operation.

for $\varphi \leq t \leq B$ (state 2)

$$i_L \approx \frac{2(V_{in} - \hat{v}_0)(t - D_aT_s)}{L + r_{loss}(t - D_aT_s)} + \frac{2L - r_{loss}(t - D_aT_s)}{2L + r_{loss}(t - D_aT_s)}i(D_aT_s) \tag{35}$$

$$i_{C_o} = i_L - \frac{\hat{v}_o}{R_L} \tag{36}$$

for $B \leq t \leq \pi$ (state 3)

$$i_L = 0 \tag{37}$$

$$i_{C_o} = -\frac{\hat{v}_o}{R_L}. \tag{38}$$

From Fig. 6, it is clear that $D_a + D_b + D_c = 1/2$, and $i_L(B) = 0$. Using the preceding relationships

$$D_b = -\frac{(V_{in} + \hat{v}_o)}{(V_{in} - \hat{v}_o) - \hat{v}_oD_aT_sr_{loss}/L}D_a. \tag{39}$$

Hence,

$$\overline{i_{c_o}} = -\frac{2D_a^2T_s}{L}\frac{(V_{out} + V_{in})(2V_{in}V_{out} - V_{out}^2D_aT_sr_{loss}/2L)}{(V_{out} - V_{in} + V_{out}r_{loss}D_aT/L)(2 + D_aT_sr_{loss}/L)} - \frac{\hat{v}_o}{R_L}. \tag{40}$$

The results of static characteristics are obtained by letting $d\hat{v}_o/dt = 0$, therefore

$$P_o = \frac{2(D_aT_s)^2}{T_sL}\frac{(V_{out} + V_{in})(2V_{in}V_{out} - V_{out}^2D_aT_sr_{loss}/2L)}{(V_{out} - V_{in} + V_{out}r_{loss}D_aT/L)(2 + D_aT_sr_{loss}/L)}. \tag{41}$$

Using $D_aT_s = \varphi$

$$P_o = \frac{2\varphi^2}{T_sL}\frac{(V_{out} + V_{in})}{(V_{out} - V_{in} + V_{out}r_{loss}\varphi/L)}\frac{(2V_{in}V_{out} - V_{out}^2\varphi r_{loss}/2L)}{(2 + \varphi_sr_{loss}/L)}. \tag{42}$$

B is calculated as

$$B = (D_a + D_b)T_s = \frac{v_o(2 + r_{loss}D_aT/L)}{(v_o - v_i) + v_or_{loss}D_aT/L}\varphi \tag{43}$$

VII. EXPERIMENTAL RESULTS

In order to select the value of r_{loss}, we perform some experiments with the prototype circuit. The main circuit is DAB dc-dc converter without additional circuits like snubber circuit. We had closed-loop-operation experiments with DSP TI TMS320F28335. And, also the value of A and B are manually supplied in this experiment. Experimental parameters are shown in Table I. Dead time of each switch is set as 1μs.

A. Power Efficiency

Fig. 13 shows the power efficiency results for the both of the conventional and the proposed operation. It can be seen that the power efficiency of buck mode can be apparently improved by up to 37% using the proposed operation at 100W as shown in Fig. 13 (a). It can be seen that the power efficiency of boost mode can be apparently improved by up to 30% at 100W as shown in Fig. 13 (b).

B. Estimating the Value of Loss

Fig. 14 shows φ - P_{o} of analysis and experimental results. The value of r_{loss} for the conventional operation is for the analysis is set to 2.0Ω. The value is the measurement result of series resistance r_{s} of the transformer as shown in Table I measured with LCR meter Agilent 4263B.

The value of r_{loss} for the proposed operation is calculated with averaged equivalent resistance with the averaged power calculation describe below.

$$\overline{P}_{loss\_conv} \approx r_s \frac{\int_0^T (i_{Lm}(t))^2\, dt}{T} = r_s \frac{V_{in}^2 T^2}{3L^2} \tag{44}$$

$$\overline{P}_{loss\_proposed} \approx \frac{\int_0^{DT} r_s (i_{Lm}(t))^2\, dt}{T} = \frac{r_s V_{in}^2}{T\,L^2} \int_0^{DT} t^2\, dt$$

$$= \frac{r_s V_{in}^2 D^3 T^2}{3L^2} = r_s D^3 \frac{V_{in}^2 T^2}{3L^2} \tag{45}$$

where D is the conduction time ratio of switching term in no load condition and T is the half of switching term.

From the calculation results, r_{loss} of the proposed operation is calculated as the averaged equivalent resistance as

$$r_{loss} = D^3 r_s. \tag{46}$$

From the result of our optional experiment, D is obtained as 0.5 ohm. Therefore, the r_{loss} for the proposed operation is set as 0.25 ohm.

Comparing loss including analysis and experimental results, the root mean square was in 4% both of boost mode and buck mode.

| Item	Symbol	Specification
Transformer		
1) Turns ratio	A	1:1
2) Leakage inductance (primary-referred)	L	110μH
3) Series resistance (primary-referred)	r_s	2Ω
Converter		
1) Rated output power	P_{o}	1kW
2) Rated input direct voltage	V_{in}	150V
3) Rated output direct voltage	V_{out}	150V
4) Switching frequency	f_{s}	20kHz
5) Absolute maximum ratings of IGBT collector-emitter	v_{CE}	600V
6) On resistance of IGBT	r_{t}	50mΩ
7) Absolute maximum ratings of diode	i_{F}	30A
8) Forward voltage of diode	v_{F}	0.8V
9) Recovery time of diode	t_{rr}	0.1μs

VIII. CONCLUSION

By the analysis of the circuit operation and the some experiments, the validation of the proposed operation for DAB dc-to-dc converter is revealed. Form the analysis, P_{o} can be calculated with the loss included analysis for both of the conventional and the proposed technique. The analysis results are well matched with the experimental results. Applying the two modes which are proposed operation in light load and conventional operation in heavy load, the circuit can be operated in the full load range. 37% maximum power efficiency improvement can be confirmed at light load.

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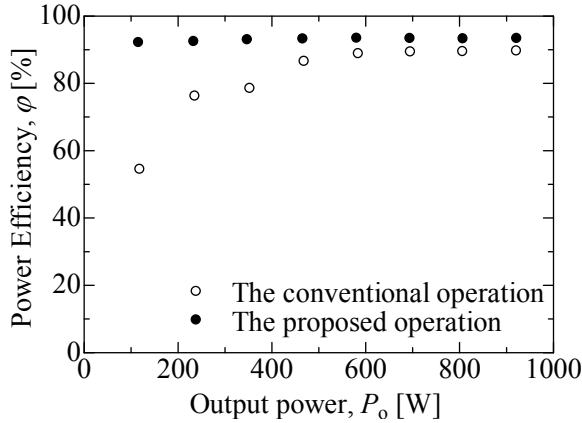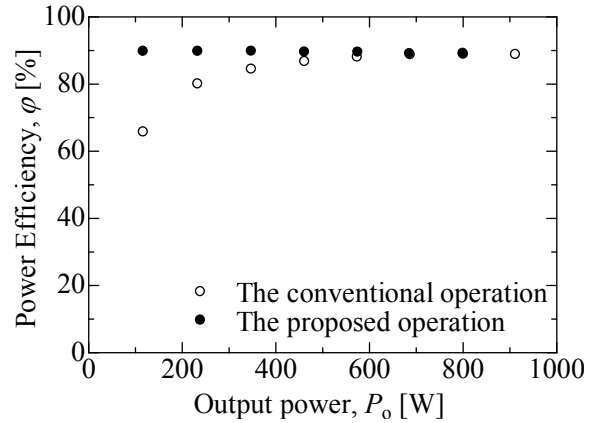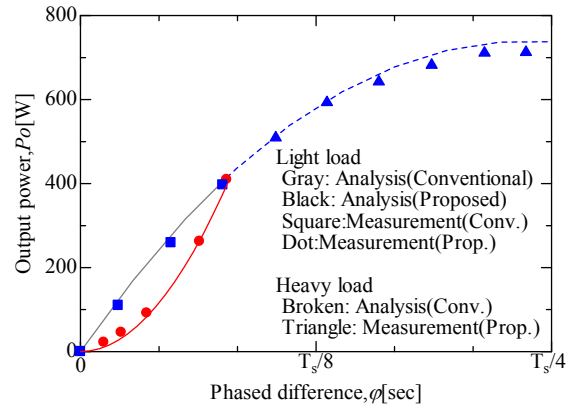
(a) Buck mode   (b) Boost mode

Fig. 13. Power efficiency: (a) Buck mode (V_{in}=200V, V_{out}=150V); (b) Boost mode (V_{in}=100V, V_{out}=150V).
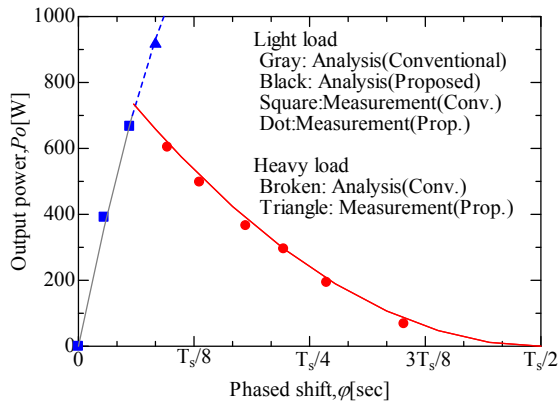
(a) Buck mode   (b) Boost mode

Fig. 14. φ - P_o (analysis and experimental results).

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