Integrated Buck-Boost Converter with Matrix-POL Architecture

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Keywords

«Voltage Regulator Modules (VRM) », «Pont-of-Load (POL) converter », «Power integrated circuit »

Abstract

In this study, integrated buck-boost converter with the Matrix-POL power supply system is proposed. From the simulation results, the validity of the Matrix-POL is revealed. The results revealed that the fast response to the load current and the voltage change can be done with duty and parallel number control by the proposed system.

Introduction

Power management of the Micro Processing Unit (MPU) has been strongly required in order to improve the performance. Figure1 shows the estimates of the increase in power consumption due to information appliance in Japan and the world. It is expected that the consumption will be brought about an increase by 5.2 times over the period 2006 to 2025 in Japan. Also, it is expected to be 9.4 times over the same period in the world [1].
Therefore, the efficient-energy-use for MPU is very important, and some adaptive techniques for power management have been proposed [2, 3]. Dynamic Voltage and Frequency Scaling (DVFS) and Power gating technique have been attracting attention as energy saving technique for MPU. DVFS is the technique that the low power consumption by the optimal value of the supply voltage and clock frequency of LSI in Fig. 2 [2]. The power-gating is the technique that is reducing the leak current by interrupting the power supply when it is not necessary to operate the circuit in Fig. 3 [3]. Power supply for the MPU is the strict conditions required that achieve high efficiency at low voltage, high current and fast response (nsec. order) for the varying of load current and target voltage. The concepts of these techniques were very effective for power management. But, bulky DC-DC converter can't achieve fast response to the very fast change of the voltage or the current, because of the effect of the package or line impedance. Therefore, nowadays, the integration of the point of load (POL) has been paid attention, rapidly [3-8]. In this paper, as one of the integrated POL study, Matrix-POL power supply system is proposed.

Matrix-POL Power Supply System Model

Figure 4 shows proposed Matrix-POL power supply system model. This system has a single-input and multiple-output. Each output terminal is connected in parallel. The parallel number is dynamically changed by the output voltage regulation feedback control when the load current is changed in transient term. And, at least, one of the parallel POL is connected to the next output stage. Each single POL is constructed with H-bridge converter as shown in Fig. 5. Figure 6 shows buck mode operation. Figure 7 shows boost mode operation. Figure 8 is the averaging model of H-bridge which is used in the simulation shown in next chapter [9, 10].

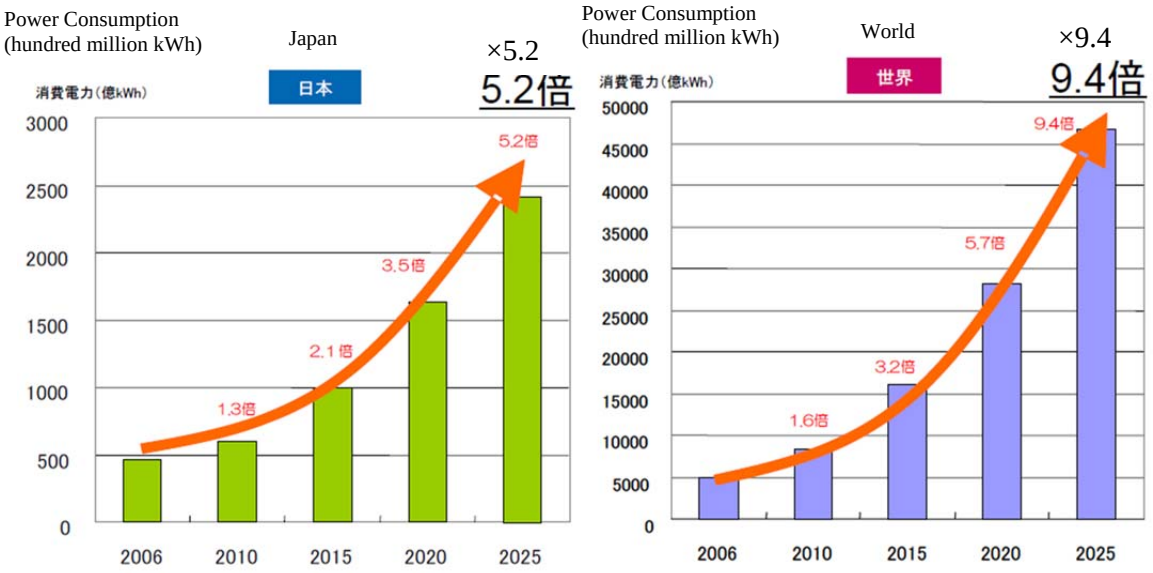

Fig. 1 Changes in estimates of power consumption by the information appliance [1]

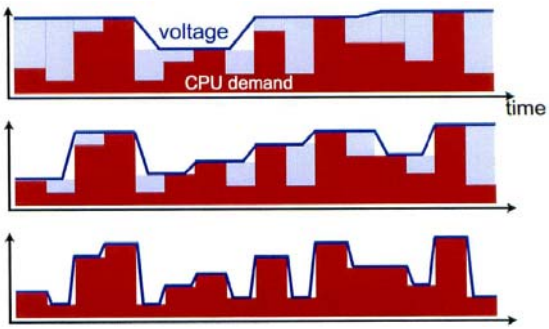

Fig. 2 DVFS [2]

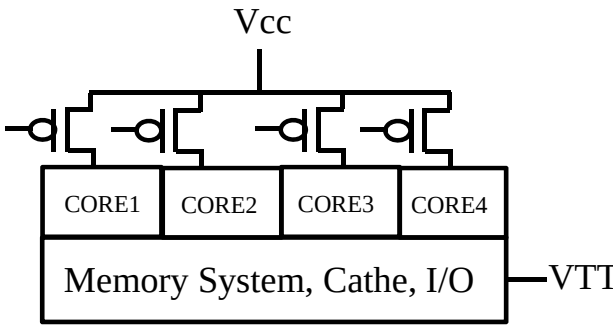

Fig. 3 Power Gating [3]

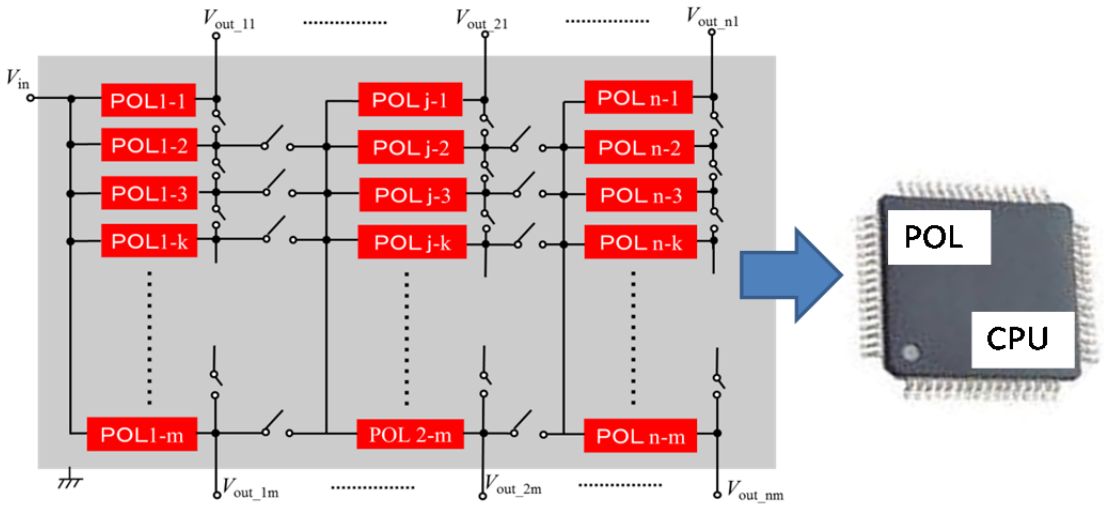

Fig. 4 Matrix-POL Power Supply System

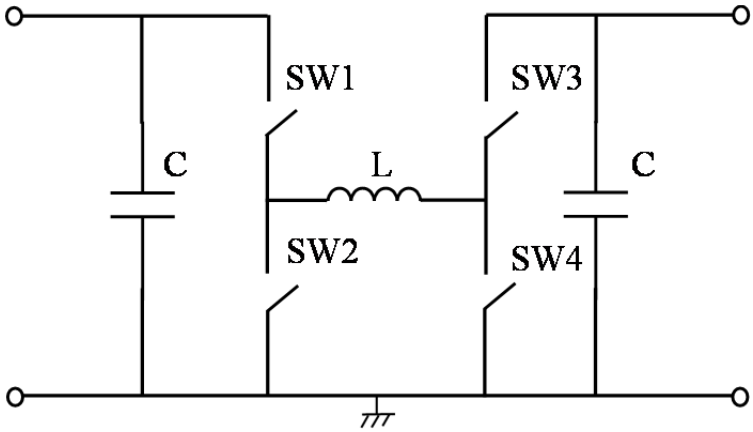

Fig. 5 H-bridge

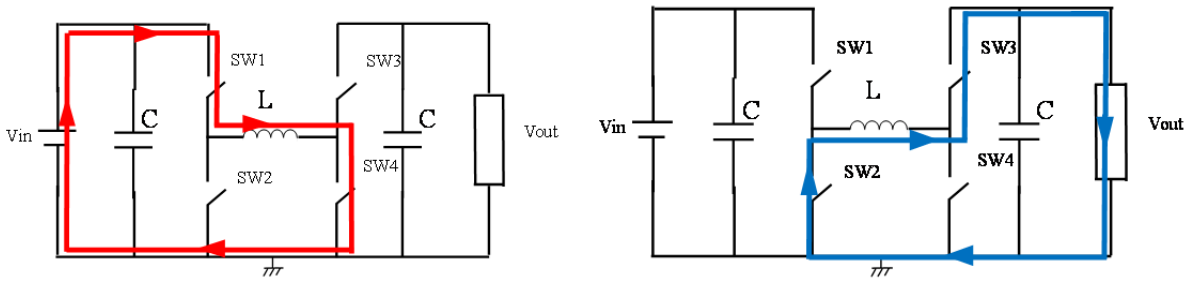

Fig. 6 H-bridge (Buck mode operation)

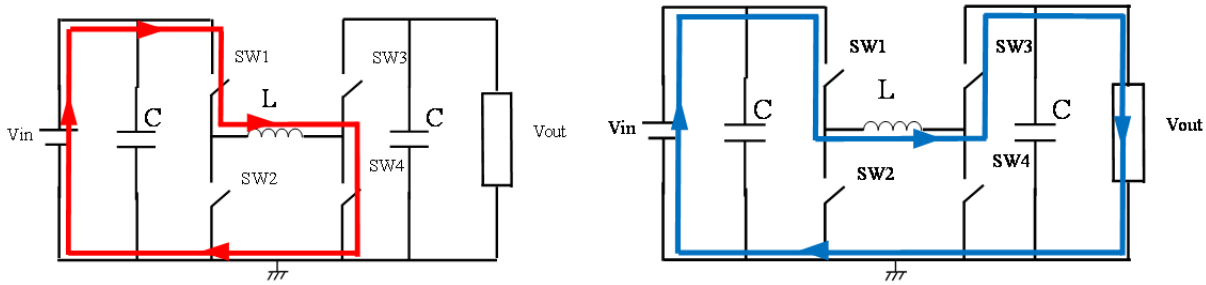

Fig. 7 H-bridge (Boost mode operation)

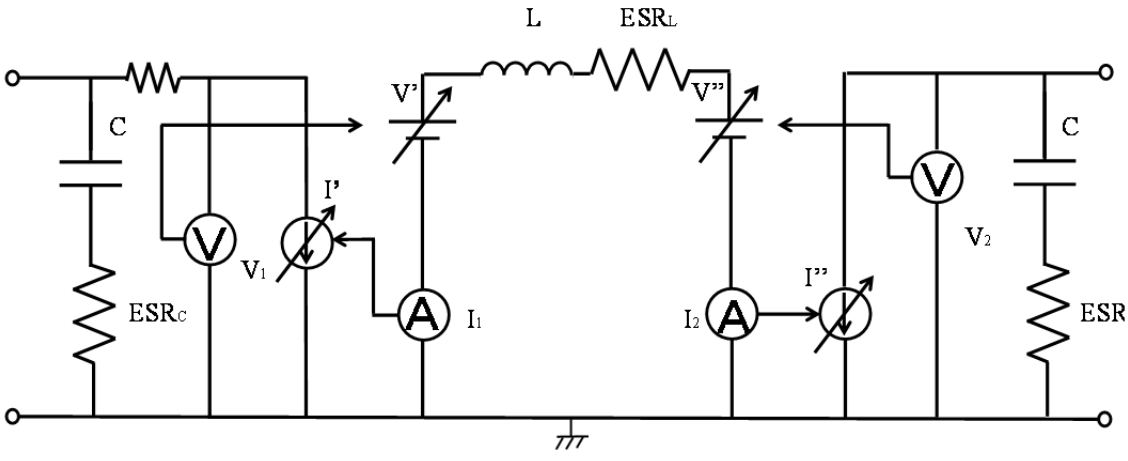

Fig. 8 Averaging model (H-bridge)

The parameters in Fig. 8 are determined as show in below.

$$V' = d * V_1 \tag{1}$$

$$V'' = (1-d) * V_2 \tag{2}$$

$$I'' = d * I_1 \tag{3}$$

$$I'' = (1-d) * I_2 \tag{4}$$

where d is duty-ratio.

Comparison of Matrix-POL with conventional POL

This proposed system has two options to control output voltage. One is by duty ratio and the other is by the parallel number.

In steady term, the each output terminal voltage is regulated with the feed-forward controlled duty ratio depends on VID of MPU. And, dynamical output voltage regulation is performed with feed-back controlled parallel number of POL. The simulation parameters are shown in Table I. Figure 9 shows conventional off-chip POL averaging model. Figure10 shows simulation model for Matrix-POL on chip. The output terminals of each ten paralleled POLs are connected to one output terminal. The gate switch can adeptly change the parallel number for the output terminal. The rest of the POLs which have not be connected to output terminal, are all connected to the input terminal of next output stage. Fig. 11 shows the load conditions for the simulation. Figure 12 shows the control algorithm. Initially, ten paralleled POL is set to five for the output and five for the next stage. When the load current change occurred, the parallel number of POL is controlled with the feedback information of the load current.

Figure 13 to 15 show the simulation results for the comparison of load current change response. Figure13 shows the result of the conventional off-chip POL. Figure 14 shows the result of single on-chip POL. Figure 15 shows the result of Matrix-POL on-chip.

From these results, it can be confirmed that the parallel number changing regulation method of Matrix-POL for the load current change is valid than duty- ratio regulation only.

Table I Simulation parameter

Vin	3.3V	Rin	100mΩ
L	10nH	ESRL	100mΩ
C	0.1mF	ESRC	10mΩ
Vo1(light-load)	1.5V	Io1(light-load)	0.3A
Vo1(heavy-load)	1.6V	Io1(heavy-load)	0.6A
parasitic components			
R	1mΩ	L'	0.1μH
C'	100nF		

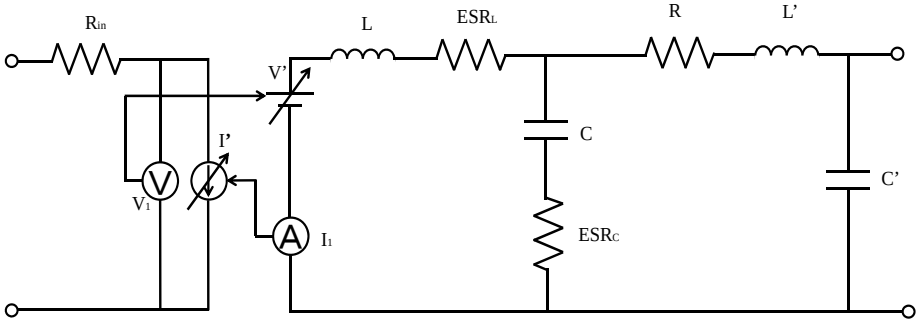

Fig. 9 Simulation circuit (Single POL)

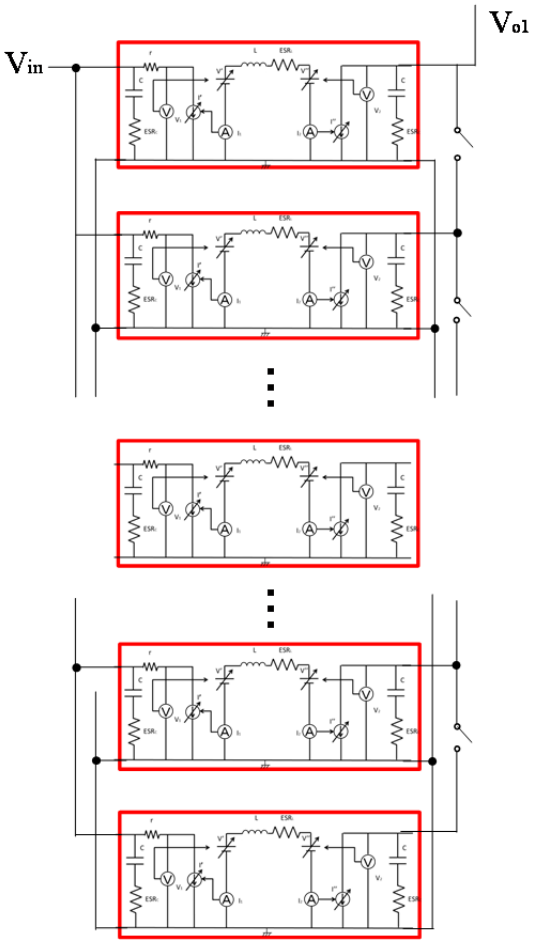

Fig. 10 Simulation circuit (Matrix-POL)

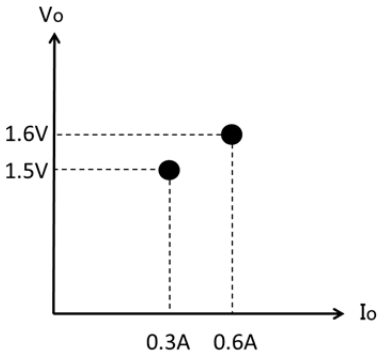

Fig. 11 Load model

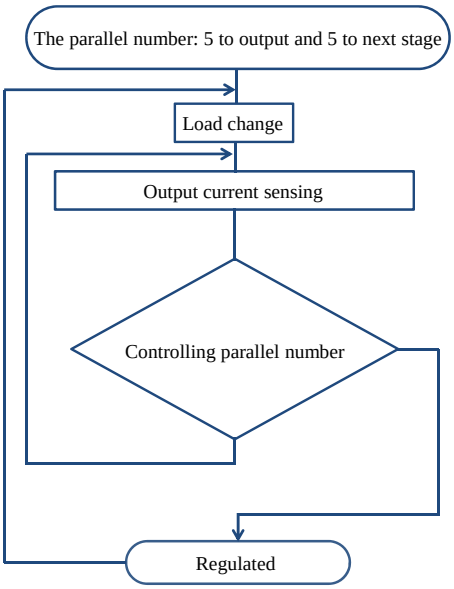

Fig. 12 Control Algorithm

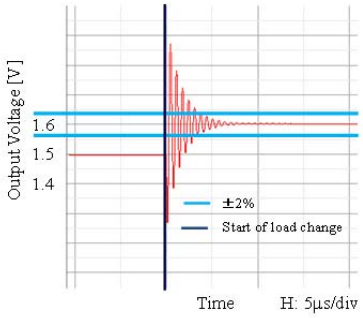

Fig. 13 Conventional off-chip POL

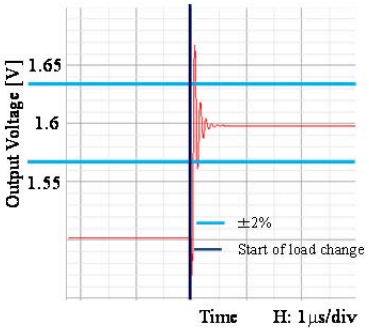

Fig. 14 Single on-chip POL

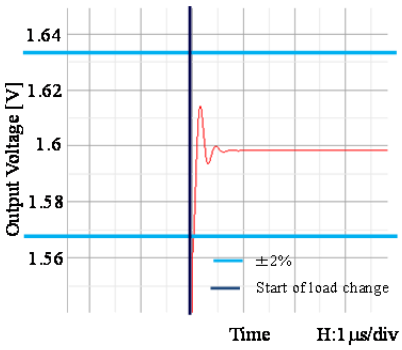

Fig. 15 Matrix-POL on-chip

Multi-Output Condition Simulation

To confirm the validation of the proposed method, we performed numerical simulation for multi-output condition with Maplesim. The Matrix-POL is configured one input voltage and three output voltage terminal. To each output voltage terminal, paralleled POL whose duty ratio is same is connected. The parallel number is dynamically changed from one to nine depends on the feed-back signal. The all of the rest parallel POL is connected to next output voltage stage. Figure 16 is simulation circuit. Table II shows simulation parameters. Table III shows first stage output number of parallel look up table, and Table IV shows second-stage output number of parallel look up table. Table V shows transition condition. Figure 16 shows simulation circuit, and Fig.17, 18, 19 shows simulation results. Output reference voltage of each stage is assumed to be changed with each load current. In each output stage, high speed response is revealed to the load and the voltage change. Output voltage surge can be suppressed in 5.6% in the worst case. From the results, it can be seen that stable and high speed response can be accomplished even in the multi-output condition.

Table II Simulation parameter

Vin	3.3V	Rin	100mΩ
L	10nH	ESRL	100mΩ
C	0.1mF	ESRC	10mΩ
Vo1(light-load)	1.5V	Io1(light-load)	0.3A
Vo1(heavy-load)	1.6V	Io1(heavy-load)	0.6A
Vo2(light-load)	1.5V	Io2(light-load)	0.3A
Vo2(heavy-load)	1.6V	Io2(heavy-load)	0.6A
Vo3(light-load)	1.5V	Io3(light-load)	0.3A
Vo3(heavy-load)	1.6V	Io3(heavy-load)	0.6A

Table III First stage output number of parallel look up table

First stage output number of parallel		Second stage load current [A]	
		0.3	0.6
First stage load current [A]	0.3	5	3
	0.6	7	5

Table IV Second stage output number of parallel look up table

Second stage output number of parallel		Second stage load current [A]	
		0.3	0.6
First stage load current [A]	0.3	5	7
	0.6	3	5

Table V Transition condition

Transition number	1	2	3	4	5	6	7
Io1/Vo1	0.3A/1.5V	0.6A/1.6V	0.6A/1.6V	0.6A/1.6V	0.3A/1.5V	0.3A/1.5A	0.3A/1.5V
Io2/Vo2	0.3A/1.5V	0.3A/1.5V	0.6A/1.6V	0.6A/1.6V	0.6A/1.6V	0.3A/1.5A	0.3A/1.5V
Io3/Vo3	0.3A/1.5V	0.3A/1.5V	0.3A/1.5V	0.6A/1.6V	0.6A/1.6V	0.6A/1.6V	0.3A/1.5V
D1/P1	0.315/5:5	0.33/7:3	0.333/5:5	0.334/5:5	0.317/3:7	0.315/5:5	0.315/5:5
D2/P2	0.466/5:5	0.477/3:7	0.492/5:5	0.495/5:5	0.49/7:3	0.466/5:5	0.466/5:5
D3/P3	0.419/10:0	0.425/10:0	0.423/10:0	0.448/10:0	0.458/10:0	0.444/10:0	0.426/10:0

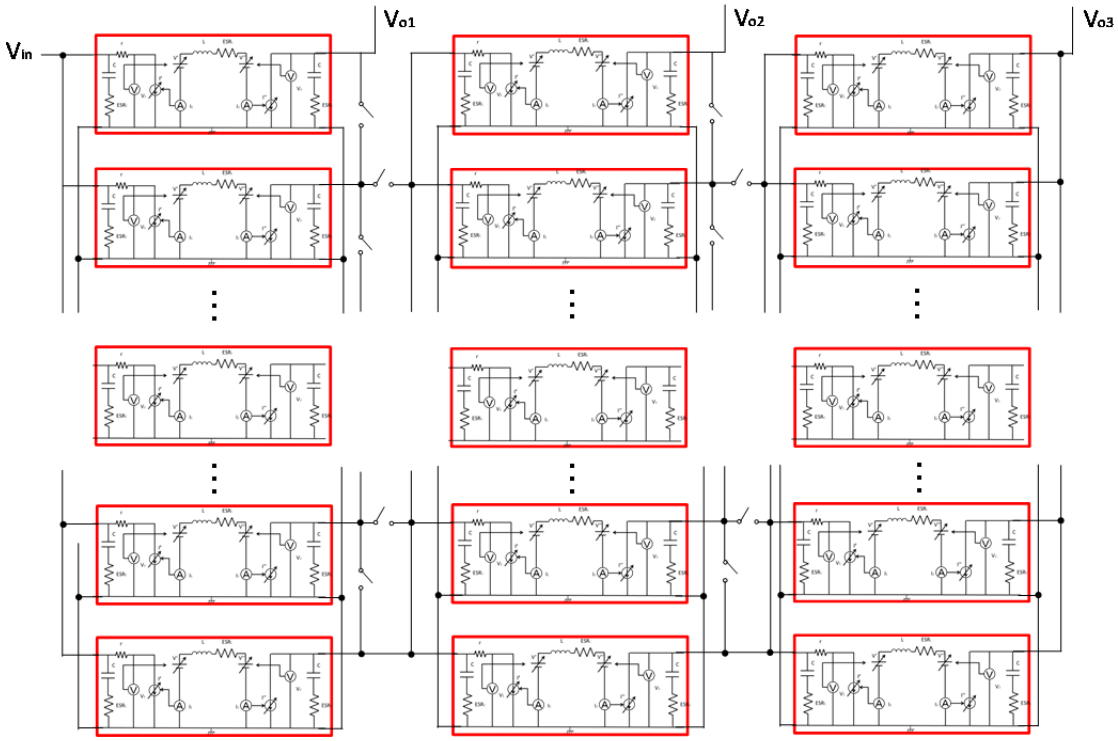

Fig. 16 Simulation circuit

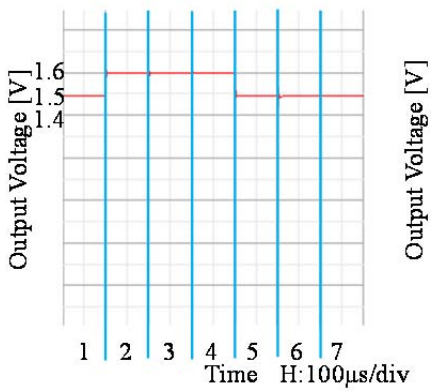

Fig. 17 V_{o1}

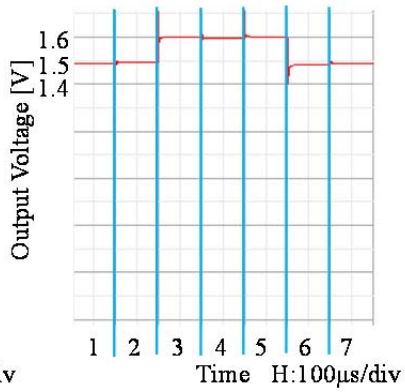

Fig. 18 V_{o2}

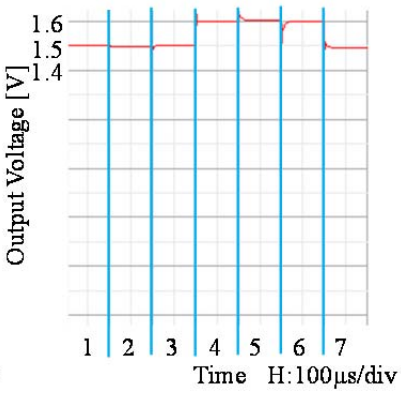

Fig. 19 V_{o3}

Conclusion

In this paper, integrated buck-boost converter with the Matrix-POL power supply system is proposed. From the simulation results, the validity of the Matrix-POL is shown. The results revealed that the fast response to the load current and the voltage change can be done with duty and parallel number control.

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