Frequency Response Analysis of Proposed Digital Control System for DPWM-POL

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Keywords

«Converter control», «High frequency power converter», «Pulse Width Modulation (PWM)», «Point-of-Load (POL) converter», «Switched-mode power supply»

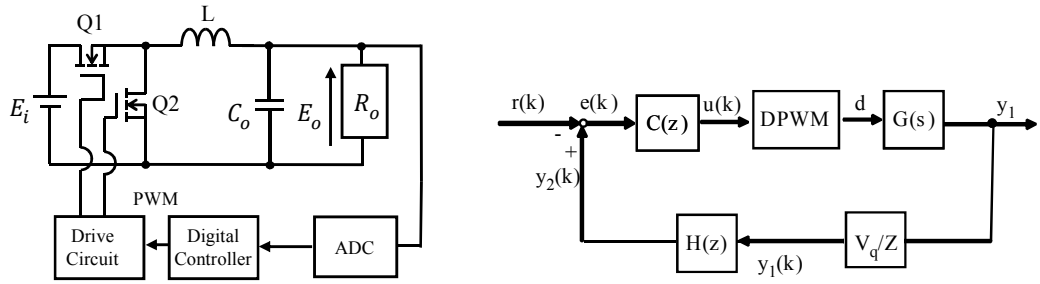
Abstract

This paper will discuss about the proposed hardware logic type digital controller for on-board SMPS which has a very small time-delay in control loop. Experimental results of the load current change experiment and the frequency characteristic of open loop transfer function has been described respectively. These results reveal the validity of the proposed technique.

Introduction

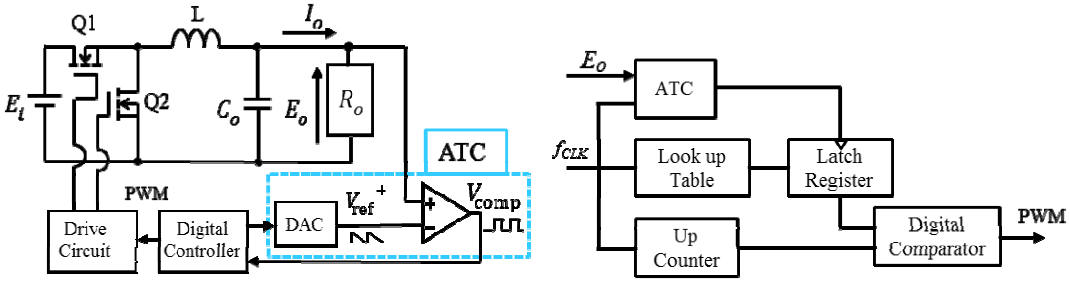
Digital electronic products have been spreading quickly by the advancement of the integrations technologies. ICs, DSPs and FPGAs require a high performance and a high speed due to the trend. Along with the situations, the power consumption is increasing. To suppress the power consumption, the power supply voltage is getting lower toward to sub 1V. Because of the severe voltage margin by the lower power supply voltages, special SMPS, point of load (POL) is disposed very near to the load.
The requirements of POL are relative low output voltage with large output current, high load change response, high-efficiency, low cost and etc. Also, the control circuit of POL is required to be high accurate, high speed, adaptive and low cost.

In these days, robustness or flexible controls for versatile conditions are demanded which cannot accomplished with analog control circuit. For the control purpose, pulse width modulation (PWM) control is a one of appropriate technique. Digital control or DPWM can accomplish robust and flexible power control with soft-tuned parameters and will become popular control technique [1-12]. Although, there are some disadvantages in cost and speed, against analog control circuit. We had proposed hardware-logic based digital PWM control circuit is effective to such requirements [13, 14]. In this paper, the proposed DPWM control method's principles of operation and circuit configurations are described firstly. At the next, the proposed technique is confirmed with some experiments.



(a) Circuit configuration (b) Control block

Fig. 1: General DPWM-POL



(a)Proposed DPWM-POL (b) Control blocks

Fig. 2: Circuit configuration of the proposed DPWM-POL

DPWM control method for POL (DPWM-POL)

The circuit configuration of general DPWM controller for POL

The circuit configuration of general DPWM controlled POL is shown in Fig. 1(a). This topology has two major time-delay problems. First, time-delay occurs at A/D converter with the conversion-delay. And, the calculation time of digital controller is another problem. Both of the time-delay directly effects on the response speed of the control circuit and influences stability of the control.

And, the cost and speed are always trade off problem. This problem is especially serious in POL DC-DC converter which is required to design the control circuit in relatively low-cost and high speed control response. Moreover, generally, there is a sample-hold circuit in front of A/D converter which degrades the response speed.

Total of the delay time will be described as the discrete delay factor Vq/Z in the control loop shown in Fig. 1(b) where Vq is a coefficient constant.

The circuit configuration of the proposed DPWM-POL

Figure 2 shows the main and the control circuit configuration of the proposed DPWM-POL in this research. Main POL circuit is a quite ordinary non-isolated buck converter. The control circuit is composed with D/A converter, analog comparator, digital controller and drive circuit. The analog timing converter (ATC) block shown in Fig. 2 (a) is composed with D/A converter and analog comparator.

In Fig. 2(b), the control block diagrams are shown. Output voltage E_O sensing at ATC block, PID control calculation block at look-up table, and gate pulse creation at up-counter block are all in parallel, synchronized with the system clock f_{CLK}.

The control circuit configuration of the proposed DPWM-POL

Figure 3 shows the precise control circuit configuration, and Fig. 4 shows control signal flow of the proposed DPWM-POL. Let's take a look at the signal flow.

As mentioned above, all blocks are synchronized with the system clock f_{CLK}. Memory 1 is used the look-up table method, and can store waveform values not only triangle or saw tooth but any waveforms. In this paper, the step-down saw tooth wave form is employed.

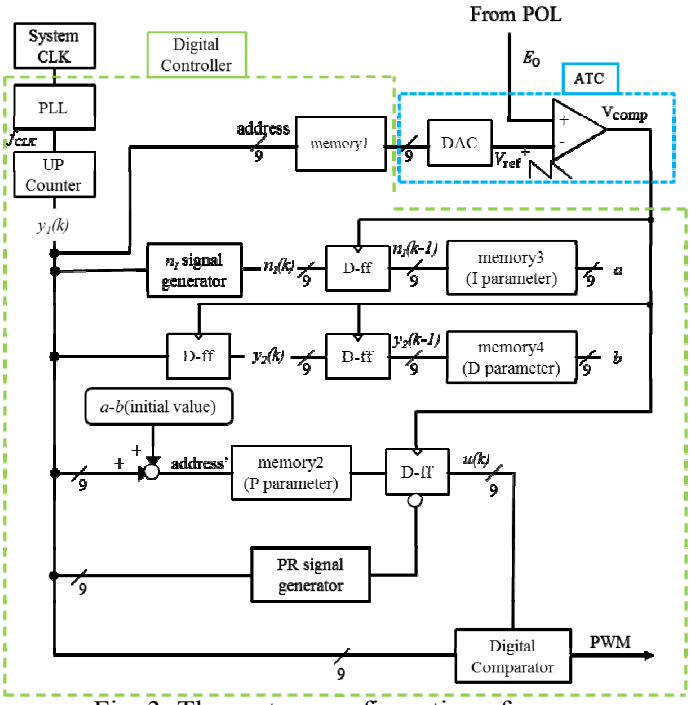


Fig. 3: The system configuration of the proposed control circuit

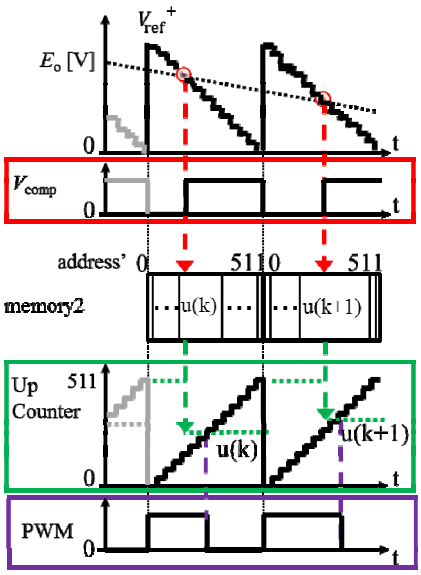


Fig. 4: Control signal flow

The output voltage E_o of POL is compared with the output voltage of D/A converter in the ATC block, successively. The comparator's output is read out to the latch signal to each D-ff at the timing that of E_o was sensed. Also, the look-up table method is used for the duty ratio calculation with memory 2, 3 and 4. Especially, the duty ratio data which is pre-calculated with the value of E_o, are stored in memory 2. The duty ratio data is read out from memory2 according to f_{CLK}. At the timing of E_o sensed, one of the duty ratio data is chosen and transferred to $u(k)$ in D-FF4, where k is the number of switching term. At the digital comparator, $u(k)$ is compared with up-counter data, and converted to real-time analog PWM waveforms. On-term $T_{on}(k)$ of DPWM signal of switching term k is decided by $u(k)$. In parallel with the processing of ATC block, the $u(k)$ is called with system clock and latched by ATC output as trigger. At the last of the switching term, $u(k)$ is preset maximum value by PR signal generator for preparing next term. The delay of the proposed control circuit is mostly dominated with the calling and the loading time of memory 2. Because of the small delay of this control technique, the sensed E_O data can affect on-term of the same switching term.

PID control with Look-up Table

$u(k)$ which is stored in memory 2 is pre-calculated by general PID digital control laws as

$$u(k) = u_{ref} + K_P e(k) + K_I n_I(k) + K_D (e(k) - e(k-1)) \qquad (1)$$

where u_{ref} is a reference value of $u(k)$, $e(k)$ is an digitalized error value between r which is digitalized reference voltage V_{ref} and, $y_1(k)$ is output data of up-counter in switching term k, so,

$$e(k) = y_1(k) - r\,, \qquad (2)$$

K_P, K_I and K_D are a proportional gain, an integral gain and an derivative gain, respectively, $n_I(k)$ is integral factor, that is

$$n_I(k) = n_I(k-1) + e(k)\,. \qquad (3)$$

At the timing of the latch signal is becoming high, $y_1(k-1)$ is latched to $y_2(k-1)$ as

$$y_2(k-1) = y_1(k-1) . \tag{4}$$

From above equations, Eq.(1) can be transformed to

$$u(k) = u_{ref} - (K_P + K_I)r + A\{y_1(k) + \frac{K_I}{A} n_I(k-1) - \frac{K_D}{A} y_2(k-1)\} \tag{5}$$

where $A = K_P + K_I + K_D$.

In Fig. 3,

$$a = \frac{K_I}{A} n_I(k\text{-}1) , \tag{6}$$

$$b = \frac{K_D}{A} y_2(k\text{-}1) . \tag{7}$$

Memory 3 and memory 4 store *a* and *b,* respectively.

In (5), $a\text{-}b$ in the term *k* is pre-calculated in the term *k-1* and the obtained value becomes the initial value of programmable counter of the term *k*. And, *address'* which indicates address of memory 2 is incremented with system clock and *u(k)* is called from memory 2, simultaneously.

$$address' = y_1(k) + a - b \tag{8}$$

From (5) and (8),

$$u(k) = u_{ref} - (K_P + K_I)r + A\{address'\} \tag{9}$$

Therefore, *u(k)* is determined as soon as E_O is sensed.

DPWM resolution

DPWM resolution is decided by value of the bit of memory 2. Therefore, it can be changed DPWM resolution easily by changing value of the bit of memory 2. In this paper, 9bit is used.

Experimental results

Experimental conditions

Some experiments are performed to verify the scheme. The proposed control system with prototype circuit is shown in Fig. 5. The digital controller part is designed with FPGA Altera Cyclone IV. The total number of logic elements is 163 including all of the memory sections. Figure 6 shows experimental waveforms. All memory blocks, memory 1, memory 2, memory 3 and memory 4, are including in the logic elements. Texas Instruments DAC900 is used as DAC. Liner Technology LT1719 is used as analog comparator. Microchip MCP14628 is used as driver. The DC-DC converter topology is basically same as buck converter in Fig.2. The experimental conditions are shown in Table I. V_{ref}^{+} is the maximum output voltage of DAC . During sensed output voltage $E_O > V_{\text{ref}}^{+}$, PWM signal becoming off, forcely.

TABLE I: Experimental conditions

Input voltage E_i	6V
Output reference voltage V_{ref}	1.5V
Output current I_o	0.01A – 2.3A
Switching frequency f_s	1MHz
Choke inductor L	10μH
Output capacitor C_o	105μF
Proportional gain K_P	0.01 - 5
Integral gain K_I	0 – 0.08
Differential gain K_D	0
V_{ref}^{+}	1.7V
f_{CLK}	500MHz

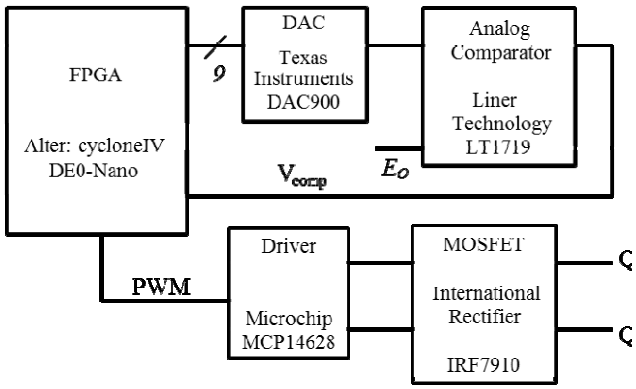


Fig. 5: Prototype proposed control circuit

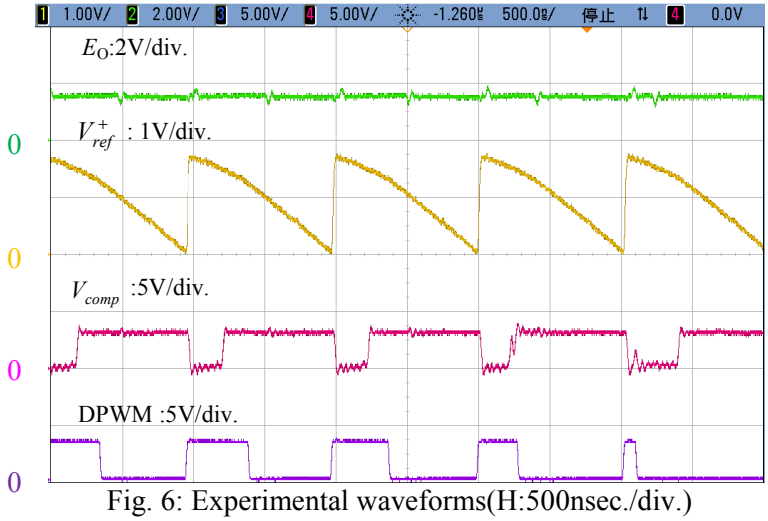


Fig. 6: Experimental waveforms(H:500nsec./div.)

Input-output characteristics of the proposed control circuit

Figure 7 shows input-output characteristics of the proposed control circuit. This figure shows results of proportional control conditions with K_I=K_D=0. Therefore, this system can do both of linear and nonlinear control.

Load current change dynamic response

The experimental results for dynamic response against load current change between 0.01A to 2.3A with 50A/μs slew rate condition are described in this section. Agilent Technologies DSO7054A is used to measure output voltage and DPWM signal, simultaneously.

Figure 8 shows experimental waveforms of load current change when K_P=5, K_I=0. And, Fig. 8(a) shows a light -to- heavy load transient. It shows output voltage change is settled in 1.48μsec. Over shoot is 56.3mV, under shoot is 87.5mV. Fig. 8(b) shows a heavy-to-light load transient. It shows output voltage change is settled in 1.44μsec. Over shoot is 112.5mV, under shoot is 81.5mV.

Figure 9 shows an enlargement of Fig.8. Figure 9 shows response time from the trigger. The prototype proposed control circuit responses in 3μsec in a light -to- heavy load transient, 1.1μsec in a heavy -to- light load transient.

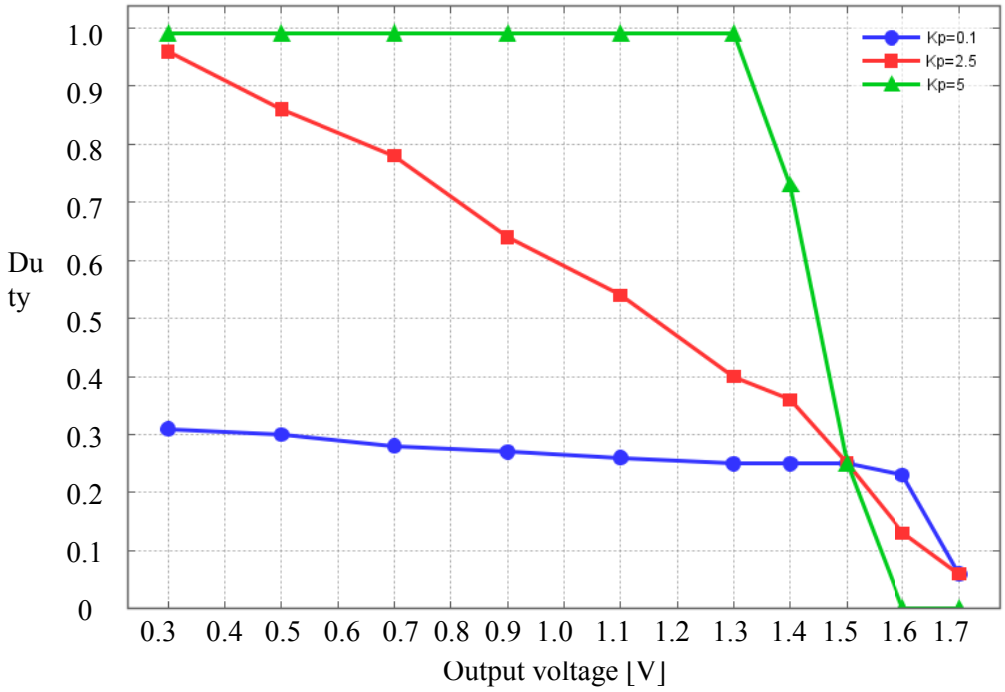
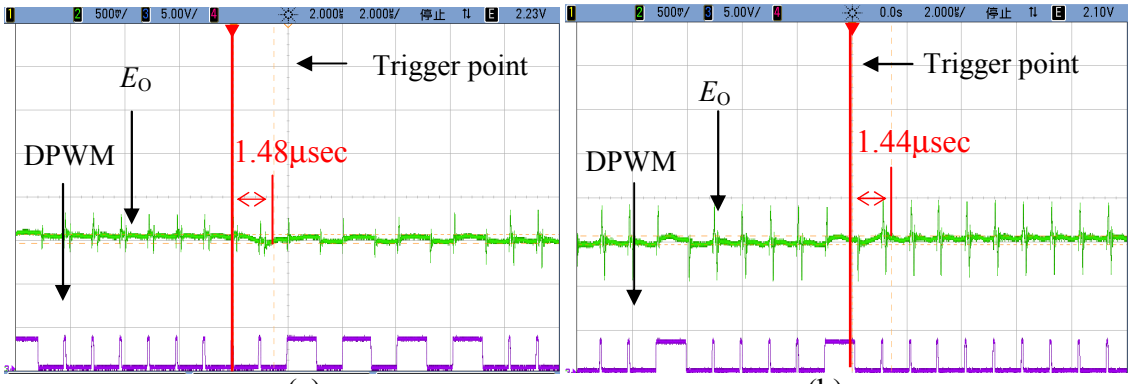
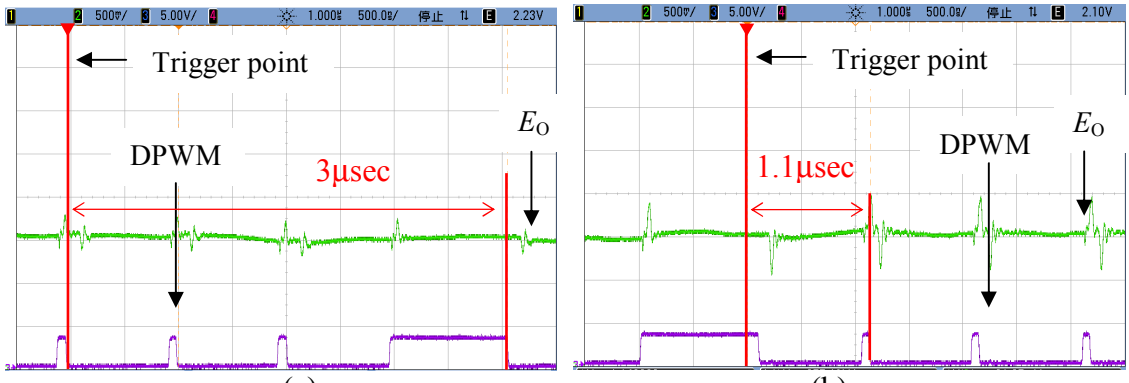


Fig. 7: Input-output characteristics of the proposed control circuit



(a) (b)

Fig. 8: Load current change dynamic response(K_P=5)



(a) (b)

Fig. 9: Load current change dynamic response (an enlargement of Fig.8)

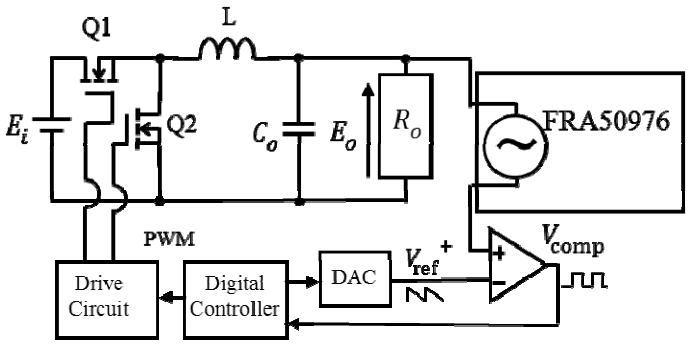


Fig. 10: Measurement system for frequency characteristic of open loop transfer function

A. Frequency characteristic of open loop transfer function

Figure 10 is measurement system for frequency characteristic of open loop transfer function. From Fig. 11 to Fig. 13 are the result of frequency characteristics of open loop transfer function with K_P=5 when I_o=0.01, 0.5 and 1A, respectively. From Fig.11 to Fig. 13, it can be seen that phase margin is about 88 degree and gain margin is about 17 dB in worst case.

Figure 14 shows the result with the condition of K_P=5 and K_I=0.08. From Fig.14, phase margin is about 109 degree and gain margin is about 30 dB. DC gain is increased about 5 dB from the condition of K_I=0.

From these results, this controller has enough phase margin and gain margin. The time-delay has small effects to the control loop.

Conclusion

In this paper, the hardware logic type digital controller for on-board SMPS, which has a very small time-delay in control loop, is confirmed with some experiments including frequency response analysis. The experimental results are confirmed with 1MHz switching frequency. From the frequency response results, the phase margin was 109 degree, gain margin was 30, and DC gain was 38 dB.

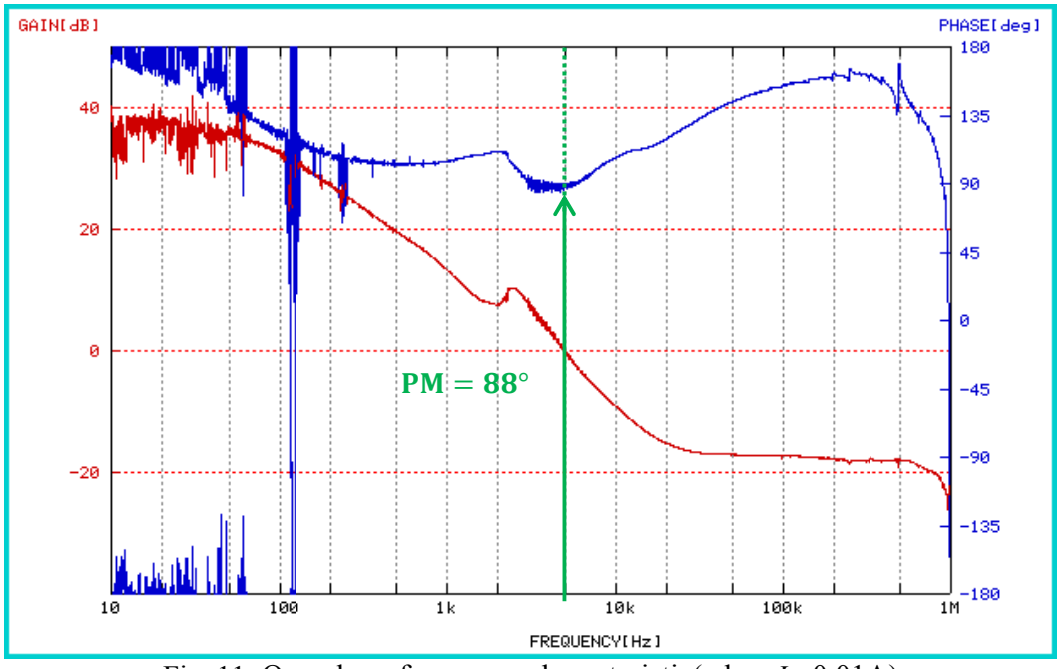


Fig. 11: Open loop frequency characteristic(when I_o=0.01A)
K_P=5, K_I=0
(Red:Gain[dB], Blue:Phase[degree])

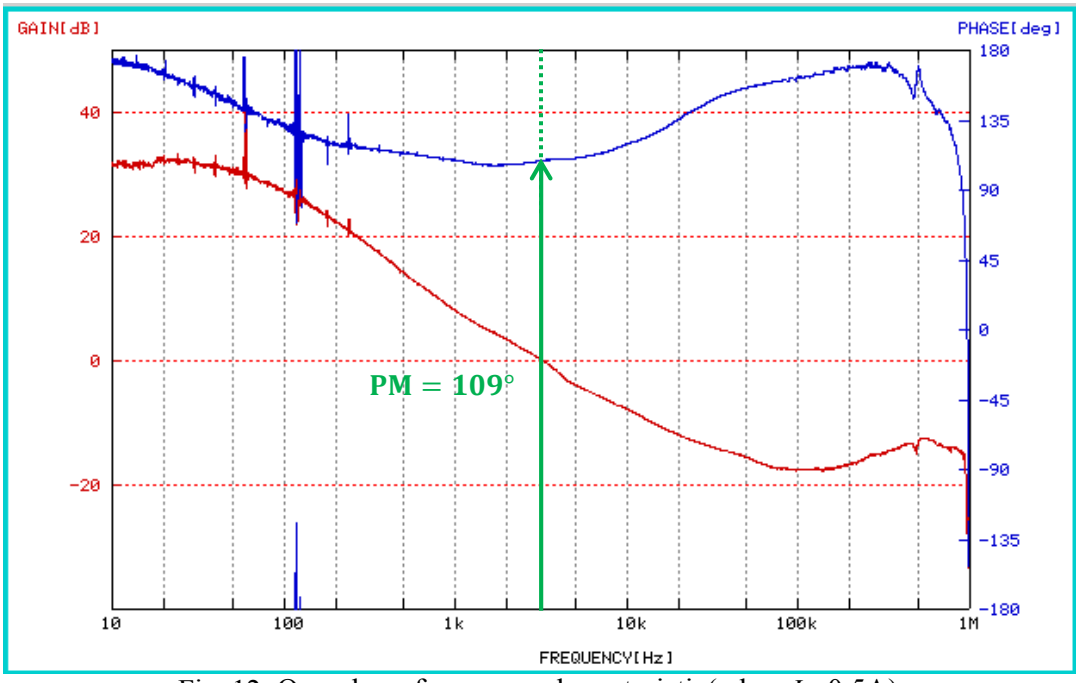


Fig. 12: Open loop frequency characteristic(when I_o=0.5A)
K_P=5, K_I=0
(Red:Gain[dB], Blue:Phase[degree])

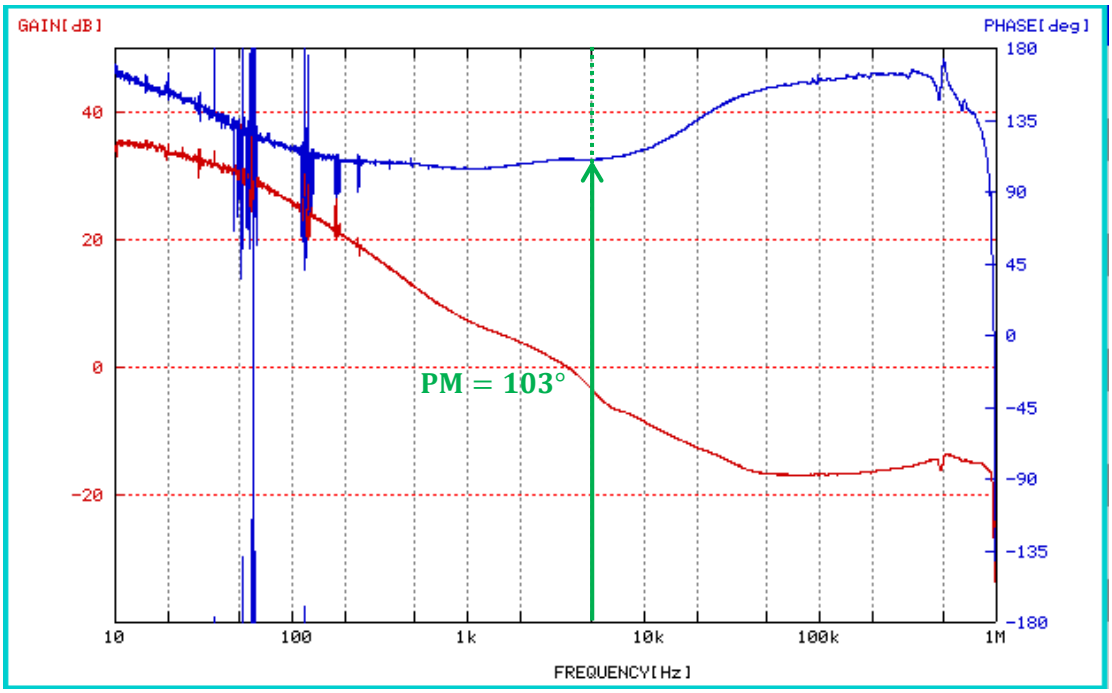


Fig. 13: Open loop frequency characteristic(when I_o=1A)
K_P=5, K_I=0
(Red:Gain[dB], Blue:Phase[degree])

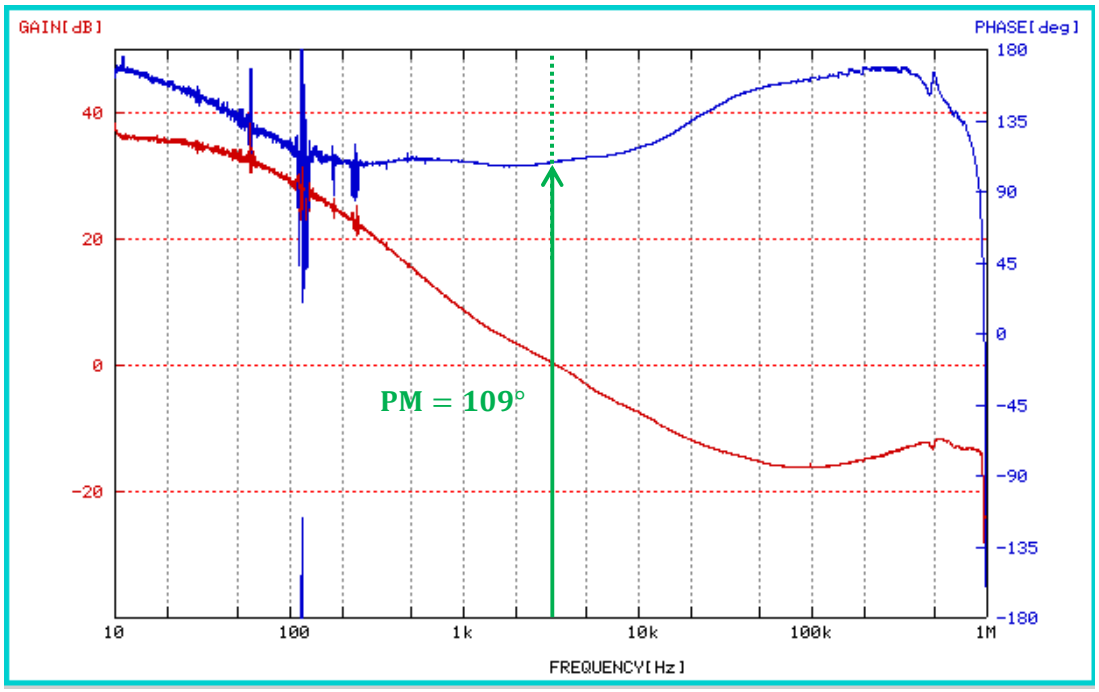


Fig. 14: Open loop frequency characteristic(when I_o=0.5A)
K_P=5, K_I=0.08
(Red:Gain[dB], Blue:Phase[degree])

References

[1] Jurgen Alico, Aleksandar Prodic," Multiphase Optimal Response Mixed-Signal Current-Programmed Mode Controller", Applied Power Electronics Conference and Exposition (APEC), 2010 Twenty-Fifth Annual IEEE.

[2] Amir Babazadeh, Luca Corradini, and Dragan Maksimović, "Near Time-Optimal Transient Response in DC-DC Buck Converters Taking into Account the Inductor Current Limit", Energy Conversion Congress and Exposition, 2009. ECCE 2009. IEEE.

[3] Edward Lam, Robert Bell and Donald Ashley, "Revolutionary Advances in Distributed Power Systems, " in Proc. IEEE APEC '03, 1.5, 2003.

[4] V. Peterchev, S. R. Sanders, "Quantization resolution and limit cycling in digitally controlled PWM converters", IEEE Transactions on Power Electronics, Vol. 18, No. 1, January 2003, pp. 301 - 308.

[5] B.J. Patella, A. Prodic, A. Zirger, D. Maksimovic, "High-frequency digital PWM controller IC for DC-DC converters", IEEE Transactions on Power Electronics, Vol. 18, January 2003.

[6] D. Maksimovic, R. Zane, R. Erickson, "Impact of Digital Control in Power Electronics", IEEE International Symposium on Power Semiconductor Devices & ICs, Kitakyushu, Japan, May 2004, pp. 13-22.

[7] S. Saggini, D. Trevisan, P. Mattavelli, "Hysteresis-Based Mixed-Signal Voltage-Mode Con-trol for dc-dc Converters", IEEE Power Electronics Conference (PESC'07), Orlando, Florida, June 2007.

[8] S. Saggini, E. Orietti, P. Mattavelli, A. Pizzutelli, A. Bianco, "Fully-Digital Hysteretic Vol-tage-Mode Control for dc-dc Converters based on Asynchronous Sampling", IEEE Applied Power Electronics Conference (APEC'08), Austin, Texas, February 2008.

[9] Aleksandar Radi´c, Zdravko Luki´c, Aleksandar Prodi´c, Robert H. de Nie, "Minimum-Deviation Digital Controller IC for DC–DC Switch-Mode Power Supplies", IEEE TRANSACTIONS ON POWER ELECTRONICS, VOL. 28, NO. 9, SEPTEMBER 2013.

[10] Eric Meyer, Zhiliang Zhang, Yan-Fei Liu, "Digital Charge Balance Controller with Low Gate Count to Improve the Transient Response of Buck Converters", Energy Conversion Congress and Exposition, 2009. ECCE 2009. IEEE.

[11] Santa C. Huerta, Pedro Alou, Oscar Garcia, Jesus Angel Oliver, Roberto Prieto, and Jose Cobos, " Hysteretic Mixed-Signal Controller for High-Frequency DC–DC Converters Operating at Constant Switching Frequency", IEEE TRANSACTIONS ON POWER ELECTRONICS, VOL. 27, NO. 6, JUNE 2012

[12] Albert Ting Leung Lee, Philip Ching Ho Chan, "Adaptive Prediction in Digitally Controlled Buck Converter with Fast Load Transient Response", Control and Modeling for Power Electronics (COMPEL), 2012

IEEE 13th Workshop on.
[13] Akira Ichinose, Yoichi Ishizuka, Hirofumi Matsuo, “A Fast Response DC-DC Converter with Digital Pulse Width”, IEICE vol. 105, no. 538, EE2005-58, pp. 67-71, January 2006.
[14] Yoichi Ishizuka, Masao Ueno, Ichiro Nishikawa, Akira Ichinose and Hirofumi Matsuo, “A Low-Delay Digital PWM Control Circuit for DC-DC Converters, “22nd Annual IEEE Ap-plied Power Electronics Conference and Exposition, Anaheim, CA, USA, 15.7, pp.579-586 , 2007. 2

Appendix

To reveal the merit of the use of the DAC and comparator in spite of the ADC for sensing output voltage E_O, we have made survey at the view point of the market price and the conversion rate. Figure 13 shows the results of comparison of several parallel interface DACs and ADCs. The horizontal axis represents the market price for 50 pcs, and the vertical axis represents the conversion rate. The products from four major companies A, B, C, and D, are compared. ADCs are shown in square mark, and DACs are triangle mark. Apparently, almost all of DACs are relatively cheaper than ADC in every grade conversion rate.

From the above, it is apparent that the proposed analog voltage sensing part which is composed with DAC and analog comparator, is superior than conventional sensing technique with ADC in the point of view of high speed response and cost.

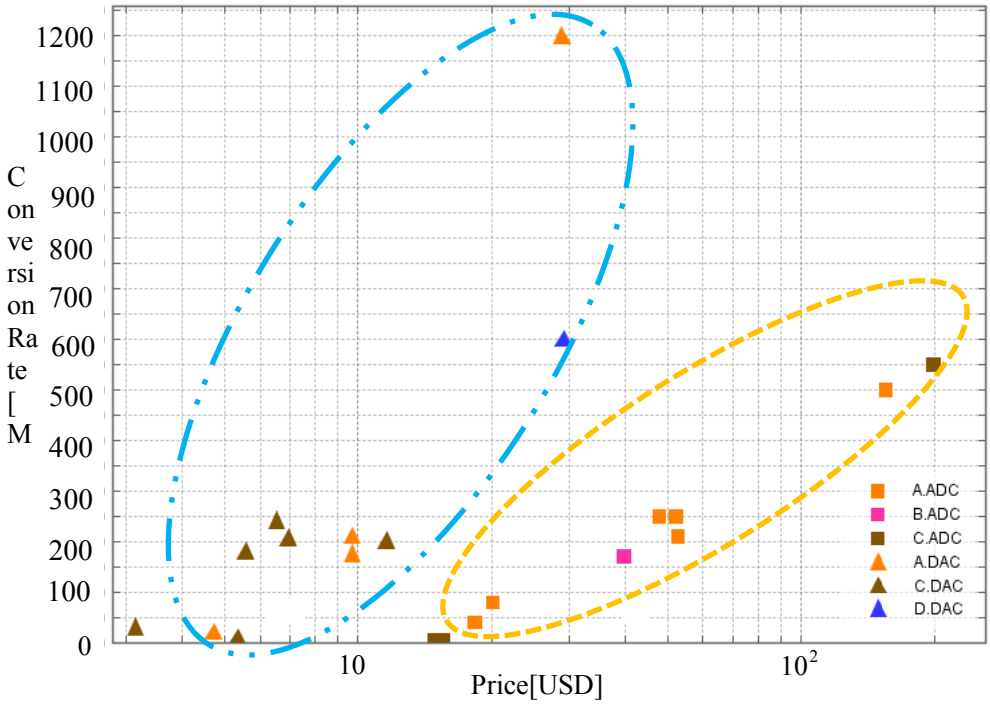


Fig. 15: Comparing 12bit ADCs and 12bit DACs