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Composite Power Semiconductor Switches for High-Power Applications

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Doctor of Philosophy

School of Engineering
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Declaration

I declare that this thesis has been composed solely by myself and that it has not been submitted, in whole or in part, in any previous application for a degree. Except where states otherwise by reference or acknowledgement, the work presented is entirely my own.

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Abstract

It is predicted that 80 % of the world's electricity will flow through power electronic based converters by 2030, with a growing demand for renewable technologies and the highest levels of efficiency at every stage from generation to load. At the heart of a power electronic converter is the power semiconductor switch which is responsible for controlling and modulating the flow of power from the input to the output. The requirements for these power semiconductor switches are vast, and include: having an extremely low level of conduction and switching losses; being a low source of electromagnetic noise, and not being susceptible to external Electromagnetic Interference (EMI); and having a good level of ruggedness and reliability. These high-performance switches must also be economically viable and not have an unnecessarily large manufacturing related carbon footprint.

This thesis investigates the switching performance of the two main semiconductor switches used in high-power applications — the well-established Silicon (Si)-Insulated-Gate Bipolar Transistor (IGBT) and the state-of-the-art Wide-Bandgap (WBG) Silicon-Carbide (SiC)-Metal–Oxide–Semiconductor Field-Effect Transistor (MOSFET). The SiC-MOSFET is ostensibly a better device than the Si-IGBT due to the lower level of losses, however the cost of the device is far greater and there are characteristics which can be troublesome, such as the high levels of oscillatory behaviour at the switching edges which can cause serious Electromagnetic Compatibility (EMC) issues. The operating mechanisms

of these devices, the materials which are used to make them, and their auxiliary components are critically analysed and discussed. This includes a head-to-head comparison of the two high-capacity devices in terms of their losses and switching characteristics. The design of a high-power Double-Pulse Test Rig (DPTR) and the associated high-bandwidth measurement platform is presented. This test rig is then extensively used throughout this thesis to experimentally characterise the switching performance of the aforementioned high-capacity power semiconductor devices.

A hybrid switch concept — termed "The Diverter" — is investigated, with the motivation of achieving improved switching performance without the high-cost of a full SiC solution. This comprises a fully rated Si-IGBT as the main conduction device and a part-rated SiC-MOSFET which is used at the turn-off. The coordinated switching scheme for the Si/SiC-Diverter is experimentally examined to determine the required timings which yield the lowest turn-off loss and the lowest level of oscillatory behaviour and other EMI precursors. The thermal stress imposed on the part-rated SiC-MOSFET is considered in a junction temperature simulation and determined to be negligible. This concept is then analysed in a grid-tied converter simulation and compared to a fully rated SiC-MOSFET and Si-IGBT. A conduction assistance operating mode, which solely uses the part-rated SiC-MOSFET when within its rating, is also investigated. Results show that the Diverter achieves a significantly lower level of losses compared to a Si-IGBT and only marginally higher than a full SiC solution. This is achieved at a much lower cost than a full SiC solution and may also provide a better method of achieving high-current SiC switches.

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List of Acronyms

AC Alternating Current

ACC Active Current Control

ADC Analogue-to-Digital Converter

AGD Active Gate-Drivers

ASIC Application-Specific Integrated Circuit

AWG American Wire Gauge

AVC Active Voltage Control

BFoM Baliga's Figure of Merit

BJT Bipolar Junction Transistor

BNC Bayonet Neill–Concelman

BW Bandwidth

C Carbon

CAD Computer Aided Design

CCL Current Commutation Loop

CE Conducted Emissions

CM Common-Mode

CMOS Complementary Metal-Oxide-Semiconductor

CMRR Common-Mode Rejection Ratio

CMTI Common-Mode Transient Immunity

CoC Chip on Chip

CSR Charge Storage Region

CT	Current Transformer
CVR	Current Viewing Resistor
DAC	Digital-to-Analogue Converter
DC	Direct Current
DLB	Direct Lead Bonding
DM	Differential-Mode
DPTR	Double-Pulse Test Rig
DUT	Device Under Test
EM	Electromagnetic
EMC	Electromagnetic Compatibility
EMI	Electromagnetic Interference
ESL	Equivalent Series Inductance
ESR	Equivalent Series Resistance
EV	Electric Vehicle
FACTS	Flexible Alternating Current Transmission System
FCC	Federal Communications Commission
FEM	Finite Element Method
FET	Field-Effect Transistor
FFT	Fast Fourier Transform
FIT	Failure in Time
FPGA	Field Programmable Gate Array
FRD	Fast Recovery Diode
FSM	Finite State Machine
FWD	Freewheeling Diode
GaN	Gallium Nitride
HEMT	High-Electron-Mobility Transistor
HS	High-Side
HVDC	High-Voltage Direct Current

IGBT Insulated-Gate Bipolar Transistor

IC Integrated Circuit

IEC International Electrotechnical Commission

JBS Junction Barrier Schottky

JFET Junction Field-Effect Transistor

JFoM Johnson's Figure of Merit

KC Kelvin-Collector

KD Kelvin-Drain

KE Kelvin-Emitter

KS Kelvin-Source

LCoE Levelised Cost of Energy

LDMOS Laterally Diffused MOSFET

LED Light-Emitting Diode

LS Low-Side

MLCC Multi-Layer Ceramic Capacitor

MELF Metal Electrode Leadless Face

MMC Modular Multi-Level Converter

MMCX Micro-Miniature Coaxial

MOS Metal–Oxide–Semiconductor

MOSFET Metal–Oxide–Semiconductor Field-Effect Transistor

MOV Metal-Oxide Varistor

MP Midpoint

MPS Merged PIN Schottky

NPC Neutral Point Clamped

NPT Non-Punch Through

NTC Negative Temperature Coefficient

Op-Amp Operational Amplifier

OVLO Over-Voltage Lockout

PCB Printed Circuit Board

PE Power Electronic

PEEK Polyether Ether Ketone

PETG Polyethylene Terephthalate Glycol-modified

PL Part-Load

PLSC Part-Load-Subcycle

PoF Power-over-Fiber

PSU Power Supply Unit

PT Punch Through

PTC Positive Temperature Coefficient

PV Photovoltaic

PVC Polyvinyl Chloride

PWL Piece-Wise Linear

PWM Pulse-Width Modulation

RC Reverse-Conducting

RE Radiated Emissions

RF Radio Frequency

RFI Radio Frequency Interference

SBD Schottky Barrier Diode

SCC Short Circuit Capacity

SEB Single-Event Burnout

SEE Single-Event Effect

Si Silicon

SiC Silicon-Carbide

SJBT Superjunction IGBT

SJMOS Superjunction MOSFET

SMA Sub-Miniature Version-A

SMPS Switched-Mode Power Supply

SMT	Surface-Mount Technology
SOA	Safe Operating Area
SoC	System on a Chip
SPICE	Simulation Program with Integrated Circuit Emphasis
SPT	Soft-Punch Through
SSR	Solid-State Relay
TIM	Thermal Interface Material
TSEP	Temperature Sensitive Electrical Parameters
UV	Ultraviolet
UVLO	Under-Voltage Lockout
VDMOS	Vertical Double-Diffused MOSFET
VSC	Voltage-Source Converter
VUMOS	Vertical U-Trench MOSFET
VVMOS	Vertical V-Groove MOSFET
WBG	Wide-Bandgap
XS	Cross-Switch
ZCS	Zero Current Switching
ZTC	Zero Temperature Coefficient
ZVS	Zero Voltage Switching

Nomenclature

Symbols

δ_{skin}	Skin Depth	[m]
ϵ_r	Dielectric Constant (Relative Permittivity)	
λ	Wavelength	[m]
λ_T	Thermal Conductivity	[W/cmK]
μ_n	Electron Mobility	[cm^2/Vs]
μ_p	Hole Mobility	[cm^2/Vs]
μ_r	Relative Permeability	
ϕ	Magnetic Flux	[Wb]
ρ	Resistivity	[Ω·m]
σ	Conductivity	[S/m]
$\sigma_{dielectric}$	Dielectric Conductivity	[S/m]
τ_{HL}	Charge Carrier High-Level Lifetime Constant	[s]
ζ	Damping Factor	
A_{busbar}	Busbar Area	[m^2]
B	Magnetic Flux Density	[T]
BW	Bandwidth	[Hz]
C	Capacitor/Capacitance	[F]
C_{bulk}	DC Bulk Capacitance	[F]
C_{busbar}	Busbar Capacitance	[F]
$C_{dc-link}$	DC-Link Capacitance	[F]

$C_{decouple}$	High-Frequency Decoupling Capacitance	[F]
C_{ds}	Drain-Source Capacitance	[F]
C_{gd}	Gate-Drain Capacitance	[F]
C_{gs}	Gate-Source Capacitance	[F]
C_{iss}	Transistor Input Capacitance	[F]
C_{oss}	Transistor Output Capacitance	[F]
C_{ox}	Gate Oxide Capacitance	[F/cm^2]
C_{par}	Parasitic Capacitance	[F]
C_{rss}	Transistor Reverse Transfer Capacitance	[F]
D	Diode	
D_{EM}	Planar EM Wave Formation Distance	[m]
E	Energy	[J]
E_0	Junction Potential	[V]
$E_{AddCond}$	Diverter Additional Conduction Energy Loss	[J]
E_{Comm}	Diverter Commutation Energy Loss	[J]
E_{crit}	Critical Electric Field	[kV/cm]
$E_{Div,Off}$	Diverter Turn-Off Switching Energy	[J]
E_{Off}	Turn-Off Switching Energy	[J]
E_{On}	Turn-On Switching Energy	[J]
E_{Switch}	Diverter Switching Event Energy Loss	[J]
E_{sw}	Switching Energy	[J]
f	Frequency	[Hz]
f_{3dB}	Corner/Cutoff/-3dB Frequency	[Hz]
f_n	Natural Resonant Frequency	[Hz]
f_o	Self Resonant Frequency	[Hz]
f_{res}	Resonant Frequency	[Hz]
f_{sw}	Switching Frequency	[Hz]
$G_{dielectric}$	Conductance of the Dielectric	[S]

I	Current	[A]
I_{CM}	Common Mode Current	[A]
I_c	Collector Current	[A]
$I_{d,sat}$	Drain Current (saturation region)	[A]
I_{DM}	Differential Mode Current	[A]
I_d	Drain Current	[A]
I_F	Forward Current	[A]
I_g	Gate Current	[A]
I_L	Load Current	[A]
I_{mos}	MOSFET Unipolar Current (IGBT)	[A]
I_{Phase}	Phase Current	[A]
I_{pnp}	BJT Bipolar Current (IGBT)	[A]
I_{rr}	Peak Reverse Recovery Current	[A]
I_s	Saturation Current	[A]
K_C	Charging Contactor	
K_D	Discharge Contactor	
L	Inductor/Inductance	[H]
L_{busbar}	Busbar Parasitic Inductance	[H]
L_{Comm}	Diverter Inter-Device Stray Commutation Inductance	[H]
L_C	Channel Length	[m]
L_{eq}	Equivalent Inductance	[H]
L_e	Busbar External Inductance	[H]
L_G	Gate Stray Inductance	[H]
L_i	Busbar Internal Inductance	[H]
L_{KS}	Kelvin-Source Stray Inductance	[H]
L_{Load}	Load Inductor	[H]
L_{stray}	Stray Inductance	[H]
L_s	Stray Inductance	[H]

M_L	Mutual Inductance	[H]
N	Number of Turns	
N_A	Acceptor Impurity Concentration	[cm^{-3}]
N_D	Donor Impurity Concentration	[cm^{-3}]
n_i	Intrinsic Carrier Concentration	[cm^{-3}]
P	Power	[W]
P_{IGBT}	Instantaneous Power Loss in IGBT	[W]
P_{L_cond}	Instantaneous Device Conduction Power Losses	[W]
P_{L_sw}	Instantaneous Device Switching Power Losses	[W]
P_L	Instantaneous Device Power Losses	[W]
P_{MOSFET}	Instantaneous Power Loss in MOSFET	[W]
Q	Charge	[C]
Q_{gs}	Required Gate Charge	[C]
Q_{rr}	Reverse Recovery Charge	[C]
R	Resistor/Resistance	[Ω]
r	Radius	[m]
$R_{\square}$	Sheet Resistance	[Ω/□]
R_{acc}	Accumulation Region Resistance	[Ω]
R_{busbar}	Busbar Resistance	[Ω]
R_B	Bleed Resistor	[Ω]
R_{ch}	Channel Resistance	[Ω]
R_{crit}	Critical Resistance (for critical damping)	[Ω]
R_C	Charging Resistor	[Ω]
R_{Drift}	Epitaxial-Layer/Drift Region Resistance	[Ω]
$R_{ds(on)}$	MOSFET On-State Resistance	[Ω]
R_D	Discharge Resistor	[Ω]
R_d	Resistance of Drain Connection	[Ω]
R_{eq}	Equivalent Resistance	[Ω]

$R_{g,int}$	Gate Resistance (internal)	[Ω]
R_{g_off}	Turn-Off Gate Resistance	[Ω]
R_{g_on}	Turn-On Gate Resistance	[Ω]
R_g	Gate Resistance (external)	[Ω]
R_{JFET}	JFET Pinching Resistance	[Ω]
R_M	CVR Measurement Resistance	[Ω]
R_{on}	On-Resistance	[Ω]
R_{sub}	Substrate Layer Resistance	[Ω]
R_s	Resistance of Source Connection	[Ω]
T_{amb}	Ambient Temperature	[K]
t_{charge}	Double-Pule Test Charging Time	[s]
T_c	Case Temperature	[K]
T_{Delay}	Diverter Delay Time	[s]
$t_{dielectric}$	Thickness of Dielectric Material	[m]
t_{fw}	Diode Freewheeling Time	[s]
t_f	Fall Time	[s]
T_j	Junction Temperature	[K]
t_{rr}	Reverse Recovery Time	[s]
t_r	Rise Time	[s]
V	Voltage	[V]
V_{br}	Breakdown Voltage	[V]
$V_{bus,+\Delta}$	DPTR Pre-Charge DC Bus Voltage	[V]
V_{bus}	DC Bus Voltage	[V]
$V_{ce(sat)}$	IGBT On-State Collector-Emitter Voltage	[V]
V_{ce}	Collector-Emitter Voltage	[V]
V_{CM}	Common Mode Voltage	[V]
V_{DM}	Differential Mode Voltage	[V]
$V_{drop,pn}$	Diode Voltage Drop (IGBT)	[V]

$V_{ds(on)}$	MOSFET On-State Drain-Source Voltage	[V]
V_{ds}	Drain-Source Voltage	[V]
V_F	Forward Voltage Drop	[V]
V_{ge}	Gate-Emitter Voltage	[V]
V_{gs}	Gate-Source Voltage	[V]
V_g	External Gate Voltage	[V]
$V_{ind.}$	Induced Voltage	[V]
V_L	Instantaneous Inductor Voltage	[V]
V_M	Voltage Measurement	[V]
V_{os}	Voltage Overshoot	[V]
V_{rr}	Peak Reverse Recovery Voltage	[V]
v_{sat}	Charge Carrier Saturation Velocity	[cm/s]
V_{Th}	Threshold Voltage	[V]
W_C	Channel Width	[m]
X_C	Capacitor Reactance	[Ω]
x_j	Junction Depth	[m]
X_L	Inductor Reactance	[Ω]
Z	Impedance	[Ω]
Z_{busbar}	Busbar Characteristic Impedance	[Ω]
$Z_{th(j-c)}$	Junction to Case Thermal Impedance	[ºC/W]
Z_{th}	Thermal Impedance	[ºC/W]
β_{pnp}	BJT Current Gain	

Physics Constants

ϵ_0	Permittivity of Free Space	$8.85418782 \times 10^{-12}$ F/m
μ_o	Permeability of Free Space	$1.25663706 \times 10^{-6}$ H/m
π	Pi	3.14159265359
eV	Electronvolt	$1.602176634 \times 10^{-19}$ J
k	Boltzmann's Constant	1.380649×10^{-23} J/K
q	Electron Charge	$1.60217662 \times 10^{-19}$ C

1 Introduction

1.1 The Role of Power Electronics

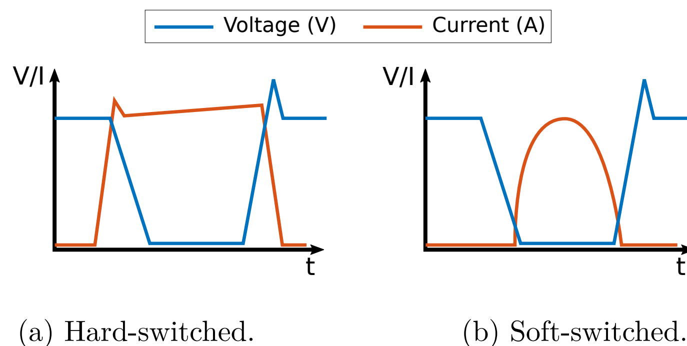
Power Electronic (PE) based converters are becoming ubiquitous in almost every aspect of how we generate, distribute and consume electricity. This technology provides the necessary functions that support applications such as: gigawatt scale High-Voltage Direct Current (HVDC) transmission and Flexible Alternating Current Transmission System (FACTS); megawatt scale grid-tied converters for renewable sources, such as wind and solar; kilowatt scale chargers and motor drives that are necessary for the forthcoming Electric Vehicle (EV) revolution; low-power converters found in consumer electronics, wireless power transfer and lighting; and many more. As we move toward a low-carbon society, the requirements for PE will be twofold in terms of efficiency and flexibility. It is these technologies that will enable future renewable energy sources and facilitate energy storage solutions whilst helping to maintain grid stability. It is predicted that 80 % of electricity will flow through PE based converters by 2030, more than double the current figure [1].

Power converters are capable of interfacing with either Direct Current (DC) or Alternating Current (AC), either single-phase or multi-phase, and range in complexity from circuits that operate using tens of components to those that use

thousands. The principal role of these systems is to convert one form of electrical energy into another. These power converters are able to achieve efficiencies of >95 % [1]. At the heart of a PE converter are the power semiconductor devices. Their job is to manage the flow of power round a converter and, with the aid of an external controller, supply or source the correct voltage and current levels. They achieve this by rapidly switching between an on and off state, typically at frequencies in the kHz range, in a controlled manner. Using a wide variety of modulation techniques, along with passive filtering components, the desired power flow can be realised.

1.2 Semiconductor Devices in a Power Converter

The way in which power semiconductor devices are used in a power converter can be generally classified as either hard-switched or soft-switched.



(a) Hard-switched.

(b) Soft-switched.

Figure 1.1: Device switching classification.

Hard-switching describes when the device's current and voltage overlap during the switching transitions resulting in an appreciable amount of switching loss ($P_{switch} = V_{switch} \times I_{switch}$) – this overlap is illustrated in Figure 1.1a. Whereas soft-switching behaviour occurs when the devices turn on or off with either zero voltage or zero current, known as Zero Voltage Switching (ZVS) and Zero Current Switching (ZCS) respectively, resulting in essentially zero switching loss.

However, soft-switching circuits can become complex and usually employ resonant techniques to achieve ZVS or ZCS. The conversion techniques which employ soft-switching of transistors are mainly found in low-power converters.

In high-power applications, the transistor is predominantly used in the hard-switched manner. This leads to switching losses which significantly contribute to total PE losses. Therefore, hard-switching will only be considered in this thesis.

1.2.1 Half-Bridge in Voltage-Source Converter (VSC)

In high-power applications, a hard-switched Voltage-Source Converter (VSC) is typically used — the most fundamental being the two-level converter. The basic structure of the two-level converter is formed using two power semiconductor switches (S_1 & S_2) in series, with diodes (D_1 & D_2) in parallel to each of them. This basic structure is termed a half-bridge, or phase-leg, and is shown in Figure 1.2. The top device is referred to as the High-Side (HS) and the bottom the Low-Side (LS).

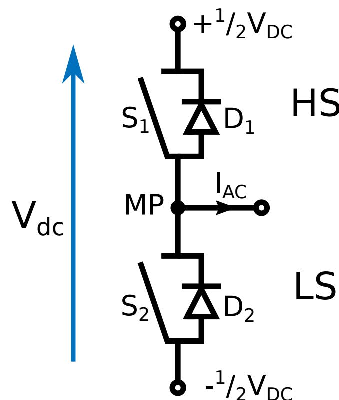


Figure 1.2: Half-bridge (HB) configuration for VSC.

The half-bridge is used to connect its Midpoint (MP) connection to either the positive or negative side of the DC voltage (V_{DC}) that is connected to its terminals. The available switching states are shown in Table 1.1. The HS and

LS devices are switched in a complimentary manner such that both are not on at the same time. If they were to simultaneously conduct, a short-circuit would be created and the devices would exhibit an over-current and fail. To avoid this happening when transitioning between HS conduction and LS conduction, a small delay period (dead-time) is used.

S2	S1	MP
0	0	Floating
0	1	$+ \nicefrac{1}{2}V_{DC}$
1	0	$- \nicefrac{1}{2}V_{DC}$
1	1	Not allowed[a]

[a] Would result in a short-circuit.

Table 1.1: Switching states of half-bridge (HB).

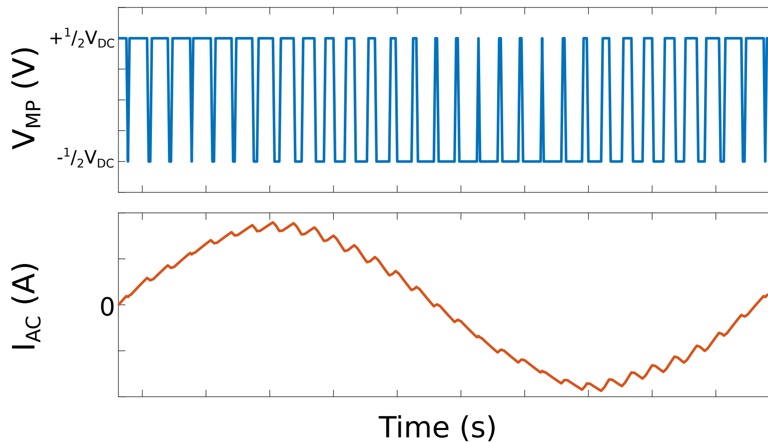


Figure 1.3: Two-level inverter voltage and current waveforms.

The top plot in Figure 1.3 shows how the half-bridge configuration is used to rapidly switch between $+\nicefrac{1}{2}V_{DC}$ and $-\nicefrac{1}{2}V_{DC}$. When this is done using modulation techniques, it can be used, with the aid of additional filtering, to produce an AC output. Figure 1.4 shows the system diagram for a typical three-phase grid-tied inverter — using three half-bridge's to realise the three-phases — with the required output LC stage (inductor and capacitor). The filter stage is connected to each phase output (MPs A, B, & C) and is used to average out the high-frequency switching to a smooth sinusoid. The switching frequency (f_{sw}) of the converter is related to the time constant of the filter stage, with an increase in

f_{sw} allowing for a reduction in the value and hence physical size of the filter. The anti-parallel diode, referred to as a Freewheeling Diode (FWD), is used for reverse inductive current flow. It also allows for rectification in the opposite direction for the inverter example shown.

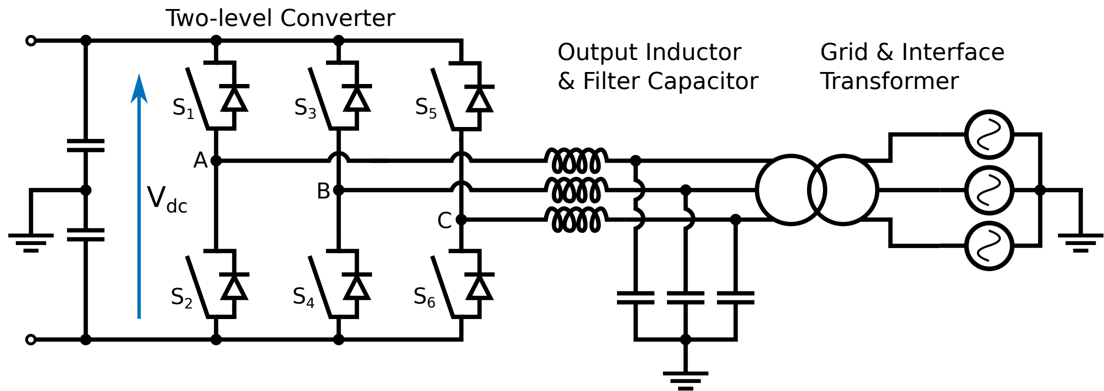


Figure 1.4: Three-phase inverter example (circuit diagram).

The “two-level” name of this converter class arises from the two voltage levels ($+\ ^1\!/_2 V_{DC}$ & $-\ ^1\!/_2 V_{DC}$) that the half-bridge can achieve. However, the half-bridge can be used to realise multi-level VSCs for high-power applications. For example; the three-level Neutral Point Clamped (NPC) converter; various multi-level flying-capacitor converters; and the Modular Multi-Level Converter (MMC) which is used in High-Voltage Direct Current (HVDC) applications.

Megawatt scale grid-tied converters that are used in, for example, wind turbine AC–AC converters, utility-scale solar farm inverters, and large-scale energy storage interfacing converters require high-capacity semiconductor devices. These high-capacity devices are required to operate at voltages in excess of 1–2 kV and conduct currents of 100s if not 1000s of amps.

1.2.2 Effective High-Capacity Semiconductor Devices

The semiconductor devices are instrumental in the efficient operation of the converter, however they do have some limitations and shortcomings. These are listed in Table 1.2.

Power Losses	A significant amount of power converter losses can be attributed to them, both when they switch and conduct.
Electromagnetic Noise	They can give rise to serious EMC issues, in the form of radiated and conducted.
Electrical Limitations	They have limited voltage, current and temperature operating capabilities.

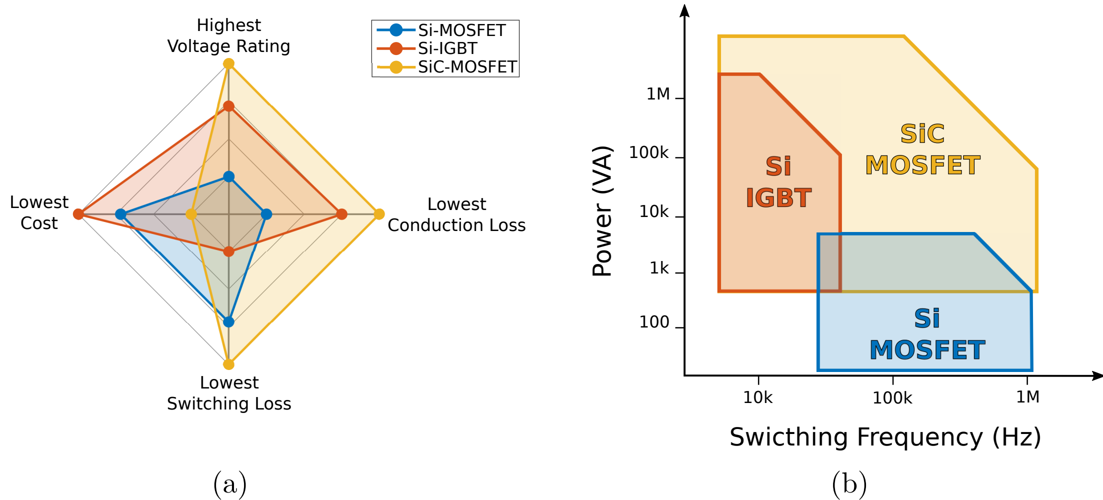
Table 1.2: Limitations and shortcomings of power semiconductor devices.

For VSC converters, the switching devices used must be fully controllable such that they can be turned on and off — a transistor offers this functionality. More than 30 years of research and development efforts have lead to the Silicon (Si)-Insulated-Gate Bipolar Transistor (IGBT) (with Si-based FWD) being the device of choice for high-power applications due to its high level of maturity. Even though further improvements are achieved with each new generation of Si-IGBT technology (however, these gains are becoming smaller with each iteration), the relatively poor switching performance of the Si-IGBT limits converter switching frequencies to $\sim$ 20 kHz for low-power converters and 2–4 kHz for high-power converters [2].

As such, there is significant interest in new compound-semiconductor materials (referred to as Wide-Bandgap (WBG) materials due to their greater bandgap and hence superior electrical performance than Si) and how they can be used in high-power devices. The most promising for the high-power industry is Silicon-Carbide (SiC), which is being used to fabricate Metal–Oxide–Semiconductor

Field-Effect Transistor (MOSFET) devices and high-performance Schottky diodes. These new SiC devices are beginning to unseat the Si-IGBT, however they come at a vast increase in cost per amp and, for reasons which will be later discussed, will always be more expensive and have a larger manufacturing related carbon footprint.

The spider chart in Figure 1.5a shows an indicative attribute comparison between the Si-IGBT and SiC-MOSFET (the Si-MOSFET is also included, however it has limited use in high-power applications). It can be seen that the SiC-MOSFET is the superior device in terms of voltage rating and losses. The plot in Figure 1.5b shows how the better traits relate to performance within a device.



(a) (b)

Figure 1.5: Power semiconductor device qualities, recreated from [3].

SiC-MOSFETs exhibit much lower switching loss due to the extremely fast switching transitions they can achieve. These fast dI/dt and dV/dt edges during the switching transitions can result in significant Electromagnetic Interference (EMI) issues. This demands very careful circuit layout and a variety of other techniques to manage this transient behaviour.

1.3 Research Motivations and Objectives

This thesis will investigate the switching performance of power semiconductor devices, with a particular focus on high-capacity state-of-the-art SiC-MOSFETs for use in hard-switched VSCs. Their switching behaviour will be experimentally compared to that of the traditional Si-IGBT. The paralleling and series connection of devices to achieve higher power ratings will be considered, as well as the techniques required to achieve this and to mitigate EMI. Finally, a hybrid configuration of SiC-MOSFET and Si-IGBT is investigated to fully understand it's potential use in high-power applications. This hybrid Si/SiC research explores techniques that may deliver improvements for high-power semiconductor switches, by balancing the compromise of switching and conduction loss, cost and complexity. The hybrid concept allows for maximising the switching speed for a power module without incurring excess EMI or overshoot voltage, which would ordinarily compromise utilisation of the device voltage rating.

This thesis will document the experimental analysis on the switching characteristics of the Si/SiC hybrid switch to prove that lower switching losses can be achieved. These results will then be used in device-level thermal simulations and system-level efficiency models to show the efficacy of the proposed hybrid switch.

1.4 Thesis Structure

The structure of this thesis is as follows:

Chapter 2 will give an overview of the operating mechanisms of power semiconductor device technologies — looking at traditional and new WBG materials.

Chapter 3 provides the theory and practical measures required for designing and testing high-power WBG systems. This is achieved through a detailed design report of the high-power Double-Pulse Test Rig (DPTR) and an overview of the experimental testing equipment and methodologies used in Chapters 4, 5 and 6.

Chapter 4 begins with a discussion on high-power Si-IGBT and SiC-MOSFET in the form of a head-to-head comparison and also shows the required measurement bandwidth for each technology at different power levels. Hybrid IGBT modules, which uses a Si-IGBT with a SiC-Schottky Barrier Diode (SBD), are analysed and discussed. The switching behaviour of high-power SiC-MOSFETs is characterised along with a discussion on techniques that can be employed to manage these fast transients.

Chapter 5 investigates the Diverter: a hybrid switch configuration of Si-IGBT and part-rated SiC-MOSFET which uses coordinated switching of the MOSFET at the turn-off transition to aide the IGBT. This chapter experimentally investigate this concept at high-power levels to discern the required timings in order to achieve minimum loss and EMI.

Chapter 6 further investigates the Diverter. Converter simulations are reported on to show the performance in an overall system. A thermal study is also carried out to understand the thermal stresses on the partially rated SiC-MOSFET.

Chapter 7 presents the conclusions of this thesis and the recommendations for future work.

* * *

2 | Power Semiconductor Devices Technology Review: Traditional & Wide-Bandgap

2.1 Chapter Introduction

This chapter will provide an overview of the power semiconductor devices used in high-power applications, both traditional Silicon (Si) based devices and new generation Wide-Bandgap (WBG) devices. It will give the reader an understanding of where the benefits and drawbacks are for unipolar and bipolar devices, in terms of static and dynamic performance. A review of high-power WBG devices — in particular Silicon-Carbide (SiC) — will be presented to show: where they are in technological maturity; the areas where further development is required; how they are theoretically superior to traditional Si devices; and why, in terms of fabrication costs, they will always be more expensive at a component level.

The chapter is structured as follows: Section 2.2 provides a overview of semiconductor materials, discusses what a WBG material is and why it is of importance; Section 2.3, 2.4, and 2.5 introduce the diode and transistor technologies that are investigated; Section 2.6 discusses how these devices can be enhanced

by using SiC technology and introduces some caveats to their adoption; and Section 2.7 covers real devices and their packaging, with an emphasis on the requirements for SiC.

2.2 Power Semiconductor Technologies

Power semiconductor devices are not intended to be operated in a linear manner like some other semiconductor families. They are designed to operate in one of two states, either on or off, and are optimised for this. However, unlike the devices found in the digital electronics field, power devices are able to process high-voltages and high-currents. In the off-state, the device offers a high impedance to the circuit and thus is able to block voltage. Conversely, in the on-state it presents itself as a low impedance path to the circuit and is able to conduct a large amount of current with little power loss. When transitioning between these two states, the power semiconductor device should be able to switch fast, with little overlap in current and voltage in order to avoid excessive levels of power loss.

2.2.1 Basic Solid-State Physics

To understand how these devices operate and how they can be effectively used, it is important to have a high-level overview of the basics of semiconductors [4, 5]. Traditionally these devices have been constructed using a monocrystalline group IV Si based semiconductor structure. Si is an abundant material that makes up more than 25 % of the earth's crust, in the form of Silicates. This makes it a relatively cheap material to use and one that manufacturers are now well experienced in processing. There are many other materials that can be used as

semiconductors, but Si is by far the most common and will be considered for this brief explanation. Pure Si, often termed as intrinsic, does not have any useful electrical properties. This is due to the lattice structure of the material, where every Si atom is connected via covalent bonds to another four Si atoms. This results in no additional/free electrons or holes[1] in the lattice. This is because Si is a group IV element with four electrons in its outer electron shell. When it is bonded with four other Si atoms, the valence of eight is complete. Intrinsic Si can be classed as an insulator that does not conduct. At the other end of the scale there are metals, which have an abundance of free electrons and will readily conduct current.

In order to make Si work as a semiconductor, small amounts of other elements are added to the material, in a process called doping. In essence, doping allows for precise control of the number of charge carriers and where they are in the material. The concentration of the doping is one parameter that defines the conductivity, or resistivity, of a material. The doped Si is now called extrinsic and comes in one of two forms: n-type, with free negative charge carriers; or p-type, with free positive charge carriers. An n-type material has additional electrons in the lattice structure and a p-type material has additional holes. Their properties are shown in Table 2.1.

	n-type	**p-type**
Dopant element group	V	III
Typical elements	P, As, Sb	B, Al, Ga, In
majority charge carriers	electrons	holes
minority charge carriers	holes	electrons

Table 2.1: Properties of n-type and p-type semiconductor materials.

There are a number of manufacturing processes and techniques which are capable of achieving this and these are summarised in [6]. On their own, n-type

[1] A hole is the absence of an electron in the outer electron shell.

and p-type materials do not achieve a great deal, but when formed adjacently they are able to work together and allow current to flow. The actual semiconductor devices that result from this will be discussed in Section 2.3. The resistivity (ρ), or conductivity (σ), of a doped semiconductor is expressed as (2.1)

$$\rho = \frac{1}{\sigma} = \frac{1}{q(\mu_n \cdot n + \mu_p \cdot p)} \qquad [\Omega \cdot \mathrm{m}] \tag{2.1}$$

where: μ_n is the electron mobility, μ_p is the hole mobility, n is the electron concentration, p is the hole concentration, and q is the charge of an electron ($1.602 \times 10^{-19}\ C$). The resistance of a semiconductor material is usually defined in terms of its sheet resistance ($R_\square$) and is expressed as (2.2)

$$R_\square = \frac{\bar{\rho}}{x_j} = (\bar{\sigma} \cdot x_j)^{-1} = \frac{1}{\int_0^{x_j} \sigma(x)dx} \qquad [\Omega/\square] \tag{2.2}$$

where: x_j is the junction depth. Resistance can then be expressed as (2.3)

$$R_{on} = \sigma \frac{L}{A} = \frac{\sigma}{t} \cdot \frac{L}{W} = R_\square \frac{L}{W} \qquad [\Omega] \tag{2.3}$$

where: A is the cross-sectional area of the semiconductor, t is the thickness, W is the width, and L is the length (as illustrated in in Figure 2.1).

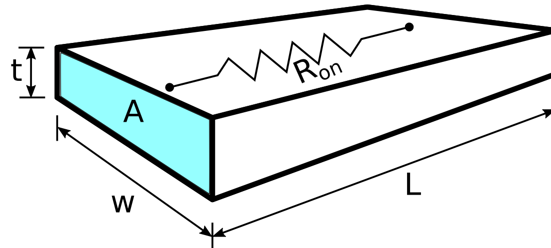


Figure 2.1: Semiconductor material resistance.

Doping a material is what gives it the ability to conduct due to either the surplus or lack of valence electrons. However, doping does not fully describe the performance of the material as a conductor or insulator. Two types of energy state bands exist in a material: the conduction band and the valence band, which are at different energy levels. For an electron to to be conducted, and hence result in current flow, it has to be able to transition from the valence band to the conduction band. When in the conduction band, charge carriers are free to move throughout the lattice structure of the material. The valence and conduction bands of metal, semiconductor, and insulator is illustrated in Figure 2.2. A metal, which is an excellent conductor, has the valence and conduction bands overlapping which results in the unimpeded flow of electrons. Conversely, insulating materials have an extremely large gap between these bands making it difficult for electrons to move from the valence band to the conduction band.

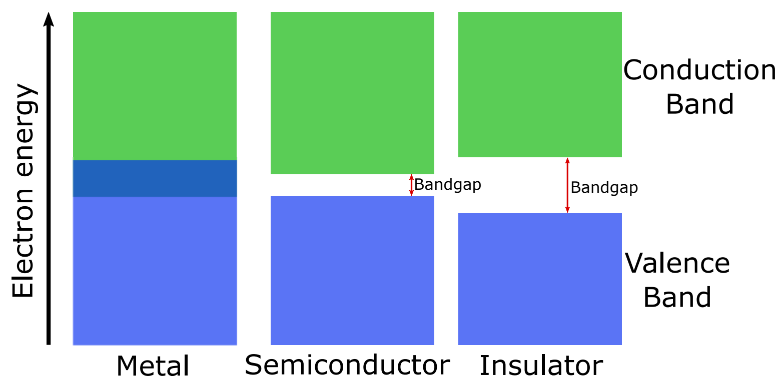


Figure 2.2: Conduction and valence bands of metal, semiconductor, and insulator materials.

The gap between these bands is called the bandgap and is quantified as the amount of energy required for an electron to be able to transition. Bandgap is measured in electron volts (eV), a unit of energy which is equal to 1.602×10^{-19} J. Semiconductors have a non-zero bandgap and this is what allows them to be able to switch between a conducting or insulating state. Si has a bandgap of 1.12 eV. Due to the constant push for efficiency and power density, newer Wide-Bandgap (WBG) materials (with a bandgap greater than 2 eV) have been emerging over

recent years which look to supersede Si as the semiconductor material of choice for the Power Electronic (PE) field [7]. The benefits of a larger bandgap will be discussed in the following section.

2.2.2 Wide-Bandgap Semiconductor Materials

	(units)	**Si**	**4H-SiC**	**GaN**	**Diamond**
Bandgap	(eV)	1.12	3.26	3.45	5.45
E_{crit}	(kV/cm)	300	2200	2000	10000
μ_n	(cm^2/Vs)	1500	1000	1250	2200
μ_p	(cm^2/Vs)	600	115	850	850
ϵ_r	-	11.9	10.1	9.0	5.5
BFoM	(Eqn:2.4)	1	500	2400	9000
JFoM	(Eqn:2.6)	1	410	790	5800
v_{sat}	(cm/s)	1×10^7	2×10^7	2.5×10^7	2.7×10^7
n_i	(cm^{-3})	1.4×10^{10}	8.2×10^{-9}	1.9×10^{-10}	1.0×10^{-22}
λ_T	(W/cmK)	1.5	4.9	1.3	22

Table 2.2: Notable properties of Si and WBG materials at 300K. BFoM and JFoM normalised to Si [1].

WBG materials have many benefits over their Si counterpart. Many materials are being investigated in semiconductor laboratories, however only a select few that are currently viable/in use will be considered, namely SiC and Gallium Nitride (GaN), with this thesis particularly focusing on SiC. SiC is a compound semiconductor made up of Si and Carbon (C), also in abundance, in a tetrahedral structure. There are over 250 polytypes of SiC that can be formed (due to variance in the manufacturing processes). However, three have received significant interest from the power electronics industry, namely 3C-SiC, 4H-SiC, and 6H-SiC. The majority of commercial SiC devices make use of the 4H-SiC polytype (bandgap of $3.62eV$ and high electron mobility of $\sim 1000\ cm^2/Vs$) [8], and thus will be the variant of SiC considered in this thesis. Table 2.2 shows some notable properties of Si along with the WBG materials SiC and GaN. Diamond, which is the theoretical limit of semiconductor materials, is also there for comparison.

The critical electric field (E_{crit}) is the maximum electric field that a device can support before avalanche breakdown. A higher value of E_{crit} allows devices to have a higher voltage blocking capability, with a higher level of doping concentration and smaller drift region, hence less resistance. Carrier mobility, both electron and hole (μ_n and μ_p respectively), is the speed at which carriers can move through the semiconductor. The dielectric constant ϵ_r of the material can cause unfavourable parasitic capacitances. Higher capacitances result in slower switching speeds of semiconductor devices. Baliga's Figure of Merit (BFoM) [9, 10] is a material parameter, expressed as (2.4)

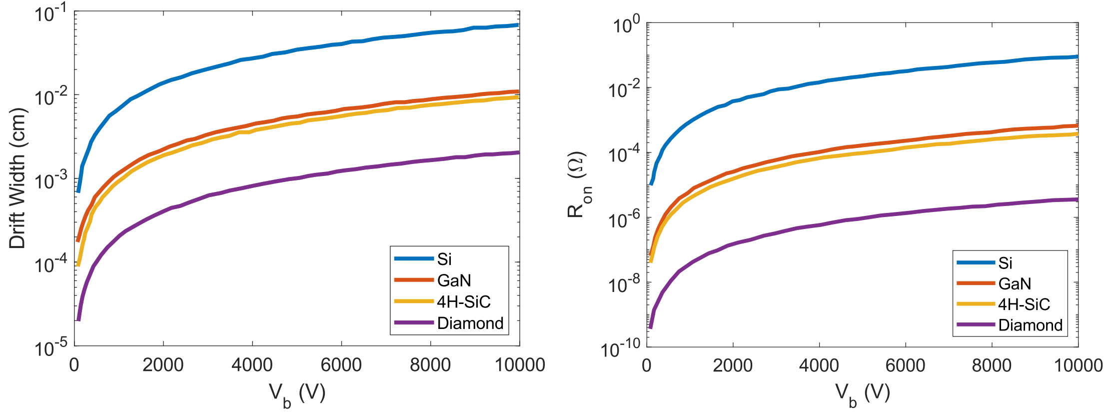
$$BFoM = \epsilon_r \cdot \mu_n \cdot {E_{crit}}^3 \tag{2.4}$$

It describes the fundamental relationship between on-resistance (R_{on}) and breakdown voltage (V_{br}), as seen in (2.5).

$$R_{on} = \frac{4 \cdot {V_{br}}^2}{\epsilon_0 \cdot BFoM} \qquad [\Omega] \tag{2.5}$$

A higher BFoM results in a lower resistance for a given V_{br}, or conversely, a similar resistance for an increase in V_{br}. Figure 2.3(b) is plotted using (2.5) and the data in Table 2.2. The superiority of WBG materials is evident in terms of resistance and voltage blocking capabilities. Johnson's Figure of Merit (JFoM) describes a semiconductor material's high-frequency and high-power capability [11]. It is a measure of a material's charge carrier saturation velocity (v_{sat}) and E_{crit}. JFoM is evaluated using (2.6)

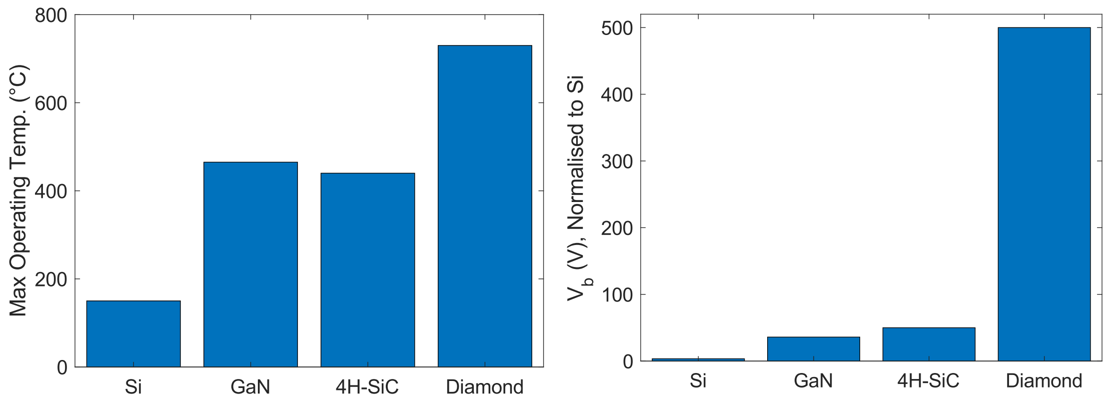
$$JFoM = \frac{{E_{crit}}^2 {v_{sat}}^2}{4\pi^2} \tag{2.6}$$



(a) Drift width against breakdown voltage (V_{br}).

(b) On-resistance against breakdown voltage (V_{br}).

Figure 2.3: Drift region width and on-resistance of Si and WBG semiconductors, digitised from [12].



(a) Maximum operating temperature.

(b) Maximum breakdown voltage (V_{br}). Materials at same doping density.

Figure 2.4: Maximum operating conditions of Si and WBG semiconductors, digitised from [12].

The saturated electron drift velocity (v_{sat}) is the speed at which a charge carrier, usually an electron, can move in a semiconductor when subject to a high electric field. A low intrinsic carrier concentration (n_i) of the intrinsic material allows for a higher level of doping. A higher level of doping results in a low resistance as shown in (2.1). The thermal conductivity (λ_T) is a measure of how readily heat can be removed from the semiconductor material. A higher thermal conductivity allows for a reduction in thermal resistance of the material and this in turn can enable higher power densities within a device.

It can be seen in Table 2.2 that the WBG materials significantly outperform Si in many areas. This is particularly apparent when considering the BFoM which shows orders of magnitude in difference. The maximum operating conditions of the four semiconductor materials are shown in Figure 2.4. These are theoretical numbers from the data in Table 2.2. To summarise, WBG semiconductor materials offer significant advantages over their traditional Si counterpart and are an important technological advancement for PE. In terms of what this actually means for the power devices fabricated using these new materials, the advantages are: higher breakdown voltages; higher current density; higher operating temperature; higher switching frequency; and most importantly, lower power losses [1]. How these advantages are realised, in terms of actual power semiconductor devices, will be discussed in Section 2.6.

2.3 Power Semiconductor Devices

This section will describe the operating mechanism of some power semiconductor devices. These devices can be classified into three groups [13] as shown in Table 2.3. Within these three device families there exists many different devices and device variants.

Device Family	Function
Diodes	The external circuitry turns the device on and off.
Transistors	Turned on and off by control signals.
Thyristors	Turned on by a control signal, can only be turned off by the external circuitry.

Table 2.3: Power semiconductor switching device families [13].

This thesis focuses on a selection of devices from the **diode** and **transistor** families, therefore Thyristors will not be discussed.

2.4 The Diode

A diode is the simplest of the semiconductor devices and is used widely in power conversion. It is a two-terminal device that only allows current to flow in one direction. It uses no control signals and requires the external circuitry to determine its operating mode. These devices are widely prevalent in power converters, either in uncontrolled rectification circuits (AC-DC) or in conjunction with transistors as a Freewheeling Diode (FWD).

2.4.1 Ideal Power Diode

Ideally, a power diode should be able to:

- block infinite voltage in one direction, with no leakage current.
- conduct infinite current in the other direction with infinitesimal impedance.
- transition between these two states instantaneously with no power loss or EMI.

However, a real diode is fabricated from semiconductor materials and does not exhibit these ideal qualities.

2.4.2 *pn* Junction

Most diodes are made from, or are a variant of, the most elementary semiconductor building-block: the *pn* junction. The *pn* junction is the fundamental architecture of semiconductor physics. It comprises *p*-type material and *n*-type material that have been fabricated adjacent to one another to form an abrupt

junction. This basic structure can be seen in Figure 2.5. At the junction of the device a depletion region, sometimes referred to as a space charge layer, is formed. This is formed due to diffusion of the electron and hole charge carriers across the junction. This diffusion of charge carriers results in an electric potential (E) gradient with no free charge carriers in the depletion region. In open-circuit (zero bias) conditions, the built-in potential (E_0) across the junction is expressed as (2.7)

$$E_0 = \frac{k \cdot T_j}{q} \cdot \ln\left(\frac{N_D \cdot N_A}{{n_i}^2}\right) \qquad [\mathrm{V}] \tag{2.7}$$

where: k is Boltzmann's constant ($1.38 \times 10^{-23}\ J/K$), T_j is the junction temperature in kelvin, q is the charge of an electron ($1.602 \times 10^{-19}\ C$), and N_D/N_A are the donors and acceptor impurity concentrations. For a standard Si *pn* junction, this potential is typically $\sim 0.7\ V$.

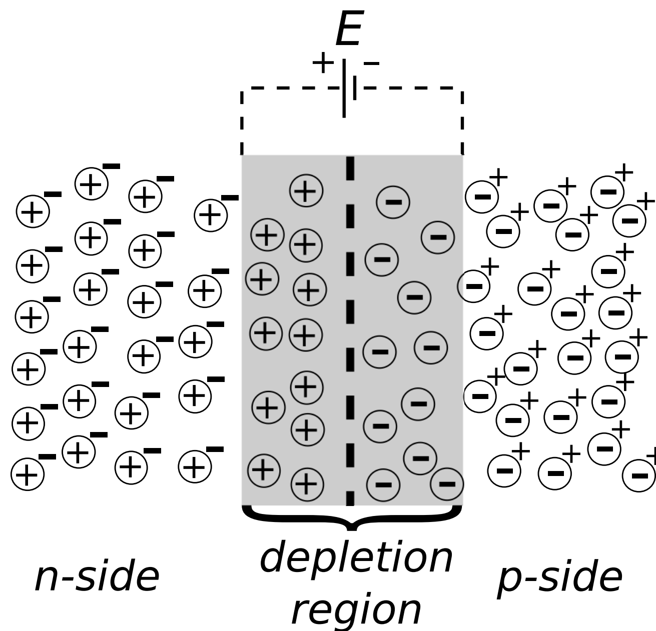


Figure 2.5: *pn* junction and depletion region. ⊕ positive donor ion, − free electrons, ⊖ negative acceptor ion, + holes.

2.4.3 *pn* Junction Diode

The circuit symbol and basic composition of the diode is shown in Figure 2.6a. The cathode is at the *n*-side of the device and the anode is at the *p*-side.

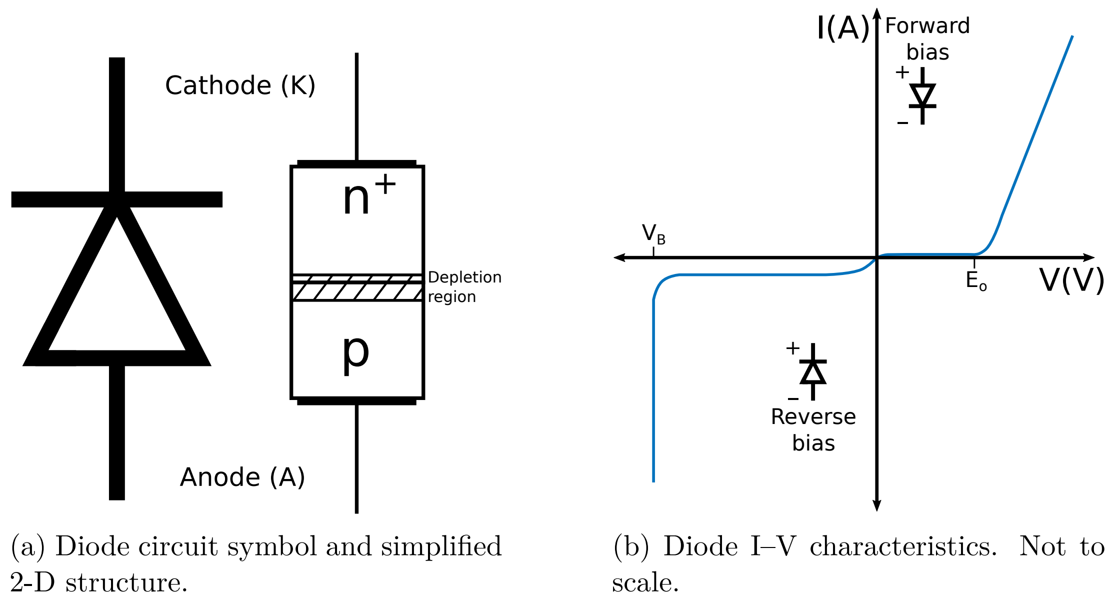
When **Forward Biased** (i.e. anode positive with respect to the cathode), current is able to flow in a bipolar manner, with majority carriers moving from the *p*-side to the *n*-side and minority carriers doing the opposite. Current is able to flow here due to the reduction in width of the depletion region which represents a low impedance path in the junction. This can be seen in the 1st quadrant of the IV characteristics in Figure 2.6b. E_0 is marked in this quadrant and shows that, regardless of the current level being conducted, the diode will always have at least this voltage drop across it - this is often termed the "knee voltage". The total on-state voltage drop (V_F) across the device also includes the resistive drop associated with the device's on resistance (R_{on}), as seen in the linear section of the 1st quadrant. The forward current through the diode can be expressed as (2.8)

$$I = I_s \cdot \left(e^{\frac{qV}{kT_j}} - 1 \right) \qquad [\mathrm{A}] \tag{2.8}$$

where: I is the total current flowing through the *pn* junction, I_s is the diode saturation current, and V is the voltage across the diode. However, the forward bias behaviour can be approximated using a Piece-Wise Linear (PWL) model, expressed as (2.9).

$$V_F(I_F) = E_0 + I_F \cdot R_{on} \tag{2.9}$$

The PWL approximation works well for steady-state circuit analysis, but fails to capture the details of the switching transients.



(a) Diode circuit symbol and simplified 2-D structure.

(b) Diode I–V characteristics. Not to scale.

Figure 2.6: *pn* Junction Diode.

When **Reverse Biased** (i.e. cathode positive with respect to the anode) the device behaves like an insulator. The positive voltage applied to the cathode attracts electrons away from the junction and, conversely, the holes are attracted away by the negatively charged anode. The net result of this is a small increase in the width of the depletion region. Ideally, under this reverse bias condition no current flows, however a small leakage current (in the order of μA) will flow through the junction. This reverse leakage current can be seen in the 3rd quadrant of Figure 2.6b. The breakdown voltage (V_{br}) is also marked, this is due to one of three phenomena: Avalanche breakdown, Zener breakdown or punch-through.

2.4.3.1 Semiconductor Breakdown

Avalanche Breakdown — This is the most common type of breakdown and occurs when the electric field in the depletion region exceeds a certain level due to the applied reverse biasing from the external circuitry. The minority carriers

associated with the reverse leakage current are accelerated to energy levels such that they begin to collide with bonded electrons, breaking them free. This in turn breaks more electrons free and the effect "avalanches". This large excess of carriers results in an extremely low impedance through the device.

Zener Breakdown (Tunnelling) — This happens when heavily doped junction regions, hence a small depletion region, are subject to a high reverse bias that causes a large electric field. Electrons can then tunnel through the device causing a large current when reversed bias. This is known as the Zener effect.

Punch-through — This happens when the depletion region widens under reverse bias such that it creates a short-circuit within the device.

In power electronics, breakdown usually results in a catastrophic failure if the external circuitry does not limit the current. However, for some applications, these breakdown characteristic can be useful, for example in Zener diodes which make use of the Zener effect to provide a clamping action.

2.4.4 Diode Transient Behaviour

The transition from forward biased state to reverse biased state, and vice versa, does not happen instantaneously and results in a non-ideal behaviour. These transitions are illustrated in Figure 2.7.

2.4.4.1 Turn-Off Transient: Forward Bias to Reverse Bias

This does not happen instantaneously due to excess charge carriers in the diode. At the start of the turn-off period, the diode is forward biased with current I_F flowing and a small non-zero on-state voltage V_F. When the polarity of voltage

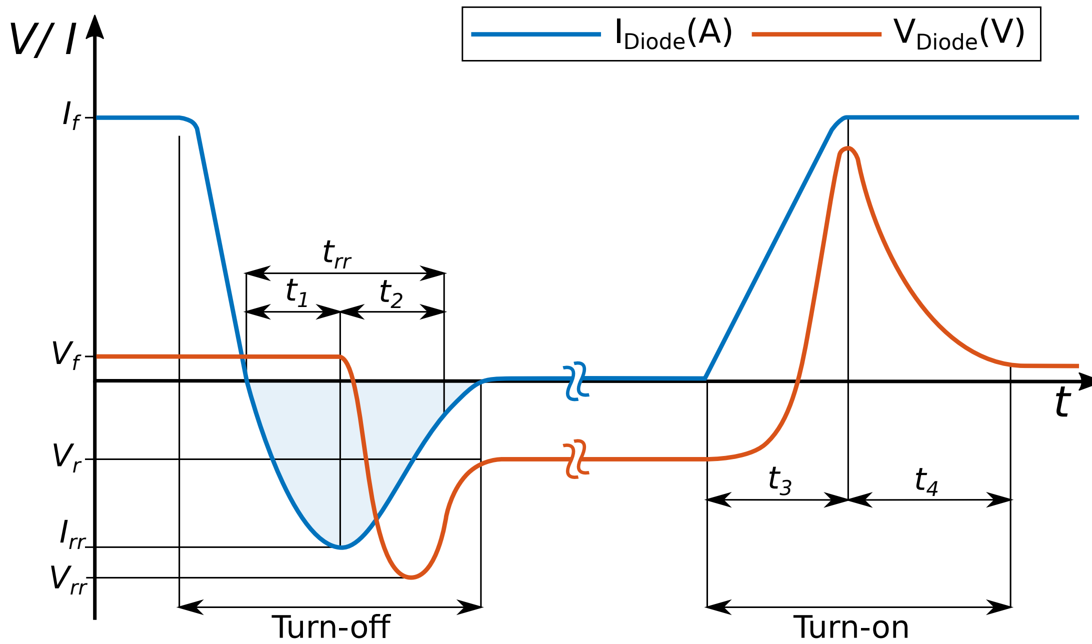


Figure 2.7: Turn-off and turn-on transients of diode. Not to scale.

across the devices is reversed, current begins to decay toward zero. The charge carriers have not yet recombined and result in a negative current due to the external potential, as seen in t_1. The diode voltage begins to rapidly decrease once the reverse current has reached it's maximum value I_{rr} which happens when the excess charge carriers have been swept out, resulting in an increase in depletion region width, hence increase in impedance. During t_2, current decreases back to zero, however the voltage reaches a peak V_{rr} due to stray inductance and the dI/dt. At the end of t_2 the diode is now reverse biased with the voltage at a certain value (set by the external circuit) and current is at 25 % of I_{rr}. The time period associated with this reversal of current is termed reverse recovery and is quantified as t_{rr}. This can also be further expressed as the amount of charge Q_{rr} (blue shaded area in Figure 2.7) due to the reverse recovery. These reverse recovery characteristics are important factors of a diode due to their high level of power loss and often electromagnetically noisy nature [14].

2.4.4.2 Turn-On Transient: Reverse Bias to Forward Bias

The forward biasing causes injection of carriers into the depletion region causing the diode to begin to conduct. The current rises slowly due to the gradual reduction in resistance of the diode and also due to the parasitic inductance. This inductance and the dI/dt of the on-state current edge cause an overshoot in voltage. The voltage then reduces back down to the non-zero on-state voltage V_F.

2.4.5 Power Diodes

Many different variants and derivatives of diodes exist across the electronics field. However, there are specific ones used for processing power:

2.4.5.1 General Purpose *pn* Diode

These are standard Si-*pn* junction diodes that are typically used for basic rectification of low-voltage at 50/60 Hz. They have a large t_{rr} and are optimised primarily for conduction loss, therefore not normally used in Switched-Mode Power Supply (SMPS) due to high levels of switching loss.

2.4.5.2 *pin* Diode

A small intrinsic layer of semiconductor can be used between the *p*-type and *n*-type layers. This results in a wider depletion layer, therefore less parasitic capacitance. The main benefit of the *pin* structure is a higher V_{br} due to the reduction in electric field strength at the junction. This arises from the electric field being spread over a wider depletion region.

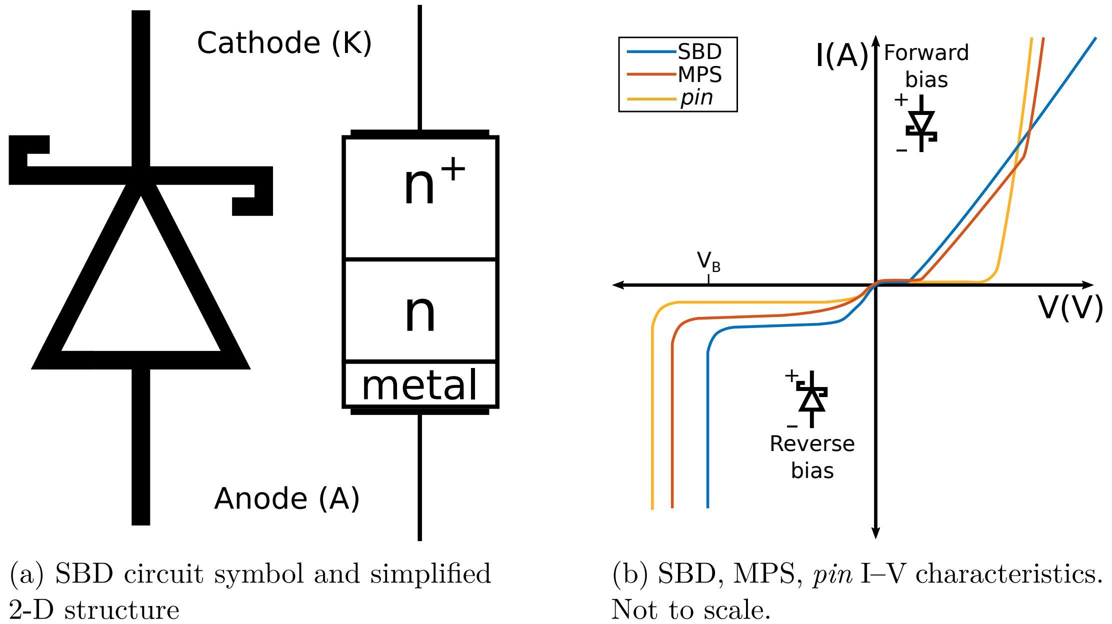
2.4.5.3 *pn/pin* Fast Recovery Diode (FRD)

In order to achieve high levels of voltage breakdown capability with low on-state resistance, device manufacturers have to balance complex geometry and doping concentrations of the *p*-side and *n*-side. This results in high levels of t_{rr} and turn-on time. The Fast Recovery Diode (FRD) is an evolution of the general purpose Si diode with, as the name suggests, a lower t_{rr} and faster turn-on time. This is done by reducing the amount of stored charge in the device as well as a reduction in carrier lifetimes. Small amounts of Gold or Platinum are diffused into the semiconductor as they provide additional carrier recombination zones and thus reduce the overall carrier lifetime. This results in a faster t_{rr}, but increases leakage current and on-state resistance. The FRD is a very common device in the power conversion industry.

2.4.5.4 Schottky Diode

Schottky Barrier Diode (SBD) — The Schottky Barrier Diode (SBD) has significant advantages over *pn/pin* diodes. It is a metal-semiconductor based diode that achieves better on-state voltages at low currents and very fast switching transients, with essentially no reverse recovery due to its unipolar majority carrier conduction mechanism. The Si variant is limited in reverse blocking voltage capabilities, but this is overcome by SiC utilisation. The SBD comprises a metal interfaced with an *n*-type semiconductor, as illustrated in Figure 2.8a. The barrier metals used are typically molybdenum, tungsten, palladium or chromium. As this is not a semiconductor-semiconductor interface it does not operate like the typical *pn/pin* device. Instead, the reverse and forward bias properties are dependant on the Schottky barrier height of the metal-semiconductor junction. This barrier height is akin to the junction potential of a *pn* diode, in terms of its effect on

forward characteristics. However, it can be as low as $\sim 0.1\ V$, much lower than a *pn* diode.



(a) SBD circuit symbol and simplified 2-D structure

(b) SBD, MPS, *pin* I–V characteristics. Not to scale.

Figure 2.8: Schottky Diode.

When **Forward Biased**, electrons (majority carriers) move from the negatively charged *n*-region at the cathode side to the positively charged metal at the anode side. Unlike a *pn* junction, holes do not pass over this potential barrier. When **Reversed Biased**, the SBD has higher levels of leakage current than its *pn* counterpart. The barrier height is effectively inversely proportional to leakage current — low barrier voltage drop results in more leakage current.

The I–V characteristics of the SBD, compared to that of the *pin* diode, are shown in Figure 2.8b. It can be seen that at higher currents the *pin* diode has lower conduction loss, whereas at lower currents the SBD performs better. The forward current of the SBD is made up of electron diffusion current, thermionic emission current, and tunneling current. As there is no *p*-type semiconductor in the device, there are no minority carriers involved in the forward conduction. This results in essentially no reverse recovery when transitioning to reverse bias, which is a very attractive feature [15]. There is, however, a parasitic *pn* diode

formed by a p-type guard-ring that is often used in high-voltage devices to improve robustness [16]. This can contribute some reverse recovery characteristics to the SBD. One of the contributing factors to high leakage current in the SBD is surface defects at the singular metal-semiconductor interface that are subjected to high electric field levels.

Junction Barrier Schottky (JBS) Diode — In an effort to reduce the metal-semiconductor surface defect issues in the SBD, the Junction Barrier Schottky (JBS) was proposed [17]. This evolution of the Schottky diode involves adding regularly spaced p^+-wells beneath the interface (in a grid type formation) to protect the device under reverse bias. This forms depletion regions below the p^+-wells, reducing the electric field stress on the metal-semiconductor interface. This in turn reduces leakage current.

Merged PIN Schottky (MPS) Diode — The Merged PIN Schottky (MPS) diode combines a Schottky structure with a *pin*-structure and is a further evolution of the JBS diode [18]. The Schottky part allows for a low built-in voltage drop, fast switching transients and low reverse recovery. The *pin*-structure results in good reverse blocking and a better overall forward conduction profile. This can be seen in the I–V characteristics in Figure 2.8b. The MPS is often considered to be a hybrid unipolar/bipolar device [19] and tends to be the preferred Schottky structure.

2.5 The Transistor

Transistors are semiconductor switches that have a more complex structure than a diode and can be turned on and off by an external control signal.

2.5.1 Ideal Power Switch

Ideally, a power switch should be be able to:

- block infinite voltage when off.
- conduct infinite current with infinitely low impedance when on.
- transition between these two states instantaneously with no power loss or EMI.

However, just like a diode, they are fabricated from semiconductor materials and do not have these ideal characteristics. Many different types exist and are used in a variety of different applications from: high-speed digital circuitry; high-speed analogue and Radio Frequency (RF) circuits; to the high-power circuits in power conversion. Two main transistor variants are used in power conversion and these will be the focus of this thesis, they are:

- Metal–Oxide–Semiconductor Field-Effect Transistor (MOSFET)
  - Unipolar Transistor, i.e. uses only one type of charge carrier
- Insulated-Gate Bipolar Transistor (IGBT)
  - Bipolar Transistor, i.e. uses both charge carriers

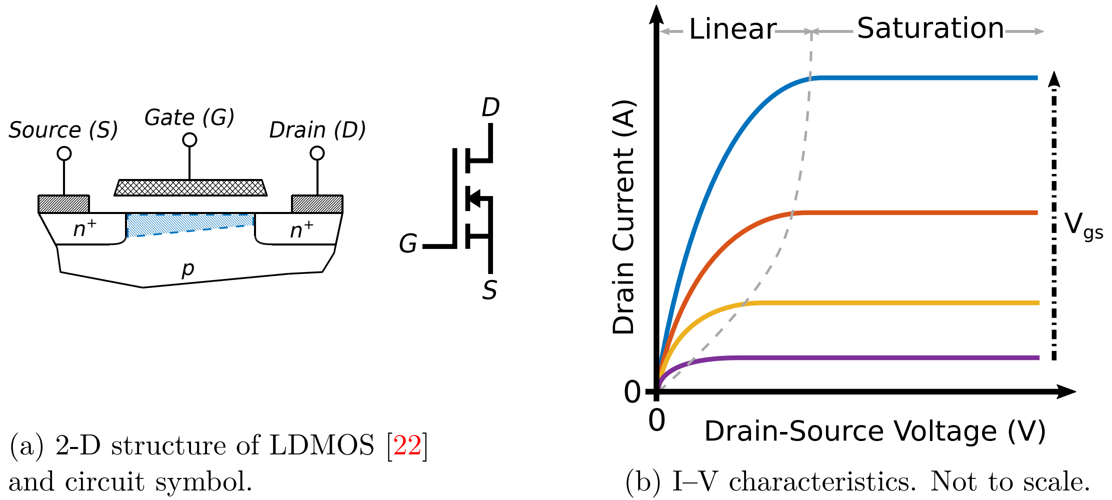
2.5.2 Metal–Oxide–Semiconductor Field-Effect Transistor (MOSFET)

The use of the MOSFET in power conversion was made possible by significant advances in the Integrated Circuit (IC) industry, with Si based MOSFET and Complementary Metal-Oxide-Semiconductor (CMOS) technology being extensively used since its invention in 1960 [20]. The form that is typically used in power converters is the *n*-channel enhancement-mode device [21]. This is due to favourable characteristics which are most suited to power conversion circuits, a normally-off device which requires a positive control signal. *p*-channel devices, which are normally-on, are not as common in power conversion circuits as this is not often a useful feature. The *n*-channel enhancement-mode MOSFET will be hereinafter considered the MOSFET.

The basic structure of a Laterally Diffused MOSFET (LDMOS) can be seen in Figure 2.9a. A lightly doped *p*-type substrate is used with two n^+-regions diffused to make the source and drain. A thin layer of Silicon Dioxide is used to insulate the metalised gate connection from the semiconductor. This is termed the gate-oxide. This Metal–Oxide–Semiconductor (MOS) structure that is formed is effectively a capacitor. The source and drain connections are classed as the power terminals (the points of the device connected to external power circuit) and the gate connection is the control signal which is controlled by a gate-driver (gate-drivers will be discussed more in Section 3.4.2).

As this is a normally-off device, no current will flow between the drain and source terminals. There are, however, two *pn* junctions formed between the *p*-region and the n^+-regions, but as they oppose each other no current flows. To turn the device on, a positive voltage is applied to the gate (with respect to the

source) which creates positive charge in the metal. This in turn induces negative charges in the p-type Si directly beneath the gate. This area of negative charge (blue dashed line illustrated in Figure 2.9a) is often called an inversion layer or channel and has mobile electrons which allow current to flow between the source and the drain. This phenomenon is termed the Field Effect, which leads to the Field-Effect Transistor (FET) terminology.



(a) 2-D structure of LDMOS [22] and circuit symbol.

(b) I–V characteristics. Not to scale.

Figure 2.9: Metal–Oxide–Semiconductor Field-Effect Transistor (MOSFET).

The I–V characteristics of the MOSFET can be seen in Figure 2.9b. It can be seen that with an increase in gate-source Voltage (V_{gs}), the MOSFET conducts more current. To fully turn the MOSFET on, or saturate it, typically $V_{gs} = 15 - 20V$. An important parameter for these devices is the Threshold Voltage (V_{Th}), which is the minimum voltage required to begin to turn a MOSFET on. As seen in Figure 2.9b, there are two distinct operating regions; the linear region and the saturation region. In the linear region the drain current (I_d) can be expressed as (2.10)

$$I_d = \mu_n C_{ox} \frac{W_C}{L_C} \left[(V_{gs} - V_{Th})V_{ds} - \frac{{V_{ds}}^2}{2} \right] \quad [\text{A}] \tag{2.10}$$

where: W_C is the width of the channel (in the z-plane not shown in Figure 2.9a),

L_C is the channel length between the drain and source regions, C_{ox} is the capacitance (per unit area) of the gate oxide, and V_{ds} is the voltage across the drain-source terminals of the MOSFET. The dashed line on Figure 2.9b represents the "pinch-off" voltage, whereby V_{ds} reaches the override voltage as expressed in (2.11)

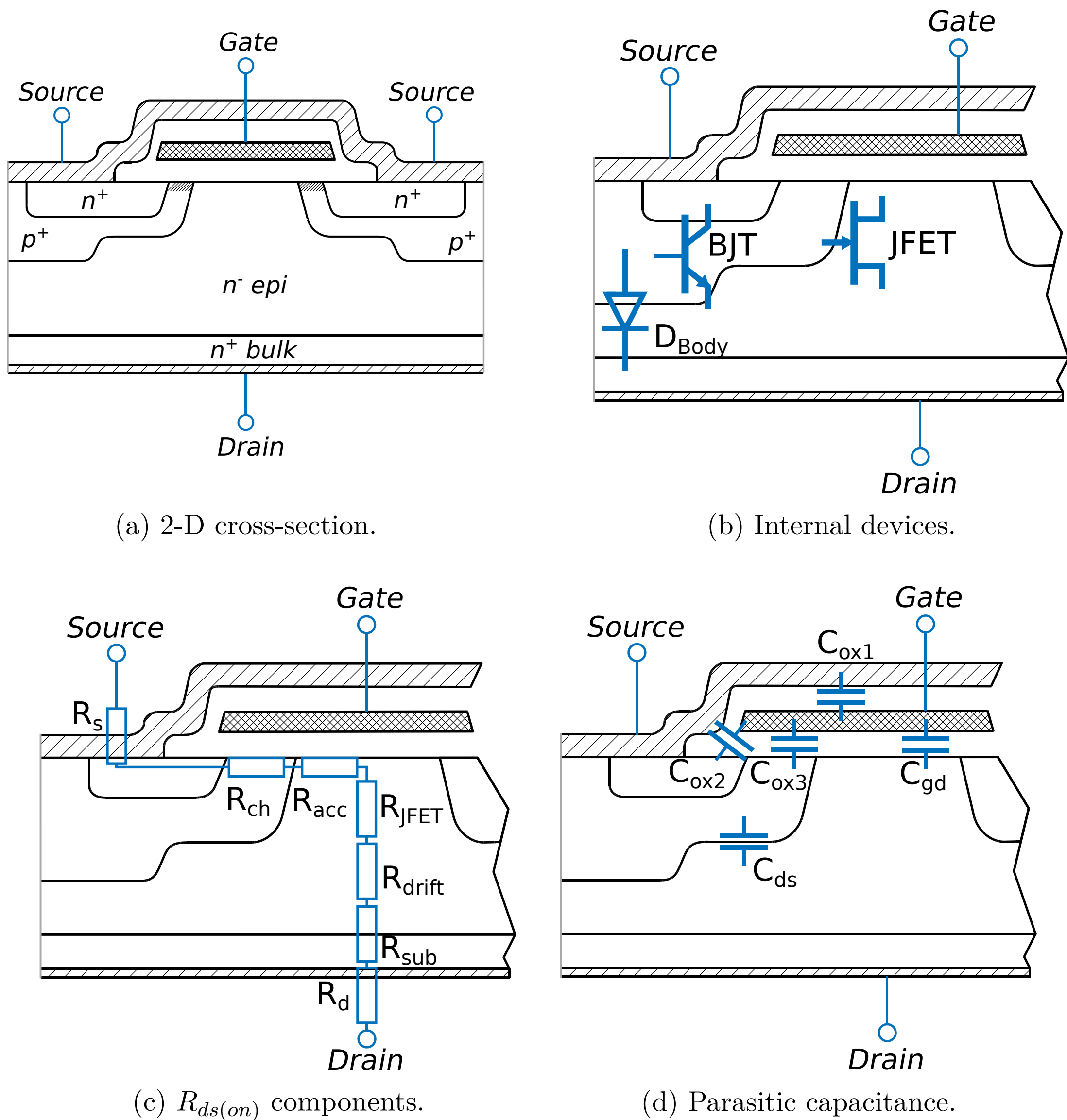
$$V_{ds} = V_{gs} - V_{Th} \qquad [\mathrm{V}] \tag{2.11}$$

At this stage, the channel of the MOSFET exhibits pinch-off effect and the device is in the saturation region. I_d is now limited by the device and can be expressed as (2.12)

$$I_{d,sat} = \mu_n C_{ox} \frac{W_C}{L_C} \left[\frac{V_{gs} - {V_{Th}}^2}{2} \right] \qquad [\mathrm{A}] \tag{2.12}$$

2.5.2.1 MOSFET Device Structure

The LDMOS (Figure 2.9a) works well for high-voltage devices, but is not a good utilisation of semiconductor area for high-current devices [21]. Therefore, vertically structured devices have proven to be a better fit for high-power applications. A vertical MOSFET structure is shown in Figure 2.10a. This device is commonly referred to as a Vertical Double-Diffused MOSFET (VDMOS). Double diffusion is required for the double well structure (n^+-well within p^+-well). The VDMOS was first released by Hitachi in 1969. The current flows vertically from the drain to the source when a positive voltage V_{gs} is applied. It can be seen in Figure 2.10b that there is a parasitic diode formed between the p^+ implanted region and the n^- epi layer; this is called the body diode. This diode does not pose as a negative



(a) 2-D cross-section.

(b) Internal devices.

(c) $R_{ds(on)}$ components.

(d) Parasitic capacitance.

Figure 2.10: Vertical Double-Diffused MOSFET (VDMOS) [23].

trait to device behaviour as the majority of circuit topologies benefit or rely on it for operation. Most packaged devices actually include an additional diode (the FWD) in parallel with the body diode. There is also a parasitic NPN Bipolar Junction Transistor (BJT) that arises from construction of the MOSFET. It is effectively disabled by having its emitter and base shorted. It can, however, be susceptible to turn-on from high dV/dt and capacitive coupling [24] or by reverse recovery from the body diode. If the BJT is turned on it can cause device breakdown in the form of a short-circuit from the drain to the source. A Junction

Field-Effect Transistor (JFET) is also present in the epitaxial n^- layer which contributes to the device resistance by limiting, or pinching, current flow [24].

The on-state resistance ($R_{ds(on)}$) can be expressed as (2.13). This series resistance is shown in Figure 2.10c.

$$R_{ds(on)} = R_s + R_{ch} + R_{acc} + R_{JFET} + R_{drift} + R_{sub} + R_d \qquad [\Omega] \tag{2.13}$$

where: R_s and R_d are the resistive components associated with the ohmic contacts and metalised connections; R_{ch} is the channel resistance which is modulated by V_{gs} and makes up the biggest quantity of $R_{ds(on)}$; R_{acc} is the accumulation resistance of the epitaxial layer directly under the gate where the current changes direction from lateral to vertical conduction; R_{JFET} is the resistive element of the JFET pinching; R_{drift} is the bulk epitaxial-layer resistance, often called the drift region resistance; and R_{sub} is the substrate layer resistance. The $R_{ds(on)}$ of a MOSFET has a positive temperature coefficient, therefore, an increase in T_j will result in an increase in $R_{ds(on)}$.

As illustrated in Figure 2.10d, multiple parasitic capacitive elements exist within the MOSFET structure and these are what severely impact the switching performance of the device. These can be seen as the drain-source capacitance (C_{ds}), the gate-drain capacitance (C_{gd}), and the gate-source capacitance ($C_{gs} = C_{ox1}+C_{ox2}+C_{ox3}$). When manufacturers list these as datasheet values they do not list them as such. Instead, they are commonly referred to as the input capacitance (C_{iss}), the output capacitance (C_{oss}), and the reverse transfer capacitance (C_{rss}).

These are defined as (2.14), (2.15), and (2.16).

$$C_{oss} = C_{ds} + C_{gd} \qquad [\text{F}] \tag{2.14}$$

$$C_{iss} = C_{gd} + C_{gs} = C_{gd} + (C_{ox1} + C_{ox2} + C_{ox3}) \qquad [\text{F}],\ C_{ds} \text{ shorted} \tag{2.15}$$

$$C_{rss} = C_{gd} \qquad [\text{F}] \tag{2.16}$$

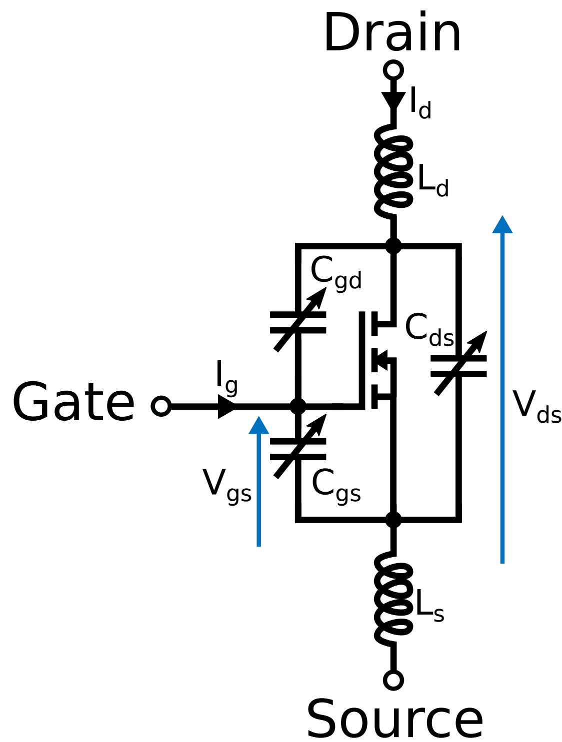


Figure 2.11: Parasitic capacitance and inductance of MOSFET.

The capacitances C_{oss}, C_{iss} and C_{rss} are all non-linear, voltage-dependant capacitances. Power devices have to be physically big to be able to block high-voltages and withstand high-current magnitude, therefore these capacitances can become quite large. These capacitances are illustrated in Figure 2.11. There is also parasitic inductance (L_d & L_s) associated with the device connections which

adversely affects switching performance.

2.5.2.2 MOSFET Transient behaviour

The turn-on and turn-off transients of the MOSFET are shown in Figure 2.12. The upper plot shows the gate-source voltage (V_{gs}), the gate current (I_g), and the external gate-drive voltage (V_g). The lower plot shows the drain-source voltage (V_{ds}) and the drain current (I_d). The blue shaded areas, where there is both V_{ds} and I_d simultaneously, are the switching losses.

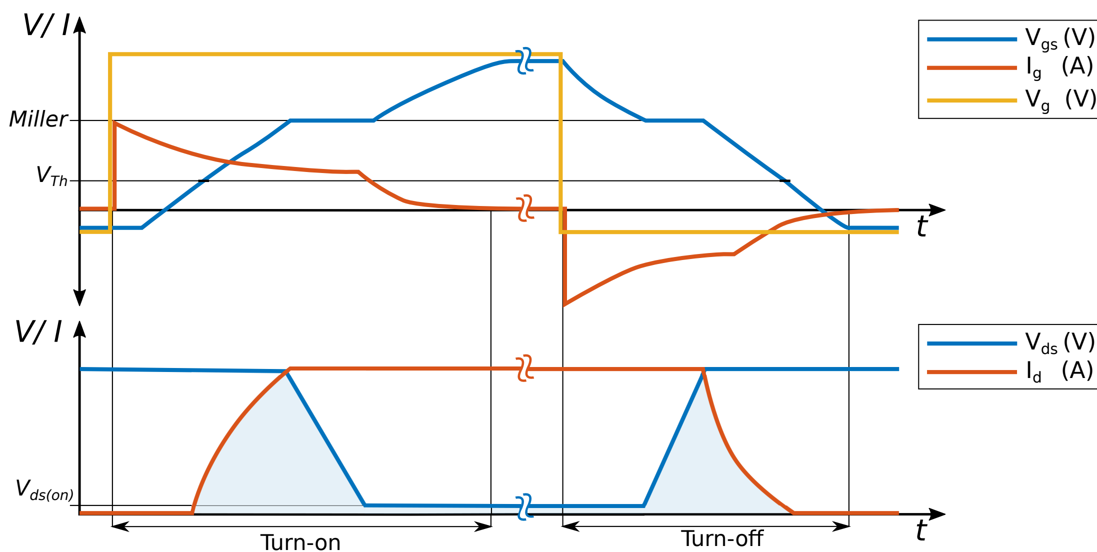


Figure 2.12: Turn-off and turn-on transients of MOSFET. Not to scale.

MOSFET Turn-On Process — The turn-on transient begins with the step voltage from the external V_g. As the MOSFET V_{gs} is at zero (or negative voltage), current rapidly flows into C_{gs} until $V_{gs} = V_{Th}$. At this point I_d begins to rise exponentially to the load current (I_L) magnitude. Once $I_d = I_L$, V_{ds} begins to fall linearly toward the on-state voltage ($V_{ds(on)}$). The **Miller effect** happens during this stage, as illustrated in Figure 2.12. This is where C_{gd} exhibits a feedback current from the falling V_{ds}, resulting in a plateau of V_{gs}. This feedback current is sourced from I_g. The MOSFET is fully on when $V_{ds} = V_{ds(on)}$.

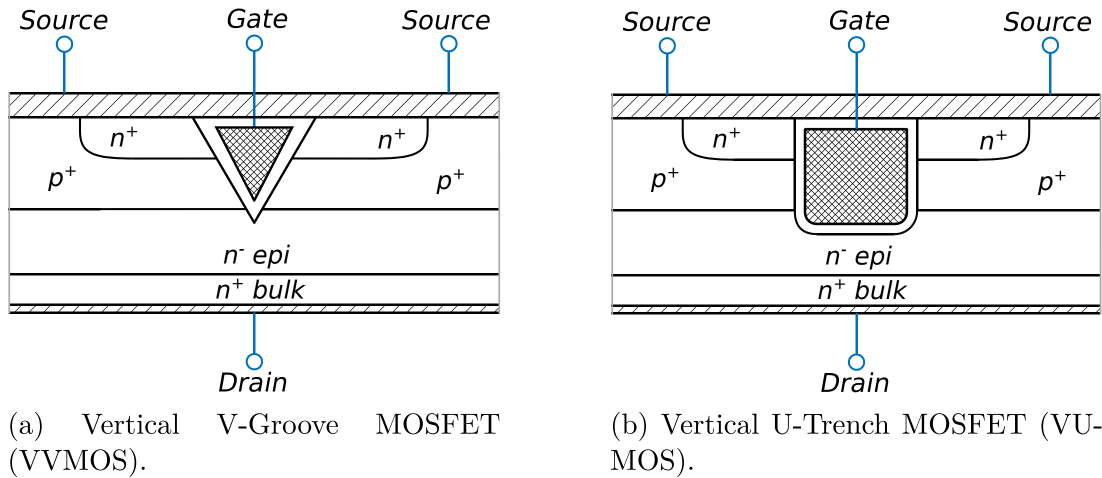
MOSFET Turn-Off Process - At the start of this turn-off process, the MOSFET is fully on and conducting current. When the gate-drive V_g goes to zero (or negative), V_{gs} falls exponentially to the Miller plateau. As the Miller capacitance is discharged via I_g, V_{ds} begins to linearly rise. Once V_{ds} is at the supply rail voltage, I_d falls exponentially toward zero.

The speed at which the MOSFET can turn on and off is directly related to the magnitude of the parasitic capacitors, in particular C_{iss} and C_{rss} (or Miller capacitance). The total gate-charge (Q_{gs}) is the amount of charge, at a given V_{gs}, that is required to be injected into C_{gs} to turn the MOSFET on. The smaller the required Q_{gs} is, the faster the switching speed and hence lower switching losses. In order to achieve a low Q_{gs} a MOSFET die can be constructed with less area, however a smaller die will have a larger $R_{ds(on)}$. These are the conflicting relations that device manufactures have to deal with.

2.5.2.3 MOSFET Discussion

The Si-based power MOSFET has undergone many iterations in an attempt to achieve a better electrical performance in terms of switching speed, on resistance, current capacity, and V_{br} capability. An interesting example of this is the trench-gate MOSFET (shown in Figure 2.13b) which is now a standard geometry in MOSFET fabrication. [24, 25].

Trench-Gate MOSFET — Here, the gate structure is implanted deep into the device structure, as illustrated in Figure 2.13. The trench MOSFET has been widely discussed in the literature and is summarised in [24]. The benefit of implanting the gate is the vast reduction in R_{acc} and the removal of R_{JFET}. The first commercial device using such a geometry was the Vertical V-Groove



(a) Vertical V-Groove MOSFET (VVMOS).

(b) Vertical U-Trench MOSFET (VU-MOS).

Figure 2.13: 2-D cross-section of trench-gate MOSFET structures [26].

MOSFET (VVMOS) (shown in Figure 2.13a) by Siliconix in 1974 [21]. This device was named the TrenchFET. The VVMOS was the first power MOSFET to achieve sub-micrometer channel widths [27]. However, high electric field stress at the tip of the "V" meant further refinement of the trench technique was required. Corners must be rounded to avoid these high stresses. The VVMOS was evolved, first by truncating the tip of the "V" resulting in a larger angle, then into a "U" shaped trench. This is termed the Vertical U-Trench MOSFET (VUMOS) and an illustration of this is shown in Figure 2.13b. The VUMOS structure achieves a low $R_{ds(on)}$, however by extending the gate structure into the drift region (n^- epitaxial layer), C_{gd} increases. This increases the Q_{gs} and switching transient time, therefore resulting in higher switching losses than the LDMOS. The additional fabrication steps required also increase the cost of trench style MOSFETs compared to the LDMOS. Many more variances of the trench MOSFET exist and are widely reported in the literature both by researchers and device manufacturers [24].

The relationship between V_{br} and $R_{ds(on)}$ for a conventional Si unipolar transistor is given by Equation (2.17), as reported in [28] — this is often termed the Si limit.

$$R_{ds(on)} \cdot Area \propto {V_{br}}^{2.4-2.6} \tag{2.17}$$

The vertical Si-MOSFETs discussed so far have a maximum V_{br} of circa 650 V, at least for a sensible $R_{ds(on)}$. While maintaining the same V_{br}, a reduction in $R_{ds(on)}$ of approximately one order of magnitude is achieved by the Superjunction MOSFET (SJMOS) [29].

Superjunction MOSFET (SJMOS) — In the conventional VDMOS, the electric field intensity (when blocking voltage) is highest at the pn interface and then decreases throughout the epitaxial layer down to the substrate. This makes E_{crit} easy to exceed at the pn interface. The SJMOS, which was first proposed in 1978 (illustrated in Figure 2.14), has columns of p-type Si which sit beneath the p^+-region allowing the electric field to be uniformly spread along this new pn interface [30, 31]. This allows for a reduction in the n^--drift region hence a lower $R_{ds(on)}$ for a specific V_{br}. This also results in substantially reduced C_{rss} and C_{iss} for a given area. Careful balancing of the additional charge that arises from these columns is required, with many approaches and subtle changes in geometries reported [24]. This technology has been most notably pioneered by Infineon with their CoolMOS™ (SJMOS) devices which they first brought out in 1998 [31, 32]. The SJMOS allows the Si unipolar $R_{ds(on)}$—V_{br} relationship to be more linear [33]. The SJMOS has substantially more fabrication steps (up to 16) than the conventional VDMOS and VVMOS (up to 6) making it a more complex and costly device to make [5].

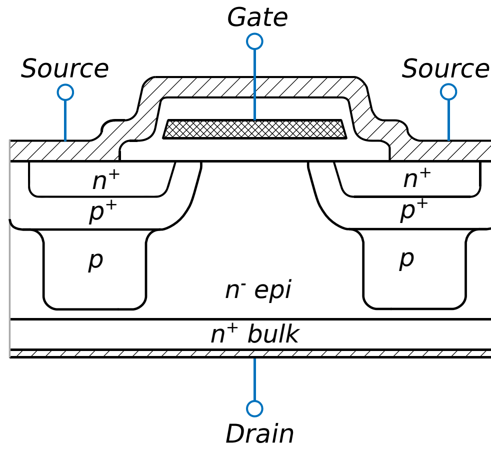


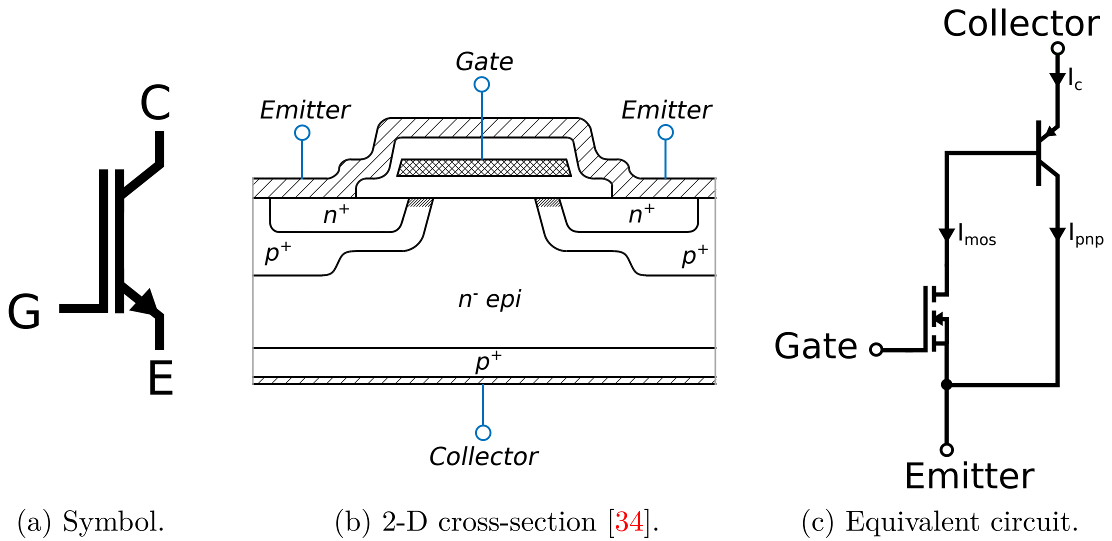
Figure 2.14: 2-D cross-section of Superjunction MOSFET structure [23].

In order to maintain a low $R_{ds(on)}$ which is necessary in efficient power conversion, conventional Si-MOSFETs are limited to $\sim 600\ V$ and Si-SJMOS devices are able to achieve $\sim 900\ V$. This is not high enough for high-power applications.

2.5.3 Insulated-Gate Bipolar Transistor (IGBT)

The high-voltage Si-Bipolar Junction Transistor (BJT) is able to conduct large currents with a very low on-state voltage. However, due to its poor switching behaviour and continuous base current driving mechanism, it is not a useful device for power conversion applications. The Insulated-Gate Bipolar Transistor (IGBT) combines the BJT on-state performance with the high impedance MOS gate structure and some of the switching performance of the MOSFET. The circuit symbol for the IGBT is shown in Figure 2.15a with the collector, emitter, and gate terminals.

The IGBT is realised by implanting a p^+-region at the drain area of the conventional n-channel VDMOS, as shown in Figure 2.15b. The operation of the IGBT is very similar to a conventional power MOSFET, requiring a positive gate-emitter voltage (V_{ge}) in order to turn the device on, and a negative (or zero)



(a) Symbol. (b) 2-D cross-section [34]. (c) Equivalent circuit.

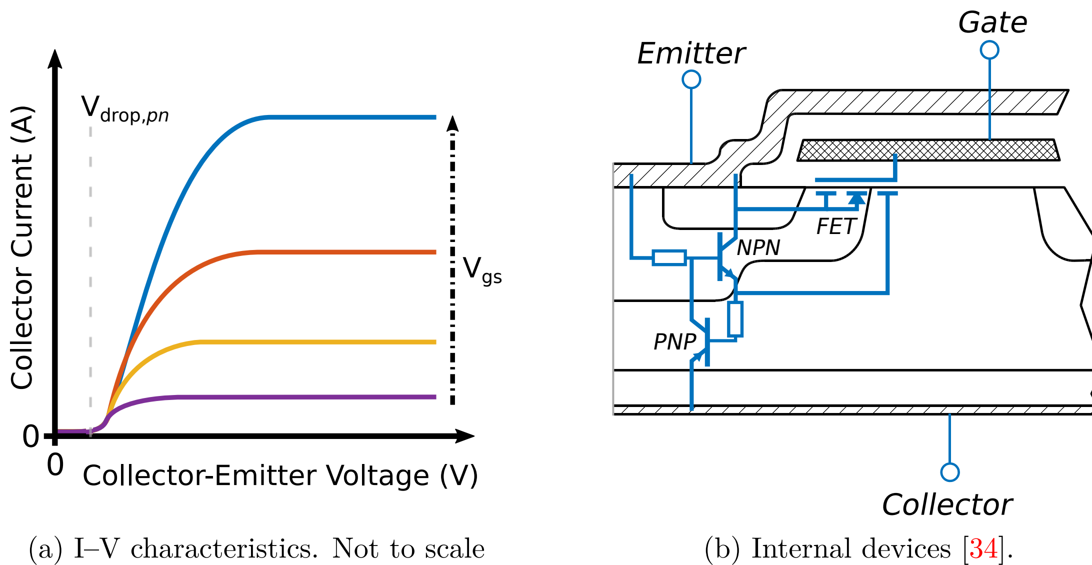
Figure 2.15: Insulated-Gate Bipolar Transistor (IGBT).

V_{ge} to turn it off. However, the inner operating principles are quite different. The equivalent circuit that is produced, shown in Figure 2.15c, comprises a Darlington arrangement of the *pnp* BJT and MOSFET, where the base current of the BJT is controlled by the MOSFET. The collector current (I_c) is made of two components: the MOSFET unipolar current (I_{mos}) which uses electrons; and the BJT bipolar current (I_{pnp}). The total collector current can be expressed as (2.18)

$$I_c = I_{mos}(1 + \beta_{pnp}) \qquad [\text{A}] \tag{2.18}$$

where: β_{pnp} is the BJT current gain. It is the bipolar conduction that allows for high-current, low on-state resistance devices that are capable of realising high levels of V_{br}. Specifically, this is due to the significant reduction in drift region (n^- epi) resistance because of increased conductivity modulation that arises from the high level of minority carrier holes that are injected [35]. The conductivity-modulated drift region is often termed the Charge Storage Region (CSR).

The I–V characteristics of the IGBT are shown in Figure 2.16a. The major difference between these characteristics and those of the MOSFET (Figure 2.9b)



(a) I–V characteristics. Not to scale

(b) Internal devices [34].

Figure 2.16: Insulated-Gate Bipolar Transistor (IGBT).

is the diode voltage drop ($V_{drop,pn}$) offset, which is typically $\sim 0.7\ V$. This arises from the pn-junction of the collector p^+-region and the n^- epitaxial drift region which is the collector-base regions of the pnp BJT. This series configuration of pn diode and MOSFET is the common way the conduction characteristics of the IGBT are considered. The MOSFET pinch-off effect, that was discussed in Section 2.5.2, holds true for the IGBT where I_c becomes saturated.

The parasitic npn BJT that exists in the MOSFET is also present in the IGBT, this is illustrated in Figure 2.16b. This non-ideal device is coupled with the pnp BJT section creating a parasitic $pnpn$ Thyrsitor. This Thyrsitor is able to latch on (turn on) if the necessary BJT gain conditions are met, resulting in a device failure [36]. This phenomenon, termed "latch-up", can happen: statically, when current density exceeds a critical level in the on-state; and dynamically, when the collector-emitter voltage (V_{ce}) rises during device turn-off and the depletion region widens [37]. As BJT gains vary with temperature, latch-up is temperature dependant. In the early days of IGBT development, latch-up caused serious issues. Extensive work was carried out on these first generation devices in the 1980s to overcome these issues [38–41], leading to the release of the first

commercial non-latch-up IGBTs by Toshiba in 1985. The parasitic JFET resistance present in the MOSFET is also an issue in IGBTs. This can be managed by better geometrical design of the gate structure, similar to the trench-gates discussed in Section 2.5.2.3. As illustrated in Figure 2.17 the input, output and Miller (reverse transfer) capacitances for the IGBT are defined as

$$C_{oss} = C_{ce} + C_{gc} \qquad [\mathrm{F}] \tag{2.19}$$

$$C_{iss} = C_{gc} + C_{ge} \qquad [\mathrm{F}],\ C_{ce} \text{ shorted} \tag{2.20}$$

$$C_{rss} = C_{gc} \qquad [\mathrm{F}] \tag{2.21}$$

These capacitances affect the transient behaviour of the IGBT in a similar manner to the MOSFET.

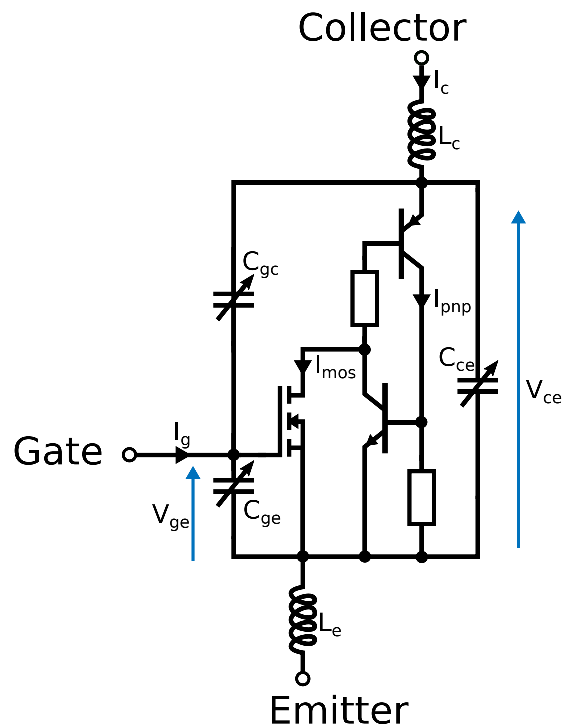


Figure 2.17: IGBT internal devices and parasitic elements.

2.5.3.1 IGBT Transient behaviour

IGBT Turn-On Process — The turn-on transient of the IGBT is very similar to that of the MOSFET shown in the "turn-on" section of Figure 2.12. The turn-on dI/dt and dV/dt values are, however, lower for a similarly rated device due to the required injection of holes (minority carriers) in the *pnp* BJT.

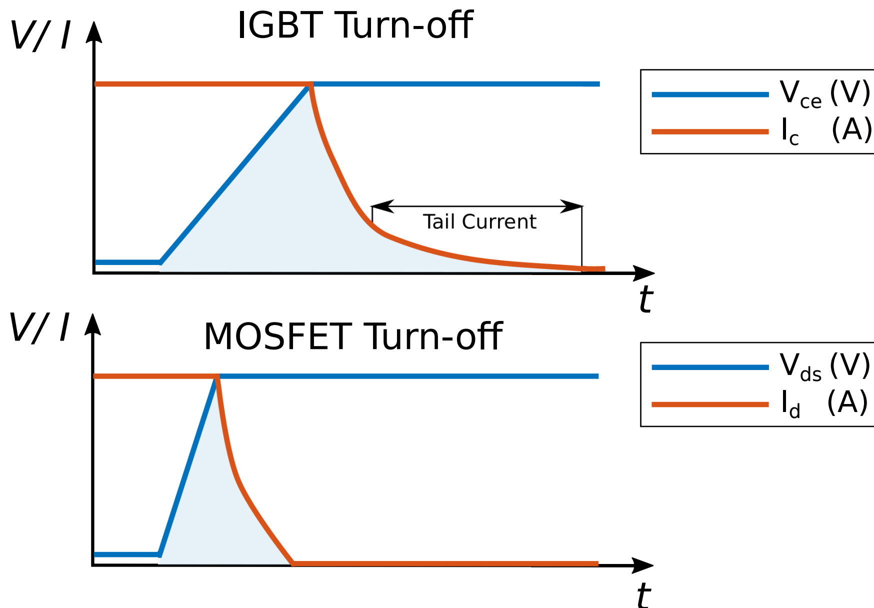


Figure 2.18: IGBT turn-off transient compared to MOSFET. Not to scale.

IGBT Turn-Off Process — The turn-off transition is one of the main disadvantages of the IGBT. The bipolar conduction, which allows for the excellent on-state voltage and V_{br}, results in a poor turn-off transient. Figure 2.18 shows the IGBT compared to the MOSFET. It can be seen that the dV/dt at turn off is slower. This is due to stored charge within the device [35], which is also negatively affected by temperature. There is also a greater delay between V_{ge} and V_{ce} compared to that of the MOSFET. The initial current decay of the IGBT is fast — this is the MOSFET (electron) portion of current in the device. The current then begins to flatten out and takes a significant period of time to reach zero. This characteristic is termed the "tail current". This is due to the slow rate of minority

carrier recombination from the CSR. Since this slow current decay happens when the full V_{ce} is supported by the IGBT, an appreciable amount of power loss is attributed to the tail current. Some techniques — such as lifetime carrier killing and an additional n^+-layer — can be used to speed up carrier recombination thus reducing switching time. These, however, reduce the *pnp* BJT gain and result in a higher on-state voltage [37], therefore higher conduction losses.

The key trade-off which has to be made for an IGBT is between the on-state performance and its turn-off transition (i.e. tail current characteristic).

2.5.3.2 IGBT Discussion

The conventional IGBT discussed so far (structure shown in Figure 2.15b) is classed as a Non-Punch Through (NPT) device. Conversely, a Punch Through (PT)-IGBT has an additional n^+ buffer region between the collector p^+ region and the n^- epitaxial drift region. The PT name arises from the effect described in Section 2.4.3.1. This is where the depletion region, under reverse blocking, extends through the n^- drift region into the n^+ buffer. Whereas in the case of the conventional NPT variant, the depletion region does not punch through the drift region. The gate structure, either planar or trench style, does not influence behaviours associated with PT and NPT.

Punch Through (PT), Non-Punch Through (NPT) & Soft-Punch Through (SPT) IGBT — The PT-IGBT has a reduced minority carrier injection and has increased recombination rate due to the n^+ buffer. This leads to an improved turn-off and therefore lower switching loss. This reduction in minority carriers comes at the expense of higher on-state voltage and conduction loss. However, the n^+ layer improves forward voltage blocking capability allowing for

a reduction in the thickness of the drift region, thus lowering the on-state voltage. The NPT-IGBT has better reverse blocking voltage capabilities than the PT-IGBT. However, most Voltage-Source Converter (VSC) topologies do not require reverse blocking as they have an additional anti-parallel diode — the Freewheeling Diode (FWD). These merits, coupled with improved latch-up characteristics, result in the PT being superior in performance [36]. The Soft-Punch Through (SPT)-IGBT, often referred to as the "fieldstop" IGBT, combines the PT and NPT technologies. This allows for devices that can achieve 6.5 kV blocking voltage capability with low on-state voltage, whilst being able to switch in a manner that does not drastically limit switching frequency [42]. For high-capacity IGBTs, most manufacturers have adopted the SPT device. This is often used along with a trench-gate structure in order to achieve further reductions in on-state voltage and switching performance.

Other IGBT Structures Reported in the Literature

Trench-Gate IGBT — As previously mentioned above, trench-gate IGBTs are commonly employed and can theoretically reduce overall losses by approximately 30–40 % [43–47]. The trench-gate structure — usually with a fieldstop collector region — is commonly used in commercial devices and ranges in complexity.

Superjunction IGBT (SJBT) — The Superjunction design that uses columns of p-type Si that sit beneath the p^+-well (discussed in Section 2.5.2.3 with regard to the MOSFET) can also be employed in bipolar devices [48]. The benefits of a Superjunction IGBT (SJBT) differs from the SJMOS. The SJMOS results in a better $R_{ds(on)}$—V_{br}, whereas in the case of the SJBT, the benefits also come in terms of improved switching performance, specifically at turn-off [49].

Reverse-Conducting (RC)-IGBT — Unlike the MOSFET, an IGBT

(PT, NPT or SPT) has no inherent body diode which can be used as a reverse conduction path. The Reverse-Conducting (RC)-IGBT has been proposed as a device that would eliminate the need for an additional FWD die in VSC applications [50]. The basic structure of the device is realised by implanting n^+ regions (termed anode shorts) into the p-collector region [51]. Infineon have commercial products of the RC-IGBT available [52]. Various evolutions of the RC-IGBT are discussed in this review article [50] and highlight that the performance trade-off between the diode and the IGBT, both dynamically and statically, are difficult to manage.

The excellent on-state performance and voltage blocking capability of the IGBT has made it the dominant device used in high-power conversion applications for the past two decades. IGBTs that are rated for up to 6.5 kV are commercially available from a number of manufacturers. However, due to their relatively large switching loss, converter switching frequencies are limited to $\sim$ 20 kHz for low-power applications and 2–4 kHz at MW scale [2].

2.6 Wide-Bandgap (WBG) Power Semiconductor Devices

As highlighted in Section 2.2.2, WBG semiconductor materials posses properties that are revolutionising the power semiconductor market. This section will discuss how these superior properties are realised in real power devices.

2.6.1 Silicon Carbide Devices

SiC will be the WBG material that is considered as it is the most technologically mature. It is also the compound-semiconductor that will make the biggest impact in the high-power PE industry for the foreseeable future. Cree manufactured the first SiC wafers for research purposes in 1991 [53]. However, it was many years after that the first devices started to appear on the market.

2.6.1.1 SiC Diodes

A WBG power device that is now considered to be mature is the SiC based Schottky diode. The First commercial Schottky diodes were SBDs by Infineon in 2001 [54] followed by Cree in 2002 [55]. Many other manufactures followed suit in subsequent years with the JBS diode. The MPS structure is now preferred by most manufacturers due to its more favourable switching, conduction and reverse blocking profile [19] .

Due to the significantly higher E_{crit} of SiC ($7.33\times$ greater), SiC based diodes are capable of operating at much higher voltages than Si devices. Traditional Si-Schottky diodes are capable of blocking voltages up to ~ 200 V, any higher than this and the on-state performance is significantly impacted[2]. Current commercially available SiC Schottky diodes are capable of blocking voltages up to 1700 V with very good on-state performance. These devices are made available at voltages of 650 V, 1200 V, and 1700 V, with current capacity for a single die up to 50 A from suppliers. These devices come with extremely low t_{rr} and Q_{rr}. Some devices are even marketed as purportedly having zero reverse recovery, such as

[2] Si diodes with ratings of several kV and kA are available. However, they have poor transient and dynamic performance.

the Z-Rec™ MPS diodes from Cree [56].

To compare this switching performance with a Si diode, a Si-FRD must be considered as it is comparable in voltage capability. It is experimentally shown in [57] and [58] that the loss associated with reverse recovery for the SiC-SBD is a small fraction of what is observed for the Si-FRD. It is also shown that the SiC device is not affected by temperature, whereas the Si device is severely affected by an increase in temperature. Other literature reports that a small amount of reverse recovery from the guard-ring *pn*-junction can be observed, as well as additional oscillatory behaviour from device capacitance and parasitic inductance in the external circuit [59, 60]. A reduction of 2/3 in turn-off loss is achievable and is relatively constant with temperature [60]. A datasheet survey of 1200 V diodes available from Infineon shows a reduction of ~ 30 % on-state loss between their Si-FRD and CoolSiC™ (SiC-MPS) diodes. However, this is a difficult comparison to make because the resistive element of the device is related to the die area which is not normally stated.

2.6.1.2 SiC-MOSFET

The first commercially available MOSFET to be fabricated using SiC was a 1200 V device by Cree in 2011 [61]. Over the past 10 years, many other manufacturers have released SiC-MOSFETs, usually with a trench-gate structure. Currently these are available at voltages of 650 V, 900 V, 1000 V, 1200 V and 1700 V; with modules that are capable of conducting upwards of 500 A [62].

As shown in Figure 2.3a (Section 2.2.2), the width of the drift region of a SiC-MOSFET device can be drastically reduced compared to a Si device for a given blocking voltage. This leads to a reduction in the specific on-resistance (per unit area) as the width of the drift region is what determines R_{drift}, with a larger

drift width resulting in a higher resistance. The theoretical reduction that SiC enables can be approximated by (2.22)

$$R_{drift}(\text{SiC}) \approx \frac{1}{500} R_{drift}(\text{Si}) \quad [\Omega] \tag{2.22}$$

This advancement can either be realised by an increased blocking voltage or lower specific on-resistance. This means that a SiC-MOSFET can have the same $R_{ds(on)}$ as a Si-MOSFET or a Si-SJMOS with a chip size that is $\sim 35\times$ and $\sim 10\times$ respectively smaller. Thus far, this has been commercially realised by an increase in voltage rating (compared to a Si-MOSFET) to bring it more in-line with a Si-IGBT for the benefit of superior conduction loss. The reduction in specific on-resistance means that less die area needs to be used. This in turn means that the overall parasitic capacitances (C_{oss}, C_{iss} and C_{rss}) and, therefore, required Q_{gs} can be much lower. This results in much faster turn-on and turn-off transients, i.e. dI/dt and dV/dt. As previously mentioned, fast switching transients result in lower switching losses and allow for faster converter switching frequencies. In 2015, ROHM released the first trench-gate SiC-VUMOS (BSM180D12P3C007) which had 50 % less on-resistance and 35 % less input capacitance than previous devices which had all used planar gate structure. Further analysis on the performance of the SiC-MOSFET will be provided in Chapter 4.

2.6.1.3 High-Voltage SiC

SiC-Diode — Engineering samples of SiC-diodes that have voltage ratings of > 10 kV have been reported in the literature [63–66]. However, these are limited in current capability and will not be commercialised any time soon.

SiC-MOSFET — There are engineering samples of SiC-MOSFETs with 3.3 kV

and 6.5 kV ratings from Cree [67], Mitsubishi [68] and ROHM [69] which are purportedly due in the coming years. Devices with ratings up to 10 kV are widely reported from research laboratories [70–73].

2.6.2 Other WBG Devices

There are other WBG devices that are not considered in this thesis, but are worth mentioning.

SiC-JFET — The SiC-JFET was in fact the first SiC transistor to be released (2006). The normally-off version would be most suited for power conversion circuits, but due to its high on-state resistance and low V_{Th} (which makes it susceptible to EMI induced turn on) it has not had much commercial success. The normally-on SiC-JFET has been released commercially and achieves a low on-state voltage [74, 75]. However, the gate-driving of this device is complex due it being normally-on. Cascode configurations, comprising a high-voltage normally-on SiC-JFET with a low-voltage normally-off Si-MOSFET have been pioneered by UnitedSiC [76]. This is a complex configuration, but ensures an overall normally-off state.

SiC-BJT — The SiC-BJT has been shown to have good on-state performance, however suffers from large parasitic capacitances which limits dV/dt and dI/dt during switching [77]. These devices require a constant base current to turn them on, unlike FET devices.

SiC-IGBT — The SiC-IGBT could be considered the ultimate high-voltage device. Devices have so far been demonstrated at > 15 kV [78, 79] with some even as high as 27 kV [80], albeit at low currents. However, commercialisation of these devices will not happen any time soon.

2.6.3 WBG Device Considerations

Emphasis on Silicon-Carbide (SiC) devices.

2.6.3.1 Thermal Properties

Operating Temperature — WBG devices are able to operate at a much higher temperature than Silicon which enables use in environments which were once thermally problematic. As shown in Figure 2.4a, Si is able to operate at ~175 °C, whereas devices fabricated from SiC should theoretically be able to operate at temperatures of up to and beyond 450 °C. However, current packaging technology limits this to not much more than what Si devices can achieve. Packaging of power semiconductors will be discussed further in Section 2.7.2.

Thermal Conductivity (λ_T) — Closely related to the temperature capabilities, the λ_T of WBG devices is also a performance enhancer. This is a measure of how readily heat can be removed from the semiconductor. An increase in λ_T allows for an increase in current density without adversely affecting the on-state resistance and switching behaviour. As shown in Table 2.2, the λ_T of SiC is $> 3\times$ that of Si. Just like maximum operating temperature, λ_T can be limited by the packaging.

2.6.3.2 Impact of Higher dI/dt & dV/dt

The increased speed of the switching transients of WBG devices allows for a large reduction in switching loss. However, there are implications from the increased dI/dt and dV/dt. During the switching transients, excessive amounts of overshoot voltage and oscillatory behaviour are present (this is not shown in the ideal

switching waveforms in Figure 2.12). Excessive overshoot voltage can limit the voltage utilisation of the device and make it more susceptible to Single-Event Burnout (SEB) — this will be further discussed in Chapter 4. The oscillatory behaviour results in a greater amount of Electromagnetic Interference (EMI), both radiated and conducted, that can lead to power converters not being compliant with Electromagnetic Compatibility (EMC) standards [81]. Device and circuit parasitic elements (inductance and capacitance) compound these issues. These issues and ways to mitigate them will be discussed further in subsequent chapters. Excessive dV/dt can also have detrimental effects on winding insulation and shaft bearings in machines which can significantly reduce their lifetime [82, 83].

2.6.3.3 Increased Cost

One of the main hurdles that SiC devices face is a substantial increase in cost compared to Si. One element of the increased cost is due to SiC being a new technology that requires further maturation and development, as well as economies of scale in order to bring the cost down. The other more fundamental reason is that SiC, along with other WBG technologies, require a greater amount of energy in the fabrication process.

SiC Wafer Development — A wafer is one slice that is cut from a crystalline Boule[3] of semiconducting material. Wafers are less than 100 μm in thickness and are used as the substrate material for epitaxial layers to be grown from. Multiple semiconductor devices are then cut from a single wafer, each of these cut pieces are called a die. An increase in wafer diameter results in more die per wafer and hence a reduction in cost. As of 2020, Si wafers that are 12" (300 mm) in diameter are used. However, this was a 40+ year development process in order to increase

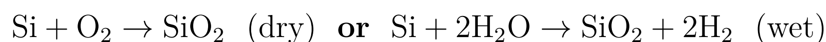
[3] A Boule is a single crystal ingot that is synthetically grown.

to that diameter whilst reducing substrate and epi defects, and maintaining high yield[4] levels.

The SiC wafers produced by Cree in 1991 were 1" (25 mm) in diameter. As of 2020 Cree and ROHM offer 6" (150 mm) wafers, with Cree increasing that to 8" (200 mm) soon. The SiC wafer production (which includes crystal growth, slicing in to wafers, polishing the wafers, and epitaxial growth) has a similar workflow to Si. However, each of these stages require very different tooling and new fabrication processes. Defects such as micropipes, screw dislocations, and edge dislocations have severely impacted yield levels during this development [84, 85]. The smaller wafer diameter and lower yield level than Si result in a more expensive material. However, this should improve with time.

The fabrication processes after wafering borrow many well established techniques from the Si industry. However, they do still come with new problems.

Oxide Growth — A MOSFET requires a gate-oxide of silicon oxide (SiO_2) to be grown and used as the gate insulator. For the Si-MOSFET gate-oxide (Si/SiO_2), the dry process uses oxygen (O) gas and the wet process uses the oxygen molecules in water (H_2O) with the additional hydrogen (H) molecules being released as a gas.



$$\mathrm{Si} + \mathrm{O_2} \rightarrow \mathrm{SiO_2} \quad \text{(dry)} \quad \textbf{or} \quad \mathrm{Si} + 2\mathrm{H_2O} \rightarrow \mathrm{SiO_2} + 2\mathrm{H_2} \quad \text{(wet)}$$

In the case of the SiC-MOSFET, the gate-oxide (SiC/SiO_2) process is not as straightforward. A dry process is used and ideally the carbon (C) atoms are removed in the form of carbon monoxide (CO) or carbon dioxide (CO_2).

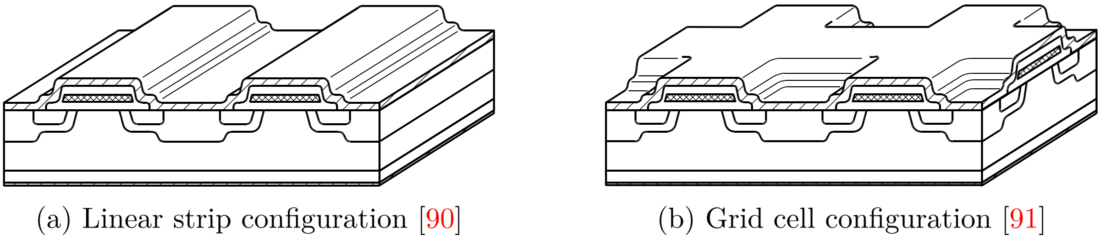
[4]Yield is the proportion of die in a wafer that functions correctly.

The process leaves many carbon atoms behind in the semiconductor. These unreacted carbon atoms form nano-islands at the SiC/SiO_2 interface. These defects are called traps [86]. This can effect channel mobility and cause V_{Th} instability. A stable V_{Th} is crucial for maintaining the operating characteristics of the MOSFET. If V_{Th} is unstable, the performance of the overall power converter may be affected. A great deal of work has been done to mitigate these issues, such as using nitrogen oxide or nitrogen dioxide at high temperatures as the oxygen delivery method [87]. The number of defects in SiC can be as much as two or three orders of magnitude greater than Si. Therefore, in order to reduce defects as much as possible; the processes take longer, require higher temperatures, and are ultimately more expensive.

Energy Intensive Process — SiC material is widely used in many industries (such as in car brakes and as ceramic plates in bulletproof vests) due its incredibly strong mechanical properties. It is one of the hardest materials known. In order to produce such a compound, a high level of energy is required. The SiC ingots require to be grown very slowly at temperatures in excess of 2000 °C and at considerably high pressures [88,89]. This makes it a very energy intensive fabrication process, resulting in the cost per mm^2 always being more than Si. This is true even if wafer diameters eventually match Si and manufacturing economies of scale help to bring the cost down. This increase in required energy also results in a larger carbon footprint relative to Si.

2.7 Real Power Devices

2.7.1 Semiconductor Die

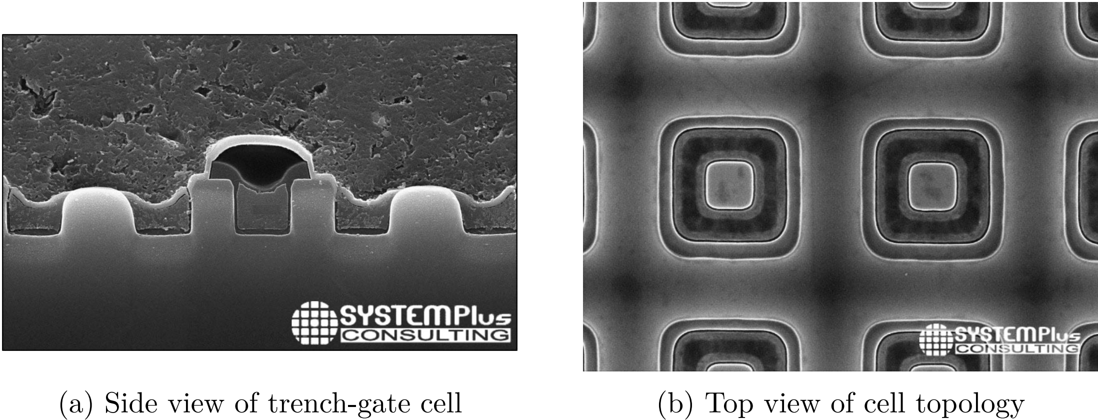


(a) Linear strip configuration [90]

(b) Grid cell configuration [91]

Figure 2.19: 3-D structure of vertical power transistor with trench-gates.

The 2-D device structures shown in the previous subsections only represent a single cell within a die. A typical device will comprise of several million of these individual cells, with cell densities in the tens of millions per cm^2 [24]. In order to make the best use of semiconductor area and increase channel density, various cell topologies can be used. A rudimentary geometry is the linear strip, shown in Figure 2.19a. More complex topologies involving grids of square and hexagonal trench-gate cells (Figure 2.19b) are commonly used in modern power devices [92,93]. Scanning electron microscope images of a SiC-MOSFET die from ROHM are shown in Figure 2.20.



(a) Side view of trench-gate cell

(b) Top view of cell topology

Figure 2.20: Scanning electron microscope images of ROHM SiC-MOSFET (BSM180D12P3C007) - copyright: System Plus Consulting.

Individual semiconductor dies are capable of conducting up to $\sim$ 300 A for a diode and $\sim$ 250 A for a transistor, however 196 A capacity dies are the largest for commercially available SiC at present. Die area is proportional to current capacity, with die sizes ranging from approximately 3 mm^2 to 200 mm^2. A selection of SiC-MOSFET bare dies from Cree are shown in Figure 2.21. Before packaging, the dies undergo a metalization stage to create the required electrical interconnects (ohmic contacts) on the semiconductor. Finally, a passivation process is done which gives the die a protective layer, usually from a material such as silicon nitride.

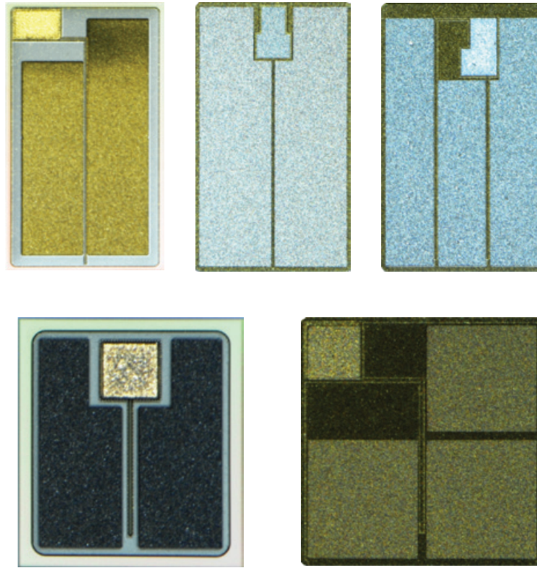


Figure 2.21: MOSFET bare die images - copyright: Cree, Wolfspeed.

For comparison, Table 2.4 shows a similarly rated SiC-MOSFET and Si-IGBT. It can be seen that the SiC device requires almost 4× less area than the Si device, hence significantly reduced input and Miller capacitance.

Device	**Part No.**	**Size (mm)**	**Area (mm^2)**	**C_{iss} (pF)**	**C_{rss} (pF)**	**V_{on} (V)**
SiC-MOSFET	CPM2-1200-0025B	4.04 × 6.44	26.02	2788	15	2.5
Si-IGBT	IGC99T120T8RQ	9.5 × 10.39	98.71	6150	345	2.42

Table 2.4: Transistor bare die comparison (1.2 kV, 100 A).

2.7.2 Device Packaging

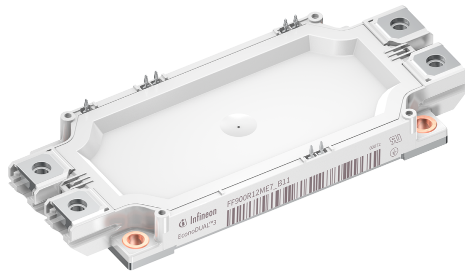
A semiconductor die requires a bespoke housing in order to electrically connect to the power circuit, thermally interface with a cooling system, and provide a good low-inductance gate connection. Metal bond-wires (usually made from copper, gold, aluminium or silver) connect the contact pads on the die to the external power pins (shown in Figure 2.24d). The die is attached to a substrate material which allows heat (power losses) to transfer to a metal base-plate and then to the cooling system. The thermal connection needs to be low in thermal impedance in order to realise the device's full capabilities, but high in electrical insulation[5] for safety reasons, as the base-plate will be connected to a heatsink or other cooling system which will be earthed. The packages are often filled with an encapsulation material, such as silicone, to protect the die from contamination and vibrations, and also provide insulation to prevent arcing between conductors.

For applications up to $\sim$ 100 A, single semiconductor dies are put into discrete packages (Figure 2.22a) intended to be assembled on a Printed Circuit Board (PCB) in either a Surface-Mount Technology (SMT) or through-hole fashion. For higher current ratings, high-capacity dies, or several lower capacity dies in parallel, are placed into modules making them capable of conducting hundreds to thousands of amps. These modules often contain the half-bridge topology, with several dies in parallel (to increase current capacity), the necessary FWDs and internal gate resistors ($R_{g,int}$). Some designs also include a temperature sensing thermistor for monitoring the internal package temperature and inferring the device's junction temperature. A selection of modules are shown in Figure 2.22, ranging in current capacity from tens of amps for the discrete package (Figure 2.22a) up to 2 kA for the large module (Figure 2.22d). These high-power

[5] In some discrete packages this is connected to one of the power terminals.

(a) TO247-4 discrete.

(b) 62 mm module.



(c) EconoDUAL™ module.

(d) PrimePACK™ module.

Figure 2.22: Selection of power semiconductor packages - copyright: Infineon.

module packages have been developed in-line with the advancements of the Si industry (mainly IGBT). They meet the requirements in terms of allowable stray inductance and thermal performance.

2.7.2.1 Kelvin Terminal

Transistors are fundamentally three-terminal components. However, many discrete packages and modules have four, sometimes even five. These additional ones are Kelvin[6] terminals, the most common being the Kelvin-Source (KS) for a MOSFET (or Kelvin-Emitter (KE) for an IGBT) that is used to aid gate driving. The KS can be seen in Figure 2.23. During a switching transient, a dI/dt will be imposed on the lead inductance L_s, resulting in a voltage perturbation. Lead inductance is typically in the order of 10s of nH. For slow switching de-

[6]The naming convention comes from Lord Kelvin's precise measurement connection method.

vices this may result in millivolts, but for faster devices this can result in a few volts. As the gate is driven with respect to the source — hence a gate-source loop — the gate-source voltage will be influenced by this series connected voltage perturbation. This results in slower switching speed and/or increased oscillatory behaviour [94]. Using a KS connection decouples the gate-source loop from the main power commutation loop.

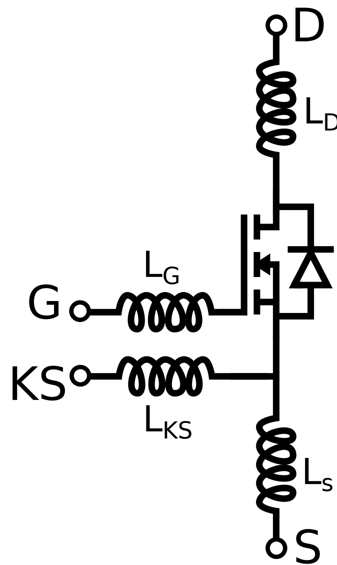
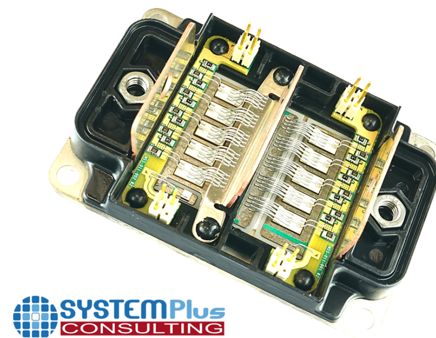


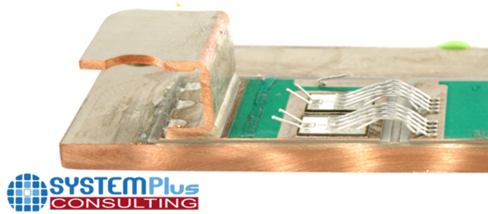
Figure 2.23: Kelvin-Source (KS) connection of MOSFET.

All of the device packages shown in Figure 2.22 have this fourth KS or KE connection. Figure 2.24d shows the gate and KS connections attached to a die (bond-wires at the top of the image). KS connections are especially important for SiC-MOSFETs. A Kelvin-Drain (KD) or Kelvin-Collector (KC) can also be used for a device voltage measurement; either for a protection feature, an intelligent gate-drive feature (discussed further in Chapter 3 and 4) or for clean voltage measurements.

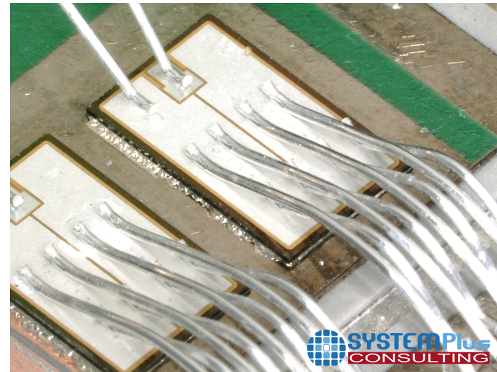
(a) Cree XM3 power module.



(b) Delidded module.



(c) Internal structure.



(d) MOSFET die and bond-wires.

Figure 2.24: Cree XM3 SiC MOSFET power module - copyright: Cree, Wolfspeed (a) and System Plus Consulting (b),(c)&(d).

2.7.3 WBG Packaging

Traditional packaging technologies do not have the capabilities to realise the full potential of WBG devices [95]. This is mainly due to a limitation in temperature capabilities (~175 °C) and excessive stray inductance.

"*I would equate it to dropping a Ferrari engine into a VW bug chassis*"
John Palmour, Cree—Chief Technical Officer [96].

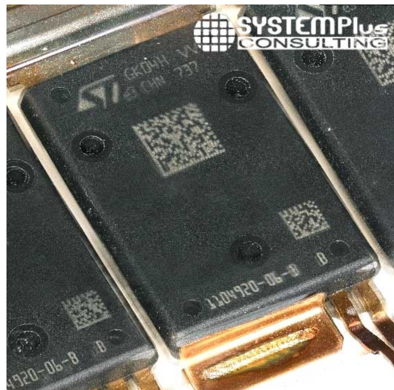
The stray inductance in a package arises from the conducting path between the die and the device terminal: from the ohmic contact on the die; the solder or sinter joints that are used; the bond-wires; and the internal power bussing structure or lead-frame. Packaging temperature limitations are determined by the melting points of the housing, encapsulation and substrate materials, as well as the package's overall thermal conductivity. The majority of commercial SiC devices thus far, both modules and discretes, have used the designs shown in Figure 2.22 or evolutions of them, albeit with an improved stray inductance. Standard EconoDUAL™ and 62 mm modules have an inductance of > 15 nH, which severely limits dV/dt and dI/dt. However, the newer commercial modules are achieving reductions of around half of that. Figure 2.24 shows a new generation 1.2 kV, 400–450 A SiC-MOSFET half-bridge module from Cree which has 6.7 nH of stray inductance and can operate at 175 °C. The packaging used for GaN devices has been significantly modernised due to significantly low stray inductance requirements [97]. The impact of stray inductance will be further discussed and experimentally demonstrated in Chapter 3.

2.7.4 Advanced WBG Packaging in Literature

Research into future packaging technologies for WBG devices has received increased attention recently. Many proof of concepts that suit the required characteristics for WBG device have been developed. However, reliability and life-time issues, manufacturing capabilities, and the additional cost of materials and tooling stop many of these concepts making it through to commercial applications.

Traditional packaging uses wire-bonding and planar assembly structures, often considered to be a 2-D approach. The first advances reported in the literature, with an aim to reduce inductance, is in the bond-wires (as they are industrially

mature) with better module layout and use of ribbon bonding. These have been proven to reduce inductance and increase current capacity [98, 99].



(a) Module

(b) DLB structure

Figure 2.25: STMicroelectronics low inductance SiC-MOSFET package - copyright: System Plus Consulting.

So called “bond-wireless” structures have seen significant attention. The Direct Lead Bonding (DLB), where a copper lead/structure that is directly soldered or sintered to the die, has been presented in various publications [100, 101] and it has been shown to significantly reduce the loop inductance. DLB has even made it into a SiC-MOSFET module from STMicroelectronics that is used in a high-performance Electric Vehicle (EV) inverter[7]. This module is shown in Figure 2.25. The DLB method has been taken further by using flexible PCBs. For multi-die modules, careful inductance matching needs to be ensured so that current is dynamically shared equally (current will share statically based upon the on-resistances of the dies).

[7]Tesla Model 3.

Whilst advanced bond-wire techniques and DLB approaches help to reduce inductance, they do not offer any improvements for thermal performance, in terms of thermal impedance from junction to ambient. Various methods which involve embedding the dies in complex geometries of conductors and thermal interfacing materials are presented [102, 103]. These structures are achieved by fabrication processes using either intricately made copper conductors and ceramics/polymers, sometimes even being grown and/or etched away in situ. This allows the die to be cooled from both sides, thus reducing the thermal impedance further [104–106]. This embedded planar structure, often referred to as 2.5-D where High-Side (HS) and Low-Side (LS) dies are side by side, can be further improved to a full 3-D system. The most common 3-D structure, which makes use of the embedded techniques, is the Chip on Chip (CoC) structure where the HS and LS dies are stacked vertically with an interconnect between them [107–110]. This is a similar concept to the press-pack design used in high-current IGBTs, thyristors and diodes. The CoC structure has been shown to achieve very low inductances of < 1 nH (0.25 nH in [109]), much better thermal performance than traditional approaches, and also a reduction in overall volume.

Integrating associated components and other features into the package can also improve performance. Embedding decoupling capacitors into the package, in both standard and advanced packing designs, as close to the half-bridge pair as possible, can further reduce the loop inductance. This has been shown in [110–113] where SMT Multi-Layer Ceramic Capacitor (MLCC) components are placed adjacent to the dies. Not only does this reduce loop inductance, improve switching performance, and reduce EMI, but it also aides with dynamic current sharing in multi-die modules. As already mentioned, gate resistors are also placed within the modules. In order to eliminate any unnecessary stray inductance in the gate-source (or gate-emitter) loop, the gate-drive IC can also be embedded [114]. The high-temperature properties of SiC can be exploited for low-voltage circuitry

[115, 116] such that gate-drive ICs can be placed directly beside the SiC power dies with no thermal issues [117]. The integration of these features into power modules is starting to give rise to the “Intelligent Power Module” terminology.

Previous paragraphs have mentioned how thermal impedance can be improved by advancements in device structure and fabrication techniques. However, there are other thermal issues which are an impediment to true high-temperature operation. The maximum temperature capabilities of the various packaging materials (including the substrate, encapsulation, and housing material) is a major hindrance. The substrate, which is the main thermal interface between the die and the base-plate, is traditionally made up of two metal layers with an insulating (most often ceramic) layer between them. Various fabrication techniques and ceramic materials are presented in [95], which shows that achieving high-temperature performance is possible. However, this requires a trade-off between cost, ease of fabrication, and structural integrity. The standard silicone encapsulation material used in traditional packaging is limited to ∼200 °C. Higher temperature encapsulation materials are being developed and show temperature capabilities of ∼300 °C [118, 119]. Nevertheless, these are difficult to fabricate and will substantially increase the cost. Material choices for the housing of the package are easier in terms of high-temperature. Despite that, this will also result in an increase in cost.

If SiC is going to be used at even higher voltages ($>$ 10 kV), whilst maintaining a high level of electrical and thermal performance, packaging also needs to be developed to suit. This high-voltage nature creates electrostatic issues which require reinforced isolation, as per IEC 61800-5-1, making low inductance designs difficult. The first-generation 10 kV SiC-MOSFETs were placed in the 6.5 kV IGBT packages [120]. However, the stray inductance was excessive, resulting in a significant amount of EMI and poor switching losses. In 2016, Cree produced

engineering samples of third-generation 10 kV SiC-MOSFETs and an improved module design [121] which achieved 16 nH of stray inductance. The prototypes produced in [122, 123] make use of the 3-D embedded packaging methods as well as the integration of decoupling capacitors. It achieves 4.4 nH of inductance and significantly reduced parasitic coupling capacitances.

* * *

3 Realisation of High-Power Double-Pulse Test Rig & Measurement Equipment for Wide-Bandgap Devices

3.1 Chapter Introduction

Investigating the nuances of the switching characteristics of power semiconductor devices, in particular Wide-Bandgap (WBG), is difficult if datasheet curves and simulations alone are relied on. SPICE based and Simulink modelling can allow for topology based investigation but do not possess the intricacies required to fully understand transient behaviours. In order to experimentally characterise high-power Silicon-Carbide (SiC)-Metal–Oxide–Semiconductor Field-Effect Transistor (MOSFET)s and Silicon (Si)-Insulated-Gate Bipolar Transistor (IGBT)s, a test rig was designed and built.

This chapter will discuss the work undertaken to realise a high-power Double-Pulse Test Rig (DPTR) that is capable of testing the switching characteristics

of power-semiconductor devices. The theory behind many of the design considerations, the associated components required to make a Power Electronic (PE) converter work, and the necessary high-bandwidth measurement equipment and testing methodologies will be discussed and presented.

The DPTR is capable of subjecting devices with voltages up to 2 kV, current magnitudes up to 1.5 kA, and temperatures up to 150 °C. It was designed specifically to realise the full switching capabilities of SiC-MOSFETs. A photograph of the DPTR can be seen in Figure 3.1. This build took almost two years to complete, from initial planning discussions through to the final commissioning tests.

This test rig was built to facilitate multiple research activities within the Power Electronics research group at the University of Edinburgh. I lead the design and build of this, however significant collaboration with Dr. Paul Judge made it possible. Thanks should also go to several technical staff within the School of Engineering who assisted with the various mechanical tasks involved in the build of this test platform — Iain Gold, Jamie Graham, James Brennan, Derek Watson, Andrew Brown, Calum Melrose, Douglas Carmichael, and Andy Mullen.

The chapter is structured as follows: Section 3.2 introduces the double-pulse testing methodology; Section 3.3 covers the build of the power circuit, with Section 3.4 discussing the full testing platform and other required components; Section 3.5 demonstrates the effect of the parasitic elements within the testing system; Section 3.6 reviews the testing equipment used and what is required for WBG devices; and Section 3.7 discusses how the measurements are used to estimate the switching losses.

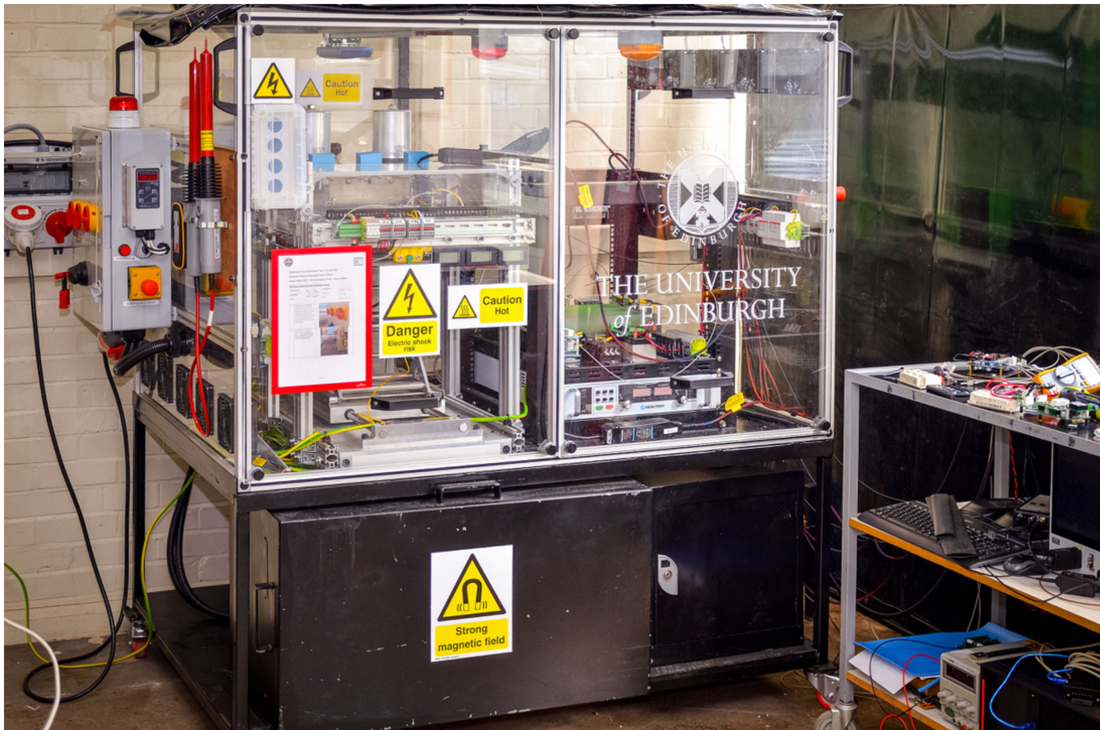


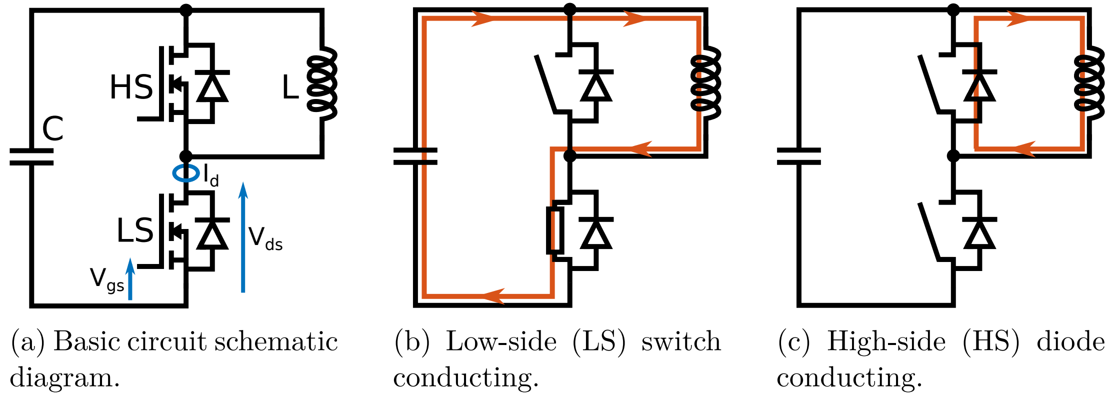
Figure 3.1: Photograph of the Double-Pulse Test Rig (DPTR).

3.2 Double-Pulse Test Rig (DPTR)

3.2.1 Double-Pulse Test

The double-pulse approach for testing power semiconductor devices is a widely used method to characterise device switching transients [124]. It works by effectively synthesising the conditions that a device would be subject to in an actual PE converter, with a set of switching transition measurements being made. A basic schematic diagram of this clamped inductive switching circuit is shown in Figure 3.2a. A half-bridge configuration is used with, in this case, the Low-Side (LS) switch as the Device Under Test (DUT). A large capacitance (C) on the DC bus is used as the energy source and is charged to the desired test voltage. An inductive load (L) in parallel with the High-Side (HS) switch is used to set the test current. In order to test the HS device, the inductor would be moved to

be in parallel with the LS switch.



(a) Basic circuit schematic diagram.

(b) Low-side (LS) switch conducting.

(c) High-side (HS) diode conducting.

Figure 3.2: Double-pulse test methodology. Low-side (LS) switch is the device under test (DUT).

3.2.2 Methodology

The “double-pulse” terminology is self explanatory — two pulses are used in the test, as shown in Figure 3.3. The test starts by charging the capacitor to the desired test voltage. The HS device remains turned off for the entirety of the test, however its Freewheeling Diode (FWD) is used for commutation. Two turn-on pulses are applied to the gate of the LS device with the turn-off and turn-on transition between these pulses being measured. The measurements typically taken are noted in Figure 3.2a (I_d, V_{ds}, & V_{gs} for the case of a MOSFET), however the same measurements may also be taken for the HS device (transistor and FWD) to observe its behaviour. The point of interest is highlighted in yellow in Figure 3.3. The first pulse is used to establish the desired load current. Equation (3.1) determines the rate of change of current in the inductor.

$$V_L = L\frac{dI}{dt} \qquad [\text{V}] \tag{3.1}$$

This can be rearranged for the charging time required for a given current

magnitude (I_L), as shown in (3.2)

$$t_{charge} = \frac{I_L \cdot L}{V_{bus}} \quad [\text{s}] \tag{3.2}$$

where: t_{charge} is the length of the first pulse, as shown in Figure 3.3; L is the magnitude of the load inductor; and V_{bus} is the voltage of the DC bus. The commutation path for the current during this first pulse is shown in Figure 3.2b.

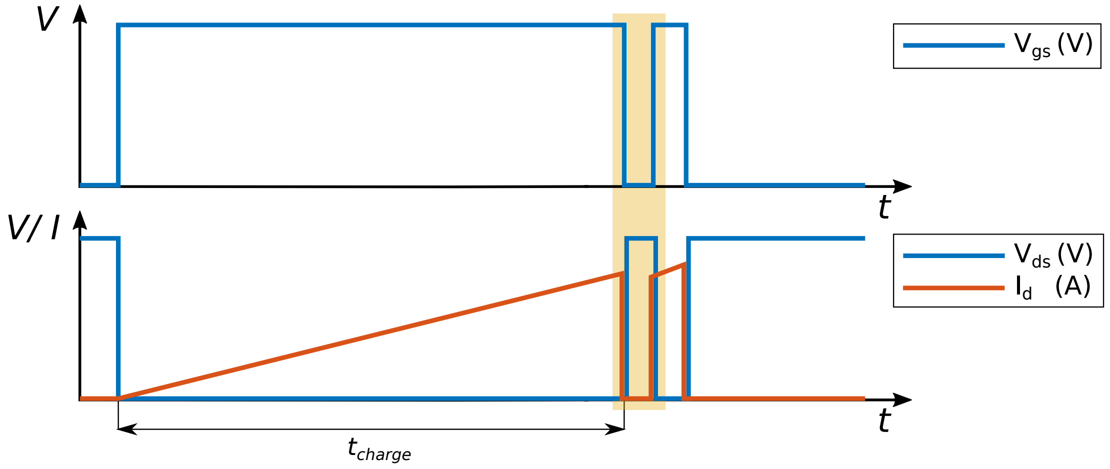


Figure 3.3: Double-pulse test waveforms.

To ensure that the voltage is precisely at the expected value at the end of the first pulse, the energy that is transferred from the capacitor to the inductor must be accounted for. This transfer of energy from electrical to magnetic results in a voltage drop. Therefore, the capacitor requires some extra energy, or rather an additional pre-charge of voltage, to begin with. The conservation of energy equation can be expressed as (3.3)

$$\frac{1}{2}CV_1{}^2 - \frac{1}{2}CV_2{}^2 = \frac{1}{2}LI^2 - 0 \quad [\text{J}] \tag{3.3}$$

This second order equation can then be solved to ascertain the required pre-

charge voltage ($V_{bus,+\Delta}$), as shown in (3.4)

$$V_{bus,+\Delta} = \sqrt{\left({V_{bus}}^2 + \frac{L \cdot {I_L}^2}{C_{dc-bus}}\right)} \quad [\mathrm{V}] \tag{3.4}$$

The period of time between the two pulses (t_{fw}) where the current commutates through the HS FWD, as shown in Figure 3.2c, should be small. This is to ensure that the subsequent turn-on transition is at a similar current value to the turn-off. The length of the second pulse is irrelevant for measurement purposes, however current will continue to increase which may exceed the device's rating. Therefore, the second pulse should be short.

3.3 DPTR Power Circuit Realisation & Theory

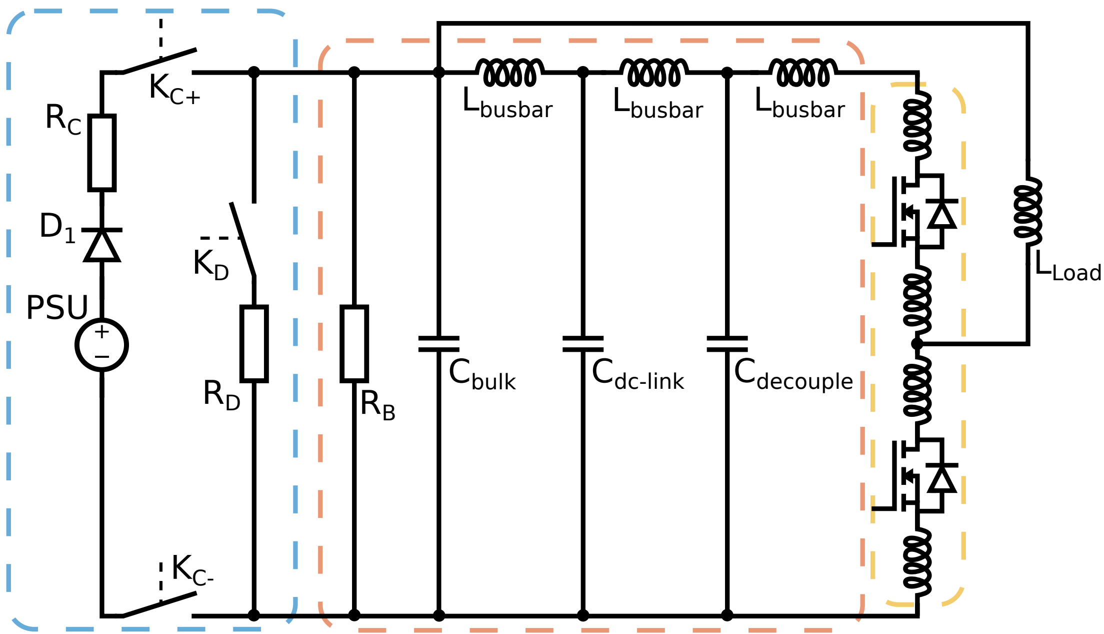


Figure 3.4: DPTR full circuit diagram. Blue dashed box: Charging circuitry. Orange dashed box: DC busbar and capacitors. Yellow dashed box: Half-bridge power module.

The double-pulse circuit requires additional components and circuitry to what

was shown in Figure 3.2a. The full circuit which includes these other necessary parts is shown in Figure 3.4.

3.3.1 Charging Circuitry

The blue dashed box in Figure 3.4 shows the charging circuitry of the DPTR. The Power Supply Unit (PSU) is a programmable DC voltage-source capable of 2 kV at 2.2 A from Magna-Power. It is from their XR series and has an isolated output stage. The reinforced isolation (+ISO) option was chosen to increase safety and also as it has a lower coupling capacitance. The PSU was also given additional reverse protection from diode D_1. A 1 kΩ resistor R_C is used to limit the inrush current from the PSUs output capacitor to the main capacitor bank. A double-pole normally-open reed relay K_C is used to connect the charging circuitry to the main power circuit (both the positive and the negative connection). This relay opens just before the test procedure commences to remove the common-mode coupling path. Figure 3.5 shows a render of the relay on a custom Printed Circuit Board (PCB) including the optical input control. This is a single-pole modular design that can be stacked to achieve the double-pole (K_{C+} & K_{C-}) functionality with one control input.

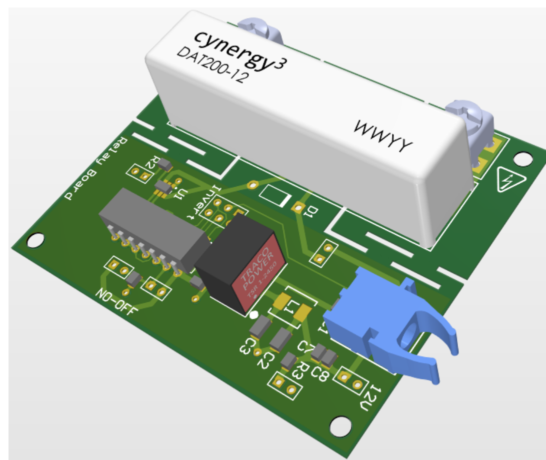


Figure 3.5: High-voltage optically controlled relay PCB.

Resistor R_D and a normally closed relay K_D are used to rapidly discharge the capacitor bank when necessary (approximately 11 s to discharge to below 50 V and 23 s to below 1 V). R_D is a 500 Ω wire wound power resistor which is capable of dissipating the required energy during a fast discharge. K_D is realised on the same PCB as seen in Figure 3.5 but with a normally closed variant of the read relay. For safety reasons, this is interlocked with micro switches on the DPTR enclosure doors.

3.3.2 DC Busbar and Capacitors

The main DC-bus is highlighted by the orange dashed line in Figure 3.4. This comprises the three capacitive elements (C_{bulk}, $C_{dc-link}$ & $C_{decouple}$), a low-inductance copper busbar (denoted by L_{busbar}) and a bleed resistor R_B. This assembly is illustrated in Figure 3.6. A structure made from aluminium extruded profile and pieces of Tufnol[1] was used to support the busbar and capacitor assembly — this is not shown in the render.

Busbars are most often made from copper and serve as the conductors for high-power applications. They provide the current carrying capacity, or ampacity, as well as offering a low inductance path for that current. They are used in everything from switchgear[2] and distribution panel boards to PE based converters. In PE applications, in particular on the DC bus of an inverter, the electrical performance requirements of the busbar are high. The busbar also provides the support structure for the necessary capacitors on the DC-bus.

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[1]Kite Tufnol was used for its high level of electrical insulation, good mechanical strength, and good temperature capabilities.

[2]Isolator switches, fuses and/or circuit breakers.

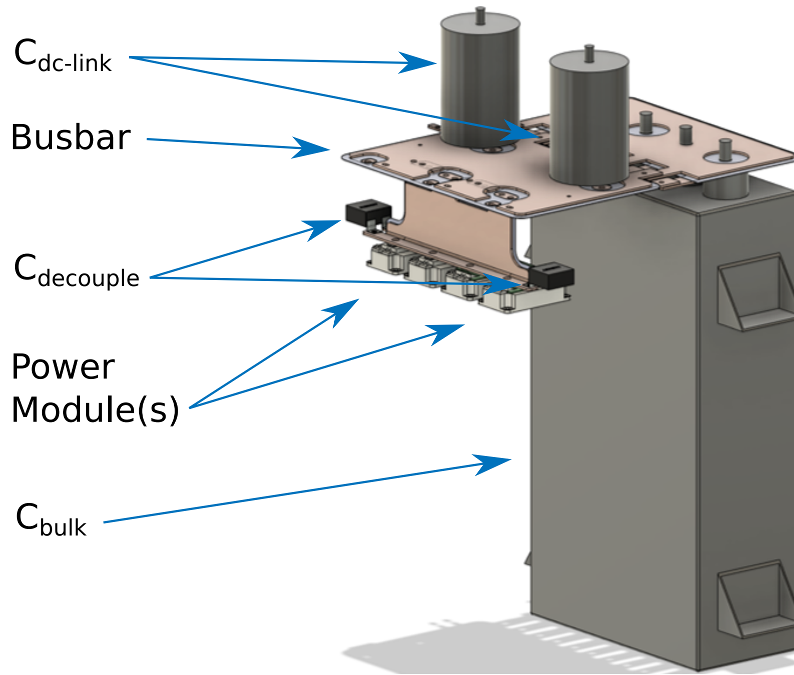


Figure 3.6: Render of the main power circuit in the DPTR. R_B not shown.

3.3.2.1 DC Side Capacitors

Due to the high dI/dt and dV/dt present in hard switched PE converters, decoupling capacitors are required on the DC-bus. They provide a low impedance path for the high-frequency energy for the switching transitions whilst helping to maintain a stable bus voltage. This capacitance is generally realised in two separate stages: a DC-link capacitance which is typically large in value and made up of parallel connected capacitors; and a high-frequency decoupling capacitor which is physically located as close to the half-bridge as possible. The high-frequency decoupling capacitor is typically at least one order of magnitude smaller than the dc-link capacitance. The DC-link and decoupling capacitors in the DPTR are illustrated in Figure 3.6 as $C_{dc-link}$ and $C_{decouple}$, respectively. The value of $C_{dc-link}$ in real applications is determined by the converter switching frequency, capacitor ripple current and allowable ripple voltage on the DC-bus. It is suggested

in [125, 126] that the magnitude of $C_{decouple}$ is chosen as (3.5)

$$C_{decouple} > \beta \cdot C_{oss} \qquad [\text{F}] \tag{3.5}$$

where: $\beta = 100$ required as a minimum (with $\beta > 250$ yielding diminishing returns); and C_{oss} is the output capacitance of the DUT.

There are two main types of capacitor technologies used in high-power applications — film and electrolytic. Electrolytic capacitors are usually the cheaper option and have the superior volume—capacitance ratio (hence better energy density). However, due to the way in which they are constructed, they generally have a larger Equivalent Series Inductance (ESL) and Equivalent Series Resistance (ESR) than their film type counterparts. The electrolyte in the electrolytic capacitor also tends to dry out in $\sim$ 10,000 hours which further increases the ESR, whereas film capacitors have life expectancies of several hundreds of thousands of hours. In high-speed inverter applications, the film capacitors tend to be the preferred option [124]. In lower power applications which are realised on PCBs, Surface-Mount Technology (SMT) ceramic capacitors are also used.

The specific capacitors used in the DPTR are listed in Table 3.1 along with their ESL and ESR. The total capacitance on the DC-bus is a simple parallel combination of these capacitors, as shown in (3.6)

$$C_{dc-bus} = C_{bulk} + C_{dc-link} + C_{decouple} \qquad [\text{F}] \tag{3.6}$$

As shown in Figure 3.8 there are two $C_{dc-link}$ on the busbar. The total capacitance is 6.26 mF with the majority contribution from C_{bulk}. This was sized in order to limit the voltage drop on the DC-bus during the double-pulse test.

Capacitor	Value	ESL	ESR	Type
$C_{decouple}$	470 nF	< 20 nH	4 mΩ	Film (Polypropylene)
$C_{dc-link}$	430 μF	54 nH	2.6 mΩ	Film (Polypropylene)
C_{bulk}	5.4 mF	< 80 nH	0.5 mΩ	Film (Oil)

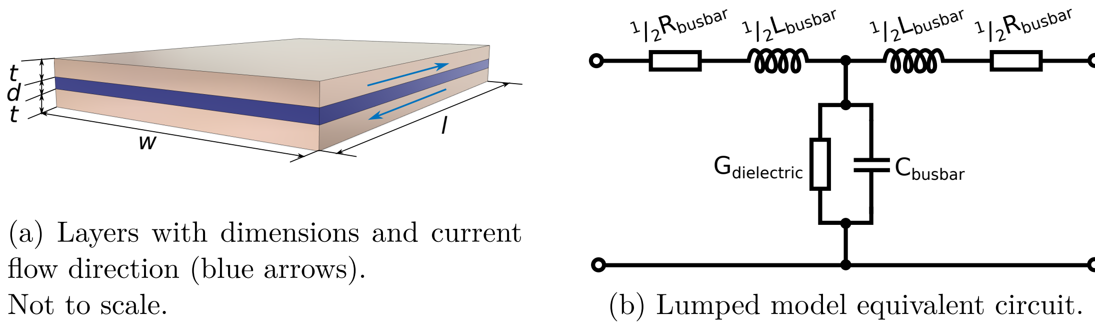
Table 3.1: Capacitors used in the high-power DPTR. $C_{decouple}$ = MKP386M447250JT1, $C_{dc-link}$ = 947D431K132CJRSN, & C_{bulk} = B25750H2548K004.

The additional voltage required is small even when operating at high-current set points, see Equation (3.4). When assessing the high-frequency of the DPTR power circuit, C_{bulk} can be considered as voltage-source instead of a decoupling capacitor. This is due to its large capacitance magnitude meaning essentially no current will be sourced from it during the switching transitions of the semiconductor DUT. This large capacitor, which is 44 kg in weight, is the type which is typically found in grid-scale filtering applications or as the capacitive component in the sub-modules of High-Voltage Direct Current (HVDC) Modular Multi-Level Converter (MMC) converters.

3.3.2.2 Low Inductance Busbar

The busbar should be considered as an electrical component in itself rather than just a simple conductor. Excessive inductance in the busbar can cause undesirable resonance with the bus capacitors. In hard-switched converters, this inductance can have a severe impact on the switching performance of the power semiconductor devices, resulting in increased losses and Electromagnetic Interference (EMI). This is particularly important for circuits which use WBG semiconductor devices due to their fast transient characteristics.

The planar DC busbar consists of two parallel plates (of resistivity ρ, length l, width w, and thickness t) separated by a thin dielectric material (of thickness



(a) Layers with dimensions and current flow direction (blue arrows). Not to scale.

(b) Lumped model equivalent circuit.

Figure 3.7: Planar two layer busbar.

$t_{dielectric}$ and dielectric conductivity $\sigma_{dielectric}$). $t_{dielectric}$ can also be considered as the separation distance d of the plates. A cross-section of the busbar is illustrated in Figure 3.7a. It is reported in [127] that a lumped parasitic model is a good approximation of a busbar. The equivalent circuit of this is shown in Figure 3.7b, where: R_{busbar} is the resistance; L_{busbar} is the inductance; C_{busbar} is the capacitance formed by the two plates and the inner dielectric material; and $G_{dielectric}$ is the conductance of the dielectric. These lumped components comprise many relationships between the physical dimensions, geometries, and electrical parameters of the busbar and its components. These will be discussed in the following subsections.

Capacitive Element of Busbar — C_{busbar} can be defined as (3.7)

$$C_{busbar} = \epsilon_o \epsilon_r \frac{A_{busbar}}{t_{dielectric}} \qquad [\text{F}] \tag{3.7}$$

where: ϵ_o is the permittivity of free space; ϵ_r is the dielectric material's relative permittivity; and A_{busbar} is the total area of the busbar in which there is overlap between the two plates. Increased C_{busbar} leads to a lower characteristic impedance of the busbar, which aides with Electromagnetic Compatibility (EMC). Therefore, maximising this capacitance by reducing $t_{dielectric}$ and using a material with a high ϵ_r is beneficial. The total C_{busbar} should be added

to $C_{DC-link}$, however, in reality C_{busbar} is typically 1–10s of nF and is therefore insignificant in terms of stored energy.

Dielectric Shunt Conductance — $G_{dielectric}$ can be considered as dielectric losses due to leakage current from one plate to the other. When using high quality dielectric materials, this is a negligible quantity. This can be calculated as (3.8)

$$G_{dielectric} = \sigma_{dielectric} \frac{w \cdot l}{t_{dielectric}} \qquad [\mathrm{S}] \tag{3.8}$$

Inductive Element of Busbar — The inductance of a two layer planar busbar comprises two parts: the individual conductors internal inductance (L_i), sometimes called self inductance; and the external inductance (L_e) of the two which arises from the magnetic flux cancellation which acts to further reduce inductance. The "skin effect", which describes how a conductor behaves at high-frequencies in terms of current density, also influences this. Low-frequency DC current will conduct uniformly throughout the entire cross-sectional area of the metal, whereas high-frequency AC current has a much higher current density at the surface of the conductor. It is shown in [127, 128] that L_i and L_e can be calculated as (3.9) and (3.10), respectively.

$$L_i = l \frac{\mu_o \mu_r}{8\pi} \qquad [\mathrm{H}] \tag{3.9}$$

$$L_e = l \frac{\mu_o \mu_r}{\pi} \left[ln \left(\frac{d}{t + w} \right) + \frac{3}{2} + \Delta_k + \Delta_e \right] \qquad [\mathrm{H}] \tag{3.10}$$

where: μ_o is the permeability of free space; μ_r is the relative permeability of the dielectric material; and Δ_k & Δ_e are geometric coefficients. In a typical high-

power PE busbar — where: $d \ll 2t$, $d \ll t + w$, and $t \ll w$ — the external inductance can be simplified to (3.11)

$$L_e = 2\mu_o\mu_r\frac{t \cdot l}{\pi(t + w)} \qquad [\mathrm{H}] \tag{3.11}$$

The total busbar inductance is expressed as (3.12). When there is minimal distance between the plates, the largest component is the internal inductance. The external inductance is significantly less due to the thin dielectric material.

$$L_{busbar} = L_i + L_e \qquad [\mathrm{H}] \tag{3.12}$$

Resistive Element of Busbar — The resistance of the busbar is also affected by the "skin effect". The DC component of the resistance is expressed as (3.13)

$$R_{busbar,DC} = \rho\frac{2 \cdot l}{w \cdot t} \qquad [\Omega] \tag{3.13}$$

For high-frequency analysis where the current density can be assumed to be greatest at the surface of the conductor, the AC component of resistance must be considered and is defined as (3.14)

$$R_{busbar,AC} = \rho\frac{4 \cdot l}{w \cdot \delta_{skin}} \qquad [\Omega] \tag{3.14}$$

where: δ_{skin} is the skin depth where the current density is at its highest and is

proportional to frequency (f) as shown in (3.15)

$$\delta_{skin} = \sqrt{\frac{\rho}{\pi f \mu_o}} \qquad [\text{m}] \tag{3.15}$$

In reality, the resistive elements are insignificant as ample busbar cross-sectional area will be used. If it isn't, the busbar would become an area of high losses.

Characteristic Impedance of Busbar — In a well designed busbar, where the resistive components (R_{DC} & R_{AC}) and the insulation conductance ($G_{dielectric}$) are negligible, the characteristic impedance (Z_{busbar}) of the two layer planar busbar is given by (3.16)

$$Z_{busbar} = \sqrt{\frac{L_{busbar}}{C_{busbar}}} \qquad [\Omega] \tag{3.16}$$

From an EMC stand point, maintaining a low Z_{busbar} of the busbar is essential. As shown in (3.16), this is achieved by reducing L_{busbar} and increasing C_{busbar} both of which are analogous.

To recapitulate, the total inductance of the two layer planar busbar can be reduced by:

- increasing width of busbar plate
- increasing thickness of busbar plate
- reducing length of busbar plate
- reducing distance (or $t_{dielectric}$) between busbar plates

- using a dielectric with high relative permittivity (ϵ_r)
- maintaining overlap of parallel plates

However, increasing the thickness and/or the area of the conductor increases material cost. Insulating materials which are thin, but high in electrical insulation, are also expensive. Some dielectric materials commonly used are Kapton (polyimide film), Ultem (polyetherimide film), and Polyethylene Terephthalate Glycol-modified (PETG).

DPTR Busbar — As previously mentioned, the C_{bulk} and its busbar are not considered in the high-frequency analysis. The planar busbar and capacitors ($C_{dc-link,1}$, $C_{dc-link,2}$, & $C_{decouple}$) which are of interest, are shown in Figure 3.8. This illustration shows one 62 mm half-bridge module connected to the busbar and, as such, only one decoupling capacitor is connected directly beside it. However, up to four devices (shown in Figure 3.6) can be connected. This allows for testing parallel connected devices, a full-bridge (H-bridge) configuration, and a hybrid configuration which will be discussed in Chapter 5 and 6.

It has been designed to be as flexible as possible and accommodate various module packages with little revision required. This was achieved by using two separate sections. The horizontal busbar section, which has the two DC-link capacitors, is held in place by insulating supports and is mounted to the busbar section of C_{bulk} — this is the permanent fixture. Whereas, the bottom vertical section, which connects to the devices and decoupling capacitors, is designed to be removed and/or replaced. Being able to easily remove this part also facilitates connecting various measurement equipment. Riveted captive nuts made out of brass were used at the interface connection points to aide with this. Whilst the additional length that arises from the bottom section of the busbar is contrary

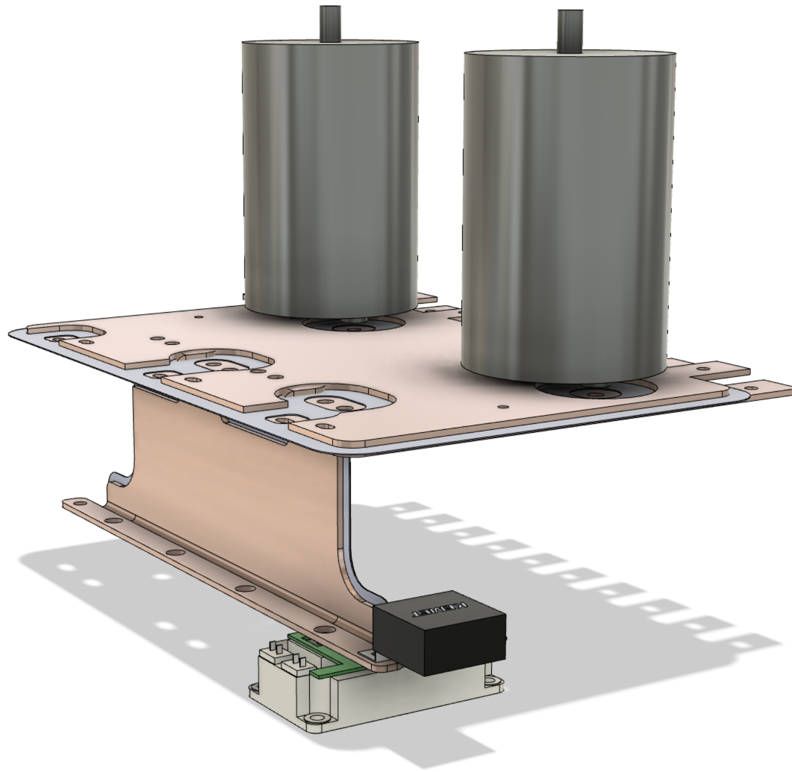


Figure 3.8: Render of the main DC busbar and decoupling capacitors.

to low inductance design methodology, it was necessary for accommodating the measurement equipment. However, the high-frequency $C_{decouple}$ is still located as close as possible to the module.

This assembly was designed using AutoCAD [129] — a Computer Aided Design (CAD) software package — and then fabricated using various laser cutting/etching and machining processes. 3 mm high-grade copper plates were used with a tin plating layer applied to stop oxidation. A 0.5 mm thick layer of PETG was used as the dielectric material, the properties of which are shown in Table 3.2.

Property	Value
Dielectric strength	16.1 kV/mm
Relative permittivity (ϵ_r), 10 kHz	2.6
Relative permittivity (ϵ_r), 10 MHz	2.4

Table 3.2: PETG dielectric properties.

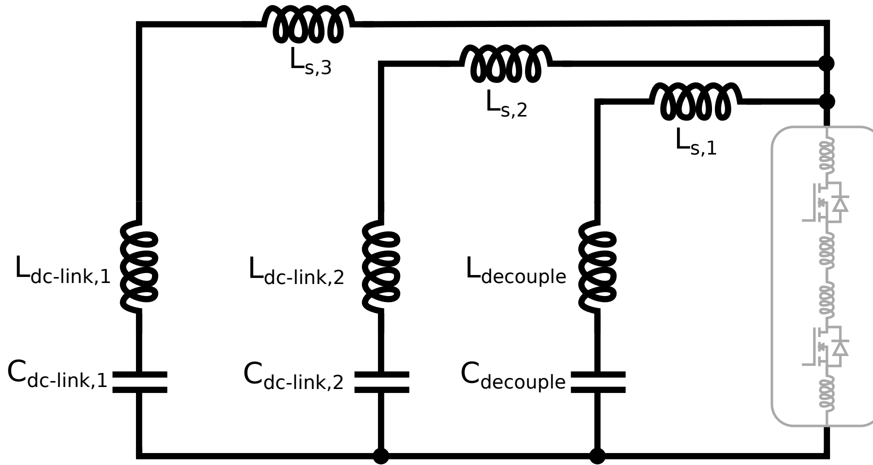
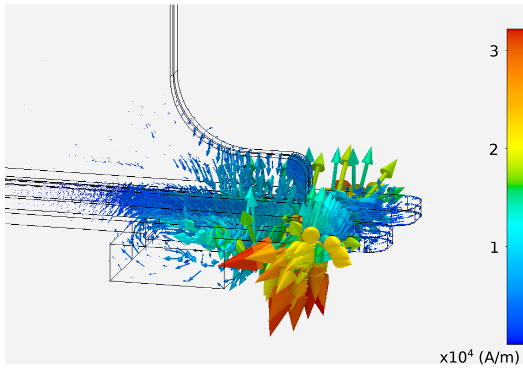


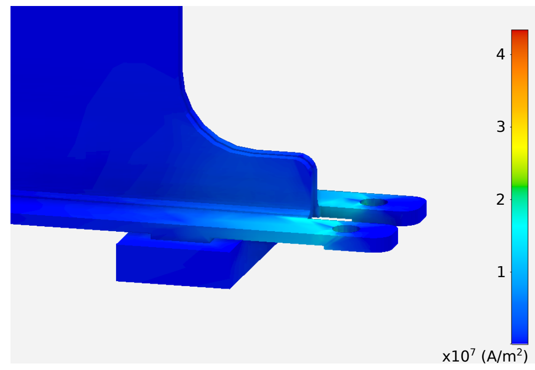
Figure 3.9: Parasitic schematic diagram of DPTR busbar.

ANSYS FEM Modelling of DPTR Busbar — Applying these formulae to an actual busbar structure is usually done by a Finite Element Method (FEM) modelling software due to the complexities of the geometry. This allows for an understanding of the complex Current Commutation Loop (CCL) [130]. Figure 3.9 shows the equivalent circuit of the DPTR including the ESL of the capacitors. As previously mentioned, each capacitor also has an ESR, however, this is not shown in the equivalent circuit. Inductive paths do exist between the three capacitors which may result in some oscillatory behaviours, but it is assumed that the CCLs during switching transitions can be solely considered as $L_{s,1}$, $L_{s,2}$, and $L_{s,3}$.

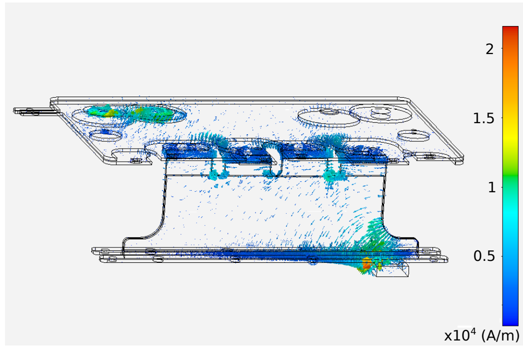
The FEM software package ANSYS [131], with the MAXWELL 3-D engine, was used to investigate the three CCLs shown in Figure 3.9. The original CAD files used in the design stage were run through the solver with a large copper block used in place of the power module (grey box in Figure 3.9). The source and return current injection terminals were connected to the busbar for the $L_{s,1}$, $L_{s,2}$, and $L_{s,3}$ CCLs where $C_{decouple}$, $C_{dc-link,1}$, and $C_{dc-link,2}$, respectively, would normally be connected.



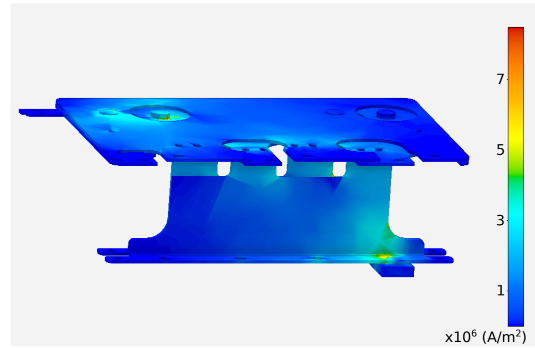
(a) $L_{s,1}$: Magnetic Field (H).



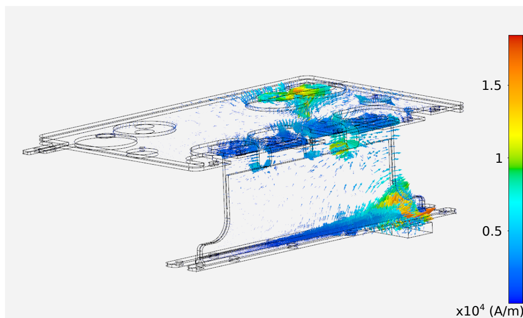
(b) $L_{s,1}$: Current Density (J).



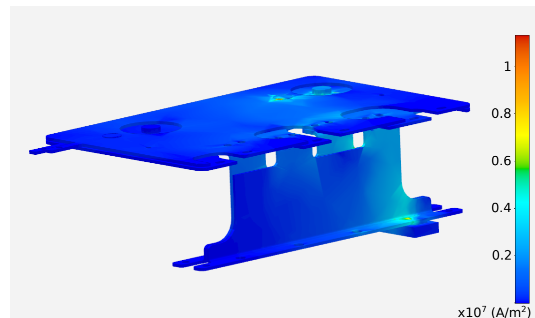
(c) $L_{s,2}$: Magnetic Field (H).



(d) $L_{s,2}$: Current Density (J).



(e) $L_{s,3}$: Magnetic Field (H).



(f) $L_{s,3}$: Current Density (J).

Figure 3.10: FEM modelling of L_s with 500 A excitation current.

Figure 3.10 shows magnetic field intensity (A/m) plots and current density (A/m^2) plots for the busbar with a 500 A operating current. It can be seen in Figure 3.10a, where $C_{decouple}$ connects, that the protruding copper bars exhibit a large magnetic field intensity. This is due to the lack of flux cancellation and relatively high level of L_i here. In Figures 3.10c and 3.10e, the areas in which there are wide parallel plate conductors show very low magnetic field intensity. However, where the current density is high in the areas close to the edges, specifically

in the region where the power module connects to the busbar, the magnetic field intensity increases. Table 3.3 shows the stray inductances that the solver computed. The copper block (that is used to short the connection where the power module would be) was analysed itself and it's inductance values are subtracted to ascertain only the inductive elements of the busbar.

Busbar L_s	**Inductance**		
	DC	AC 10 kHz	AC 10 MHz
$L_{s,1}$	16.7 nH	12.6 nH	12.3 nH
$L_{s,2}$	53.2 nH	31.7 nH	31.4 nH
$L_{s,3}$	53.0 nH	32.8 nH	32.5 nH

Table 3.3: Busbar stray inductance (L_s).

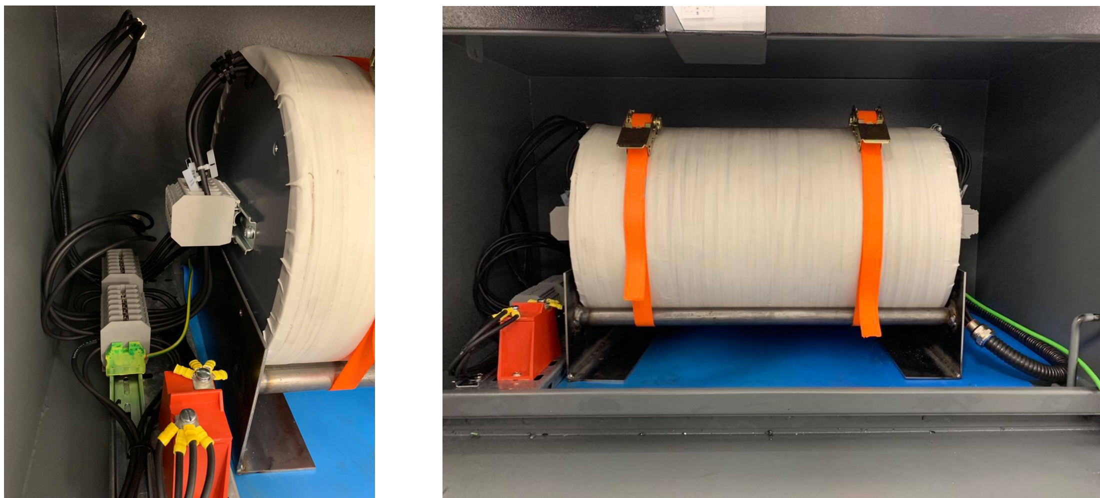
When considering the total inductance of each CCL, the power module's own internal stray inductance (which is in series) must be added to these values (shown in Figure 3.9). The impact of this stray inductance will be further discussed in Section 3.5.

3.3.2.3 Bleed Resistor

As there is a significant amount of energy stored in the capacitive bank, a bleed resistor (R_B) is permanently connected in parallel as shown in Figure 3.4. This is a high-power wire wound resistor of 30 kΩ. This was chosen to be high in magnitude so that there is little discharge during the period of time between the charging phase and the double-pulse phase. Bleed resistors are almost always used so that capacitors self discharge after use. When series connected capacitors are used, individual bleed resistors will be used for each capacitor. This has the added benefit of ensuring that voltage is split equally between the stack.

3.3.3 Inductive Load

The load (L_{Load}) used in the DPTR is a large 957 μH air-cored inductor (shown in Figure 3.11). This is housed inside a large steel box underneath the rig and strapped to a steel cradle, this can be seen in Figure 3.1. The housing is used to contain/reduce the level of magnetic field for safety reasons and to ensure it does not impact any measurement or control hardware.



(a) Side view. (b) Front view.

Figure 3.11: Photograph of DPTR inductive load (L_{Load}).

A power inductor is typically formed by winding an insulated wire round a core. A core is used to confine and guide the magnetic field within an inductor, and is made from various ferromagnetic or ferrimagnetic materials. The properties of a core can greatly influence inductor performance. These can be negative impacts due to core losses which heat the core and can vary the inductance and/or core saturation. A cylindrical air-cored inductor was chosen for L_{Load} as it means that the inductance value would remain constant and core will never saturate. In order to reach large inductance values, an air-cored inductor requires more turns for a given inductance value than a magnetic-core. The inductance (L) of

a cylindrical inductor is expressed as (3.17)

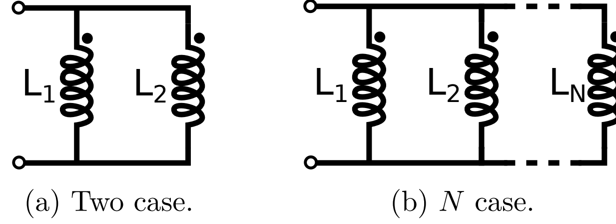
$$L = \mu_o \mu_r \frac{N^2 \cdot A}{l} \qquad \text{[H]} \tag{3.17}$$

where: μ_o is the permeability of free space; μ_r is the relative permeability (for air or vacuum $\mu_r = 1$); N is the number of turns; A is the cross-sectional area of the inductor; and l is the length of the inductor.

L_{Load} is made up of five parallel windings of cable rated at 60 A (4 AWG—21.2mm^2), 2.5 kV ($\sim$ 470 m in total). This gives a DC rating of 300 A, however, considering the short pulses of current, L_{Load} should be suitable for $\sim$1500 A (pulsed). A large Polyvinyl Chloride (PVC) hollow tube (30 cm in diameter and 80 cm in length) was used as the coil former. The μ_r of PVC is approximately 1.0 and therefore has no impact on Equation (3.17). The individual windings were wound one on top of the other with a layer of woven glass cloth tape in between each. Multiple layers of the glass cloth tape were then applied to the outside of the completed inductor. This tape was used to provide structural integrity under a fault condition which may cause the excessive magnetic fields to force the various coils apart. As the cross-sectional area increases for each subsequent winding, the inductance increases accordingly. Each winding also uses a longer length of cable due to the increased diameter, therefore, its ESR also marginally increases. This can be seen in Table 3.4. Parallel inductors would normally follow the sum of reciprocals law, however, there is mutual coupling between them which needs to be considered. For the case of two mutually-coupled parallel connected coils, the equivalent inductance (L_{eq}) can be expressed as (3.18)

$$L_{eq} = \frac{L_1 L_2 - {M_L}^2}{L_1 + L_2 - 2M_L} \qquad \text{[H]} \tag{3.18}$$

where: M_L is the mutual inductance between the two coils of inductance L_1 and L_2 (provided the current flow is in the same direction) as shown in Figure 3.12a.



(a) Two case. (b) N case.

Figure 3.12: Mutually-coupled parallel inductors.

For the case of N mutually-coupled parallel inductors (Figure 3.12b), the equivalent inductance can be expressed as a ratio of the determinants of two matrices which combine the various mutual and self inductances [132]. This becomes more complex when the inductors have asymmetrical ESR and inductance magnitudes, which is the case for L_{Load}. A precision magnetics analyser from Wayne Kerr Electronics was used to characterise the individual windings and the overall L_{Load}. The values for which are listed in Table 3.4.

Winding	Inductance	ESR
$L_{Load,1}$	895 μH	350 mΩ
$L_{Load,2}$	944 μH	360 mΩ
$L_{Load,3}$	1030 μH	374 mΩ
$L_{Load,4}$	1116 μH	387 mΩ
$L_{Load,5}$	1116 μH	414 mΩ
L_{Load}	957 μH	50.6 mΩ

Table 3.4: Characteristics of DPTR inductive load (L_{Load}).

Additionally, an inductor also has a parasitic parallel capacitive element. This arises from inter-winding capacitances. The impact of this capacitance is only at high-frequencies which can significantly alter an inductor's impedance characteristics over frequency. Figure 3.13 shows the impedance vs. frequency of L_{Load} (blue line) measured using the magnetics analyser. At low frequencies the 957 μH of inductance is shown, however at frequency of approximately 100 kHz and above, the measured inductance value significantly changes. This is due to

self resonant frequency (f_o) of the inductor. At frequencies $< f_o$ the inductor possesses mostly inductive traits; at frequencies $\approx f_o$ the inductor is effectively an open circuit; and at frequencies $> f_o$ the inductor appears capacitive, hence the negative inductance reading. This capacitance is an inter-winding capacitance, both between consecutive coils within the individual windings and between adjacent windings (from the mutually-coupled parallel construction). This parasitic capacitive element (C_{par}) is in parallel with the inductor.

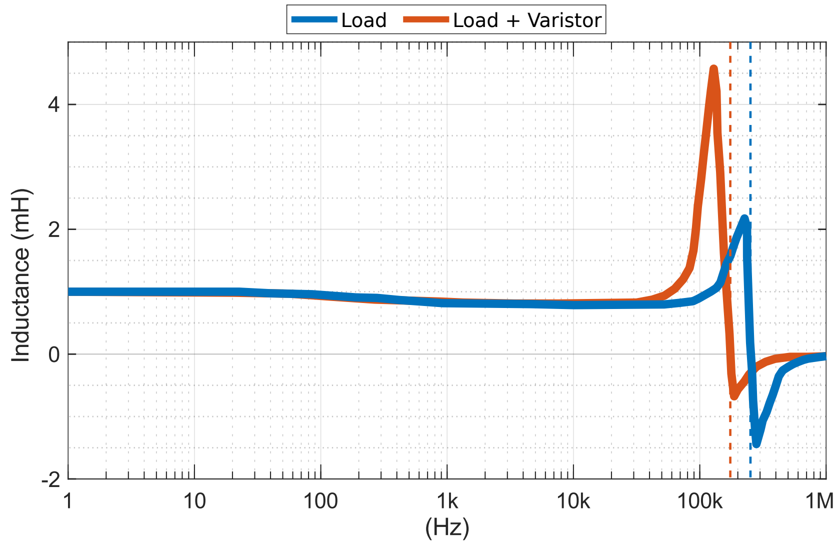


Figure 3.13: Inductance vs. frequency of L_{Load}. Measured using magnetics analyser from Wayne Kerr Electronics.

At f_o the measured reactance is zero and can therefore be read off Figure 3.13. At this particular frequency the parasitic capacitor reactance (X_C) cancels out the inductor reactance (X_L), as shown in (3.19). This can be expanded using the impedance of each component, as expressed in (3.20)

$$X_L \approx X_C \tag{3.19}$$

$$2\pi f L \approx \frac{1}{2\pi f C} \tag{3.20}$$

This can be rearranged in order to calculate C_{par}, as shown in (3.21)

$$C_{par} \approx \frac{1}{(2\pi f_o)^2 L_{Load}} \quad [\mathrm{F}] \tag{3.21}$$

The measured f_o of L_{Load} in Figure 3.13 (blue line) is 250 kHz which yields a C_{par} of 423 pF.

A Metal-Oxide Varistor (MOV) was initially connected in parallel with L_{Load} to be employed as a protection device should there be a power module failure (V242BB60 from Littelfuse). A MOV is a voltage-dependent nonlinear device that provides transient suppression at a certain voltage — this can be seen in Figure 3.11 (red component). During the commissioning phase it was found that parasitic capacitance of the MOV, along with the inductance of the connecting wires, was resulting in oscillatory behaviour. Therefore, the MOV was disconnected. The orange curve in Figure 3.13 shows the impact of the parallel connected MOV on L_{Load}. This results in $f_o \approx 180$ kHz which corresponds to an effective C_{par} of 817 pF, almost double that of the original parasitic capacitance of L_{Load}.

3.4 DPTR Full System & Associated Components

This section will highlight the full system and the associated components which are necessary in converter design.

3.4.1 System Architecture

A combination of MATLAB [133] and LabVIEW [134] was used to fully automate the charging procedure, firing commands, and high-bandwidth data acquisition for the DPTR. The full system diagram is shown in Figure 3.14.

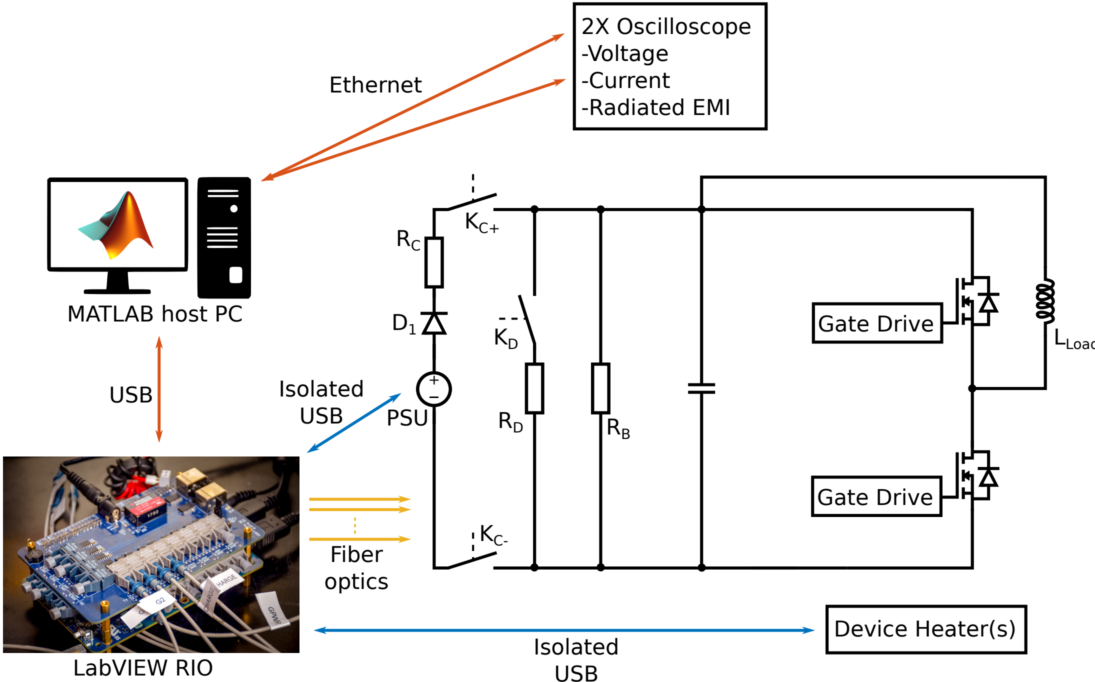


Figure 3.14: Overview of the full DPTR platform [135].

3.4.1.1 Controller Platform

An embedded version of LabVIEW was deployed on a MyRIO development board. This board uses the Zynq-7000 System on a Chip (SoC) which is an integrated ARM Cortex processor and Field Programmable Gate Array (FPGA). This is an ideal system as it allows for accurate FPGA based pulse timing for the firing signals and various communication drivers on the processor. A custom high-speed optical interface PCB was designed to be used in conjunction with the MyRIO. This allows for fiber-optical based control of the power circuit. Fiber-optics (for the MOSFET firing commands and the opening/closing of contactors) and isolated USB cables (for the PSU and heater controllers) were used for safety and to the minimise common-mode coupling paths. A photograph of the MyRIO board with the optical interface board atop can be seen in the bottom left of Figure 3.14. A Finite State Machine (FSM) was used to make sure the DPTR functions as expected — an overview of this is summarised in Table 3.5.

	Step	Tasks
1.	Initialise	Perform system checks and configure comms with PSU.
2.	Charge	Close K_C, open K_D, and charge capacitive bank.
3.	Test	Open K_C, perform double-pulse test.
4.	Discharge	Close K_D.

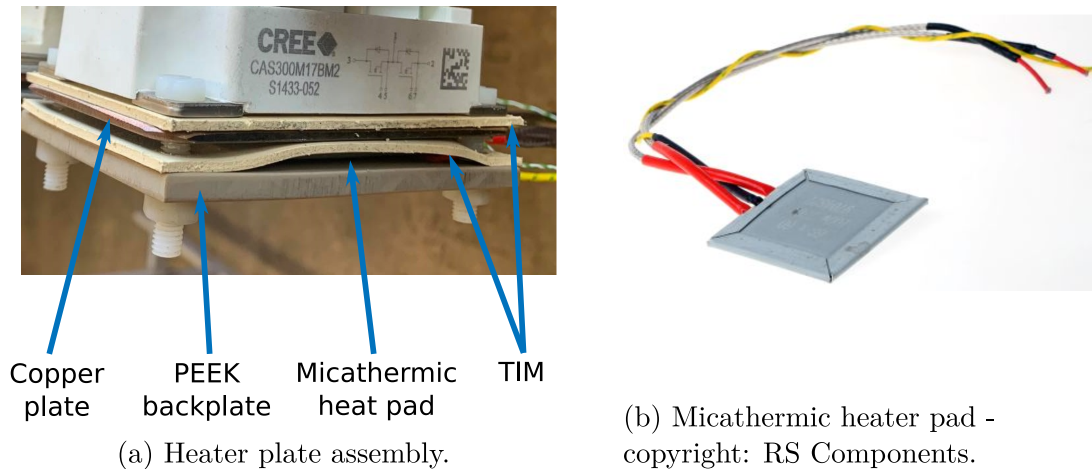
Table 3.5: LabVIEW FSM for DPTR.

Steps 2 and 3 can be repeated as many times as required, with varying set-points, before moving onto step 4.

A host computer running MATLAB is used as the main user interface to the test platform. A variety of functions were built which: communicate with the LabVIEW system to set up test routines and move the FSM through its stages, whilst using various "handshakes" to ensure correct and safe operation; set up and pull measurement data from two oscilloscopes; and process, display, and save the test data.

3.4.1.2 DUT Heat Source

By itself, the power circuit for the DPTR does not fully synthesise converter conditions. Most notably, normal device operating temperature is not reached due to the extremely low duty cycle of the testing. Therefore, the DUT requires an additional heat source to test under realistic conditions.



(a) Heater plate assembly.

(b) Micathermic heater pad - copyright: RS Components.

Figure 3.15: DUT heat source.

The heat source in the DPTR is realised by a heater plate assembly attached to the DUT where the heatsink usually connects. The heater plate assembly is shown in Figure 3.15a. It consists of: a Polyether Ether Ketone (PEEK)[3] backplate; a micathermic heater pad (Figure 3.15b); a 3 mm copper plate to provide thermal capacity; two Thermal Interface Material (TIM) silicone pads used to provide low thermal impedance and aid heat transfer; and a type T thermocouple. A micathermic heat pad is essentially a heating element comprising a resistive wire wound round a mica[4] sheet. The temperature is controlled by a PID controller from Omega. The controller uses the thermocouple to monitor the copper plate's temperature and controls the state of a Solid-State Relay (SSR) in

[3]PEEK is a high-temperature thermally insulating engineering plastic.

[4]Mica can be a variety of phyllosilicate crystals that have near perfect basal cleavage.

series with the heating element to maintain the desired operating temperature. A custom enclosure which has two separate controllers was built and fitted with optically isolated USB interfaces. This allows for independent control of two devices with temperatures up to 150 °C.

3.4.2 Gate-Drivers

Gate-drivers are an essential associated component for power transistors. As explained in Chapter 2, they are responsible for turning the device on and off. A gate-drive Integrated Circuit (IC) translates a logic-level control signal into a signal which has the correct voltage levels and current capability. There are, however, other components that are required in order to achieve this functionality, usually with additional performance and protection features. The “gate-drive” blanket term is often used when describing this overall gate-driving circuitry.

3.4.2.1 Basic Gate-Driver Functionality

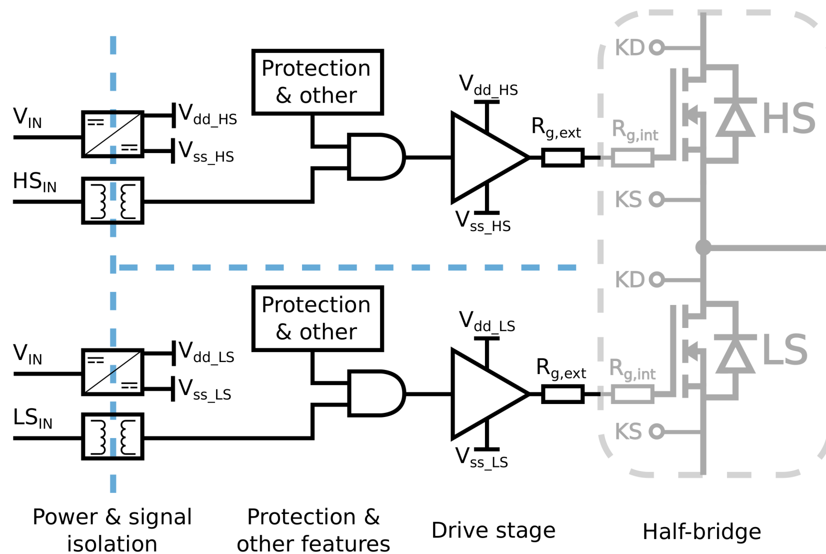


Figure 3.16: Basic gate-drive functionality.

A block diagram showing the core components of a traditional half-bridge gate driver are shown in Figure 3.16.

Power & Signal Isolation — The blue dashed line in Figure 3.16 represents the isolation barriers that exist. Gate-driver isolation is primarily required for two reasons — functionality and safety. The functionality aspect is in terms of: Common-Mode Transient Immunity (CMTI) from the high slew-rate (dV/dt) transients at the transistors; level shifting the gate-drive signal to the reference of the HS switch; and to reduce cross-talk or parasitic induced turn-on of a device. An isolated DC-DC converter provides the power to both the LS and HS switch. This will typically have a bipolar output for V_{dd} and V_{ss}, the positive and negative voltage rails respectively, to drive the gate of the transistor to. There are other techniques to achieve the HS biasing, such as diode bootstrapping and capacitive charge pump circuitry, however in high-power application an isolated supply tends to be used. There are three main methods of achieving galvanic isolation for the firing control signal:

- **Magnetically** — a high-frequency carrier wave is used to pass the signal over a transformer.
- **Optically** — a Light-Emitting Diode (LED) and phototransistor are used to transfer the signal.
- **Capacitively** — capacitor structure used to pass control signal.

An isolator IC comes with: insulation ratings, such as maximum working, transient, and surge voltage; a CMTI rating, usually 100s of V/ns for WBG drivers (with coupling capacitance rating); and propagation delays.

Protection & Other Features — A gate-driver may also include other operational and protection features:

- **Dead-Time** — Due to the non-instantaneous switching of transistors, dead-time compensation is used in hard switched inverter applications. This is a small delay period between the gating signal of the HS and LS devices to prevent them simultaneously conducting, resulting in a short circuit of the DC-bus [136]. This can be implemented in a converter control system using a variety of techniques or the function can be applied in the gate-driver circuitry.
- **Over-Current Protection (OCP) & Short-Circuit Protection (SCP)** — When the device current is above the nominal current rating and becomes desaturated, fast protection circuitry can be employed to safely turn the device off. This can be due to: a short-circuit on the DC-bus; load side short-circuit; converter controller error; or other external factors. Over-current scenarios can be detected by the top-level converter control system, however it is governed by the round-trip time of a current sensor signal and the sampling rate of the controller which may not be fast enough.

  The frequently used desaturation (often shortened to desat) detection circuit can be used for both Si-IGBTs and SiC-MOSFETs [137] at the gate-drive level. It works by monitoring the on-state voltage of the transistor and triggering a shutdown sequence if this goes above a set value. The voltage across the transistor can swing between 100s of volts in the off-state and single digit volts in the on-state, therefore, a diode is used in the detection circuit [138]. These circuits are able to turn-off transistors in a very short period of time, with a fault signal usually being sent to the controller.
- **Under-Voltage Lockout (UVLO) & Over-Voltage Lockout (OVLO)** — To ensure that the gate-drive circuitry always maintains full control of the state of the transistor, UVLO and OVLO circuitry is used. This monitors the input supply to the gate-driver and performs a safe shutdown, and turn-off of the transistor, should it go above or below a safe level.

Drive Stage — This includes the specific driving IC and gate resistor(s), as shown in Figure 3.16. This is the stage which is directly responsible for the turn-on and turn-off mechanism, and in particular, influencing the trajectory of the transition. Typical voltage rails (V_{dd} & V_{ss}) for Si-IGBTs are ±15 V, whereas the rails for SiC-MOSFETs are not as standard. For example, rails such as $+20$ V/-4 V and $+18$ V/-6 V are given for the SiC devices. This is one of the areas where transitioning from a Si to a SiC solution is more complex than a simple "drop-in" replacement. Single die devices require a peak sink/source current of 1–3 A, however larger multi-die modules can require upwards of 10 A. Therefore, the driving stage needs to be able to readily provide that current with the required dI/dt. The drive stage generally comprises a push-pull or totem-pole transistor complimentary pair.

Traditionally, $R_{g,ext}$ is chosen to control the trajectory, with an increase in $R_{g,ext}$ slowing the rate of charge into the gate capacitance, thus slowing the switching period. A separate turn-on and turn-off path can be realised by the use of series connected directional diodes or separate connections to the Midpoint (MP) of the drive stage (with no internally connected MP). To reduce inductance in the gate path, the type of resistor used is normally a SMT Metal Electrode Leadless Face (MELF) package due to its extremely low ESL. A high-value pull-down resistor, between the gate and source, is often also used to ensure that V_{gs} cannot float up.

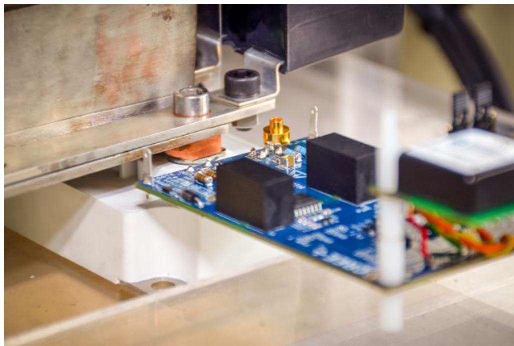
This rudimentary technique of basic driver and gate resistor tuning can be taken further by adopting an active gate driving system. This technique and the relevant literature will be discussed in Chapter 4.

The aforementioned stages for a gate-driver can also be packaged into a single IC for lower power applications. However, gate-drivers used in high-power

applications tend to have these stages in a discrete form.

3.4.2.2 Gate-Drivers used in DPTR

The gate-drivers used in the DPTR are shown in Figure 3.17. The CGD15HB62P1 gate-driver from Cree (Figure 3.17a) and the L6100231 Skyper 32 Pro R gate-driver from Semikron (Figure 3.17b) are interfaced by a custom power and signal PCB. This PCB has a low coupling capacitance isolated DC-DC converter and fiber-optical receivers for the firing signals. This, in turn, is powered by an isolated AC-DC supply. These isolation stages were all employed to strengthen the common-mode immunity.



(a) CGD15HB62P1 (Cree). SiC-MOSFET driver.

(b) L6100231 SKYPER 32PRO R (Semikron). Si-IGBT driver.

Figure 3.17: Half-bridge gate-drivers used in DPTR.

During the commissioning and tuning stages in the development of the DPTR; a 300 A, 1.2 kV Si-IGBT was used with the Semikrom gate-driver. When performing a test at the same set point multiple times to check for repeatability of results, a significant amount of jitter in time was observed (this was evident as the oscilloscopes are set to trigger on an external optical trigger sent from the LabVIEW board). However, when repeating the test with the Cree gate driver no jitter was present. This was realised to be down to the isolation technique used in the gate-drivers. The Semikron driver makes use of a transformer to magneti-

cally couple the signal, with a carrier frequency of 8 MHz (period = 125 ns). As there is no synchronisation between the gate-driver and the measurement system, there is $\sim$ 250 ns of jitter possible, depending on when during the period of the carrier the signal is latched. The gate-driver from Cree uses capacitive coupling for its isolators and was found to have no jitter at all, with results being very repeatable. Using Equation (3.2), at 500 V the dI/dt of the load is 0.5 $A/\mu s$ and at 1000 V is 1 $A/\mu s$. For a converter, this 250 ns jitter will cause a deviation of $>$ 0.5 A and will pose no issues. However, for the case of the DPTR where ascertaining precise switching characteristic measurements is the objective, the Semikron driver was not used in subsequent experimental work.

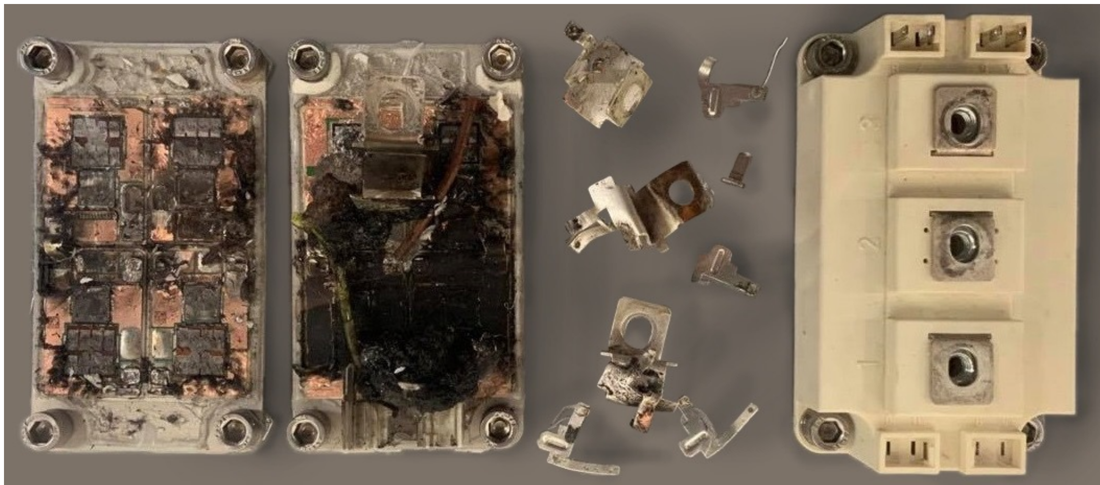
3.4.3 DPTR Commissioning Tests

Various commissioning tests were done during the development of the DPTR. From checking the communication links and tuning the automation to destructive device failure tests. Failure tests were carried out to check the destructive nature of the devices, verify if the plexiglass safety enclosure was adequate, and to further inform the necessary safe working procedures and risk assessments. Figures 3.18a and 3.18b show two Si-IGBTs that were subject to intentional failure tests.

In both tests a Si-IGBT was used. These were 300 A, 1.7 kV (FF300R17KE3) devices from Infineon (Figure 3.18d).

3.4.3.1 Failure Test 1

Both HS and LS devices were turned on causing a short circuit on the DC-bus which was charged to 1.5 kV. This failure is termed a shoot-through. Theoretically, a peak current of 65 kA could be sourced from the 6.26 mF DC-bus into the



(a) Failure test 1. (b) Failure test 2. (c) Internal busbar structure. (d) 62 mm power module.

Figure 3.18: Photograph of device failures from commissioning tests.

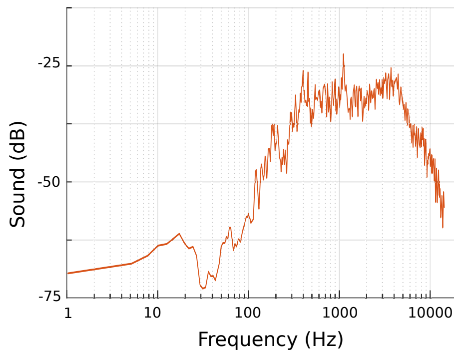
two devices. However, the devices will have failed at a significantly lower amount than this. This failure was very explosive, both audibly and visually. It can be seen in Figure 3.18a that the plastic casing and encapsulation material were blown away. The explosive nature is due to the bond wires instantly vaporising which causes a large gas expansion. At 1.5 kV, there is ∼7 kJ of energy stored in the capacitor bank.

3.4.3.2 Failure Test 2

The second failure test was an over-current of the LS device. The HS device was held off and the LS device was simply turned on. A Rogowski coil on the inductor showed that the device failed at ∼ 3 kA. This test was notably quieter than the first, but with significantly more arcing (the arcing can be seen in Figure 3.19b). This arcing was between the MP connection of the half-bridge (i.e., the inductor) and the DC- terminal of the busbar. This resulted in a large section of burned material as shown in Figure 3.18b. This was due to the stored magnetic energy in the inductor that continued to support the arc up to the point where the voltage

was zero.

Both failure tests resulted in a severe explosion causing damage to the busbar system. However, the safety enclosure contained the blast. Due to the loud noise produced (Figure 3.19a) it was deemed that ear defenders should be worn when testing. The large arc flash and explosion (Figure 3.19b) are shielded by Ultraviolet (UV) blocking welding curtains.



(a) Explosion noise profile. Measured 3 m from test rig

(b) Photograph from above.

Figure 3.19: Intentional failure commissioning tests.

3.5 Effect of Parasitic Elements on Device Switching

Parasitic inductive and capacitive circuit elements can have severe impacts on the transient performance of power semiconductor devices. The switching characteristics shown in Chapter 2 (Figure 2.12 and 2.18) are ideal and do not show any of the realistic behaviours that are present with real devices. Figure 3.20 shows experimental measurements from the DPTR. The DUT is a 300 A, 1.7 kV SiC-MOSFET with SiC-Merged PIN Schottky (MPS) half-bridge module from Cree (CAS300M17BM2 [139]). It can be seen that there is a significant amount of: oscillatory behaviour in V_{ds} and I_d waveforms; voltage overshoot at turn-off;

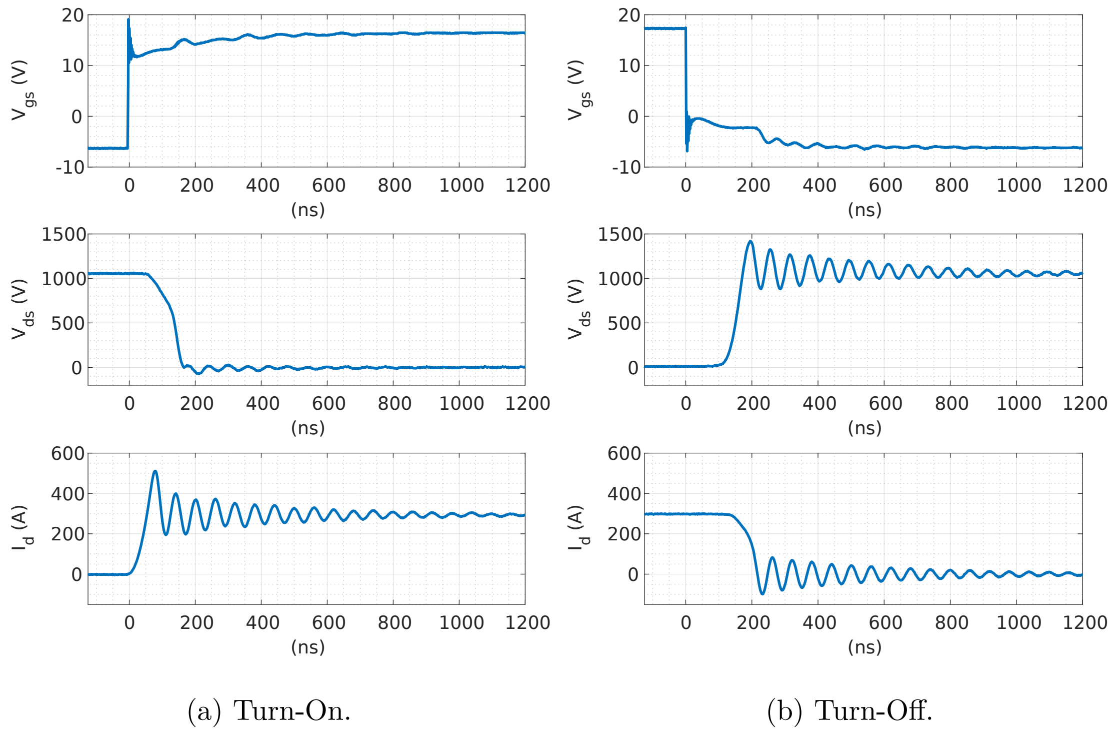


Figure 3.20: Experimental measurements of SiC-MOSFET [139] transient behaviour. Tested at 300 A, 1 kV with device baseplate set to 100 °C.

and current overshoot at turn on.

3.5.1 Current Overshoot at Turn-On (Reverse Recovery)

When the LS device turns on, the reverse recovery current (as explained in Section 2.4.4.1) from the HS FWD and/or body-diode results in an overshoot current. This can be seen in I_d plot in Figure 3.20a. As previously mentioned, SiC-Schottky diodes, which have very little or no reverse recovery, can be employed to reduce this effect, however this most often comes with the addition and/or intensifying of capacitive oscillation from the diode.

3.5.2 Voltage Overshoot at Turn-Off

When the LS device turns off a significant voltage overshoot on V_{ds} occurs. This can be seen in the V_{ds} plot of Figure 3.20b where an overshoot of 37 % (1368 V) is observed. The overshoot voltage (ΔV_{os}) is due to the stray inductance in the CCL and the fast dI/dt [140]. This can be expressed as (3.22)

$$\Delta V_{os} = \Sigma L_{stray} \cdot \frac{dI_d}{dt} \qquad [\mathrm{V}] \tag{3.22}$$

where: ΣL_{stray} comprises all of the stray inductive element as shown in (3.23)

$$\Sigma L_{stray} = L_{s,1} + L_{decouple} + L_{device} \qquad [\mathrm{H}] \tag{3.23}$$

where: $L_{s,1}$ is the CCL busbar inductance obtained from the FEM modelling (16.7 nH); $L_{decouple}$ is the ESL of the decoupling capacitor (< 20 nH); and L_{device} is the total stray inductance of the device (15 nH) [139]. The peak voltage across the switch can then be written as (3.24)

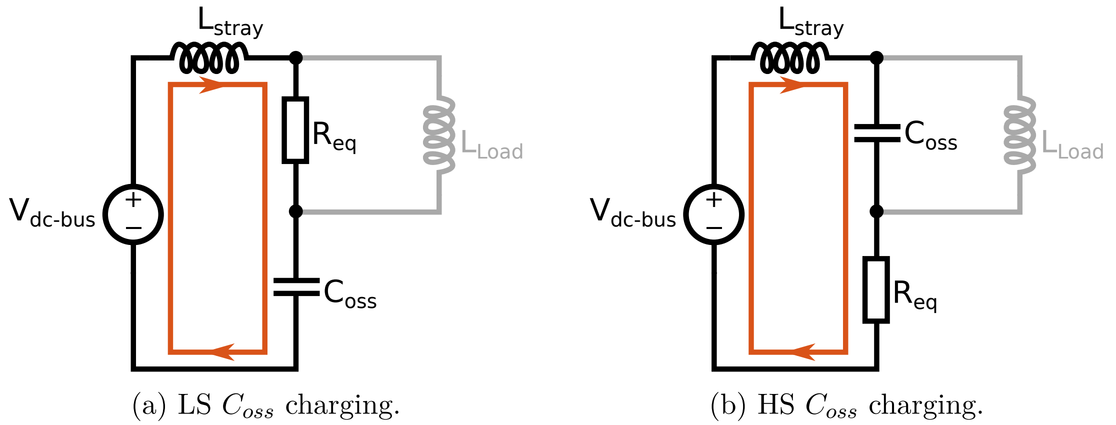
$$V_{ds,peak} = V_{dc-bus} + (L_{s,1} + L_{decouple} + L_{device}) \cdot \frac{dI_d}{dt} \qquad [\mathrm{V}] \tag{3.24}$$

From the I_d plot in Figure 3.20b, the dI_d/dt is measured to be 9 A/ns. Using the above formulae, this would suggest a ΣL_{stray} of 40.8 nH which is approximately the same as that which can be calculated using the known values.

Voltage overshoot is one of the reasons that a device will be typically used at 60–70 % of its rating to give headroom for this peak.

3.5.3 Oscillations in Voltage & Current

Significant oscillatory behaviour in voltage and current are shown in Figure 3.20. The frequency (f_{res}) of this oscillation, for both I_d and V_{ds} at turn-on and turn-off, is measured to be 16.9 MHz. These oscillations arise from two resonant circuits that are formed during transients where the C_{oss} of each device is charged [141, 142]. These two circuits are shown in Figure 3.21.



(a) LS C_{oss} charging.

(b) HS C_{oss} charging.

Figure 3.21: Half-bridge resonant charging circuit. Orange line shows CCL.

Figure 3.21a shows the charging of the LS C_{oss} when the LS has just turned off and the HS FWD is now conducting, and vice versa for Figure 3.21b. These RLC circuits comprise: a resistive element R_{eq}, predominately made up of the device $R_{ds(on)}$ but also includes the ESR of the decoupling capacitor and any other resistive component in the CCL; the total stray inductance L_{stray}, as defined in Equation (3.23); and C_{oss}. The RLC circuits have a natural resonance frequency (f_n) as expressed in (3.25)

$$f_n = \frac{1}{2\pi\sqrt{L_{stray}C_{oss}}} \approx f_{res} \qquad \text{[Hz]} \tag{3.25}$$

rearranging for L_{stray} gives (3.26)

$$L_{stray} \approx \frac{1}{4C_{oss}\pi^2 {f_{res}}^2} \qquad [\mathrm{H}] \tag{3.26}$$

Using the C_{oss} value from the CAS300M17BM2 datasheet [139] (2.5 nF at 1 kV) and the measured f_{res} of 16.9 MHz from Figure 3.20, Equation (3.26) yields a stray inductance of 35.5 nH. This shows good agreement with the previously estimated 40.8 nH from the voltage overshoot analysis and the FEM estimate.

The damping of a RLC circuit is a consequence of its resistive element. This can be described by a damping factor (ζ), which is related to the circuit parameters as expressed in (3.27)

$$\zeta = \frac{1}{2R}\sqrt{\frac{L_{stray}}{C_{oss}}} \tag{3.27}$$

To achieve critical damping of the resonant circuit [143], the critical resistive element (R_{crit}) is given by (3.28)

$$R_{crit} = \frac{1}{2}\sqrt{\frac{L_{stray}}{C_{oss}}} \qquad [\Omega] \tag{3.28}$$

Using the values of L_{stray} ($\sim$ 35.5–40.8 nH), Equation (3.28) yields an R_{crit} of 1.88–2.02 Ω. Considering that the $R_{ds(on)}$ of the device is 8 mΩ, the ESR of $C_{decouple}$ is 4 mΩ, and the busbar resistance will be substantially lower than both of these, the resultant R_{eq} of the resonant circuit is two orders of magnitude less than R_{crit}. Therefore, there is very little damping from the resistive elements resulting in an under-damped system. Techniques such as using snubber circuits and active gate-driving can be used to limit and manage voltage overshoot and

the oscillatory behaviour. These will be discussed and reviewed in Chapter 4.

3.5.4 Further Experimental Results on Parasitic Effects

3.5.4.1 Increase of Stray Inductance

The bottom section of the busbar was adapted to test a different device. This DUT was the BSM600D12P3G001 [144] SiC-MOSFET and SiC-Schottky Barrier Diode (SBD) half-bridge module from ROHM, which is rated for 1.2 kV, 576 A and is housed in the ROHM type-G module (similar to the Infineon EconoDUAL™ module) with 10 nH of internal stray inductance.

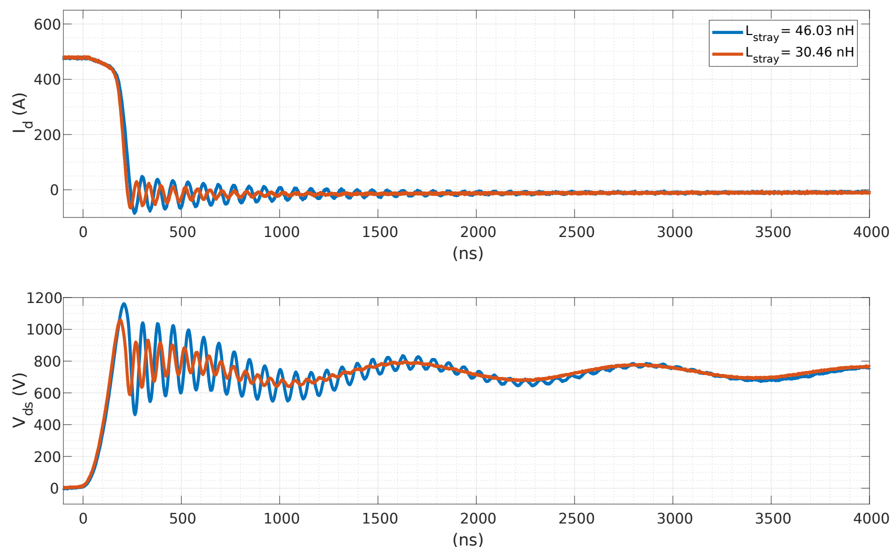


Figure 3.22: Experimental measurements of the SiC-MOSFET BSM600D12P3G001 [144], showing impact of increased L_{stray}. Tested at 480 A, 750 V with device baseplate set to 100 °C.

Figure 3.22 shows the turn-off transition for this device with two different values of L_{stray}. This was not an intentional investigation, rather a realisation that the L_{stray} was initially too much and required reducing. On the first attempt (blue line in Figure 3.22), when testing the device at 480 A which is much less than rated current, it was observed that the overshoot voltage was nearing the

rated breakdown voltage for the device. The improved design (red plot) shows a reduction in overshoot of $\sim$ 140 V. This improvement was achieved by placing the high-frequency decoupling capacitor closer to the device terminals, thus reducing L_{stray}. It can also be seen that there is significantly reduced amplitude of the high-frequency oscillations. Using the previous approach — Equations (3.22) & (3.26) — L_{stray} was found to be 46.03 nH and 30.46 nH, for the initial and improved attempt, respectively.

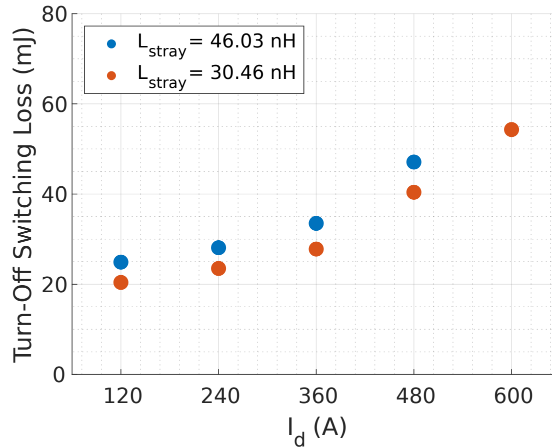
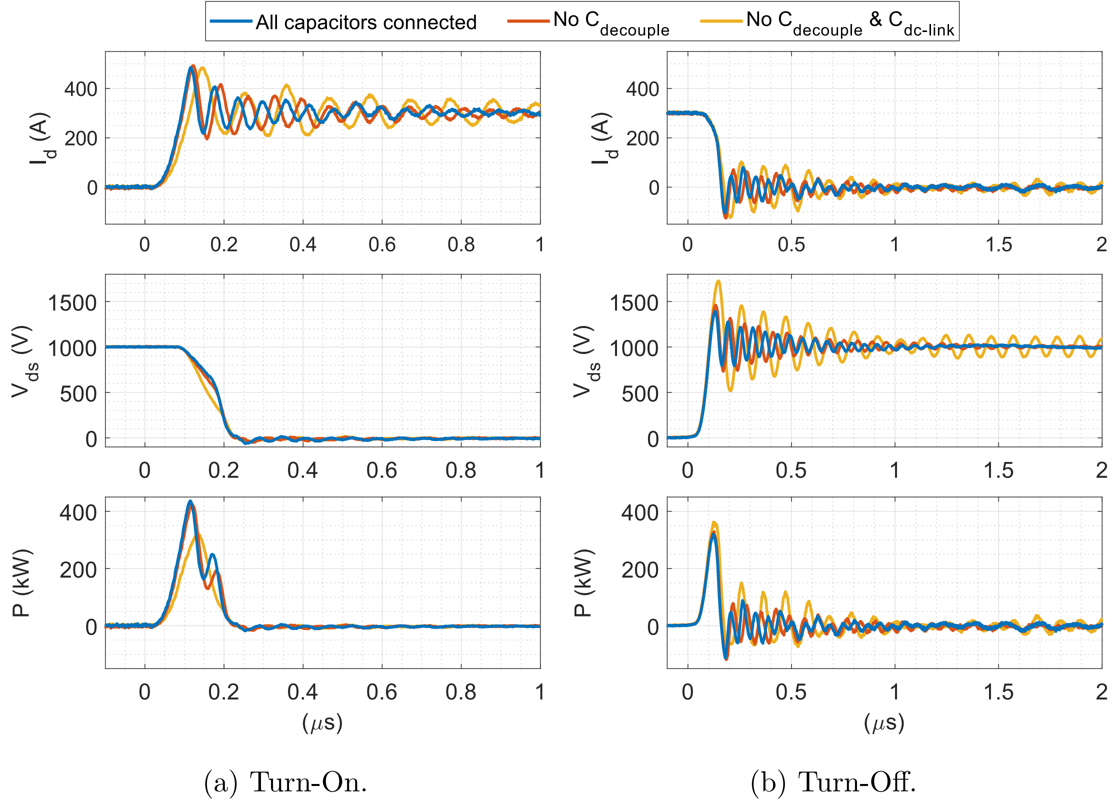


Figure 3.23: Turn-off switching loss energy of the SiC-MOSFET BSM600D12P3G001 [144], showing impact of increased L_{stray}. Tested at 750 V with device baseplate set to 100 °C.

The switching energy associated with the turn-off transient for the two L_{stray} arrangements are shown in Figure 3.23. It can be seen that a larger stray inductance results in a higher level of switching loss. This is due to the increased overshoot and magnitude of oscillations. In order to avoid exceeding the 1.2 kV voltage rating, a test at 600 A was not performed for the larger L_{stray}.

3.5.4.2 Removing Decoupling Capacitors



(a) Turn-On.

(b) Turn-Off.

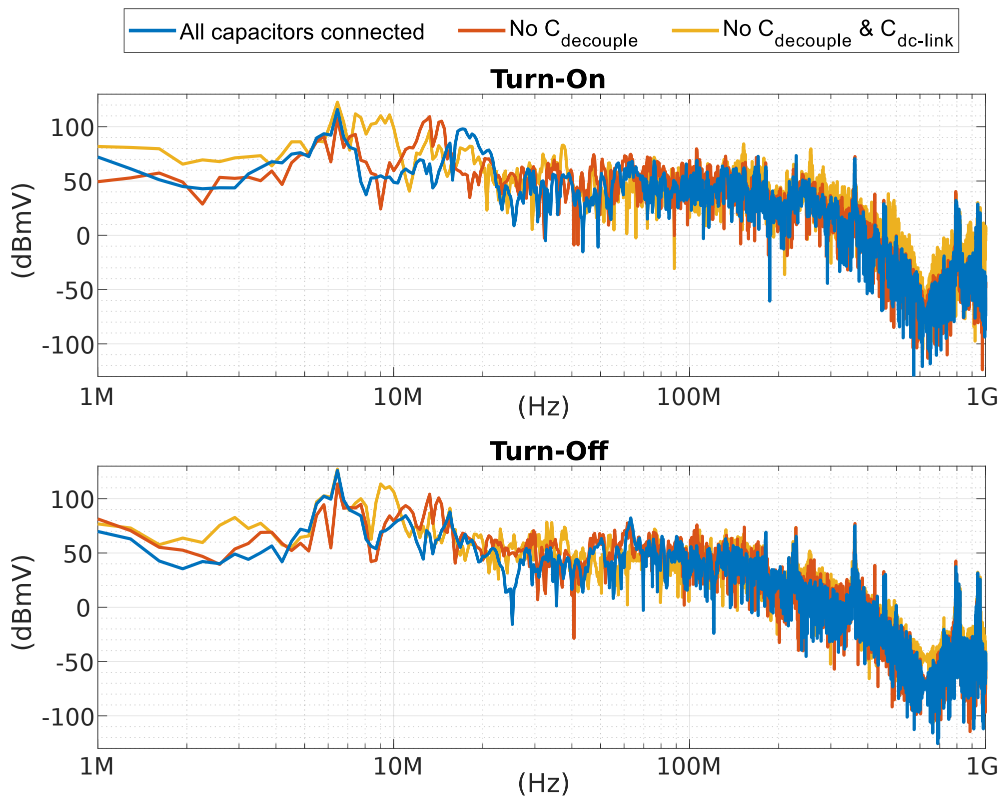
Corresponding FFT of antenna measurement shown in Fig. 3.25.

Figure 3.24: Experimental measurements of the SiC-MOSFET CAS300M17BM2 [139], showing impact of removing decoupling capacitors. Tested at 300 A, 1000 V with device baseplate set to 100 °C.

The plots in Figure 3.24 show how removing decoupling capacitors impact the switching characteristics. The blue line shows the performance when both the high-frequency decoupling capacitor ($C_{decouple}$) and the two DC link capacitors ($C_{dc-link}$) are connected — i.e. normal conditions; the orange line has $C_{decouple}$ removed; and the yellow line shows the switching transients when both the $C_{decouple}$ and $C_{dc-link}$ capacitors are removed, therefore all of the charging currents are sourced from the large 5.4 mF bulk capacitor through a relatively high inductance path. It is clear from Figure 3.24 that the effective L_{stray} has been increased as the frequency of resonance has changed. This is particularly apparent in the turn-

off waveforms (Figure 3.24b) where the overshoot voltage is significantly higher, this in turn results in a larger magnitude of the oscillatory behaviour.

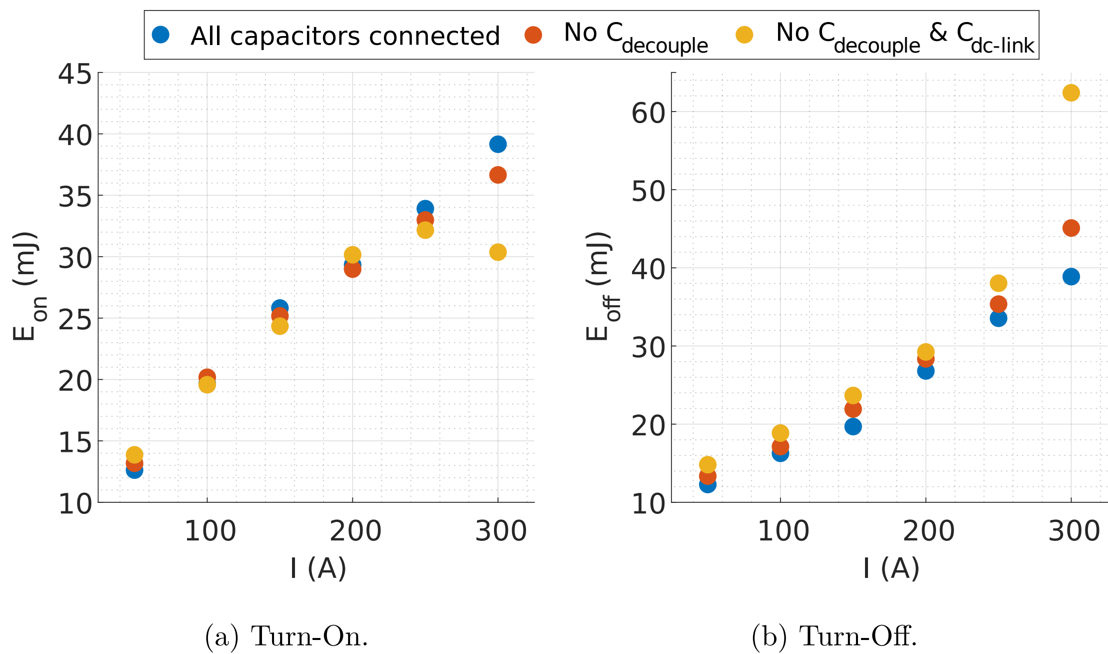
The FFTs of the corresponding radiated RF emissions are shown in Figure 3.25. The increase in emissions at the resonant frequencies evidently increase for the cases with the capacitors removed, with the blue line (all capacitors connected) showing the lowest overall level of emissions for both turn-on and turn-off. These plots confirm that the increase in oscillatory behaviour and overshoot — from removing the decoupling capacitors — has a significant impact on the amount of EMI which is generated from a switching event.



Corresponding voltage & current waveforms shown in Fig. 3.24.

Figure 3.25: FFT of antenna measurements.

The turn-on and turn-off switching energy losses are shown in Figure 3.26. For the turn-off transition (Figure 3.26b), it can be seen that the decoupling capacitor has a considerable impact on the switching energy, with an increase of 16% loss at 300 A. In general, the turn-on switching loss (Figure 3.26a) does not exhibit any discernible difference, however the 300 A case curiously shows a lower level of loss for the configuration where both $C_{decouple}$ and $C_{dc-link}$ are removed. This is due to the resonance decreasing in frequency, resulting in the first trough of the current oscillation occurring when V_{ds} has reached the on-state voltage level. This is affirmed by observing the instantaneous power plot in 3.24a.



(a) Turn-On.

(b) Turn-Off.

Figure 3.26: Switching loss energy of the SiC-MOSFET CAS300M17BM2 [139], showing impact of removing decoupling capacitors. Tested at 1000 V with device baseplate set to 100 °C.

3.5.5 Electromagnetic Interference (EMI) Impact of Device Transients

Due to the high values of dI/dt and dV/dt, from the fast rise and fall times and the high-frequency oscillations in voltage and current, EMI can pose serious issues. This can make complying with EMC standards difficult. EMI can be described as Conducted Emissions (CE) and/or Radiated Emissions (RE), with a few different mechanisms leading to each.

In PE switch-mode converters, Common-Mode (CM) currents are created from the fast dV/dt of the switching devices. Any associated parasitic capacitance (C_{par}) that is subject to this dV/dt gives rise to this CM current (I_{CM}), as expressed in (3.29)

$$I_{CM} = C_{par} \frac{dV}{dt} \qquad [\text{A}] \tag{3.29}$$

The resultant I_{CM} can then propagate through any conductor or other capacitive element (parasitic or intentional) in the system. The half-bridge arrangement, plus other typical system components in a two-level converter, is shown in Figure 3.27. This system diagram shows many of the parasitic coupling capacitances (in blue) and the possible I_{CM} paths (in orange).

The three capacitors connected between the heatsink and the half-bridge represent a complex distributed capacitance. However, as the MP node experiences the full voltage swing ($\pm\ V_{dc}$), the capacitance between this point and the heatsink is of most significance [145]. The gate-driver stage can also pose a significant weak point due to the capacitances across the isolation barriers. The grounding connections of the gate-drive/control circuitry ($\stackrel{\perp}{=}2$) and heatsink ($\stackrel{\perp}{=}3$)

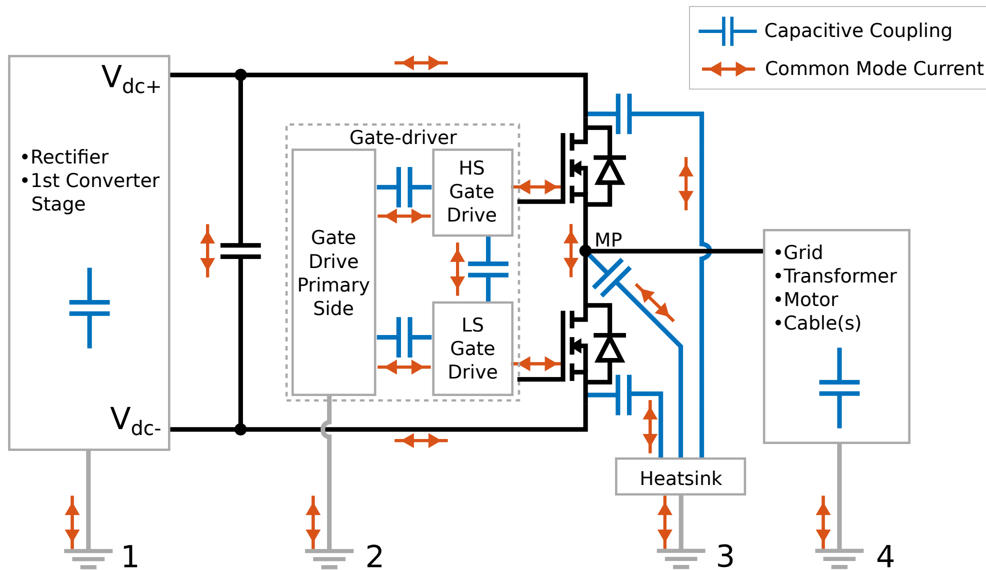


Figure 3.27: Capacitive coupling paths and common-mode current paths in a typical two-level converter system.

provide the required loop for I_{CM} to be established. All of the ground points (⏚) in typical systems are common connections through intentional bonding or any other miscellaneous conductive pathways through the system enclosure. Figure 3.27 illustrates that many I_{CM} loops can be formed throughout the system — whether that is localised to the two-level converter and it's associated components or encompasses the input and/or the output stages and any conductors in the system. Although it is not shown in Figure 3.27, the transistor parasitic capacitances (Figure 2.11) can provide coupling paths between the devices.

When considering the dV/dt magnitudes for WBG devices (20–50 V/ns), even as little as 1–10s of pF of capacitance can result in several tens of mA of I_{CM}. This I_{CM} can cause small voltage perturbations which, if on low-voltage circuitry, can lead to unintended behaviours. This is of particular importance in gate-drive circuitry, where a voltage perturbation could momentarily turn-on a device if V_{Th} is surpassed. This is one of the reasons that the transistor gates are driven to a negative voltage [146]. In the DPTR, fiber-optical cabling was used wherever possible to avoid these coupling paths. That situation addresses conducted EMI

issues internal to the half-bridge, however CE EMC levels can be broken by I_{CM} propagating to other victim systems through grounding connections. Therefore, it can be beneficial to place Y-capacitors[5] between neutral and/or live to ground at the input to the rectifier stage, thus creating a small loop for I_{CM} (i.e. MP $\rightarrow$ ⏚3 $\rightarrow$ ⏚1 $\rightarrow$ Y-capacitor $\rightarrow$ V_{dc-} or V_{dc+} $\rightarrow$ LS or HS device). If this isn't done, a loop may be established that encompasses another system and the interconnecting cables, thus disturbing that other system. Another way to limit the common-mode, in both high-voltage power circuits and low-voltage gate-drive circuits, is to use a common-mode choke. In motor and generator based applications, I_{CM} can cause serious issues if these machines are subject to it, with bearing currents and shaft voltages widely reported on [82].

Radiated Emissions (RE) EMI can be classed as near-field or far-field. Near-field comprises capacitive/electrostatic coupled E-field or inductive/magnetically coupled H-field, whilst far-field covers Electromagnetic (EM)-field radiation. E-field is similar to what was previously discussed, with regard to fast dV/dt and I_{CM}. However, these fast dV/dt's also result in radiated E-field. Good design practice to reduce this is to minimise conductor area at high dV/dt nodes, thus reducing its antenna properties — for example, at the MP node. H-field radiation arises from the magnetic field generated by any stray inductance and, in the main, the Differential-Mode (DM) currents that flow in the CCLs. It is the AC component, oscillations and fast dI/dt, of the current that generates the H-field. These generated fields can inductively couple to another circuit resulting in an induced voltage.

[5] Any capacitor placed between live and/or neutral to ground on the ac side will be a Class-Y type. Class-Y capacitors are limited in value to reduce leakage current, are high-voltage rated to avoid short-circuits, and are self-repairing.

The induced voltage ($V_{ind.}$) on the victim can be expressed as (3.30)

$$V_{ind.} = M_L \frac{dI}{dt} \qquad [\text{V}] \tag{3.30}$$

where: M_L is the mutual inductance between the aggressor and the victim. To reduce this, a low loop inductance (L_{stray}) for the power circuit is essential. This is achieved by low-inductance layout and the use of well-placed, high-quality decoupling capacitors. As shown theoretically in Section 3.3.2 and experimentally in Section 3.5.2, this is also of great relevance to switching performance. Reducing any loop inductance, or rather antenna, of the victim also prevents unwanted magnetic coupling. A potential victim circuit could be a gate-driver as it is in close proximity to the power circuit. Therefore, good EMI design practice is also required in gate-drivers to reduce their susceptibility. There also exists a possibility for I_{CM} to radiate H-field should the conducting path act as an antenna.

The far-field radiation consists of an EM wave which is the result of a E-field vector and H-field vector perpendicular to each other — with the H-field component a result of low impedance inductive loops and the E-field component a result of high impedance monopoles or dipoles (where the length of the antenna is $> \lambda/4$, where λ is the wavelength). The planar EM wave is formed at a specific distance (D_{EM}) from the source, as expressed in (3.31)

$$D_{EM} = \frac{\lambda}{2\pi} \qquad [\text{m}] \tag{3.31}$$

where:

$$\text{Near-field} : 1 < \frac{\lambda}{D_{EM} 2\pi}$$

$$\text{Far-field} : 1 > \frac{\lambda}{D_{EM} 2\pi}$$

These EMI phenomena have always been an issue with electronics. However, due to the magnitudes of power involved in PE, power converters require very stringent EMC design considerations. With the move from Si based PE to WBG based converters, EMI issues are compounded by the faster rise/fall times and amount of oscillatory behaviour. The current frequency boundaries for EMC testing are 0.15–30 MHz for CE and 0.03–1 GHz for RE. It is reported that standards agencies and working groups are considering increasing the upper limits of these boundaries as required to take account of the higher frequencies (both the fundamentals and the resultant harmonics) associated with WBG devices and the converter switching frequencies now possible [147].

3.6 High-Bandwidth Measurement Equipment

Investigations into high-power converter circuit topologies, where the switching frequency is in the order of 1–20 kHz, do not require particularly high-bandwidth measurement systems. However, when investigating the switching transients of power semiconductor devices, as is the case in this study, there is a need for high-bandwidth equipment.

The following subsection will discuss the measurement equipment and methodologies used in the experimental work for this study.

3.6.1 Oscilloscope

An oscilloscope (scope) is used to measure, view and save the time-varying electrical signals of a circuit. The commonly used approximation for the effective bandwidth (i.e. the -3dB point) of an oscilloscope is expressed as (3.32) [148]

$$\mathrm{BW} = f_{3dB} \cong \frac{N}{t_r} \qquad [\mathrm{Hz}] \tag{3.32}$$

where: t_r is the rise time (10–90 %) of the signal; and $N = 0.339$ for a Gaussian response scope (however, industry has settled on $N = 0.35$) and $N = 0.4$ to 0.5 for a flat response scope [149]. The majority of high-bandwidth scopes make use of a Gaussian type response input stage as a higher overall bandwidth and more accurate measurement can be achieved. As a general rule, the bandwidth of the scope should also be at least 5× that of the signal to be measured [149].

SiC-MOSFET	t_r	Min. Bandwidth
C3M0032120K - 63 A, 1.2 kV *Cree, TO-247-3*	18 ns	∼ 100 MHz
C2M0025120D - 90 A, 1.2 kV *Cree, TO-247-3*	32 ns	∼ 50 MHz
CAS120M12BM2 - 120 A, 1.2 kV *Cree, 62 mm*	34 ns	∼ 50 MHz
CAS300M17BM2 - 300 A, 1.7 kV *Cree, 62 mm*	72 ns	∼ 25 MHz

Table 3.6: Required oscilloscope bandwidth for SiC-MOSFETs (C3M0032120K [150], C2M0025120D [151], CAS120M12BM2 [152], & CAS300M17BM2 [139]).

Using these guides, the minimum required scope bandwidth for three different capacity SiC-MOSFETs are shown in Table 3.6. It can be seen that the smaller single-die discrete devices necessitate significantly more bandwidth than the higher capacity multi-die power modules.

3.6.1.1 Oscilloscope used in DPTR

The two four-channel scopes used in conjunction with the DPTR are listed in Table 3.7. Both scopes were used in "single-shot" mode and triggered externally with a custom optical receiver PCB. To reduce vertical noise and increase resolution the chosen scopes also have a high Analogue-to-Digital Converter (ADC) bit-depth.

Oscilloscope	Bandwidth	Sample Rate	ADC Resolution	t_r
MSO64 *Tektronix*	1 GHz	25 GS/s	12 bits	400 ps
WaveRunner 604Zi *LeCroy*	400 MHz	20 GS/s	11 bits	875 ps

Table 3.7: Oscilloscopes used in experimental work.

3.6.1.2 Oscilloscopes Probes

An oscilloscope is a sensitive voltage input device which requires a probe to physically interface to the circuit or DUT. A variety of different probe types are used — such as voltage, current, and antennas — and they either convert and/or attenuate their measured signal to a representative voltage signal which the scope's front-end can manage and process. The probes themselves have a particular characteristic bandwidth which impacts the overall system bandwidth. For a Gaussian response scope (which is the case for both scopes in Table 3.7), the resultant system bandwidth is the sum of squares of the individual components, as expressed in (3.33)

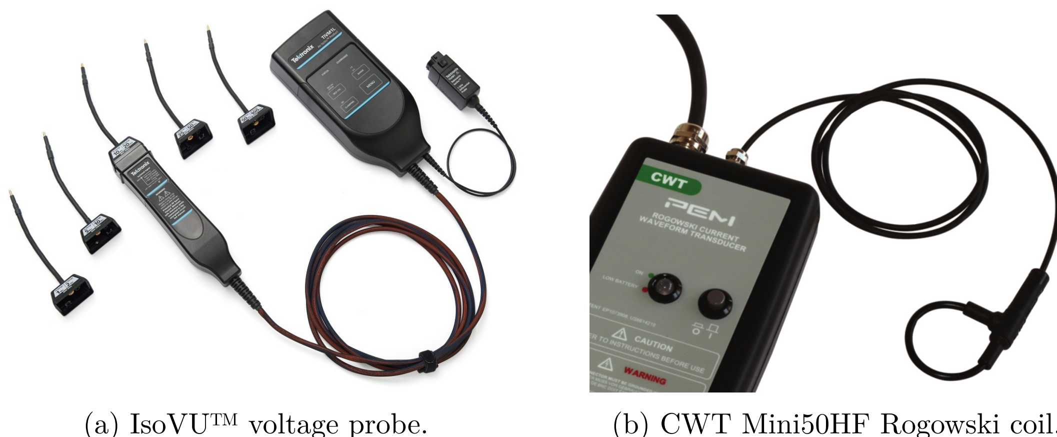
$$BW_{system} = \frac{1}{\sqrt{\left(\frac{1}{{BW_{scope}}^2} + \frac{1}{{BW_{probe}}^2}\right)}} \quad \text{[Hz]} \tag{3.33}$$

This is the why the stated bandwidth for the scopes in Table 3.7 is significantly higher than the minimum required bandwidth values for the SiC-MOSFETs (Table 3.6) — i.e. the effect of Equation (3.33) does not impact the measurement capabilities.

One consideration that must be taken when measuring the DUT is the “Observer Effect” — that is that the act of observing will have an impact on the phenomenon. For the case of the DPTR and characterising power transistors this can be summarised by:

- **Loading** – loading the circuit/DUT with additional resistance, capacitance, and/or inductance (self and mutual).

- **Common-mode** – creating additional unwanted coupling paths for I_{CM}, also possibly introducing noise into the measurement.



(a) IsoVU™ voltage probe. (b) CWT Mini50HF Rogowski coil.

Figure 3.28: Measurement probes used in this study - copyright: Tektronix (a) and Power Electronic Measurements (PEM) Ltd. (b).

3.6.2 Voltage Measurement

3.6.2.1 Voltage Probes

Voltage probes generally attenuate the measured signal by 10×, 100×, or more for higher voltages. They are classed as either: single-ended, where the ground reference point is shared by the probe end and oscilloscope; and differential, where the measurement can be made at high CM voltages (V_{CM}) with high impedance or isolation between the probe end ground and the oscilloscope ground. Due to the nature of voltage measurements in PE, in terms of high V_{CM} and required safety, differential probes are most often used. The differential probes used in this work are listed in Table 3.8. As of 2020, the IsoVu probes from Tektronix are the highest performance differential probes available, however, they cost approximately £22,000 each. The HVD3605A differential probe from LeCroy is the next best available and costs approximately £7,000.

Probe	Bandwidth	$V_{Diff.}$	V_{CM}	CMRR	t_r
TIVM IsoVu™ *Tektronix*	1 GHz	±1 V→ ±50 V [a]	60 kV	120 dB (DC) 90 dB (1 GHz)	≤ 350 ps
TIVH IsoVu™ *Tektronix*	800 MHz	±25 V→ ±2.5 kV [b]	60 kV	160 dB (DC) 90 dB (1 GHz)	435–700 ps
HVD3605A *LeCroy*	100 MHz	±700 V, ±7 kV	±7.6 kV	85 dB (DC) 30 dB (0.1 GHz)	4.3 ns
P5210 *Tektronix*	50 MHz	±2.2 kV	4.4 kV	80 dB (DC) 50 dB (1 MHz)	—

[a] Realised with 5 different probe tips, [b] realised with 7 different probe tips.

Table 3.8: Differential voltage probes used in experimental work.

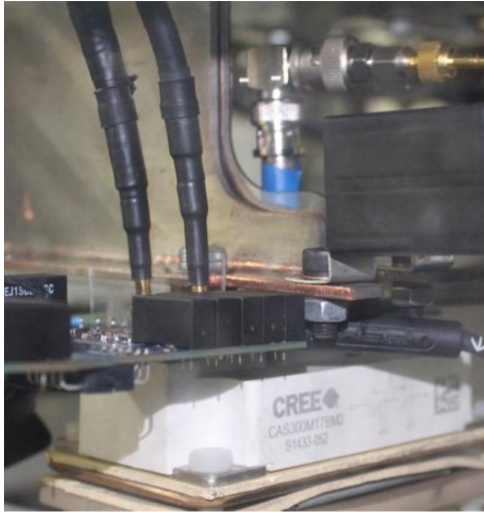
The HVD3605A probe uses a RC based attenuation network (resistive DC divider with parallel capacitive AC divider) to step the differential voltage down and then passes that to a differential amplifier. Due to the requirement for a high Common-Mode Rejection Ratio (CMRR), the bandwidth is only 100 MHz. Standard single-ended (passive or active) probes which are based on simple RC

divider and compensator networks are able to achieve a much higher bandwidth because they do not have a high CMRR or V_{CM} requirement.

The IsoVu™ probes (Figure 3.28a), which come in a high-voltage (TIVH) and low-voltage (TIVM) configuration, are vastly more expensive but have far superior capabilities. They achieve such high V_{CM} and CMRR by completely galvanically isolating the probe head from the oscilloscope. This is realised by five fiber-optical cables between the measurement head and the base unit — three that transmit the measured signal digitally and two that power the measurement head via Power-over-Fiber (PoF). A high-speed ADC is used in the measurement head to convert the signal to be transferred and a high-speed Digital-to-Analogue Converter (DAC) is used in the base unit to decode and convert the signal back to an electrical signal. As is standard for any sensitive electrical signal path in a measurement system, coaxial cable is used as a transmission line to connect the base unit to the scope. A variety of probe tips, which use inline RF-class coaxial attenuators of different values, can be interchanged on the measurement head to achieve different differential voltage scales as shown in Table 3.8 (five increments between these values). This allows for a low-voltage measurement to be made upon a high V_{CM} with the full resolution of the probe and scope — for example, HS V_{gs} measurement. Other high-voltage probes (HVD3605A included) are poor at measuring these low differential voltages.

3.6.2.2 Interfacing Voltage Measurements

Connecting the measurement probe to a circuit or DUT requires careful connection if the parasitic elements are to be kept to a minimum and the maximum bandwidth is to be achieved. For the low-voltage IsoVu™ probe tips, the connection is made via a MMCX plug connector at the end of a coaxial cable. A MMCX



(a) IsoVu™ probes, CVR and Rogowski coil.

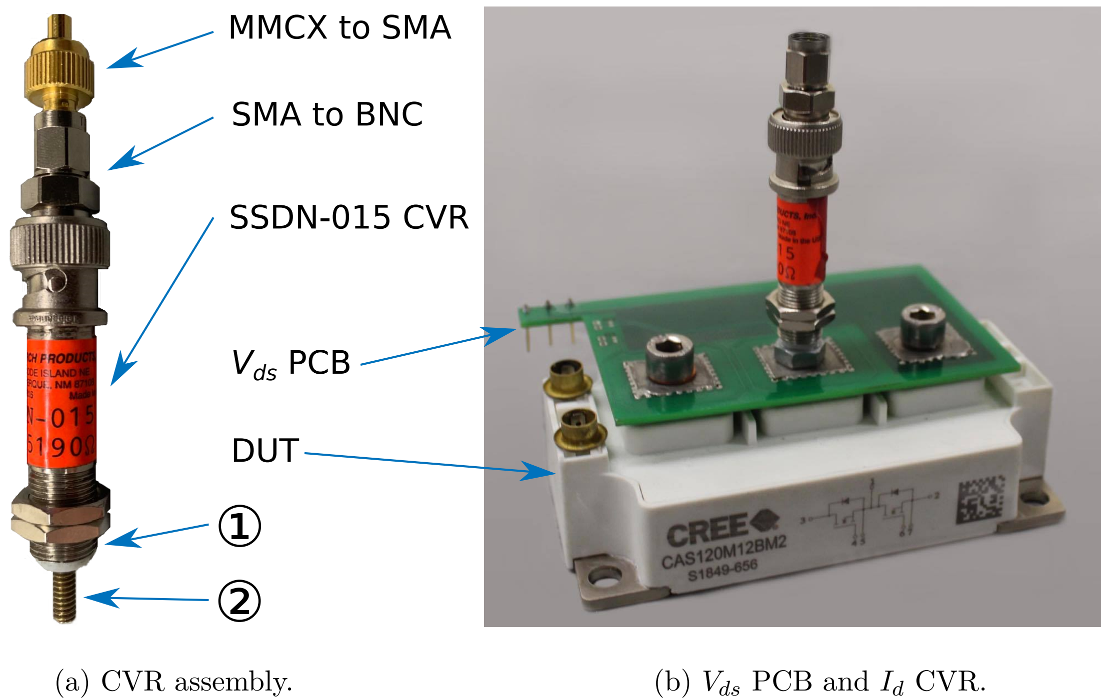
(b) V_{gs} MMCX test point.

Figure 3.29: Power module measurements.

socket connector for measuring V_{gs} was directly soldered between the gate-drive terminals — this can be seen in Figure 3.29b. The photograph in Figure 3.29a shows the coaxial cable of the IsoVu™ measurement tip coming down to the DUT.

A custom PCB was designed for making low-insertion V_{ds} measurements. This was designed to be connected in-between the metal tabs of the power module and the busbar with 3 mm thick copper square inserts acting as the conduction path. These were soldered into a square cut-out in the PCB which was done in an effort to reduce additional inductance to the power circuit CCL. An 8 mm bolt hole was then drilled through it for the fastening bolt. The thickness of the copper spacers was intentionally larger than the thickness of the PCB to ensure that it protrudes on either side, thus no force was exerted on the PCB when torquing the assembly. The square cut-outs in the PCB have plated half-holes — called castellated holes — along their perimeter which allow for the solder connection to be made. For high-voltages that pose a clearance issue for the MMCX (> 500 V), the IsoVu™ probe tips use a standard 0.2” (5.08 mm)

receptacle. A corresponding header, which connects to the copper spacers via traces, is positioned at the front of the PCB. A photograph of this PCB is shown in Figure 3.30b. These headers also allow for connecting the hook clips at the end of the probe leads of the HVD3605A. When connecting the HVD3605A, the probe leads were twisted to reduce the inductance of that loop. This inductance is well known to be a weak-point in voltage probes, particularly in the ground leads of traditional single-ended probes. The effect of this inductance in voltage probe leads is shown in Figure 6 of [153]. Power modules exist which provide dedicated Kelvin-Drain (KD)/Kelvin-Collector (KC) and Kelvin-Source (KS)/Kelvin-Emitter (KE) connections. These make interfacing to the measurement device easier and also provide a better measurement point to the semiconductor die which is not impacted by $L\frac{di}{dt}$ effect on internal stray inductance.



(a) CVR assembly.

(b) V_{ds} PCB and I_d CVR.

Figure 3.30: Power module measurements.

3.6.3 Current Measurement

Two current sensing techniques are used in this study, and can be classified as: "Ohm's Law of Resistance" where the current is inferred from the voltage drop across a known resistance; and "Faraday's Law of Induction" where the current carrying conductors flux induces a voltage on a secondary winding.

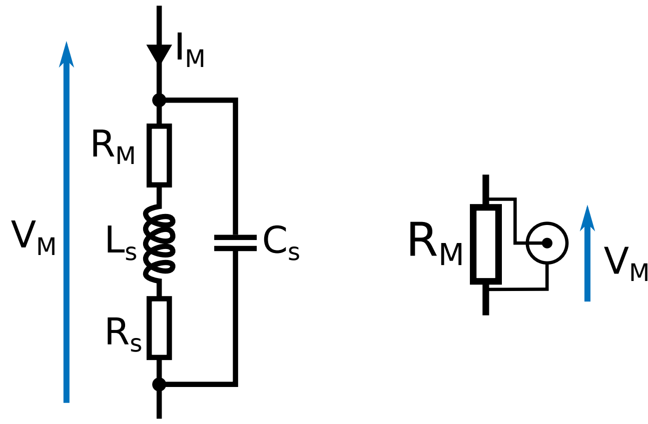
3.6.3.1 Coaxial Current Viewing Resistor (CVR) — *Ohm's Law*

For measuring device current resistively, the resistor component is placed directly into the current path (i.e. in series) and requires to be low in value so that it does not limit the current and dissipate excessive levels of power. Due to their physical construction, resistors are not purely resistive. They also include parasitic series inductance (L_s), parallel capacitance (C_s) and additional resistance (R_s) — as shown in Figure 3.31a — which, as previously discussed, are detrimental to device switching behaviour. As the frequency of the current increases the resistance of a current sensing component also increases due to the skin effect and proximity effect. Whilst SMT sense resistors can have low levels of parasites, they are still not low enough.

A CVR — sometime called a coaxial shunt — is a high-performance sense resistor that can overcome these issues [154]. The circuit symbol for the CVR is shown in Figure 3.31b. The measured voltage (V_m) can be expressed as (3.34)

$$V_M(t) = I_M(t)R_M + I_M(t)R_s + L_s\frac{dI_M(t)}{dt} \qquad \text{[V]} \tag{3.34}$$

The CVR is constructed in a shielded coaxial manner which is cylindrically



(a) Equivalent circuit. (b) Schematic symbol.

Figure 3.31: Coaxial Current Viewing Resistor (CVR).

symmetrical in shape. The magnetic flux generated by the internal conductor (on which the small resistive element is situated) is cancelled out by the return path of the outer conductor. This flux cancellation results in a L_s in the low pH range [155]. The -3dB cutoff frequency (f_{3dB}) is defined as when the resistance is equal to the inductor reactance ($X_L = 2\pi f L$) [156], and is given by (3.35)

$$f_{3dB} = \frac{R_M}{2\pi L_s} \quad [\text{Hz}] \tag{3.35}$$

A L_s in the low pH range and a total resistance in the mΩ range results in an effective bandwidth in the GHz range. The resistive element of the device R_M is high in resistivity yet small in length, thus low in overall resistance. This design alleviates the skin effect and proximity effect [157]. Kelvin connections are made across the resistive element and lead to a RF-connector, usually a BNC type.

Probe	Type	Bandwidth	R	E_{max}	t_r
SSDN-015 *T&M Research Products*	CVR	1.2 GHz	15.335 mΩ	1.5 J	300 ps

Table 3.9: CVR used in experimental work.

The CVR used in this study is the SSDN-015 from T&M Research Product (Table 3.9) which has a flat frequency response from DC–1.2 GHz. Photographs of this can be seen in Figure 3.30. This particular model uses screw terminals and is bolted to the busbar at ① and to the power module terminal at ②, as illustrated in Figure 3.30a. However, models are available which connect via through-hole or metal strip connections intended for use on a PCB. There are, however, two main issues when it comes to using CVRs. Namely: that they have a maximum energy (E_{max}) rating for the device; and that interfacing them to the power circuit and also the subsequent measurement equipment is not easy.

Due to the intricate high-frequency design of the CVR, the heat that is generated from the power dissipation cannot readily be removed from the element. Therefore, there is an E_{max}, as expressed in (3.36)

$$E_{max} = R_M \int_0^{T_p} {I_M}^2 dt \qquad [\mathrm{J}] \tag{3.36}$$

This limits the CVR to use cases like the double-pulse test and does not allow for continuous operation.

Traditionally, the CVR has not always been considered as a viable option for testing power semiconductor devices, even with their excellent frequency characteristics. This is because connecting them to a scope has to be done using a simple coaxial cable, thus negating any floating measurements at high V_{CM} points in the circuit and introducing I_{CM} paths and ground loops. Utilising the low-voltage IsoVu probes to make this voltage measurement overcomes these issues. In order to connect the IsoVu probe to the CVR, the assembly shown in Figure 3.30a was used. This included a BNC → SMA adapter and then a SMA → MMCX adapter that the IsoVu could connect to. A right-angle BNC adapter was also used at the

end of the CVR when required.

The CVR provides excellent high-frequency current measurements but, due to its E_{max} limitations and required measurement probes, it is impractical for online converter measurements.

Whilst it has not been used in this study, the low-voltage IsoVu probe allows for gate-current measurements to be made by observing the voltage drop across the external gate-resistor.

3.6.3.2 Rogowski Coil — *Faraday's Law*

A Rogowski coil was the non-contact current sensing device used in this work. A diagram showing the basic working principle of the Rogowski coil method is shown in Figure 3.32. The current (I_M) being measured is illustrated by the orange arrow in the centre of the measurement coil.

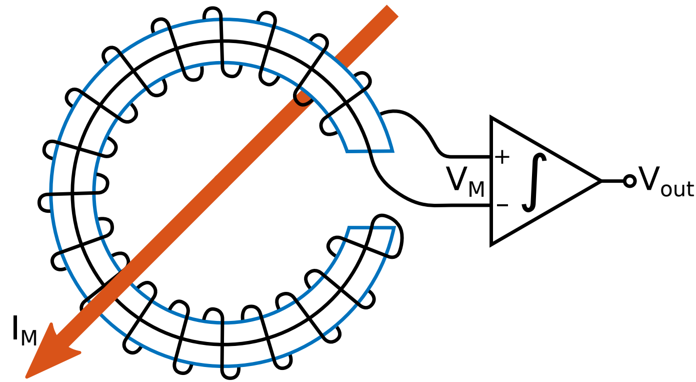


Figure 3.32: Diagram of Rogowski coil principle.

Amperes law is first used to define the magnetic flux density (B) resulting from I_M, as shown in (3.37)

$$\oint \overrightarrow{B} \cdot \overrightarrow{dl} = \mu_o I_M \qquad [\mathrm{T}] \tag{3.37}$$

where: μ_o is the permeability of free space. This can be simplified to show B at the measurement coil (3.38)

$$B = \frac{\mu_o I_M}{2\pi r} \qquad [\mathrm{T}] \tag{3.38}$$

where: r is the radius of the coil (from the centre of the current conductor). The measurement coil — which is the secondary winding of this mutual inductance — is shown to be wound round a toroidal former, with the return path coming back through the centre of this winding (Figure 3.32). Faraday's law of induction is used to determine the induced voltage (V_M) on the measurement winding [158]. This is expressed as (3.39)

$$V_M = -N\frac{d\phi}{dt} = -NA\frac{dB}{dt} = -\frac{NA\mu_o}{2\pi r}\frac{dI_M}{dt} \qquad [\mathrm{V}] \tag{3.39}$$

where: N is the number of turns of the measurement winding; ϕ is the magnetic flux; and A is the cross-sectional area of the toroid. V_M is proportional to the derivative of I_M, therefore an integration stage is then required. This can be expressed as (3.40)

$$V_{out} = -\frac{NA\mu_o}{2\pi r}\int_t \frac{dI_M}{dt} \cdot dt + V_{out}(0) \qquad [\mathrm{V}] \tag{3.40}$$

As V_M only provides the rate of change of I_M (i.e. it's AC component), the DC component is unknown. This is denoted by $V_{out}(0)$, the voltage at $t = 0$. For use in testing power semiconductor device switching, this is not a major issue as the starting point is most often zero. One major benefit of using inductive based measurements is the inherent galvanic isolation. This make measuring current

in areas of high potential significantly easier. Another benefit is that because there is no core in the toroid, the device does not saturate. It should be noted, however, that due to the inductive coupling, this does result in a small amount of losses for the system under test.

The Rogowski coils used in this study are listed in Table 3.10 — a photograph of the CWT Mini50HF is shown in Figure 3.28b. These are the highest bandwidth commercially available Rogowski coils. These come in a variety of current ranges, however the models used in this study were one 600 A CWT MiniHf, one 1200 A CWT MiniHf, and one 1200 A CWT Mini50Hf.

Probe	Type	Bandwidth	t_r
CWT MiniHF *PEM*	Rogowski coil	30 MHz	>12 ns
CWT Mini50HF *PEM*	Rogowski coil	50 MHz	12 ns

Table 3.10: Current probes used in experimental work.

The Rogowski coil concept has seen some attention in the literature. A hand-wound coil was built in [159] which has a bandwidth of 100 MHz. Devices which are designed to be used with Gallium Nitride (GaN) transistors have been shown to achieve much higher bandwidths. An inline Rogowski was proposed in [112] and realised a bandwidth of 500 MHz, with a low insertion inductance of 350 pH. This was realised by a half-brass tube in series with the DUT and a pick-up wire which runs through its centre. In [160] a planar version of the Rogowski coil — named the “Infinity Sensor” — sits directly above the PCB trace and achieves 225 MHz with a 200 pH insertion inductance.

Figure 3.33: BicoLOG 20100 X from Aaronia. Positioned to detect radiated emissions from DPTR.

Probe	Type	Bandwidth	Z
BicoLOG 20100 X *Aaronia*	Biconical antenna	20 MHz–1 GHz	50 Ω

Table 3.11: EMI antenna used in experimental work.

3.6.4 Radiated EMI Probes

The radiated EMI was measured using far-field antenna from Aaronia. A photograph of this is shown in Figure 3.33 and its properties are listed in Table 3.11. A biconical antenna is a broadband dipole antenna which comprises two cone-shaped conductive bodies. This model has an integrated RF amplifier which outputs a voltage proportional to the electric component of the incident EM wave. This voltage is then measured using an oscilloscope with a Fast Fourier Transform (FFT) being applied to show the frequency components and their power.

The RE which was measured cannot be classed as a proper EMC measurement. EMC measurements take place in very controlled environments, such as in an anechoic chamber where there are no reflections and extremely low levels of background EM noise, and under strict guidance from IEC or FCC standards. However, as a purely comparative based measurement, the measured EM wave can be considered. The FFT plot in Figure 3.34 shows the background RF noise which was measured by the EMC antenna. As expected, a considerable amount of RF content can be seen in this spectrum. This includes various communication and broadcasting frequencies, as detailed in the Ofcom United Kingdom Frequency Allocation Table [161].

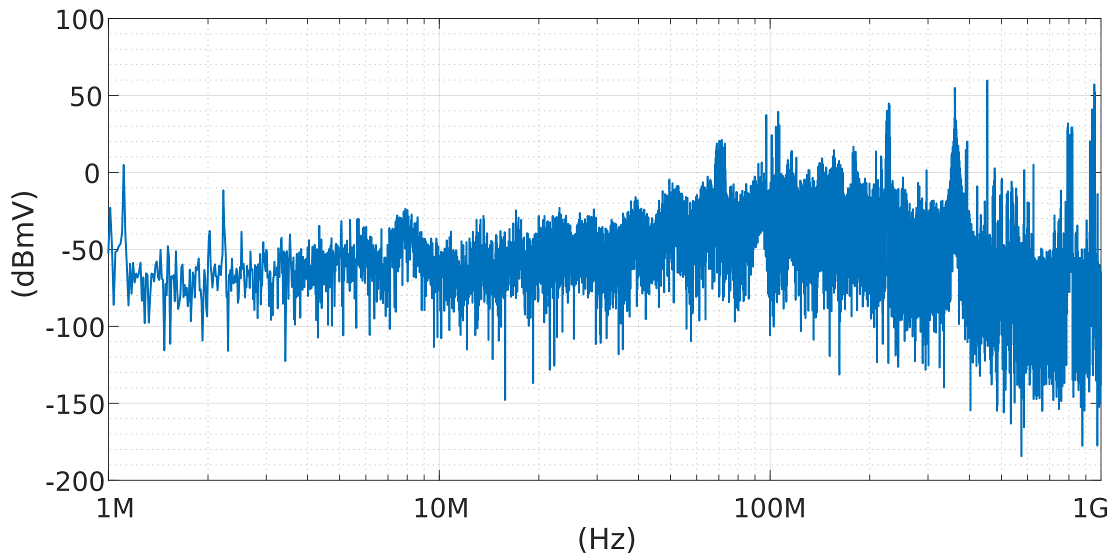


Figure 3.34: FFT plot of background EMI measured using the BicoLOG 20100 X antenna.

3.7 Switching Loss Calculations

3.7.1 Data Processing

As part of the automated testing procedure, once a test was performed MATLAB pulled the measurement data from both scopes. The data then went through a

processing stage. This included:

Scaling Factors — Applying scaling factor for Rogowski coil ($\times$100 for 1 mV/A) and inferring current from voltage on CVR ($\times$1/0.015335).

Time Deskew — Aligning data in time using known and calculated time delays.

Correcting Offsets — A function was created to add vertical offsets to align zero points in the data to a true zero value. This was particularly necessary with Rogowski coil data.

Filtering — In order to remove noise on the signal a basic filter was used. The majority of this noise is due to the oscilloscopes own noise floor. The built-in MATLAB function *movmean* [162], with a window size of 11, was used — this equates to an averaging window of 440 ps for the MSO64 data. Only the noise component is removed with accurate amplitude and phase of the waveforms being maintained.

Resampling — The data from the two scopes was at different sample rates (as noted in Table 3.7). If a calculation was to be made using data from each scope, the data needs to be of the same sample rate/time step. If this was required, the built-in MATLAB function *resample* [163] was used.

3.7.2 Switching Loss Estimations

The switching loss calculations were done by integrating the instantaneous power ($V_{ds} \times I_d$) during the transition period. This is shown in (3.41)

$$E_{sw} = \int_{t_0}^{t_1} V_{ds} I_d \, dt \qquad [\mathrm{J}] \tag{3.41}$$

The standards which specify how semiconductor devices are characterised

differ for a MOSFET [164] and an IGBT [165]. The integration limits (t_0 & t_1) are defined at slightly different points in the transition for both turn-on and turn-off. The MOSFET standards can also negate some of the oscillatory behaviour. This makes comparing the Si-IGBT, the SiC-MOSFET and the Si-SiC hybrid switch inequitable using these integration limits. Therefore, for fair comparisons the integration limits used in this study are as follows:

Turn-On, t_0 — V_{gs} or V_{ge} rise above 10 %.

Turn-On, t_1 — V_{ds} or V_{ce} fall below 2 % and, if present, I_d or I_c oscillations are damped to 2 % of peak oscillation magnitude.

Turn-Off, t_0 — V_{gs} or V_{ge} fall below 90 %.

Turn-Off, t_1 — I_d or I_c fall below 2 %, without rising again.

As accurate as they are, the resultant switching energy measurements can only ever be viewed as estimates. In order to determine true switching losses, a calorimeter is required [66, 166, 167]. However, for the purpose of comparing devices in the DPTR, the calculations are more than sufficient.

Experimental results of Si-IGBT and SiC-MOSFET switching will be shown in Chapter 4. This will show the performance of the high-bandwidth measurement equipment that has been discussed in the preceding sections.

* * *

4 | SiC-MOSFETs & Si-IGBTs: Characterising High-Capacity Devices & Considerations for full Exploitation

4.1 Chapter Introduction

This chapter will identify some of the key practical features of high-capacity power semiconductor devices for use in high-power applications. A comparison of the Silicon-Carbide (SiC)-Metal–Oxide–Semiconductor Field-Effect Transistor (MOSFET) and the Silicon (Si)-Insulated-Gate Bipolar Transistor (IGBT) is presented, including experimental testing and considerations for their use.

The chapter is structured as follows: Section 4.2 provides a head-to-head comparison of Si-IGBTs and SiC-MOSFETs; Section 4.3 experimentally shows the required bandwidth of measurement equipment for SiC devices; Section 4.4 investigates the performance of a hybrid Si-IGBT which employs a SiC-Freewheeling Diode (FWD); Section 4.5 investigates how much the switching transients of SiC-

MOSFETs need to be “slowed down” in order to make the radiated Electromagnetic Interference (EMI) comparable to a Si-IGBT; and Section 4.6 discusses further techniques which can be used to passively and actively manage these switching transients.

4.2 Head-to-Head: Si-IGBT & SiC-MOSFET

As previously mentioned, the Si-IGBT has been the de facto option for high-power semiconductor based switches in the Voltage-Source Converter (VSC) applications for several years. However, due to their poor transient performance, particularly at turn-off, the switching frequency of converters which use them are limited to a maximum of 2–4 kHz (20 kHz for low-power applications) [2]. The reason for this being the bipolar conduction mechanism, which allows for an excellent on-state performance relative to the blocking voltage capability, as detailed in Chapter 2. The SiC-MOSFET — which is a unipolar conduction device — is widely forecasted to unseat the Si-IGBT due to its superior dynamic and static characteristics. This will lead to the MOSFET outperforming the IGBT in terms of switching loss and part-load conduction loss.

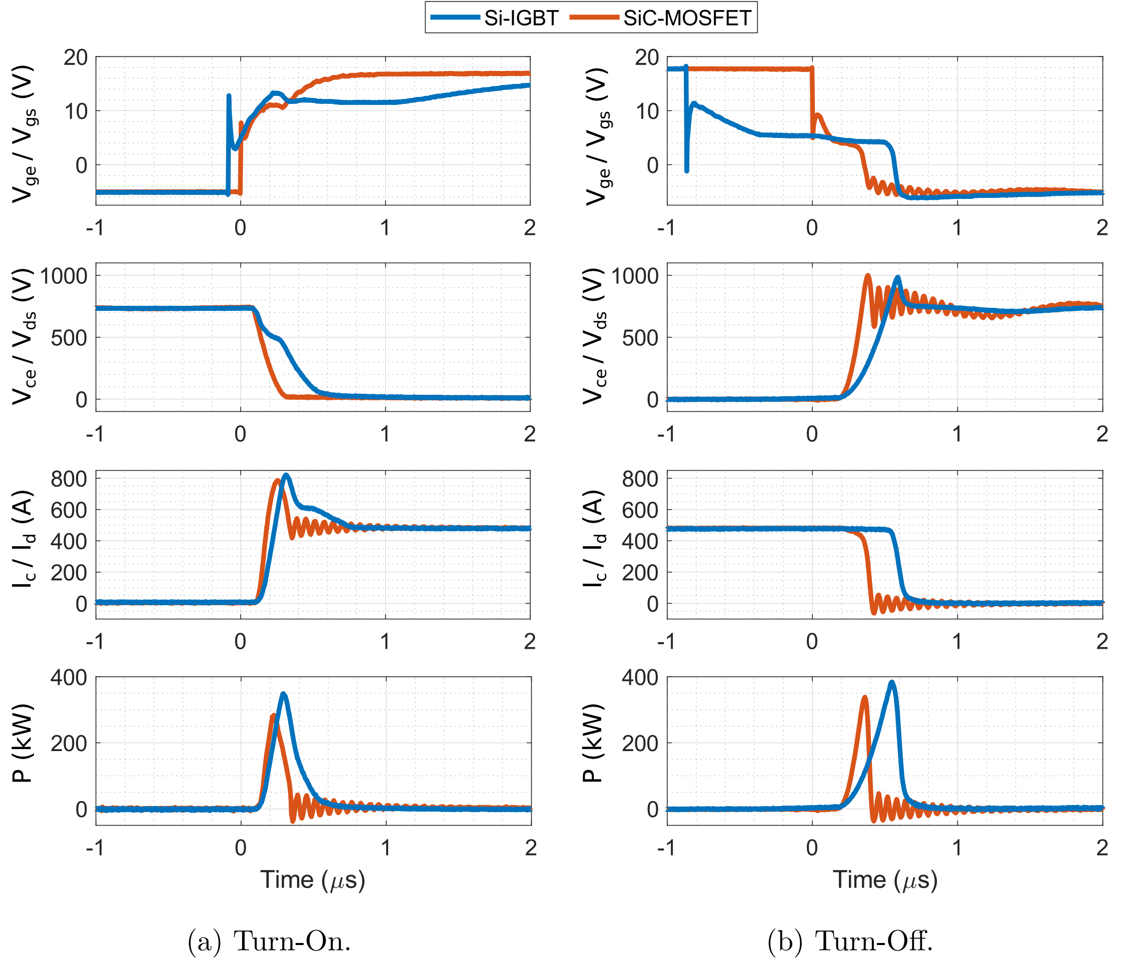
This section will experimentally characterise the switching performance of the differing technologies and discuss other considerations for high-capacity devices. The experimental results in this section also provide the benchmark results for Chapter 5 and 6 and show the performance of the Double-Pulse Test Rig (DPTR).

4.2.1 Experimental Comparison of Switching Transients

To assess the difference in switching characteristics of these two technologies, a Si-IGBT (FF450R12KT4 [168]) and a SiC-MOSFET (BSM600D12P3G001 [144]) were tested in the DPTR. This does not provide a full comparison as many more models of devices from different manufacturers would need to be tested. However, the devices chosen are representative of typical Si-IGBTs and SiC-MOSFETs used in high-power applications. Specifically, the IGBT is a Trench/Fieldstop Punch Through (PT) device which is the optimisation/tuning which is used for high-power devices. This is because PT-IGBTs have a Positive Temperature Coefficient (PTC) at high-current densities, therefore allowing for safe parallel connection of multiple dies to produce high-current modules.

Switching waveforms at 480 A, 700 V, and 100 °C are shown in Figure 4.1. The devices were driven with their datasheet recommended gate resistance values. The plots have been zeroed to the V_{gs} of the SiC-MOSFET — for the turn-on plots (Figure 4.1a), the MOSFET and IGBT have been aligned using the device current and for the turn-off (Figure 4.1b), the device voltage was used for alignment. This was done to show the additional turn-on and turn-off delay that the IGBT exhibits.

It can be seen in the device voltage plots (V_{ce} & V_{ds}, second plot from the top) that the SiC-MOSFET has a significantly faster dV/dt than the Si-IGBT. This is a consequence of the larger die area (hence greater output capacitance and larger gate-charge requirement that the Si-IGBT has) as well as the rate of recombination of minority carriers. The device current plots (I_c & I_d, third plot from the top) show that whilst there is a difference in dI/dt (MOSFET faster than IGBT), the improvement in the current rise time is not to the same degree as the dV/dt. However, the tail-current behaviour in the Si-IGBT turn-off exists.



(a) Turn-On.

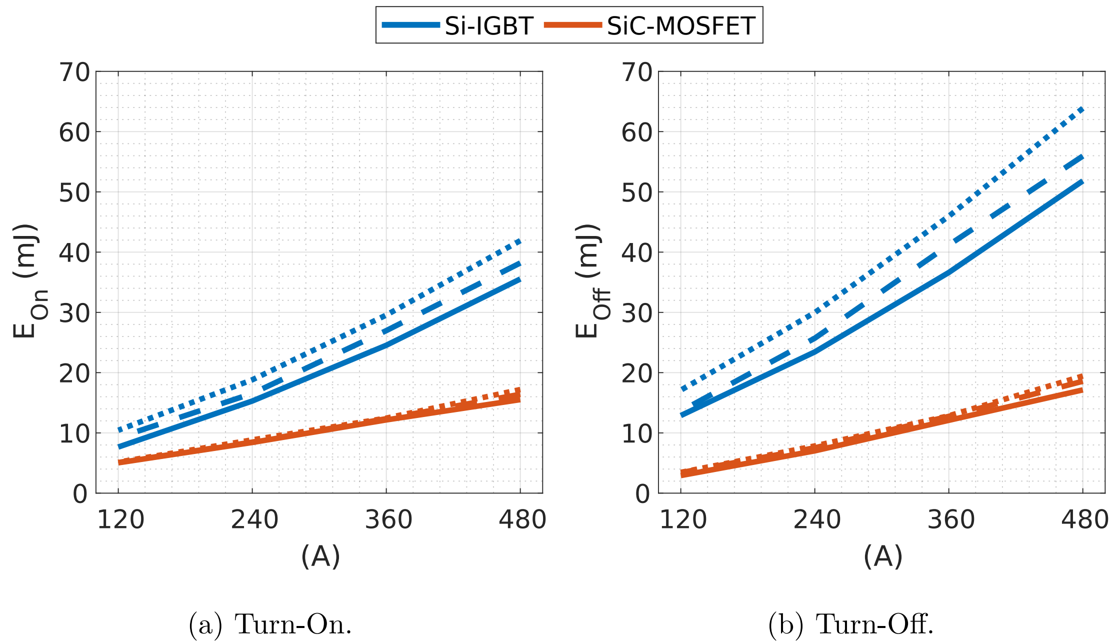
(b) Turn-Off.

Corresponding FFT of antenna measurement shown in Fig. 4.3.

Figure 4.1: Experimental waveforms of switching transitions, Si-IGBT (FF450R12KT4 [168]) compared to SiC-MOSFET (BSM600D12P3G001 [144]). Tested at 480 A, 700 V with device baseplate set to 100 °C.

As previously mentioned, this is due to excess minority carriers within the IGBT and contributes considerably to E_{Off}. The resultant instantaneous power which is dissipated within each device is shown in the bottom plot of Figure 4.1. It can be seen empirically that there is less power loss in the SiC-MOSFET for each switching event. These instantaneous power traces are then used to determine the switching energy using the method outlined in Section 3.7.2.

A comparison of the turn-on and turn-off switching losses for both the Si-IGBT and SiC-MOSFET are shown in Figure 4.2. These comparison plots show the performance across various current set points and at three different temper-



(a) Turn-On.

(b) Turn-Off.

Figure 4.2: Switching energy of Si-IGBT and SiC-MOSFET. Solid line = 75 °C, dashed line = 100 °C, & dotted line = 125 °C. Tested at 700 V.

atures. It can be seen that, for both turn-on (Figure 4.2a) and turn-off (Figure 4.2b), the SiC-MOSFET considerably outperforms the Si-IGBT. The IGBT also exhibits a substantial increase in loss with an increase in temperature due the temperature dependence on dI_c/dt. A more substantial increase is evident with E_{Off} due to the effect of temperature on the recombination process of the excess minority carriers (this mechanism is further detailed in Section 5.3.3.2). The SiC-MOSFET shows very little sensitivity to temperature. However, a small increase can be observed which is due to the temperature effect on dI_d/dt [169].

Whilst a lower level of switching loss is achieved with a SiC-MOSFET, a substantial amount of oscillatory behaviour can be seen in the voltage and current waveform in Figure 4.1. A resonance of ∼16 MHz, which is large in magnitude, can be seen. FFTs of the radiated emissions (measured using the active EMC antenna detailed in Section 3.6.4) are shown in Figure 4.3. As shown in these spectral content plots, the ∼16 MHz oscillations result in a large amount of

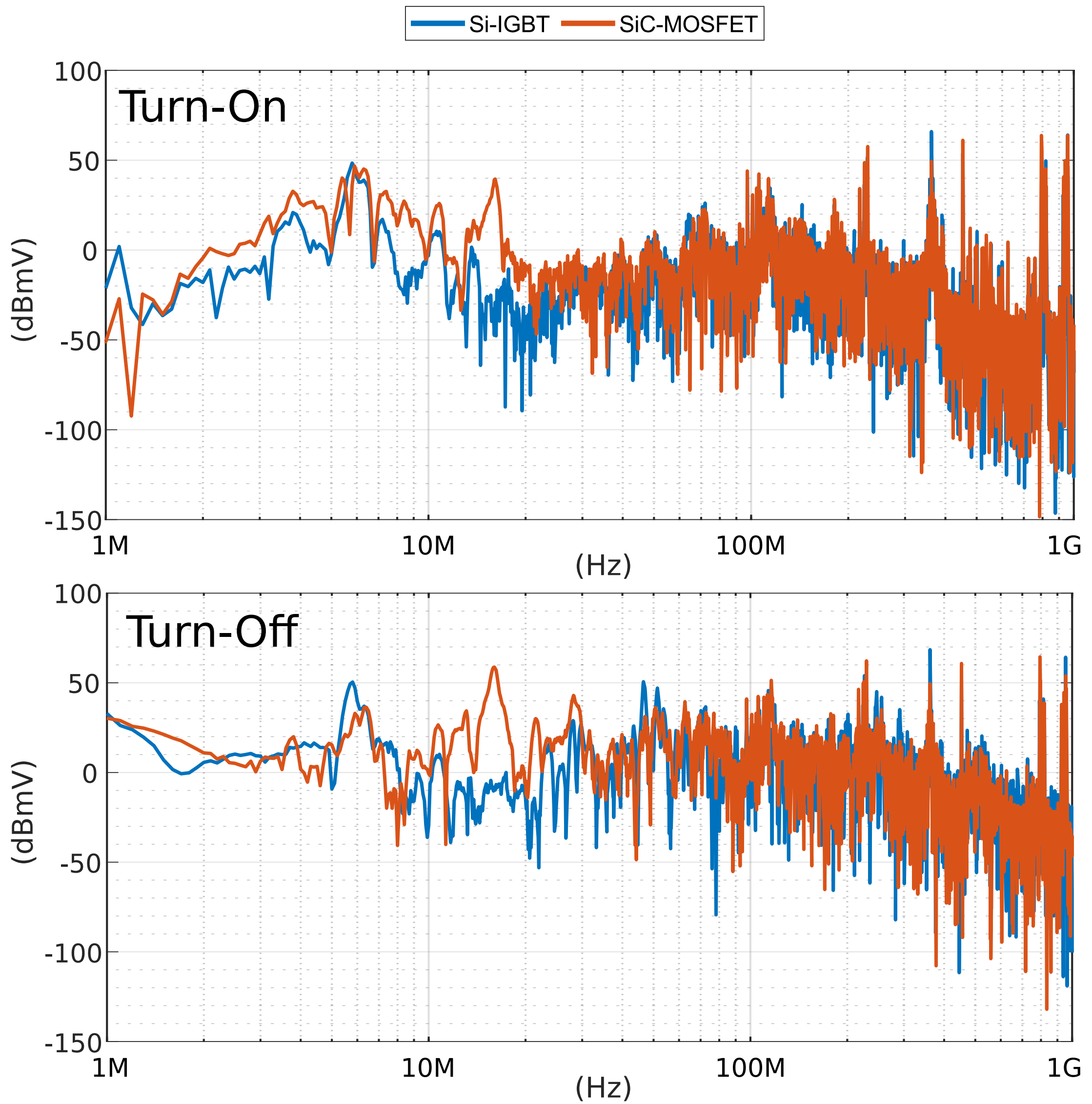


Figure 4.3: FFT of antenna measurements.

energy radiated at this frequency — 40 dB at turn-on and 59 dB at turn-off. This confirms that moving to a SiC solution results in a heightened chance of radiated EMI related issues. It should be noted that it is difficult to make any clear comparison on relative spectrum above around 30 MHz. The higher dV/dt values also come with the likelihood of an increase in conducted EMI relative to a traditional Si-IGBT solution.

4.2.2 Further Comparison

The benefits of fabricating devices out of Wide-Bandgap (WBG) materials and also moving from an IGBT device to MOSFET device are not just limited to switching performance, as discussed in Chapter 2. The following sections will continue the head-to-head comparison of the Si-IGBT and SiC-MOSFET.

4.2.2.1 Conduction Characteristics

The on-state I–V characteristics for a MOSFET device and IGBT device differ. The MOSFET has a purely resistive equivalent circuit, whereas the IGBT has a resistive element with an additional series diode. This results in an inherent diode voltage drop in addition to the ohmic losses for the IGBT. This will be further explained and used in a hybrid switching concept in Chapter 6.

4.2.2.2 Parallel Connecting Die

It was discussed in Section 2.7.2 that high-capacity switches are realised by the parallel configuration of multiple dies within a package. This is due to the die size, and hence the associated current ratings of available Si and SiC transistors which are not sufficient in many applications.

Whilst paralleling transistors for multi-die devices (or the paralleling of multiple discrete devices or modules) is ostensibly easy, the steady-state and transient current sharing of the paralleled dies needs to be considered. If three or more dies/devices are used, the layout of the conductors cannot be symmetrical and hence will have an imbalance of stray inductance (L_s) [159]. If L_s is not balanced — i.e. the inductances of the conductors used to connect the multiple dies are

not of exactly the same value — the switching transient is affected for each die. This can cause a difference in the voltage transient (overshoot and oscillations) and also result in a transient current which is not uniformly distributed. This could result in a larger amount of switching losses in one of the dies, thus leading to an increased junction temperature of that specific die. Once there is an unequal temperature distribution, the on-state resistance also becomes unequally distributed which results in a non-uniform sharing of the steady-state current. Current imbalances adversely affect the reliability and lifetime of SiC-MOSFET power modules [170], due to their parallel die configuration.

A SiC-MOSFET exhibits a PTC for its $R_{ds(on)}$ [171], creating a natural feedback loop for equal current distribution. This means that the die with the lowest $R_{ds(on)}$ conducts the most current, subsequently increases its junction temperature (hence an increase in its $R_{ds(on)}$) and allows paralleled dies to return to uniform current distribution. The PTC characteristic means that the device will not be susceptible to thermal runaway. The Si-IGBT has a similar PTC behaviour for the on-state voltage at rated current. However, at low-current levels, when there is a lower level of minority carrier injection into the device drift region, the on-state voltage exhibits a Negative Temperature Coefficient (NTC) [171]. In an on-state NTC situation a device can suffer from thermal runaway. The point at which a device (MOSFET, IGBT or Diode) moves from PTC to NTC is defined as the Zero Temperature Coefficient (ZTC), usually at the lower end of the current rating. Operating in this region should be avoided as it could easily transition into the NTC range and lead to a thermal runaway situation.

On the other hand, the threshold voltage for a SiC-MOSFET and a Si-IGBT has a NTC, which can adversely effect the switching transient due to the threshold voltage shift.

To aid with simultaneous switching of parallel die modules, many commercially available high-capacity devices are often purposely slowed down by means of a large gate resistance (relative to a single die solution). Active Gate-Drivers (AGD) techniques are currently an area of interest for parallel connected SiC-MOSFET [172] and Si-IGBT [159]. The use of gate resistors and advanced gate-drive architectures will be discussed further in Sections 4.5 and 4.6.

Due to the differing on-state equivalent circuit — as mentioned in Section 4.2.2.1 — the MOSFET device can be viewed as an inherently better device in terms of its conduction properties across the full rating of the device. This is because the MOSFET can achieve a lower voltage drop at low currents compared to the IGBT which displays the classic bipolar voltage drop. As a result of this, increasing the die area of a MOSFET (be that by paralleling or merely creating a larger die area device) will continue to reduce the on-state losses at low set-points, whereas an IGBT will always be clamped at the level of the diodes voltage drop. However, from a cost perspective, the goal should be to use as little SiC die area as possible in any given application.

A quick datasheet survey of commercially available bare dies of SiC-MOSFET and PT Si-IGBT was carried out to discern how much die area is required to have equal conduction loss at rated current. It suggested that, on average, a minimum of approximately 50 % additional die area is required for the MOSFET device to equal the IGBT in terms of conduction loss at full rated current.

4.2.2.3 Undesirable Characteristics

Single-Event Burnout (SEB) — Cosmic ray induced terrestrial neutrons can cause a Single-Event Effect (SEE) in semiconductor devices, most often in the form of the destructive Single-Event Burnout (SEB) [173]. This occurs when a

device is in the off-state and blocking voltage. If a terrestrial neutron collides with the semiconductor lattice, a device failure is probable, either from the turn-on of the parasitic bipolar transistor or a gate rupture [174]. This problem is exacerbated at higher altitudes due to the exponentially rising level of neutrons with increasing altitude [175]. The SEB rates are proportional to the DC voltage applied to a device, with a higher voltage resulting in exponentially higher failure rates [173, 176]. This limits the device utilisation to a maximum of 60–70 % of its voltage rating to maintain a low level of failures. This is especially crucial for those designed to be used at high altitudes, for instance in aerospace applications.

A cosmic ray induced event is not predictable, however the statistical probability of such a failure can be determined. This is defined as the low-altitude Failure in Time (FIT). This has been used in various publications to compare the ruggedness of SiC-MOSFET devices and Si-IGBT devices against cosmic ray induced SEB. The SiC-MOSFET has been found to be more robust — i.e. has a lower level of FIT — compared to the Si-IGBT [176]. It has also been shown that commercially available SiC diodes are more robust than the Si diodes [173, 176]. These investigations involved steadily increasing the applied voltage and monitoring for an avalanche event, whilst applying a constant source of neutrons from a spallation neutron flux beam. What is unclear from these investigations is whether or not the superior robustness of SiC can be attributed to an over-rating of the manufacturers stated breakdown voltage for the device.

4.3 Required Measurement Bandwidth for SiC

This work builds on the discussion and overview presented in Section 3.6, which outlined the measurement equipment used in conjunction with the DPTR, to show experimentally what bandwidth of measurement equipment is actually required for high-capacity SiC devices. Two of the SiC-MOSFETs listed in Table 3.6 are tested: the 90 A C2M0025120D [151] which is housed in a TO-247-3 discrete package and the 300 A CAS300M17BM2 [139] which is housed in a 62 mm module. These were chosen as there is a clear difference in current rating, hence die area and switching speed.

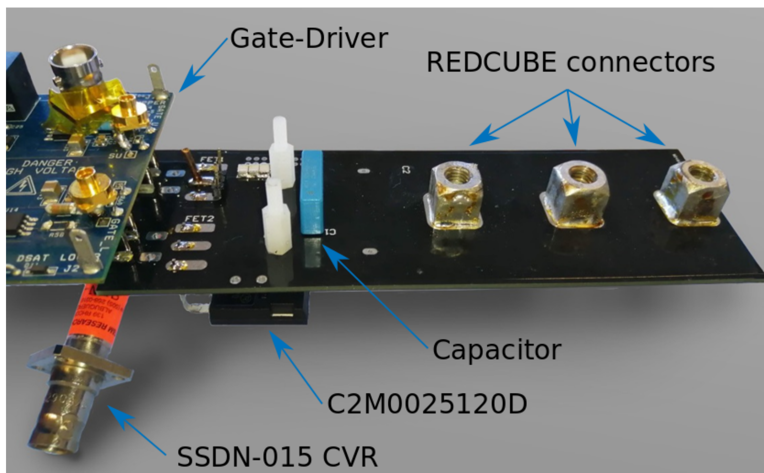


Figure 4.4: TO-247-3 busbar interface PCB.

As the DPTR was primarily intended to test large modules — with the first iteration of busbar designed to interface with 62 mm module — a bespoke Printed Circuit Board (PCB) was required for testing the C2M0025120D TO-247-3 discrete device. A photograph of this can be seen in Figure 4.4. This PCB was designed such that it emulates the mounting fixtures of the 62 mm modules. This was achieved using the Würth Elektronik REDCUBE wire-to-board high-current connectors. A local high-frequency decoupling capacitor was also placed close and adjacent to the half-bridge.

4.3.1 Voltage Probe Measurements

The differential voltage probes used were: the 800 MHz IsoVu TIVH optically isolated probe from Tektronix; the 100 MHz HD3505a probe from Teledyne LeCroy; and the 50 MHz P5210 probe form Tektronix. Full details of these probes are listed in Table 3.8. Turn-on and turn-off for the 90 A and 300 A SiC-MOSFETs are shown in Figure 4.5.

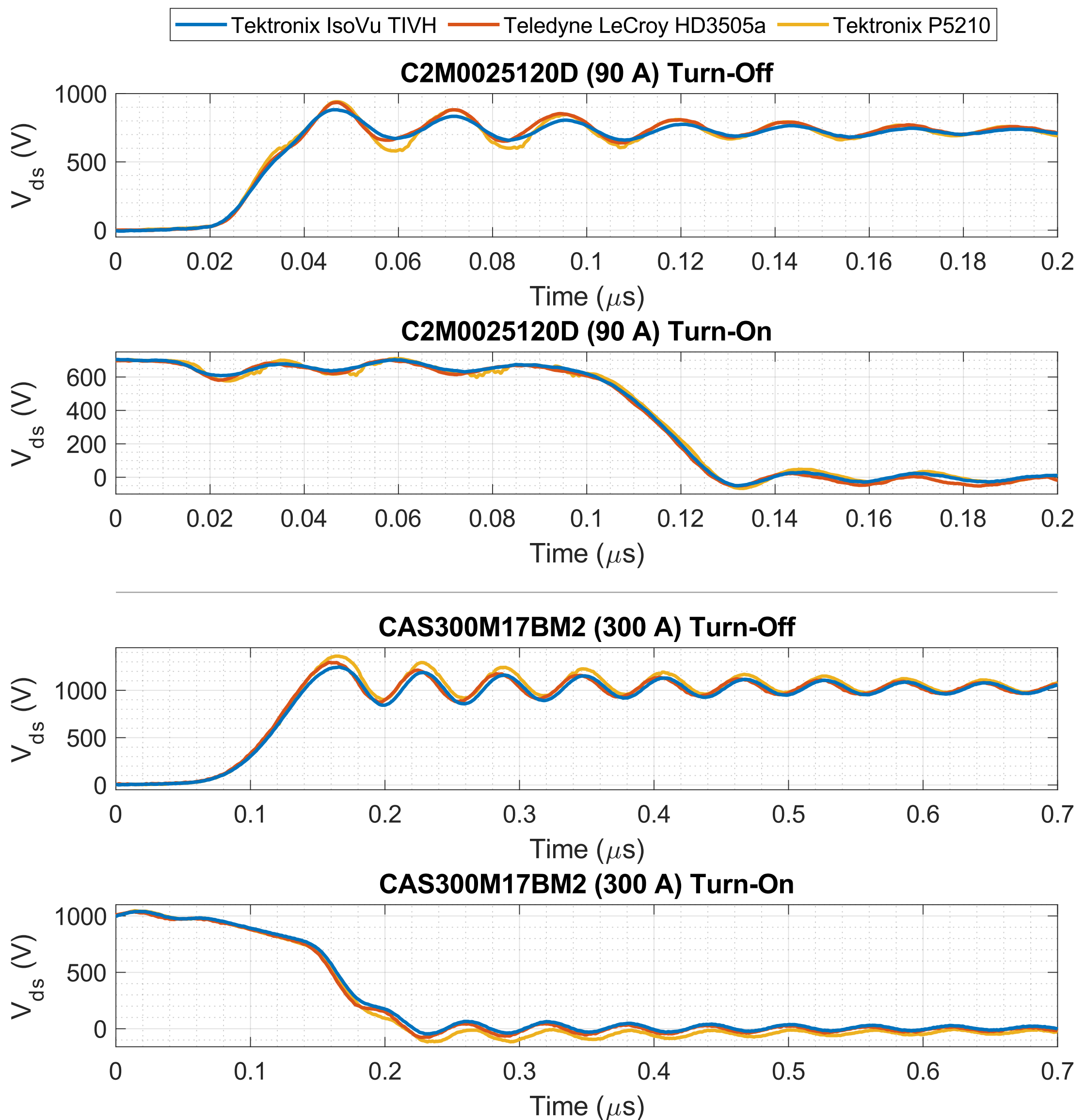


Figure 4.5: High-bandwidth experimental equipment — voltage measurements.

4.3.2 Current Probe Measurements

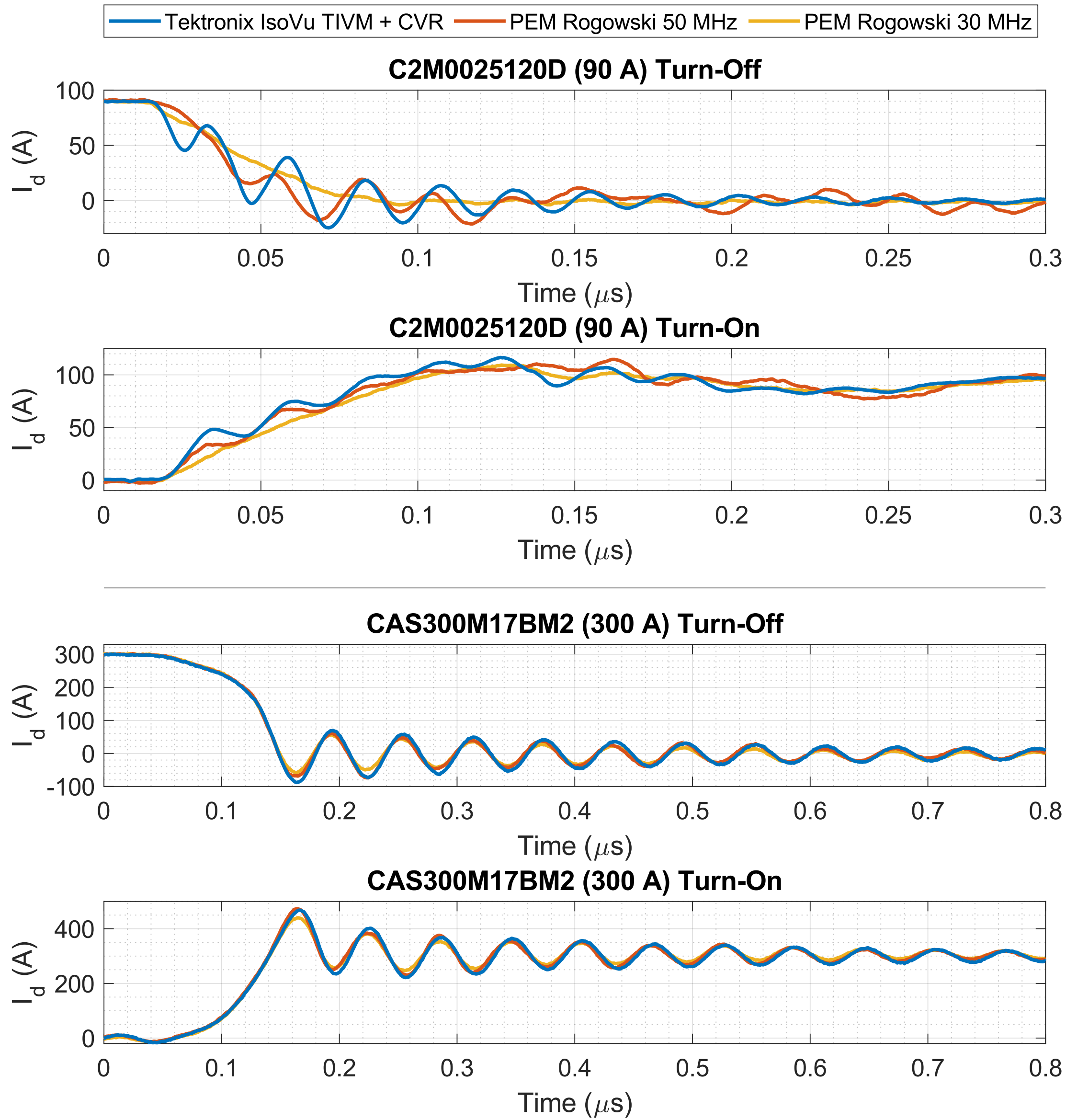


Figure 4.6: High-bandwidth experimental equipment — current measurements.

As discussed in Section 3.6, two current measurement methods were used: the voltage drop across a coaxial shunt, achieved using the 1 GHz IsoVu TIVM optically isolated probe from Tektronix with the 1.2 GHz Current Viewing Resistor (CVR) from T&M Research Products; and a 50 MHz and a 30 MHz Rogowski coil from PEM. Further details of these are in Tables 3.9 and 3.10. Both Rogowski coil measurements were taken with the CVR connected to ensure that any im-

pact from CVR does not skew the comparison. Figure 4.6 shows the turn-on and turn-off current waveforms of the 90 A and 300 A SiC-MOSFETs.

4.3.3 Discussion on the Probes

In Section 3.6, it was determined that a minimum measurement equipment bandwidth of 50 MHz for the 90 A C2M0025120D MOSFET and 25 MHz for the 300 A CAS300M17BM2 MOSFET was required.

The voltage measurement plots (Figure 4.5) show that all three of the probes tested are able to capture the rising/falling edge of the device voltage. If the 800 MHz IsoVu probe — which in 2020 costs >£22,000 — is to be accepted as the most accurate, the 100 MHz HD2505a and 50 MHz P5210 (which cost £2,000 and £1,400, respectively) exhibit a small difference in gain at high-frequencies, which is noticeable during the oscillations. A small amount of phase difference can also be observed.

When considering the current measurement device (Figure 4.6), a significant discrepancy can be seen when testing the 90 A C2M0025120D SiC-MOSFET. The IsoVu and CVR combination shows a resonance of ∼42 MHz. The 50 MHz Rogowski coil is able to capture a large proportion of this, however there is a significant difference in gain and phase due to this resonance being close to the probe's corner frequency. The 30 MHz, which clearly has less bandwidth than the resonant frequency of the DUT, detects none of the oscillatory behaviour. For the 300 A CAS300M17BM2 SiC-MOSFET the waveforms are comparable, albeit with some gain variations. At the time of purchase the IsoVu + CVR, 50 MHz Rogowski coil, and 30 MHz Rogowski coil cost >£22,000 (+£350 for CVR), £1,000, and £800, respectively.

4.4 Hybrid IGBT

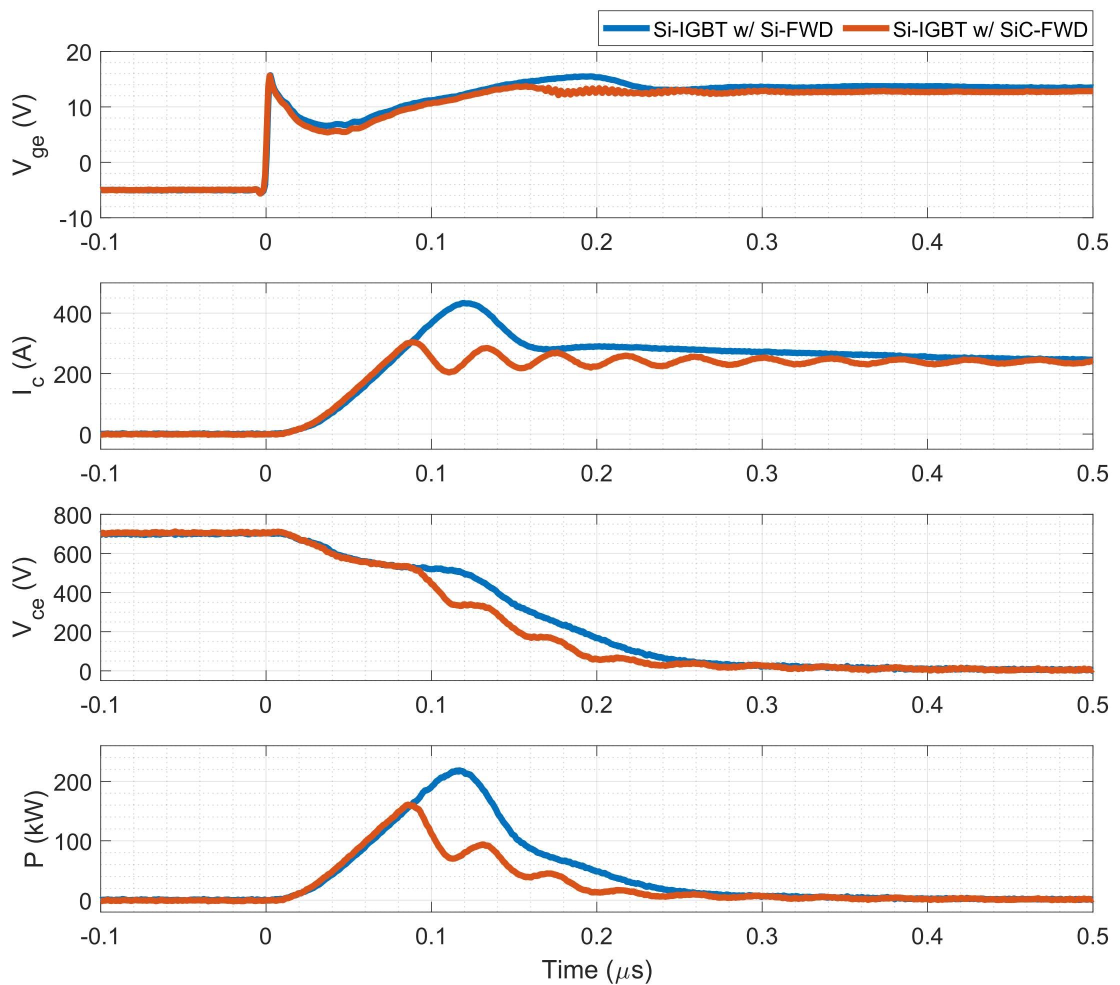
This section investigates a hybrid IGBT concept which has started to attract interest from device manufacturers. It makes use of the Si-IGBT with the now relatively mature SiC-Schottky diode as its FWD. It is not yet clear if this solution will act as an intermediary stage before moving to a full SiC solution, or in fact be considered as a legitimate option in the future. Whilst the benefits of this hybrid device are already known, the experimental investigation in this section confirms these benefits and functions as a verification that the DPTR is capable of comparing different devices in terms of their EMI characteristics and switching losses.

4.4.1 Si-IGBT with SiC-FWD

The Si/SiC hybrid IGBT has been shown to significantly reduce E_{On} [177, 178]. This is achieved as a result of the improvement — potentially even nullification depending on the specific device technology used — in the reverse recovery characteristics of the SiC-Schottky diode. This vastly reduces the overshoot current event which happens at turn-on. This was experimentally verified by testing two identical IGBT devices from Semikron in the DPTR. These were: the SKM200GB12F4 module [179], a Si-IGBT with Si-Fast Recovery Diode (FRD); and the SKM200GB12F4SiC2 module [180], a Si-IGBT with SiC-Schottky Barrier Diode (SBD). The SiC-SBD used in the package is manufactured by ROHM.

The turn-on switching waveforms of this comparison are shown in Figure 4.7. The reduction in overshoot current is evident when using the hybrid IGBT. It can also be seen that the elimination of the reverse recovery current results in the

voltage collapse in V_{ce} occurring earlier in time. As shown in the instantaneous power plot, using the SiC-SBD allows for a lower level of loss at turn-on. The E_{On} for the standard Si module is 22.9 mJ, whereas the hybrid module achieves an E_{On} of 14.6 mJ. This corresponds to a reduction in E_{On} of 36.5 %. Furthermore, the Si-FRDs reverse recovery time increases significantly with an increase in temperature as it is a bipolar conduction device. In the case of the hybrid IGBT, there is still an increase in E_{On} with temperature, however this is not compounded by the SiC-SBD. This is due to SiC-SBD being capacitive, thus minimally impacted by temperature increases.

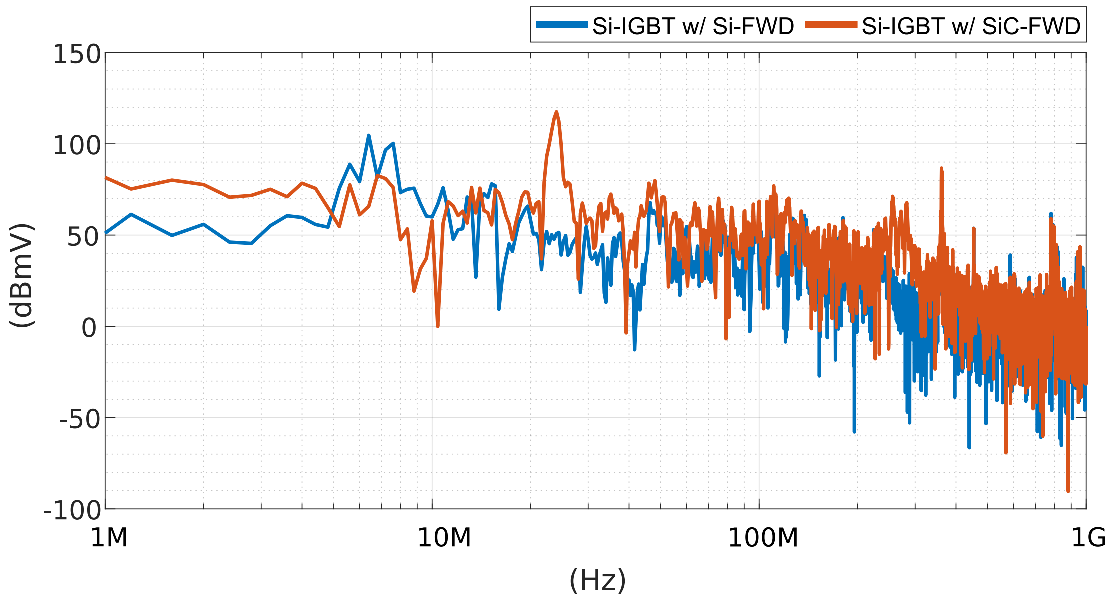


Corresponding FFT of antenna measurement shown in Fig. 4.8.

Figure 4.7: Experimental waveforms of turn-on switching transition, standard Si-IGBT with Si-FRD (SKM200GB12F4 [179]) compared to Si-IGBT with SiC-SBD (SKM200GB12F4SiC2 [180]). Tested at 250 A, 700 V with device baseplate set to 100 °C.

The turn-off switching waveforms are not shown, however a small improvement is also realised during this transient due to a faster dV/dt in the case of the hybrid device. This is due to the reduced parallel capacitance from the FWD. This can also be inferred from the stated dV/dt values in the datasheets [179,180]. By analysing the diode forward characteristics in each datasheet, the SiC-SBD shows a ~20 % reduction in on-state voltage to the Si-FRD, hence an additional improvement when the diode is conducting.

Whilst a lower level of E_{On} has been shown in Figure 4.7, a substantial amount of additional oscillatory behaviour is present with the SiC-SBD. This can be seen in the I_c plot (Figure 4.7) as an oscillation of ~24 MHz. The Fast Fourier Transform (FFT) plot of the antenna measurement (Figure 4.8) confirms that a large amount of energy is radiated at ~24 MHz — approximately 67 dB more than the standard Si-IGBT solution at this frequency. It should also be noted that there is a reduction in the SiC-SBD emissions just bellow 10 MHz which is not fully understood.



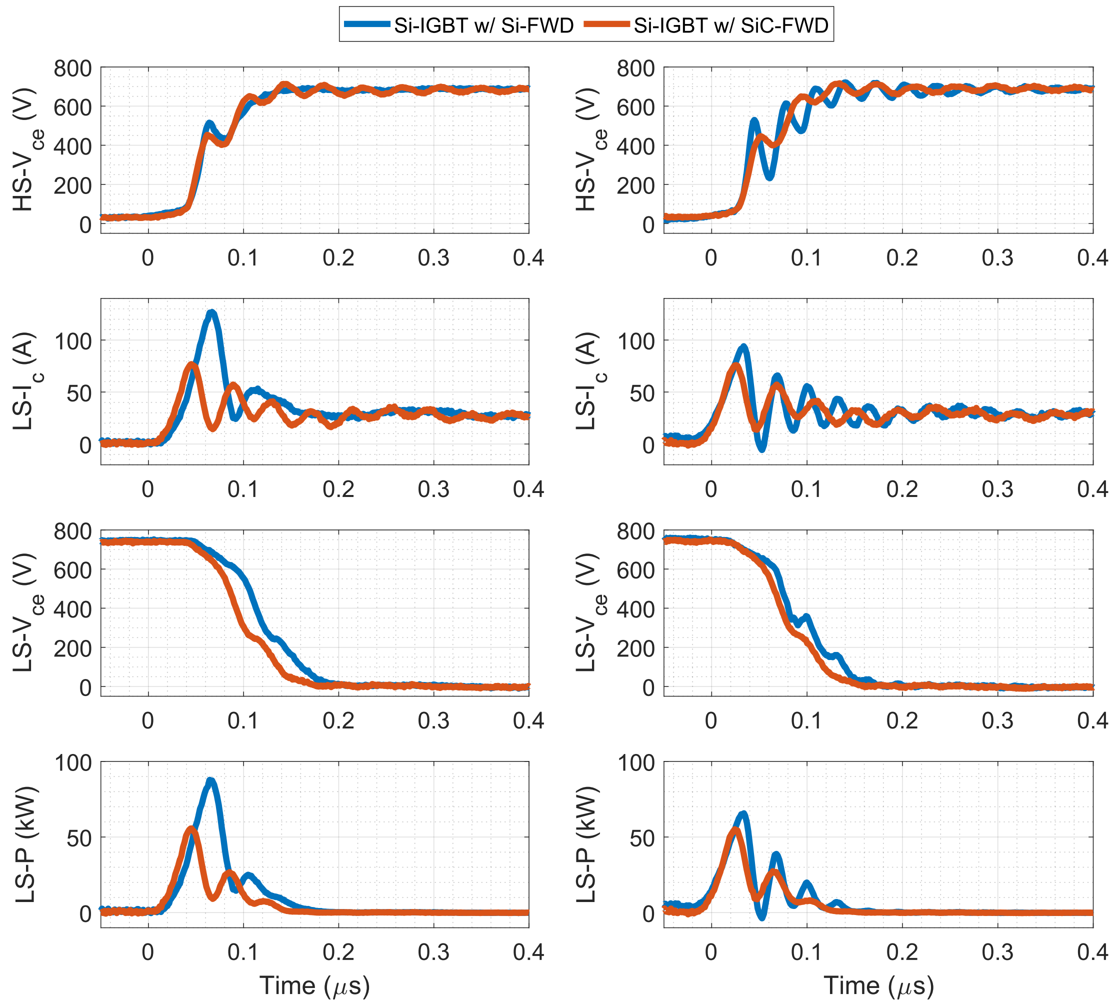
Corresponding voltage & current waveforms shown in Fig. 4.7.

Figure 4.8: FFT of antenna measurements.

4.4.2 Snappy Diode Recovery Behaviour

One further benefit that can be realised by moving from a Si-FRD to a SiC-SBD is the elimination of any "snappy" behaviour, thanks to using a diode technology which does not exhibit a reverse recovery mechanism. This is not a consequence of utilising the WBG material, it is in fact due to moving from a bipolar *pin* structure in the Si-FRD to a unipolar Schottky structure in the SiC-SBD (as explained in Chapter 2, SiC allows unipolar devices to be used at higher voltages than their Si counterparts, hence Schottky diodes principally are manufactured using SiC). Diode snappiness is defined as a high dI/dt during the recovery which cause voltage overshoot and oscillatory behaviour, and is due to the minority carrier lifetime. The *pin* diode will be designed to have soft-recovery characteristics, however at some specific operating conditions a severe snap-off can occur — specifically at low-current levels (relative to nominal current rating) and where the freewheeling diode time (t_{fw}) is small [181–183]. It is reported in [184] that this snappy behaviour is affected by t_{fw}, with shorter on periods at low currents being particularly worse.

To demonstrate this — and to show how using a SiC-Schottky option negates this issue — Figure 4.9 shows a 20 A test; Figure 4.9a with a t_{fw} of 1.0 μs and Figure 4.9b with a t_{fw} of 0.4 μs. The High-Side (HS) device voltage (i.e. the diode which possesses the potential snappy behaviour) is also shown. It can be seen that the waveforms in Figure 4.9a show a typical turn-on of the Low-Side (LS) device. The full Si option (in blue) shows a normal voltage transient across the HS and LS device with the expected current overshoot in the LS I_c due to the reverse recovery of the HS diode. The hybrid module (in orange) shows no reverse recovery characteristics from the SiC-SBD but with some oscillatory behaviour. When moving to a t_{fw} of 0.4 μs (Figure 4.9b), the snappy behaviour of the Si-



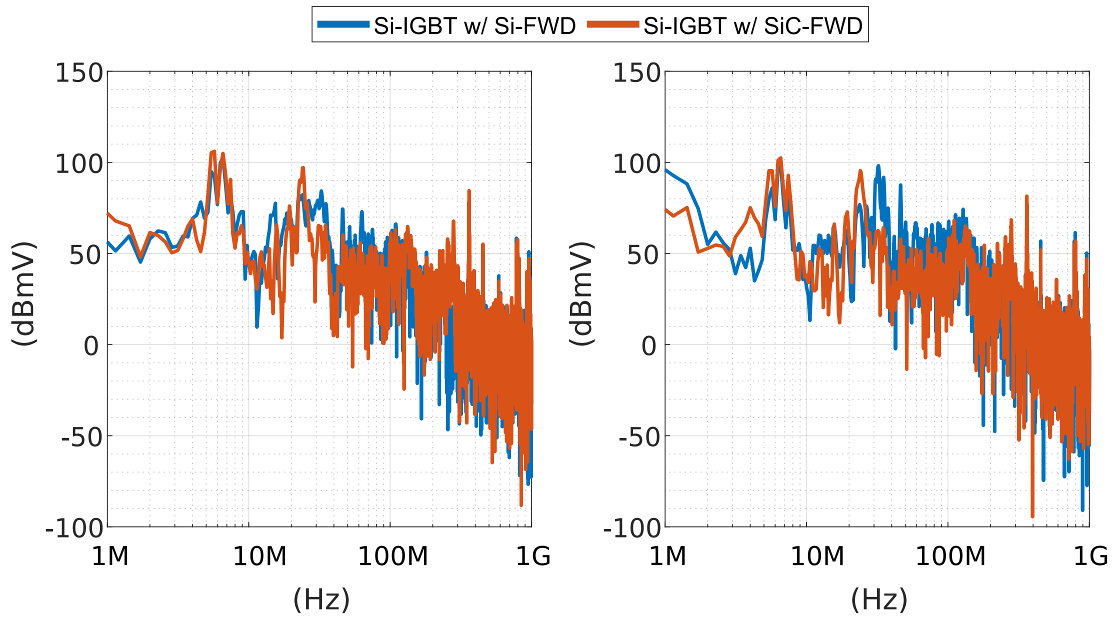
(a) $t_{fw} = 1.0$ μs.

(b) $t_{fw} = 0.4$ μs.

Corresponding FFT of antenna measurement shown in Fig. 4.10.

Figure 4.9: Experimental waveforms of turn-on switching transition showing snappy diode behaviour, standard Si-IGBT with Si-FRD (SKM200GB12F4 [179]) compared to Si-IGBT with SiC-SBD (SKM200GB12F4SiC2 [180]). Tested at 20 A, 700 V with device baseplate set to 100 °C.

FRD can be seen. A large amount of oscillations (with a frequency of 32 MHz) in both the HS diode voltage and LS device current is evident. The behaviour of the hybrid IGBT remains unchanged between the 1.0 μs and 0.4 μs t_{fw}.



(a) $t_{fw} = 1.0\ \mu$s.

(b) $t_{fw} = 0.4\ \mu$s.

Corresponding voltage & current waveforms shown in Fig. 4.9.

Figure 4.10: FFT of antenna measurements.

The antenna measurements of each t_{fw} (shown in Figure 4.10) confirms that the snappy diode event does produce a significant amount of RF emissions at 32 MHz — an increase of 8 dB from 1.0 μs to 0.4 μs.

In an operational converter, the minimum diode conduction period can normally be set by controlling the IGBT off periods. However, when a switching event happens at, or close to a zero crossing point in the phase current, any diode freewheeling period could result in a snappy diode event due to a momentary change in polarity of the phase current. The results in Figures 4.9 and 4.10 show that the small free wheeling period would not result in large RF emission events if a SiC-SBD is employed. Nonetheless, moving to hybrid IGBT solutions comes with the caveat of the customary oscillatory behaviour. However, this would be predictable and could be adequately addressed when designing the converter and its Electromagnetic Compatibility (EMC) filters.

4.5 Slowing Down SiC-MOSFET Transients

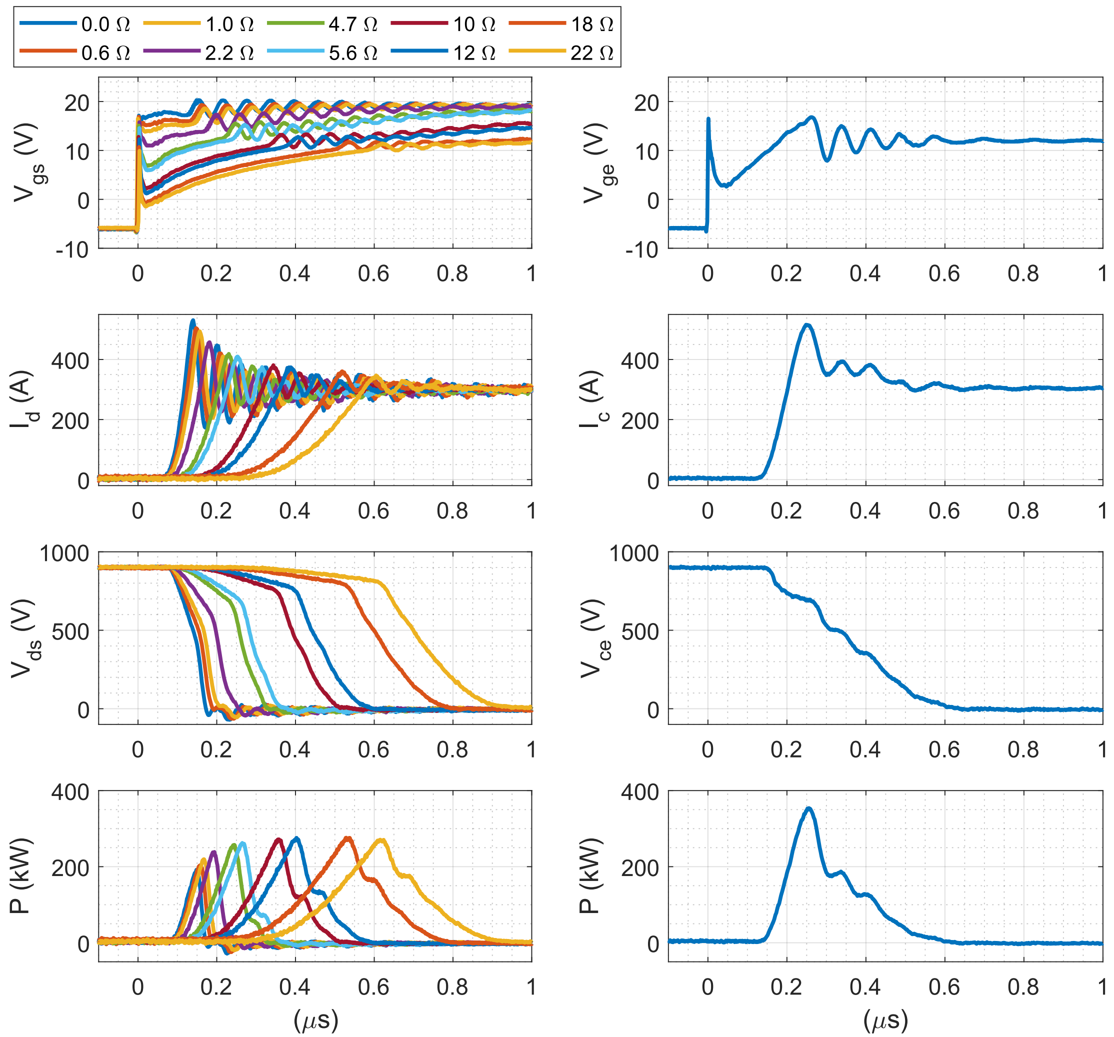
A significant barrier to the uptake of SiC-MOSFETs is the high dI/dt, dV/dt, and oscillatory behaviour that has already been discussed and experimentally shown in this thesis. With these behaviours resulting in increased radiated and conducted emissions. These emissions can be a concern for passing emissions standards testing, but more fundamentally, can also compromise a Power Electronic (PE) converter's functional self-immunity[1].

This section will show how much a high-capacity SiC-MOSFET must be "slowed" down — by means of increasing the value of the gate resistance — to make the potential sources of EMI equal or less than that of a similarly rated Si-IGBT, without compromising the switching loss benefits. The compromises in SiC switching speed are illustrated by this indicative study which compares similarly rated SiC and Si devices.

The SiC-MOSFET device and Si-IGBT device used in this investigation were the CAS300M17BM2 [139] from Cree and the FF300R12KT4P [185] from Infineon, respectively. The external gate resistance for the SiC device was varied between 0.0–22.0 Ω (internal device $R_g = 3.7\ \Omega$). The turn-on and turn-off transients are shown in Figure 4.11 and Figure 4.12, respectively. The gate resistor used for the Si-IGBT was the datasheet recommended value of 1.8 Ω.

As shown in both Figures 4.11 and 4.12, an increase in gate resistance decreases the switching speed of the SiC-MOSFET. This reduction in switching speed can clearly be seen to reduce the magnitude of oscillations and overshoot

[1]Functional self-immunity being defined as the converter's ability to operate as expected and not have internally produced EMI cause unexpected behaviour – e.g., noise pick-up on gate signals, corruption of measurement signals, and/or noise induced errors in the control platform.



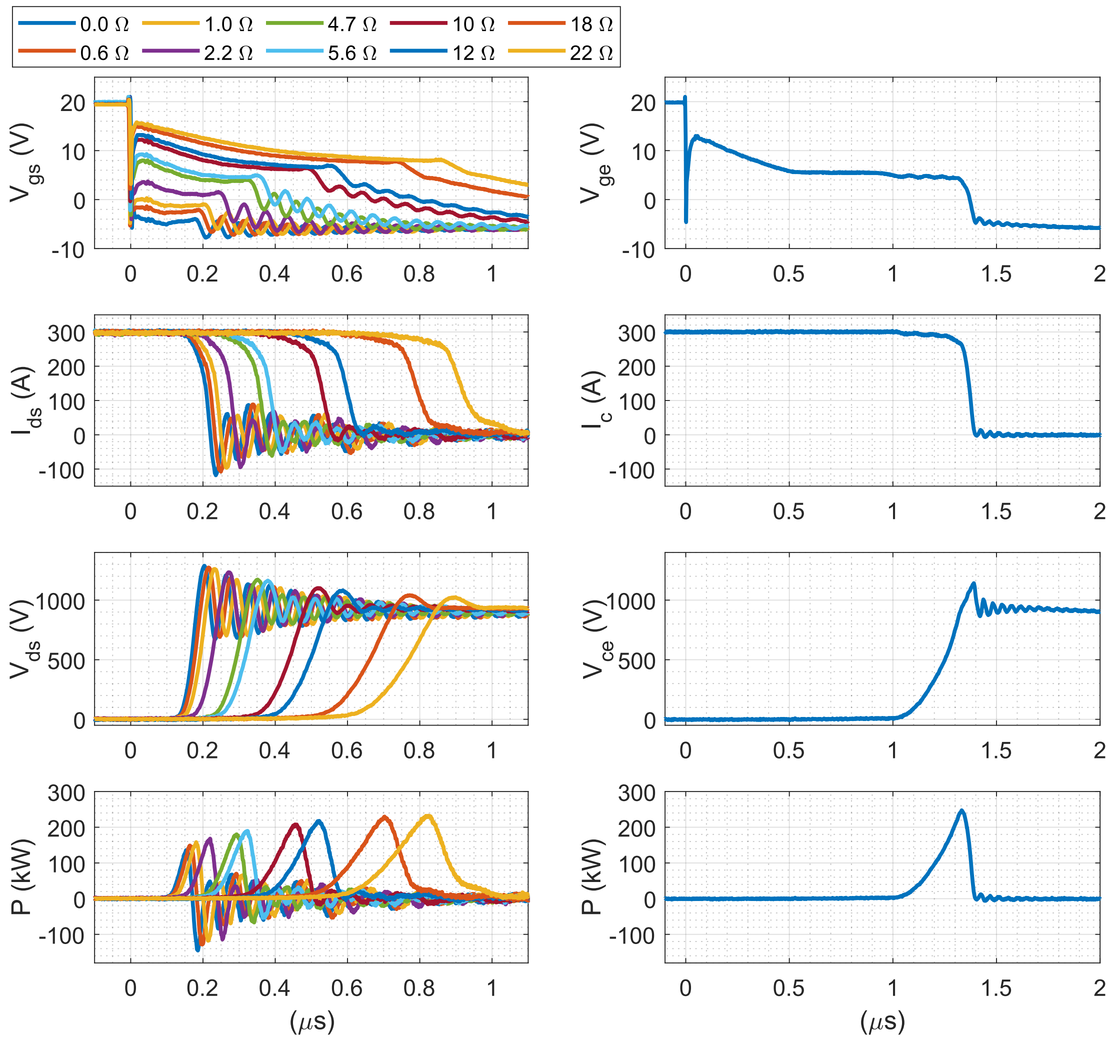
(a) SiC-MOSFET CAS300M17BM2 [139].

(b) Si-IGBT FF300R12KT4P [185].

Corresponding FFT of antenna measurement shown in Fig. 4.14a.

Figure 4.11: Experimental waveforms of SiC-MOSFET turn-on transient, varying gate resistance.

phenomena, however this comes at the expense of an increase in switching energy. This can be empirically observed as an enlargement of the "power triangle" in the instantaneous power plots.



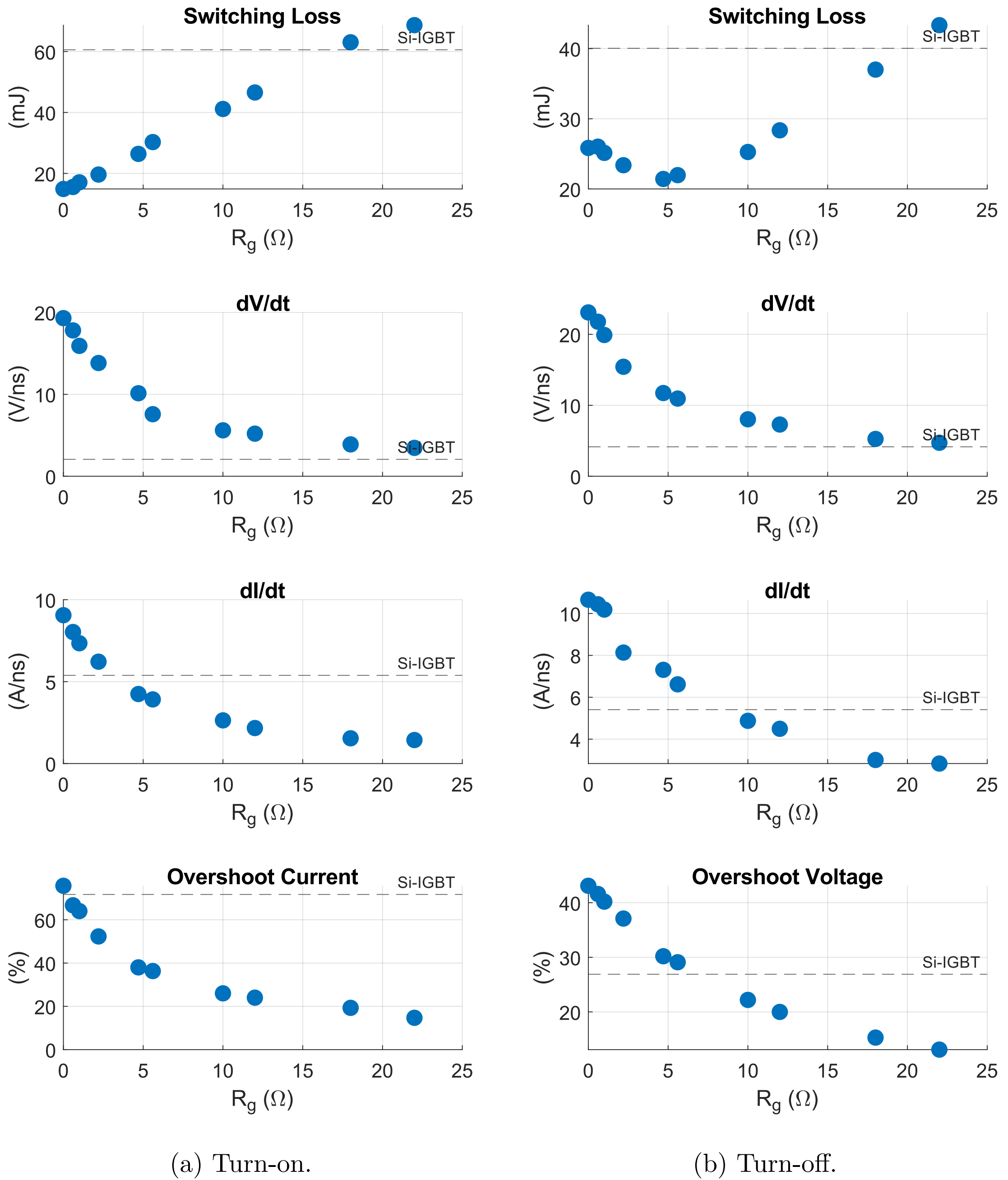
(a) SiC-MOSFET CAS300M17BM2 [139].

(b) Si-IGBT FF300R12KT4P [185].

Corresponding FFT of antenna measurement shown in Fig. 4.14b.

Figure 4.12: Experimental waveforms of SiC-MOSFET turn-off transient, varying gate resistance.

In order to equate the SiC-MOSFET dI/dt, dV/dt and resultant energy dissipation with that of the Si-IGBT, the plots in Figure 4.13 have been generated with the grey dashed line representing the IGBT level and the blue dots representing the data values for the MOSFET.



(a) Turn-on. (b) Turn-off.

Figure 4.13: Slowing down SiC-MOSFET, current and voltage waveform analysis.

The top two plots in Figure 4.13 show the switching energy analysis. It can be seen that it requires $R_{g_on} \approx 17.5\ \Omega$ and $R_{g_off} \approx 20.0\ \Omega$ for the SiC-MOSFET to be equal to the switching loss performance of the Si-IGBT. Therefore, any value of gate resistance less than that will still result in an improvement in switching loss. It should also be noted that for the case of the turn-off, the minimum switching loss is not in fact achieved with the lowest level of R_g, unlike the turn-on transient. This is due to the extreme oscillatory behaviour and voltage overshoot which occurs with a very low level of resistance. This trend can also be clearly observed in Figure 4.13b. The other plots in Figure 4.13 are all precursors to EMI — the rate of switching speed (both dV/dt and dI/dt), the amount of current overshoot at turn-on, and the amount of voltage overshoot at turn-off. Trend lines were added to the data points in order to identify the required gate resistance values which yield the same level as the Si-IGBT for each category. These specific values of R_g are listed in Table 4.1 along with the resultant switching losses. The minimum switching loss with its corresponding R_g value and the aforementioned maximum value of R_g — which results in an equal switching loss — are also shown. These are both listed in the top two entries of each section in the table.

Clearly the values in Table 4.1 of switching loss, gate resistance and other switching parameters are specific to the particular devices which have been characterised in these tests (and with this circuit's unique parasitic characteristics). However, this provides an indicative comparison to show approximately how much "slowing down" of SiC-MOSFETs is required if the EMI precursors are to be kept in line with traditional Si-IGBTs. The potential for being a common-mode current aggressor — which comes as a result of large dV/dt transients and parasitic coupling capacitances — can be inferred from the data in Figure 4.13 and Table 4.1. At turn-on, the MOSFET requires to be slowed down to a point where E_{On} is actually greater than that of the IGBT to make the dV/dt values equal. However, if $R_{g_on} = 17.5\ \Omega$ is chosen, and E_{On} is the same for both devices,

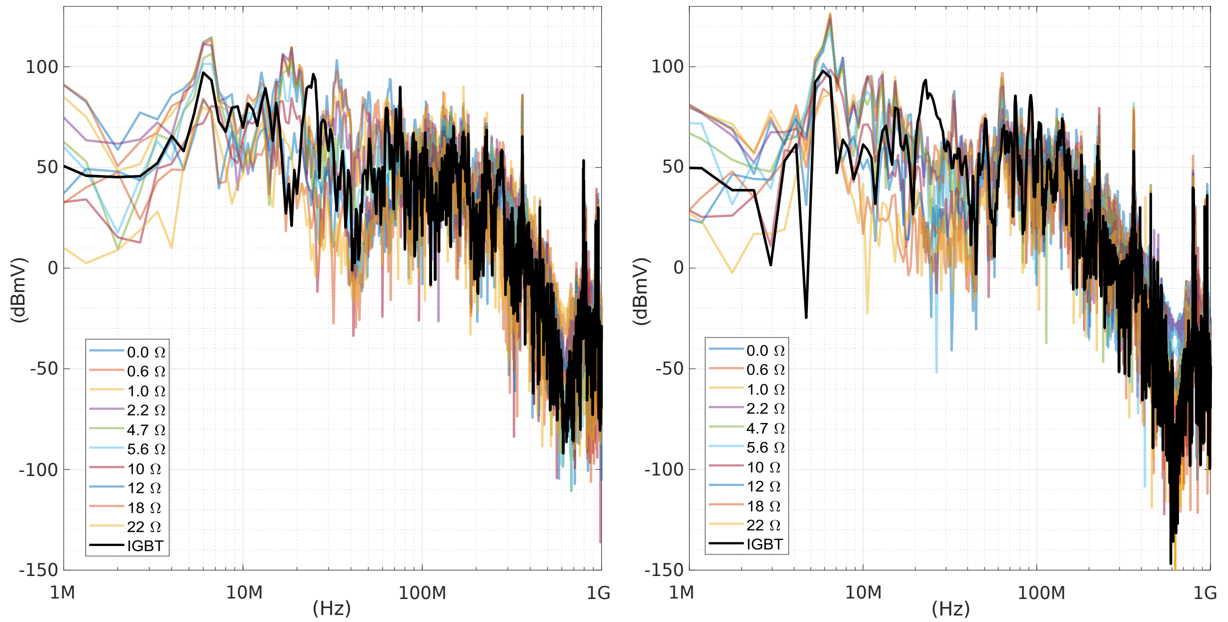
	SiC-MOSFET Turn-On		
	R_{g_On}	E_{On}	
min. E_{On}	0.0 Ω	14.9 mJ	
$= E_{On}$ of Si-IGBT	∼ 17.5 Ω	61.6 mJ	
$= dV/dt$ of Si-IGBT	∼ 25.5 Ω	∼ 80.0 mJ	(2.06 V/ns)
$= dI/dt$ of Si-IGBT	∼ 3.7 Ω	∼ 24.3 mJ	(4.15 A/ns)
	SiC-MOSFET Turn-Off		
	R_{g_Off}	E_{Off}	
min. E_{Off}	4.7 Ω	21.4 mJ	
$= E_{Off}$ of Si-IGBT	∼ 20.0 Ω	40.5 mJ	
$= dV/dt$ of Si-IGBT	∼ 21.2 Ω	∼ 42.5 mJ	(5.38 V/ns)
$= dI/dt$ of Si-IGBT	∼ 9.6 Ω	∼ 24.7 mJ	(5.41 A/ns)
Overshoot Voltage	∼ 7.7 Ω	∼ 23.0 mJ	(26.9 %)

Table 4.1: Gate resistance required for SiC-MOSFET to achieve level of Si-IGBT in EMI precursors in Fig. 4.13.

the magnitude of the MOSFET dV/dt is ∼4 V/ns — this is still double that of the IGBT but one quarter that of the MOSFET with its recommended R_{g_on}. At turn-off, making the dV/dt equal results in approximately the same level of E_{Off}. Matching the dI/dt values, for both turn-on and turn-off, does not require a large increase in gate resistance. The voltage overshoot of the SiC-MOSFET at turn-off can be made equal to the Si-IGBT for a small increase in gate resistance which only results in an additional 2.6 mJ of E_{Off}.

To look at the potential of far-field radiated RF noise, the FFT plot of the antenna measurement is also shown in Figure 4.8. The Si-IGBT is shown as the solid black line and the R_g varying SiC-MOSFET measurements shown as the 50 % opacity coloured lines.

The high levels of oscillatory behaviour that can be seen in the SiC-MOSFET voltage and current waveforms (Figure 4.11 and Figure 4.12) for the low levels of R_g can be seen to result in a significant amount of radiated RF noise in Figure 4.14. As expected, an increase in R_g results in a high degree of reduced EMI



(a) Turn-on.

(b) Turn-off.

Corresponding voltage & current waveforms shown in Fig. 4.11 & 4.12.

Figure 4.14: FFT of antenna measurements.

at certain frequencies. This is particularly apparent at many of the spikes in spectral content between 5–100 MHz. In general, the Si-IGBT data line is situated in the middle of the MOSFET data, i.e. approximately at the 5.6 Ω and 10 Ω lines. However, due to the IGBTs own resonant frequencies, there are some points at which the IGBT radiated emissions are higher than the MOSFET.

If the deployment of SiC is not to improve switching losses and/or increase switching frequency of the converter but instead to merely improve conduction losses, slowing down the MOSFET is feasible. This could make the transition to SiC easier in terms of radiated and conducted EMI concerns. However, if the improvement in switching losses is requisite, the SiC-MOSFET can still achieve low levels of E_{On} and E_{Off} with an increase in the datasheet recommended gate resistance values such that the EMI precursors can be avoided. Increasing the gate resistance has been shown to have a significant impact on the switching transients, however this passive technique clearly has a considerable impact on

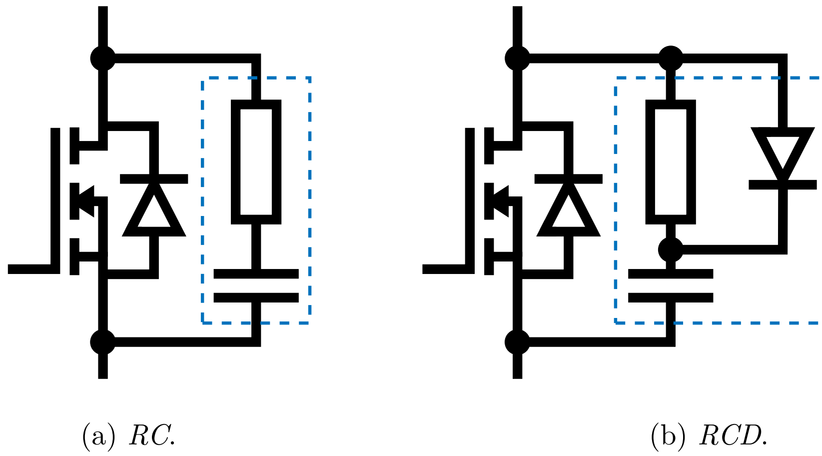
power losses.

4.6 Managing Switching Transients

The previous section has detailed how increasing the gate resistance can manage the switching transients. However, as experimentally shown this comes with an increase in switching loss, thus compromising converter efficiency. Employing techniques to manage the switching transients, whilst not significantly impacting the losses, has seen considerable attention for WBG devices in recent years. Many of these techniques have been invented for use with traditional Si devices, however WBG devices are pushing these concepts further in order to control dI/dt and dV/dt speeds and to dampen oscillations and/or overshoot of voltage and current. This section will briefly discuss two techniques which manage switching transients without increasing the gate resistance, namely the use of snubber circuits and advanced active gate-driving.

4.6.1 Snubber Circuits

The use of passive snubber circuits is one of the most fundamental ways of achieving damping in hard-switched applications. For the purpose of managing the voltage overshoot and subsequent ringing across the transistor during a turn-off switching transition, a snubber network is connected in parallel to the device as shown in Figure 4.15. These networks are tuned such that they limit dV/dt to avoid overshoot and absorb the energy associated with oscillations.



(a) *RC.* (b) *RCD.*

Figure 4.15: Transistor snubber circuits.

Using a snubber network provides the ability to reduce adverse oscillatory and overshoot behaviour and inhibit a lot of RF emission [186]. An increased gate resistance will achieve similar results, but with a larger switching energy. However, due to the snubber network containing a resistive element, there is also an additional loss associated with it. This power dissipation ($P_{snubber}$) can be expressed as (4.1)

$$P_{snubber} = \frac{1}{2} C {V_{dc}}^2 f_{sw} \qquad [\mathrm{W}] \tag{4.1}$$

where: C is the value of the capacitor used; V_{dc} is the DC link voltage; and f_{sw} is the switching frequency. This power loss is independent of load current magnitude. In low-power applications this may be insignificant, however in high-power and/or high switching frequency applications the losses can become excessive. A range of snubber energy recovery circuits have been proposed, these reduce the associated switching loss at the expense of additional passive components [187].

Nonetheless, snubber circuit components can become physically large and thus difficult to integrate into systems, especially in WBG where low-inductance layouts are required. This, along with the additional losses that they incur, have

resulted in snubber circuits being unattractive for many applications.

4.6.2 Active Gate-Drivers (AGD)

Controlling the gate current (amplitude, shape and width) which is sourced or sinked to a transistor has a significant impact on the switching transient. This is confirmed in Section 4.5 by simply varying the gate resistance, a passive way of managing the transients. The use of Active Gate-Drivers (AGD) is a technique which has attracted a significant amount of research attention. Unlike conventional gate-drivers, which apply a step voltage to the transistor gate, AGD involves using circuitry within the gate-driver stage which is designed to control the device switching transients by controlling the amplitude, shape and width of the gate current during the switching transition. This can be done in either a closed-loop or open-loop manner and with various driving techniques.

AGD techniques have previously been used with traditional Si devices, however it is widely reported that this technique is crucial for full exploitation and uptake of WBG devices [188–207].

4.6.2.1 Driving Method

As discussed in Section 3.4.2.1, the two-level drive stage of a conventional gate-driver consists of amplification circuitry (for amplifying the control signal level to levels suitable for gate-driving) usually with separate turn-on and turn-off resistors. In order to influence the gate-current, the AGD driving techniques which have thus far been reported in the literature, range from online tuning of the gate resistance to having a variable voltage- or current-source.

Topologies which utilise the variable gate-resistor approach have been demonstrated in a variety of publications. In [188] an AGD is reported which uses a conventional two-level totem-pole topology with two different switched resistors in both the turn-on and turn-off path. The switched resistors are achieved by placing fast low-voltage transistors in series with the resistors. The topology shown in [189, 190] consists of three parallel connected two-level drive stages (totem-pole with resistors in series with HS and LS transistors). By selecting the number of the branches which are active in the parallel network, the effective gate resistance can be established. The AGDs developed in [188–190] were targeted towards high-capacity SiC-MOSFETs, however the variable gate resistor concept has also seen a lot of attention with respect to driving a Gallium Nitride (GaN) High-Electron-Mobility Transistor (HEMT) device. For example, in [191] a bespoke high-bandwidth Application-Specific Integrated Circuit (ASIC) was developed which is able to finely tune its pull-up or pull-down resistance with a GHz level update rate. This programmable resistive approach can furthermore be considered as a controllable current-source. A bespoke current-drive ASIC was also presented in [192, 193], where a two level Complementary Metal-Oxide-Semiconductor (CMOS) based driver is used. The output stage comprises 63 drive stages in parallel which can be individually selected to determine the current level of the AGD.

Current-source drive techniques, which produce a continuously varying output (as opposed to the discrete styles mentioned in the previous paragraph), are also reported on. These predominantly are achieved using voltage controlled current-sources. An analogue signal, which is typically produced by an Digital-to-Analogue Converter (DAC), is amplified in order to provide enough drive strength. A push-pull emitter follower approach is shown in [194] and [195] using a *pnp* and *npn* Bipolar Junction Transistor (BJT) pair. In [196], the push-pull amplifier approach is improved by adding a bipolar current mirror stage to fur-

ther increase the drive strength. The use of high-bandwidth Operational Amplifier (Op-Amp) was demonstrated in [197, 198]. In these studies the Op-Amp is used in the transconductance mode, such that it acts as a current-source.

In terms of a controllable voltage-source based AGD, two methods can be considered. Either using a continuously variable high-bandwidth voltage-source or using a multi level-based voltage-source with at least three or more levels. However, realising a continuously variable voltage-source at the necessary bandwidth for use with SiC, and at the required drive strength (i.e. current output), for high-capacity modules is not easy. Therefore, multi level-based approaches are emerging as the preferred option. In [199] a three-level approach is demonstrated, where the upper and lower driving levels are at conventional voltage levels (i.e. to fully turn on or off the MOSFET) and the third mid-level voltage is at an intermediate tunable level. This intermediate level can be switched in to provide damping at critical points during the switching transition by briefly sourcing more charge into the gate. For example, a single pulse during the miller plateau period to reduce dI/dt or dV/dt. This level-based voltage drive was shown to achieve good control of the switching trajectories. The level-based concept was also shown in [200], with the addition of the active driver ASIC developed in [191] being employed as the intermediary level which is able to provide a high-resolution of active driving around the gate threshold. This study has shown that being able to influence the device gate voltage with a high-resolution and number of drive levels whilst the device is in the active region, allows for excellent control of fast switching SiC devices.

4.6.2.2 Controller Methods & Use Cases

Both open-loop and closed-loop controller concepts have been demonstrated for AGDs in the literature.

Open-Loop — These methods use predetermined patterns to produce gate-drive signals using either of the drive-stage methods discussed in the previous section. Some of the studies have shown that patterns can be found by manual tuning. However, in much of the literature, various algorithms were employed to search for patterns which are effective. Using an open-loop approach would require various patterns to be determined for the various operating conditions that a device may be exposed to in a converter.

Closed-Loop — A closed-loop approach offers a solution which can adapt to the operating conditions — such as device ageing (for example, V_{Th} shift) and changes in operating voltage, current, temperature and/or EMI. These closed-loop methods can be broadly categorised into two groups:

1. **Instantaneous Closed-Loop** — Those which use circuit-level feedback mechanisms and operate in real-time manner.
2. **Next-Cycle Closed-Loop** — Those which use open-loop style circuitry at the drive-stage, however close the loop by employing feedback signals to a local gate-drive level controller.

The "instantaneous closed-loop" methods have been reported on since the mid-2000s with regard to slower switching Si devices [201, 202]. These rely on high-bandwidth analogue feedback loops using one or more device measurements. The measurements which are fed back are compared to a reference signal using

a comparator with the resultant error signal being used as the gate-drive signal (with one of the driving methods discussed in Section 4.6.2.1). The measurements which are typically used are: a scaled down device voltage, using a voltage divider network, referred to as Active Voltage Control (AVC); the gradient of that voltage (dV/dt) which can be capacitively coupled; the device current, referred to as Active Current Control (ACC); and/or the dI/dt magnitude of the device current. These methods are summarised in [203] and [204]. Other feedback methods exist which do not rely on the device following a predefined pattern, rather the feedback signals can be used to trigger circuitry. For example, dV/dt or dI/dt has been shown to trigger switchable gate resistors [189]. This allows for an increase in gate resistance to dampen the trajectory if the measured gradients go above a certain level. In [205], a small transformer is used as a direct feedback path. The transformer is used to couple energy from the power path back to the gate path during a switching event. The inductive volts that are induced in the gate-side winding can be used to increase or decrease the drive strength depending on the polarity/winding configuration and the device dI/dt.

The “next-cycle closed-loop” methods rely on a local controller (i.e. Field Programmable Gate Array (FPGA) or microcontroller) and one or more Analogue-to-Digital Converter (ADC)s. The drive-stage is then coordinated by the controller — either using the continuously variable or level based current-/voltage-source and/or adjustable gate resistance as previously discussed. This approach allows for patterns to be adjusted for subsequent firing commands, and thus fine-tuned over multiple cycles. The “instantaneous closed-loop” methods can also benefit from this digital feedback which can be used to adjust the pattern at a slower control-loop rate based on measured device parameters.

Due to the extremely fast switching speed of SiC-MOSFETs (and GaN-HEMTs), the “next-cycle closed-loop” is emerging as the preferred option for

closed-loop AGDs. This is due to the "instantaneous closed-loop" being a complex, noise-sensitive, and expensive task. This arises from the necessity of the high-bandwidth circuitry — this includes fast analogue ICs (such as Op-Amps, comparators, and DACs) as well as passive components which are, for instance, used in the RC voltage divider networks. These must have very predictable frequency response and temperature stability. As the "instantaneous closed-loop" method forms a real-time closed-loop controller, it is also bound by control theory, and can thus become unstable if not properly designed.

The main use cases which are reported on for AGD are with regard to managing the switching transients of the transistors to reduce EMI, whilst maintaining low levels of switching losses. This is achieved using the previously mentioned techniques to shape the current and voltage waveforms during the switching transition. The majority of the literature proposes maintaining the fast edges whilst damping the overshoot and oscillatory behaviour in voltage and/or current. However, utilisation of AGDs has been reported on [206, 207] to minimise the EMI issues that arise from the fast edges and sharp corners of the square waves which can, for instance, propagate through the system in the form of common-mode currents. This has been achieved by forcing the devices to switch with "S"-shaped or trapezoidal shaped transients which can negate some of the high-frequency content and high-order harmonics.

Another significant use case for AGDs is in enabling series or parallel connection of multiple devices to reach current or voltage magnitudes that are not possible with single devices. This can be in the form of multiple dies, discrete packages, or modules (as mentioned in Section 4.2). For increasing the voltage rating by means of series connection, all of the switches in the stack need to transition between states at exactly the same time. This is to ensure that any of the devices in the stack are not subject to a higher voltage than they are able

to block. An AVC technique was demonstrated in [202] to achieve switching of series connected Si-IGBTs. The requirements of uniformly synchronised switching are similar when paralleling devices to achieve higher currents. If this is not achieved a device may be forced to conduct a higher current than it is rated for. The cause of different switching transients can come from variances in threshold voltage and stray inductance imbalances (either module parasitic inductance or busbar inductance).

* * *

5 | The Diverter: A Si/SiC Hybrid Switch

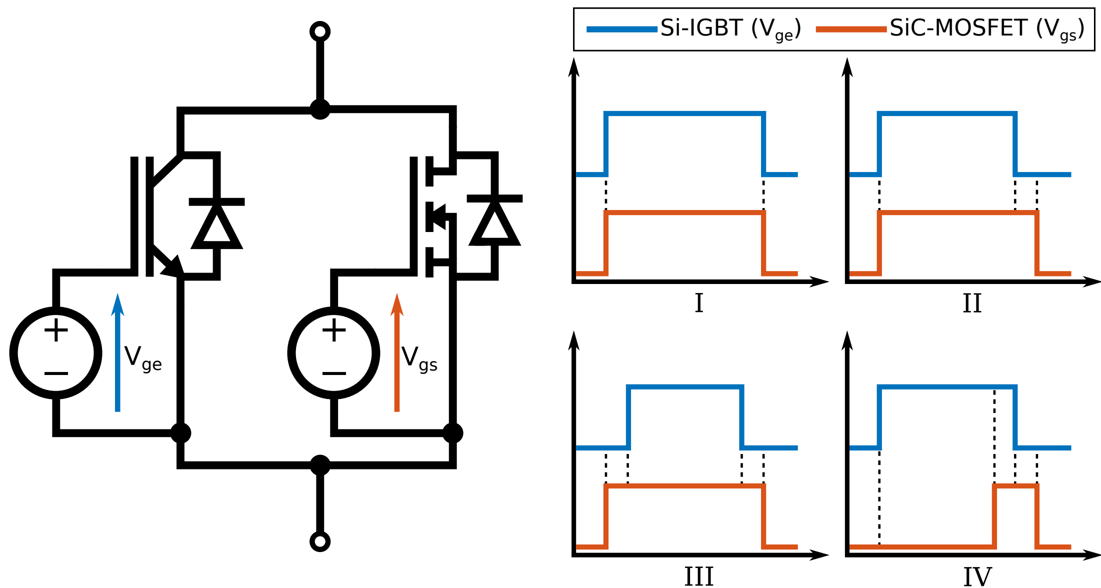
5.1 Chapter Introduction

This chapter details the work undertaken to investigate the complementary switching of Silicon-Carbide (SiC)-Metal–Oxide–Semiconductor Field-Effect Transistor (MOSFET) and Silicon (Si)-Insulated-Gate Bipolar Transistor (IGBT). The resultant hybrid switch, the "Diverter", makes use of the best traits of the composite devices. The core idea of the Diverter is to use a parallel configuration of a fully rated Si-IGBT and partially rated SiC-MOSFET, shown in Figure 5.1a, with coordinated switching used to exploit the complementary traits of each device. These traits being the static performance of Si-IGBT and the dynamic performance of the SiC-MOSFET at turn-off. This method is employed to increase dV/dt and eliminate tail current of traditional Si-IGBT, hence reducing turn-off loss, for only a small increase in cost.

The chapter is structured as follows: Section 5.2 reviews the existing literature, discusses the operating mechanism of the Diverter, and the selection of the devices used in the study; Section 5.3 presents the experimental work that was undertaken to ascertain the optimum timings for the coordinated switching

to achieve minimum switching losses; Section 5.4 provides further performance analysis and covers additional benefits that arise; and finally, Section 5.5 compares the resultant performance to a fully rated SiC-MOSFET and Si-IGBT, and critically discusses the Diverter.

5.2 Diverter: Principle of Operation



(a) Parallel devices. (b) Gate-drive switching schemes.

Figure 5.1: Hybrid switching.

5.2.1 Previous Work in Literature

The concept of a hybrid device consisting of parallel connected SiC-MOSFET and Si-IGBT has been previously reported. Various methods of coordinating the gate signals to each device have been explored. The four gate sequences reported are shown in Figure 5.1b.

5.2.1.1 Gate Sequence: I

ABB experimentally demonstrated a 1.2 kV bespoke module, they called the "Cross-Switch (XS)", which comprised parallel arrangement of one Si-IGBT die and one SiC-MOSFET die [208,209]. The current capacities of the dies were 25 A (6.5 mm $\times$ 6.5 mm) and 30 A (4.1 mm $\times$ 4.1 mm) for the Si-IGBT and SiC-MOSFET, respectively, hence effectively a 1:1 ratio. In this study the composite devices share a gate-driving signal (gate sequence I) and hence share current during the switching and conduction periods. The result of this work shows a small improvement in on-state performance compared to a full Si-IGBT and switching loss performance in-between that of a full Si-IGBT and full SiC-MOSFET, with a reduction in oscillatory behaviour compared to the full SiC solution [210]. A study was carried out in [211] and [212] with a different die arrangement, but similar overall current rating and equal ratio, and showed similar results to the ABB work.

5.2.1.2 Gate Sequence: II & III

Subsequent studies began to investigate varying the timing of the gating signals to each device so that the SiC-MOSFET performs the switching transition(s).

In [213] the driving sequence II was used. In this driving sequence both devices are turned on together and simultaneously conduct, however at the turn-off edge the Si-IGBT is turned off first with the SiC-MOSFET turn-off subsequently delayed by a predefined increment. This allows the IGBT to effectively realise Zero Voltage Switching (ZVS) and the composite device turn-off, using the MOSFET, also achieves a faster dV/dt edge. This study, like the XS work, used equal rating dies with a total current capacity of approximately 50 A

(1.2 kV devices). This was tested in a 20 kHz buck converter and showed a good cost/performance trade-off. Driving sequence III was used in [214]. This is an extension of sequence II, in which the SiC-MOSFET is additionally used on its own at turn-on. This study again used a similar voltage rating, current rating and equal ratio and showed that a buck converter could be operated up to 100 kHz. When the Si-IGBT was used on its own the system was 90.8 % efficient at full load, however the hybrid approach saw an increase in efficiency to 95–96 %.

It is worth noting that sequence II and III are effectively the same. This is due to the faster turn-on speed of the SiC-MOSFET, hence in sequence II the SiC-MOSFET will turn on almost all the current, thus determining the turn-on behaviour.

In [215] a demonstration of sequence II/III at 4 kV, 40 A was presented, with comparisons of a Junction Field-Effect Transistor (JFET) and a MOSFET device as the SiC component. In these studies, the ratio of the current capacity for the dies was altered. This used 10 kV, 10 A SiC device prototypes from Cree and a commercial 6.5 kV, 25 A Si-IGBT from ABB, hence a current capacity ratio of 2.5:1 (Si:SiC). By using a less SiC die area, the turn-off edge achieves an even greater dV/dt due to the reduced device capacitances. A further publication [216] by the same researchers presented a 1.2 kV, 200 A solution 1.5:1 (Si:SiC) and showed that turn-off energy could be reduced by 50 %, however that came at an increase in cost of 4×.

Clearly, using sequence II/III will result in a small period of over-current time for the SiC-MOSFET and, by reducing the current rating of the SiC die, this is only made worse. However, these periods of time are in the low μs and are thus well within the devices Safe Operating Area (SOA). In order to manage any adverse thermal stress on the SiC device, studies have implemented device

temperature as a control parameter. In [217] — sequence II/III, 1.2 kV, 37.5 A, 1.5:1 (Si:SiC) — a 20 kHz buck converter was demonstrated with a temperature control algorithm.

The area in which the biggest gains are realised in all the studies thus far is at the turn-off edge [213–217]. Two mechanisms are responsible for the reduction in turn-off switching loss compared to the Si-IGBT, namely:

Elimination of Tail Current — As discussed in previous chapters, the bipolar conduction and large amount of excess carriers in the Charge Storage Region (CSR) of the IGBT allows for low on-state voltage. This stored charge is relatively slowly swept out (compared to initial MOS-type dI/dt) of the CSR at turn-off and results in a tailing current. The delay period (T_{Delay}) introduced between the turn-off of IGBT and the MOSFET allows that stored charge to be swept out before the main switching transition occurs.

Increase in dV/dt — With the turn-off edge now essentially a SiC-MOSFET transient, the dV/dt is much faster. This is enhanced further when a MOSFET with less die area is used.

Both of these mechanisms are what lead to large reductions in turn-off loss. The difference in switching speed/loss at turn-on between a Si-IGBT and a SiC-MOSFET is far less than the difference in turn-off, hence any gains made using the hybrid switching at turn-on are marginal. This, coupled with the benefit of using less MOSFET die area, would imply that gating sequence IV with a partially rated MOSFET is most likely the best approach.

5.2.1.3 Gate Sequence: IV (The Diverter)

Gating sequence IV (the method investigated in this thesis) has the Si-IGBT conducting for the nominal on period and then briefly diverts the current — hence the name Diverter — to the SiC-MOSFET allowing it to perform the turn-off in the same manner as the previously mentioned studies. The first reporting on using this exact technique was in 1994 [218], however in this study a Si-MOSFET was used as the current bypass device, thus inherently limiting the voltage capability to ∼600 V.

This method is experimentally demonstrated in [219] at 20 A and showed a turn-off loss reduction of 58.3 %. The work published in [220] shows verification of this technique at 60 A, using less SiC die area — 3:1, 4:1, 5:1 (Si:SiC) — and shows good turn-off loss reduction 50–65 %. The concept was also demonstrated in [221–223] by means of a bespoke 1.2 kV, 200 A module with a die ratio of 4:1 (Si:SiC), for high-frequency operation. In these studies, a lot of effort was put into reducing any inter-device stray inductance and the claim was made that this was a necessity for optimum performance of the hybrid switch. Their hybrid switch was tested in a 50 kHz three-phase inverter [222] and a 50 kHz wireless-power transmission converter [223].

5.2.2 Diverter: This Study

The previous work on hybrid switching of Si-IGBT and SiC-MOSFET has focused on achieving high switching frequencies at relatively low-power levels. This imposes a limit on the permissible delay time; necessitates that internal inductance must be minimised, thus leading to specialised hybrid modules; and the turn-off loss benefits that could be achieved by these techniques are compromised

by Pulse-Width Modulation (PWM) minimum off-time. This study focuses on high-power applications with composite high-capacity switches built from a combination of modules.

The experimental investigation will look at the Diverter concept at current levels up to 480 A that would be applicable for use in high-power applications. An ampacity ratio of 4:1 (Si:SiC) of the dies is considered, using off-the-shelf commercially available power modules. The impact of inter-device stray inductance (due to using separate power modules) is investigated to assess whether an integrated composite device is required. The radiated Electromagnetic Interference (EMI) which is generated is analysed, including a natural damping effect on oscillatory behaviour and voltage overshoot — a phenomenon which has not previously been reported on. The Diverter is investigated in the Low-Side (LS) position of the half-bridge using the Double-Pulse Test Rig (DPTR) (discussed in Chapter 3).

5.2.3 Diverter: Overview of Coordinated Switching at Turn-Off

A breakdown of the coordinated switching scheme for the Diverter is illustrated in Figure 5.2. The various stages of which are broken down as follows:

Time t_0 — Close to the end of the Si-IGBT on-period, a turn-on command is given to the SiC-MOSFET. Once the MOSFET is turned on ($V_{gs} > V_{Th,MOSFET}$) the devices begin to share current.

Time t_1 — The turn-off command is given to Si-IGBT. Current continues to share.

Time t_2 — When the Si-IGBT gate volts are not sufficient to support the load

current (this starts a little before the threshold voltage is reached), all of the current rapidly commutates into the SiC-MOSFET causing a large dI/dt. The inter-device stray inductance (L_{Comm}) and large dI/dt result in a small voltage perturbation.

Time t_3 — The SiC-MOSFET now conducts the full load current.

Time t_4 — Turn-off command given to SiC-MOSFET. The Diverter turns off with a fast dV/dt and no tail-current.

Time t_5 — The Diverter is now in the off-state and is blocking voltage.

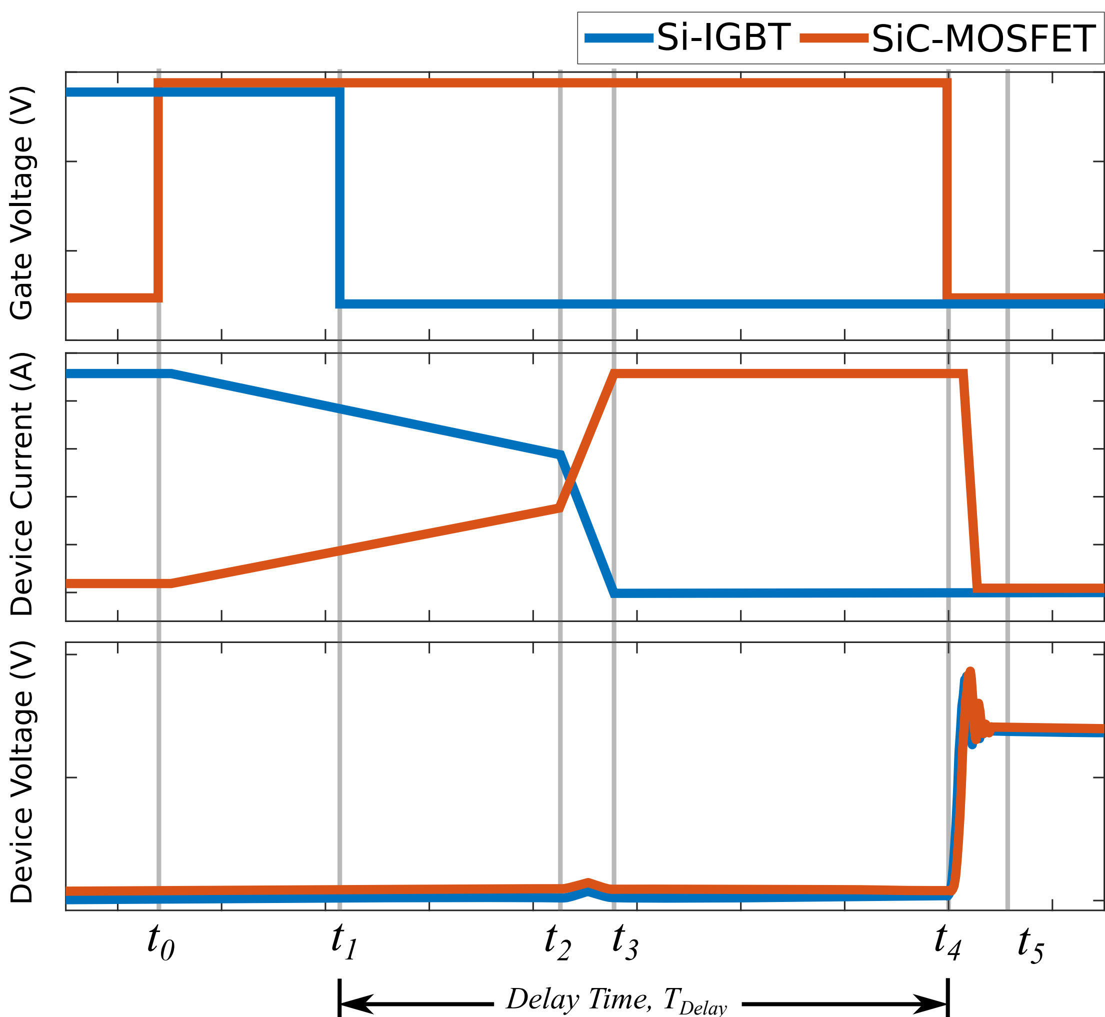


Figure 5.2: Illustration of coordinated turn-off switching scheme for Si/SiC-Diverter.

5.2.4 Diverter: Selection of SiC-MOSFET & Si-IGBT

The devices used for the Diverter switch are shown in Table 5.1. A Si trench-gate field-stop [224] IGBT4 from Infineon (FF450R12KT4 [168]) was selected as the IGBT device. These generation four devices have been designed to favour the conduction profile, by having a significantly increased carrier density in the CSR compared to previous generations, over the switching performance. The result of this is an increased carrier lifetime and hence longer tail current, making it a good candidate for the hybrid concept. A partially rated (4:1) SiC-MOSFET from Cree (CAS120M12BM2 [152]) was selected as the current bypass device — this ratio aligns with the repetitive short-pulse over-current capacity indicated in the datasheet. The composite devices are housed in the 62 mm module package. The performance of the Diverter was compared to a fully rated SiC-MOSFET from ROHM (BSM600D12P3G001 [144]) and the Si-IGBT, used in the Diverter, on its own.

	Diverter Devices		**Full SiC Device**
	Si-IGBT	SiC-MOSFET	SiC-MOSFET
	FF450R12KT4	CAS120M12BM2	BSM600D12P3G001
	Infineon [168]	*Cree* [152]	*ROHM* [144]
Voltage Rating	1.2 kV	1.2 kV	1.2 kV
Current Rating	450 A	120 A	600 A

Table 5.1: Power semiconductor devices used in experimental work.

5.3 Diverter: Determining Delay Period for Minimum Turn-Off Loss

This section will detail the work undertaken to ascertain the value for the required delay period (T_{Delay}) to achieve minimum switching loss — where T_{Delay} comprises the sum of t_1–t_4. The LabVIEW FPGA controller, used to control the DPTR, allowed for fine timing sweeps of T_{Delay} ($2\ \mu s \rightarrow 6.5\ \mu s$ in steps of 250 ns, with high level of repeatability and accuracy). These sweeps were performed with a DC-link voltage of 700 V; at current magnitudes of 120 A, 240 A, 360 A and 480 A; and with the device baseplate set to ∼25 °C (room temperature), 75 °C, 100 °C and 125 °C. The gate resistance for each device was selected to be the datasheet recommended value — $R_{g,ext} = 2.5\ \Omega$ for the SiC-MOSFET and $R_{g,ext} = 1.0\ \Omega$ for the Si-IGBT.

The total Diverter turn-off switching energy E_{off}, can be expressed as (5.1)

$$E_{Div,Off} = E_{Comm} + E_{AddCond} + E_{Switch} \qquad [\mathrm{J}] \tag{5.1}$$

where: E_{Comm} is the commutation energy loss from L_{Comm} and the fast dI/dt; $E_{AddCond}$ is the additional conduction loss penalty that arises from briefly using the SiC-MOSFET to conduct; and E_{Switch} is the actual turn-off switching event. The following sections will discuss each of these components and how they were analysed and measured. Experimental waveforms of the Diverter are shown in Figure 5.3.

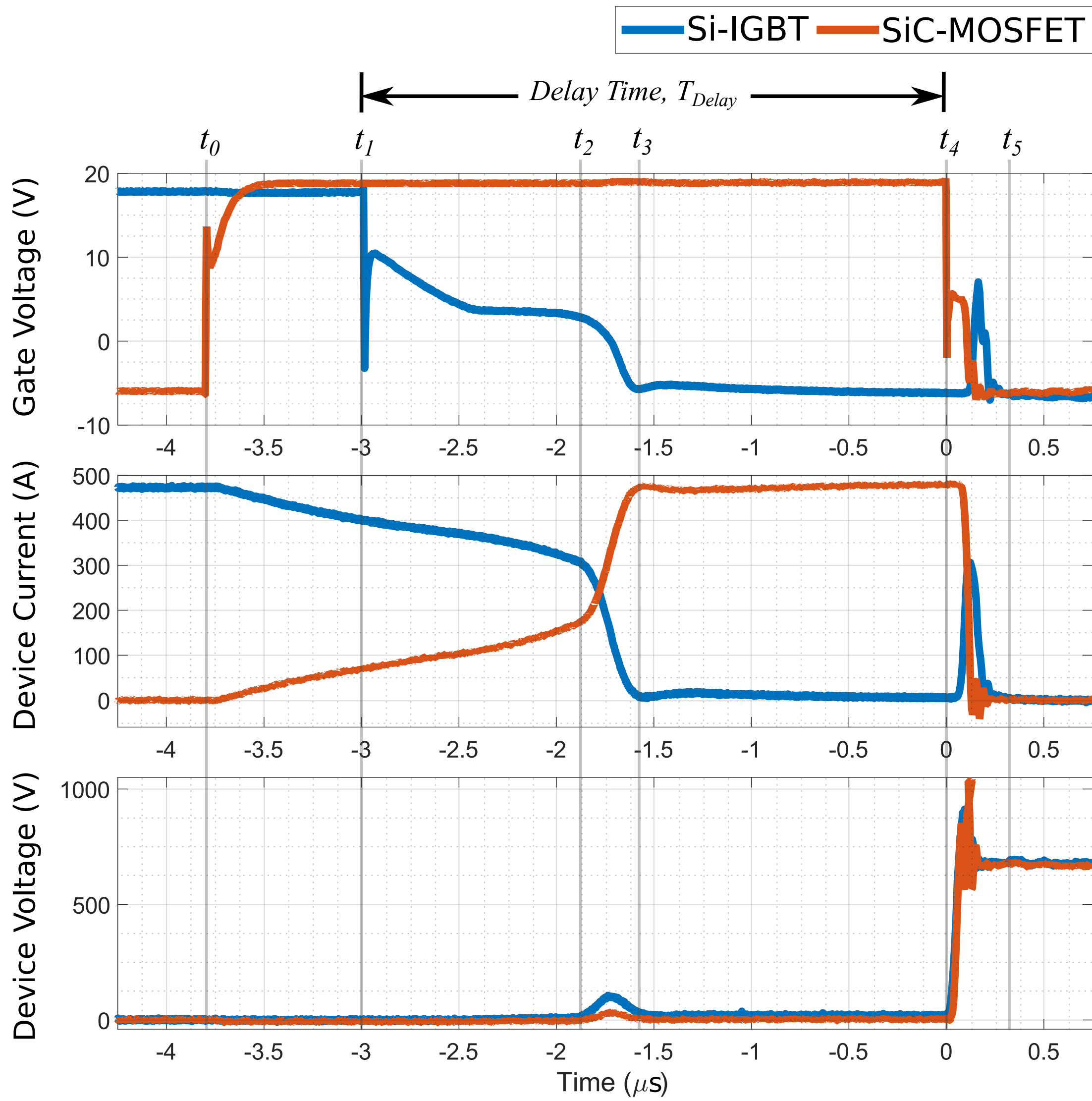
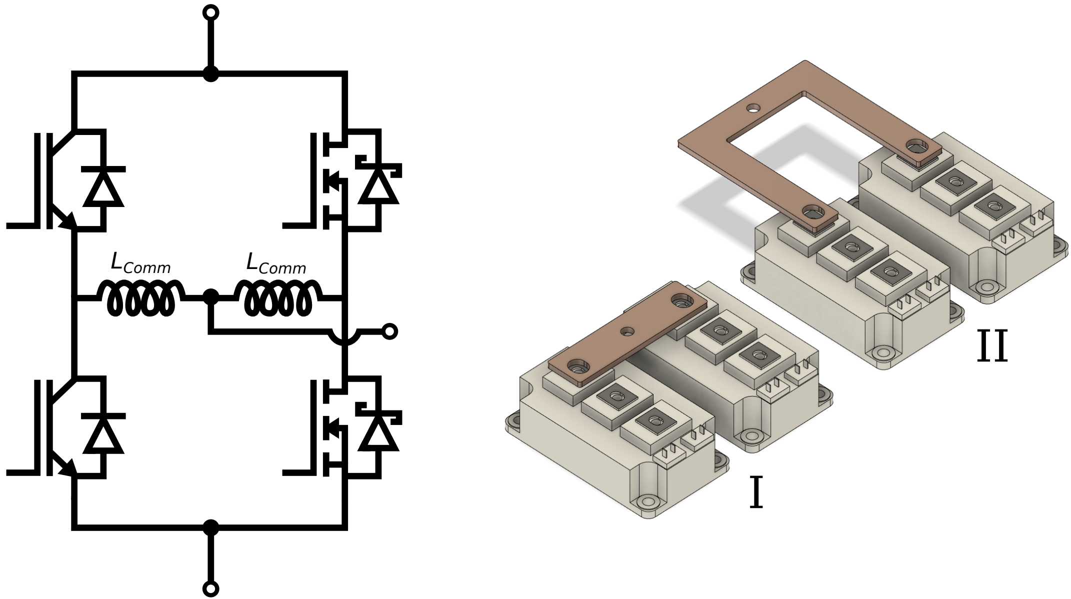


Figure 5.3: Experimental waveforms of Si/SiC-Diverter, $T_{Delay} = 3\ \mu$s. Tested at 480 A, 700 V with device baseplate set to 100 °C.

5.3.1 Current Commutation from IGBT to MOSFET

As shown in the experimental waveforms in Figure 5.3, a voltage perturbation occurs during periods $t_2 \rightarrow t_3$. As previously mentioned, this is due to the large dI/dt which happens after the Si-IGBT fully turns off and all of the load current flows into the SiC-MOSFET. As the device is turned on during this period, hence conducting, any voltage across either device results in power dissipation,



(a) Diverter half-bridge showing L_{Comm}.

(b) Render of L_{Comm}, standard link (I) and exaggerated link (II).

Figure 5.4: Inter-device stray inductance (L_{Comm}).

resulting in an energy loss (E_{Comm}). The inter-device stray inductance L_{Comm} is illustrated in Figure 5.4a. This arises from using individual power modules and is made up of internal module inductance and the link between them (shown in Figure 5.4bI).

The calculation for E_{Comm} is shown in (5.2). A MATLAB script was written to detect t_2 and t_3, the conditions being $t_2 : V_{ds} > 5$ V and $t_3 : V_{ds} < 5$ V.

$$E_{Comm} = \int_{t_2}^{t_3} V_{ds} I_d + V_{ce} I_c \, dt \qquad [\mathrm{J}] \tag{5.2}$$

To understand the impact of L_{Comm} on the commutation, the copper link which connects both devices and acts as the Midpoint (MP) connection was replaced with an exaggerated link (shown in Figure 5.4bII). The standard link has an inductance of ~ 40 nH and the exaggerated link is ~ 100 nH. One set of measurements from this test are shown in Figure 5.5. It can be seen that the peak

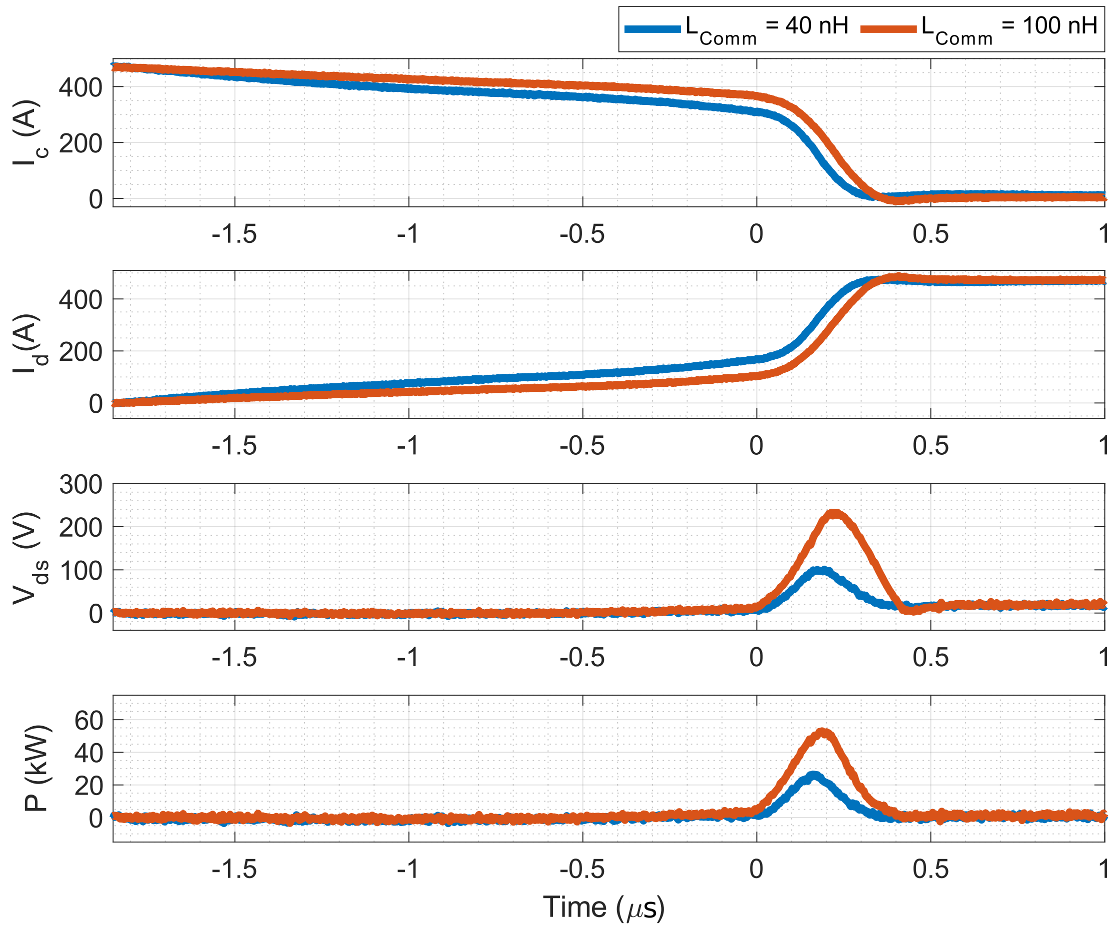


Figure 5.5: Experimental waveforms of Si/SiC-Diverter showing the impact of L_{Comm}. Tested at 480 A, 700 V with device baseplate set to 100 °C.

voltage perturbation for the standard link is 100 V, however for the exaggerated link there is a substantial increase to a peak of 230 V. This results in a peak instantaneous power dissipation of 25 kW and 53 kW, respectively.

The E_{Comm} associated with this perturbation, for all of the current set points tested at, is shown in Figures 5.6. At 120 A this is almost negligible which is most likely why this has never been properly shown in previous publications as they have all investigated this area at < 100 A. A line of $^1/_2 LI^2$ for both inductance values has been added to the plot which closely aligns with the measured data points, showing that E_{Comm} follows a square law. It is evident that the increase in parasitic inductance results in a higher level of loss. The data points shown in Figure 5.6 are with the device baseplate set to 100 °C, however the results are

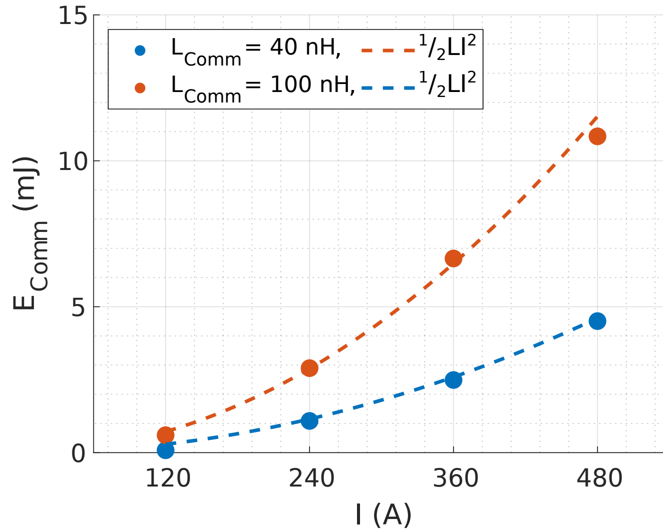


Figure 5.6: Measured E_{Comm} of Si/SiC-Diverter at two values of L_{Comm}. Tested at 700 V with device baseplate set to 100 °C.

near identical for 25 °C, 75 °C and 125 °C — demonstrating that temperature has no discernible impact on E_{Comm}.

In an effort to reduce the effect of L_{Comm}, the time period before the Si-IGBT turns off ($t_0 \rightarrow t_1$) was increased in order to allow the current (I_c) to reach a lower value before it is rapidly commutated between the devices. The waveforms for which are shown in Figure 5.7. It can be seen that I_c reaches a marginally lower level (thus higher level for I_d) as this time increases, however the ratio of the current in each device is determined by the effective on-state resistance of each device once in steady-state. There is a very small reduction in voltage perturbation as this time period was increased, however it can be considered as insignificant. No significant reduction was achieved as the mechanism resulting in the voltage perturbation is due to the dI/dt and not simply the current magnitude. Using a higher turn-off gate resistance for the Si-IGBT was investigated. The outcome of this being a decrease in the turn-off speed of the IGBT (period $t_1 \rightarrow t_2$), however no impact on the dI/dt during period $t_2 \rightarrow t_3$ — thus no reduction in E_{Comm}.

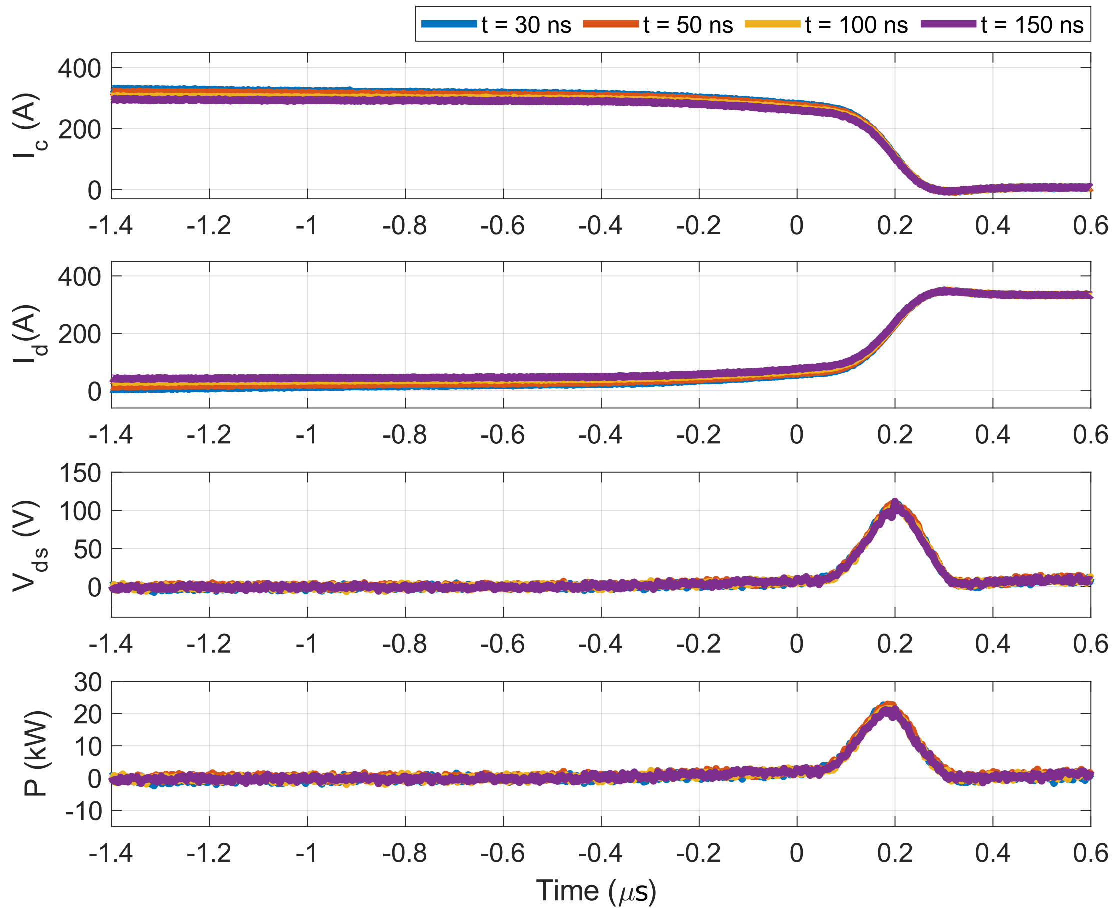


Figure 5.7: Experimental waveforms of Si/SiC-Diverter, varying time of $t_0 \rightarrow t_1$. Tested at 480 A, 700 V with device baseplate set to 100 °C.

The impact of E_{Comm} in terms of the overall $E_{Div,Off}$ will be further discussed in Section 5.3.4.

5.3.2 MOSFET Conduction Period

As the objective of the Diverter is to use a partially rated SiC-MOSFET, with a subsequently smaller die area, the forward characteristics are poorer than that of the Si-IGBT. Therefore, during periods $t_0 \rightarrow t_4$, the current in the SiC-MOSFET (I_d) is flowing through a higher resistance path than it would have been if it was just in the Si-IGBT. This results in an increased conduction loss during this period which needs to be attributed to the switching loss of the Diverter. This

additional energy loss ($E_{AddCond}$) is expressed in (5.3)

$$\begin{aligned} E_{AddCond} &= \int_{t_0}^{t_4} \left(P_{MOSFET} + P_{IGBT} - P_{IGBT,nominal}\right) dt \quad [\mathrm{J}] \\ &= \int_{t_0}^{t_4} \left({I_d}^2 R_{ds(on)} + I_c V_{ce(sat)} - I_{nom} V_{ce(sat)}\right) dt \quad [\mathrm{J}] \end{aligned} \tag{5.3}$$

where: $R_{ds(on)}$ is the MOSFET on-state resistance taken from the datasheet [152]; $V_{ce(sat)}$ is the forward voltage drop of the IGBT taken from the datasheet [168]; and I_{nom} is the nominal current that the IGBT would be conducting if it were not in the Diverter configuration, i.e. a continued straight line on I_c from $t_0 \rightarrow t_4$. $R_{ds(on)}$ and $V_{ce(sat)}$ were digitised from the datasheet curves and implemented as look-up tables in a MATLAB script. The largest contribution to $E_{AddCond}$ are the ${I_d}^2 R_{ds(on)}$ losses, which linearly increase with T_{Delay}. Using a SiC-MOSFET with a large die area would clearly reduce this, however that is in contrast to the goal of the Diverter. The penalty of $E_{AddCond}$ will be assessed in Section 5.3.4.

5.3.3 Turn-Off Event

5.3.3.1 Switching Loss

The calculation for the energy loss during the actual switching event (E_{Switch}) is shown in (5.4)

$$E_{Switch} = \int_{t_4}^{t_5} V_{ds} I_d + V_{ce} I_c \, dt \quad [\mathrm{J}] \tag{5.4}$$

At the end of the T_{Delay} period is where the SiC-MOSFET turn-off transition

happens (during period $t_4 \rightarrow t_5$). It can be seen in Figures 5.3 and 5.8 that a fast dV/dt turn-off is achieved along with a fast dI_d/dt. There is, however, a brief rise (or reconduction) of the IGBT current. This is due to the minority carriers with the CSR which have not yet been swept out. This characteristic contributes to the switching loss.

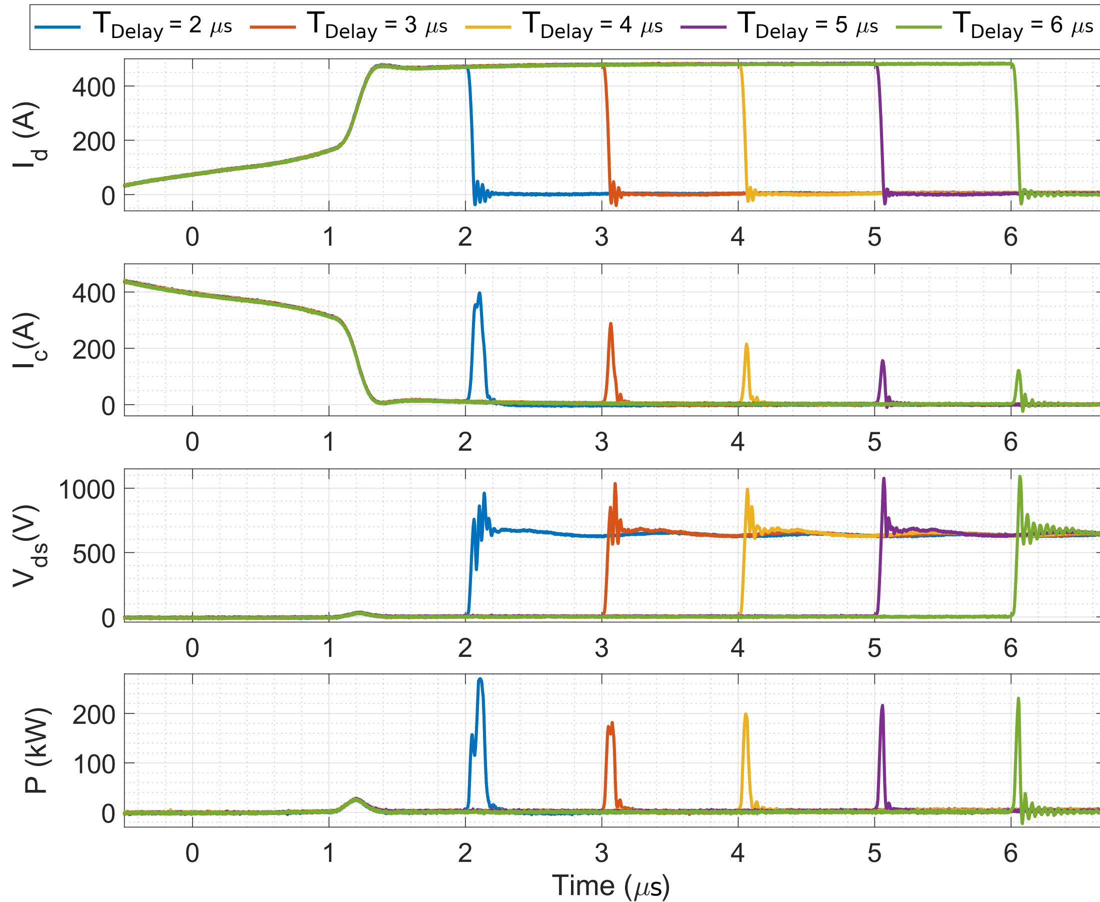


Figure 5.8: Experimental waveforms of Si/SiC-Diverter, varying T_{Delay} to show IGBT reconduction. Tested at 480 A, 700 V with device baseplate set to 100 °C.

5.3.3.2 IGBT Reconduction Current

The main purpose of the T_{Delay} period is to allow any excess minority carriers that are still in the Si-IGBTs CSR to recombine in order to avoid the traditional tail current. When the SiC-MOSFET turns off and the voltage is reapplied across the Diverter, minority carriers that are still in the Si-IGBTs CSR begin to conduct

causing the device to briefly turn back on. Figure 5.8 shows a sample of the experimental results where T_{Delay} is varied from 2–6 μs. It can be observed that the amount of reconduction current (I_c) reduces as T_{Delay} is increased. This is due to the increased hole injection from the IGBT collector region. It can be seen empirically from the instantaneous power plot that E_{Switch}, i.e. the area under the power triangle, also decreases as a result of an increase in T_{Delay} (due to the reduced amount of reconduction of I_c). The peak of that power triangle does, however, increase with T_{Delay}. This is due to an increased voltage overshoot present on V_{ds} — this will be further discussed in Section 5.4.

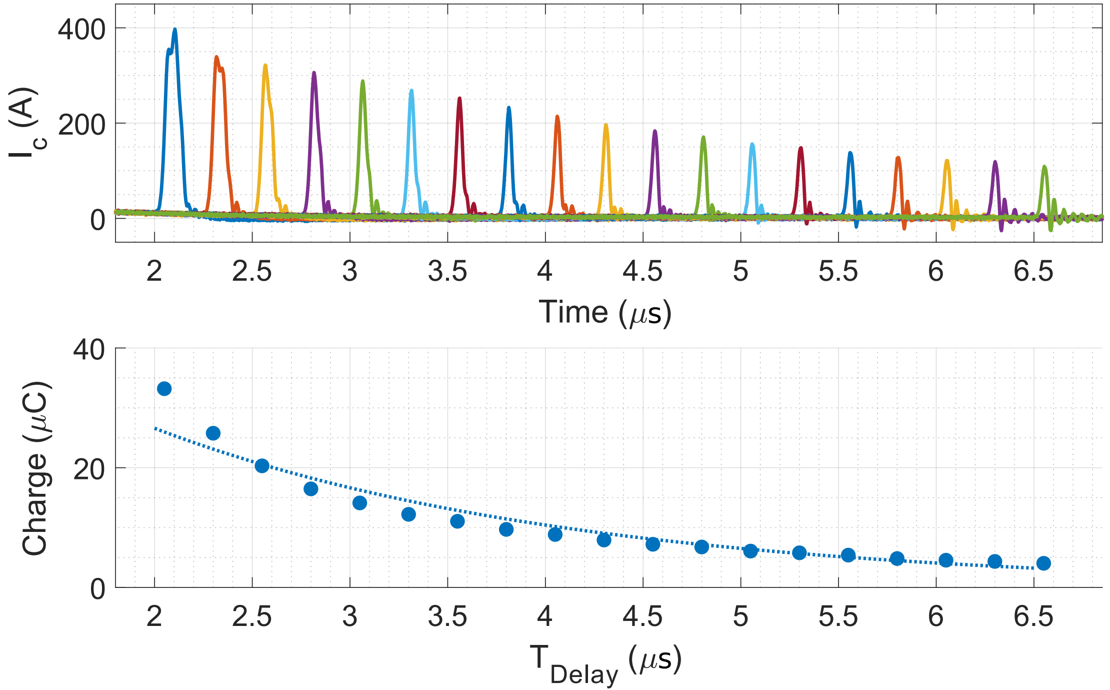


Figure 5.9: Si-IGBT reconduction current analysis. Top: reconduction current. Bottom: charge analysis. Tested at 480 A, 700 V with device baseplate set to 100 °C.

The excess minority carrier decay can be quantified by the instantaneous charge (Q) in the CSR [225]. This can be expressed as (5.5)

$$\frac{dQ}{dt} = -\frac{Q}{\tau_{HL}} \quad [\text{C/s}] \tag{5.5}$$

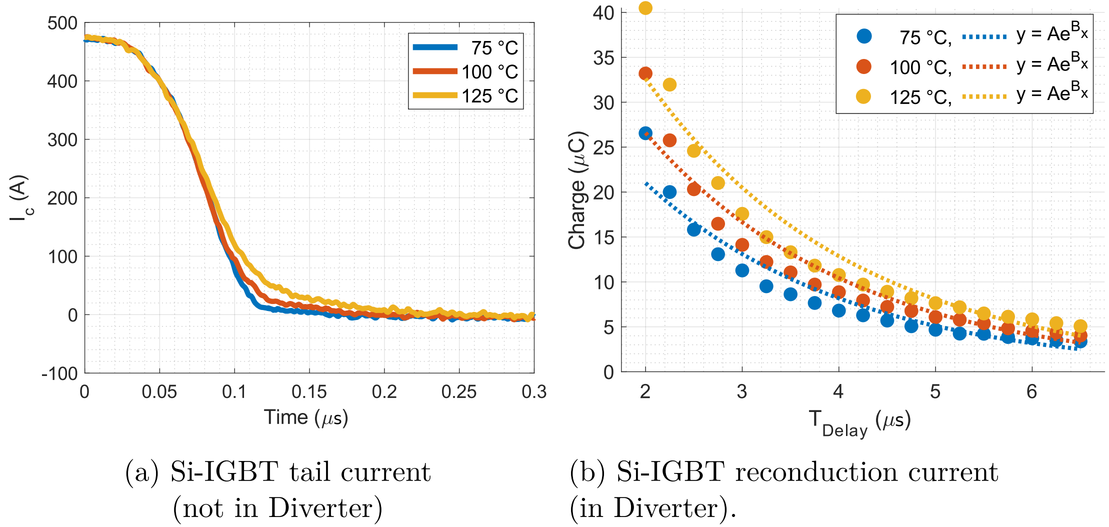
where: τ_{HL} is the high-level lifetime constant. Equation (5.5) can be further derived to show the exponential decay of Q [226], as expressed in (5.6)

$$Q = Q_0 e^{-\frac{t}{\tau_{HL}}} \quad [\mathrm{C}] \tag{5.6}$$

The top plot in Figure 5.9 shows the reconduction of I_c for the full data set of T_{Delay}. By integrating these current pulses, the amount of charge can be determined – a plot of which is shown in the bottom of Figure 5.9. The curve fitting tool in MATLAB was used to add an exponential trend line (blue dashed line, $y = Ae^{Bx}$) to this data [216], i.e. in the same manner as equations (5.6).

The rate of recombination of minority carriers becomes slower when a Si-IGBT die is at a higher temperature [227]. This is confirmed experimentally in Figure 5.10a, where the Si-IGBT used in the Diverter (FF450R12KT4 [168]) is tested on its own to show the temperature effect on the tail current properties. It can be seen that the difference, in terms of slower dI_c/dt during the tailing period, between 100–125 °C is greater than the difference between 75–100 °C. This can also be inferred from the temperature dependant switching loss curves (I_c vs. E_{off}) on page 5 of the datasheet [168].

Using the previous curve fitting technique with Equation (5.6), the impact that temperature has on the recombination, and hence the reconduction of I_c for the Diverter, is shown (Figure 5.10b). As expected an increase temperature results in a larger required T_{Delay}. The coefficients for the fitted curves are shown in Table 5.2. The high-level lifetime constant (τ_{HL}) for each temperature is also shown.



(a) Si-IGBT tail current (not in Diverter)

(b) Si-IGBT reconduction current (in Diverter).

Figure 5.10: Effect of temperature on recombination rate of minority carriers.

	A	**B**	τ_{HL}
75 °C	5.398×10^{-5}	-4.719×10^{5}	2.11 μs
100 °C	6.78×10^{-5}	-4.68×10^{5}	2.13 μs
125 °C	8.277×10^{-5}	-4.654×10^{5}	2.15 μs

Table 5.2: Curve fitting exponent coefficients.

5.3.4 Overall Turn-Off Switching Loss

A breakdown of $E_{Div,Off}$ against T_{Delay} for each current set point at 100 °C is shown in Figure 5.11. This is compared to the E_{Off} for the Si-IGBT (purple line, FF450R12KT4 [168]) and fully rated SiC-MOSFET (green line, BSM600D12P3G001 [144]). As previously mentioned, the full turn-off switching loss $E_{Div,Off}$ for the Diverter consists of: the commutation loss E_{Comm} resulting from L_{Comm} (red portion of bar); the additional conduction loss penalty $E_{AddCond}$ (yellow portion of bar); and the energy dissipated during the actual switching transient E_{Switch} (blue portion of bar) — as defined in Equation (5.1).

For each current magnitude, it can be seen that E_{Switch} of the Diverter decreases, as T_{Delay} is increased, to a lower level than that of the fully rated SiC-MOSFET [168] from ROHM. This is due to the smaller die area, hence lower

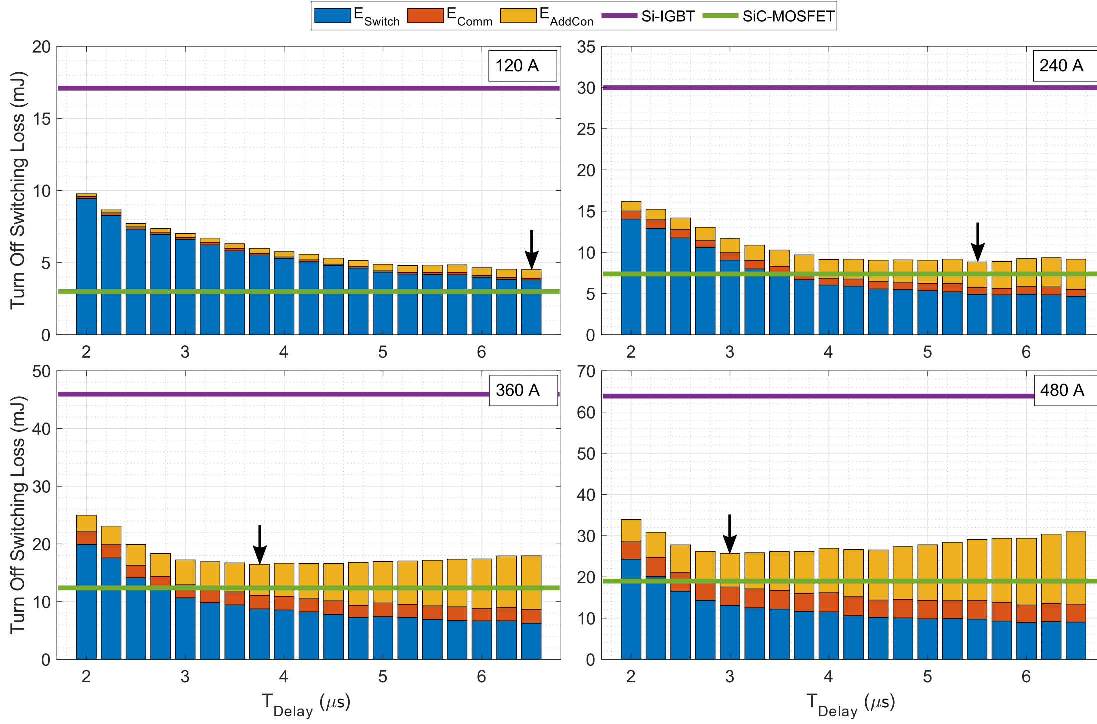
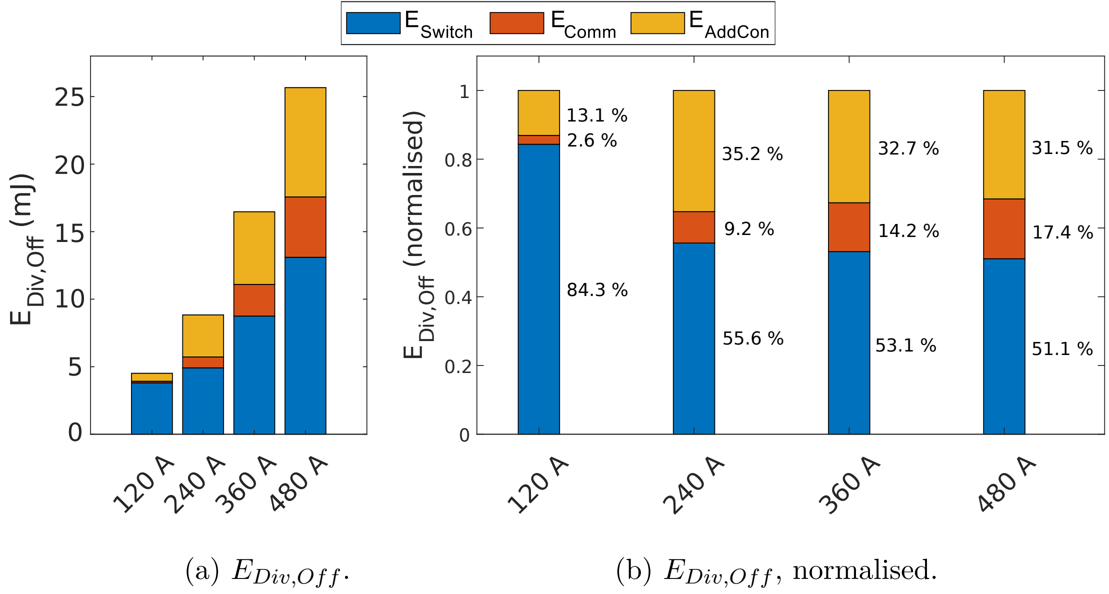


Figure 5.11: Breakdown of Si/SiC-Diverter $E_{Div,Off}$ with respect to T_{Delay}, compared to the E_{Off} for the Si-IGBT (FF450R12KT4 [168]) and SiC-MOSFET (BSM600D12P3G001 [144]). Tested at 700 V with device baseplate set to 100 °C.

capacitances, of the SiC-MOSFET used in the Diverter. However, when the contributions from E_{Comm} and $E_{AddCond}$ are considered, the total loss is marginally higher. The resultant T_{Delay} value, for minimum switching loss, can be inferred and is marked on each plot with an arrow (↓). These minima are also shown in Figure 5.12 — as the raw energy values (5.12a) and normalised (5.12a) to show the percentage of E_{Switch}, E_{Comm}, and $E_{AddCond}$.

When considering the 120 A case, it is clear that E_{Comm} (red) and $E_{AddCond}$ (yellow) have minimal impact on $E_{Div,Off}$. At the point of minimum loss (T_{Delay} = 6.5 μs), the contribution from E_{Comm} and $E_{AddCond}$ are 2.6 % and 13.1 %, respectively, of the total $E_{Div,Off}$. Previous studies have operated in this power range where L_{Comm} has little to no effect. As discussed in Section 5.3.1, E_{Comm} follows an I^2 law and accordingly progressively becomes larger as current is increased. Notwithstanding this, E_{Comm} only represents 17.4 % of the loss at 480 A. At



(a) $E_{Div,Off}$.

(b) $E_{Div,Off}$, normalised.

Figure 5.12: Minimum $E_{Div,Off}$ for each current set point. Tested at 700 V with device baseplate set to 100 °C. T_{Delay} = 6.50 μs (120 A), 5.50 μs (240 A), 3.75 μs (360 A), & 3.00 μs (480 A).

240–480 A, $E_{AddCond}$ makes up a considerable amount of the loss. This can be empirically seen in the full breakdown plots (Figure 5.11) where clear inflection points appear for $E_{Div,Off}$ due to the rapid increase in $E_{AddCond}$. As shown in Figure 5.12a, this additional conduction loss penalty represents 31.5–35.2 % percent of the loss — this is when the SiC-MOSFETs nominal current rating is exceeded. Despite this, the Diverter achieves a large reduction in turn-off loss compared to the Si-IGBT used — this is in the region of a 60–74 % at 100 °C.

Figure 5.13 shows the temperature dependency of T_{Delay}, with the minimum $E_{Div,Off}$ points marked by a purple star. These T_{Delay} values are listed in Table 5.3. The required delay times are the same for 75 °C and 100 °C — however, if a smaller step size (< 250 ns) was used, this may not be the case. Excluding the 120 A case, an additional 250 ns is required when at 125 °C. This is a result of the slower recombination rate of the minority carriers when a Si-IGBT die is at a higher temperature, as discussed in Section 5.3.3.2.

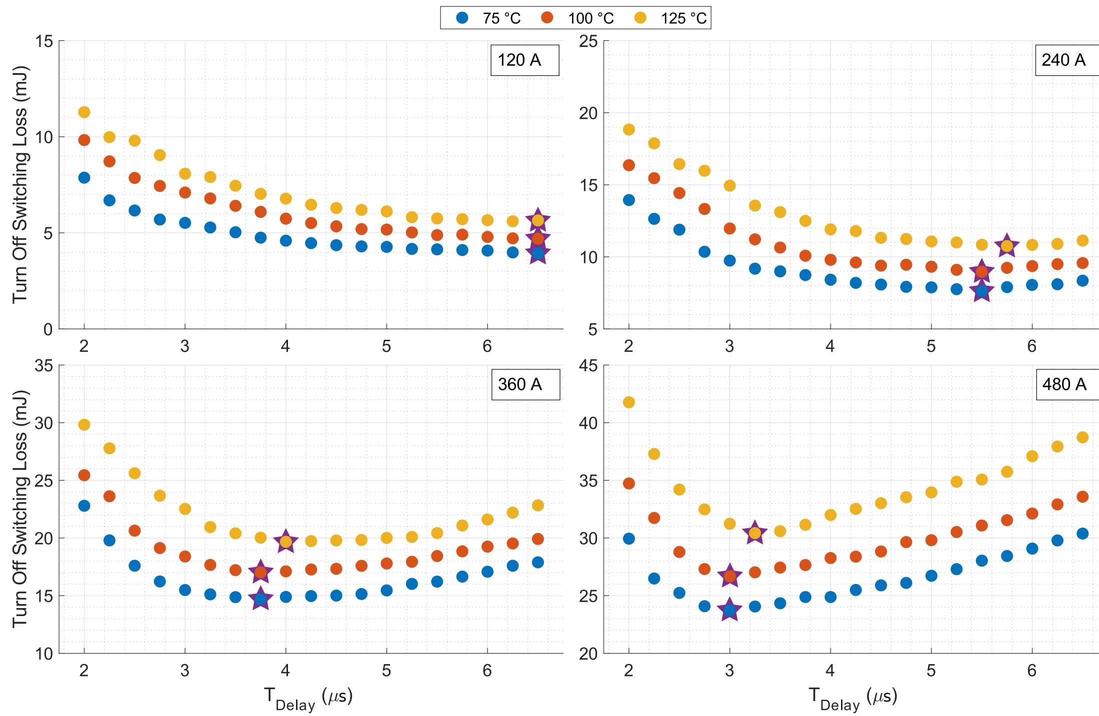


Figure 5.13: Si/SiC-Diverter $E_{Div,Off}$ against T_{Delay}, varying device temperature. Tested at 700 V.

	120 A	240 A	360 A	480 A
75 °C	6.50 μs	5.50 μs	3.75 μs	3.00 μs
100 °C	6.50 μs	5.50 μs	3.75 μs	3.00 μs
125 °C	6.50 μs	5.75 μs	4.00 μs	3.25 μs

Table 5.3: T_{Delay} for minimum overall turn-off loss.

5.4 Diverter: Further Analysis on Turn-Off

5.4.1 Influence of Parallel Connected SiC-MOSFET on Si-IGBT Turn-On Behaviour

Whilst the main Diverter operation is with regard to the turn-off operation, the affect that the parallel connected SiC-MOSFET has on the Si-IGBT must be investigated. This comprises an additional capacitance across the IGBT (from

the MOSFETs C_{oss}) and some form of additional anti-parallel diode (from either the additional Freewheeling Diode (FWD) and/or the MOSFETs body diode). Figure 5.14 shows turn-on waveforms for the Si-IGBT with (solid line) and without (dashed line) the SiC-MOSFET physically connected, at the four different current magnitudes.

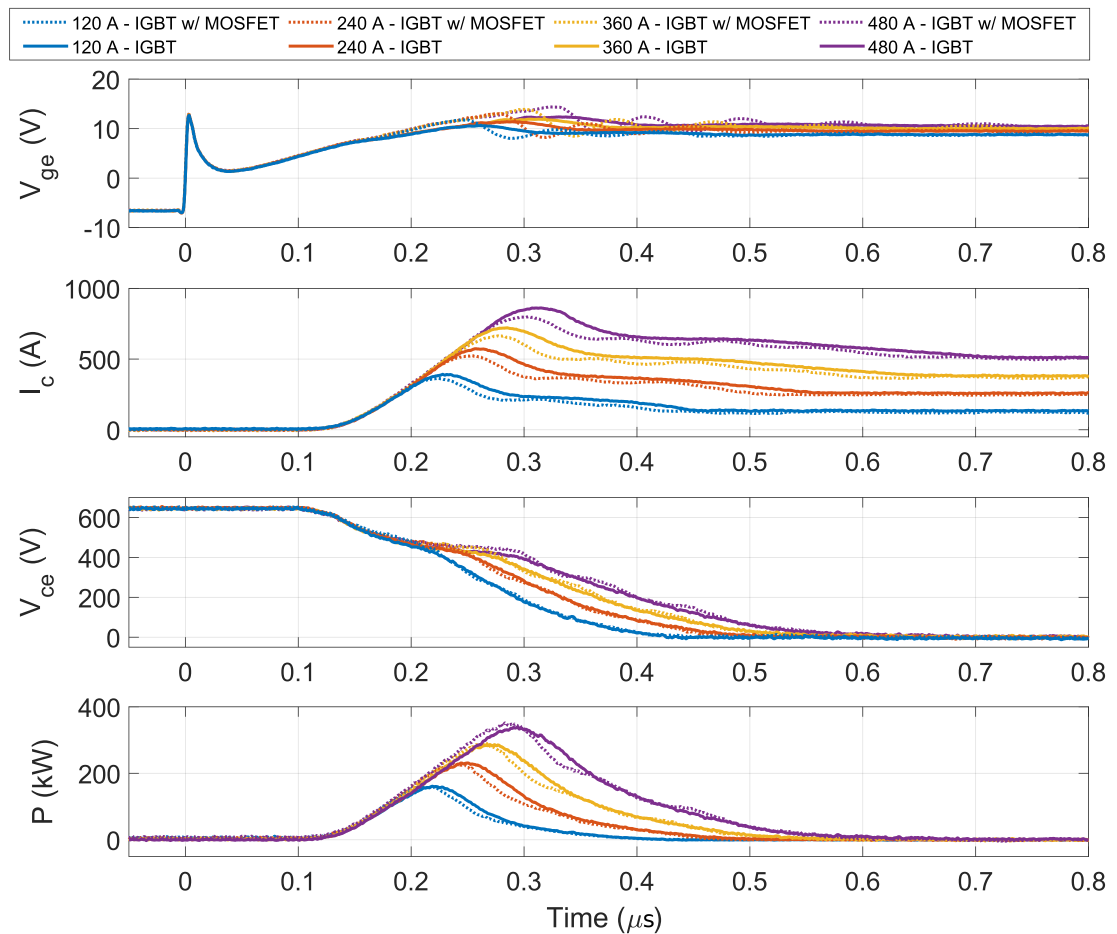


Figure 5.14: Experimental waveforms of Si/SiC-Diverter at turn-on. Tested at 700 V with device baseplate set to 100 °C.

The most apparent impact is in the I_c plot, where a reduction in current overshoot — a result of the reverse recovery from upper device — can be observed when the SiC-MOSFET is connected. This is due to the SiC-MOSFETs FWD, which conducts a proportion of the current, being a close to zero reverse

recovery (Z-Rec®) Merged PIN Schottky (MPS) diode. However, a small amount of oscillatory behaviour is present which is typical with SiC-MPS diodes [228]. Datasheet curves for the FWDs forward characteristics of the Si-IGBT [168] and SiC-MOSFET [152] were extracted to determine the current sharing under steady-state conditions. The ratio of the forward voltage drop aligns with the effective current rating ratio of the device (4:1), therefore, in steady-state conditions current should not exceed device ratings. As the SiC-MPS diode has a faster transient speed than the Si-Fast Recovery Diode (FRD) [228], for a small period of time the SiC diode will conduct all of the current. However, a SPICE simulation using generic Si-FRD and SiC-MPS diodes has shown that this time period is < 5 ns. The effect of the additional capacitance across the Si-IGBT is more subtle. It causes a marginally slower voltage collapse and results in a miller plateau that is at a slightly higher level. Analysing the voltage waveforms also shows that the oscillations in I_c are somewhat reflected in V_{ce}.

To understand the overall impact, the turn-on switching energy (E_{on}) was calculated across the current and temperature range. E_{on} was calculated using the method described in Section 3.7.2. Using the calculated values for E_{on}, both with and without the SiC-MOSFET, a ΔE_{on} for each set point was calculated. This can then be expressed as a relative change $\Delta E_{on}(\%)$, as shown in in (5.7)

$$\Delta E_{on}(\%) = \frac{E_{on,+MOSFET} - E_{on}}{E_{on}} \cdot 100 \qquad [\%] \tag{5.7}$$

	75 °C	100 °C	125 °C
120 A	+2.2 %	-1.5 %	-1.6 %
240 A	+3.8 %	-1.4 %	-1.4 %
360 A	+5.2 %	-1.2 %	-1.3 %
480 A	+6.7 %	+3.8 %	+2.5 %

Table 5.4: $\Delta E_{on}(\%)$ for different currents and temperatures, showing impact of parallel connected SiC-MOSFET on Si-IGBT turn-on. Positive number represents additional loss, negative number represents less loss.

Table 5.4 shows $\Delta E_{on}(\%)$ for the full range of set points. At 75 °C, across the full power range, there is additional loss (2.2–6.7 %) due to the SiC-MOSFET. When operating at 480 A, it appears that there is always an additional loss, however this decreases as temperature increases — this is most likely to do with how the SiC-MPS diode behaves at higher temperatures. An interesting observation is that at 100–125 °C and 120–360 A, there is a reduction in E_{on} of $\sim$ 1.5 %. It it suspected that this is due to the temperature effect on the switching speed of the bipolar Si-FRD device. Overall, it can be stated that there is marginal negative impact from the SiC-MOSFET, although this largely depends on the operating temperature.

5.4.2 Naturally Damped Oscillations and Overshoot

An intriguing observation that has been made whilst investigating the Diverter is a T_{Delay} dependant damping phenomenon. As discussed in previous chapters, switching devices — particularly SiC-MOSFETs — experience a considerable amount of oscillatory behaviour and voltage overshoot. Techniques can be employed to manage this, however the Diverter offers a unique mechanism to naturally achieve damping at turn-off. This reduction in overshoot voltage and damping of oscillations can be seen in a previous plot (Figure 5.8), however the effect is more easily observed in Figure 5.15.

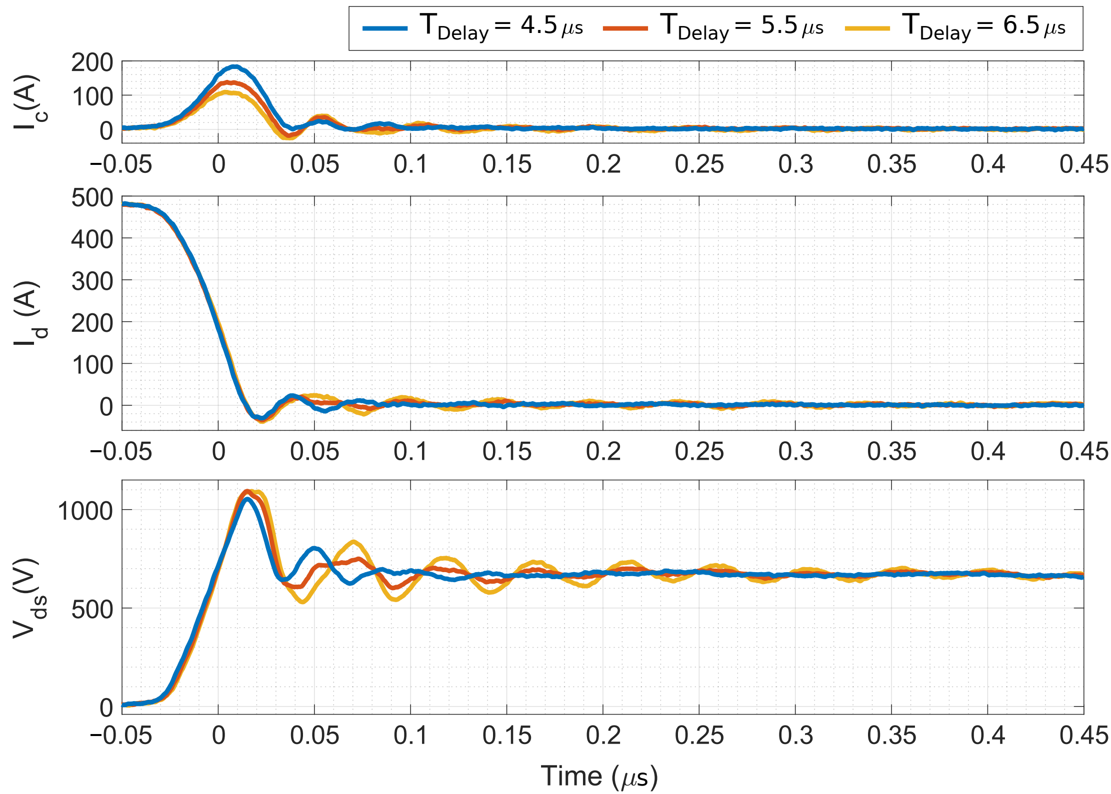


Figure 5.15: Experimental waveforms of Si/SiC-Diverter, showing damping of oscillatory behaviour and voltage overshoot. Tested at 480 A, 700 V with device baseplate set to 100 °C.

This effect is suspected to act in a similar way to that of a snubber network, where energy is removed from the resonant circuit that is formed during the switching operations. A snubber is designed to provide damping at a particular frequency (i.e. RC network tuned to have low impedance at certain frequencies, as discussed in Section 4.6.1), whereas the dynamic snubbering observed in the Diverter can be attributed to the reconduction of the Si-IGBT, which removes energy from the resonant circuit. It is shown in Figure 5.15 that the effectiveness of this is dependant on T_{Delay} or rather the magnitude of the reconduction of I_c that occurs. When T_{Delay} = 4.5 μs, an overshoot voltage of 1053 V (50.4 %) with no oscillations after 100 ns (t = 0 when V_{ds} > 700 V) can be seen. The reconduction of I_c reaches a peak current of 183 A (8.3 μC). For the T_{Delay} = 6.5 μs case, an overshoot of 1093 V (56.1 %) is observed with very underdamped oscillatory behaviour. The reconduction of I_c in this case only reaches a peak of

106 A with approximately half the associated charge (4.2 μC).

To asses the time dependency of T_{delay} for effective damping, the *stepinfo* [229] MATLAB function was used on V_{ds} for the full data set. Two of the characteristics were assessed: the "Settling Time" to quantify the oscillatory behaviour; and "Overshoot" to identify the percentage of voltage overshoot.

5.4.2.1 Oscillation Damping

The settling time is defined as from the start of the initial voltage rise to when the signal has settled to within ±2 % of the final steady-state value. The results of this are shown in Figure 5.16.

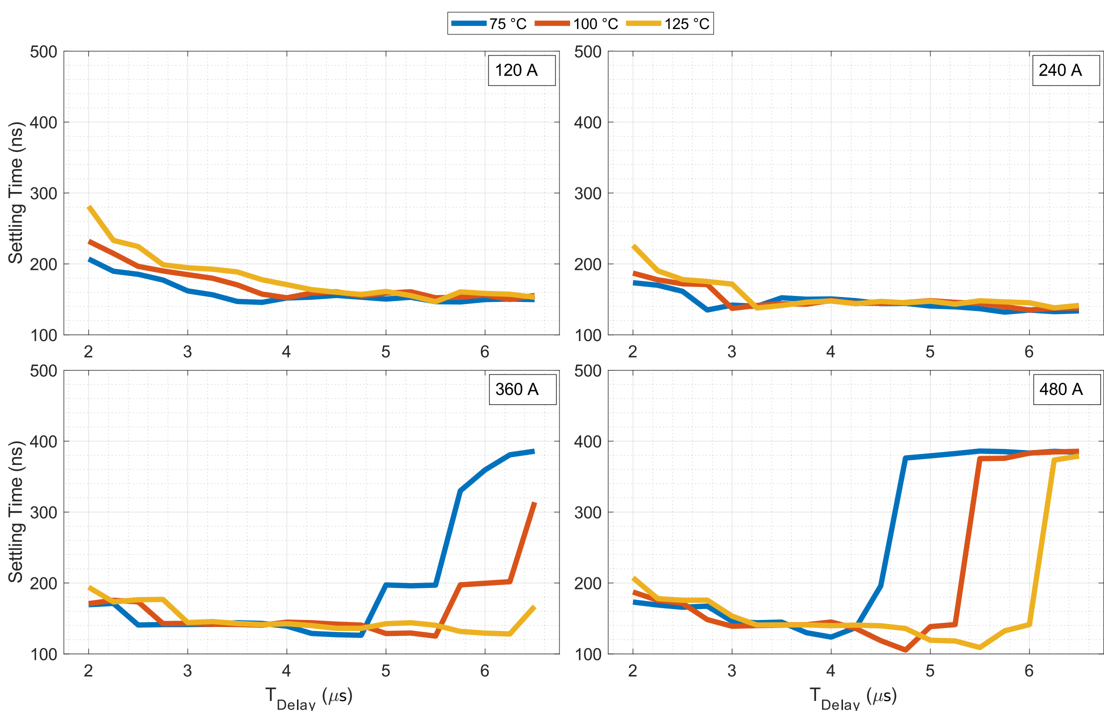


Figure 5.16: Si/SiC-Diverter settling time data from *stepinfo* function. Tested at 700 V.

Considering the data at 480 A (Figure 5.16), it can be seen that the settling time ramps up from ~140 ns to ~380 ns towards the end of the time series shown. The general trend exhibits a delay in time of ~ 1 μs as temperature is increased

from 75 °C to 100 °C and a further ∼ 1 μs from 100 °C to 125 °C. A similar trend is observed in the 360 A data. It is suspected that if T_{Delay} was extended to a value greater than 6.5 μs, the settling time would plateau in a similar manner to the 480 A plot. When tested at 120 A and 240 A, the oscillatory behaviour at turn-off is insubstantial due to significantly reduced energy when compared to the higher current set points. As can be seen in the corresponding plots in Figure 5.16, the settling time is at a similar level to the damped points of the higher current set points. To establish the sensitive temperature and T_{Delay} dependency of this damping phenomenon, the 480 A settling time curves are illustrated beside the charge analysis curves of the Si-IGBT reconduction current (as discussed in Section 5.3.3.2). These plots are shown in Figure 5.17 alongside the $E_{Div,Off}$ curves.

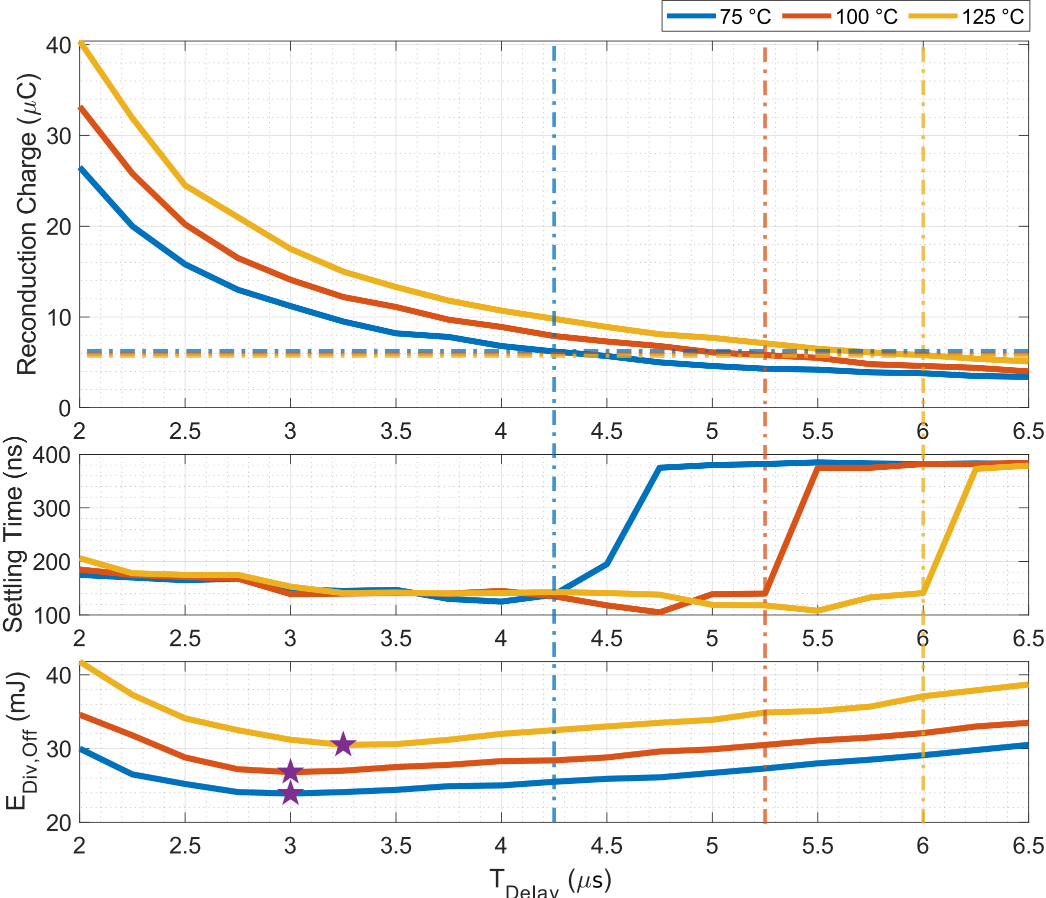


Figure 5.17: Si/SiC-Diverter settling time analysis. Tested at 480 A, 700 V.

Dashed marker lines have been added to the plots to determine this relationship — colour coordinated vertical lines at the point just before the rise in settling time and horizontal lines where these vertical lines intersect with the corresponding charge curve. As denoted by these markers, a minimum amount of reconduction can be determined. This point relates to ∼ 6 μC for the three temperatures. This is a 280–290 ns pulse with a peak current of ∼ 150 A which is delayed in time due to the temperature properties of the Si-IGBT minority carrier recombination process. The respective values of T_{Delay} that are marked clearly require a larger delay period than those for minimum $E_{Div,Off}$, however they can be considered as a maximum value as the T_{Delay} values preceding them all result in a good level of damping.

5.4.2.2 Voltage Overshoot Reduction

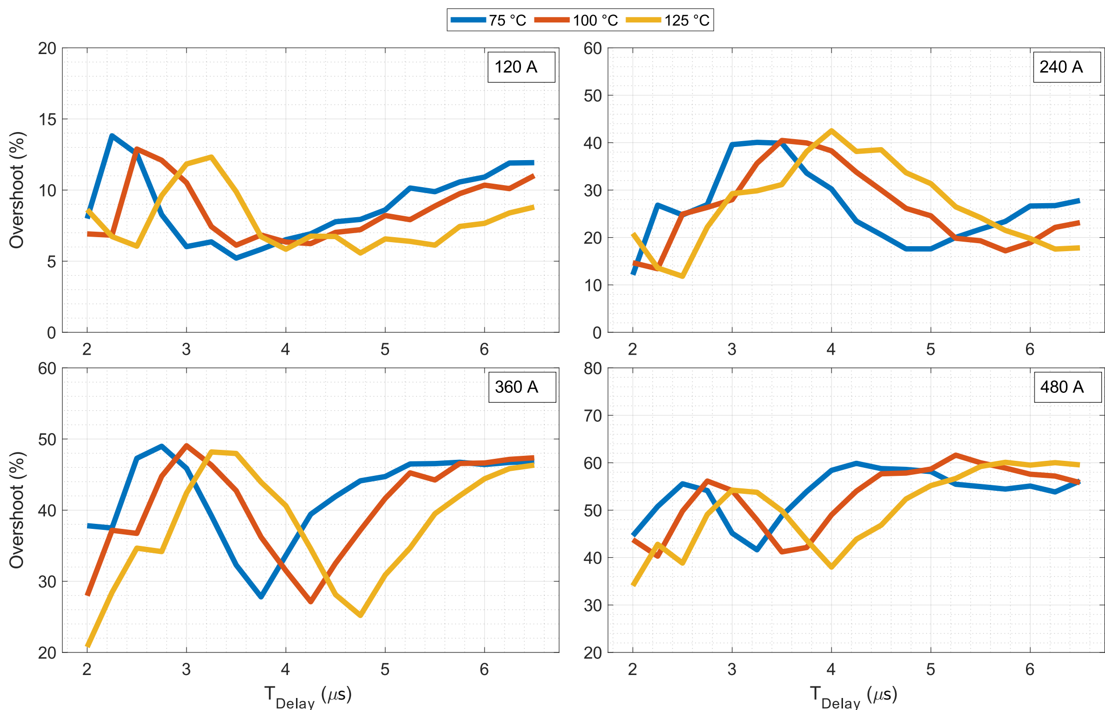


Figure 5.18: Si/SiC-Diverter overshoot data from *stepinfo* function. Tested at 700 V.

The voltage overshoot data is shown in Figure 5.18. The reductions in voltage

overshoot are significant, with a 20–30 % reduction being achieved. Similar to the settling time, a distinct temperature dependant trend can be identified in the overshoot analysis. However, here there is a definitive point of minimum voltage overshoot in each curve, rather than a wide range of values like was noted for the settling time.

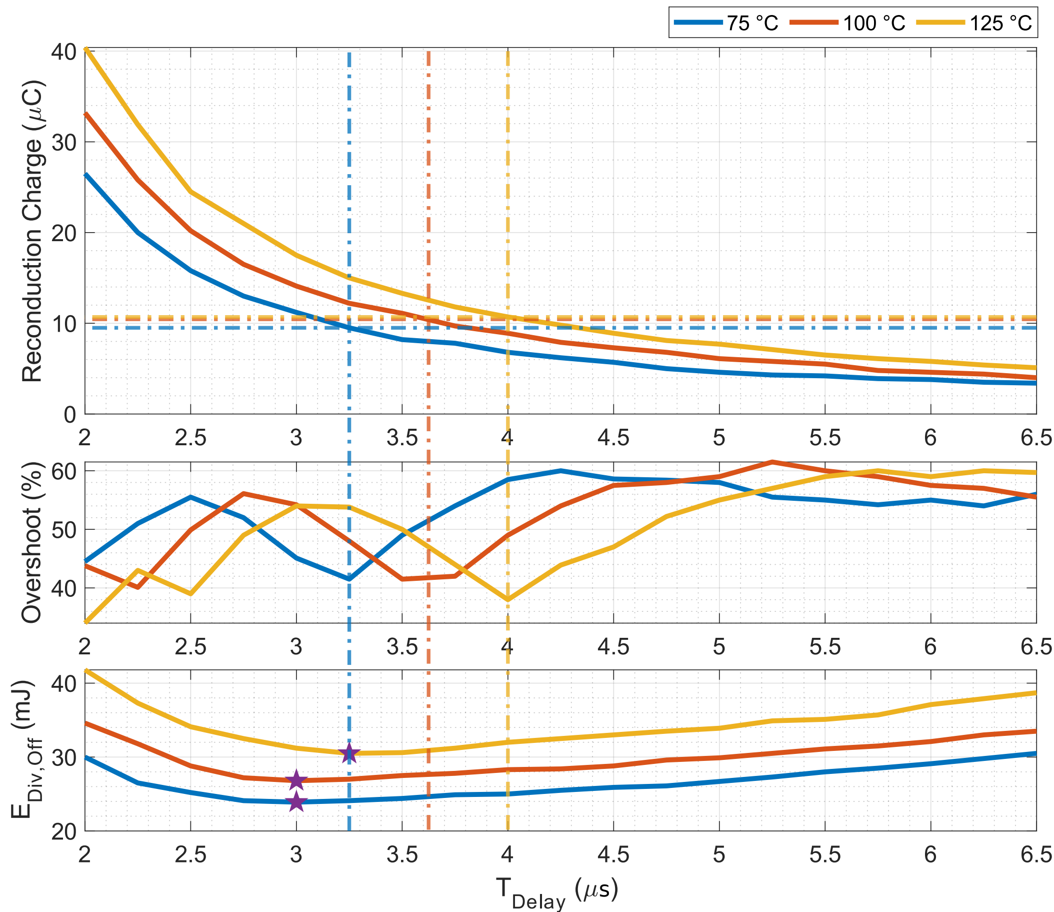


Figure 5.19: Si/SiC-Diverter overshoot analysis. Tested at 480 A, 700 V.

In a similar fashion to the settling time analysis above, Figure 5.19 shows how the minimum overshoot points correspond to the reconduction of I_c for the 480 A case. This plot would suggest that $\sim$ 10 μC — a 280–290 ns pulse with a peak current of $\sim$ 240 A — results in the lowest level of overshoot for each temperature. It can also be seen that the T_{Delay} value associated with minimum overshoot only requires an additional 0.25–0.75 μs of delay period than those for minimum $E_{Div,Off}$.

5.4.3 Relating Damping to Radiated EMI

To confirm whether or not the damping performance in Section 5.4.2 results in a perceptible difference in radiated EMI, the radiated emissions incident on the far-field EMC antenna were analysed. Figure 5.20 shows V_{ds} and a FFT of the radiated EMI at two value of T_{Delay}. The radiated emissions at 22.4 MHz — which are present in the undamped V_{ds} waveform ($T_{Delay} = 6.5\ \mu$s) and not present in the damped V_{ds} waveform ($T_{Delay} = 3\ \mu$s) — are shown to be significantly reduced. There is a reduction of approximately 35 dB. This confirms that this snubbering phenomenon does actually result in a reduction in radiated Radio Frequency (RF) emissions.

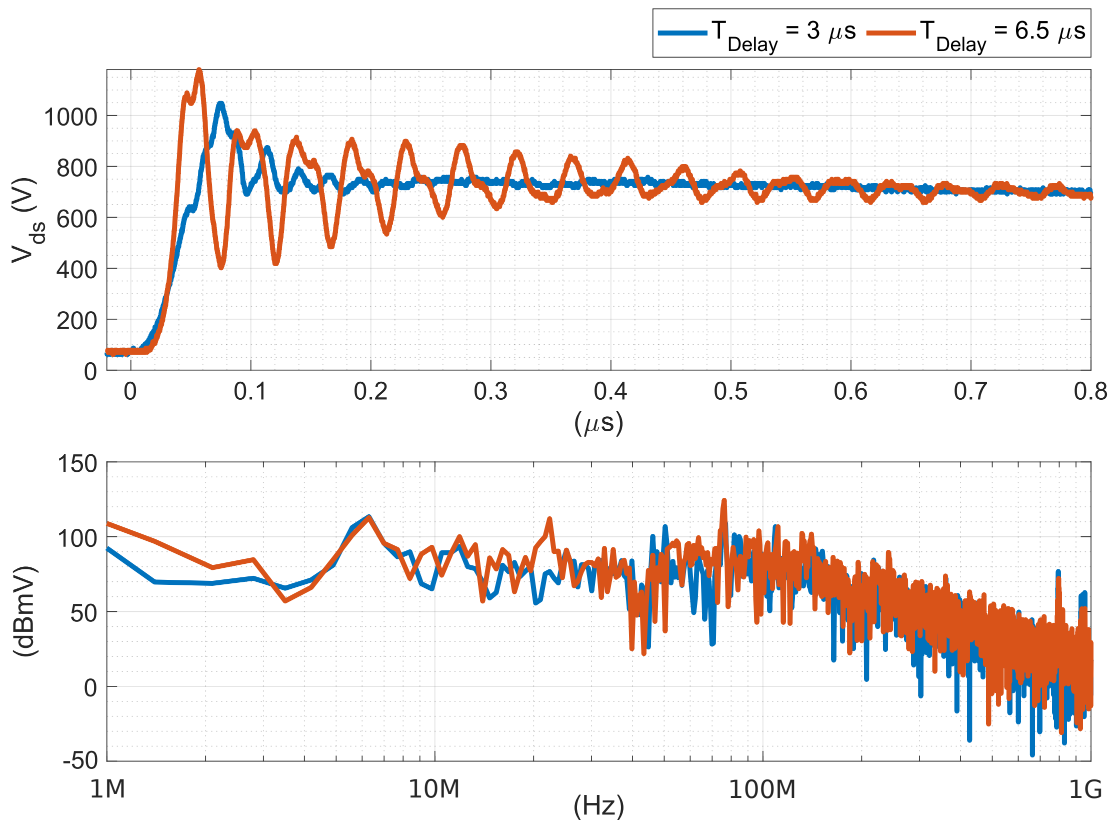


Figure 5.20: Experimental waveforms of Si/SiC-Diverter showing correlation of damping of oscillatory behaviour with radiated emissions. Tested at 480 A, 700 V with device baseplate set to 75 °C. Top: Device voltage (V_{ds}), bottom: Antenna measurement.

5.4.4 Delay Period for Minimum Switching Loss, Voltage Overshoot, and/or Oscillations

Depending on the desired performance traits — minimum turn-off loss, minimum voltage overshoot, maximum damping of oscillations, or a combination of all three — the T_{Delay} for the Diverter could be tuned accordingly.

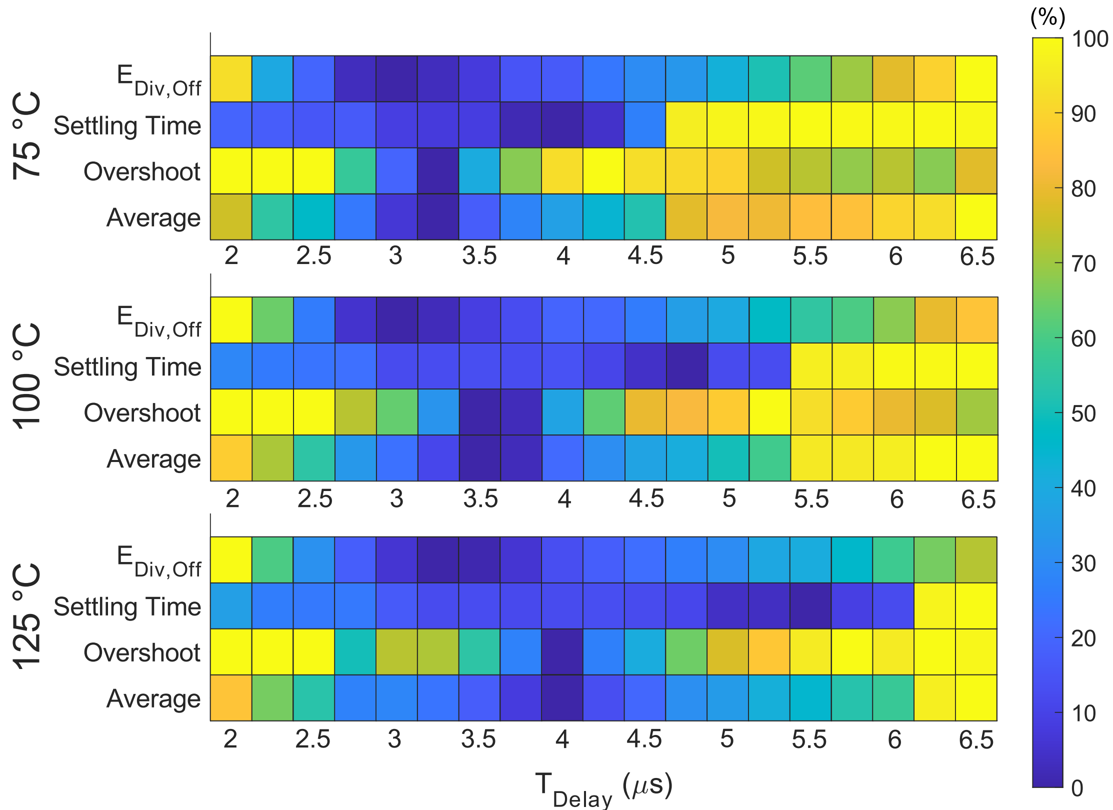


Figure 5.21: Heat map showing spread of best T_{Delay} in terms of minimum $E_{Div,Off}$, Settling Time, Overshoot, and an overall average. Tested at 480 A, 700 V.

Figure 5.21 shows a selection of heat maps for each performance trait at 480 A across the range of temperatures tested at. These have been normalised such that the maximum level is 100 % (yellow) and the minimum level is 0 % (blue) — i.e. the best in each case being 0 %. An average of the three is also given for each temperature to show the best possible T_{Delay} considering the three traits. In the case of the overshoot data, the first three data points (2–2.5 μs) have been negated

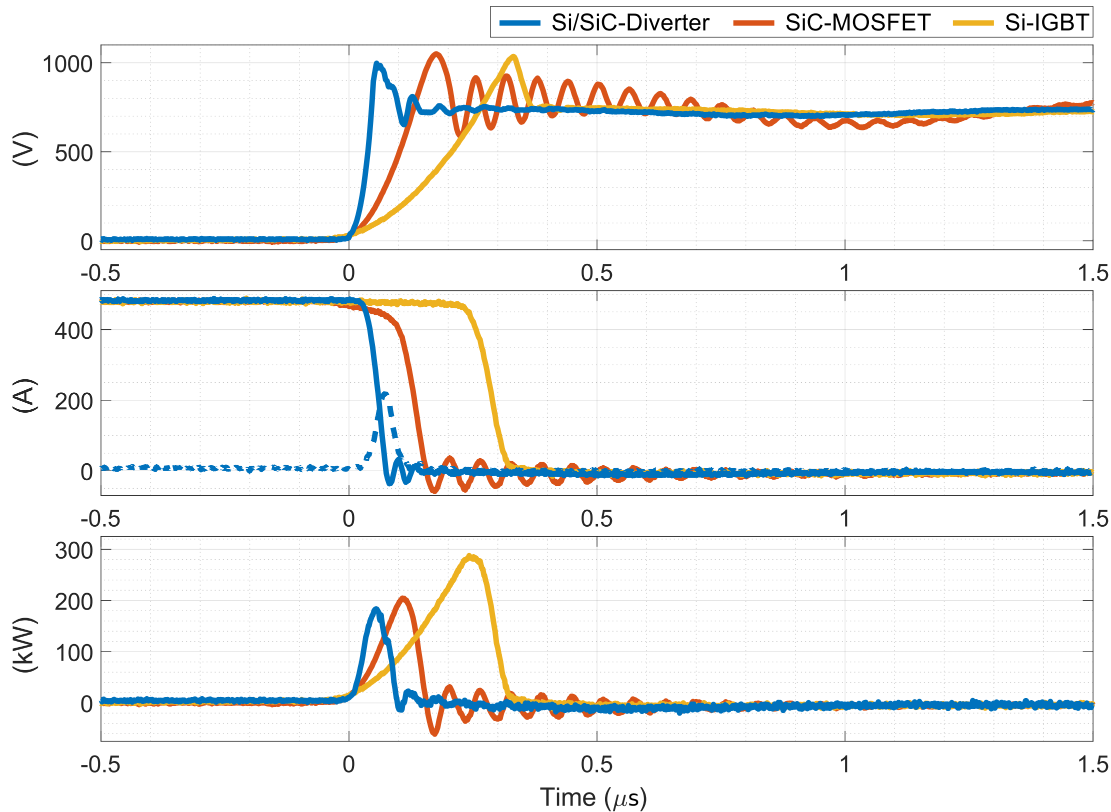
— i.e set to 100 % — to show only the desired window of delay period values. This is due to these shorter delay periods not aligning well with the marked troughs of the loss curves, as shown in Figure 5.19. The resultant prime T_{Delay} values are listed in Table 5.5. It can be seen that T_{Delay} values compatible with effective damping of oscillations correspond with those of low $E_{Div,Off}$. However, if the average values are selected (an additional 0.25–0.75 μs), the lowest level of overshoot can be realised, with a good level of damping of oscillations and only a marginal increase in energy loss.

	$E_{Div,Off}$	Settling Time	Voltage Overshoot	Average
75 °C	3.00 μs	$<$4.00 μs	3.25 μs	3.25 μs
100 °C	3.00 μs	$<$4.75 μs	3.50 μs	3.50 μs
125 °C	3.25 μs	$<$5.50 μs	4.00 μs	4.00 μs

Table 5.5: Best T_{Delay} for each performance trait.

5.5 Discussion: Si/SiC-Diverter vs. SiC-MOSFET vs. Si-IGBT

In this section the SiC/Si-Diverter — with the best T_{Delay} value in terms of turn-off loss (Table 5.3) — is compared to the fully rated SiC-MOSFET [144] and the Si-IGBT [168] used in the Diverter. As mentioned in Section 4.2.1, this comparison can be made due to IGBT being a Trench/Fieldstop Punch Through (PT) device which is used for high-current multi-die modules. The SiC-MOSFET used in the comparison is rated for 600 A, thus will have a larger die area and slower switching speed than a 480 A device. However, the availability of high-current modules at the time of testing limited the choice. The switching waveforms of all three devices at 480 A, 100 °C are shown in Figure 5.22, with the headline characteristics noted in Table 5.6.



Corresponding FFT of antenna measurement shown in Fig. 5.25.

Figure 5.22: Experimental waveforms of Si/SiC-Diverter (T_{Delay} = 3 μs) compared to fully rated Si-IGBT and SiC-MOSFET. Tested at 480 A, 700 V with device baseplate set to 100 °C. Dashed line represents reconduction of I_c.

5.5.1 Turn-Off Loss

The Diverter has been primarily considered as a way to improve the turn-off performance of the traditional Si-IGBT. As mentioned in previous sections it achieves this by a vastly increased dV/dt and quashing of the tail current. This has been demonstrated in the preceding figures. Additionally, this is clear from the comparison shown in Figure 5.22. It can be empirically confirmed from these waveforms that the improvement is achieved with a significant reduction in loss. When considering the fully rated SiC-MOSFET, it would appear that the Diverter achieves a lower level of E_{Off} as a faster dV/dt is realised with subsequently less area under the power triangle. Nevertheless it has been shown in Section 5.3 that

	Si/SiC-Diverter	SiC-MOSFET	Si-IGBT
E_{Off}	25.6 mJ	19.2 mJ	56.1 mJ
Overshoot Voltage	33 %	40 %	38 %
Oscillations	Low	High (16.1 MHz)	N/A
dV/dt	17 V/ns	6 V/ns	3 V/ns

Table 5.6: Headline characteristics from comparison in Fig. 5.22.

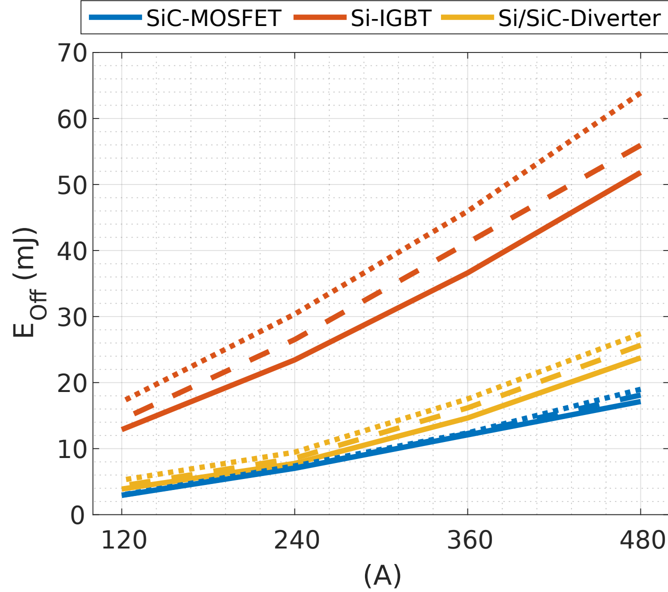


Figure 5.23: Comparison of turn-off switching energy for Si/SiC-Diverter, SiC-MOSFET, and Si-IGBT. Solid line = 75 °C, dashed line = 100 °C, & dotted line = 125 °C.

there are additional loss mechanisms to consider.

The total turn-off switching loss for the Diverter can be seen in Figure 5.23, plotted against the Si-IGBT and fully rated SiC-MOSFET at different load currents and temperatures. It can be seen that as temperature is increased the Si-IGBT performs significantly worse, whereas the SiC-MOSFET exhibits very little temperature dependence. This propitious characteristic can also be observed for the Diverter. The Si-IGBT also exhibits a non-linear relationship between E_{Off} and current, whereas the Diverter follows a much more linear relationship like the SiC-MOSFET. This results in a comparative increase in E_{Off} reduction as current is increased. This is shown in Figure 5.24 where a reduction of ~55 % at

120 A is reached, however this increases to ∼70 % at 480 A. It is also confirmed in this plot that a larger reduction is achieved with an increase in temperature.

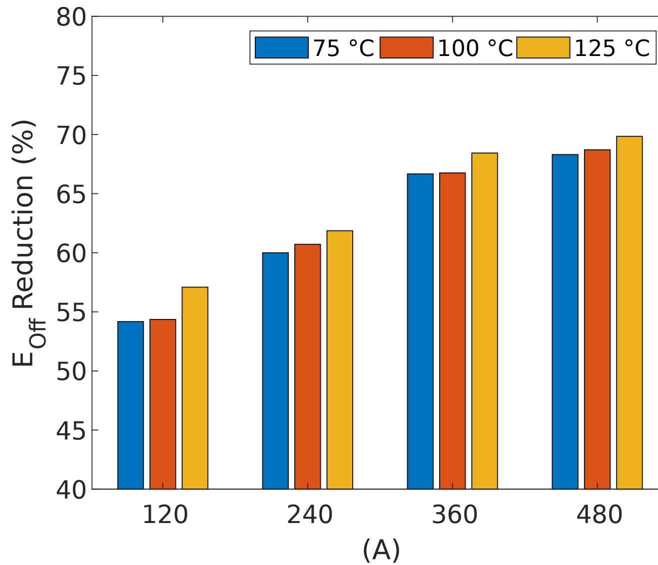
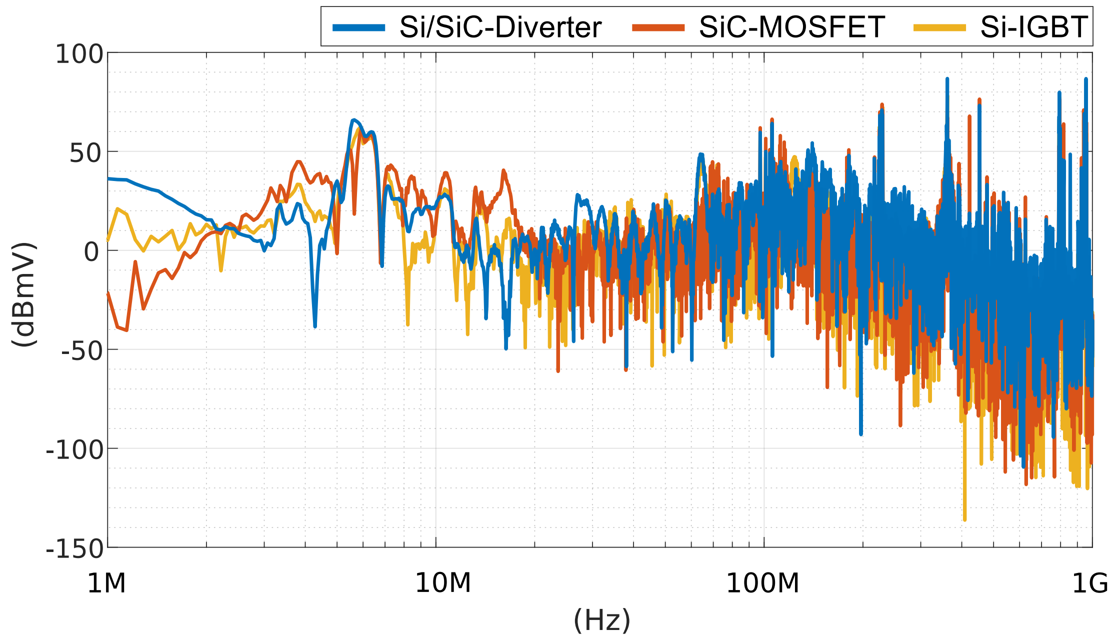


Figure 5.24: Reduction in turn-off switching energy from Si-IGBT to Si/SiC-Diverter.

5.5.2 Oscillatory Behaviour and Overshoot Voltage

The voltage and current waveforms of fully rated SiC-MOSFET in Figure 5.22 show that there is a considerable amount of oscillatory behaviour at turn-off — ±50 A, ±150 V oscillating at 16.1 MHz. In contrast, the Diverter has a similar level of turn-off loss with none of the high energy oscillations. To determine whether this has an appreciable impact on radiated EMI, the measured E-field using the far-field antenna was considered. The resultant FFTs of the spectral content are shown in Figure 5.25.

The 16.1 MHz oscillations that were identified in the SiC-MOSFET voltage and current waveforms (Figure 5.22) can clearly be seen in the antenna measurements as an increase in energy at this frequency up to ∼50 dB, whereas the Diverter registers ∼5 dB at the same frequency. This confirms that this high-frequency oscillation attributed to the SiC-MOSFET does result in a considerable



Corresponding voltage & current waveforms shown in Fig. 5.22.

Figure 5.25: FFT of antenna measurements.

amount of radiated noise. Due to the different packaging/layout between the SiC-MOSFET and the composite Diverter switch — ROHM type-G module and parallel combination of 62 mm modules, respectively — it is not a completely one-to-one comparison, however large magnitude differentials in spectral content can still be considered.

An increase of ~25 dB can be seen at 27–29 MHz for the Diverter. This is suspected to be due to the sharp dV/dt realised by the partially rated SiC-MOSFET used in the Diverter. When comparing the dV/dt magnitudes of the three switches — 17 V/ns, 5 V/ns, and 3 V/ns for the Diverter, SiC-MOSFET, and Si-IGBT, respectively — the Diverter has 3.4× higher dV/dt than the fully rated MOSFET. The datasheet values for C_{oss} are: C_{oss} = 0.88 nF, partially rated SiC-MOSFET [152]; and C_{oss} = 3 nF, fully rated SiC-MOSFET [144]. This reduction in C_{oss} is a result of a physically smaller die area of the partially rated device. The ratio between the output capacitances is also 3.4×, clarifying the reason for the increased switching speed. The increase in dV/dt for the Di-

verter does unfortunately mean that capacitive common-mode current injection may increase relative to Si-IGBT and full SiC-MOSFET implementation. This is an especially important consideration for gate-drive circuitry, particularly in avoiding dV/dt induced turn-on of the other device in a half-bridge [230]. However, this is becoming a well understood and managed issue when moving to a SiC based power converter [231].

In terms of the overshoot voltage, the Diverter achieves a lower level than the SiC-MOSFET but also a 5 % decrease from the Si-IGBT. Theoretically this could allow for an increase of the operating voltage in an inverter system, thus reduction in operating current. This is often a goal in high-power applications — in particular in renewable applications — where reducing I^2R losses in components and busbar/cabling is desired. These benefits can also be realised by a reduction in the weight of conductors, which is advantageous for the automotive and aerospace sector. However, increasing the operating voltage requires consideration of Single-Event Burnout (SEB) behaviour, particularly at high altitudes, as discussed in Section 4.2.2.3.

5.5.3 Justification for the Diverter

5.5.3.1 Impact of Delay Period on Converter Controller and Switching Frequency

A potential limitation of the coordinated switching scheme is the delay that must be considered in the converter controller. This arises from the T_{Delay} period plus the time period before the Si-IGBT turns off (i.e. $t_0 \rightarrow t_4$) that happens at the end the nominal duty period. This can be easily compensated for within the controller, using techniques such as the approaches in dead-time compensation

[232]. Nevertheless, this gives rise to a minimum on period for the switching scheme. Previous reporting on hybrid switching has focused on increasing the switching frequency of Si-IGBT converters beyond what they have traditionally been able to reach for an all round system improvement, such as reduction in size and cost of filtering components. It has been established in this study that a T_{Delay} period of 3–6.5 μs is required at this power level. If operating at a switching frequency of 20–50 kHz (period of 50–20 μs) like much of the previous work suggests, the delay period would, as a minimum, make up 6–32.5 % of the duty period. This would clearly be a limitation posed on the controller. However, applications that are high-power and use a relatively slow switching frequency (1–2 kHz), such as wind turbine converters, where any gain in efficiency can vastly reduce the Levelised Cost of Energy (LCoE) [233], may be more appropriate. If operating at 1–2 kHz, the delay period only represents 0.3–1.3 % of the duty period, thus not limiting the modulation scheme.

Another benefit of operating at these switching frequencies, where the effective duty cycle of the MOSFET device in the Diverter is 0.3–1.3 % (that is T_{Delay} relative to converter switching frequency), is that any thermal stress on the device due to the small period of over current happens on a very low duty cycle basis. The thermal stress on the devices will be further discussed in Section 6.3.

5.5.3.2 High-Capacity Switching Devices

As highlighted in previous chapters, at the time of writing (2020) high-capacity SiC-MOSFET modules are limited to currents of 500–600 A and voltages of 1.2–1.7 kV, whereas Si-IGBT modules exist which can support up to 6.5 kV and upwards of 2 kA. High-capacity SiC offerings will undoubtedly be available in the coming years, however, as discussed in Section 2.7.4, many challenges with

regard to packaging need to be addressed. This may result in: vastly more expensive modules due to the complex packaging solutions; and/or MOSFETs which require to be slowed down, by means of increased gate resistance, in order to have simultaneous switching of the multiple dies.

The Diverter configuration investigated in this study was at 480 A, with a 4:1 (Si:SiC) ratio used. This could be scaled up to larger current magnitudes — using currently available devices — to realise SiC style switching that could be used in high-capacity MW scale applications, with the added benefit of heavily damped oscillatory behaviour that is customary with SiC-MOSFETs. Si-IGBTs which are optimised for on-state performance (i.e. more die area and a high carrier density in the CSR, thus low forward voltage drop but higher capacitance, slower switching speeds and long tail current) could be used.

One of the other intentions of this study was to show that individual modules can be used to construct the composite Diverter switch. Section 5.3 has shown that whilst the interconnect inductance does contribute additional losses, at full current this only makes up 17.4 % of the total turn-off loss. For the power levels considered in this study this negates the need for a new family of devices to be introduced by manufacturers into a market which already has a plethora of options, contrary to what is stated in previous publications [221–223]. This would allow power converter designers to choose a configuration tailored to their specific application from a variety of off-the-shelf devices. In spite of that, when scaling up to larger current magnitudes, a bespoke module which possesses low inter-die stray inductance may need to be considered due to the squared law on the commutation current.

All of the aforementioned benefits that arise from the Diverter come at only a small increase in cost compared to adopting a full SiC-MOSFET solution. As a

purely indicative exercise, a cost comparison is considered. It should be noted that these costs only reflect what is commercially available in 2020 and are at the price point advertised when purchasing a single unit. The cost of the Si/SiC-Diverter investigated in this study is ∼£400 — the *Infineon* Si-IGBT (FF450R12KT4 [168]) costing ∼£140 and the *Cree* SiC-MOSFET (CAS120M12BM2 [152]) costing ∼£260. This equates to a price per amp of ∼0.31 £/A and ∼2.16 £/A for the Si-IGBT and SiC-MOSFET, respectively. Combining these individual components yields ∼0.83 £/A for the complete Diverter.

Considering the cost of similarly rated high-capacity SiC-MOSFET modules — including the one tested in this study — the Diverter is significantly cheaper. The *ROHM* SiC-MOSFET BSM600D12P3G001 [144] costs ∼£1,204 (∼2.00 £/A) and one of the latest *CREE* SiC-MOSFETs CAS480M12HM3 [234] costs ∼£1,916 (∼4.00 £/A). This results in a cost reduction of approximately 58.5–79.3 %. Whilst the cost of high-current SiC devices will drop with further maturation, and benefit from economies of scale, as discussed in Chapter 2, the price will never be comparable to that of a Si-IGBT, or the marginally more expensive Diverter.

The Diverter configuration offers an attractive and affordable option either as an intermediary stage, before further maturation and cost reduction of SiC-MOSFETs, or as alternative to implementing a full SiC solution.

* * *

6 | The Diverter: Converter Losses & Thermal Stress Simulations

6.1 Chapter Introduction

The previous chapter introduced the Si/SiC-Diverter concept. The required timing for the coordinated turn-off event, in terms of minimum turn-off loss and also maximum damping of voltage and current oscillations and voltage overshoot, was discussed. This chapter will use the experimentally determined losses and resultant power profile to investigate further aspects of the configuration and its use in a system. The part-load improvements that a Metal–Oxide–Semiconductor Field-Effect Transistor (MOSFET) can achieve over an Insulated-Gate Bipolar Transistor (IGBT) will also be explored.

The chapter is structured as follows: Section 6.2 discusses the performance of the Si/SiC-Diverter in a three-phase grid-tied two-level inverter by means of simulations to produce efficiency estimates; and Section 6.3 reports on the thermal simulations that were carried out in order to understand the thermal stress on the partially rated Silicon-Carbide (SiC)-MOSFET.

The system-level efficiency estimates and the device-level thermal analysis

were carried out in simulation format due to the restrictions of the hardware setup. In order to perform these studies in hardware, it would required a significantly more complicated testing setup. Moreover, computer based modelling of these aspects of the Diverter concept are a crucial first step in its development.

6.2 Diverter: Use in a Converter

This section examines the Diverter switch configuration in a converter simulation to assess the overall Power Electronic (PE) losses compared to a fully rated SiC-MOSFET and the Silicon (Si)-IGBT used in the Diverter. This will use the switching loss data — both turn-off and turn-on — that was experimentally ascertained in the DPTR (covered in Chapter 5) and the conduction loss properties from the datasheet curves. Whilst the purpose of the SiC-MOSFET in the Diverter is primarily to aide with the turn-off transition, the opportunity for conduction assistance at part-load is also assessed.

6.2.1 Part-Load

As discussed in previous chapters, the conduction profile — the on-state forward voltage drop (V_F) relationship with the forward operating current (I_F) — for a MOSFET device is linear due to a purely resistive on-state characteristic. Whereas, an IGBT device exhibits some linearity plus an offset from the diode voltage drop. This can be explicitly seen in Figure 6.1, which shows the conduction profile for the three devices used in this study. This includes the partially rated SiC-MOSFET (CAS120M12BM2 [152]) and the Si-IGBT (FF450R12KT4 [168]) that make up the Diverter hybrid switch, plus a fully rated SiC-MOSFET (BSM600D12P3G001 [144]). The MOSFET curves are converted from the I_d–

$R_{ds(on)}$ relationship to the corresponding I–V characteristics for comparison with the IGBT. It can be seen in Figure 6.1 that the part-rated SiC-MOSFET achieves a lower level of forward voltage drop than the Si-IGBT when the current is < 120 A. This reduction in on-state voltage at lower currents allows for a lower level of conduction loss at part-load operating conditions.

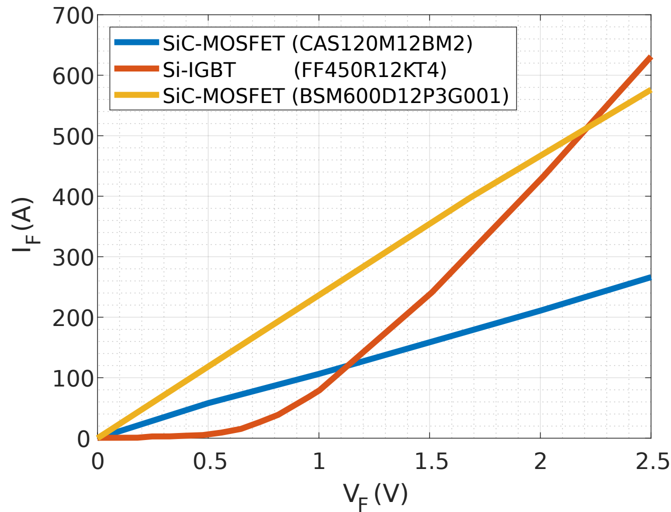
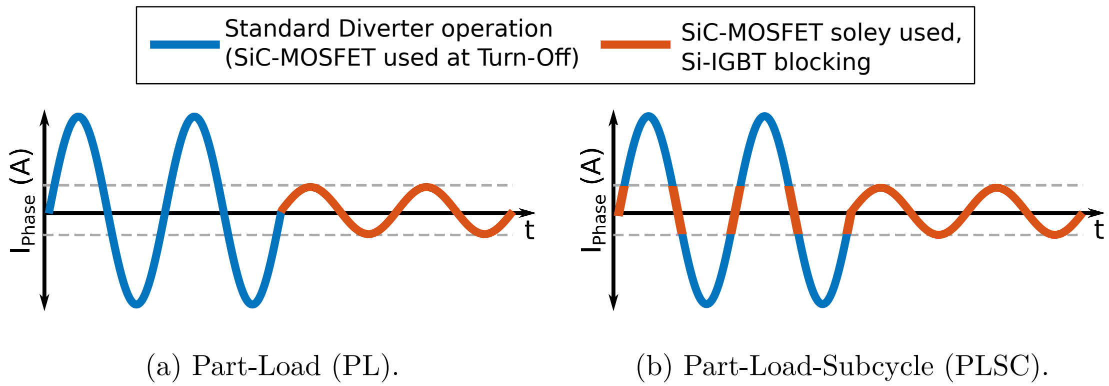


Figure 6.1: I–V forward conduction loss curves of MOSFET and IGBT at 25 °C, digitised from [144, 152, 168].

6.2.1.1 SiC-MOSFET Conduction Assistance

This concept of using partially rated SiC-MOSFETs to aide Si-IGBT converters has been shown in [235], which makes use of two parallel connected converters — one fully rated Si-IGBT based inverter and one partially rated SiC-MOSFET based inverter. For the case of the Diverter, the SiC-MOSFET can provide conduction assistance when the phase current (I_{Phase}) is within the MOSFETs current range. The conduction assistance modes of operation for the Diverter are shown in Figure 6.2.



(a) Part-Load (PL).

(b) Part-Load-Subcycle (PLSC).

Figure 6.2: Diverter conduction assistance modes of operation.

The two identified modes of operation function as follows:

Part-Load (PL) — The PL method, shown in Figure 6.2a, uses the standard Diverter functions when $I_{Phase_max} > 120$ A, however switches to just using the SiC-MOSFET when $I_{Phase_max} < 120$ A.

Part-Load-Subcycle (PLSC) — The PLSC method is shown in Figure 6.2b. This can be considered as an expansion of the PL method, in which the MOSFET is also used for any point in the phase current where the magnitude is < 120 A.

An further improvement in switching loss (including turn-on) should also be achieved when solely using the SiC-MOSFET.

6.2.2 Converter Simulation

The converter simulation that was carried out to assess PE losses and perform efficiency estimations uses a three-phase grid-tied two-level inverter in Simulink. This model comprised a DC source; the inverter, which was made up of ideal switching components; a RC filter branch; and then a Y-Y transformer which interfaces to a three phase voltage source acting as the grid. Figure 1.4 (in Chapter 1) illustrates a similar circuit. The controller for the inverter was a basic

PI controller operating in the dq frame, with the system operating at unity power factor.

This simulation was not fully electro-thermal as the loss data used for the transistors and diodes (to generate the instantaneous power dissipation) was in a 2-D lookup table. However, these loss values selected were at the hottest temperature available (datasheet conduction data and experimentally derived switching data). Therefore, the simulation can be assumed as worst case scenario.

6.2.2.1 Power Electronic Loss Calculations

The power semiconductor devices used in the simulation (transistor and FWD) were ideal switch components and do not provide the loss estimations, instead their firing signals and forward current are passed to a dedicated block which performs calculations. These Simulink blocks are based upon a method presented in [236, 237] — many thanks to Dr. Paul Judge for providing the model which was then adapted to suit. Five categories of PE losses are considered and are shown in Table 6.1, separated as conduction and switching.

Conduction Losses	Switching Losses
• Transistor conduction loss. • FWD reverse conduction loss.	• Transistor turn-on. • Transistor turn-off. • FWD reverse recovery loss.

Table 6.1: Power electronic loss categories/mechanisms.

The measured turn-on and turn-off switching loss data (from Chapter 5), along with extracted datasheet curves for the reverse recovery characteristics and conduction losses, were transformed into look-up table blocks in Simulink. The conduction loss I–V characteristics for the fully rated SiC-MOSFET and Si-IGBT have curves at 25 °C and 125 °C, however the partially rated SiC-MOSFET from Cree only provides data at 25 °C and 150 °C. Therefore, a 125 °C curve was

extrapolated so that the simulation could be run at 125 °C for each configuration. The SiC-MOSFET T_j–$R_{ds(on)}$ curve was also used to fine-tune this curve.

The conduction and switching losses were calculated as shown below:

Conduction Losses — An instantaneous power dissipation value, resulting from conduction losses in the transistor and diode, is calculated. This is achieved by passing the device current to the $I-V$ look-up table and then multiplying the resultant forward voltage drop with the device current.

Switching Losses — The device gate signals are used to trigger a switching loss event, either a turn-on or turn-off. The operating current, at the point of the switching event, is passed to the switching energy look-up table (I–E_{On} or I–E_{Off}). The output energy value is converted to a single pulse of power by dividing by the time step of the simulation.

All of the loss data used is at the worst case scenario (i.e. T_j at the hottest). Once the simulation has reached steady-state, an average value for the total conduction loss and for the total switching loss is taken.

6.2.3 Power Electronic Efficiency Estimates & Discussion

The simulation was run for 5 different configurations: the fully rated Si-IGBT (FF450R12KT4 [168]); the Diverter (CAS120M12BM2 [152] and FF450R12KT4 [168]) under normal operation mode; the Diverter using the Part-Load (PL) mode; the Diverter using the Part-Load-Subcycle (PLSC) mode; and, for comparison, the fully rated SiC-MOSFET (BSM600D12P3G001 [144]).

The results of these simulations are shown in Figure 6.3, with the loss data at 125 °C (i.e. worst case scenario) and the converter operating at a switching frequency of $f_{sw} = 2$ kHz. This is presented as a bar chart of the total PE losses — as a percentage of the converter rated power — for the full operating power range. The bar comprises a stack containing both components of the PE losses — where the switching loss is denoted by the solid colour bar and the conduction by a bar with 50 % transparency. It should be noted that this is only semiconductor losses and does not include other converter losses, such as filter losses.

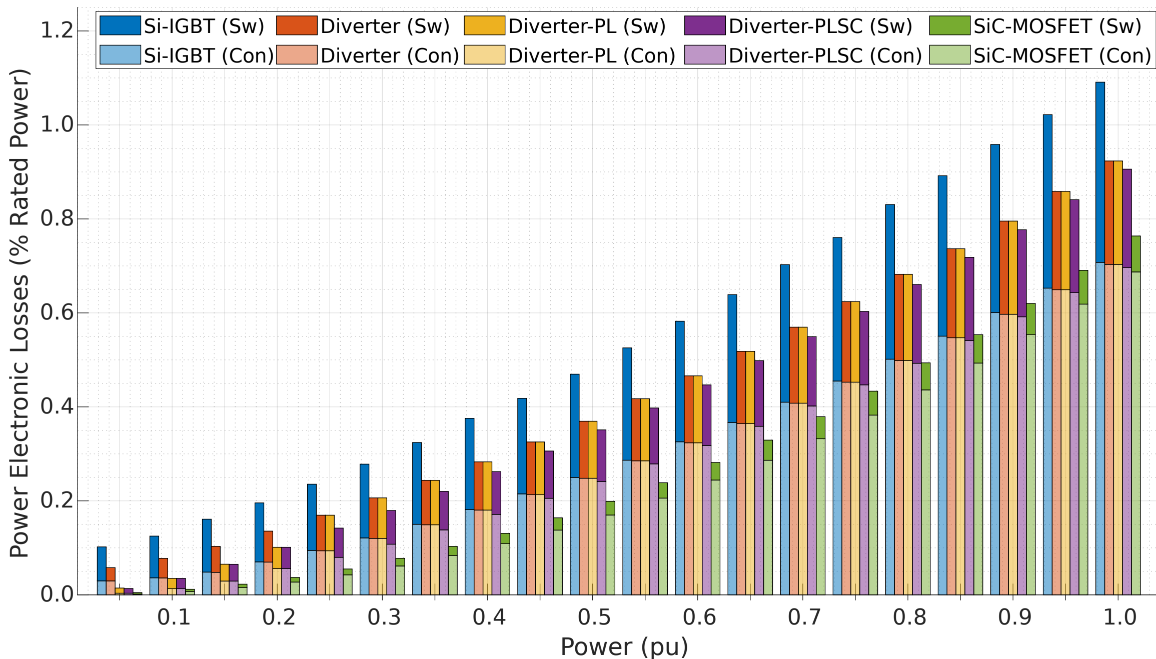


Figure 6.3: Power electronic losses from inverter simulation. Losses as a percentage of rated power ($f_{sw} = 2$ kHz).

As expected, the Si-IGBT performs worst across the full power range, with the fully rated SiC-MOSFET clearly outperforming the IGBT and Diverter.

It was established in the previous chapter that the Si/SiC-Diverter achieves a reduction in turn-off loss of ∼55 % at 120 A and up to ∼70 % at 480 A. It can be seen from Figure 6.3 that at full power (i.e. 1.0 pu power, $I_{Phase_max} = 480$ A), the total PE losses when using the Si-IGBT are 1.091 %. This is reduced to 0.923 % when using the Diverter, and further to 0.906 % when the Diverter is operated in PLSC mode. This represents a reduction of ∼17 % total PE losses. A similar trend continues as the current level is reduced, however this becomes difficult to discern on Figure 6.3. To better appreciate the trends that emerge, and the fine details at the lower end of the power range, the loss data has been normalised to that of the Si-IGBT and is shown in Figure 6.4. The additional performance gains that the Diverter can achieve when operating in PL or PLSC are clear.

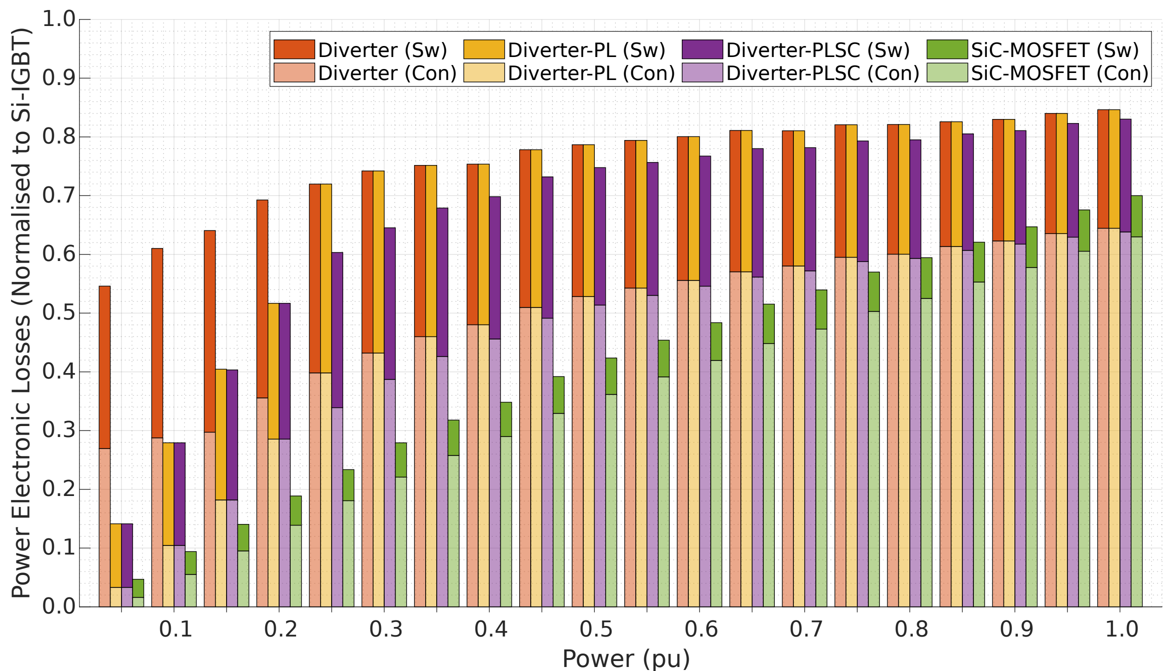


Figure 6.4: Power electronic losses from inverter simulation. Losses normalised to Si-IGBT ($f_{sw} = 2$ kHz).

It can be observed that the level of loss for the Diverter (all modes) falls considerably relative to the IGBT as the operating point is reduced. Considering the Diverter in PL mode (yellow bars), between 0.05–0.2 pu power, there is a significant further reduction due to the improved conduction and switching from solely using the SiC-MOSFET at these set points. However, when the PLSC method is employed, a reduction in conduction loss is achieved across the full power range. This is marginal, yet still pertinent, at the higher end, but becomes a larger reduction as the operating point reduces due to using the SiC-MOSFET for a larger proportion of the sinusoid. Between 0.05–0.2 pu power, the PL and PLSC are operating in the same manner, thus the level of loss is the same.

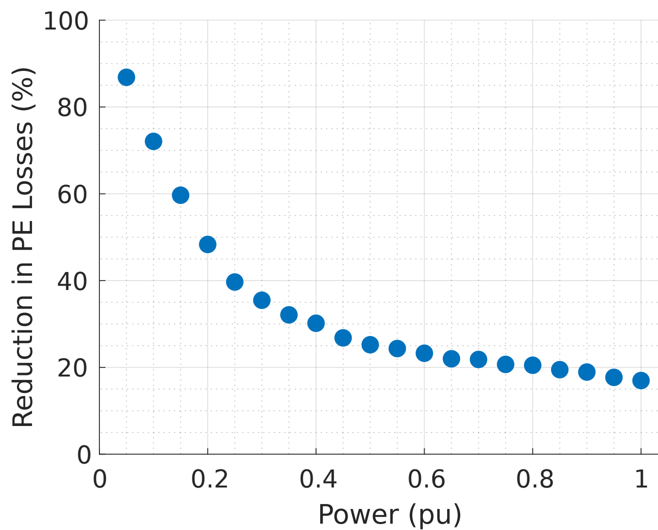


Figure 6.5: Power electronic loss reduction, Diverter (PLSC) losses normalised to Si-IGBT losses.

In order to make the improvement more distinct, Figure 6.5 shows the total reduction in PE losses that can be achieved when using the Diverter in PLSC mode compared to just the Si-IGBT. At 1 pu power, PE losses are reduced by $\sim$17 % (1.09 % $\rightarrow$ 0.9 % of rated power), however at 0.05 pu this is increased to a vast $\sim$87 % (0.1 % $\rightarrow$ 0.013 % of rated power).

6.3 Diverter: Thermal Stress on SiC-MOSFET

Even though the partially rated SiC-MOSFET is only over-loaded for 3–6.5 μs during the turn-off switching assistance, and within the repetitive short-pulse over-current capacity, the thermal stress that the device is subject to must be examined. In order to do this a thermal simulation of the MOSFETs junction temperature was conducted. This was done using the transient thermal impedance (Z_{th}) information from the datasheet and the power that is dissipated on the SiC die, in a Simulink thermal model.

6.3.1 Thermal Impedance Z_{th}

The transient thermal impedance (Z_{th}) describes the thermal behaviour when a pulse of a certain time period and power magnitude is applied to a semiconductor. Specifically, this is defined as a junction to case quantity ($Z_{th}(j\text{–}c)$) and characterises how heat can be transiently dissipated from the die junction to the module case, i.e. the baseplate of the package.

The thermal path from junction to case for a semiconductor device is not purely resistive and linear. Rather, it is a complex network made up of various thermal capacities and paths of thermal resistance. This arises from the various layers of materials (substrate layer, solder/sinter attaching materials, copper baseplates, ceramic electrical insulators, etc.) and differing thermal properties of these layers and the semiconductor. Therefore, the resultant thermal impedance — which has units of $^{o}C/W$ — can be quantified as a time-dependant multi-order exponential function. Figure 6.6 shows the $Z_{th}(j\text{–}c)$ plot for the SiC-MOSFET. Multiple curves are displayed on this plot — the lines that are numerically marked

relate to specific duty cycles for steady-state conditions and the bottom-most line (with blue markers) relating to a single pulse width. This single pulse line is what is used to extract the information for the thermal model. The thermal impedance curves are determined by methods documented in [164,165], these are summarised in [238].

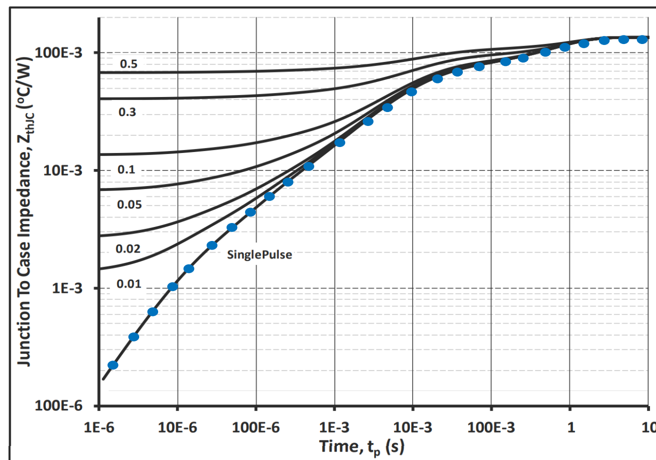
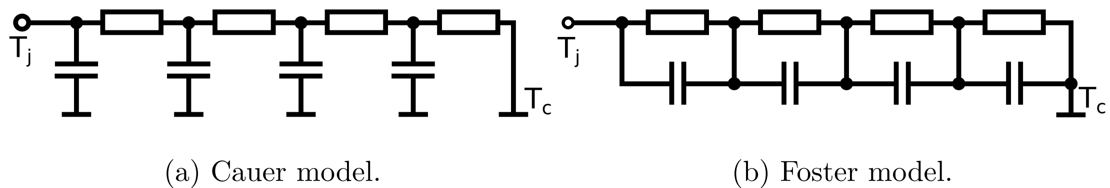


Figure 6.6: Junction to case thermal impedance ($Z_{th}(j\text{–}c)$) of CAS120M12BM2 SiC-MOSFET, adapted from [152] - copyright: Cree, Wolfspeed.

Two different models are commonly used to model Z_{th}: the Cauer and Foster equivalent models, both of which comprise RC networks as shown in Figure 6.7.



(a) Cauer model.

(b) Foster model.

Figure 6.7: Thermal network equivalent circuits.

Cauer (Figure 6.7a) — A continued-fraction circuit which corresponds to the physical layers and structure of the thermal system, where each RC branch can be assigned to one layer. This can be used when the characteristics of the individual layers are known.

Foster (Figure 6.7b) — A partial-fraction circuit where the RC elements do not correspond exactly to specific layers. Rather, the entire network reflects the

thermal system and can be analytically modelled using the single pulse Z_{th}(j–c) curve. Therefore, this was the thermal network chosen for this study.

6.3.1.1 Foster Thermal Network

Using the Foster network method, the partial-fraction model can be expressed as (6.1)

$$Z_{th}(t) = \sum_{i=1}^{n} r_i \left(1 - e^{-\frac{t}{\tau_i}}\right) \qquad [\Omega] \tag{6.1}$$

where: the time constant $\tau_i = r_i c_i$ — i.e. the RC components of each branch [238]. A 4$^{\text{th}}$ order Foster system is shown in Figure 6.8.

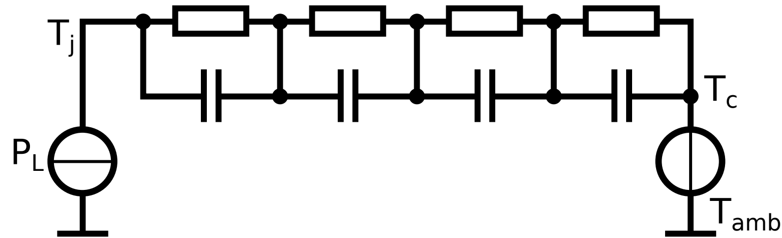


Figure 6.8: Foster thermal network (4th order).

In an electrical equivalence of a thermal model, a heat source is defined as a current-source which drives a thermal impedance. The resultant voltage is analogous to the rise in temperature. This can be seen in Figure 6.8, where the power losses dissipated in the device (P_L) are connected to the junction thermal node (T_j). The second source in the Figure can be used to set a known case temperature (T_c). T_j can then be calculated as expressed in (6.2)

$$T_j(t) = P_L(t) \cdot Z_{th}(t) + T_c(t) \qquad [^{0}\text{C}] \tag{6.2}$$

The Z_{th} of the thermal interfacing pad/paste and the cooling system can also be modelled in a similar fashion by adding additional RC elements to the network, however for this study that was not necessary.

6.3.2 Thermal Simulink Model

Figure 6.9 shows the full thermal model that was built in Simulink [239] using the Simscape multi-domain physical system simulator. The built-in Foster Thermal Model [240] was used to simulate the heat transfer through the SiC-MOSFET.

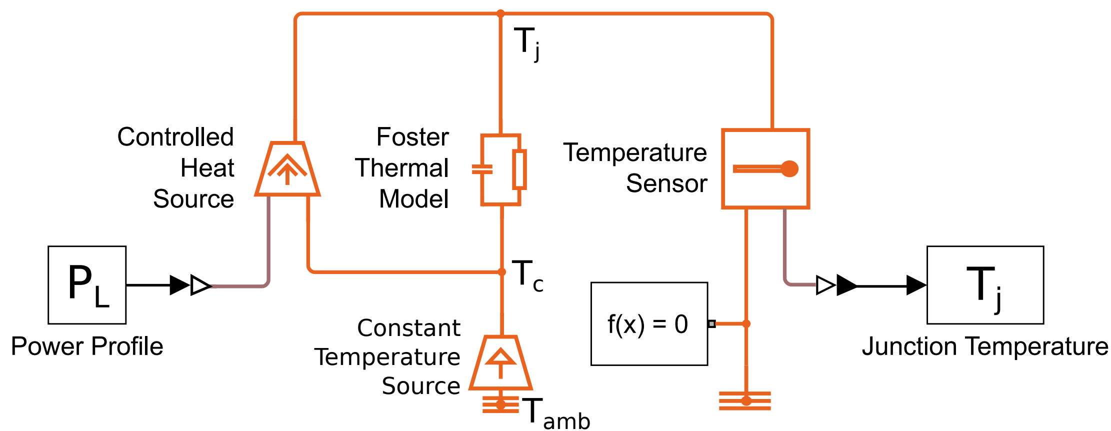


Figure 6.9: Junction temperature Simulink model.

The Foster Thermal Model requires a series of $Z_{th}(j\text{–}c)$ values and corresponding time constant values — this was taken from the single pulse line in Figure 6.6. The power profile P_L was constructed from the experimental data in Chapter 5. This includes the three areas of loss identified: commutation ($V_{ds} \cdot I_d$), conduction (${I_d}^2 \cdot R_{ds(on)}$), and the actual switching event ($V_{ds} \cdot I_d$). This instantaneous power data is used in the P_L source which in turn drives a controllable heat source. This is connected to the Foster network at T_j. As it is the absolute temperature rise that is of interest, T_c was set to 0 °C by the constant temperature source. A temperature sensor block is then used to measure T_j.

6.3.2.1 Single Pulse Response

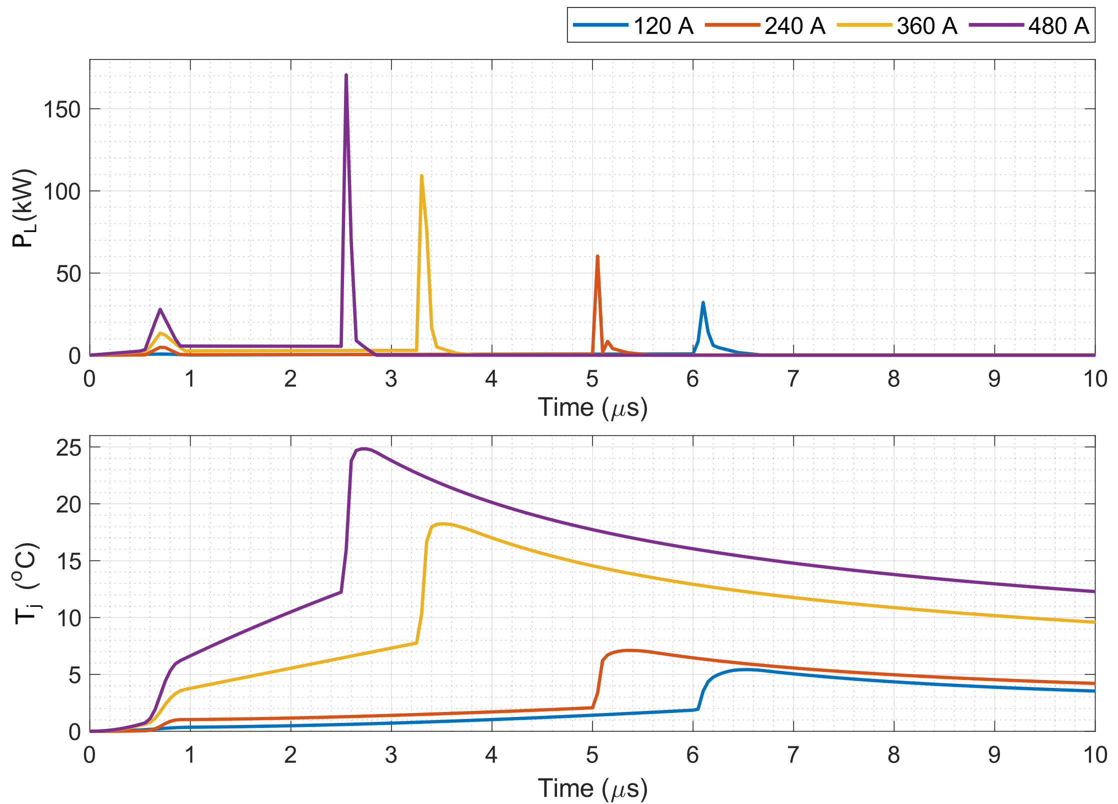


Figure 6.10: Power loss profiles of Diverter (P_L) and resultant junction temperature (T_j) response (above heatsink temperature).

The thermal response to a single switching event is shown in Figure 6.10 for the four current set points tested (with the determined T_{Delay} values). For each set point there is a similar trend in each phase of the Diverter operation:

Commutation Phase — An initial fast rise in T_j.

Conduction Phase — A slower, yet significant rise in T_j. This is where the device is conducting up to 4× its rated ampacity.

Switching Phase — A sharp increase in T_j. This is due to the high magnitude of P_L, but also due to this pulse having a very fast rise and fall time.

The length of T_{Delay}, which dictates the length of the conduction time, clearly has a significant impact on the subsequent peak T_j. Therefore, as expected and

pursued in Chapter 5, T_{Delay} should be kept to a minimum. Considering the 480 A case, a peak temperature rise of 25 °C is reached. The cooling curve is then shown to slowly fall back toward 0 °C. This exponential fall can be better appreciated in Figure 6.11 which is plotted on a logarithmic x-axis. For the 480 A case, T_j <1 °C after ∼1 ms — this shows that even for a relatively small T_{Delay} period of 3 μs, plus the switching event, the thermal impact is significant.

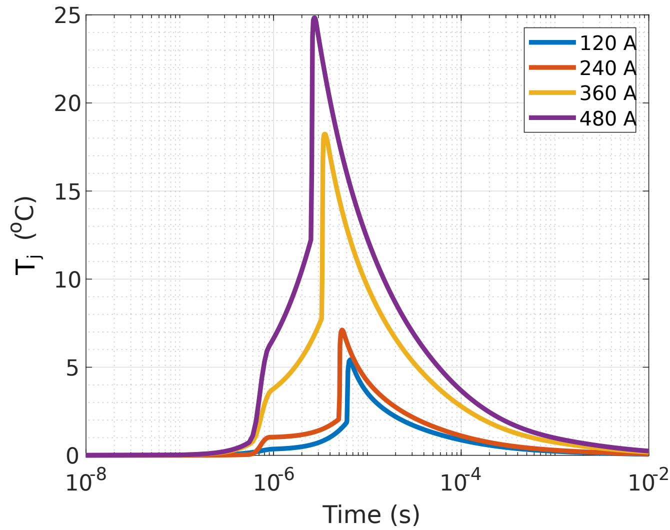


Figure 6.11: Junction temperature (T_j) response (above heatsink temperature), on logarithmic scale.

6.3.3 Thermal Simulation: Constructing the Power Profile for Steady-State

To understand the cumulative impact of these pulsating temperature spikes, the power stimulus at P_L was then adapted to allow for continuous operation. To analyse this thermal stress on the SiC-MOSFET under continuous conditions, a sinusoidal based P_L was constructed, whereby P_L is varied such that the device operating current follows a sinusoidal phase current. This was done by assigning bins to the sinusoid, with a bin width equal to the period of the switching frequency. For each bin, a single pulse P_L from Figure 6.10 (the closest of 120 A,

240 A, 260 A, or 480 A to I_{Phase}) was selected. This scheme is shown in Figure 6.12 and 6.13. In Figure 6.12 I_{Phase} is shown in the top plot and P_L shown in the middle plot. The resultant rise in T_j is shown in the bottom plot.

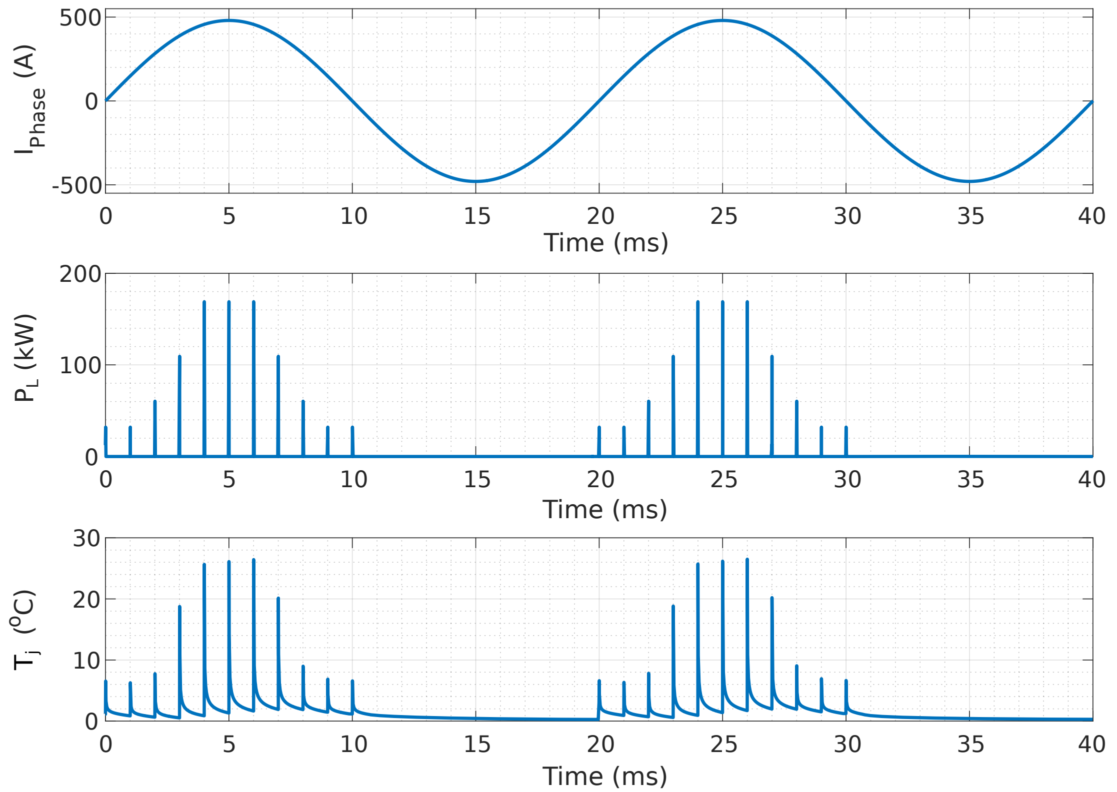


Figure 6.12: Continuous thermal stress simulation, $f_{sw} = 1$ kHz.

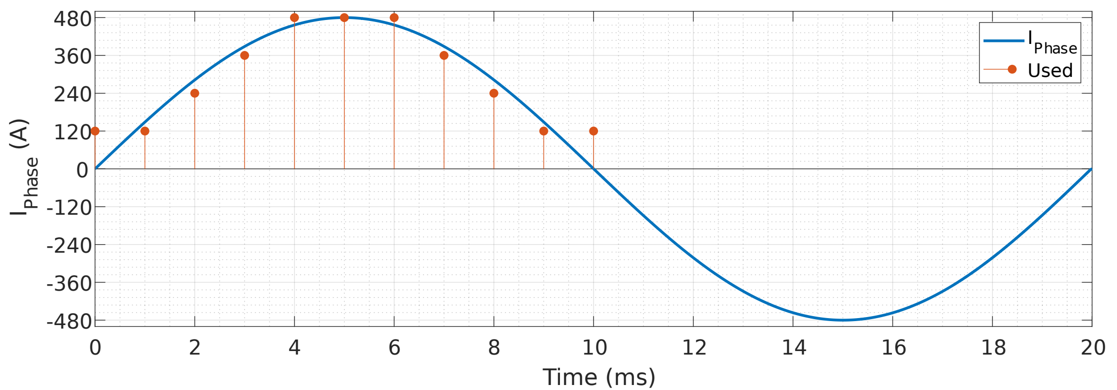


Figure 6.13: Thermal simulation scheme, $f_{sw} = 1$ kHz.

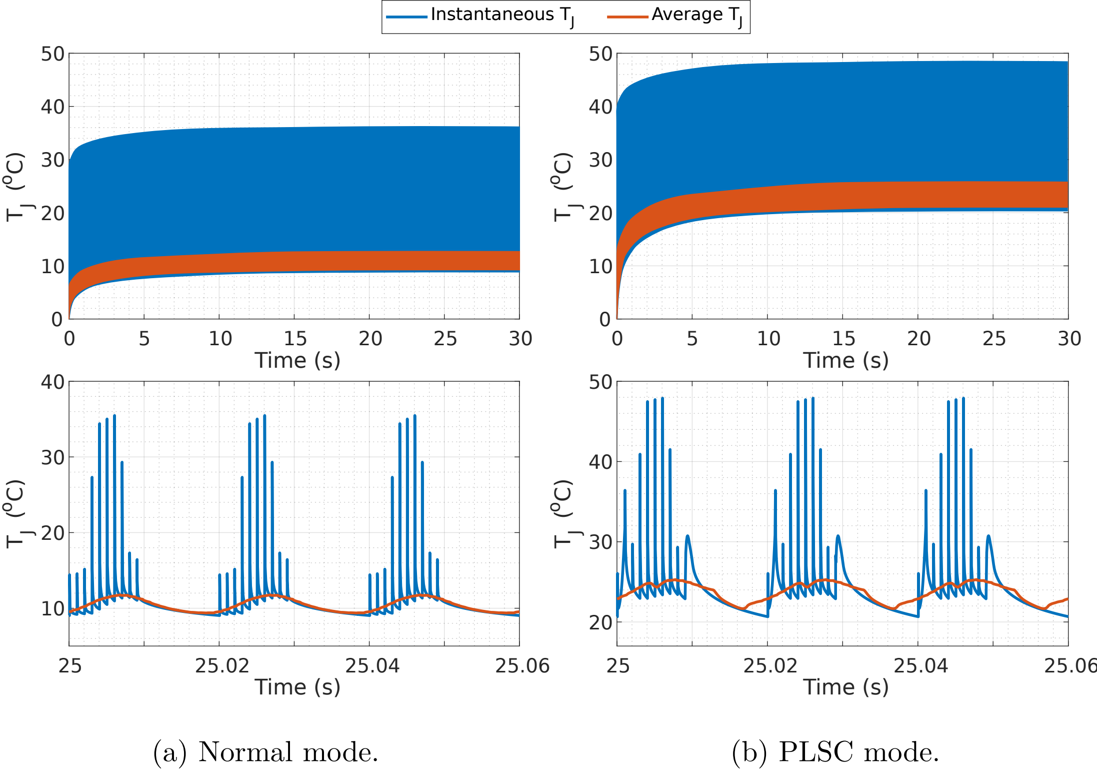
As shown in Figure 6.13, there is a caveat to this exact method, in which the limited range of test data has been fitted to the simulation. The blue line is what the level of current should be and the red stem lines represent the values which are used in the simulation. In some cases there is an underestimation of P_L due

to it being at a lower level of current than I_{Phase} stipulates. However, in other areas it has been overestimated. Therefore, it is a good approximation of what would happen in an actual converter.

6.3.4 Thermal Simulation: Steady-State

The following sections will consider the steady-state thermal conditions which are realised for the different operating mode considered for the Diverter (Section 6.2), and the impact of switching frequency.

6.3.4.1 Operating Mode



(a) Normal mode.

(b) PLSC mode.

Figure 6.14: Thermal simulation: Si/SiC-Diverter mode of operation, $f_{sw} = 1$ kHz.

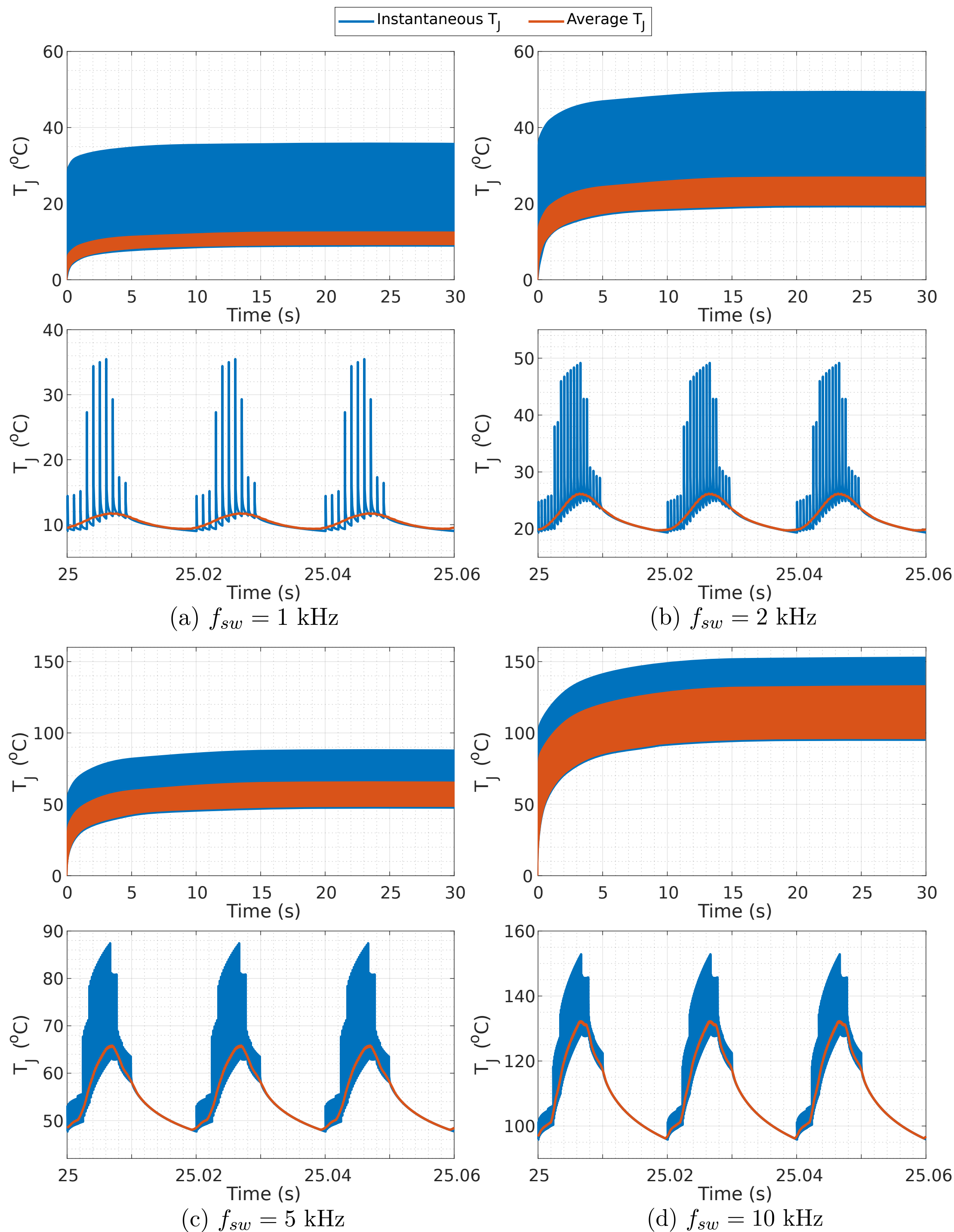
The simulations were set to run at a switching frequency of 1 kHz. This was run for 30 s in order to give the thermal system enough time to reach a steady-state value. The result of the Diverter operating in normal mode (i.e. solely turn-off switching assistance) is shown in Figure 6.14a. The top plot shows the entirety of the simulation and the bottom plot shows a 60 ms window of the run. The single pulse response which was identified in Section 6.3.2.1 results in a high-frequency temperature variation. The *movmean* filter was used to remove the high-frequency spikes to discern an average T_j at the SiC junction. It can be seen that after ∼10 s, a steady-state has been reached. This is an average T_j of 9.5–12 °C, however with a high-frequency ΔT_j of 9–36 °C. The PLSC mode was then run to assess the impact of the additional conduction period. These results are shown in Figure 6.14b. The conduction periods can be seen to increase T_j, this is apparent when comparing to Figure 6.14a. The average T_j for the PLSC mode fluctuates between 22–25 °C (ΔT_j spikes between 21–48 °C).

6.3.4.2 Switching Frequency

	1 kHz	2 kHz	5 kHz	10 kHz
ΔT_j	9–36 °C	19–49 °C	47.5–87 °C	96–153 °C
Average T_j	9.5–12 °C	19.5–26 °C	48–66 °C	97–133 °C

Table 6.2: SiC-MOSFET junction temperature, varying switching frequency.

To assess the impact that the device switching frequency has on the thermal stress, four different switching frequencies were investigated — 1 kHz, 2 kHz, 5 kHz, and 10 kHz. These runs, which only use the Diverter for switching assistance, are shown in Figure 6.15 with the resultant ΔT_j value listed in Table 6.2. As expected, an increase in switching frequency results in an increase in T_j. There is an increase of approximately 11.6 °C for every 1 kHz increase in f_{sw}.



(a) $f_{sw} = 1$ kHz (b) $f_{sw} = 2$ kHz

(c) $f_{sw} = 5$ kHz (d) $f_{sw} = 10$ kHz

Figure 6.15: Thermal simulation: Si/SiC-Diverter, varying switching frequency.

6.3.5 Discussion on Thermal Stress

The thermal stress on the partially rated device due to over-loading it is significant. Considering that the maximum datasheet value T_j for the SiC-MOSFET is

150 °C, the operating switching frequency is clearly of importance and requires constraints. The rise in T_j is relative to a $T_c = 0$ °C, therefore, the temperature of the baseplate when applied in an actual converter must be taken into account. As described in Chapter 5, the SiC-MOSFET would be placed adjacent to the Si-IGBT. As a result of the IGBT losses, the cooling system (heatsink or liquid cooling block) will be at temperature — this could be in the range of 75–100 °C. Hence the T_j temperature rises that have been derived from the simulations should be considered relative to a realistic T_c temperature. Consequently, the thermal modelling carried out in this study would suggest that operating the Diverter at 1–2 kHz is appropriate. Higher operating frequencies — which much of the previous work in literature would suggest — is likely to result in T_j exceeding the maximum allowable value. This is compounded when including the additional temperature rise from the PLSC mode. The separation of the SiC-MOSFET die and the Si-IGBT die (by virtue of using separate modules) will also aide with thermal management of the MOSFET. If the devices were housed in the same module, the SiC-MOSFET would undoubtedly be at an increased temperature to what it would be in a separate module.

The thermal simulations that have been carried out provide a good approximation of T_j under various conditions. Nonetheless, further work is required to fully investigate detailed thermal cycling of the SiC-MOSFET. Finite Element Method (FEM) modelling of the semiconductor would provide a deeper insight into the thermal behaviour. However, that would be limited by what is made available by the device manufacturer as device specifics would be required. Moving on from double-pulse testing to running the Diverter in a continuous manner, in a fully rated converter, would provide the best understanding of the actualities of the system and is imperative to further this work.

Typical thermal cycling profiles of power semiconductor devices is a well

understood and documented area, with temperature-induced degradation and parameter shifts of SiC devices being widely reported on [241, 242]. Various thermo-mechanical issues arise due to excessive temperature stress on a device, however the studies have shown this is a result of exceeding T_{j_max} for continued periods of time over many power cycles. These issues can present as: cracking in the semiconductor crystal structure and bond-wire lift-off or breakage, both of which result in an increased $R_{ds(on)}$; delamination/cracking of die-attach layers; and substrate solder/sinter fatigue. Semiconductor and other material layer degradation usually occurs gradually over time, whereas bond-wire defects most often happen quickly. The main mechanisms which lead to these defects are differing thermal expansion coefficients for the various layers of the die, as well as the other thermal, electrical, and mechanical materials within the package. A shift in V_{Th} can also happen with thermal stresses, however SiC-MOSFETs have shown to maintain stability up to ∼200 °C.

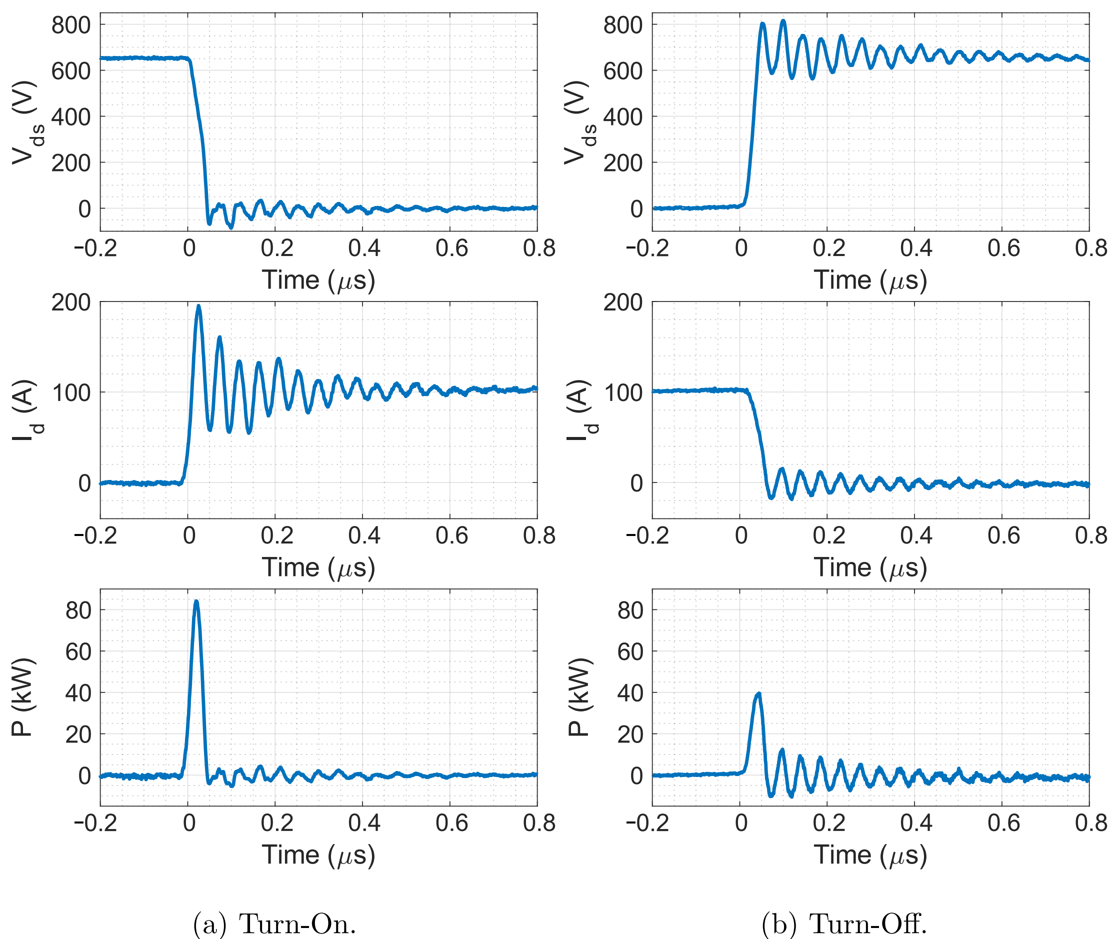
Monitoring degradation of a device has seen a lot of attention in recent years, particularly with the widening adoption of SiC-MOSFETs and their use at higher temperatures. On-line condition monitoring techniques which utilise Temperature Sensitive Electrical Parameters (TSEP) have been reported [243]. Whilst T_j can be inferred from TSEP shifts by comparison to known temperature coefficients, degradation can also be deduced. Commonly used TSEPs include [244]: V_{Th}, $R_{ds(on)}$, MOSFET body diode forward voltage drop, switching trajectories (dI_d/dt, dV_{ds}/dt and miller plateau), and gate leakage current.

What is unknown, however, is the ageing effects of the high-frequency ΔT_j on the SiC die. A switching frequency of 1–2 kHz has been shown to stay below the T_{j_max}, however a $\Delta T_j \approx$ 27–30 °C — which is aligned with the switching intervals — occurs and could pose as an ageing mechanism. Currently no literature is available on this specific behaviour. This is an area which will require

continuous operation testing and thermal cycling to comprehend. Visual evidence of degradation is also commonly used for off-line analysis.

6.3.5.1 Thermal Stress Compared to Standard Operation of SiC-MOSFET

To understand if this ΔT_j is comparable to what the SiC-MOSFET is ordinarily qualified to withstand, a further thermal simulation was conducted. This involved modelling the MOSFET in an application where the device is subject to a constant, maximum allowable load under a standard Pulse-Width Modulation (PWM) switching scheme.

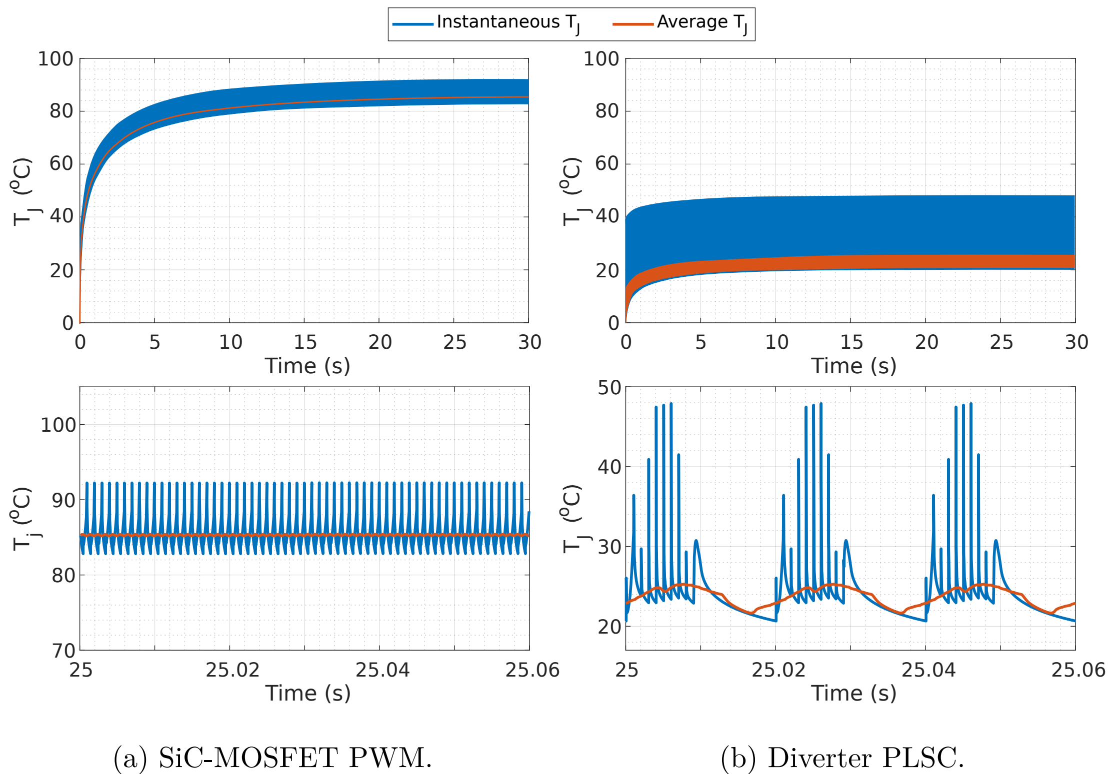


(a) Turn-On. (b) Turn-Off.

Figure 6.16: Experimental waveforms of 120 A SiC-MOSFET (CAS120M12BM2 [152]) switching transients.

The experimentally measured switching transients of the device, shown in

Figure 6.16 were used. The resultant calculated instantaneous power plots made up the switching components of the loss profile. For the conduction loss component, this was derived in a similar manner to Section 6.3.3 where $P_{L_cond} = {I_d}^2 R_{ds(on)}$. The current was set to track a repeating ramp (50–120 A) during the conduction period as if it were determined by an Inductor, which is typical in a buck or boost converter. A fixed duty cycle of 0.5 was selected with a switching frequency of 1 kHz. The thermal simulation results of this are shown in Figure 6.17a compared to Diverter (PLSC mode) in Figure 6.17b.



(a) SiC-MOSFET PWM.

(b) Diverter PLSC.

Figure 6.17: Thermal simulation: Si/SiC-Diverter vs. standard PWM on SiC MOSFET, $f_{sw} = 1$ kHz.

Whilst there is a difference in the steady-state low-frequency temperature that each configuration reaches, it is irrelevant as it is the high-frequency ΔT_j that is of interest. It can be seen in Figure 6.17a that the PWM switched SiC-

MOSFET exhibits a $\Delta T_j \approx 10$ °C, whereas the SiC-MOSFET in the Diverter configuration is subject to a $\Delta T_j \approx 27$–30 °C. This represents a 2.7–3× increase in ΔT_j when using the Diverter configuration compared to what would occur in a typical operating manner. The thermo-mechanical stress that is a result of this requires further investigation.

*   *   *

7 | Conclusions

The work presented in this thesis has focused on the switching performance of high-capacity semiconductor switches, with a particular emphasis on the emergent Wide-Bandgap (WBG) transistor — the Silicon-Carbide (SiC) Metal–Oxide–Semiconductor Field-Effect Transistor (MOSFET) — and its use within a hybrid switch configuration alongside the traditional Silicon (Si) Insulated-Gate Bipolar Transistor (IGBT).

7.1 Conclusions on Hybrid Switching & The Si/SiC Diverter

Two hybrid concepts — which comprise a mixture of Si and SiC semiconductor material — were investigated in this thesis.

Hybrid IGBT (Si-IGBT with SiC-FWD) — The first hybrid concept, which was briefly looked at, makes use of a SiC-Merged PIN Schottky (MPS) as the Freewheeling Diode (FWD) for the Si-IGBT. This is an established technique due to the maturation of SiC-Schottky diodes and is offered by various manufacturers. However, it does not appear to be used extensively in industry at present. It was experimentally verified that this device achieves a lower level of

switching loss than a full Si device. It was also shown that the "snappy" diode behaviour, which is an issue with the standard high-capacity Si-Fast Recovery Diode (FRD) is eliminated, thus making the Electromagnetic Interference (EMI) behaviour across the full operating range more predictable.

Si/SiC-Diverter — The main piece of investigative work in this thesis focused on the Si/SiC-Diverter concept, which involves a fully rated Si-IGBT with a part-rated SiC-MOSFET used to assist with the turn-off transition.

The delay period (T_{Delay}, i.e. the period of time which the SiC-MOSFET conducts on its own at the end of the conduction period) was found to be in the order of 3–6 μs. These T_{Delay} values make the Diverter best suited for applications which do not require high converter switching frequencies, which is the case for high-power converters which typically use 1–2 kHz. This means that the delay period does not limit the minimum on-time as it only represents 0.3–1.3 % of the duty period. The thermal simulations which were carried out confirmed that a lower switching frequency ensured that the average device junction temperature remained within a safe level. However, the effect of the high-frequency temperature perturbations on the SiC-MOSFET die is an area which requires further investigation. The current capacity of the part-rated SiC-MOSFET was chosen in accordance with its short-pulse over-current rating from the datasheet, which was 4× nominal current. Therefore, the 120 A SiC-MOSFET was used in conjunction with a 480 A Si-IGBT with the thermal simulations confirming that these repetitive small over-current events on the MOSFET are tolerable. The turn-off switching loss was found to be reduced by 55 % at low current and 70 % at full current compared to the Si-IGBT, whilst only being marginally greater than a fully rated SiC-MOSFET.

The T_{Delay} dependant snubbering action on the oscillatory behaviour and voltage overshoot was also investigated. It was shown that a significant amount of

damping is achieved from the brief reconduction of the Si-IGBT. A conduction assistance mode of operation was considered, which used solely the part-rated SiC-MOSFET when the load current was within the device's current capabilities. This is enabled by the superior conduction loss of the MOSFET at low current levels compared to an IGBT at low current levels. This, along with only the turn-off switching assistance, was compared to a fully rated SiC-MOSFET and fully rated Si-IGBT in a two-level grid-tied converter simulation. This simulation used the datasheet specified conduction losses and the experimentally attained switching loss value to determine converter efficiencies. The Part-Load-Subcycle (PLSC) mode of operation results in the Diverter configuration achieving a reduction of approximately 17 % total power electronic losses at 1.0 pu power and a vast 87 % at 0.05 pu power.

The power loss performance is comparable to that of a fully rated SiC-MOSFET, however these benefits come at only a small increase in cost relative to a Si-IGBT and at a significantly reduced cost to a full SiC solution. The Diverter concept may act as an intermediary stage before higher current level SiC-MOSFETs are achievable. Alternatively, this technique could offer a better solution to high-capacity SiC-MOSFETs, due to a more economic configuration of semiconductor die and with the additional benefit of the natural snubbering action.

7.2 State of the Art High-Capacity Transistors - Literature Review Conclusions

Chapters 2, 3 and 4 of this thesis provided a critical analysis and explanation of the nuances of high-power semiconductor transistors and their associated components; a detailed design overview of a testing and measurement platform which is capable of characterising these high-capacity, fast switching devices; and an experimental comparison of the two prominent device technologies, as well as various discussions on what is required to fully utilise them. Whilst they have similar structures, a MOSFET is fundamentally a different device to an IGBT and, as discussed, has superior switching and conducting properties. However, the MOSFET device is only made viable at high-power levels thanks to the SiC semiconducting material which has more desirable characteristics than Si. A SiC-MOSFET can achieve approximately 15 % of the power electronic losses (combined switching and conduction) of an equally rated Si-IGBT. The diode device, which is commonly connected in an anti-parallel manner with the transistor, has also been improved by the adoption of SiC, and the Schottky structure. Despite the advancements that SiC ostensibly brings, there are certain factors which are currently, and may always be, a hindrance. The main barriers to the adoption of SiC-MOSFETs can be summarised as follows:

Increased Cost — A SiC-MOSFET is more expensive relative to a Si-IGBT. This is in terms of both the semiconductor die, due to increased cost of the fabrication process, and the more advanced packaging technologies which are required in order to fully utilise the theoretical performance. As of 2020, the price per amp of a SiC-MOSFET is 5–6× greater than a Si-IGBT. Whilst advancements in manufacturing processes and the benefits in economies of scale will reduce this

disparity, the price of a SiC-MOSFET will always be greater due to the more complex and energy intensive fabrication processes.

EMI Precursors — The fast switching edges of a SiC-MOSFET lead to a reduction in switching losses compared to a Si-IGBT, however this results in an increase in the likelihood of EMI problems. Specifically this is due to an increase in dI/dt, dV/dt, oscillatory behaviour and voltage overshoot. These traits can result in Electromagnetic Compatibility (EMC) issues and can also compromise a converter's functional self-immunity. The extreme dV/dt also necessitate improved insulation of inductive components and machine windings. Circuits which were built to work with traditional Si devices undoubtedly will require a redesign in order to work with these fast switching SiC devices — both the physical power circuits (PCB or busbar based) and the gate drivers. These gate drivers will most likely also require a variety of advanced features in order to fully exploit the possible performance of SiC-MOSFETs.

High-Current Capability — Si-IGBTs, which are used in MW scale applications, have current ratings of at least 1.5 kA, however the highest rated commercially available SiC-MOSFETs are ∼600 A. Whilst this will clearly increase in the years to come, the paralleling of multiple dies to achieve current ratings in this range will always be a difficult challenge to ensure the composite transistor switches in a uniform manner due to stray inductance mismatches. To overcome this, these devices will most likely require large internal gate resistors to intentionally slow the switching edges, or some form of Active Gate-Drivers (AGD).

Nevertheless, moving from a Si-IGBT to a SiC-MOSFET based design has some major advantages. As previously stated, the SiC device can operate more efficiently than it's Si counterpart due to the reduced switching and conduction losses, resulting in reductions in power electronic losses of greater than 80 %. The reduction in the switching loss component — due to the increased speed of the

switching transients — can be exploited as either: a straightforward reduction in loss; an increase in converter switching frequency; or somewhere in between. If an increase in converter switching frequency is the motivation, a reduction in the weight and volume of the circuit's magnetic components can be realised, which can in effect result in a reduction in overall system costs.

In order to fully exploit the material, the packaging technologies need to be improved. A SiC-MOSFET can theoretically reach blocking voltage levels of > 10 kV, however the balance between low stray inductance and high-voltage isolation makes packaging techniques difficult and expensive. High temperature operation is another SiC characteristic which is also currently obstructed by current packaging. Notwithstanding this, there is a lot of research in the area of WBG device packaging which seeks to address these issues.

Accurately characterising the switching performance of SiC-MOSFETs — both in terms of the losses and the transient characteristics — can necessitate higher performance measurement equipment than is required for Si devices. This is due to the fast speed of the switching transients and the amount of high-frequency oscillatory behaviour that SiC-MOSFETs possess. The most expensive and highest performance state-of-the-art equipment which has been designed for use with WBG devices is required for low-current devices. However, as shown in Chapters 3 and 4, these are not required for the high-capacity SiC-MOSFET devices, with more budget-friendly options (in the range of 50–100 MHz bandwidth) proving to be sufficient.

7.3 Recommendations for Future Work

The Diverter

The Si/SiC hybrid switch is an intriguing area and should be considered for further investigations. The recommendations for future research in this area are summarised as follows:

1. Further investigations on the dynamic snubbering action and the ratio of Si–SiC die area.

2. Testing of the Diverter at higher current magnitudes, in the order of 1.5 kA as this is currently not achievable by a single SiC-MOSFET solution and is desirable for MW scale applications. Si-IGBTs which have been designed to significantly favour their on-state characteristics — often termed “long tail current devices” — should be considered.

3. Verification of the thermal stresses on the part-rated SiC-MOSFET by operating the Diverter in a continuous manner and monitoring device temperature and/or Temperature Sensitive Electrical Parameters (TSEP). Particular attention should be given to the high-frequency perturbations.

4. Integration of the Diverter into a converter system to further investigate the conduction assistance modes of operation and develop the required control systems.

5. A techno-economic assessment of a converter using the Diverter concept. This could be targeted towards a renewable application and set to follow the power profile of a wind turbine or large Photovoltaic (PV) system, both of which have large fluctuations in their operating set-point.

7.4 Impact of High-Power Double Pulse Test-Rig

The work that was carried out during this study has contributed to several publications and the advancement of various projects within the Power Electronics Research Group at the University of Edinburgh.

The high-power Double-Pulse Test Rig (DPTR) and the high-bandwidth testing platform which was developed has enabled the following research opportunities and contributions to knowledge:

1. The Si/SiC hybrid switching study covered in this thesis.

2. EPSRC projects — "Quietening ultra-low-loss SiC & GaN waveforms" and "High Current Module and Technologies Optimised for HVDC". It is envisaged that future funding proposals will also be strengthened by the UoE high-power DPTR platform.

3. Dissemination of the measurement techniques and required equipment for characterising the switching performance of SiC power devices to various companies at an EPSRC industry engagement event.

4. Industrial partnerships in the area of high-power WBG devices. One current project on 1800 A SiC-MOSFETs, supported by a £31,414 award from the EPSRC Impact Acceleration Account (IAA) and an industrial partner.

7.5 Publications Arising from this Thesis

Si/SiC Hybrid Switch for Improved Switching and Part-Load Performance

R.E. Mathieson, P.D. Judge, S. Finney

Control and Modelling for Power Electronics, IEEE COMPEL, November 2020

A Six Level Gate-Driver Topology with 2.5 ns Resolution for Silicon Carbide MOSFET Active Gate Drive Development

P.D. Judge, R.E. Mathieson, S. Finney

Electrical and Electromechanical Energy Conversion, ECCE Asia, May 2021

High-Current Hybrid Switch using Si-IGBT and Partially Rated SiC-MOSFET

R.E. Mathieson, P.D. Judge, M.M.C. Merlin, S. Finney

In Draft - Expected submission to IEEE Journal of Emerging and Selected Topics in Power Electronics

Gate Driving Strategy for Parallel Connected SiC MOSFET Modules for 1.6 kA

R.E. Mathieson, P.D. Judge, M.M.C. Merlin, S. Finney

In Draft - Expected submission to IEEE Transactions on Power Electronics

Automated Generic Gate-Voltage Profiling of High-Power SiC MOSFET Modules for Reduced Current/Voltage Oscillations and Overshoots

P.D. Judge, R.E. Mathieson, S. Finney

In Draft - Expected submission to IEEE Transactions on Power Electronics

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