A New Approach to the Design of CMOS Inductorless Common-gate Low-noise Amplifiers

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***Abstract*—This work proposes a new approach to design a simple and effective LNA reaching very competitive results in 1.2-V 65-nm standard CMOS technology. The proposed design uses a transconductance enhancement technique to achieve 2.3 dB of noise figure at the 5 GHz band. The paper exposes the advantages of a reduced number of devices in the circuit and analyses the topology. Simulations with complete technology models and statistical analysis are presented for more precise results.**

***Index Terms*—CMOS analog design, design strategy, inductorless, LNA, low-noise amplifier, single-ended, noise figure, transconductance-enhancement**

I. Introduction

The growing interest in applications of wireless communication and integrating the whole systems into a single chip leads to more demanding requirements of transceivers [1]. This causes that low-noise amplifiers (LNA), as the first block in the receiver chain, must guarantee a low Noise Figure (NF), while providing adequate input power matching, normally measured in terms of the reflection coefficient (S_{11}), and enough gain (G). Moreover, it should attain good linearity, typically referred by $IIP3$, and bandwidth described normally by the cut-off frequency (f_C) in wideband LNAs. Moreover, modern CMOS technology usually implies a limited headroom voltage.

As all those requirements should be maximized even having opposite dependencies, improving the trade-off is key for more-competitive LNAs. This is especially noticeable when the desired features are at the limit of achievable performance for certain CMOS technology.

This work proposes using simpler LNA topologies and focusing the effort on the optimization. Reducing the number of components allows the designer to spend more resources (voltage, power, area,...) on every single device, and, as consequence, better performance might be obtained in these scarce-resource conditions. Besides, the optimization process will be more reliable with a low number of elements. The decrease of complexity leads to more understandable analytical expressions and a greater similarity between simulation and low-order approach. In other words, the main design dependencies will be direct and clear, and, thus, the optimization methodology.

Therefore, simpler LNA topologies have the potential to be more effective, providing an equivalent performance after an easier and more consistent optimization process.

This paper is organized as follows. Section II describes the selection of the LNA topology. Section III provides a theoretical analysis. Section IV presents the optimization via simulation, Monte Carlo analysis and comparison with other LNA from literature. Finally, the main conclusions are drawn in Section V.

II. LNA Topology

An important issue designing inductorless LNAs is achieving an adequate input impedance (R_{in}), which must match source impedance (R_s). Normally, this implies that a feedback resistor or a common-gate (CG) stage is required [2]. However, both techniques present important disadvantages to overcome.

On the one hand, when dealing with an amplifier using resistive feedback, the relationship between the output resistance and the feedback resistor defines both input impedance and gain. Thus, matching impedances causes a severely limited voltage gain [2].

On the other hand, a simple CG stage can also present a matchable impedance to R_s. Nevertheless, the required transconductance (g_m) for this performance is high. However, as the main noise term is proportional to g_m, the resultant NF may be excessively high.

Fortunately, a g_m enhancement technique [3] can be used to maintain CG-stage transconductance while reducing the actual g_m of the matching transistor, and, thence, the noise without compromising input matching. In this technique, the input

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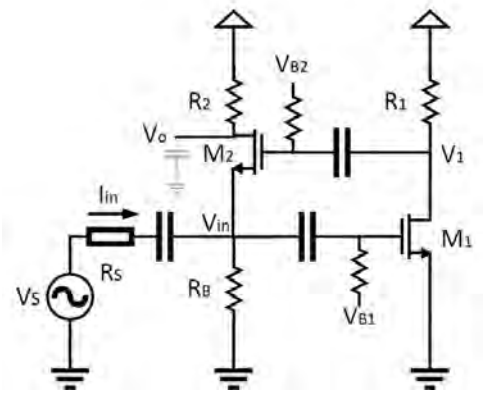


Fig. 1: Topology of the proposed LNA.

signal is inverted and applied to the CG gate to contribute to CG stage transconductance. This basic idea can be found in the literature in different topologies with [3] and without inductors [4].

Following the proposed strategy of minimizing the number of components, instead of complex or differential structures, the simplest single-ended implementation is selected: a common-source (CS) stage between source and gate of the CG transistor. As a result, the CG transconductance is boosted by CS gain plus one. Fig. 1 shows resultant circuit.

Besides, this configuration creates a negative feedback loop through $R_s//R_B$, the CS stage, and CG transistor, granting the intrinsic advantages of this kind of system to the circuit, such as stability. Furthermore, the reduction of the M_2 transconductance (g_{m2}) entails a decrease of M_2 size and, therefore, its parasitic capacitances. As a result, the value of R_2 can be increased to improve the LNA gain without jeopardizing bandwidth.

Alternatively, the noise-cancelling technique could be used to compensate for noise from CG [5]. However, it would imply more devices or differential output. Thus, it is neglected in this paper in favour of a simpler topology based on g_m-enhancement. Note that each technique implies different constraints among the devices. This results in very different sizing, even if the netlist (disregarding outputs) is the same [1].

Thus, in sum, the selected topology is a simple but effective single-ended LNA, capable of achieving very competitive performance in the state-of-the-art for 1.2-V 65-nm CMOS technology.

III. Theoretical Design-Oriented Analysis

The small-signal equivalent offers a first-order approach to the circuit constrains. Drain-source resistances are neglected by comparison, as well as voltage bias resistors. Similarly, decoupling capacitors can be considered short-circuits for the intention of the analysis.

Capacitance load is not considered for the expressions of impedance matching, noise figure, and gain as it has little impact on those specifications inside the bandwidth. However, cut-off frequency calculus does consider the parasitics, as it is a critical factor for it.

It is worth noting that R_B is required for a proper polarization of the CG stage, and it is larger than other resistors. This means that it can be neglected in some analytical expression under certain conditions while also reduces current from the supply.

A. Impedance Matching

The input impedance can be calculated from the relationship between the voltage v_{in} and the input current (i_{in}), this is:

$$R_{in} = \frac{1}{g_{m2}(g_{m1}R_1 + 1)}//R_B = \frac{1}{g_{m2}(A_1 + 1)}//R_B \quad (1)$$

where g_{m1} and g_{m2} are the transconductance of M_1 and M_2, respectively; and A_1 the gain of the CS stage.

As R_{in} must be equal to R_s for input adaptation, R_B, at least one order of magnitude larger, is negligible by comparison. Under those conditions, g_{m2} should be:

$$g_{m2} = \frac{1}{(g_{m1}R_1 + 1)R_s} = \frac{1}{(A_1 + 1)R_s} \quad (2)$$

In other words, as it was expected, g_{m2}, and therefore the source of the main noise, can be reduced by a factor of $A_1 + 1$ because of the CS stage.

B. Gain

From the small-signal model, circuit voltage gain is found as:

$$\frac{V_o}{V_{in}} = -\frac{R_2 g_{m2}(V_1 - V_{in})}{V_{in}} = R_2 g_{m2}(1 + R_1 \cdot g_{m1}) \quad (3)$$

Considering the condition of input impedance matching from (2), V_o/V_{in} will be:

$$\frac{V_o}{V_{in}} = \frac{R_2}{R_s} \quad (4)$$

Also, due to the input impedance adaptation, necessarily, $V_{in} = V_S/2$.

Thus, R_2 should be maximized to optimize the gain, although the actual value will be limited by its influence over the system bandwidth.

C. Cut-off Frequency

Frequency response is primarily defined by the main poles of CS and CG stages, which derive from the capacitance and resistance in nodes V_1 and V_0, respectively. However, as R_2 will be larger than R_1 to maximize gain; and parasitic capacitance in the output (due to the contribution of next stage) will be larger than it is V_1; Furthermore, the combination of R_2 and parasitic capacitances at the output node defines the most restrictive pole in the frequency response.

$$f_C \approx \frac{1}{2\pi R_2 C_{load}} \quad (5)$$

being C_{load} the parasitic capacitance due to the next stage and the connection with it.

D. Noise Calculation

The NF of the topology employing the proposed single ended output can be expressed as:

$$NF = 1 + \gamma g_{m1}(R_1 g_{m2})^2 R_s + \gamma g_{m2} R_s + R_1 g_{m2}^2 R_s + \frac{4R_s}{R_2} \quad (6)$$

where the second term comes from M_1, the third one from M_2 and fourth and fifth from resistors R_1 and R_2, respectively. γ is the bias-dependent channel thermal noise factor.

Besides, if the condition of input matching (2) is applied, (6) can be rearranged into:

$$NF = 1 + \gamma g_{m2}(R_1 + R_s) + g_{m2}^2 R_1 R_s (1 - \gamma) + \frac{4R_s}{R_2} \quad (7)$$

From (7), three noise terms are easily identified. Two of them have a dependency with g_{m2}, R_s and R_1, while the last one depends on R_s/R_2, thus, according to (4), it is inversely proportional to gain and highlights the interest in maximizing R_2.

The second and third terms show a clear advantage of reducing g_{m2} to improve NF. It could be noticed that R_1 has also a great impact on those terms. However, diminishing R_1 implies a reduction in CS-stage gain, and, therefore, it requires a larger g_{m2} due to (2).

Note that g_{m1} does not appear in (7) due to being defined by g_{m2}, R_1 and R_s in (2). For the same reason, g_{m1} should be maximized to decrease g_{m2}. However, power consumption, area or cut-off frequency will limit M_1 current and/or sizing. Besides, parasitics could have an impact on other specifications. For example, a large M_1 gate capacitance could alter input impedance.

IV. Simulation Results

Previous expressions provide initial values for the LNA. However, more precise models are required for optimization. The LNA is designed in 65-nm standard CMOS technology and complete BSIM4.6 MOS models supplied by the manufacturer for this technology are employed in the simulations. Parasitic load capacitance from the following stage is estimated at 50 fF from its layout level characterization. The target specifications are compatible with 5-GHz wireless LAN systems based on the IEEE 802.11a standard: $G >$ 17 dB, $NF <$ 2.5 dB, $S_{11} <$ -10 dB, $f_C >$ 5 GHz, $IIP3 >$ -11 dBm and $P <$ 8.5 mW.

The right balance between CG and CS stage conditions LNA performance. In other words, g_{m1} determines g_{m2} and vice versa. Due to this circularity, a simultaneous parametric analysis with both transistor widths is carried out to obtain the optimum pair. The result can be graphically depicted in terms of the desired specifications by an isograph. In that representation, the space of W_1-W_2 pairs that fulfil all specifications is the design window [6].

The rest of the available variables for the designer becomes the point of operation of the system, and they modify the shape or size of the design window. R_1, R_2, and R_B are set to 100 Ω, 450 Ω, and 600 Ω, respectively; bias voltages are selected to guarantee that transistors work in moderate inversion (which tend to present better performance than strong inversion [7]). Transistor length is selected to be the minimum available in the technology (60 nm) for a better trade-off between BW and NF.

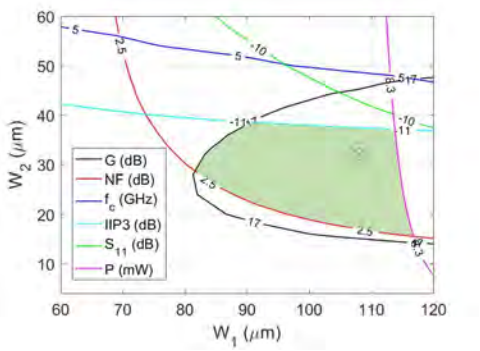


Fig. 2: Design window for transistor width. Each isoline represents a restriction from its corresponding specification.

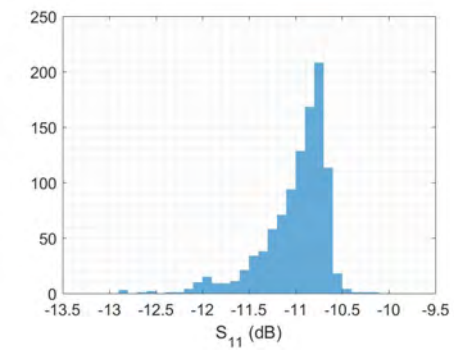
TABLE I: Monte Carlo Results (1024 samples)

	Best	Worse	Mean	Std Dev
NF @ 5 GHz	2.20 dB	2.68 dB	2.31 dB	71 mdB
S_{11} @ 5 GHz	-12.86 dB	-10.11 dB	-11 dB	362 mdB
S_{21} @ 5 GHz	17.78 dB	15.87 dB	17.15 dB	263 mdB
f_c	6.56 GHz	4.97 GHz	5.65 GHz	239 MHz
$IIP3$	-6.22 dBm	-15.05 dBm	-9.93 dBm	2 dBm

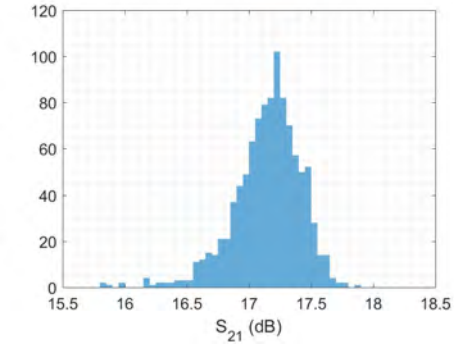
Fig 2 depicts the design window for the mentioned component values. Each curve is an isoline that corresponds with a specification limit. For example, all pairs at the red line produce an LNA with 2.5 dB of NF. Thus, the area enclosed by all the curves is the design window. A central point in the design window, more specifically $W_1 = 108\ \mu m$ and $W_2 = 32\ \mu m$, is selected to leave a margin for process variations and mismatch.

Also, a Monte Carlo analysis (1024 samples) is made to evaluate the robustness of the proposed strategy against random process variations. Table I shows the results of the simulations and Fig. 3 depicts histograms of S_{11}, S_{21} and NF. The designed LNA fulfil the specifications in all the samples. Unbalance due to process variation has some impact on NF (about 0.5 dB). However, the margin to the desired NF is wide enough and the deviation is lesser than other LNA topologies in the same technology.

Table II summarizes the results of the proposed LNA and gives a comparison with other LNA in similar CMOS technologies. Among all designs, the proposed LNA presents the lowest NF even considering the worst Monte Carlo samples. Besides, it is worth mentioning that the gain of the proposed LNA is not differential but single-ended. Also, this particularity implies that $IIP3$ will be lower: distortion will appear at a lower input power because single signal output



(a)



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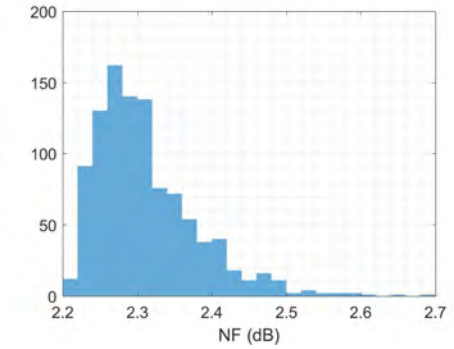

(c)

Fig. 3: Histograms for the proposed design from Monte Carlo analysis of (a) S_{11}, (b) S_{21}, and (c) NF.

TABLE II: Comparison of LNA Performance

Spec.	This work	[1]	[2]	[4]	[5]	[8]
Tech. (nm)	65	130	65	65	130	65
V_{DD} (V)	1.2	1.2	1.2	1.2	1.2	1.2
NF (dB)	2.3-2.6$^{\Diamond}$	3.8$^{\triangleright}$	2.9-5.9	4.0$^{\triangleleft}$	3.5	5$^{\triangleright}$
G (dB)	18*	16.6**	20**	20**	15.6**	20**
f_C (GHz)	5.6	2	10	2.7	5.2	7
S_{11} (dB)	-11	-10	-10	-10	-10	-6
$IIP3$ (dBm)	-9	-3.4	-11.2	-12	0	2
P (mW)	8	3	22	1.32	14	3.84

* Single-ended output ▷ De-embedded meas. ◊ Simulation results with
** Differential output ◁ Average meas. device variations and parasitics

power will be higher. Last, but not least, this work LNA uses a minimum number of devices. Thus, obtaining the final design values should be is much more simple when compared to others.

V. Conclusions

In 65-nm standard CMOS technologies, simple topologies of inductorless LNA are capable of achieving very competitive performance, thanks to being able to dedicate more of their limited resources (voltage headroom, current,...) to each device. The design process can also be done even in a shorter time than a more complex structure.

However, the key to obtaining good trade-off among the conflicting specifications is the optimization process. The simpler the topology is, the more reliable and achievable the optimization will be.

Also, most of LNAs are based on an adequate balance between two parts. This is the case of g_m-enhanced as well as noise cancelling. Thus, simpler design ease identifying two main variables to control the two parts of the LNA.

Paradoxically, this simple design requires a complex model of the transistors for improving results from the a priori expected performance. Several second- and third-order effects have a noticeable impact on all the specifications, hindering obtaining a design window without simulations with the technology models. Indeed, the NMOS moderate inversion region seems to provide better results for this topology than the traditional polarization in strong inversion.

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