DYNAMIC DAMPING IN OPTICAL RECEIVERS

Pouria Aminfar

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By: **Pouria Aminfar**

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Signed by the final examining commitee:

_____ Chair

Dr. Rabindranath Raut

_____ Examiner

Dr. Rabindranath Raut

_____ Examiner

Dr. Brandon W. Gordon

_____ Supervisor

Dr. Glenn Cowan

Approved _____

Dr. Yousef R. Shayan, Chair of Department

July 21

_____ 20 ____ _____

MOURAD DEBBABI, Ph.D., P.Eng., Dean

Faculty of Engineering and Computer Science

Abstract

Dynamic Damping in Optical Receivers

Pouria Aminfar

Today's telecommunications involves ever-increasing amounts of optical communication. Besides being an important component of the long-haul network, optical communications are also being used in data centers, circuit boards, integrated circuits, and the next generation of mobile networks. This thesis proposes an optical receiver in which the damping factor of both the transimpedance and post amplifiers is modulated synchronously with incoming data. Modulation of the damping factor allows the fast response of the low-damping factor while mitigating the intersymbol interference (ISI) associated with underdamped systems.

To investigate the modulated damping shunt-feedback transimpedance amplifier (SF-TIA), some methods, including switching the feedback resistor and modulating the damping factor by a sine wave, are used. Due to damping factor value limitation by changing the shunt-feedback and complexity of producing appropriate value of the sine wave with proper DC offset, amplitude and phase, damping factor modulation by a rail-to-rail square wave signal is presented where only phase adjustment is necessary and has better noise performance, Vertical Eye Opening (VEO) gain and gain to power ratio.

The extension of dynamic damping to the post amplifier is investigated through simulation at 10 Gb/s. A shunt-feedback TIA with cross-coupled inverters at the output, optimized to reach minimum input-referred noise is used as a reference for creating SF-TIA and Cherry-Hooper post-amplifier (CH-PA) blocks. By modulating the damping factor in both blocks, the proposed system achieves more than three times the VEO and lower input-referred noise compared to the optimized reference. Alternatively, an equal-gain modulated system has 40 % lower power consumption compared to the reference design.

Acknowledgments

First and foremost, I would like to express my appreciation to my supervisor Prof. Glenn Cowan (Concordia University, Montreal, Canada) for his expert knowledge, patience, and motivation throughout my study and research. I am so grateful for the opportunity he gave me to do this research on the optical receivers.

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I would like to acknowledge Canadian Microelectronic Corporation (CMC) Microsystems for providing access to CAD tools and Quebec's Microelectronics Strategic Network (ReSMiQ) for financial support. I also thank Ted Obuchowicz for CAD support.

I am deeply indebted to many people for my success. I pay my sincerest gratitude to my parents, my sister Narges and my partner Elnaz for the love and inspiration they've shown me through this thoughtful journey. This wonderful step in my life would not be possible without them.

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List of Abbreviations

BER Bit error rate
BW Bandwidth
CDR Clock-and-data recovery
CH-PA Cherry-hooper post-amplifier
CML Current-Mode Logic
CMOS Complimentary metal oxide semiconductor
Gb/s Giga-bit per Second
ISI Inter-symbol interference
LD Laser diode
LTI Linear time invariant
LPTV Linear periodically time-varying
MOSFET Metal-oxide semiconductor field effect transistor
NMOS n-channel MOSFET
PD Photodiode
PDS Power spectral density
PMOS p–channel MOSFET
PP Power penalty
rms Root mean squared
RX Receiver
SF-TIA Shunt-feedback transimpedance amplifier
SNR Signal-to-noise ratio
TX Transmitter
UI Unit interval
VEO Vertical eye opening

Chapter 1

Introduction

Nowadays, high-speed optical systems and electronic devices are increasingly required by telecommunication networks due to the increasing volume of data [1]. An optical communication system relies on light in order to carry large amounts of data all over the place [2]. In fact, the idea of using light to transmit signals first emerged more than a century ago. Researchers proposed using optical fiber as a means to propagate light in the mid-1950s. [3].

Electrical systems typically end up at each end of an optical link, so the optical signal must be converted from electrical to optical and back again. Through the use of a photodiode, the optical signal received by the optical/electrical interface is converted into a current, which is then amplified by the analogue frontend circuit. Specifically, this work is concerned with this receiver front-end.

In frontend circuit design, one of the challenges is the need to deal with increasingly high data rates. At a circuit level, the frontend is typically required to higher analogue bandwidth to handle higher data rates. Extending bandwidth can often be achieved through the use of a number of methods that have limited capability and may lead to a worse dynamic response, overshoot, and ringing [4].

In this work, we propose the new optical receiver front-end design method to increase the front-end's effective gain and dissipate lower power without limitations of low intrinsic BW systems and poor time response of extendend BW systems. By per-UI damping-factor modulation in optical receiver front-ends, focusing on the transimpedance amplifier design at first and extending this method to the post-amplifier, we can take advantage of both low damping factor systems (high-speed system) and

high damping factor systems (low ISI) simultaneously in one system.

1.1 Optical communication systems

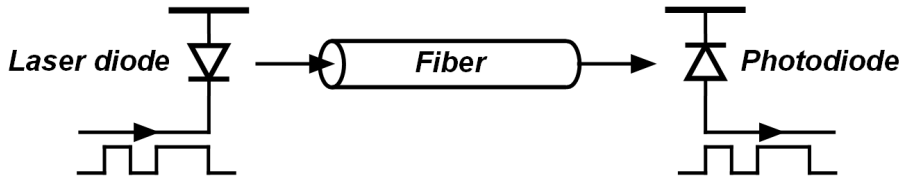


Figure 1.1: An ideal optical communication system (TX + Channel + RX)

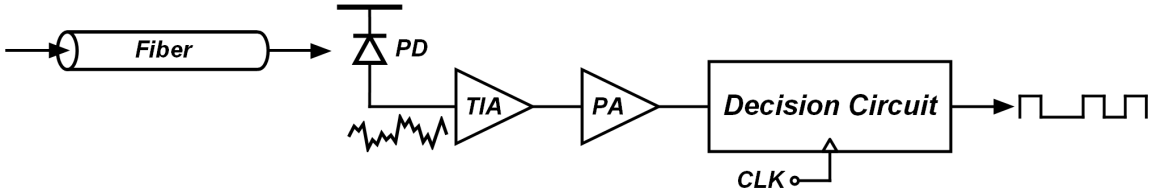


Figure 1.2: A simplified optical receiver (RX)

A simple optical communication system consists of three components [5]:

- An electro-optical transmitter which generates optical signals from electrical data (near end)
- A fiber which carries the light consisting of data
- A receiver including a photodetector which senses the light at the end of the fiber and converts it to an electrical signal (far end)

Fig. 1.1 shows an ideal optical system including all three required components. For long-distance communications, the signal experiences attenuations and dispersion by traveling in the fiber. However, by adding a high gain laser driver, the generated light by the LD has higher intensity; still, more amplification at the receiver side front-end is needed. A simplified optical receiver is shown in Fig. 1.2, including a photodiode, a transimpedance amplifier followed by a post-amplifier and a decision circuit to generate digital outputs.

Input current incoming from the photodiode (PD) is converted by a transimpedance amplifier (TIA) to a voltage to be applied to a decision circuit such as a sense-amplifier based latch. The small input current generated by the PD and the inherent gain-bandwidth trade-off of the TIA usually require additional stages of PA, such as Cherry-Hooper (CH) post-amplifiers between the TIA and the decision circuits to obtain additional gain [6], [7].

1.2 Optical receiver front-ends

This thesis focuses entirely on the analog frontend of optical receiver. The important specification which we are looking at is the effective gain or vertical eye opening (VEO) gain of the system. The effective gain of the system, Z_{VEO}, is calculated as the ratio between the output VEO voltage and the peak-to-peak input current signal in the unit of ohms (Ω). For the transistor-level design of the front-end, the components are optimized for minimum input-referred noise current and high effective gain, besides considering the overall power consumption of the optical receiver front-end.

1.2.1 Transimpedance Amplifier (TIA)

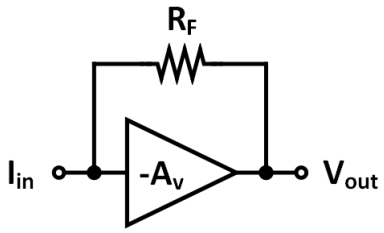


Figure 1.3: Shunt-feedback transimpedance amplifier (SF-TIA) topology

The generated current by the photodiode (PD) from attenuated input light at the receiver needs to be amplified and converted to a voltage. The transimpedance amplifier (TIA) gain is in ohms (Ω) unit, which means the ratio of the output voltage to the input current.

A common TIA topology is shown in Fig. 1.3, an inverter-based TIA, with an inverting voltage amplifier and a shunt-feedback resistor. Different performance characteristics are obtained by using different amplifier topologies. Using inverter-based

TIA gives us both advantages of lower input and output resistance with the ratio of $1 + A_v R_F$, providing a fast and high output driving capability compared to the open-loop TIAs [5].

The main issue in shunt-feedback TIA design is the trade-off between the bandwidth (BW), noise and gain. In this work, we increase the effective gain of the TIA and lower the input noise current without bothering inadequate time response and ringing.

1.2.2 Post-Amplifierr (PA)

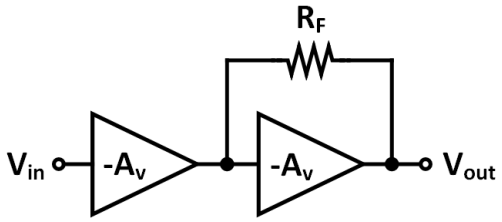


Figure 1.4: Cherry-hooper post-amplifier (CH-PA) topology

Having the small input current generated by the PD and the typical gain of the TIA usually give rise to using additional stages of post-amplifiers (PAs) between the TIA and the decision circuits to obtain larger gain [6]. Due to the inherent gain-bandwidth trade-off of the TIA, it may be challenging to obtain sufficient gain; thus, a PA, a voltage-to-voltage amplifier, produces extra gain. Fig. 1.4 shows a cherry-hooper post-amplifier which is one the common post-amplifiers used in the optical receiver [7].

The proposed method of TIA design is extended to the post-amplifier and increases the overall front-end gain by more than 3x, and the overall sensitivity of the front-end is improved.

For the rest of this thesis, we will mainly focus on shunt-feedback transimpedance amplifier (SF-TIA) and cherry-hooper post-amplifier (CH-PA) circuit design.

1.3 Objectives

We first investigate a new TIA design method that incorporates modulated damping factors in order to realize our proposed idea. In a 2^{nd}-order TIA, by shifting poles

of the system to the right half plane during a portion of the unit interval (UI), regeneration gives rise to a larger effective gain. And, during another portion of UI, increasing the damping factor mitigates the intersymbol interference (ISI) associated with the underdamped system.

After observing the advantage of using the new method, fast response and low ISI system, modulation is applied to the post-amplifier in the next step. And finally, the complete receiver, including blocks of shunt-feedback transimpedance amplifier, cherry-hooper post-amplifier, DC and offset compensation and decision circuit blocks, is designed and simulated.

This work demonstrates that:

- By modulating the damping factor with a sinusoidal signal, the TIA achieves more than twice the VEO gain and net improvement in receiver sensitivity for reasonable output voltage swing requirements (25 mV) compared to a reference circuit [8].

- Modifying the modulation signal to a rail-to-rail square wave removes the complexity of generating a sine wave with appropriate DC offset, amplitude, and phase. While a square wave only needs phase adjustment, TIA reaches higher VEO gain and lower input-referred noise [9]

- The extension of dynamic damping design method to the post-amplifier gives rise to more than three times the gain and the Gain/Power ratio compared to the reference. In addition, it is shown that the modulated damping system with the same gain compared to the reference design dissipates 40 % less power [10].

To illustrate the effectiveness of these approaches, a differential shunt-feedback TIA is optimized to reach its minimum input-referred noise current, with and without cross-coupled inverters across the output as reference designs. Furthermore, the same circuit design is used for the Cherry-Hooper post-amplifier schematic to investigate the advantage of damping factor modulation in both TIA and post-amplifier. The results of the modulated TIA and post-amplifier designs are compared to the reference design to illustrate the improvement.

1.4 Contributions and publications

This work presents the per-UI damping-factor modulation in optical receiver front-ends, focusing on a shunt-feedback transimpedance amplifier and Cherry-Hooper post-amplifier to take advantage of both low and high damping factor systems where this design approach was not previously used.

In particular:

- By replacing the modulation signal with a square wave, alongside optimizing the size of transistors, only the initial phase of the modulation signal compared to the incoming data needs alignment.

- For small input currents, the system is considered a linear periodically time-varying (LPTV) system and time-varying operating point varies the output noise over each UI. Therefore, conventional AC noise analysis is not applicable. In design chapters, transient noise analysis is used to obtain noise performance of the LPTV system. In a separate chapter, it is shown that the new method of noise analysis provided in [11] gives us the same results as transient noise simulation for a modulated damping system.

- Despite the unconventional eye diagram at the output of the modulated damping TIA, this system is compatible with a convention cherry-hooper post-amplifier. As well, modulation can be added to the PA to obtain higher gain or lower power dissipation.

Two published and one accepted for publication conference papers related to this thesis:

- P. Aminfar and G. Cowan, "Multi-Stage Damping Factor Modulation in Optical Receiver Front-Ends," *Accepted to 2021 IEEE 64rd International Midwest Symposium on Circuits and Systems (MWSCAS)*, Springfield, MA, USA, 2021.

- P. Aminfar and G. Cowan, "Square-Wave Modulated Damping in Transimpedance Amplifiers," *2020 IEEE 63rd International Midwest Symposium on Circuits and Systems (MWSCAS)*, Springfield, MA, USA, 2020, pp. 691-694.

- P. Aminfar and G. Cowan, "Dynamic Damping in Transimpedance Amplifiers," *2020 IEEE International Symposium on Circuits and Systems (ISCAS)*, Seville, Spain, 2020, pp. 1-5.

1.5 Thesis organization

Chapter 2 reviews background related to the theory of pulse response and output eye-opening of second-order systems. Also, the damping factor of 2^{nd} order systems and modulation, inverter-based TIA and cherry-hooper post-amplifier are explained briefly.

Chapter 3 presents the transistor-level implementation of the shunt-feedback transimpedance amplifier and shunt-feedback TIA with cross-coupled inverters at the output.

Damping factor modulation using different methods by sine and square wave signal is shown in Chapter 4.

Chapter 5 examines noise analysis of linear periodically time-varying (LPTV) systems where conventional AC noise analysis is not applicable.

The compatibility of the new TIA design with conventional cherry-hooper post-amplifier and extension of the damping factor modulation to the post-amplifier is presented in Chapter 6.

Chapter 7 then presents and discusses overall chip design and simulations.

Finally, Chapter 8 summarizes and concludes the investigation of the damping factor modulation in optical receiver front-ends.

Chapter 2

Background and literature review

This chapter provides an overview of the necessary background for the studies conducted in the subsequent chapters. It gives a brief overview of relevant recent literature in the same and related areas. At first, we will provide definitions of damping factor and vertical eye-opening in 2^{nd}-order systems in the subsequent section. In particular, we will review the background and literature for the pulse response, eye diagram of a system; then, we introduce the vertical eye opening gain as an effective gain of the system and the input-referred noise current and its definition in our work. Next, we will look at the damping factor modulation theory in 2^{nd}-order systems and enlarge the system's output vertical eye-opening. The subsequent sections give an overview of the shunt-feedback transimpedance amplifier (SF-TIA) and cherry-hooper post-amplifier (CH-PA) schematics and transfer function parameters. Finally, in the last two sections, transient noise analysis and sensitivity calculations are discussed.

2.1 Pulse response and vertical eye opening

In communication systems, bandwidth limitation can give rise to intersymbol interference (ISI). Therefore contrary to the ideal channel, the symbol at one decision point is influenced by the symbols transmitted in previous and future symbols. If it is assumed that our system is 1^{st}-order, the transfer function of the system, $H(s)$, is given by

$$H(s) = \frac{\omega_0}{s + \omega_0} \tag{2.1}$$

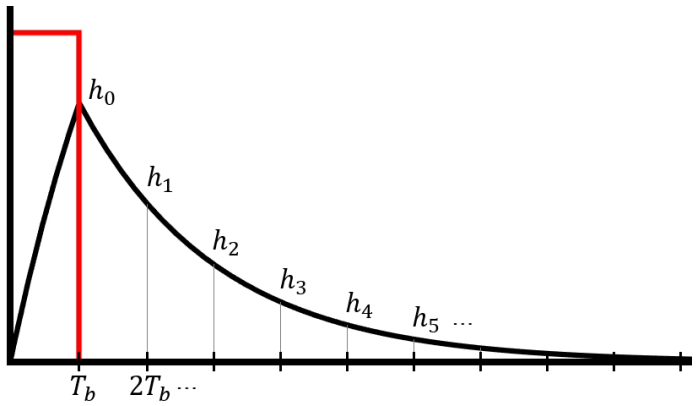


Figure 2.1: 1st-order system response to an unit-pulse input signal

The random input signal, $x(t)$, can be written as

$$x(t) = \sum_{k=-\infty}^{\infty} d_k r(t - kT_b) \tag{2.2}$$

Where $r(t)$ is a rectangular pulse lasting one UI and d_k represents the k$^{\text{th}}$ transmitted bit, which can have the values of "1" or "0". The input unit-pulse, $r(t)$, corresponding to the unit interval of T_b using the unit-step function ($u(t)$) is given by

$$r(t) = u(t) - u(t - T_b) \tag{2.3}$$

The response of a system to the unit step signal is referred to as the unit-step response, denoted as $v(t)$. Based on the time-invariant system theory, the unit-pulse response of the system can be written as

$$h_{UI}(t) = v(t) - v(t - T_b) \tag{2.4}$$

For a Linear Time-Invariant (LTI) system if we know the unit-step response of the system $v(t)$, we can find the unit-pulse response of the system $h_{UI}(t)$ as s subtraction of shifted $v(t)$ [13]. The step response of the system with the transfer function of $H(s)$ is given by

$$V(s) = \frac{1}{s}H(s) = \frac{1}{s}\frac{\omega_0}{s + \omega_0} = \frac{1}{s} - \frac{1}{s + \omega_0} \tag{2.5}$$

In the time domain, the step response becomes

$$v(t) = (1 - e^{-\omega_0 t})u(t) \tag{2.6}$$

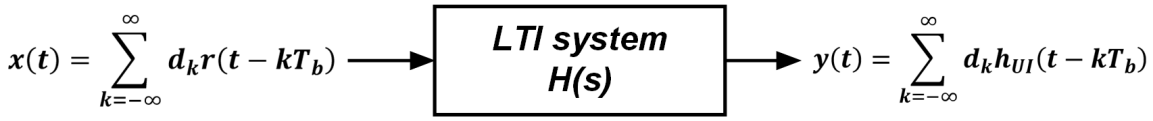


Figure 2.2: Relation between a random pulse signal input and output of a Linear Time-Invariant (LTI) system [13]

From the time of 0 to T_b, the pulse response of the system is evaluated by Eq. (2.6). After T_b, when input pulse is zero

$$v(t) - v(t - T_b) = (1 - e^{-\omega_0 t}) - (1 - e^{-\omega_0 (t - T_b)}) = e^{-\omega_0 (t - T_b)}(1 - e^{-\omega_0 T_b}) \tag{2.7}$$

Therefore, the unit-pulse response of the system becomes

$$h_{UI}(t) = \begin{cases} 1 - e^{-\omega_0 t}, & 0 \leq t < T_b \\ (1 - e^{-\omega_0 T_b}) e^{-\omega_0 (t - T_b)}, & t \geq T_b \end{cases} \tag{2.8}$$

Fig. 2.1 shows a 1st-order system response to an input of a unit-pulse signal lasting one UI of T_b. The main cursor is the maximum value of the pulse response and denoted by h_0.

As shown in Fig. 2.2, if we know $h_{UI}(t)$, we can find the output of the system with a random input signal $x(t)$, shown in Eq. (2.2), as a summation of shifted and scaled instances of $h_{UI}(t)$:

$$y(t) = \sum_{k=-\infty}^{\infty} d_k h_{UI}(t - kT_b) \tag{2.9}$$

If we assume that there is no ISI and mid-band gain of the system is one, a transmitted one leads to a value of $y(t) = h_0$, and a transmitted zero leads to a value of $y(t) = 0$. The midpoint between the zero and one signal values or 0.5 is the decision threshold. Fig. 2.3 (a) shows an eye diagram with modest ISI. To compute the worst-case ISI, we assume all combinations of transmitted bits are possible. The ISI from preceding and following bits can degrade a given main cursor. Therefore, the ISI_{MAX} becomes

$$ISI_{MAX} = \sum_{k \neq 0} |h_k| \tag{2.10}$$

If we assume that the signal will be processed without further equalization to remove ISI, the vertical eye opening (VEO) is the most important amplitude metric in optical receivers, called the effective gain of the system. The VEO is computed as

$$VEO = h_0 - ISI_{MAX} \tag{2.11}$$

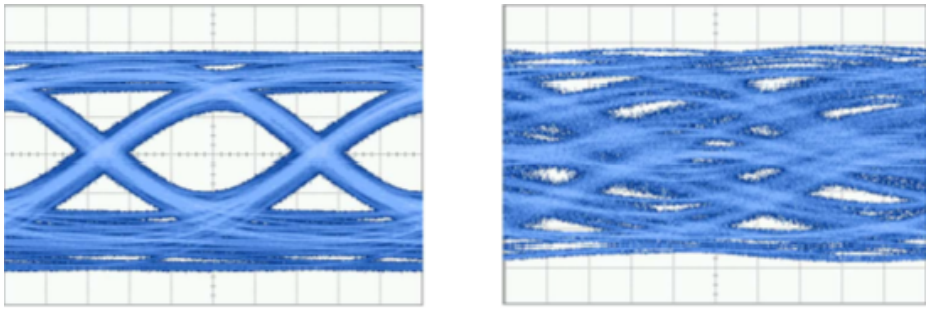


Figure 2.3: Real eye diagrams (a) with modest ISI, (b) with severe ISI [14]

An eye diagram with severe ISI is shown in Fig. 2.3 (b) where introduced ISI is large and the eye is completely closed.

2.2 VEO gain and input-referred noise current

In the rest of this work, to design transistor-level implementation of the systems, input-referred noise current calculation is done by referring the output noise voltage to the input using the effective gain of the TIA, following the approach in [12]. Since the front-end may introduce ISI, but has no follow-on equalization, the effective gain, Z_{VEO}, is the ratio between the output VEO voltage and the peak-to-peak input current signal in units of ohms (Ω).

$$Z_{VEO} = \frac{VEO}{I_{in,pp}} \tag{2.12}$$

Therefore, input-referred noise current, defined as referring the rms value of the output noise voltage to the input using the effective gain of the front-end, is computed as:

$$I_{n,in} = \frac{V_{n,out}}{Z_{VEO}} \tag{2.13}$$

where $I_{n,in}$ is the rms value of the input-referred noise current, $V_{n,out}$ is the rms of output noise voltage and Z_{VEO} is the effective gain of the system defined in Eq. 2.12.

2.3 Second-order system

A second-order system based on two integrators is shown in Figure 2.4. It has two integrators, each with transfer function $\frac{\omega_0}{s}$ and overall feedback b_0 and local feedback

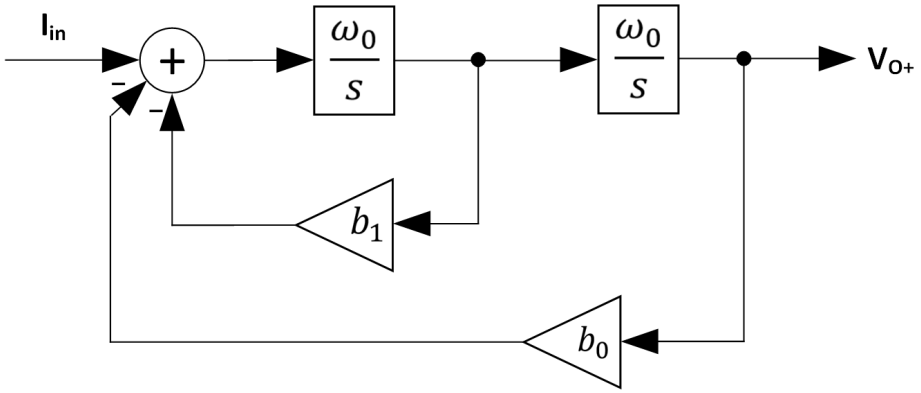


Figure 2.4: A 2nd-order system model

b_1. The overall transfunction is:

$$A(s) = \frac{\omega_0^2}{s^2 + b_1\omega_0 s + b_0\omega_0^2} \tag{2.14}$$

To find the parameters of the transfer function, We can rewrite Eq. 2.14 as

$$A(s) = \frac{1}{b_0}\frac{b_0\omega_0^2}{s^2 + b_1\omega_0 s + b_0\omega_0^2} = \frac{1}{b_0}\frac{\omega_n^2}{s^2 + 2\zeta\omega_n s + \omega_n^2} \tag{2.15}$$

Therefore, the transfer function has the following parameters:

$$A_{dc} = \frac{1}{b_0} \tag{2.16}$$

$$\omega_n = \omega_0\sqrt{b_0} \tag{2.17}$$

$$\zeta = \frac{b_1}{2\sqrt{b_0}} \tag{2.18}$$

where ω_n is the natural frequency and ζ is the damping factor.

As an example to explore the response of a LTI 2nd-order system to random data and its output eye diagram, the global gain b_0 was set to $\frac{1}{40}$ giving a low-frequency gain of 40. With $\omega_0 = 2\pi\ Grad/s$ the system has a natural frequency of 1 $Grad/s$. In order to have a damping factor $\zeta = 1/\sqrt{2}$ using Eq. 2.18, $b_1 = \sqrt{2b_0} = \sqrt{\frac{1}{20}} = 0.224$. With this damping factor, the 3dB bandwidth of the system is equal to natural frequency, $\omega_{3dB} = \omega_n$. In Hz, this corresponds to only $158MHz$. The system was investigated for random binary input data with a unit interval (UI) of 2 ns corresponding to 0.5 $Gbps$. The output eye diagram of the system is shown in Fig 2.5. The bandwidth of the system is only 31.6% of the input data rate, giving rise to significant intersymbol interference (ISI) and eye closure (small VEO). As a solution, the bandwidth could be

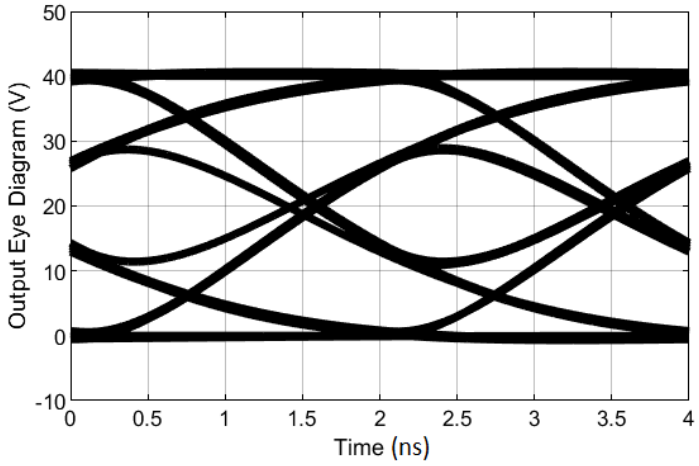


Figure 2.5: Output eye diagram of the 2[nd]-order LTI system (Fig. 2.4), $\omega_0 = 2\pi\ Grad/s$, $b_0 = 1/40$, $b_1 = 0.25$, $f_{bit} = 0.5\ Gb/s$

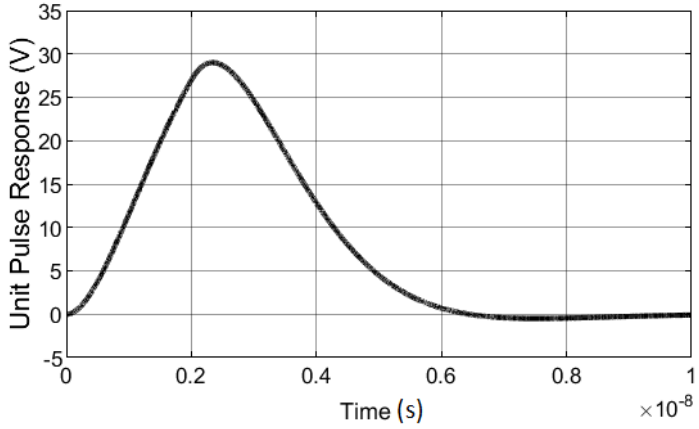


Figure 2.6: The pulse response of the 2[nd]-order LTI system (Fig. 2.4), $\omega_0 = 2\pi\ Grad/s$, $b_0 = 1/40$, $b_1 = 0.25$, $f_{bit} = 0.5\ Gb/s$

increased by lowering the gain (through b_0). As an example, doubling the bandwidth to a target bandwidth of 63.2 % of the data rate would require $b_{0,new} = 4\ b_{0,old}$ giving a dc gain of only 10. This trade-off between gain and bandwidth is consistent with that predicted in the "Transimpedance Limit" [15].

If the damping factor of the system is reduced, the step and pulse responses of the system will have overshoot, giving rise to high value of ISI and eye closure. Eq. 2.18 shows that reducing the b_1 gives rise to damping factor reduction. $b_1 = 0$ corresponds to an ideal oscillator with poles on the $j\omega$ axis whereas $b_1 < 0$ gives poles in the right-half plane. Although amplifiers go unstable with such pole locations, we

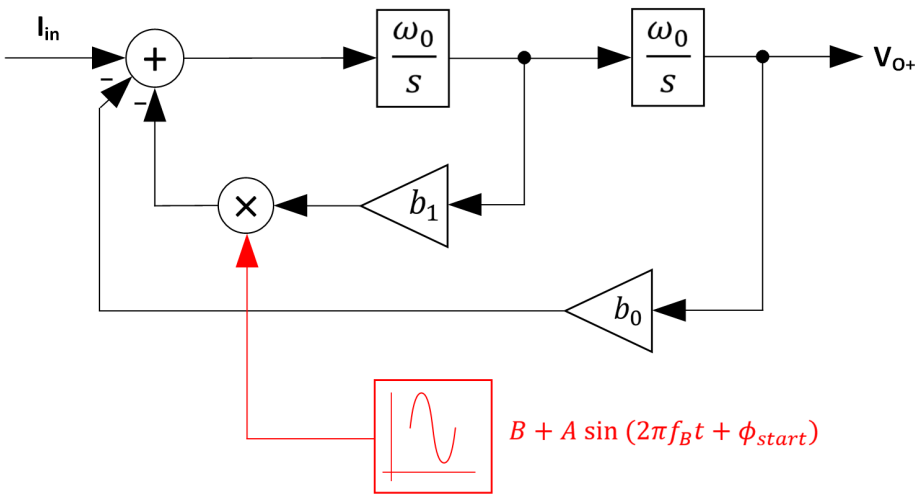


Figure 2.7: A 2nd-order system model with damping factor modulation by a sinusoidal wave signal

routinely move poles into the right-half plane in regenerative circuits such as high-speed latches [16].

To obtain the response of the 2nd-order system to a unit-pulse signal, defined by Eq. 2.3, roots of the transfer function are calculated

$$\begin{cases} r_1 = (-\zeta + \sqrt{\zeta^2 - 1})\omega_n \\ r_2 = (-\zeta - \sqrt{\zeta^2 - 1})\omega_n \end{cases} \tag{2.19}$$

Then, to compute the unit-step response of the system in the s-domain we have

$$b_0 V(s) = \frac{1}{s}A(s) = \frac{1}{s}\frac{\omega_n^2}{s^2 + 2\zeta\omega_n s + \omega_n^2} = \frac{1}{s} - \frac{r_2}{r_2 - r_1}\frac{1}{s - r_1} + \frac{r_1}{r_2 - r_1}\frac{1}{s - r_2} \tag{2.20}$$

Therefore, the step response of the system in the time domain becomes

$$v(t) = \frac{1}{b_0}(1 - \frac{r_2}{r_2 - r_1}e^{r_1 t} + \frac{r_1}{r_2 - r_1}e^{r_2 t}) \tag{2.21}$$

Using Eq. (2.4) and Eq. (2.21), the unit-pulse response of the 2nd-order system can be writen as

$$h_{UI}(t) = \begin{cases} \frac{1}{b_0}(1 - \frac{r_2}{r_2 - r_1}e^{r_1 t} + \frac{r_1}{r_2 - r_1}e^{r_2 t}), & 0 \le t < T_b \\ \frac{1}{b_0}\left(\frac{r_2(1 - e^{r_1 T_b})}{r_2 - r_1}e^{r_1(t - T_b)} - \frac{r_1(1 - e^{r_2 T_b})}{r_2 - r_1}e^{r_2(t - T_b)}\right), & t \ge T_b \end{cases} \tag{2.22}$$

Fig 2.6 shows the pulse response of the system for a unit-pulse signal. In this simulation, the input unit-pulse signal lasts from 0 to 2 ns. For the pulse response of

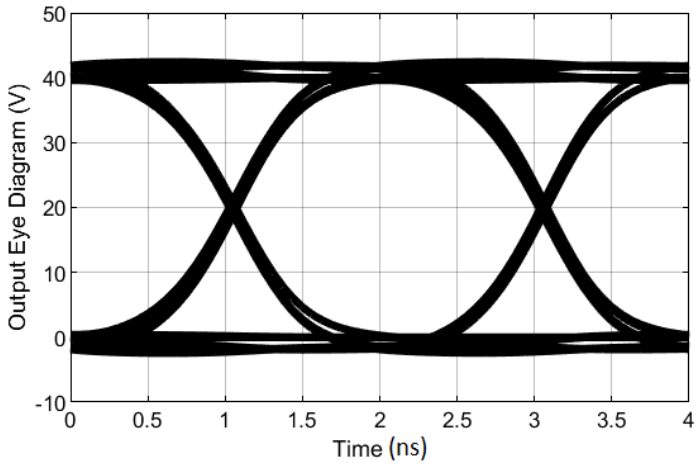


Figure 2.8: Output eye diagram of the 2nd-order LPTV system (Fig. 2.7), $A = 1.825$, $B = 1$, ϕ_{start}= 2.67, $\omega_0 = 2\pi\ Grad/s$, $b_0 = 1/40$, $b_1 = 0.25$, $f_{bit} = 0.5\ Gb/s$

the LTI system, the output pulse response of the LTI system increases and reaches a peak value of about 29 at the sampling time of 2.5 ns and then decreases to 0 over about 1.5 UI. Using Eq. 2.10, the maximum value of the ISI is computed as

$$ISI_{MAX} = \sum h_{-1} + h_1 + h_2 = 4 + 8.5 + 0.5 = 13 \tag{2.23}$$

Eq. 2.11 gives the VEO

$$VEO = 29 - 13 = 16 \tag{2.24}$$

which has the same result compared to the VEO observed in Fig. 2.5.

2.4 Dynamic Damping Factor in 2nd-order systems

The presented model in Fig. 2.7 is now investigated to modulate the damping factor of the 2nd-order system with a sinusoidal input to the multiplier. The modulation signal $m(t)$ is defiend as

$$m(t) = B + A\ sin(2\pi f_{bit} + \phi_{start}) \tag{2.25}$$

Through B, A and ϕ_{start} parametric sweeps that varied the dc offset, amplitude and initial phase of the sinusoidal excitation respectively, a wider eye-opening was found, as shown in Figure 2.8. The particular values were a dc offset of 1, an amplitude of 1.825 and an initial phase of 2.67 rad. Notice that the peak values of the output are

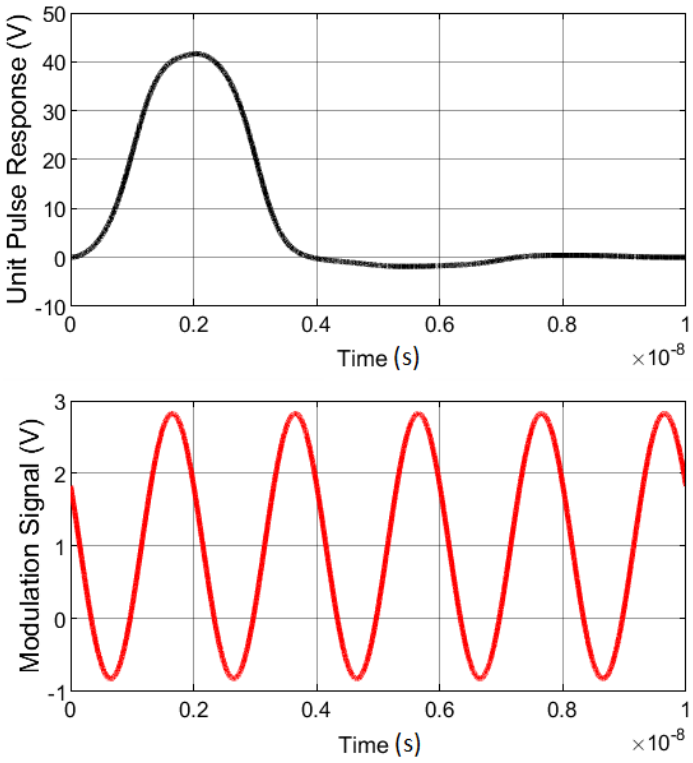


Figure 2.9: The pulse response of the 2nd-order LPTV system (Fig. 2.7), $A = 1.825$, $B = 1$, ϕ_{start}= 2.67, $\omega_0 = 2\pi$ $Grad/s$, $b_0 = 1/40$, $b_1 = 0.25$, $f_{bit} = 0.5$ Gb/s

still clustered around 0 and 40. We are not increasing the AC gain, but only adjusting the damping over a range set by:

$$(B - A)\ b_1 \leq b_1(t) \leq (B + A)\ b_1 \tag{2.26}$$

where A is the amplitude and B is the dc offset of the sinusoid, b_1 is the static value in the feedback path and $b_1(t)$ is the time-varying gain. For our values, this corresponds to $-0.825\ b_1$ to $1.825\ b_1$. Having the values of $b_0 = 0.025$ and $b_1 = 0.224$ with Eq. 2.18 give us the sweep range of damping factors from -0.58 to 1.29.

The results in Fig. 2.8 show an increase in vertical eye opening from about 16 units to 40 units. This comes without changing the unity-gain frequency of the integrators, the main system parameter that would be limited by the finite f_T of a transistor technology used to implement an amplifer. Instead the feedback gain was modulated over a modest range. For small input currents, the system is considered a *Linear* Periodically Time-Varying (LPTV) system.

To gain further insight into what is happening, Fig. 2.9 shows the pulse response of the LPTV system and the modulation signal. In this system, reduction of the

damping factor by the sine wave modulation signal, when the output signal is rising, changed the system to a fast response system. After one UI, while the output reaches to peak calue of 40, the low frequency gain of the system, the damping factor of the system increases to a high value to prevent ringing associated with the underdamped system. Then, the damping factor returns to the low value, and the output decreases to zero below one UI. Here, by modulating the damping factor of the system, pulse response of the system has no pre-cursor and post-cursor ISIs, therefore the value of the ISI_{MAX} is equal to 0. The Eq. 2.11 computes the VEO as

$$VEO = h_0 = 40 \tag{2.27}$$

which has the same result compared to the obtained value of the VEO showed in Fig. 2.8.

2.5 Inverter-based transimpedance amplifier

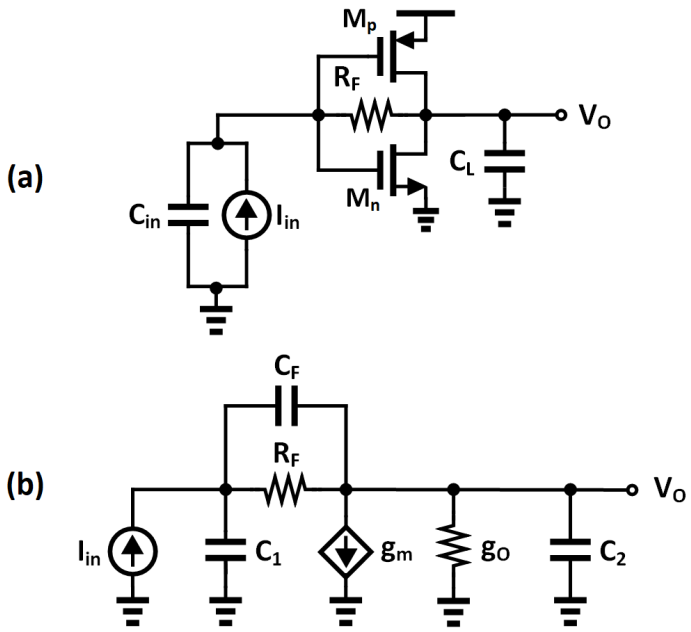


Figure 2.10: An inverter-based shunt-feedback TIA [5] (a) transistor-level schematic (b) AC small-signal model

Fig 2.10 (a) shows an inverter-based TIA formed by a CMOS digital inverter with a feedback resistor to bias the TIA and operate as an amplifier. This topology

is similar to the common-source shunt feedback TIA but using both NMOS and PMOS transistors provides greater overall transconductance and thus higher gain with the same amount of bias current and power consumption since the two transistors contribute to g_m value of the amplifier [17]. The input-referred noise is also low in these transimpedance amplifiers [18].

To compute the frequency response of the TIA, the AC small-signal model of the circuits is shown in Fig. 2.10 (b). Component parameters are as follows:

$$g_m = g_{m,n} + g_{m,p} \tag{2.28}$$

$$g_o = g_{o,n} + g_{o,p} \tag{2.29}$$

$$C_1 = C_{gs,n} + C_{gs,p} + C_{in} \tag{2.30}$$

$$C_2 = C_{db,n} + C_{db,p} + C_L \tag{2.31}$$

$$C_F = C_{gd,n} + C_{gd,p} \tag{2.32}$$

The transfer function of the circuit from input small-signal current to the output voltage is given by

$$\frac{V_o}{I_{in}} = \frac{(R_F C_F s + 1 - g_m R_F) R_o}{R_F R_o C s^2 + \big(R_F(1 + g_m R_o)C_F + (R_F + R_o)C_1 + R_o C_2\big)s + 1 + g_m R_o} \tag{2.33}$$

where $C = C_1C_2 + C_1C_F + C_2C_F$ and $R_o = 1/g_o$. C_{gd} of the MOSFETs has been ignored for preliminary modelling; therefore, by putting $C_F = 0$:

$$\frac{V_o}{I_{in}} = \frac{(1 - g_m R_F) R_o}{R_F R_o C_1 C_2 s^2 + \big((R_F + R_o)C_1 + R_o C_2\big)s + 1 + g_m R_o} \tag{2.34}$$

At low freqeuncies, we can write

$$\frac{V_o}{I_{in}} = -\frac{g_m R_F - 1}{g_m R_o + 1} R_o \tag{2.35}$$

$$R_{in} = \frac{R_F + R_o}{g_m R_o + 1} \tag{2.36}$$

$$R_o = R_o || \frac{1}{g_m} \tag{2.37}$$

Assuming $g_m R_F, g_m R_o \gg 1$, the transimpedance gain is $-R_F$ approximately. Therefore, the inverter-based TIA provides the same gain but with higher input and output resistance [5].

To determine the conditions for the pulse response, the natural frequency of the system is computed as

$$\omega_n = \sqrt{\frac{1 + g_m R_o}{R_F R_o C_1 C_2}} \tag{2.38}$$

and the damping factor becomes

$$\zeta = \frac{1}{2}\frac{R_o C_2 + (R_o + R_F)C_1}{\sqrt{R_F R_o C_1 C_2 (1 + g_m R_o)}} \tag{2.39}$$

2.6 Inverter-based cherry-hooper post-amplifier

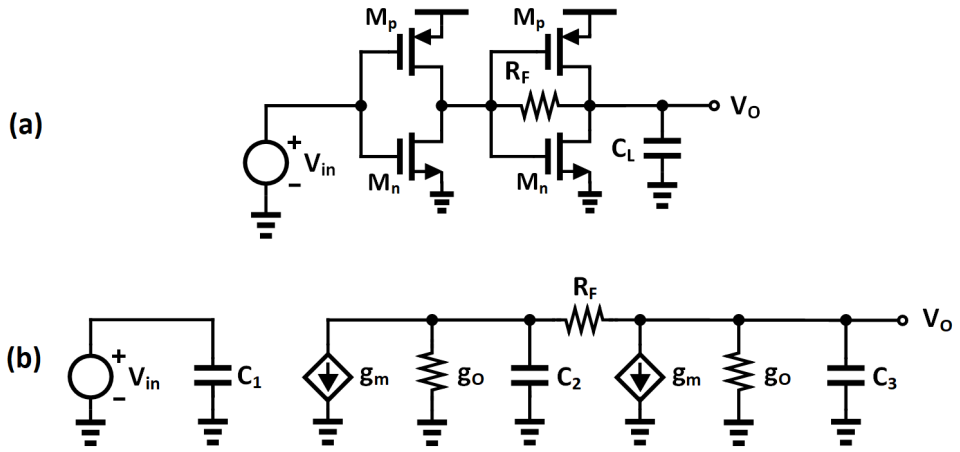


Figure 2.11: Schematic of an inverter-based cherry-hooper post-amplifier (a) transistor-level schematic (b) AC small-signal model

Fig 2.11 (a) shows a Cherry-Hooper post-amplifier (SF-PA), a two-stage voltage amplifier including a transconductance stage (voltage-to-current) followed by a transimpedance stage (current-to-voltage). The local feedback in the second stage reduces the impedance seen at the intermediate node and output node, allowing the pole frequencies to become much higher than a common-source amplifier with load resistance equal to R_F [5].

The AC small-signal model of the circuit is shown in Fig. 2.11 (b). C_{gd} of the MOSFETs has been ignored to simplify calculations.

Component parameters are as follows:

$$g_m = g_{m,n} + g_{m,p} \tag{2.40}$$

$$g_o = g_{o,n} + g_{o,p} \tag{2.41}$$

$$C_1 = C_{gs,n} + C_{gs,p} \tag{2.42}$$

$$C_2 = C_{gs,n} + C_{gs,p} + C_{db,n} + C_{db,p} \tag{2.43}$$

$$C_3 = C_{db,n} + C_{db,p} + C_L \tag{2.44}$$

The low frequency gain of the amplifier is

$$\frac{V_o}{V_{in}} = -g_m \frac{g_m R_F - 1}{g_m R_o + R_F/R_o + 2} R_o \tag{2.45}$$

The transimpedance gain approximates as $g_m R_F$ by assuming $g_m R_F, g_m R_o \gg 1$.

The voltage-to-voltage transfer function of the amplifier is given by

$$\frac{V_o}{V_{in}} = \frac{g_m(g_m R_F - 1)R_o}{R_F R_o C_2 C_3 s^2 + (R_F + R_o)(C_2 + C_3)s + 2 + g_m R_o + R_F/R_o} \tag{2.46}$$

Therefore, the parameters of natural frequency and the damping factor are computed as

$$\omega_n = \sqrt{\frac{2 + g_m R_o + R_F/R_o}{R_F R_o C_2 C_3}} \tag{2.47}$$

$$\zeta = \frac{1}{2} \frac{(R_o + R_F)(C_2 + C_3)}{\sqrt{R_F R_o C_2 C_3 (2 + g_m R_o + R_F/R_o)}} \tag{2.48}$$

2.7 Transient noise analysis

For LTI systems where the damping factor has a constant value during transient simulations, the mean-squared noise at the system's output does not vary over the unit interval. In other words, the value of the noise is independent of sampling time location. Therefore, ac noise analysis calculates the output noise voltage of the system properly. Time-varying operating point varies the mean-squared noise at the output of the proposed LPTV system over each UI. Instead of conventional ac noise analysis, transient noise analysis is used. The mean-squared output noise is calculated along the UI by:

$$v_n(t) = \sqrt{\frac{\Sigma_{n=0}^{N} v_o^2(t + nT_b)}{N}} \tag{2.49}$$

where N is the number of UIs used in the estimate, T_b is the bit period, and v_o results from a transient noise simulation in Spectre when no input signal is applied. Note that we are assuming that since input and output signals are relatively small, the system is still linear. Therefore, the output when we have an input signal will be the sum of the output due to the signal and the output due to noise. For LPTV systems, the sampling time is an important parameter in the value of the noise.

2.8 Sensitivity

The electrical sensitivity of a receiver is defined as the minimum peak-to-peak value of the input signal current of the receiver necessary to achieve a specified bit-error rate. The value of the sensitivity ($i_{pp,min}$) is given by:

$$i_{pp,min} = SNR \times I_{n,in} \times PP \tag{2.50}$$

where SNR is the signal-to-noise ratio required to achieve the targeted bit-error rate assuming an ideal decision circuit, $I_{n,in}$ is the input-referred noise of the analog circuitry and PP denotes the power penalty incurred by the swing needed at the Clock-and-Data Recovery (CDR). The basic receiver sensitivity is determined by the receiver noise. However, to calculate the power penalty more precisely, it is defined for a particular impairment as the increase in average transmit power necessary to achieve the same BER as in the absence of the impairment. Therefore the value of the power penalty is given by [19]:

$$PP = 1 + \frac{V_{CDR}}{SNR \times I_{n,in} \times Z_{VEO}} \tag{2.51}$$

where V_{CDR} is the minimum voltage swing required at the input of the CDR system that follows the TIA. In this work, the sensitivity of each designed system is calculated for $V_{CDR} = 25$ mV and $BER = 10^{-12}$ which needs $SNR = 14$ in linear units.

Chapter 3

SF-TIA design

In the previous chapter, we talked briefly about inverter-based shunt-feedback transimpedance amplifiers. The calculation in Eq. 2.39 makes it possible to design a SF-TIA with the optimum value of damping factor by selecting appropriate values of transistors size and the shunt-feedback resistor regarding the input and load capacitors. In this chapter, in addition to considering the value of the damping factor, we focus on the design of differential shunt-feedback TIAs with and without cross-coupled inverters at the output with minimum input-referred noise current, computed by Eq. 2.13. The mentioned TIAs act as linear time-invariant (LTI) systems, and to obtain the mean-squared noise at the output, ac noise analysis performs accurately. The proposed optimized TIA with cross-coupled inverters across the output achieves a larger bandwidth and vertical eye opening compared to the TIA without cross-coupled inverters and better performance to obtain lower input referred to noise and sensitivity.

The following two sections present how the design parameters of LTI TIAs are optimized to achieve the minimum value of the input noise and the results of the design. For all simulations of this chapter using Cadence in 65 nm technology, $f_{bit} =$ 10 Gb/s for random input data with peak-to-peak amplitude of 2 μA, $C_{in} = 200$ fF, $C_L = 50$ fF.

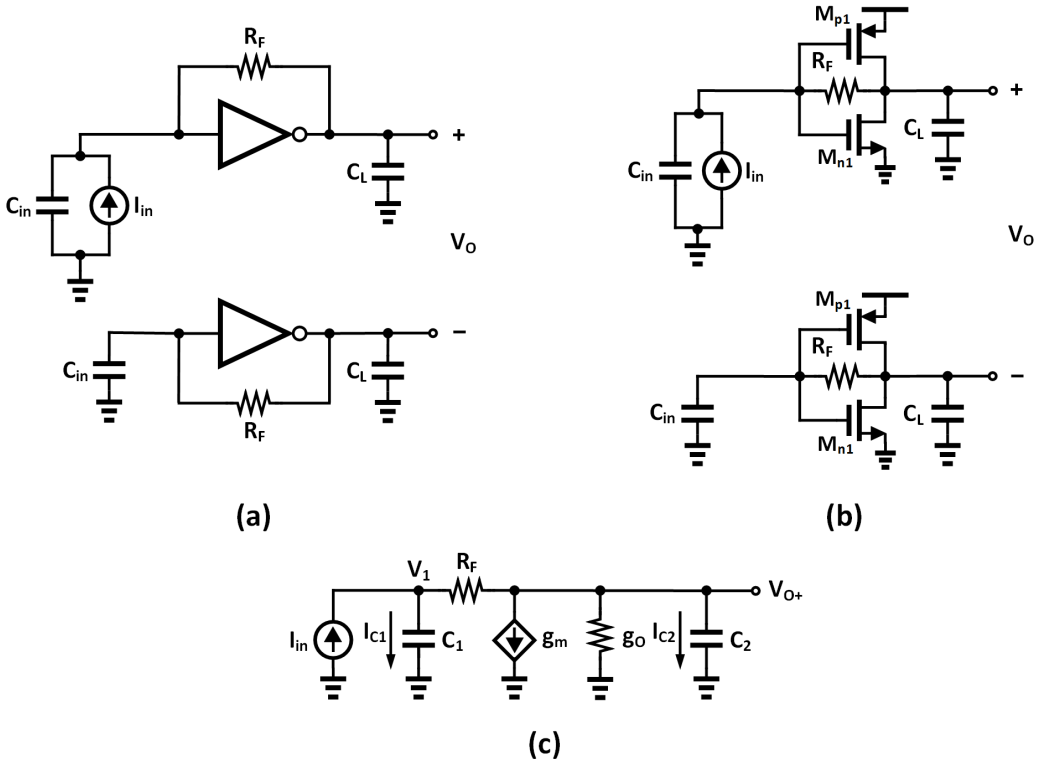


Figure 3.1: Differential shunt-feedback TIA (a) high-level schematic (b) transistor-level schematic (c) ac small-signal model of the differential half of circuit

3.1 Differential shunt-feedback TIA design

The high-level schematic of the proposed differential inverter-based shunt-feedback TIA is shown in Fig. 3.1 (a). It consists of static-CMOS inverters and feedback resistors R_F. Fig. 3.1 (b) shows the transistor-level schematic of the system. C_{in} includes the capacitance of the PD and the capacitance of the TIA's input pad, and C_L is the load capacitance of the TIA drives, including latches and buffers. DC and Offset compensation circuits have been ignored. To explore the performance of the SF-TIA, an AC small-signal model of the differential half circuit of the SF-TIA is shown in Fig. 3.1 (c). C_{gd} of the MOSFETs has been ignored for preliminary

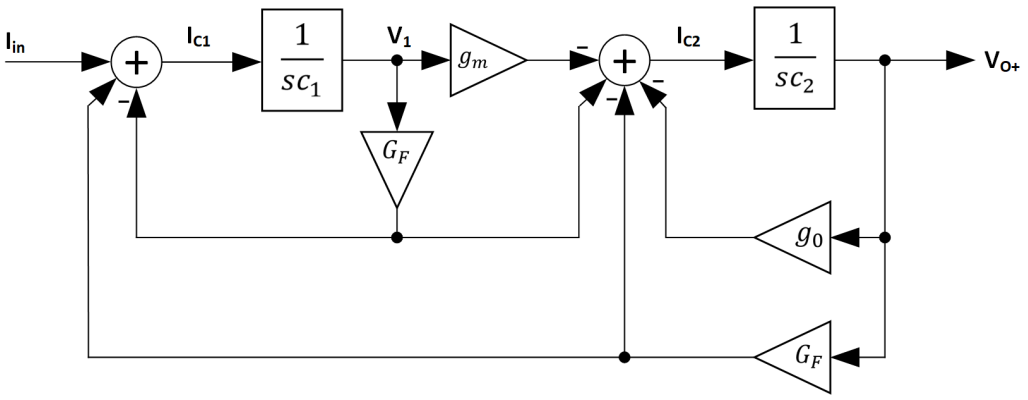


Figure 3.2: SIMULINK model of the shunt-feedback TIA, shown in Fig. 3.1

modelling. Component parameters are as follows:

$$C_1 = C_{gs,n1} + C_{gs,p1} + C_{in} \tag{3.1}$$

$$C_2 = C_{db,n1} + C_{db,p1} + C_L \tag{3.2}$$

$$g_m = g_{m,n1} + g_{m,p1} \tag{3.3}$$

$$g_o = g_{o,n1} + g_{o,p1} \tag{3.4}$$

Using the small-signal model of the TIA, the s-domain equations used to develop a SIMULINK model are:

$$v_1 = \frac{i_{C_1}}{sC_1} \quad \text{where} \quad i_{C_1} = i_{in} + \frac{v_{o+} - v_1}{R_F} \tag{3.5}$$

$$v_{o+} = \frac{i_{C_2}}{sC_2} \quad \text{where} \quad i_{C_2} = \frac{v_1 - v_{o+}}{R_F} - g_m v_1 - g_o v_{o+} \tag{3.6}$$

These equations are represented in a behavioral model shown in Fig. 3.2 where $G_F = 1/R_F$.

Fig. 3.3 shows output of the shunt-feedback TIA model in SIMULINK using $R_F = 1\ k\Omega$ and transistor parameters corresponding to $W_{n1} = W_{p1} = W_1 = 20\ \mu m$ in a 65 nm technology for an input current with peak-to-peak amplitude of 1 A. In this case, damping factor calculaation by Eq. 2.39, results in $\zeta = 0.92$, notably higher than the optimum values of $\frac{1}{\sqrt{2}}$. The VEO gain of the system is 800 V.

To design the transistor level of the circuit with minimum input-referred noise current, we should go through the following steps. Since no equalization is used for our design and by assuming that TIA's output is directly connected to the latches, the input-referred noise current is defined as Eq. 2.13, the rms value of the output

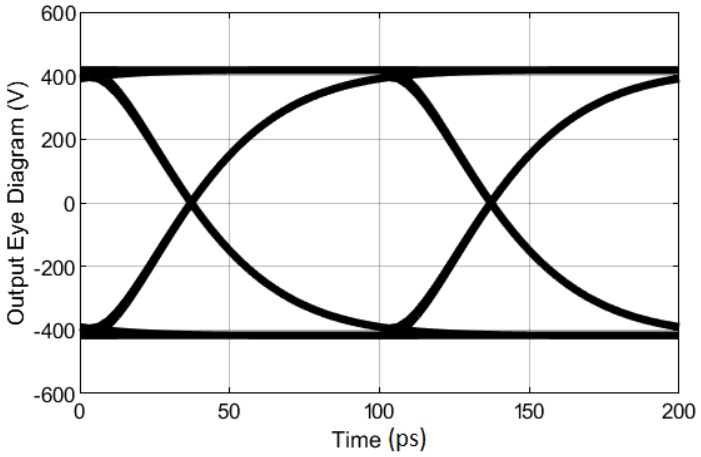


Figure 3.3: Output eye diagram of the shunt-feedback TIA model in SIMULINK (Fig. 3.2) for input data with peak to peak amplitude of 1 A and $f_{bit} = 10\ Gb/s$

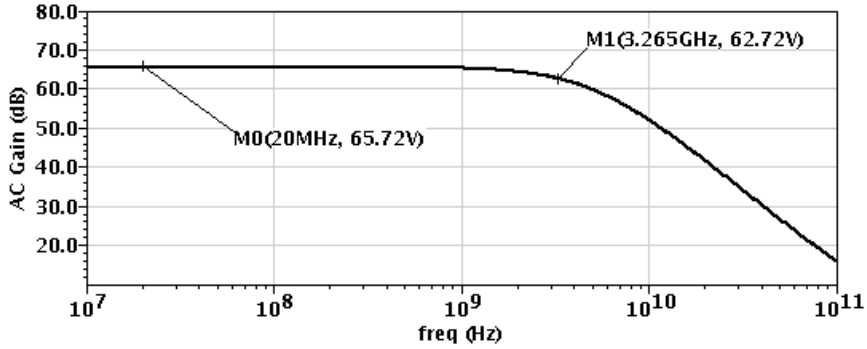


Figure 3.4: Frequency response of the shunt-feedback TIA in the range of 10 MHz to 100 GHz for an ac input current value of 2 A, $W_1 = 23\ \mu m$ and $R_F = 1.15\ k\Omega$

noise voltage divided by VEO gain, which is called effective gain [12]. First, based on the design specifications, the bit rate of the input signal f_{bit}, load capacitors C_L and the input capacitor C_{in} including capacitance of the PD and the TIA's input pad are given. In the next step, a size of transistors, $W_{n1} = W_{p1} = W_1$, is chosen, and three parameters C_1, C_2 and $R_o = 1/g_o$ are computed by Eq. 3.1, Eq. 3.2 and Eq. 3.4 respectively. Now, a value of the feedback resistor is selected, and Eq. 2.39 calculates the value of the damping factor. Transient simulations give us the effective gain or VEO gain of the TIA for a random input pulse signal. In the next step, the rms value of the output noise voltage is calculated by ac noise analysis, and to refer the value of the noise to input, the input-referred noise current is computed by Eq. 2.13. Selecting the value of the R_F lasts until reaching the lowest value of the

Table 3.1: Noise optimization procedure of SF-TIA

Step	Description	Values
1	By specifications we have:	f_{bit} C_{in} C_L
2	Choose a W_1 and calculate:	C_1 C_2 R_o
3	Select a R_F and Eq. 2.39 computes:	ζ
4	Run a transient simulation for a random input data at f_{bit} to obtain the output eye diagram and calculate the value of:	VEO gain
5	By measuring the value of the output noise voltage and having the TIA's effective gain, Eq. 2.13 Calculates:	$I_{n,in}$
6	Repeat steps 3 to 5 until finding the lowest value of $I_{n,in}$ that gives us the value of:	$R_{F,optimum}$
7	Repeat steps 2 to 6 until achieving the minimum value of $I_{n,in}$ which gives rise to the value of:	$W_{1,optimum}$

$I_{n,in}$. Again for another inverter size (W_1) previous steps are repeated until finding the minimum value of the $I_{n,in}$ or optimal TIA. Therefore, this procedure gives rise to achieve optimal values of W_1 and R_F. All steps of the optimization procedure are presented in Table 3.1 briefly.

The input-referred noise current reaches its minimum value of 0.94 μA_{rms} with $W_1 = 23\ \mu m$ and $R_F = 1.15\ k\Omega$. Fig. 3.4 shows the frequency response of the TIA in the range of 10 MHz to 100 GHz for an ac current value of 2 A. The mid-band gain of the TIA is 0.97 $k\Omega$, and the 3dB bandwidth of the circuit is 3.27 GHz.

For random input data with peak-to-peak amplitude of 2 μA, the output eye diagram of the TIA is shown in Fig. 3.5. The VEO gain or effective gain of the TIA is 0.65 $k\Omega$.

In another simulation, the pulse response of the TIA is shown in Fig. 3.6 for a single pulse current with the peak-to-peak amplitude of 4.45 μA and the pulse width of 100 ps. Gain of the TIA using pulse response height is 0.8 $k\Omega$. Eq. 2.10 computes

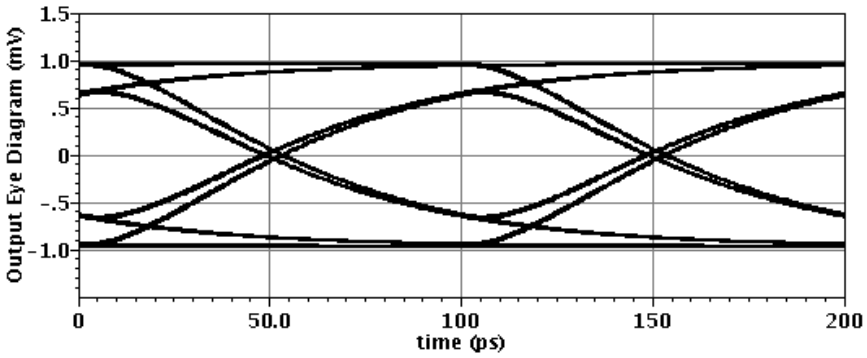


Figure 3.5: Output eye diagram of the shunt-feedback TIA, $W_1 = 23\ \mu m$, $R_F = 1.15\ k\Omega$ and $f_{bit} = 10\ Gb/s$

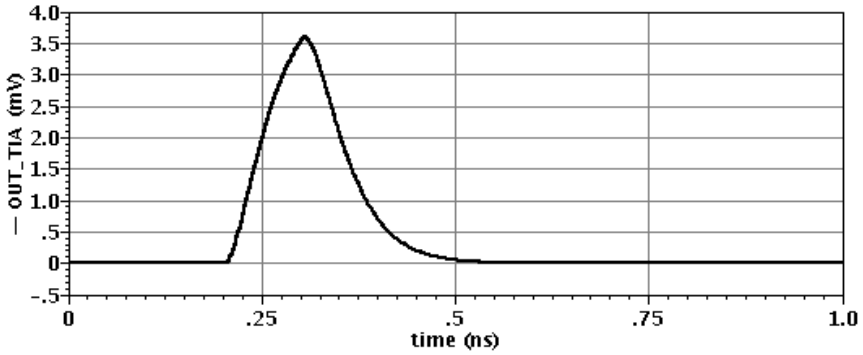


Figure 3.6: Pulse response of the of the shunt-feedback TIA, $W_1 = 23\ \mu m$, $R_F = 1.15\ k\Omega$ and $f_{bit} = 10\ Gb/s$

the maximum value of the ISI as

$$ISI_{MAX} = 0.1 + 0.65 + 0.1 = 0.85\ mV \tag{3.7}$$

using Eq. 2.11, the VEO gain of the circuit is calculated as

$$Z_{VEO} = \frac{3.55 - 0.85}{4.45} = 0.6\ k\Omega \tag{3.8}$$

which is close to VEO gain obtained from Fig 3.5.

Now to calculate the sensitivity of a receiver using the proposed designed TIA, the power penalty is computed by Eq. 2.51 as

$$PP = 1 + \frac{25}{14 \times 0.94 \times 0.65} = 3.92 \tag{3.9}$$

And using Eq. 2.50,the receiver sensitivity becomes

$$i_{pp,min} = 14 \times 0.94 \times 3.92 = 51.62\ \mu A_{pp} \tag{3.10}$$

Therefore, the minimum peak-to-peak value of the receiver input current to obtain BER of 10^{-12} is equal to 51.62 μA_{pp}.

3.2 Differential shunt-feedback TIA design with cross-coupled inverters at the output

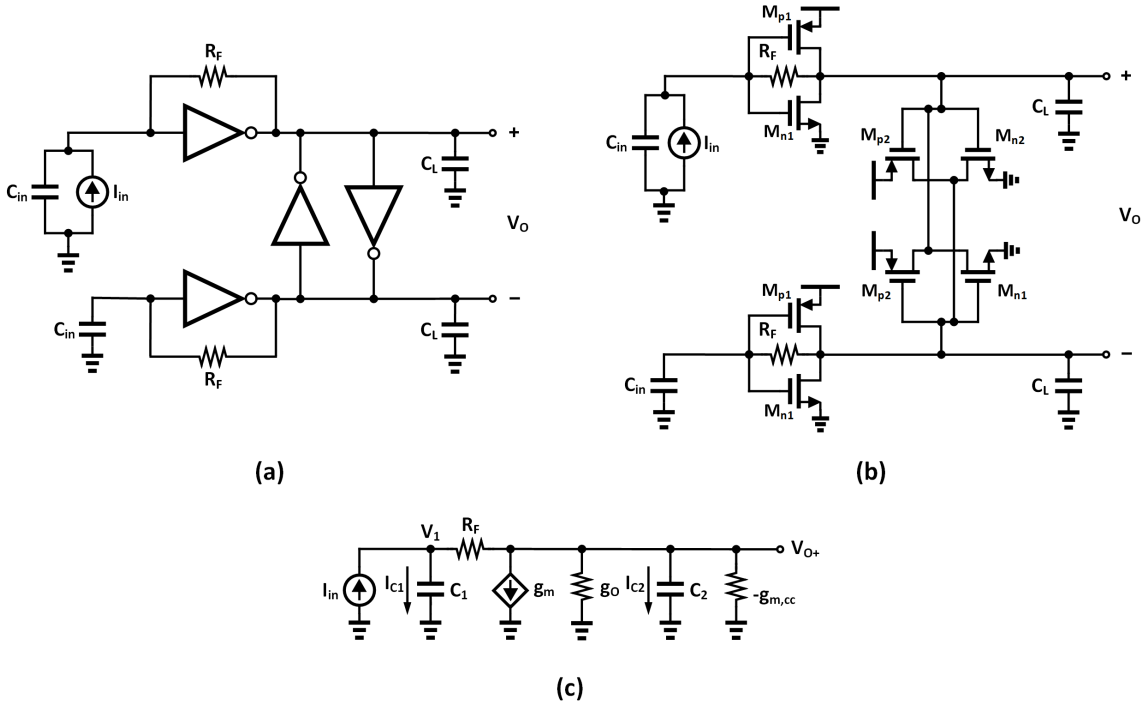


Figure 3.7: Differential shunt-feedback TIA with cross-coupled inverters at the output (a) high-level schematic (b) transistor-level schematic (c) ac small-signal model of the differential half of circuit

When an amplifier is implemented using a static-CMOS inverter, due to its low intrinsic gain, a higher damping factor often results, leading to slower settling and a reduction in vertical eye-opening (VEO). Cross-coupled inverters can be added to the output of a differential TIA, increasing the voltage amplifier's gain [20]. Fig. 3.7 (a) shows the high-level schematic of the proposed differential inverter-based shunt-feedback TIA with cross-coupled inverters across the output. Transistor-level schematic of the system is shown in Fig. 3.7 (b). And same to the previous section, DC and Offset compensation circuits have been ignored, C_{in} includes the capacitance

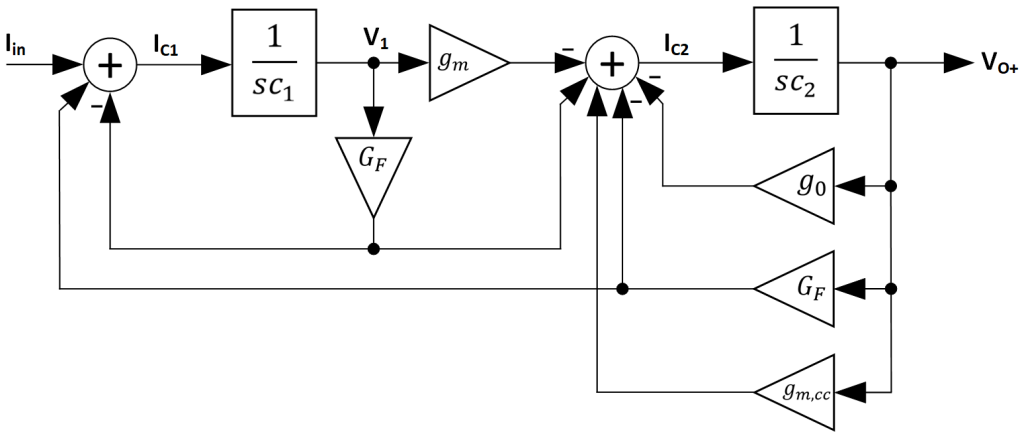


Figure 3.8: SIMULINK model of the shunt-feedback TIA with cross-coupled inverters at the output, shown in Fig. 3.7

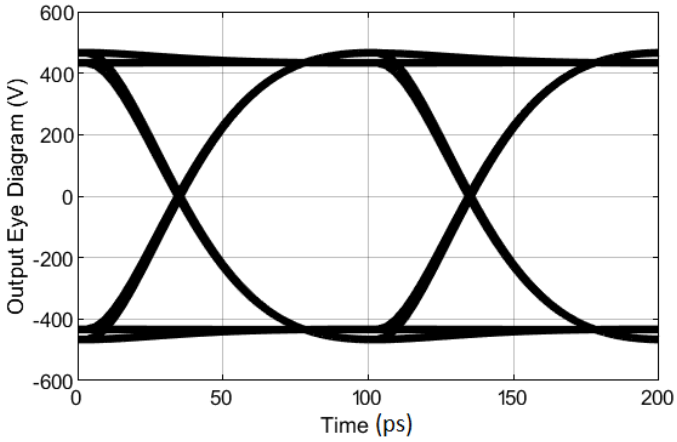


Figure 3.9: Output eye diagram of the shunt-feedback TIA model in SIMULINK with cross-coupled inverters at the output (Fig. 3.8) for input data with peak to peak amplitude of 1 A, $g_{m,cc} = 1\mho$ and $f_{bit} = 10\ Gb/s$

of the PD and the capacitance of the TIA's input pad, and C_L is the load capacitance the TIA drives. C_{gd} of the MOSFETs has been ignored, and the AC small-signal model of the differential half circuit of the TIA is shown in Fig. 3.7 (c). Component parameters are as follows:

$$C_1 = C_{gs,n1} + C_{gs,p1} + C_{in} \tag{3.11}$$

$$C_2 = C_{db,n1} + C_{db,p1} + C_{gs,n2} + C_{gs,p2} + C_{db,n2} + C_{db,p2} + C_L \tag{3.12}$$

$$g_m = g_{m,n1} + g_{m,p1} \tag{3.13}$$

$$g_o = g_{o,n1} + g_{o,p1} \tag{3.14}$$

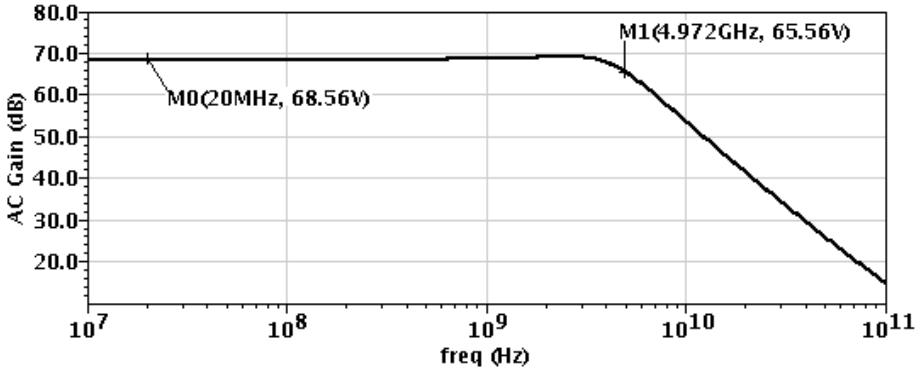


Figure 3.10: Frequency response of the shunt-feedback TIA with cross-coupled inverters at the output in the range of 10 MHz to 100 GHz for an ac input current value of 2 A, $W_1 = 30\ \mu m$, $W_2 = 4.5\ \mu m$ and $R_F = 1.15\ k\Omega$

In differential design, cross-coupled inverters can reduces the output conductance as [21]:

$$g_{o,tot} = g_o - g_{m,cc} \tag{3.15}$$

where g_o is the output conductance of the main inverters and $g_{m,cc}$ is the transconductance of the cross-coupled inverters.

Writing the s-domain equations as

$$v_1 = \frac{i_{C_1}}{sC_1} \quad \text{where} \quad i_{C_1} = i_{in} + \frac{v_{o+} - v_1}{R_F} \tag{3.16}$$

$$v_{o+} = \frac{i_{C_2}}{sC_2} \quad \text{where} \quad i_{C_2} = \frac{v_1 - v_{o+}}{R_F} - g_m v_1 + (g_{m,cc} - g_o)v_{o+} \tag{3.17}$$

let us developing the SIMULINK model of the TIA shown in Fig. 3.8 where $G_F = 1/R_F$.

For $R_F = 1\ k\Omega$, a cross-coupled inverter with conductance of $-1\ m\mho$ ($g_{m,cc} = 1$) and transistor parameters corresponding to $W_{n1} = W_{p1} = W_1 = 20\ \mu m$ in a 65 nm technology for an input current with peak-to-peak amplitude of 1 A, output eye diagram of the SIMULINK model is shown in Fig. 3.9. Compared to the SIMULINK model in the previous section, the damping factor of the system changed from 0.92 to 0.7, and the VEO of the output increased slightly from 800 V to 900 V.

The transistor-level circuit is designed for minimum input-referred noise current. The bit rate of the input signal f_{bit}, the input capacitor C_{in} and the load capacitor C_L are given as design specifications. After selecting a size of main inverter transistors $W_{n1} = W_{p1} = W_1$, a size of transistor for cross-coupled inverters $W_{n2} = W_{p2} = W_2$ are

Table 3.2: Noise optimization procedure of SF-TIA with X-coupled inverters at the output

Step	Description	Values
1	By specifications we have:	f_{bit} C_{in} C_L
2	Select a W_1	
3	Choose a W_2 and calculate:	C_1 C_2 R_o
4	Select a R_F and Eq. 2.39 computes:	ζ
5	Run a transient simulation for a random input data at f_{bit} to obtain the output eye diagram and calculate the value of:	VEO gain
6	By measuring the value of the output noise voltage and having the TIA's effective gain, Eq. 2.13 Calculates:	$I_{n,in}$
7	Repeat steps 4 to 6 until finding the lowest value of $I_{n,in}$ that gives us the value of:	$R_{F,optimum}$
8	Repeat steps 3 to 7 to obtain the smallest value of $I_{n,in}$ that generates the value of:	$W_{2,optimum}$
9	Repeat steps 2 to 8 until achieving the minimum value of $I_{n,in}$ that gives rise to the value of:	$W_{1,optimum}$

chosen. Therefore, parameters of C_1, C_2 and $R_o = 1/g_o$ are obtained by Eq. 3.11, Eq. 3.12 and Eq. 3.14 respectively. Now, a value of the feedback resistor is selected, and Eq. 2.39 calculates the value of the damping factor. In the next step, the VEO gain of the TIA, Z_{VEO}, for the random input data is obtained by a transient simulation. The input-referred noise current is calculated by Eq. 2.13 after measuring the rms value of output noise voltage by ac noise analysis. The value of the R_F is changed to reach the smallest value of the input-referred noise. Then, we continue this process to find a W_2 for the selected W_1 where the input-referred noise current has the lowest value. Finally, this procedure is repeated for different values of W_1 until reaching the minimum value of the $I_{n,in}$ or optimal TIA. Therefore, we have optimal values of W_1, W_2 and R_F for the shunt-feedback TIA with cross-coupled inverters at the output.

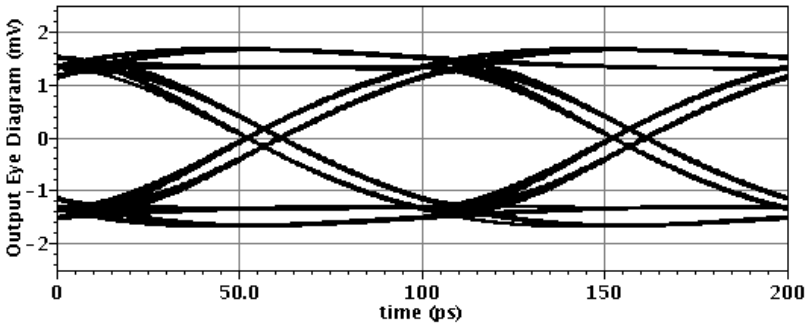


Figure 3.11: Output eye diagram of the shunt-feedback TIA with cross-coupled inverters at the output, $W_1 = 30\ \mu m$, $W_2 = 4.5\ \mu m$, $R_F = 1.4\ k\Omega$ and $f_{bit} = 10\ Gb/s$

Table 3.2 summarizes all steps of input-referred noise optimization in TIA design, including cross-coupled inverters at the output. With $W_1 = 30\ \mu m$, $W_2 = 4.5\ \mu m$ and $R_F = 1.4\ k\Omega$ input-referred noise current reaches its minimum value of 0.74 μA_{rms}. Frequency response of the TIA for AC current value of 2 A is shown in Fig. 3.10. The mid-band gain of the TIA is 1.35 $k\Omega$, and the bandwidth of the circuit is 4.97 GHz.

Fig. 3.11 shows the output eye diagram of the TIA with cross-coupled inverters at the output for random input data with peak-to-peak amplitude of 2 μA. The VEO gain is 1.25 $k\Omega$.

The pulse response of the TIA with cross-coupled inverters is shown in Fig. 3.12 for a single pulse current with the peak-to-peak amplitude of 4.45 μA and the pulse width of 100 ps. Pulse response gain of the TIA is 1.34 $k\Omega$. The maximum value of the ISI is given by Eq. 2.10 as

$$ISI_{MAX} = 0.175 + 0.375 + 0.1 = 0.65\ mV \tag{3.18}$$

And Eq. 2.11 computes the VEO gain of the circuit as

$$Z_{VEO} = \frac{6 - 0.65}{4.45} = 1.2\ k\Omega \tag{3.19}$$

which is close to VEO gain obtained by the output VEO of the system in Fig 3.5.

Having the designed shunt-feedback TIA with cross-coupled inverters at the output needs the another calculation of the receiver sensitivity. The power penalty is obtained by Eq. 2.51 as

$$PP = 1 + \frac{25}{14 \times 0.74 \times 1.25} = 2.93 \tag{3.20}$$

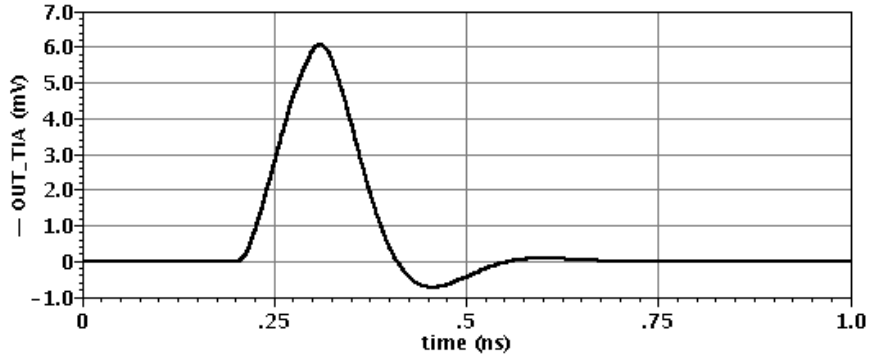


Figure 3.12: Pulse response of the shunt-feedback TIA with cross-coupled inverters at the output, $W_1 = 30\ \mu m$, $W_2 = 4.5\ \mu m$, $R_F = 1.4\ k\Omega$ and $f_{bit} = 10\ Gb/s$

The receiver sensitivity is calculated by Eq. 2.50

$$i_{pp,min} = 14 \times 0.74 \times 2.93 = 30.36\ \mu A_{pp} \tag{3.21}$$

Therefore, the minimum peak-to-peak current value of 30.36 μA_{pp} is needed at the receiver to reach BER of 10^{-12}.

Results of the TIA design, including shunt-feedback TIA with and without the cross-coupled inverters (LTI systems), are summarized in Table 3.3. Having cross-coupled inverters at the output, increased the AC gain of the TIA. In addition, the system with cross-coupled inverters reaches to higher bandwidth, half of the data rate, giving rise to the same gain value calculated by ac analysis and pulse response height. Furthermore, adding the cross-coupled inverters at the output of the TIA increased the computed effective gain by Eq. 2.12, Z_{VEO}, of the TIA and the ratio of VEO gain and power dissipation. If we have two shunt-feedback TIAs with and without cross-coupled inverters designed for optimal damping factor and consume the same power, the TIA with cross-coupled inverters shows the higher value of effective gain. About the noise performance issue, comparing the calculated input-referred noise current using Eq. 2.13, using cross-coupled inverters in the system gives rise to lower input noise value and better noise performance. And finally, using the Eq. 2.50 for 25 mV voltage swing at the CDR block and bit-error rate of 10^{-12}, the receiver, including the proposed, designed TIA with cross-coupled inverters, gives better sensitivity compared to the TIA without cross-coupled inverters.

Table 3.3: Results summary of LTI shunt-feedback TIA design

LTI SF-TIA including:	Main inverters	Main and X-coupled inverters
Size of transistors (μm)	$W_1 = 23$	$W_1 = 30$ $W_2 = 4.5$
R_F (kΩ)	1.15	1.4
Data rate (Gb/s)	10	10
f_{3dB} (GHz)	3.27	4.97
AC gain (kΩ)	0.97	1.35
Pulse gain (kΩ)	0.8	1.34
VEO gain (kΩ)	0.65	1.25
$I_{n,in}$ (μA_{rms})	0.94	0.74
Power (mW)	2.65	4.03
Z_{VEO}/Power ratio (kΩ/mW)	0.25	0.31
$i_{pp,min}$ (μA_{pp}) for $V_{CDR} = 25$ mV	51.62	30.36

Chapter 4

Damping factor modulation in SF-TIAs

In the previous chapter, we focused on designing LTI transimpedance amplifiers with and without the cross-coupled inverters across the output. In chapter 2, it was shown that in a second-order system, modulation of the damping synchronously with the incoming data increases the VEO gain of the system. Therefore, in the next sections of the following chapter, we will show the shunt-feedback TIA circuit designs to make the modulation possible.

Inspired by observations of the dependence of a 2^{nd}-order system's settling behavior on its damping factor, we modulate the damping factor of an inverter-based shunt-feedback TIA, a commonly used TIA. In the first section, switching the R_F between high and low values increases the VEO gain of the TIA. In the next section, dynamic damping is introduced by adding a triode-region transistor with a sine wave bias voltage across the outputs, which modulates the damping factor of the system each unit interval. With dynamic damping, the TIA achieves more than twice the VEO compared to the optimized reference TIA. In the remainder section, the damping factor is modulated by applying a rail-to-rail square-wave bias voltage, which changes the damping factor of the system between negative and positive values each unit interval. The proposed TIA achieves more than twice the vertical eye opening, and lower input referred noise compared to the optimized reference TIA, as well as higher gain and lower input referred noise compared to the TIA with sinusoidal damping-factor modulation. In this chapter, using time-varying operating

points creates a time-varying system, which for the small input currents generated by the photodiode (PD) is considered to be a *linear* periodically time-varying (LPTV) system. Therefore, transient noise analysis with Eq. 2.49 are used to calculate noise performance instead of conventional ac noise analysis.

For all simulations of this chapter using Cadence in 65 nm technology, $f_{bit} = 10$ Gb/s for random input data with peak-to-peak amplitude of 2 μA, $C_{in} = 200$ fF, $C_L = 50$ fF.

4.1 R_F switching

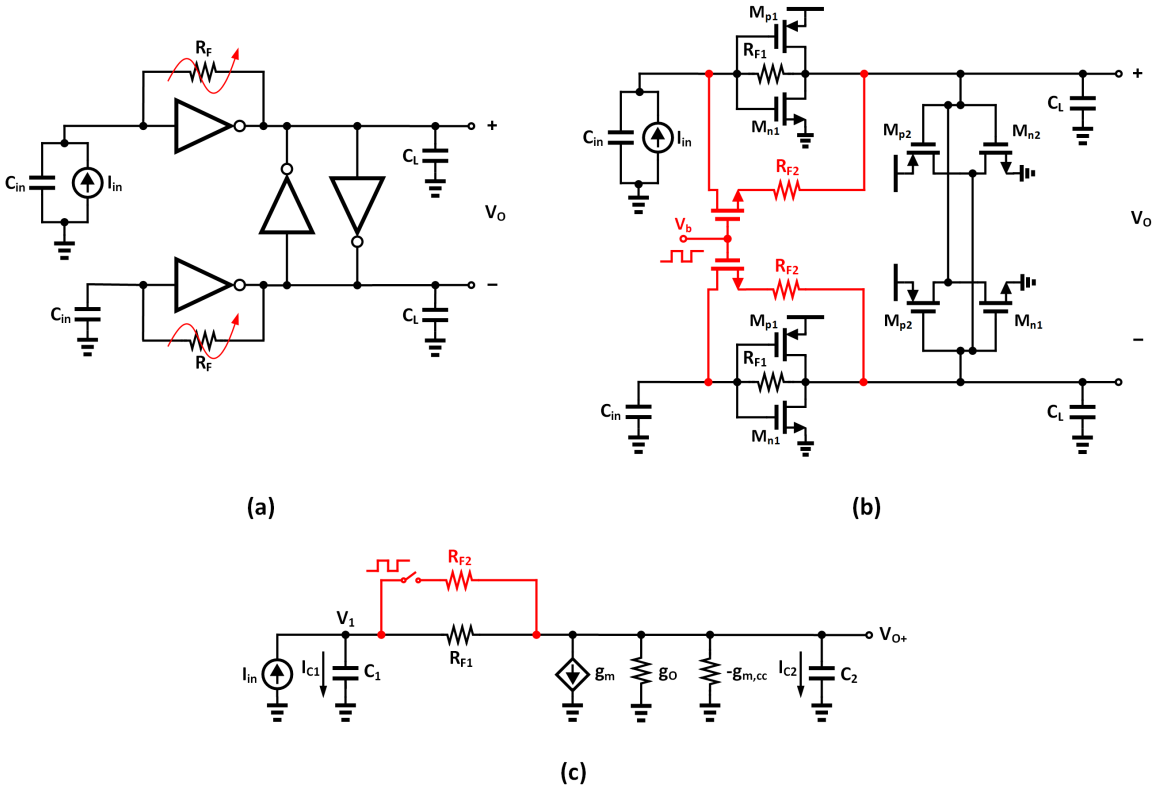


Figure 4.1: Differential shunt-feedback TIA with cross-coupled inverters at the output and modulated feedback resistor ($V_b = V_{DD} \sum p(t - kT_b - t_d)$) (a) high-level schematic (b) transistor-level schematic (c) ac small-signal model of the differential half of circuit

At first, we would like to thank Professor Shanthi Pavan for suggesting feedback resistor modulation. Before designing a TIA that realizes modulating the damping, we need to get some insights into the systems model. For a second-order system

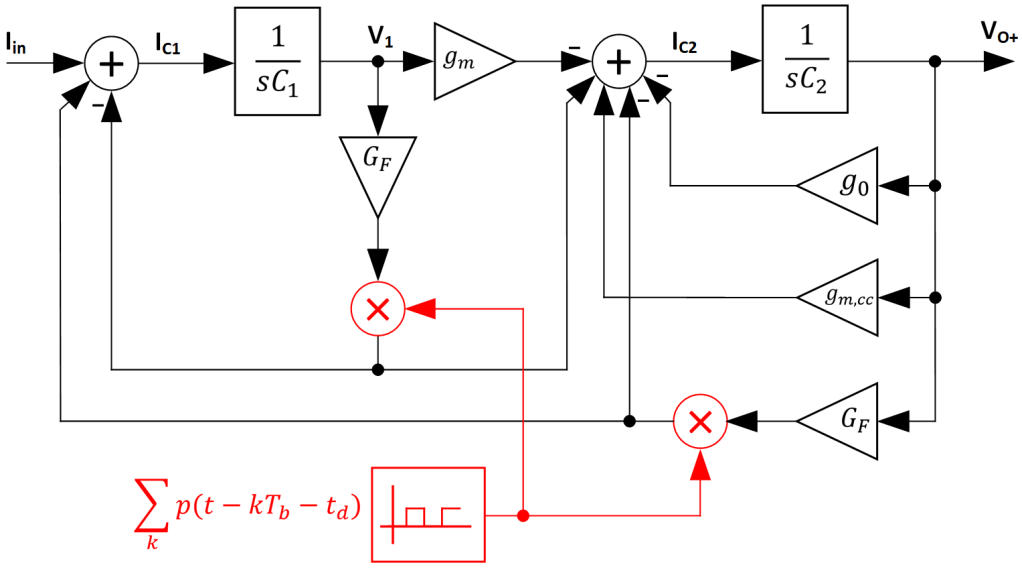


Figure 4.2: SIMULINK model of the shunt-feedback TIA with cross-coupled inverters at the output and R_F modulation, shown in Fig. 4.1

shown in Fig. 2.4, modulating the b_1 gives rise to modulating the damping factor. But, the presented block diagram of the shunt-feedback TIA in Fig. 3.2 and the Eq. 2.39 indicate that damping factor is a more complicated relation among several parameters. Changing resistor values of R_F or R_o in a unit interval can modulate the value of the damping factor and may increase the VEO at the output. For the first step, we start by modulating the shunt-feedback resistor. The high-level and transistor-level schematics of the differential shunt-feedback TIA with R_F modulation and cross-coupled inverters at the output are shown in Fig. 4.1 (a) and (b). Red arrows indicate proposed dynamic modulation.

To investigate this method, the feedback resistor (R_F) is increased to a high value of R_{F1} and a switched small resistor (R_{F2}) is connected parallel across it synchronously with the incoming data. Therefore, a rail-to-rail square wave signal is used as the bias voltage applied to switches.

$$V_b = V_{DD} \sum p(t - kT_b - t_d) \tag{4.1}$$

where p(t) denotes the unit-amplitude pulse with 50 % duty cycle, and t_d is the initial delay time.

Fig. 4.1 (c) shows the ac small-signal model of the differential half circuit, ignoring the DC and Offset compensation circuits, C_{in} includes the capacitance of the PD and

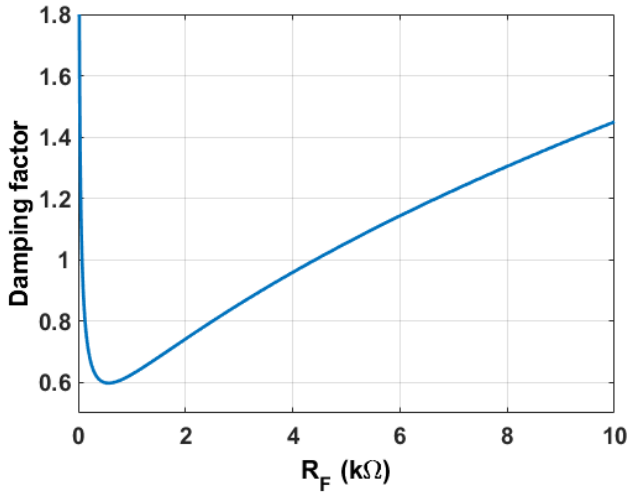


Figure 4.3: Damping factor value of the shunt-feedback TIA SIMULINK model vs. shunt-feedback resistor (R_F)

the capacitance of the TIA's input pad, and C_L is the load capacitance the TIA drives. C_{gd} of the MOSFETs has been ignored. Component parameters are as follows:

$$C_1 = C_{gs,n1} + C_{gs,p1} + C_{in} \tag{4.2}$$

$$C_2 = C_{db,n1} + C_{db,p1} + C_{gs,n2} + C_{gs,p2} + C_{db,n2} + C_{db,p2} + C_L \tag{4.3}$$

$$g_m = g_{m,n1} + g_{m,p1} \tag{4.4}$$

$$g_o = g_{o,n1} + g_{o,p1} \tag{4.5}$$

Using cross-coupled inverters reduces the output conductance as [21]:

$$g_{o,tot} = g_o - g_{m,cc} \tag{4.6}$$

where g_o is the output conductance of the main inverters and $g_{m,cc}$ is the transconductance of the cross-coupled inverters. The SIMULINK model of the TIA is developing by s-domain equations as

$$v_1 = \frac{i_{C_1}}{sC_1} \quad \text{where} \quad i_{C_1} = i_{in} + \frac{v_{o+} - v_1}{R_F} \tag{4.7}$$

$$v_{o+} = \frac{i_{C_2}}{sC_2} \quad \text{where} \quad i_{C_2} = \frac{v_1 - v_{o+}}{R_F} - g_m v_1 + (g_{m,cc} - g_o) v_{o+} \tag{4.8}$$

assuming ideal switches with no series resistor

$$R_F = R_{F1} || \left(R_{F2} \sum p(t - kT_b - t_d) \right) \tag{4.9}$$

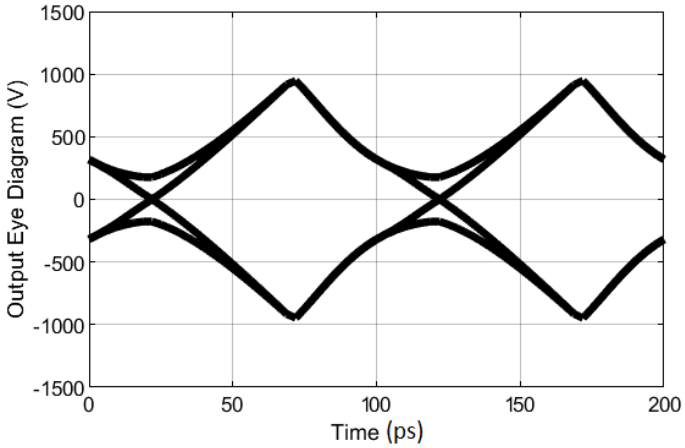


Figure 4.4: Output eye diagram of the shunt-feedback TIA model in SIMULINK with cross-coupled inverters at the output and R_F modulation (Fig. 4.2) for input data with peak to peak amplitude of 1 A, $g_{m,cc} = 1$ $\mho$, $G_F = 2$ $m\mho$, $t_d = 18$ ps and $f_{bit} = 10$ Gb/s

where $G_F = 1/R_F$ and $p(t)$ denotes the unit-amplitude pulse with 50 % duty cycle and t_d is initial delay time.

The SIMULINK model of the TIA consisting of cross-coupled inverters at the output and modulated shunt feedback resistor is shown in Fig. 4.2 where transistor parameters are corresponding to $W_{n1} = W_{n2} = W_1 = 20$ μm in a 65 nm technology, the cross-coupled inverters have a conductance of -1 $m\mho$ ($g_{m,cc} = 1$) and $G_F = 1/R_F$ is equal to 2 $m\mho$. The overall shunt-feedback resistor is computed as

$$R_F = \frac{1}{G_F \sum p(t - kT_b - t_d)} \tag{4.10}$$

In a half portion of unit interval (UI), when the value of $p(t)$ is 0, the TIA has a large value of feedback resistor hence significant gain. The remaining portion of UI where $p(t)$ goes to 1, TIA, has a small feedback resistor and low gain value. Therefore, the damping factor of the system calculated by Eq. 2.39 is modulated by the square-wave signal. Fig. 4.3 shows the value of the damping factor (Eq. 2.39) for different values of shunt-feedback resistor. The damping factor of the system reaches its minimum value of 0.6 with $R_F = 0.5$ $k\Omega$. Therefore, for this system, it is not possible to obtain a much faster system by decreasing the damping factor lower than 0.6 by modulating the shunt-feedback resistor.

For a random input current with peak-to-peak amplitude of 1 A and $t_d = 18$ ps, the output eye diagram of the model is shown in Fig. 4.4. $G_F \sum p(t - kT_b - t_d)\big)$

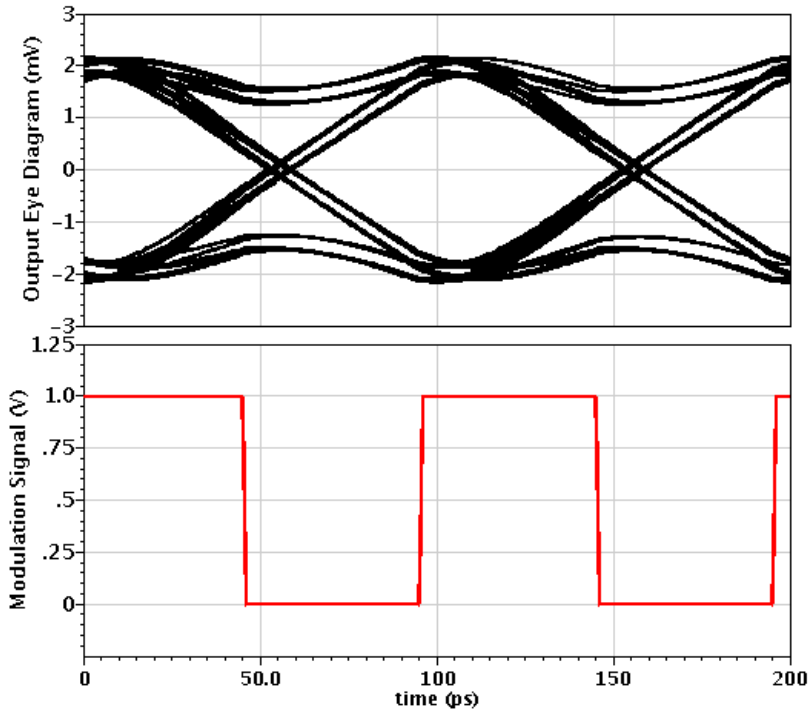


Figure 4.5: Output eye diagram of the shunt-feedback TIA with cross-coupled inverters at the output and R_F modulation, the rail-to-rail square wave modulation signal, $W_1 = 30\ \mu m$, $W_2 = 4.5\ \mu m$, $R_{F1} = 100\ k\Omega$, $R_{F2} = 0.9\ k\Omega$, $t_d = 10\ ps$ and $f_{bit} = 10\ Gb/s$

changes along the UI between $\{0\ \mho,\ 1\ m\mho\}$ hence the value of R_F switches between $\{1\ k\Omega,\ \infty\}$. The output VEO of the system with R_F modulation increased from 900 V to 1900 V compared to the system with constat feedback value $G_F = 1\ m\mho$.

To explore the performance of the TIA with a dynamic shunt-feedback resistor, the gate of switches is driven by a rail-to-rail square wave voltage of $V_b = V_{DD} \sum p(t - kT_b - t_d)$. The square wave signal modulates the overall shunt-feedback of the TIA and the damping factor. Here, the size of transistors ($W_{n1} = W_{p1} = W_1$ and $W_{n2} = W_{p2} = W_2$) is not changed compared to the LTI TIA designed with cross-coupled inverts at the output. By selecting appropriate values for R_{F1}, R_{F2} and t_d, overall feedback resistor and the damping factor of the system swings between low and high values. The output eye diagram of the system and the modulation signal, a rail-to-rail square wave signal, are shown in Fig. 4.5. Here, $R_{F1} = 100\ k\Omega$, $R_{F2} = 0.9\ k\Omega$ and $t_d = 10\ ps$. The gain of the system is 1.78 $k\Omega$ and higher than 1.7 $k\Omega$ over a range of more than 12.5 ps delay variation of the signal $p(t)$, corresponding to a 45°

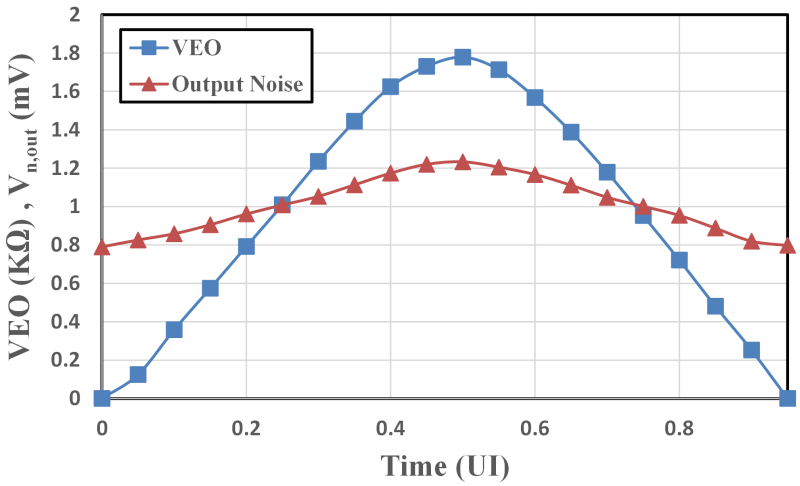


Figure 4.6: VEO and output noise voltage of shunt-feedback TIA with cross-coupled inverters at the output and R_F modulation in one UI

phase range. Assuming the resistor value of the ideal switches are negligible, R_F and ζ change along the UI between $\{0.89\ k\Omega,\ 100\ k\Omega\}$ and $\{0.1,\ 1\}$ respectively.

The VEO and output noise voltage of the LPTV TIA with R_F modulation by a square wave signal are shown in Fig. 4.6, over one unit interval. At a sampling time of 0.5 UI, the system reaches to its maximum vertical eye opening gain of 1.78 $k\Omega$. The input-referred noise current at this sampling time is 0.7 μA_{rms}. By increasing rise/fall times of the modulation signal to 0.25 UI, VEO gain and input-referred noise current change to 1.72 $k\Omega$ and 0.85 μA_{rms}. For the $V_{CDR} = 25\ mV$, the sensitivity of the system computed by Eq. 2.50 is 23.85 μA_{pp}.

The single pulse response of the system is shown in Fig. 4.7 for a current with the peak-to-peak amplitude of 4.45 μA and the pulse width of 100 ps. The pulse response gain of the TIA is 2.13 $k\Omega$. The effective gain of the system, VEO gain, has a smaller value due to the presence of ISI.

The maximum value of the ISI is given by Eq. 2.10 as

$$ISI_{MAX} = 0.4 + 0.7 + 0.5 = 1.6\ mV \tag{4.11}$$

And the VEO gain of the circuit is computed using the ISI_{MAX} by Eq. 2.11

$$Z_{VEO} = \frac{9.5 - 1.6}{4.45} = 1.78\ k\Omega \tag{4.12}$$

which has the same result compared to calculated VEO gain in Fig 4.5.

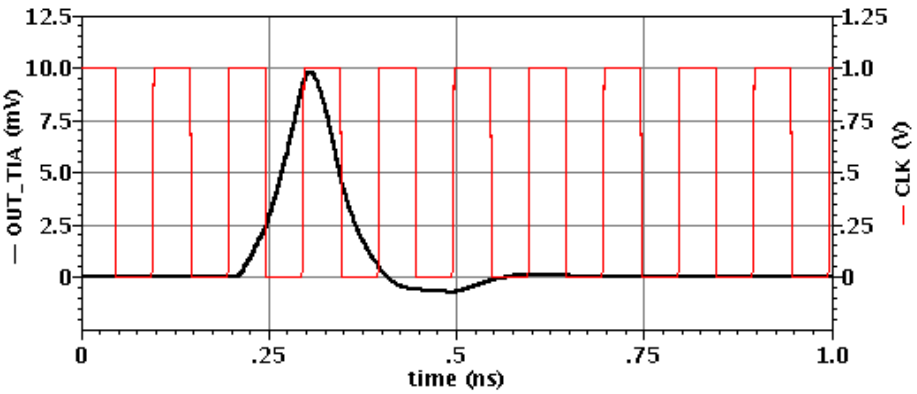


Figure 4.7: Pulse response of the shunt-feedback TIA with cross-coupled inverters at the output, $W_1 = 30\ \mu m$, $W_2 = 4.5\ \mu m$, $R_{F1} = 100\ k\Omega$, $R_{F2} = 0.9\ k\Omega$, $t_d = 10\ ps$ and $f_{bit} = 10\ Gb/s$

Also, to calculate the receiver sensitivity, the power penalty is obtained by Eq. 2.51 as

$$PP = 1 + \frac{25}{14 \times 0.7 \times 1.78} = 2.43 \tag{4.13}$$

Using Eq. 2.50 the receiver sensitivity becomse

$$i_{pp,min} = 14 \times 0.7 \times 2.43 = 23.85\ \mu A_{pp} \tag{4.14}$$

To reach BER of 10^{-12} at the receiver, the minimum required peak-to-peak current value of 23.85 μA_{pp} is needed.

To conclude the transistor-level designed TIA, shunt-feedback resistor modulation increased the effective gain of the system compared to the reference LTI TIAs as well as the gain to power ratio. In addition, using R_F modulation decreased the input-referred noise current value and improved the sensitivity of the system.

4.2 Modulation by a sine wave signal [8]

The previous section showed that by switching the shunt-feedback resistor, the minimum achievable value of the damping factor has limitation and it is not possible to reach close to zero and negative values. The next adjustable parameter to modulate the damping factor is the output transconductance of the TIA based on Eq. 2.39. The high-level and transistor-level schematics of the differential shunt-feedback TIA with the cross-coupled inverters and M_r to realize damping factor modulation are

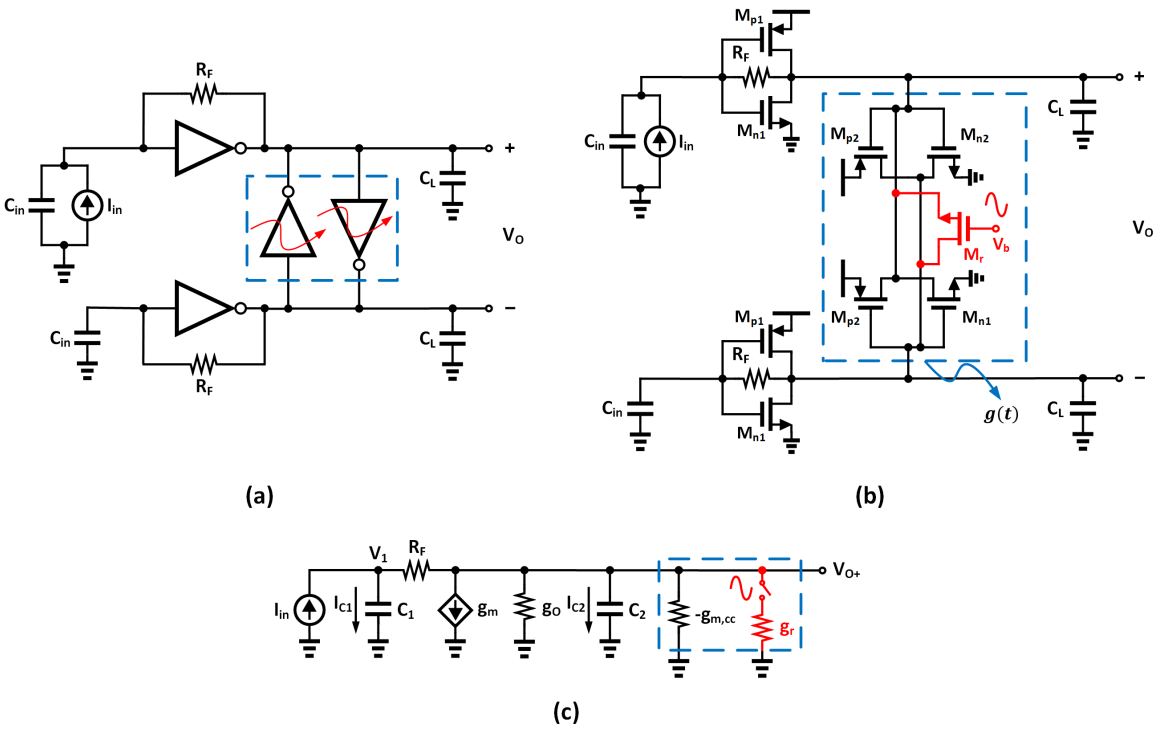


Figure 4.8: Differential shunt-feedback TIA including transconductance modulation by a *sin* wave signal at the output ($V_b = B + A\ sin(2\pi f_{bit} + \phi_{start})$) (a) high-level schematic (b) transistor-level schematic (c) ac small-signal model of the differential half of circuit

shown in Fig. 4.8 (a) and (b). M_r is working in the triode region since the differential dc value of the output voltage is 0 ($V_{DS,r} = 0\ V$). Ignoring the DC and Offset compensation circuits, C_{in} includes the capacitance of the PD and the capacitance of the TIA's input pad, and C_L is the load capacitance the TIA drives. To explore the performance of the TIA with dynamic damping factor (output conductance modulation), M_r is biased by a sinusoidal wave at the frequency of the input data rate.

$$V_b = B + A\ sin(2\pi f_{bit} + \phi_{start}) \tag{4.15}$$

where B is the dc offset, A is the amplitude and ϕ_{start} is the initial phase of the modulation biased voltage. The damping factor of the TIA is modulated synchronously with the incoming data by the sinusodial wave.

The ac small-signal model of the differential half of circuit is shown in Fig. 4.8 (c). For simplifying the calculations, C_{gd} of the MOSFETs and capacitors of the M_r

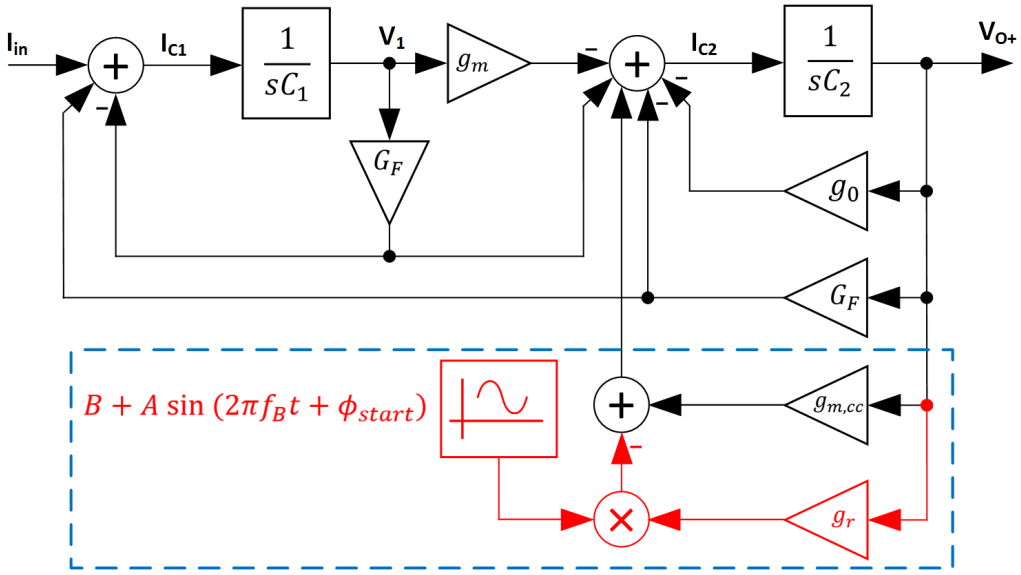


Figure 4.9: SIMULINK model of the shunt-feedback TIA with transconductance modulation by a *sin* wave signal at the output, shown in Fig. 4.8

have been ignored. Component parameters of the small-signal model are as follows:

$$C_1 = C_{gs,n1} + C_{gs,p1} + C_{in} \tag{4.16}$$

$$C_2 = C_{db,n1} + C_{db,p1} + C_{gs,n2} + C_{gs,p2} + C_{db,n2} + C_{db,p2} + C_L \tag{4.17}$$

$$g_m = g_{m,n1} + g_{m,p1} \tag{4.18}$$

$$g_o = g_{o,n1} + g_{o,p1} \tag{4.19}$$

where g_o is the output conductance of the main inverters. The overall transcondutce of the cross-coupled inverters and the triode region transsior M_r is given as

$$g(t) = -g_{m,cc} + g_r\big(B + A\ sin(2\pi f_{bit} + \phi_{start})\big) \tag{4.20}$$

where $g_{m,cc}$ is the transconductance of the cross-coupled inverters, and g_r is the transconductance of the M_r biased by V_b.

The SIMULINK model of the TIA is developing by s-domain equations as

$$v_1 = \frac{i_{C_1}}{sC_1} \quad \text{where} \quad i_{C_1} = i_{in} + \frac{v_{o+} - v_1}{R_F} \tag{4.21}$$

$$v_{o+} = \frac{i_{C_2}}{sC_2} \quad \text{where} \quad i_{C_2} = \frac{v_1 - v_{o+}}{R_F} - g_m v_1 - \big(g_o + g(t)\big)v_{o+} \tag{4.22}$$

where $G_F = 1/R_F$ and $g(t)$ denotes the overall conductance of the cross-coupled inverters and the triode region transistor indicated in the blue box.

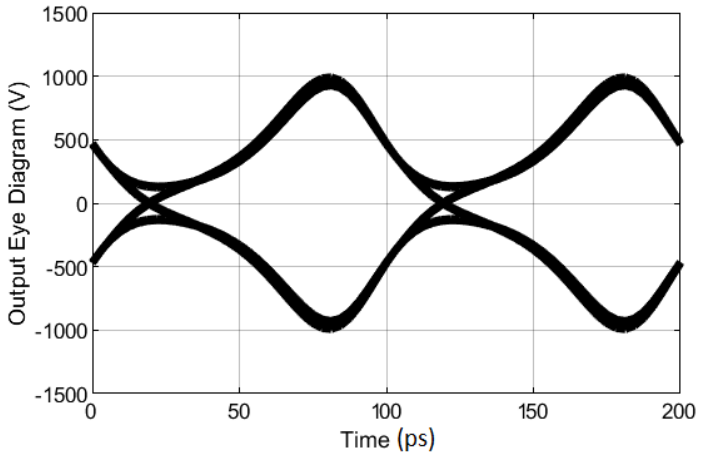


Figure 4.10: Output eye diagram of the shunt-feedback TIA model in SIMULINK with transconductance modulation by a *sin* wave signal at the output (Fig. 4.9) for input data with peak to peak amplitude of 1 A, $g_{m,cc} = 1\mho$, $G_F = 1\ m\mho$, $g_r = 1\ m\mho$, $A = 3$, $B = -0.2$, $\phi_{start} = 0.6\ rad$ and $f_{bit} = 10\ Gb/s$

Fig. 4.10 shows the output of the SIMULINK model of the shunt-feedback TIA with cross-coupled inverters whose output conductance is modulated. Transistor parameters are corresponding to $W_{n1} = W_{n2} = W_1 = 20\ \mu m$ in a 65 nm technology and for the feedback resistor of $R_F = 1\ k\Omega$; the cross-coupled inverters have a conductance of $-1\ m\mho$ and conductance of the triode region transistor is $g_r = 1\ m\mho$. The values were a dc offset of -0.2, an amplitude of 3 and an initial phase of 0.64 rad. By modulating the damping factor, the VEO doubles to 1800 V compared to the SIMULINK model of the TIA with cross-coupled inverters. The damping factor ranges from -0.28 to 1.26. The system, no longer time-invariant, is nevertheless linear.

Assuming M_r is in triode region, the transconductance of the cross-coupled circuit is given by:

$$g(t) = -g_{m,cc} + \mu_n C_{ox} \frac{W_r}{L} \big(B + A\ sin(2\pi f_{bit} + \phi_{start}) - V_{O,DC} - V_{t,n}\big) \qquad (4.23)$$

Therefore the total conductance of the cross-coupled inverters and M_r is modulated by the *sin* wave. By selecting appropriate values for W_2, W_r, B, A and ϕ_{start}, the damping factor of the system swings between negative and positive values. The output eye digram of the LPTV system and the *sin* wave modulation signalare shown in Fig. 4.11. Here, $W_{n1} = W_{p1} = W_1 = 30\ \mu m$, $W_{n2} = W_{p2} = W_2 = 15\ \mu m$, $W_r = 4\ \mu m$, $R_F = 1.4\ k\Omega$ and $V_b = 1.15 + 0.3\ sin(2\pi f_{bit} + 310°)\ V$. This corresponds to variations in g and ζ along the UI of $-8.9\ m\mho < g < 18.8\ m\mho$ and $-0.42 < \zeta < 3.5$ each unit

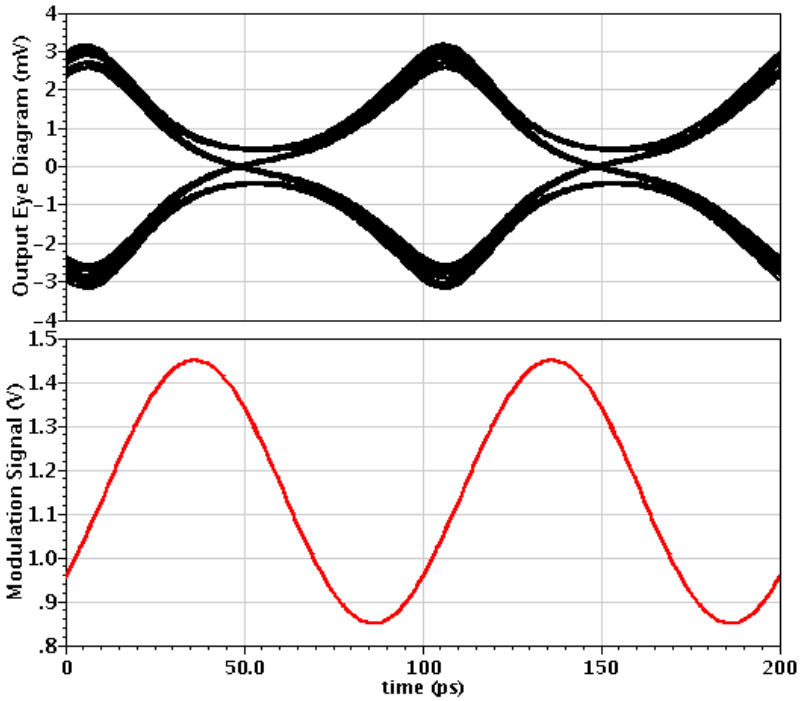


Figure 4.11: Output eye diagram of the shunt-feedback TIA with transconductance modulation by a *sin* wave signal at the output, the sinusoidal wave modulation signal, $W_1 = 30\ \mu m$, $W_2 = 15\ \mu m$, $W_r = 4\ \mu m$ $R_F = 1.4\ k\Omega$, $A = 0.3\ V$, $B = 1.15\ V$, $\phi_{start} = 310°$ and $f_{bit} = 10\ Gb/s$

interval.

Using transient noise simulations and Eq. 2.49 to determine noise performance of the system, the VEO and output noise voltage of the damping factor modulated TIA by the *sin* wave in one unit interval are shown in Fig. 4.12. The maximum vertical eye opening gain is 2.62 $k\Omega$ at a sampling time of 0.57 UI. The input-referred noise current at this sampling time is 0.9 μA_{rms}. Although the proposed technique of damping factor modulation requires a signal synchronous with the incoming data, the gain of the LPTV system is higher than 2.5 $k\Omega$ over a range of more than 45°, allowing generation from a 4-stage differential ring oscillator.

Fig. 4.13 shows the single pulse response of the *sin* wave modulated damping TIA for a current with the peak-to-peak amplitude of 4.45 μA and the pulse width of 100 ps besides the modulation signal. Injecting the pulse current, the system starts to work in the low damping region; the system has a fast response and high gain, which increased the peak value and height of the pulse response. Before reaching the peak

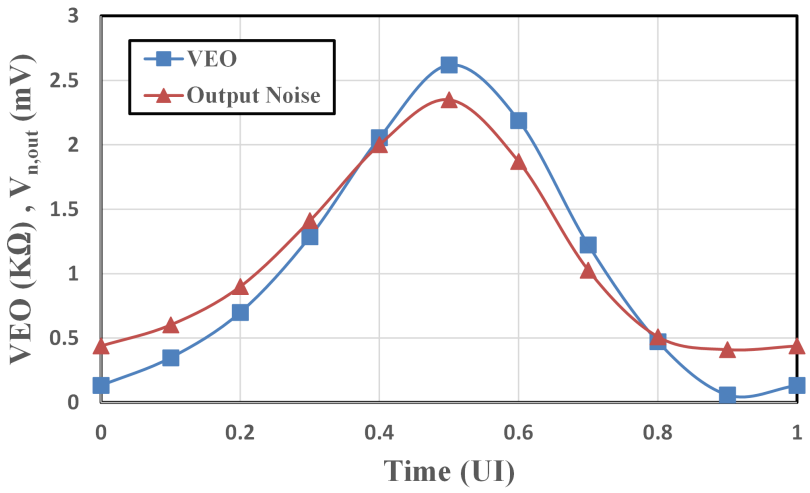


Figure 4.12: VEO and output noise voltage of the modulated damoing factor TIA by a *sin* wave in one UI

value, the system goes to the high damped region and removes the ISI generated by the underdamped system. The pulse response gain of the TIA is 2.92 $k\Omega$. To obtain the effective gain of the system (Z_{VEO}), first, the maximum value of the ISI needs to be calculated. Using the Eq. 2.10

$$ISI_{MAX} = 0.1 + 0.2 + 0.6 + 0.45 = 1.35\ mV \tag{4.24}$$

And Eq. 2.11 gives us the VEO gain value of the modulated damping TIA

$$Z_{VEO} = \frac{13 - 1.35}{4.45} = 2.61\ k\Omega \tag{4.25}$$

which approves the result of the output eye diagram in Fig 4.11.

To compare the performance of the damping factor modulation on the sensitivity of the receiver, Eq. 2.51 calculates the power penalty as

$$PP = 1 + \frac{25}{14 \times 0.9 \times 2.62} = 1.75 \tag{4.26}$$

And the sensitivity of the receiver, using Eq. 2.50, to reach BER of 10^{-12} becomes

$$i_{pp,min} = 14 \times 0.9 \times 1.75 = 22.14\ \mu A_{pp} \tag{4.27}$$

Therefore, the minimum required peak-to-peak current value of 23.85 μA_{pp} is needed at the input of the proposed TIA.

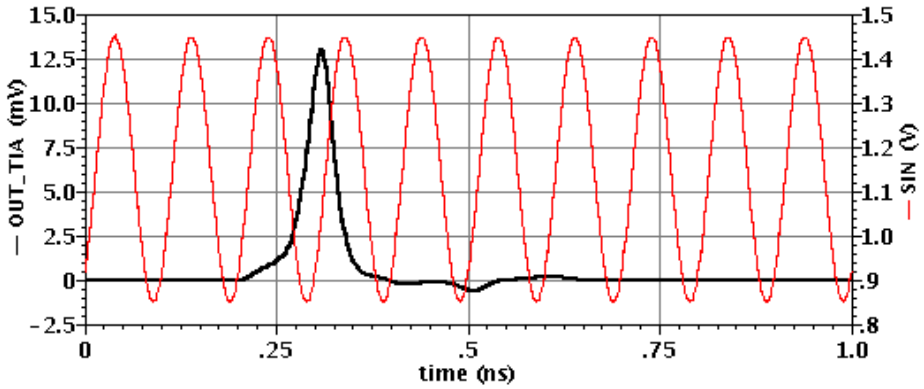


Figure 4.13: Pulse response of the shunt-feedback TIA with transconductance modulation by a sin wave signal at the output, the sinusoidal wave modulation signal, $W_1 = 30\ \mu m$, $W_2 = 15\ \mu m$, $W_r = 4\ \mu m$ $R_F = 1.4\ k\Omega$, $A = 0.3\ V$, $B = 1.15\ V$, $\phi_{start} = 310°$ and $f_{bit} = 10\ Gb/s$

The LPTV system has an $I_{n,in}$ degradation of 0.85 dB compared to the cross-coupled inverter-based TIA. The net performance improvement in dB is given by the difference between the improvement in power penalty and the degradation in $I_{n,in}$:

$$Net\ improvement = PP\ improvement - I_{n,in}\ degradation \tag{4.28}$$

Fig. 4.14 shows the results of the net improvement for minimum clock-and-data recovery voltage swing over a range of 5 mV to 55 mV. Notice that for all but the smallest values of V_{CDR} the proposed technique provides a net improvement.

Design of the shunt-feedback TIA with output conductance modulation by a *sin* wave, by adding large cross-coupled inverters and M_r, increases the output noise voltage. The input-referred noise current is larger compared to the reference design with cross-coupled inverters but no modulation. However, damping factor modulation provides significantly increased VEO gain eliminating the need for extra stages of amplification. The highest value of the Gain/Power ratio is obtained by the LPTV system implying that having a variable damping factor decreases the power dissipation of the overall receiver. And the proposed modulated damping TIA improved the sensitivity and net performance of the system for reasonable values of the V_{CDR}.

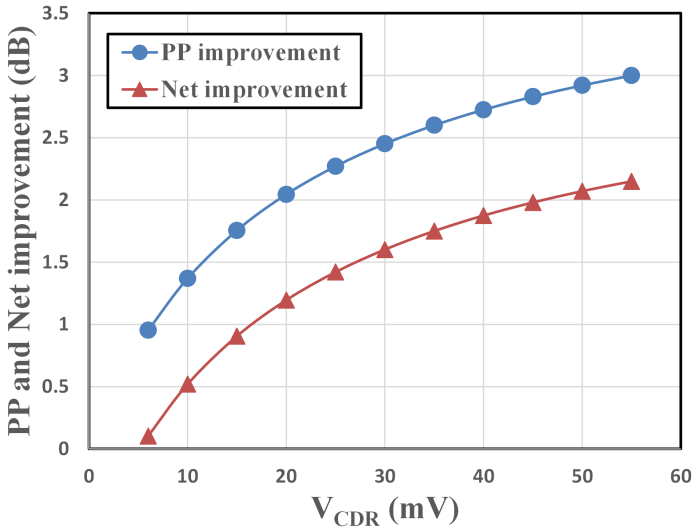


Figure 4.14: Power Penalty (PP) and net performance improvement of the TIA with damping factor modulation with *sin* wave compared to the TIA with cross-coupled inverters at the output over a range of minimum clock-and-data recovery voltage swing

4.3 Modulation by a rail-to-rail square wave signal [9]

In this section, the modulation voltage is simplified to a rail-to-rail square-wave signal. Therefore, the damping factor switches between two discrete values each UI. Using a square-wave signal removes the complexity of generating a sinusoidal signal with a particular DC offset and amplitude. The high-level and transistor-level schematics of the differential shunt-feedback TIA with at the output are shown in Fig. 4.15 (a) and (b). M_r is working in the triode region since the differential dc value of the output voltage is 0 ($V_{DS,r} = 0\ V$). Ignoring the DC and Offset compensation circuits, C_{in} includes the capacitance of the PD and the capacitance of the TIA's input pad, and C_L is the load capacitance the TIA drives. Compared to the system with the damping factor modulation by the *sin* wave, the system remains in the regeneration region or negative damping factor region during a half portion of the UI. Therefore, we decrease the size of cross-coupled inverters and enlarge the size of triode region transistor (M_r), which is biased by the modulation signal, a rail-to-rail square wave signal with peak-to-peak amplitude of V_{DD}:

$$V_b = V_{DD} \sum p(t - kT_b - t_d) \tag{4.29}$$

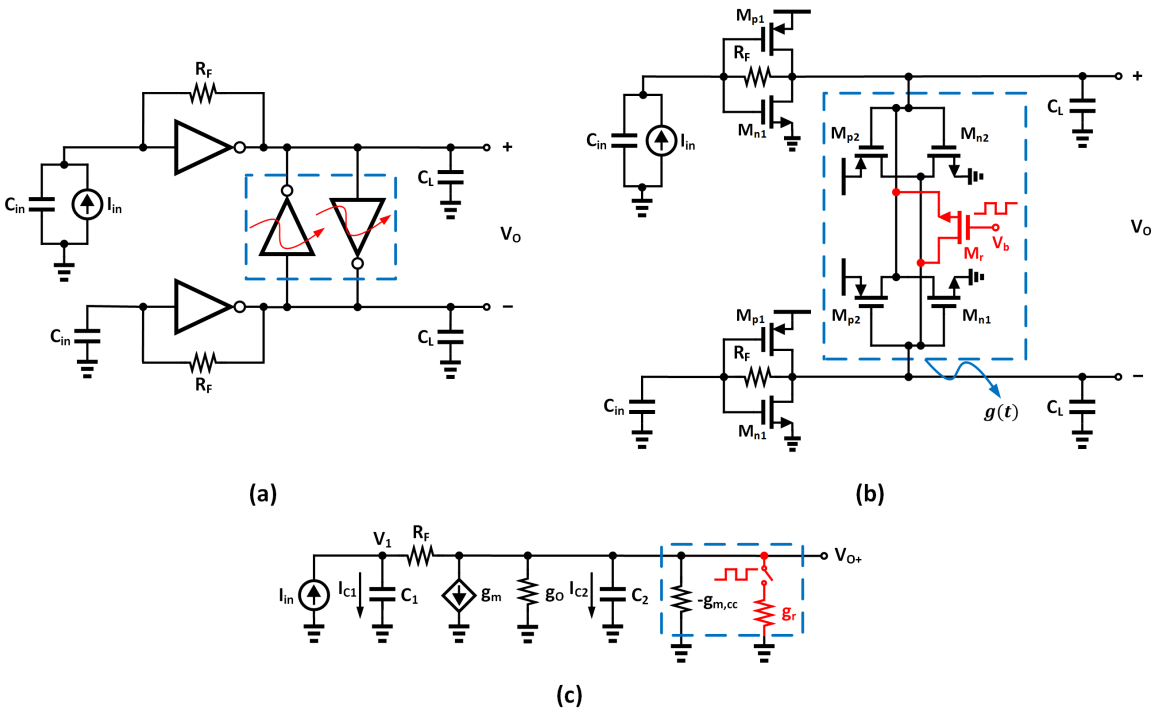


Figure 4.15: Differential shunt-feedback TIA including transconductance modulation by a rail-to-rail square wave signal at the output ($V_b = V_{DD} \sum p(t - kT_b - t_d)$) (a) high-level schematic (b) transistor-level schematic (c) ac small-signal model of the differential half of circuit

where p(t) denotes the unit-amplitude pulse with 50 % duty cycle, and t_d is the initial delay time.

The ac small-signal model of the differential half of circuit is shown in Fig. 4.15 (c). For simplifying the calculations, C_{gd} of the MOSFETs and capacitors of the M_r have been ignored. Small-signal model component parameters are as follows:

$$C_1 = C_{gs,n1} + C_{gs,p1} + C_{in} \tag{4.30}$$

$$C_2 = C_{db,n1} + C_{db,p1} + C_{gs,n2} + C_{gs,p2} + C_{db,n2} + C_{db,p2} + C_L \tag{4.31}$$

$$g_m = g_{m,n1} + g_{m,p1} \tag{4.32}$$

$$g_o = g_{o,n1} + g_{o,p1} \tag{4.33}$$

where g_o is the output conductance of the main inverters. The overall transcondutce of the cross-coupled inverters and the triode region transsior M_r is given as

$$g(t) = -g_{m,cc} + g_r \sum p(t - kT_b - t_d) \tag{4.34}$$

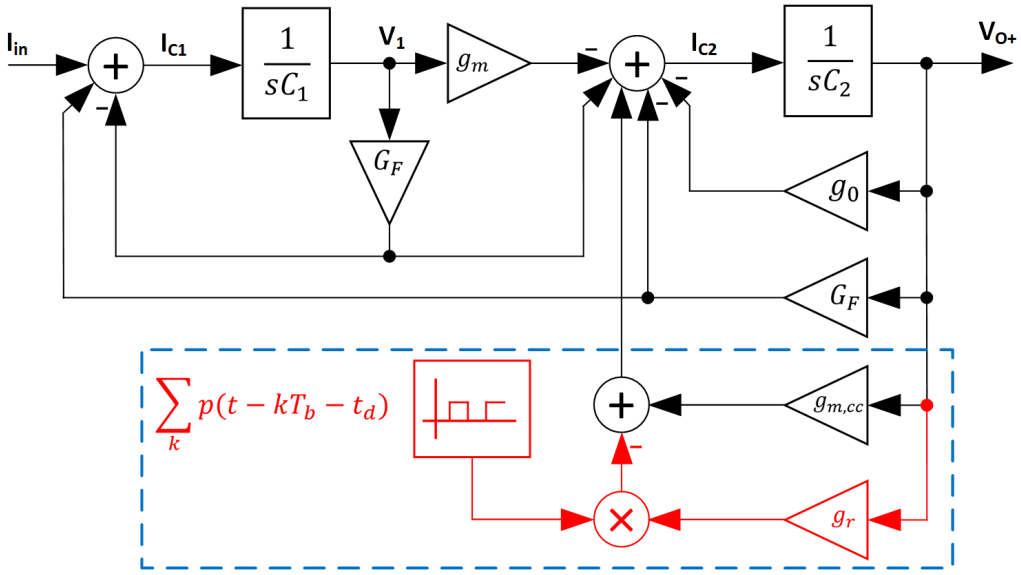


Figure 4.16: SIMULINK model of the shunt-feedback TIA with transconductance modulation by a rail-to-rail square wave signal at the output, shown in Fig. 4.15

where $g_{m,cc}$ is the transconductance of the cross-coupled inverters, and g_r is the transconductance of the M_r biased by V_{DD}.

Using the s-domain equations to develop a SIMULINK model:

$$v_1 = \frac{i_{C_1}}{sC_1} \quad \text{where} \quad i_{C_1} = i_{in} + \frac{v_{o+} - v_1}{R_F} \tag{4.35}$$

$$v_{o+} = \frac{i_{C_2}}{sC_2} \quad \text{where} \quad i_{C_2} = \frac{v_1 - v_{o+}}{R_F} - g_m v_1 - \big(g_o + g(t)\big)v_{o+} \tag{4.36}$$

These equations are represented in a behavioral model shown in Fig. 4.16 where $G_F = \frac{1}{R_F}$.

Fig. 4.17 shows the output of the SIMULINK model of the shunt-feedback TIA with cross-coupled inverters whose output conductance is modulated by the rail-to-rail square-wave signal (Eq. 4.34). Transistor parameters are corresponding to $W_{n1} = W_{n2} = W_1 = 20\ \mu m$ in a 65 nm technology and for the feedback resistor $R_F = 1\ k\Omega$; the cross-coupled inverters have a conductance of $g_{m,cc} = 4.4\ m\mho$, conductance of the triode region transistor is $g_r = 3.3\ m\mho$ and initial delay time of the modulation signal is $t_d = 69\ ps$. By switching ζ between negative (-0.01) and positive (0.75) values each unit interval, the VEO increases to 2000 V. The system, no longer time-invariant, remains linear.

To explore the performance of the TIA with dynamic damping factor (output conductance modulation), the gate of M_r is driven by a rail-to-rail square wave voltage

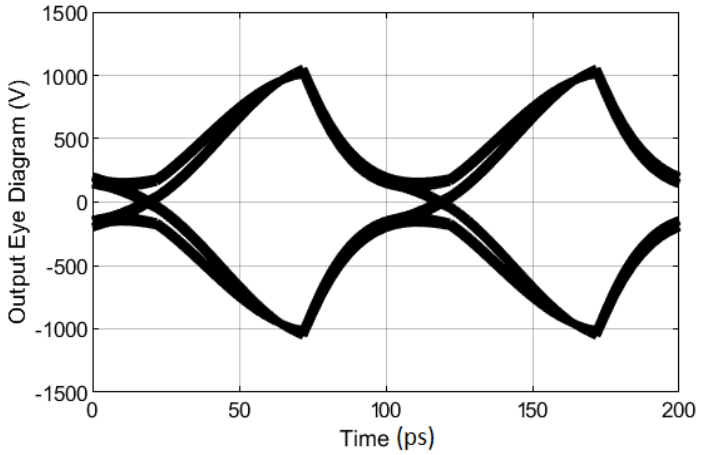


Figure 4.17: Output eye diagram of the shunt-feedback TIA model in SIMULINK with transconductance modulation by a rail-to-rail square wave signal at the output (Fig. 4.16) for input data with peak to peak amplitude of 1 A, $g_{m,cc} = 4.4\ m\mho$, $G_F = 1\ m\mho$, $g_r = 3.3\ m\mho$, $t_d = 69\ ps$ and $f_{bit} = 10\ Gb/s$

expressed in Eq. 4.29. The total output conductance of the TIA is expressed by:

$$g_{o,tot}(t) = g_o + g(t) \tag{4.37}$$

where $g(t)$ is the total conductance of the cross-coupled inverters and M_r is modulated by the square wave (the cross-coupled circuit in the blue box). The overall transconductance of the cross-coupled circuit is given by:

$$g(t) = -g_{m,cc} + \left(\mu_n C_{ox}\frac{W_r}{L}(V_{DD} - V_{O,DC} - V_{t,n})\right)\sum p(t - kT_b - t_d) \tag{4.38}$$

Therefore the total conductance of the cross-coupled circuit is modulated by the square wave yielding two values of g:

$$g = \begin{cases} -g_{m,cc} & \text{when } V_b = 0 \\ -g_{m,cc} + \mu_n C_{ox}\frac{W_r}{L}[V_{DD} - V_{O,DC} - V_{t,n}] & \text{when } V_b = V_{DD} \end{cases} \tag{4.39}$$

By selecting appropriate values for W_2, W_r, and t_d, the damping factor of the system swings between negative and positive values. The output eye diagram of the LPTV system and the rail-to-rail square wave madulation signal are shown in Fig. 4.18. Here, $f_{bit} = 10$ Gb/s, $W_{n1} = W_{p1} = W_1 = 30\ \mu m$, $W_{n2} = W_{p2} = W_2 = 11\ \mu m$, $W_r = 20\ \mu m$, $t_d = 5\ ps$, $R_F = 1.4\ k\Omega$ and rise/fall times of the modulation signal is 0.15 UI. g and ζ change along the UI between $\{-5.4\ m\mho, 9.2\ m\mho\}$ and

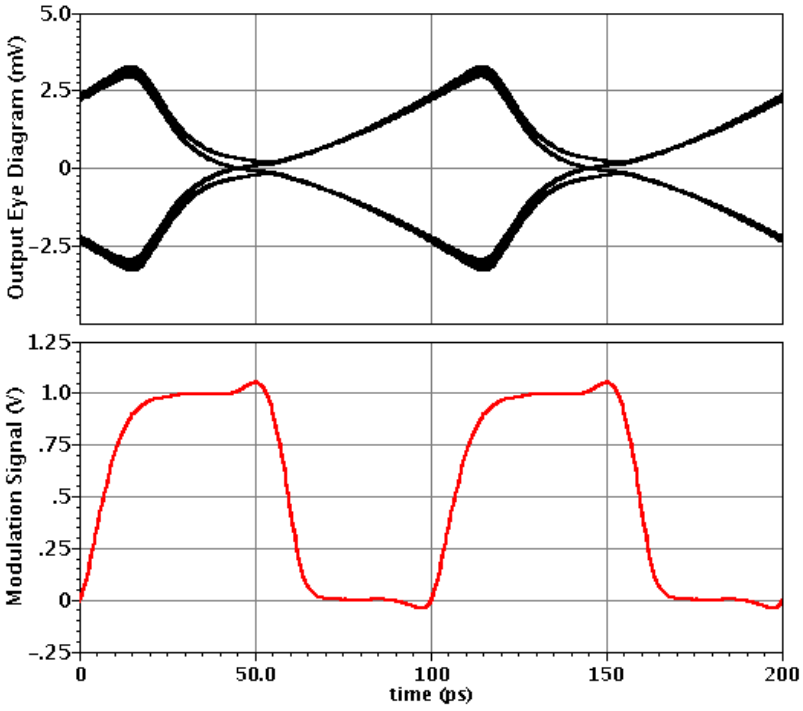


Figure 4.18: Output eye diagram of the shunt-feedback TIA with transconductance modulation by a rail-to-rail square wave signal at the output, the rail-to-rail square wave modulation signal, $W_1 = 30\ \mu m$, $W_2 = 11\ \mu m$, $W_r = 20\ \mu m$ $R_F = 1.4\ k\Omega$, $t_d = 5\ ps$ and $f_{bit} = 10\ Gb/s$

$\{-0.15, 2.5\}$. The gain of the system is higher than 2.25 $k\Omega$ over a range of more than 12.5 ps delay variation of the signal $p(t)$, corresponding to a 45° phase range.

The output noise voltage of the LPTV system modulated by a square wave signal with rise/fall times of 0.15 UI, using transient noise simulations and Eq. 2.49, and VEO of the system are shown in Fig. 4.19, over one unit interval. At a sampling time of 0.7 UI, the system reaches to its maximum vertical eye opening gain of 2.98 $k\Omega$. The input-referred noise current at this sampling time is 0.66 $\mu\mathrm{A_{rms}}$. By changing rise/fall times of the modulation signal from 0.15 UI to 0.25 UI, VEO gain and input-referred noise current range from 2.98 $k\Omega$ to 2.89 $k\Omega$ and 0.66 $\mu\mathrm{A_{rms}}$ to 0.8 $\mu\mathrm{A_{rms}}$.

Fig. 4.20 shows the single pulse response of the square wave modulated damping TIA for a current with the peak-to-peak amplitude of 4.45 μA and the pulse width of 100 ps besides the modulation signal. The pulse response gain of the TIA is 3.09 $k\Omega$. Detailed pulse response analysis is discussed in the next section. To obtain the effective gain of the system (Z_{VEO}), first, the maximum value of the ISI needs to

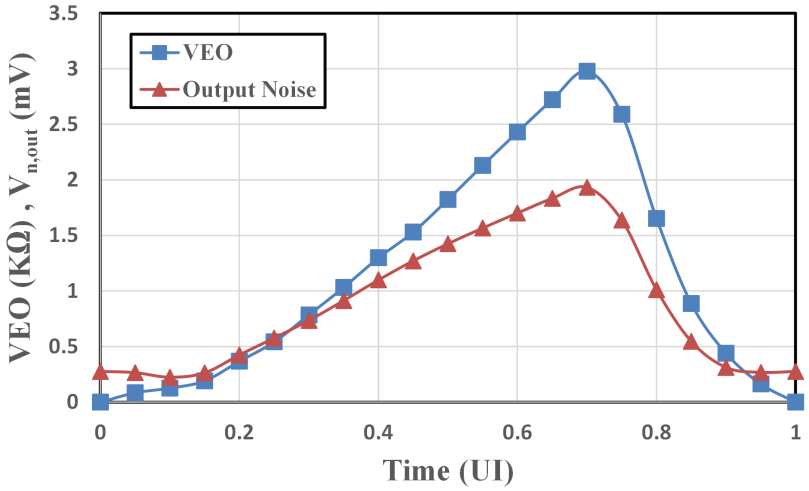


Figure 4.19: VEO and output noise voltage of the modulated damping factor TIA by a square wave in one UI

be calculated. Using the Eq. 2.10

$$ISI_{MAX} = 0.45 + 0.25 + 0.25 = 0.95\ mV \tag{4.40}$$

And Eq. 2.11 gives us the VEO gain value of the modulated damping TIA

$$Z_{VEO} = \frac{13.75 - 0.95}{4.45} = 2.87\ k\Omega \tag{4.41}$$

which approves the result of the output eye diagram in Fig 4.11.

To compare the performance of the damping factor modulation on the sensitivity of the receiver, Eq. 2.51 calculates the power penalty as

$$PP = 1 + \frac{25}{14 \times 0.66 \times 2.98} = 1.9 \tag{4.42}$$

And the sensitivity of the receiver, using Eq. 2.50, to reach BER of 10^{-12} becomes

$$i_{pp,min} = 14 \times 0.66 \times 1.9 = 17.63\ \mu A_{pp} \tag{4.43}$$

Therefore, the minimum required peak-to-peak current value of 17.63 μA_{pp} is needed at the input of the proposed TIA.

To calculate the net performance improvement in dB

$$Net\ improvement = PP\ improvement \pm I_{n,in}\ changes \tag{4.44}$$

Fig. 4.21 shows net performance improvement of LPTV systems with damping factor modulation by *sin* and square wave signals, for a range of 5 mV to 55 mV minimum

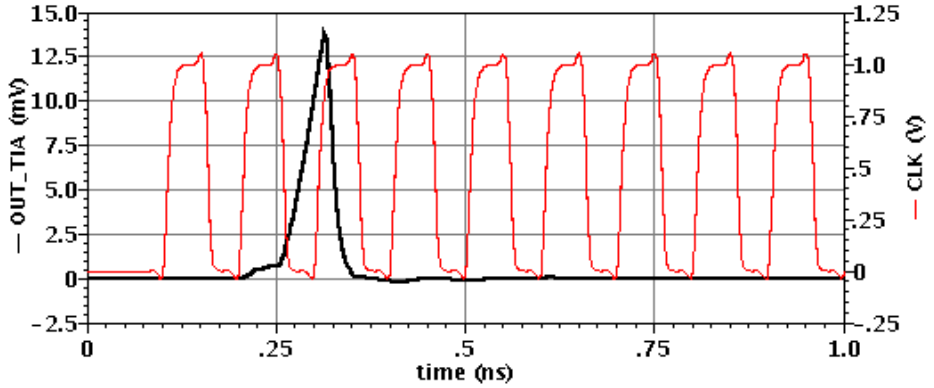


Figure 4.20: Pulse response of the shunt-feedback TIA with transconductance modulation by a rail-to-rail square wave signal at the output, the rail-to-rail square wave modulation signal, $W_1 = 30\ \mu m$, $W_2 = 11\ \mu m$, $W_r = 20\ \mu m$ $R_F = 1.4\ k\Omega$, $t_d = 5\ ps$ and $f_{bit} = 10\ Gb/s$

clock-and-data recovery voltage swing. Compared to the cross-coupled inverter-based TIA, the LPTV system with *sin* wave modulation signal and the LPTV system with square wave modulation signal have $I_{n,in}$ degradation of 0.85 dB and $I_{n,in}$ improvement of 0.5 dB. The LPTV system with *sine* wave modulation has a more significant power penalty improvement than the LPTV system with a square wave modulation signal. But, due to the input-referred noise current degradation using *sin* wave for modulation, the net performance improvement of the LPTV system has a higher value by using the square wave signal modulation.

Table 4.1 summarizes linear periodically time-varying shunt-feedback transimpedance amplifier (LPTV SF-TIA) designs. In the previous section, a sinusoidal wave performed damping-factor modulation but in this work, a rail-to-rail square wave was used. This modification to the modulation signal removes the complexity of generating a sine wave with appropriate DC offset, amplitude and phase, replacing it with a square wave where only phase adjustment is necessary. The proposed modulation signal increases the shunt-feedback TIA's effective gain from 1.25 $k\Omega$ to 2.98 $k\Omega$. The input-referred noise current of the LPTV system modulated by a square wave is lower compared to the reference design with cross-coupled inverters, R_F modulated system and the LPTV system modulated by a sine wave. Also, using a rail-to-rail square wave increased VEO gain and the value of the Gain/Power ratio. The LPTV system modulated by a square wave gives better sensitivity compared to the reference design with cross-coupled inverters and the LPTV systems, R_F modulated and damping

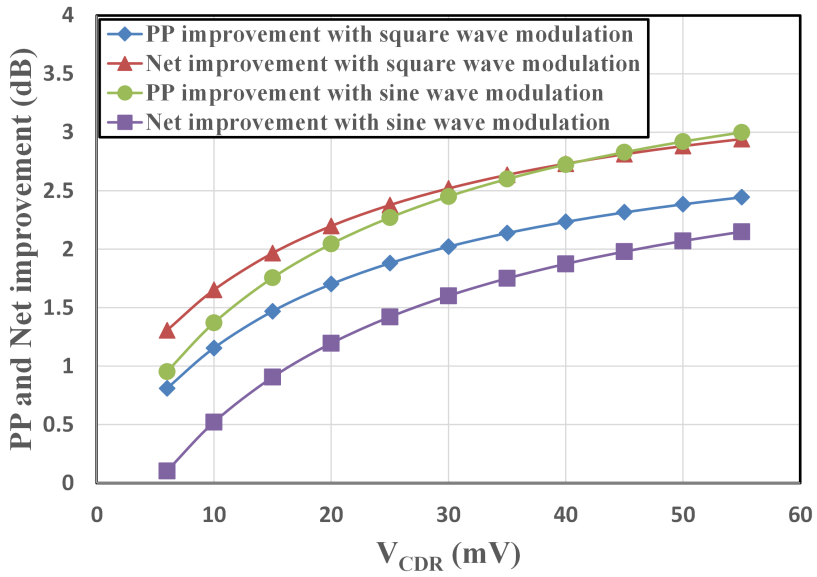


Figure 4.21: Power Penalty (PP) and net performance improvement of the TIA with damping factor modulation by *sin* and rail-to-rail square waves compared to the TIA with cross-coupled inverters at the output over a range of minimum clock-and-data recovery voltage swing

factor modulated by a sine wave.

Table 4.1: Results summary of LPTV shunt-feedback TIA design

LPTV SF-TIA including:	R_F switching	Damping factor modulation by sine wave	Damping factor modulation by square wave
Size of transistors (μm)	$W_1 = 30$ $W_2 = 4.5$	$W_1 = 30$ $W_2 = 15$ $W_r = 4$	$W_1 = 30$ $W_2 = 11$ $W_r = 20$
R_F (kΩ)	{0.9,100}	1.4	1.4
Data rate (Gb/s)	10	10	10
f_{3dB} (GHz)	—	—	—
AC gain (kΩ)	—	—	—
Pulse gain (kΩ)	2.13	2.92	3.09
VEO gain (kΩ)	1.78	2.62	2.98
$I_{n,in}$ (μA_{rms})	0.7	0.9	0.66
Power (mW)	4.03	5.29	4.81
Gain/Power ratio (kΩ/mW)	0.44	0.5	0.62
$i_{pp,min}$ (μA_{pp}) for $V_{CDR} = 25$ mV	23.85	22.14	17.63

4.3.1 Pulse response analysis

Fig. 4.22 shows the enlarged pulse response of the LPTV shunt-feedback TIA modulated by a square wave, the input pulse current with the peak-to-peak amplitude of 20 μA and the input voltage of the TIA. To investigate pulse response analysis of the system, ac small-signal model of the TIA is shown in Fig. 4.23. Where I_{in} is the input current source, C_1 is the overall capacitors at the input node, C_2 is the overall capacitors at the output node, g_o is the output conductance of the main inverters, $g_{m,cc}$ is the transconcductance of the corss-coupled inverters. When the input current is injected at the input, the bias voltage (V_b) of the triode region transistor has the value of V_{DD}, and the TIA operates in high damping mode. The ac small-signal model of the TIA is shown in Fig. 4.23 (a), where a resistor models the triode region transistor with the vale of g_r. After about 0.5 UI, the value of the V_b changes to 0 and the system switches to the low damping factor operation mode. Fig. 4.23 (b)

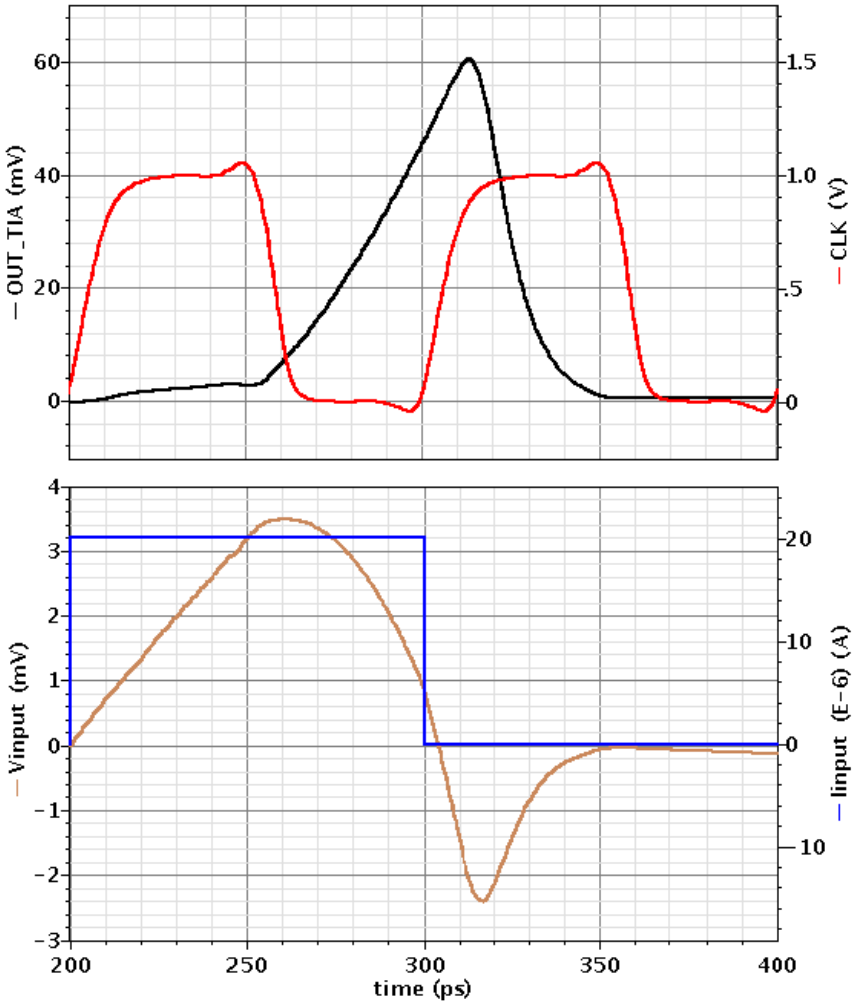


Figure 4.22: The magnified pulse response of the modulated damping shunt-feedback TIA shown in Fig. 4.20, including the modulation signal, the input pulse current and input voltage of the TIA

shows the ac small-signal model of the low damping TIA. Then, after one UI from the injection of input current, the value of I_{in} goes to 0 and V_b returns to V_{DD}. Now, the triode region transistor is modeled by the (g_r) and an initial dc voltage ($V_{o,peak}$) models the final value of the output voltage in the previous operation mode shown in Fig. 4.23 (c).

In general, we can obtain the poles of the system using the damping factor (Eq. 2.39) and the natural frequency (Eq. 2.38), given by

$$p_{1,2} = (-\zeta \pm \sqrt{\zeta^2 - 1})\omega_n \tag{4.45}$$

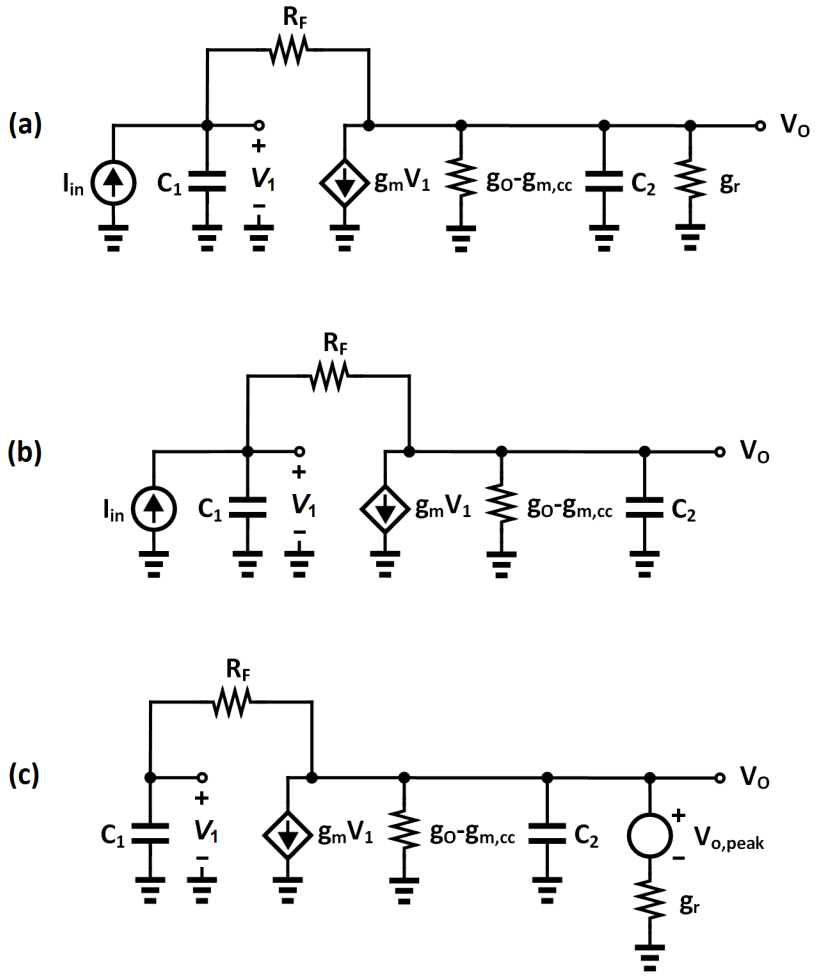


Figure 4.23: Ac small-signal model of the SF-TIA with damping factor modulation in operation mode of (a) high damping where triode-region transistor is modeled by a resistor (g_r) (b) low damping (c) high damping where an initial dc voltage ($V_{o,peak}$) models the final value of the output voltage in the previous operation mode

where ζ is the damping factor and ω_n denotes the natural frequency of the system. Using the exact value of the poles complicates the calculations and prevents us from getting insight into the system's behaviour. Location of the poles of a 2^{nd}-order system as the damping factor goes from ∞ to 0 is shown in Fig. 4.24. At first, if we assume that in the transfer function, the damping factor is larger than 1 ($\zeta > 1$) and the condition of $p_2 \gg p_1$ is valid (p_1 is the dominant pole which determines the behaviour of the system), the denominator can be written as

$$(\frac{s}{p_1}+1)(\frac{s}{p_2}+1) = \frac{1}{p_1 p_2}s^2 + (\frac{1}{p_1}+\frac{1}{p_2})s + 1 = \frac{1}{p_1 p_2}s^2 + \frac{1}{p_1}s + 1 \qquad (4.46)$$

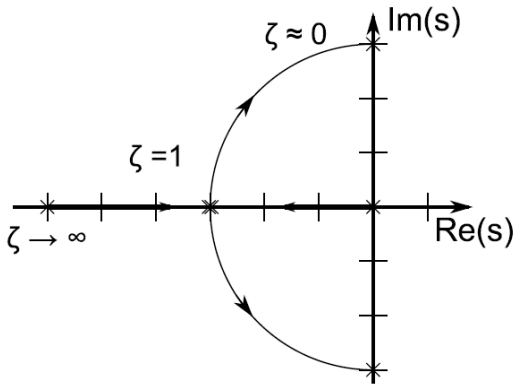


Figure 4.24: Location of the poles of a 2nd-order system as the damping factor ζ goes from ∞ to 0 [22]

By lowering ζ, the poles reach each other along the real axis. In the case of further decreases in ζ, a conjugate pole pair moves along a quarter circle to the imaginary axis and calculated as

$$p_{1,2} = (-\zeta \pm j\sqrt{1-\zeta^2})\omega_n \tag{4.47}$$

The imaginary axis forms a pole pair where $\zeta = 0$, which represents an unattenuated, periodic oscillation. And for $\zeta < 0$, system works in the regeneration region.

The input pulse current is injected from 0 to $T_b/2$ (200 ps to 250 ps), and TIA works in the high damping mode. The input node voltage of the TIA is charging by the current, and the output voltage is rising slowly. Using the small-signal model of Fig. 4.23 (a), the transfer function of the system from input current to output voltage becomes

$$\frac{V_o}{I_{in}} = \frac{R_{o1}(1-g_m R_F)}{R_F R_{o1} C_1 C_2 s^2 + \big((R_F + R_{o1})C_1 + R_{o1}C_2\big)s + 1 + g_m R_{o1}} \tag{4.48}$$

where

$$R_{o1} = \frac{1}{g_o - g_{m,cc} + g_r} \tag{4.49}$$

Since R_{o1} is small, we can rewrite the transfer function Eq. 4.48 as

$$\frac{V_o}{I_{in}} = \frac{R_{o1}(1-g_m R_F)}{R_F R_{o1} C_1 C_2 s^2 + R_F C_1 s + 1} \tag{4.50}$$

and using Eq. 4.46, poles of the system are given by

$$p_1 = \frac{1}{R_F C_1} \tag{4.51}$$

$$p_2 = \frac{1}{R_{o1} C_2} \tag{4.52}$$

After $T_b/2$ (250 ps), the system switches to the underdamped region. Input current still has the value of $20\mu A$, input node voltage discharges quickly, and the output voltage rises so fast since the TIA works in the regeneration mode ($\zeta < 0$). In addition, the modulation method is working for small and positive values of the damping factor. Therefore, assuming $0 < \zeta \ll 1$, the small-signal model of the system changes to Fig. 4.23 (b). The transfer function from input current to output voltage, until the time of T_b (300 ps), is calculated as

$$\frac{V_o}{I_{in}} = \frac{R_{o2}(1 - g_m R_F)}{R_F R_{o2} C_1 C_2 s^2 + \big((R_F + R_{o2})C_1 + R_{o2}C_2\big)s + 1 + g_m R_{o2}} \tag{4.53}$$

where

$$R_{o2} = \frac{1}{g_o - g_{m,cc}} \tag{4.54}$$

Here R_{o2} has a large value, the Eq. 4.53 can be rewritten as

$$\frac{V_o}{I_{in}} = \frac{R_{o2}(1 - g_m R_F)}{R_{o2}\big(R_F C_1 C_2 s^2 + (C_1 + C_2)s + g_m\big)} \tag{4.55}$$

Poles of the system are computed as

$$p_{1,2} = \frac{(C_1 + C_2) \pm \sqrt{\Delta}}{2R_F C_1 C_2} \tag{4.56}$$

where

$$\Delta = (C_1 + C_2)^2 - 4g_m R_F C_1 C_2 \approx C_1^2 + C_2^2 - 4g_m R_F C_1 C_2 \tag{4.57}$$

Since $g_m R_F \gg 1$, the value of the delta is negative ($\Delta < 0$). Therefore,

$$p_{1,2} = -\frac{1}{2}\frac{1}{R_F \frac{C_1 C_2}{C_1 + C_2}} \pm j\sqrt{\frac{g_m}{R_F C_1 C_2}} \tag{4.58}$$

The conjugate pole pair increases the speed of the system and the height of the pulse response. The pulse response of the TIA reaches its maximum value before switching to the next operation mode.

When T_b (300 ps), TIA returns to high damping mode, and the input current goes to 0. The discharged input voltage rises to reach 0 with a delay, and the output voltage drops so fast. The triode-region transistor is modeled by g_r shown in Fig 4.23 (c). $V_{o,peak}$ is the initial dc voltage with the final value of the output voltage in the previous operation mode. The transfer function from $V_{o,peak}$ to the V_o is given by

$$\frac{V_o}{V_{o,peak}} = \frac{1 + R_F C_1 s}{r R_F C_1 C_2 s^2 + (R_F + r + r R_F/R_{o2})C_1 s + 1 + g_m r + r/R_{o2}} \tag{4.59}$$

where $r = 1/g_r$ and R_{o2} is given by Eq. 4.54. Since R_{o2} is large enough, Eq. 4.59 becomes

$$\frac{V_o}{V_{o,peak}} = \frac{1 + R_F C_1 s}{r R_F C_1 C_2 s^2 + R_F C_1 s + 1} \tag{4.60}$$

The transfer function has a zero and two poles that are calculated using Eq. 4.46 as

$$z_1 = \frac{1}{R_F C_1} \tag{4.61}$$

$$p_1 = \frac{1}{R_F C_1} \tag{4.62}$$

$$p_2 = \frac{1}{r C_2} \tag{4.63}$$

The dominant pole is compensated by zero. The time constant of the system is $\tau = rC_2$ where the value of the r is infinitesimal, and the system is so fast. Therefore, the output pulse response returns to zero immediately when the modulation signal goes to V_{DD}.

4.4 Shunt-feedback TIA design conclusion

Chapter 3 and 4 present damping factor modulation in a 2^{nd}-order system to take advantage of both low and high damping factor systems (high-speed and low ISI). A simple shunt-feedback TIA and a shunt-feedback TIA with a cross-coupled inverter at the output are designed for minimum input-referred noise current in a 65 nm technology. Switching the feedback resistor between high and low values could increase the effective gain or VEO gain of the system and improve the input-referred noise current and sensitivity. But, raising the VEO gain has a limitation due to the limited minimum achievable value of the damping factor by modulation of the feedback resistor. By adding a time-varying resistor at the output, the damping factor of the system is changed synchronously with the incoming data, giving rise to twice the gain, and a net improvement in receiver sensitivity for reasonable output voltage swing requirements. Finally, a rail-to-rail square wave was used to modulate the damping factor of the TIA. This modification to the modulation signal removes the complexity of generating a sine wave with appropriate DC offset, amplitude and phase, replacing it with a square wave where only phase adjustment is necessary. In addition, this new design has better noise performance and VEO gain. All design parameters and simulation results are summarized in Table 4.2.

Table 4.2: Results summary of LTI and LPTV shunt-feedback TIAs design

SF-TIA including:	Main inverters	Main and X-coupled inverters	R_F modulation	Damping factor modulation by sine wave	Damping factor modulation by square wave
Size of transistors (μm)	$W_1 = 23$	$W_1 = 30$ $W_2 = 4.5$	$W_1 = 30$ $W_2 = 4.5$	$W_1 = 30$ $W_2 = 15$ $W_r = 4$	$W_1 = 30$ $W_2 = 11$ $W_r = 20$
R_F (kΩ)	1.15	1.4	{0.9,100}	1.4	1.4
Data rate (Gb/s)	10	10	10	10	10
f_{3dB} (GHz)	3.27	4.97	—	—	—
AC gain (kΩ)	0.97	1.35	—	—	—
Pulse gain (kΩ)	0.80	1.34	2.13	2.92	3.09
VEO gain (kΩ)	0.65	1.25	1.78	2.62	2.98
$I_{n,in}$ (μA_{rms})	0.94	0.74	0.7	0.9	0.66
Power (mW)	2.65	4.03	4.03	5.29	4.81
Gain/Power ratio (kΩ/mW)	0.25	0.31	0.44	0.5	0.62
$i_{pp,min}$ (μA_{pp}) for $V_{CDR} = 25$ mV	51.62	30.36	23.85	22.14	17.63

Chapter 5

Noise analysis of LPTV systems

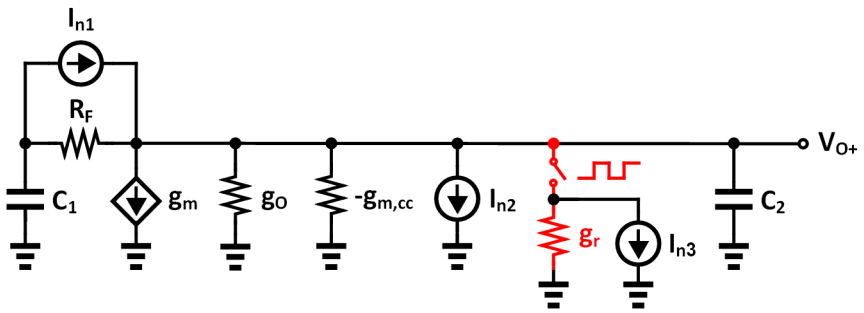


Figure 5.1: AC small-signal model, including current noise sources, of a shunt-feedback TIA with damping factor modulation by a square wave signal

LPTV TIAs in the previous sections, due to having the time-varying operating point, the output noise of the TIA varies over each UI and renders conventional ac noise analysis inaccurate. In our simulations, to obtain output noise voltage of the TIA, transient noise is used where the mean-squared output noise of the system is calculated by Eq. 2.49. [11] demonstrates that based on the multiple source LPTV network and the sampled output, it is possible to determine the equivalent LTI system to use just one time-domain simulation to analyze the circuit. This chapter shows that the proposed method of creating the equivalent LTI system based on the LPTV system works for noise analysis of LPTV TIAs and obtains the same results compared to the transient noise simulation.

Fig. 5.1 shows the ac small-signal model of the differential half of a shunt-feedback TIA with damping factor modulation by a square wave signal, including noise sources which are categorized into three different sources as:

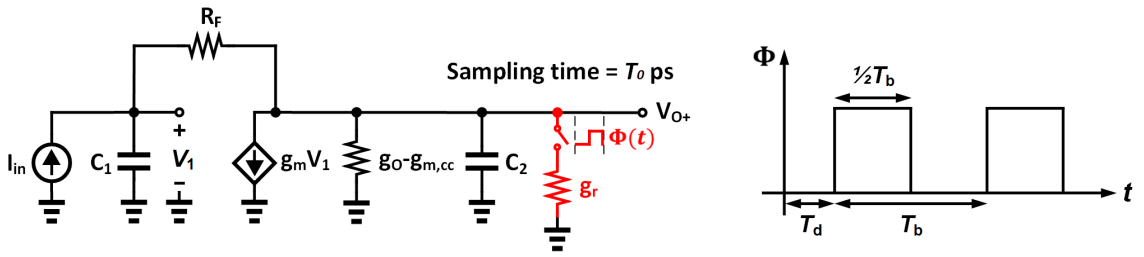


Figure 5.2: Network model ($\mathcal{N}$) of the modulated damping shunt-feedback TIA with a square wave signal shown in Fig. 5.1

- I_{n1}: current noise of the shunt-feedback resistor (R_F)
- I_{n2}: current noise associated by main and cross-coupled inverters' transistors (M_{n1}, M_{p1}, M_{n2}, M_{p2})
- I_{n3}: current noise of the triode-region transistor (M_r)

Since input and output signals are relatively small, the system is still linear. The output is the sum of the system response to each input source separately. Furthermore, each input source, noise currents, are independent. Therefore, the rms value of the output noise voltage is given by

$$V_{n,out} = \sqrt{V_{n1,out}^2 + V_{n2,out}^2 + V_{n3,out}^2} \tag{5.1}$$

where $V_{nl,out}$ denotes the rms value of the system's output noise voltage due to the lth noise source.

To investigate the calculation of the output noise in LPTV systems, using the given method in [11], the network model of the proposed square-wave modulated damping factor shunt-feedback TIA is shown in Fig. 5.2. Where $C_1 = 230\ fF$, $C_2 = 50\ fF$, $R_F = 1.4\ k\Omega$, $g_m = 22\ m\mho$, $g_o - g_{m,cc} = -1\ m\mho$, $g_r = 10\ m\mho$, $T_b = 100\ ps$, $T_d = 9\ ps$. The output eye diagram for the random input data in $f_{bit} = 10\ Gb/s$ with peak-to-peak amplitude of 2 μA is shown in Fig. 5.3. The VEO gain of the system reaches the maximum at the sampling time $T_0 = 91\ ps$ equals 3.6 $k\Omega$.

To model the equivalent noise sources of the modulated damping TIA, we use

- current noise source of R_F for I_{n1}
- current noise source of R_o for I_{n2} (where $R_o = 1/(g_o - g_{m,cc})$)

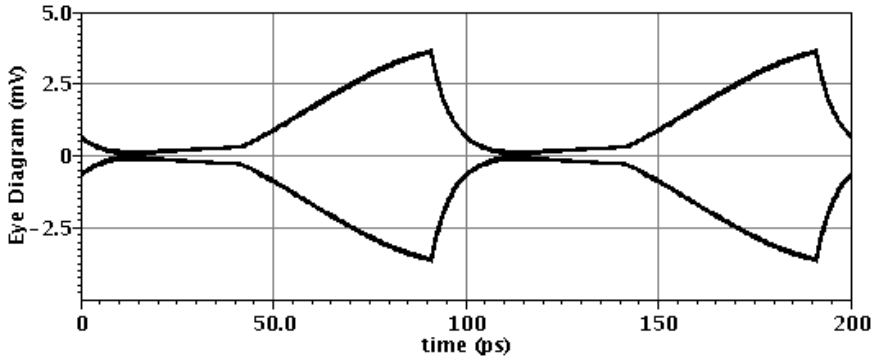


Figure 5.3: Output eye diagram of the network model ($\mathcal{N}$) shown in Fig. 5.2, $C_1 = 230\ fF$, $C_2 = 50\ fF$, $R_F = 1.4\ k\Omega$, $g_m = 22\ m\mho$, $g_o - g_{m,cc} = -1\ m\mho$, $g_r = 10\ m\mho$, $T_b = 100\ ps$, $T_d = 9\ ps$ and $f_{bit} = 10\ Gb/s$

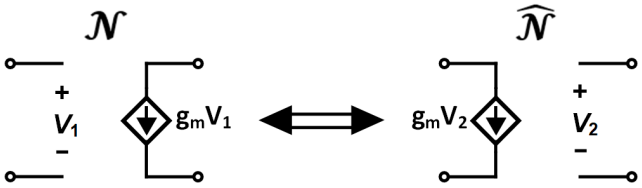


Figure 5.4: Transformation of linear voltage-controlled sources from $\mathcal{N}$ to $\widehat{\mathcal{N}}$ [23]

- current noise source of r for I_{n3} (where $r = 1/g_r$)

Using transient noise analysis and Eq. 2.49, output noise voltages are computed as

$$V_{n_1,out} = 1.05\ mV_{rms} \tag{5.2}$$

$$V_{n_2,out} = 0.22\ mV_{rms} \tag{5.3}$$

$$V_{n_3,out} = 0.2\ mV_{rsm} \tag{5.4}$$

Therefore, the overall output noise voltage calculated by Eq. 5.1 is

$$V_{n,out} = \sqrt{(1.13)^2 + (0.23)^2 + (0.22)^2} = 1.09\ mV_{rms} \tag{5.5}$$

Based on Tellegan's theorem and Interreciprocal LPTV networks, to change the network model to the adjoint network model, every resistive branch in $\mathcal{N}$ is transported to the same resistive branch in $\widehat{\mathcal{N}}$. The corresponding branch consisting of a capacitor in $\widehat{\mathcal{N}}$ is also chosen to be the same value as the capacitor in $\mathcal{N}$. For the periodically operated switches with $\Phi(t)$ in $\mathcal{N}$, time-reversal ($\Phi(T_b - t)$) operated switches are used in $\widehat{\mathcal{N}}$. The voltage-controlled current source in $\mathcal{N}$ is transferred by

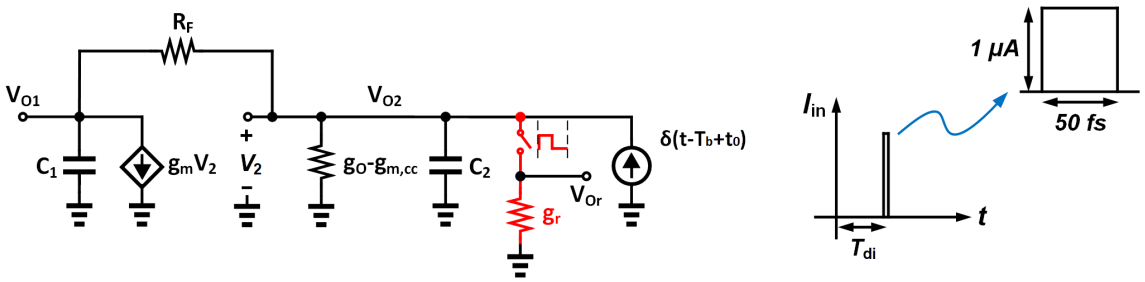


Figure 5.5: Adjoint network model ($\widehat{\mathcal{N}}$) of the modulated damping shunt-feedback TIA, $C_1 = 230\ fF$, $C_2 = 50\ fF$, $R_F = 1.4\ k\Omega$, $g_m = 22\ m\mho$, $g_o - g_{m,cc} = -1\ m\mho$, $g_r = 10\ m\mho$ and $T_{di} = T_b - T_0 = 9\ ps$

the presented method in Fig. 5.4 to $\widehat{\mathcal{N}}$ [23]. Therefore, based on the aforementioned tips, the adjoint network model of the system is created and shown in Fig. 5.5 where $T_{di} = T_b - T_0 = 9\ ps$. The injected impulse current source is modelled by a narrow width pulse current with an amplitude of 1 μA and width of 50 fs.

The autocorrelation function of the equivalent LTI system from the input noise source to the output corresponds to [11]

$$R_l(\tau) = R_{n,l}(\tau) * h_{eq,l}(\tau) * h_{eq,l}(-\tau) \tag{5.6}$$

where $*$ denotes convolution, $R_{n,l}(\tau)$ is the autocorrelation function of the lth noise process and the transfer function from the injected impulse response to a voltage corresponding to each noise source is denoted by $h_{eq,l}$. To obtain transfer functions, we need to observe the following voltages at the adjoint network model.

- $V_{o1} - V_{o2}$: corresponding to the noise of R_F
- V_{o2}: corresponding to the noise associated by R_o
- V_{or}: corresponding to the noise of the r

The summation of all $h_{eq,l}(\tau) * h_{eq,l}(-\tau)$ values at sampling times of $0, \pm T_b, \pm 2T_b, ...$, gives us the value of autocorrelation function of the noise sequence after sampling. Since the injected current is not an ideal impulse signal, to realize the unit area of the impulse signal, the amplitude of convolved signals ($h_{eq,l}(\tau) * h_{eq,l}(-\tau)$) needs to be multiplied by the value of

$$k_a = (\frac{1}{10^{-6} \times 50 \times 10^{-15}})^2 = (2 \times 10^{19})^2 = 4 \times 10^{38} \tag{5.7}$$

called noise constant. The final rms value of output noise voltage due to each of current noise sources are computed as:

$$V_{nl,out} = \sqrt{k_a \times \overline{I_{nl}}^2 \times \sum_{k=0}^{\pm\infty} \big(h_{eq,l}(\tau) * h_{eq,l}(-\tau)\big)\big|_{\tau=kT_b}} \tag{5.8}$$

where $\overline{I_{nl}}^2$ denotes the power spectral density (PSD) of lth noise source. Fig. 5.6 shows the output Autocorrelation function of the equivalent LTI system for all three noise sources. To calculate the output noise voltages, first, we compute the PSD of each noise source and using the Eq. 5.10, the rms output noise voltages are obtained.

For the noise of R_F we have

$$\overline{I_{n1}}^2 = \frac{4KT}{R_F} = \frac{4 \times 4.11 \times 10^{-21}}{1.4 \times 10^3} = 11.74 \times 10^{-24}\ A^2/Hz \tag{5.9}$$

and the output noise voltage becomes

$$V_{n1,out} = \sqrt{4 \times 10^{38} \times 11.74 \times 10^{-24} \times 220.12 \times 10^{-24}} = 1.02\ mV_{rms} \tag{5.10}$$

About the noise of R_o

$$\overline{I_{n2}}^2 = \frac{4KT}{R_{out}} = \frac{4 \times 4.11 \times 10^{-21}}{1 \times 10^3} = 16.44 \times 10^{-24}\ A^2/Hz \tag{5.11}$$

and the output noise voltage is calculated as

$$V_{n2,out} = \sqrt{4 \times 10^{38} \times 16.44 \times 10^{-24} \times 7 \times 10^{-24}} = 0.22\ mV_{rms} \tag{5.12}$$

Finally for the noise of r

$$\overline{I_{n3}}^2 = \frac{4KT}{r_m} = \frac{4 \times 4.11 \times 10^{-21}}{100} = 16.44 \times 10^{-23}\ A^2/Hz \tag{5.13}$$

and the output noise voltage is computed as

$$V_{n3,out} = \sqrt{4 \times 10^{38} \times 16.44 \times 10^{-23} \times 6 \times 10^{-25}} = 0.2\ mV_{rms} \tag{5.14}$$

Using the Eq. 5.1, the rms value of the output noise voltage becomes:

$$V_{n,out} = \sqrt{(1.02)^2 + (0.22)^2 + (0.2)^2} = 1.06\ mV_{rms} \tag{5.15}$$

Results of measuring output noise voltage using transient noise simulations and equivalent LTI system are summarized in Table 5.1. In conclusion, the equivalent LTI system presented in [11] offers us a possibility to evaluate the noise performance of the designed LPTV shunt-feedback TIA without having to use transient noise simulations.

Table 5.1: Noise results summary of a modulated damping LPTV SF-TIA by a square wave shown in Fig. 5.2

Circuit components	Calculated output noise voltages	Using transient noise simulation	Using equivalent LTI system [11]
R_F	$V_{n1,out}$ (mV_{rms})	1.05	1.02
$R_o = 1/(g_o - g_{m,cc})$	$V_{n2,out}$ (mV_{rms})	0.22	0.22
$r = 1/g_r$	$V_{n3,out}$ (mV_{rms})	0.2	0.2
Overall	$V_{n,out}$ (mV_{rms})	1.09	1.06

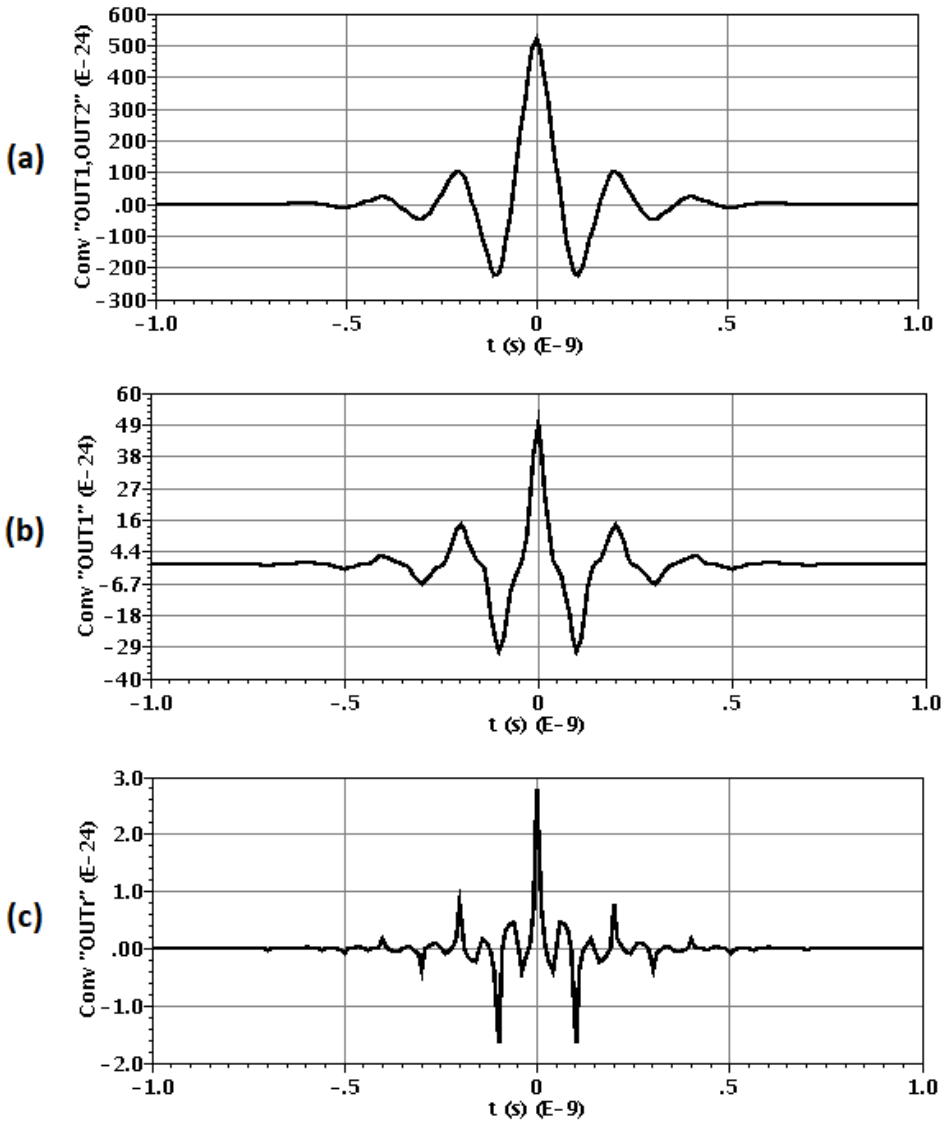


Figure 5.6: The output Autocorrelation function of the equivalent LTI system for the (a) R_F (b) R_o (c) r

Chapter 6

Extention of the modulation to post-amplifier blocks [10]

The small input current generated by the PD and the inherent gain-bandwidth trade-off of the TIA usually require additional stages of post-amplifiers, such as Cherry-Hooper (CH) post-amplifiers between the TIA and the decision circuits to obtain additional gain [6]. Such post-amplifiers can dissipate the majority of front-end power. In this chapter, the dynamic-damping technique is extended to CH-PAs and compared against a reference design consisting of an LTI CH-PA and SF-TIA. The effective gain increased more than 3x, and the overall sensitivity of the front-end improved. By downsizing the modulated damping CH-PA to reach the same overall VEO gain as the reference design, the LTI system, the front-end consumed 40 % less power than the reference. For all simulations of this chapter using Cadence in 65 nm technology, f_{bit} = 10 Gb/s for random input data with peak-to-peak amplitude of 2 μA, C_{in} = 200 fF, C_L = 50 fF.

The high-level schematic of the proposed differential front-end structure is shown in Fig. 6.1 (a). It consists of static-CMOS inverters and feedback resistors R_F in TIA and PA blocks. At the output of each block, transconductance (g) modulation is added to realize damping-factor modulation. Fig. 6.1 (b) shows the transistor-level schematic of the system, including inverter-based SF-TIA and CH-PA, cross-coupled inverters and triode region transistor biased by a rail-to-rail square wave signal to modulate the damping factor. C_{in} includes the capacitance of the PD and the capacitance of the TIA's input pad and C_L is the load capacitance the post-amplifier

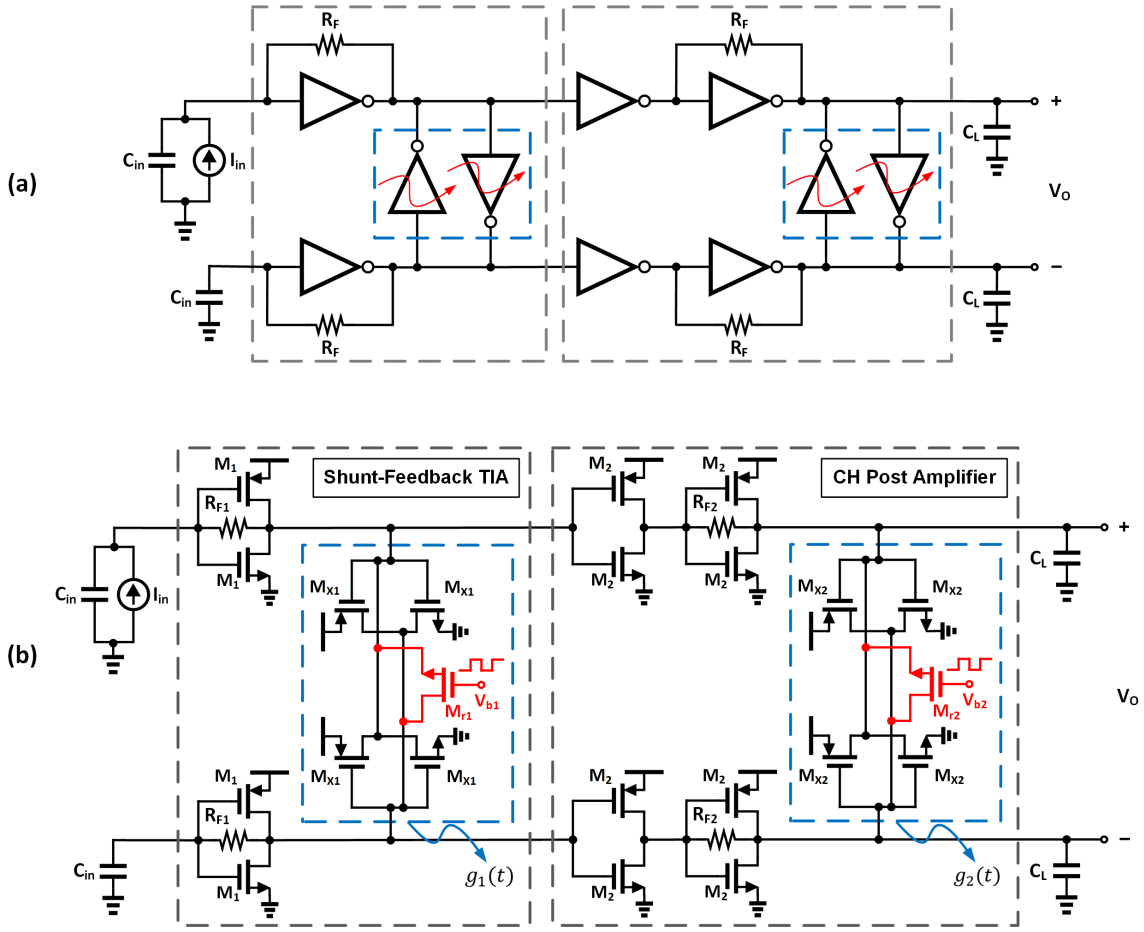


Figure 6.1: Differential shunt-feedback TIA followed by CH post-amplifier with conductance modulation at outputs (a) high-level schematic (b) transistor-level schematic. Transistors $M_{r1,2}$ are modulated with voltages $V_{b1,2}$ synchronously with incoming data.

drives, including latches and buffers. Offset compensation has been ignored.

To explore the performance with damping-factor modulation, an AC small-signal model of the differential half circuit of the SF-TIA is shown in Fig. 6.2. C_{gd} of the MOSFETs has been ignored for preliminary modelling. The damping factor of this system is given by Eq. 2.39, where $R_o = 1/(g_o - g(t))$. Eq. 2.48 also computes the damping factor of a cherry-hooper PA. The total output conductance is:

$$g_o - g(t) = g_o - g_{m,cc} + g_r \sum p(t - kT_b - t_d) \tag{6.1}$$

where $p(t)$ denotes the unit-amplitude pulse with 50 % duty cycle and t_d is initial delay time. Therefore the total conductance of the cross-coupled inverters (M_X) and

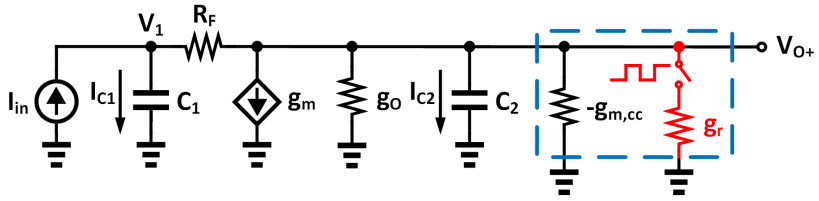


Figure 6.2: AC small-signal model of the differential half of SF-TIA

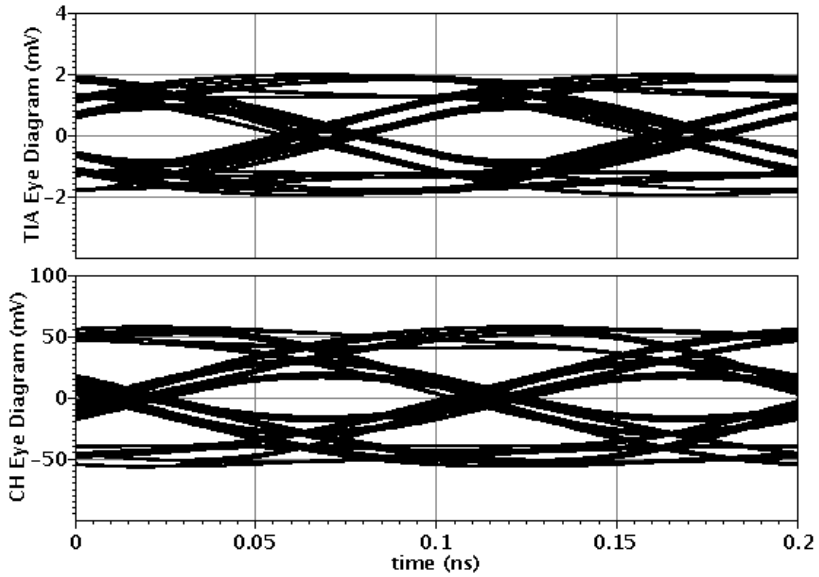


Figure 6.3: Output eye diagram of LTI SF-TIA + LTI CH-PA, $W_{1,2} = 30\ \mu m$, $W_{X1,2} = 4.5\ \mu m$, $R_{F1,2} = 1.4\ k\Omega$ and $f_{bit} = 10\ Gb/s$

the triode-region transistor (M_r) is modulated by the square wave (V_b) yielding two values of g:

$$g = \begin{cases} -g_{m,cc} & \text{when } V_b = 0 \\ -g_{m,cc} + g_r & \text{when } V_b = V_{DD} \end{cases} \tag{6.2}$$

where g_r is the conductance of M_r. By selecting appropriate values for g_o, $g_{m,cc}$, g_r and t_d, the damping factor of the system switches between small negative and moderate positive values synchronously with the incoming data which allows the fast response of a low-damping factor while mitigating ISI associated with an underdamped system.

Three variants of the system are simulated. Section 6.1 consists of an LTI TIA and CH-PA. It is only the TIA for section 6.2 that is equipped with damping-factor modulation, making it an LPTV system. Finally, Section 6.3 uses a LPTV TIA and CH-PA. In all simulations using Cadence in 65 nm technology, $f_{bit} = 10\ Gb/s$ for random input data with peak-to-peak amplitude of 2 μA, $C_{in} = 200\ fF$, $C_L = 50\ fF$

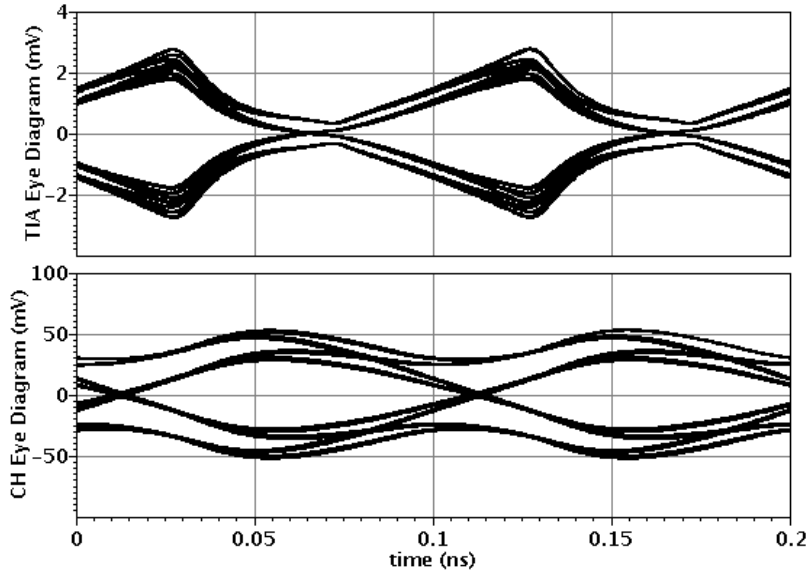


Figure 6.4: Output eye diagram of LPTV SF-TIA + LTI CH-PA, $W_{1,2} = 30\ \mu m$, $W_{X1} = 11\ \mu m$, $W_{X2} = 4.5\ \mu m$, $W_{r1} = 20\ \mu m$, $R_{F1,2} = 1.4\ k\Omega$ and $f_{bit} = 10\ Gb/s$

and rise/fall times of the rail-to-rail square wave modulation signals is 0.15 UI.

6.1 LTI SF-TIA + LTI CH-PA

Fig. 6.3 shows the outputs of the reference design, TIA and PA with cross-coupled inverters at the outputs. Here, the size of transistors and the value of R_F were optimized to reach the minimum input-referred noise current. In this case, $I_{n,in} = 1.2\ \mu\mathrm{A_{rms}}$ by using $W_{1,2} = 30\ \mu$m, $W_{X1,2} = 4.5\ \mu$m and $R_{F1,2} = 1.4\ k\Omega$. The effective gain is 15.5 $k\Omega$.

6.2 LPTV SF-TIA + LTI CH-PA

The cross-coupled inverters (M_{X1}) were enlarged giving a smaller damping factor. Dynamic damping was also introduced by adding a triode-region transistor (M_{r1}) across the outputs driven by a rail-to-rail square wave voltage of $V_{b1} = V_{DD}\ \sum p_1(t - kT_b - t_{d1})$. The output eye diagrams of the LPTV TIA and LTI PA are shown in Fig. 6.4, where $W_{1,2} = 30\ \mu$m, $W_{X1} = 11\ \mu$m, $W_{X2} = 4.5\ \mu$m, $W_{r1} = 20\ \mu$m, $R_{F1,2} = 1.4\ k\Omega$ and $t_{d1} = 90\ ps$. g_1 and ζ_1 change along the UI between $\{-5.4\ m\mho, 9.2\ m\mho\}$ and $\{-0.07, 1.2\}$, respectively. $I_{n,in} = 0.86\ \mu\mathrm{A_{rms}}$ and the gain of the system is

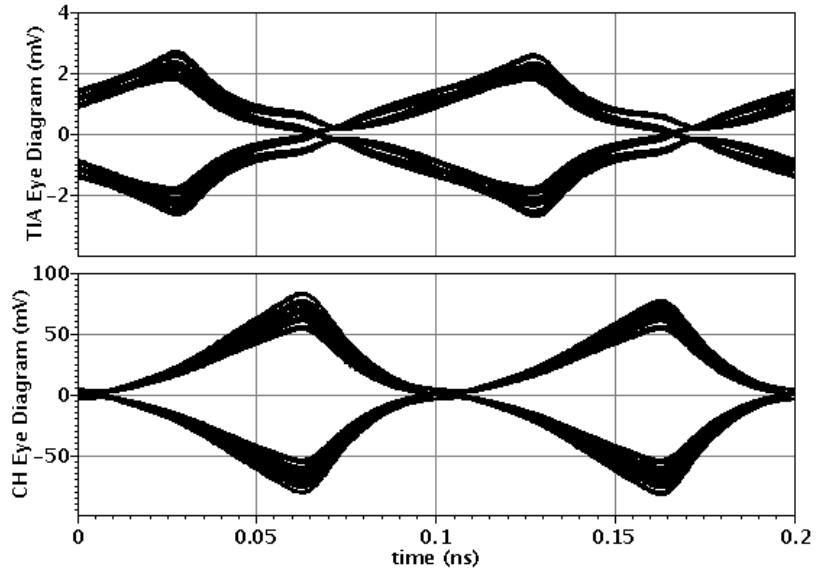


Figure 6.5: Output eye diagram of LPTV SF-TIA + LPTV CH-PA, $W_{1,2} = 30\ \mu m$, $W_{X1,2} = 11\ \mu m$, $W_{r1,2} = 20\ \mu m$, $R_{F1,2} = 1.4\ k\Omega$ and $f_{bit} = 10\ Gb/s$

28.2 $k\Omega$ and higher than 25 $k\Omega$ over a range of more than 12.5 ps delay variation of the signal $p_1(t)$, corresponding to a 45° phase range. This variant demonstrates that an LPTV TIA as presented in [9], despite its unconventional output eye is compatible with a convention CH-PA.

6.3 LPTV SF-TIA + LPTV CH-PA

To explore the performance of the system with g modulation at the output of both TIA and PA, M_{r2}, driven by $V_{b2} = V_{DD} \sum p_2(t - kT_b - t_{d2})$, is added across the output of the PA. Here, $W_{1,2} = 30\ \mu$m, $W_{X1,2} = 11\ \mu$m, $W_{r1,2} = 20\ \mu$m, $R_{F1,2} = 1.4\ k\Omega$, $t_{d1} = 90\ ps$ and $t_{d2} = t_{d1} + 35\ ps$. Fig. 6.5 shows the output eye diagrams of LPTV TIA and LPTV PA where the gain of the system increased to 55.8 $k\Omega$, higher than 50 $k\Omega$ over a range of more than 25 ps delay variation of the signal $p_2(t)$ compared to t_{d1} $(t_{d2} - t_{d1})$, corresponding to a 90° phase range. Along the UI, g_2 and ζ_2 alternate between $\{-5.4\ m\mho, 9.2\ m\mho\}$ and $\{-0.1, 2\}$.

The 65 ps shifted and scaled VEO of the TIA, VEO and output noise voltage of the PA are shown in Fig. 6.6, over one unit interval. At a sampling time of 0.6 UI, the system reaches its maximum vertical eye opening gain. The input-referred noise current at this sampling time is 0.84 μA_{rms}. By relaxing rise/fall times of modulation

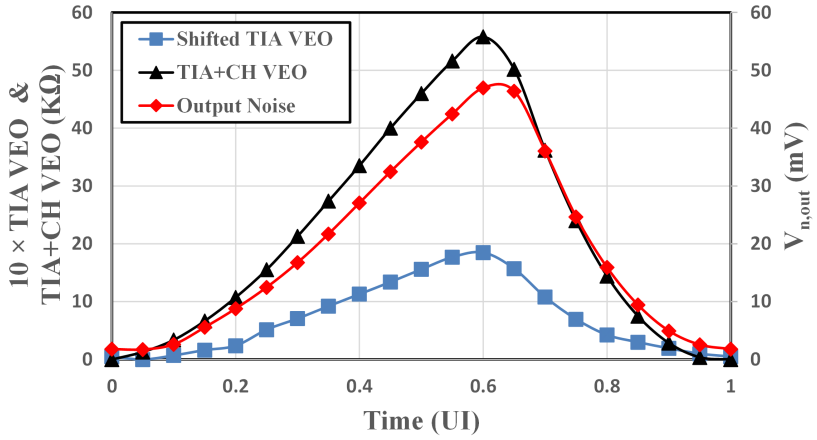


Figure 6.6: VEO, shifted VEO of the TIA and output noise voltage for the LPTV TIA + LPTV PA in one UI

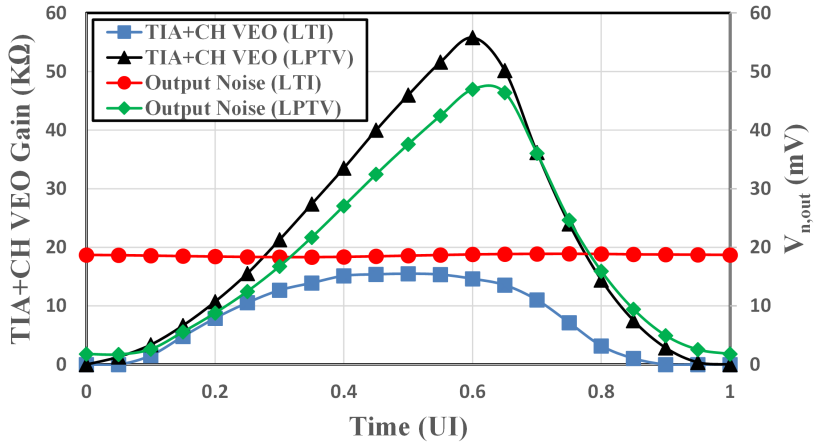


Figure 6.7: VEO and output noise voltage for the LTI TIA + LTI PA and the LPTV TIA + LPTV PA in one UI

signals from 0.15 UI to 0.25 UI, VEO gain and input-referred noise current range from 55.8 $k\Omega$ to 54.4 $k\Omega$ and 0.84 μA_{rms} to 1 μA_{rms}. VEO and output noise voltage of the LTI TIA + LTI PA and LPTV TIA + LPTV PA are shown in Fig. 6.7, over one unit interval. The LPTV system has higher than 20 $k\Omega$ VEO gain and lower input-referred noise current compared to the LTI system, over a range of more than 0.5 UI sampling time variation.

Compared to the reference design, VEO gain increased more than three times with the cost of 13.5 % power dissipation. In another simulation, by decreasing the transistor widths and feedback resistor in the PA block, the system reaches the same gain as the reference design but with lower power dissipation. Design parameters are

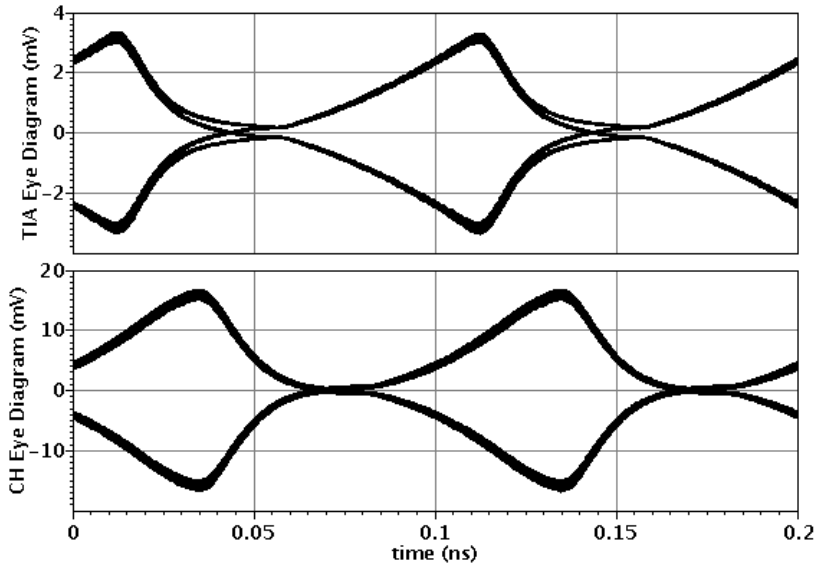


Figure 6.8: Output of the low power LPTV SF-TIA + LPTV CH-PA system, $W_1 = 30\ \mu m$, $W_2 = 8\ \mu m$, $W_{X1} = 11\ \mu m$, $W_{X2} = 4\ \mu m$, $W_{r1} = 20\ \mu m$, $W_{r2} = 8\ \mu m$, $R_{F1} = 1.4\ k\Omega$, $R_{F2} = 0.8\ k\Omega$ and $f_{bit} = 10\ Gb/s$

$W_1 = 30\ \mu$m, $W_2 = 8\ \mu$m, $W_{X1} = 11\ \mu$m, $W_{X2} = 4\ \mu$m, $W_{r1} = 20\ \mu$m, $W_{r2} = 8\ \mu$m, $R_{F1} = 1.4\ k\Omega$, $R_{F2} = 0.8\ k\Omega$, $t_{d1} = 75\ ps$ and $t_{d2} = 0\ ps$. Output eye diagrams are shown in Fig. 6.8. g_2 and ζ_2 change along the UI between $\{-4.1\ m\mho, 2.4\ m\mho\}$ and $\{-0.2, 1.6\}$. Therefore, the LPTV TIA + LPTV PA has the same effective gain as the reference design, but damping-factor modulation enables a 40 % power reduction. Whereas, by decreasing the power consumption in the reference design, the system has less AC gain and more ISI, so smaller effective gain.

Table 3.3 summarizes simulation results. Compared to the reference design and LPTV TIA + LTI PA, the input-referred noise current of the LPTV TIA + LPTV PA system is lower. Using damping factor modulation in the PA circuit increased VEO gain and the value of the Gain/Power ratio compared to the other two systems. Also, the new system provides the opportunity to design the front-end with a reasonable VEO gain and reduced power dissipation. The LPTV TIA + LPTV PA system gives better sensitivity compared to the reference design, LTI TIA + LTI PA, and the LPTV TIA + LTI PA system.

To wrap it up, by adding a time-varying resistor (a triode-region transistor with a square wave rail-to-rail bias voltage) across the outputs, the damping factor of the

TIA and PA is changed between a small negative and a large positive values, synchronously with the incoming data, giving rise to more than three times the gain and the Gain/Power ratio. Furthermore, this new design has better noise performance. In another simulation, it is shown that this system match the gain of the reference design while dissipating 40 % less power compared.

Table 6.1: Results summary of the shunt-feedback TIA followed by the cherry-hooper PA design

SF-TIA + CH-PA	LTI + LTI	LPTV + LTI	LPTV + LPTV	LPTV + LPTV
Size of transistors (μm)			high power	low power
W_1	30	30	30	30
W_2	30	30	30	8
W_{X1}	4.5	11	11	11
W_{X2}	4.5	4.5	11	4
W_{r1}	—	20	20	20
W_{r2}	—	—	20	8
Shunt-feedback resistor (kΩ)				
R_{F1}	1.4	1.4	1.4	1.4
R_{F2}	1.4	1.4	1.4	0.8
Data rate (Gb/s)	10	10	10	10
f_{3dB} (GHz)	3.74	—	—	—
AC gain (kΩ)	43.3	—	—	—
VEO gain (kΩ)	15.5	28.2	55.8	15.5
$I_{n,in}$ (μA_{rms})	1.2	0.86	0.84	0.84
Power (mW)	11.57	12.36	13.14	7.12
Gain/Power ratio (kΩ/mW)	1.34	2.28	4.25	2.17
$i_{pp,min}$ (μA_{pp}) for V_{CDR} = 25 mV	18.41	12.92	12.2	13.37

Chapter 7

Receiver design

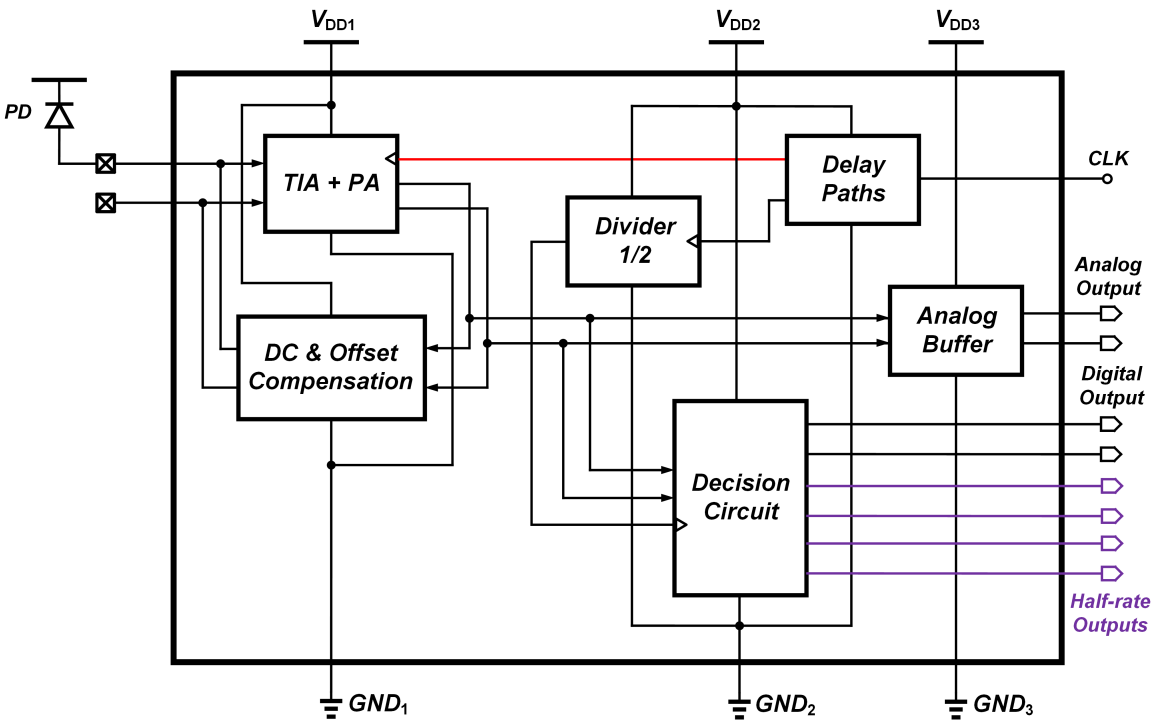


Figure 7.1: Block diagram of the designed receiver chip including the modulated damping shunt-feedback TIA and Cherry-Hooper post-amplifier, a DC/Offset compensation, an analog buffer and a decision circuit

In previous chapters, we focused on TIA and post-amplifier design with dynamic damping factor. Using the damping factor modulation in both TIA and PA blocks decreased 40 % the power consumption of the front-end. In this chapter, we present the receiver's blocks to implement the system at 10 Gb/s including modulated damping

Table 7.1: TIA and post-amplifier design parameters

Name of components	Value
W_1	30 μm
W_{X1}	11 μm
W_{r1}	20 μm
W_2	8 μm
W_{X2}	4 μm
W_{r2}	8 μm
R_{F1}	1.4 kΩ
R_{F2}	0.8 kΩ

factor shunt-feedback TIA and Cherry-Hooper post-amplifier.

The block diagram of the chip is shown in Fig. 7.1. For this system, it is assumed that the photodiode is connected to the single input of the TIA and the generated CLK signal is available at 10 Gb/s where the initial phase is adjustable. The receiver has two differential outputs, analog and digital output [24]. To explore the performance of the system, C_{in} of 200 fF are connected to each input. The analog output of the chip differentially drives 100 Ω resistance load and 50 fF capacitor, which means 50 Ω and 100 fF loads for each single-ended output. At the digital output, a capacitor of 50 fF is driven differentially, or 100 fF capacitance loads at every single digital output.

A DC & offset compensation block is used to cancel the DC current of the photodiode. The CLK signal goes to the delay block to adjust the initial phase of TIA and post-amplifier modulation signals. Two parallel half-rate paths of latches are designed to generate the digital output signal at the decision block. Therefore, the CLK signal is divided by two and fed into the decision circuits. Finally, an analog buffer is connected at the output of the post-amplifier to drive analog output loads. The designed test bench and blocks of the chip in Cadence are shown in Appendix A and Appendix B.

There are three separate supply voltages for the chip, V_{DD1}, V_{DD2} and V_{DD3} to minimize the supply noise of the system. Therefore, the chip is built as

- shunt-feedback TIA + Cherry-Hooper post-amplifier and offset/DC compensation blocks are connected to the V_{DD1}
- The delay path block, the divider block and the decision circuit block which

generates the digital output signal are supplied by V_{DD2}

- The analog buffer which produces the analog output voltage of the chip has another supply voltage, V_{DD3}

To design the shunt-feedback TIA and the Cherry-Hooper post-amplifier, we used design parameter values of the low power LPTV TIA + LPTV PA from the previous chapter, shown in Fig. 6.1. In addition, the size of transistors and the value of feedback resistors are presented in Table 7.1.

The rest of this chapter, briefly explain the design of each block of the chip, schematics of the circuits and parameters value.

7.1 DC and offset compensation block

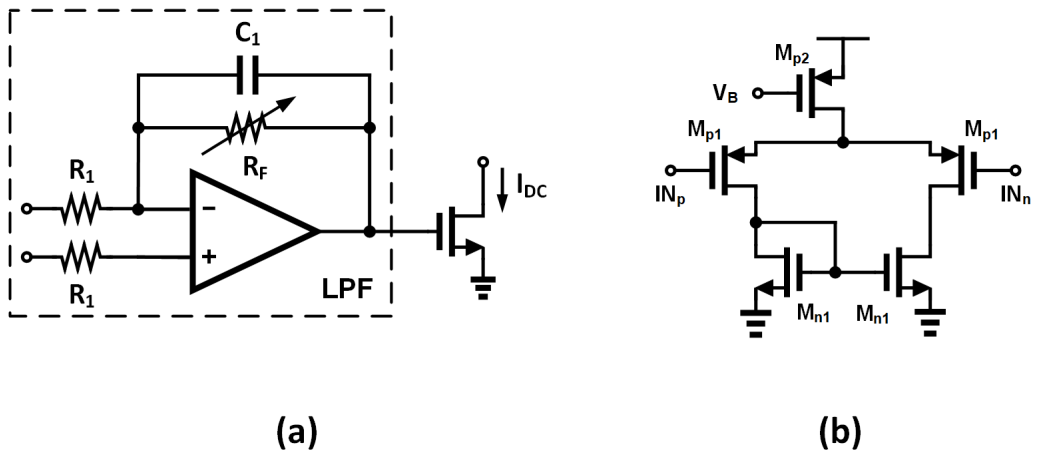


Figure 7.2: Schematic of (a) DC/offset compensation including an active low-pass filter followed by a current source (b) the single-ended differential amplifier

The schematic of the DC and offset compensation block is shown in Fig. 7.2 (a) [25]. Using the low pass filter helps us sense the DC value of the differential output voltage of the post-amplifier and use this value as a feedback signal for enabling sinking the current from the input node connected to the photodiode and filtering the high-frequency signal (post-amplifier output data) additionally. The low pass filter includes the *RC* filter and a single-ended amplifier shown in Fig. 7.2 (b) [26]. Since the DC value of the post-amplifier output is around 0.45 V, PMOS transistors are used to input the amplifier. To filter the high-frequency components, if we choose

Table 7.2: DC and offset compensation parameters

Name of components	Value
W_{n1}	40 μm
W_{p1}	40 μm
W_{p2}	120 μm
R_1	1 MΩ
C_1	5 pf
V_b	0.5 mV

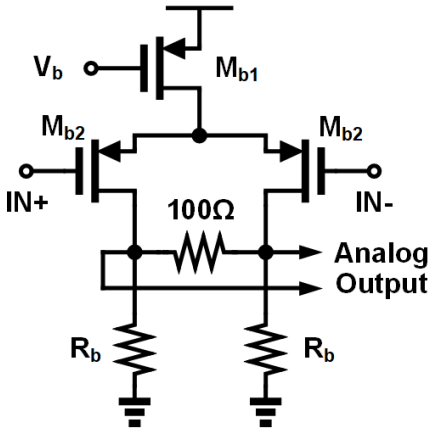


Figure 7.3: Schematic of the CML analog buffer to drive 100 Ω resistance load

the values of resistors around some $M\Omega$s and some pfs for the capacitor, the lower corner frequency is less than 1 MHz.

The value of the feedback resistor is variable to adjust the range of compensation. By assuming enough gain of the amplifier, the low-frequency gain of the filter is $1+\frac{R_F}{R_1}$. Table 7.2 summarized parameter values of the DC/offset compensation block. As an example, assuming the value of the R_F is 1 $k\Omega$, the low-frequency gain is $1+\frac{1}{1}=2$. If the minimum voltage of 0.5 V is needed to activate the current source of I_{DC}, the DC cancellation works for a minimum voltage difference of $\frac{0.5\ V}{2}=0.25\ V$ at the output of the post-amplifier. By choosing the overall gain value of 10 $k\Omega$, the minimum value of input current computed as $\frac{0.25}{10}=25\ \mu A$. Therefore, the DC/offset compensation block cancels the DC input currents of more than 25 μA properly. By changing the feedback resistor, the minimum compensable DC current of the photodiode is determined.

7.2 Analog buffer block

The schematic of the CML analog buffer to drive 100 Ω is shown in Fig. 7.3 [27]. Again due to the DC value of the post-amplifier output voltage, PMOS transistors are used. Since the gain of the receiver's front-end is large enough, there is no obligation to have a unit gain buffer with large transistors' size (due to intrinsic low transconductance PMOS), increasing the capacitance load of the post-amplifier (lower VEO) and power dissipation. For this work, a CML buffer with a mid-band gain of 0.5 $\frac{V}{V}$ is design with parameters values presented in Table 7.3.

Table 7.3: Analog buffer parameters

Name of components	Value
W_{b1}	120 μm
W_{b2}	120 μm
R_b	0.5 kΩ
V_b	0.5 V

7.3 Decision block

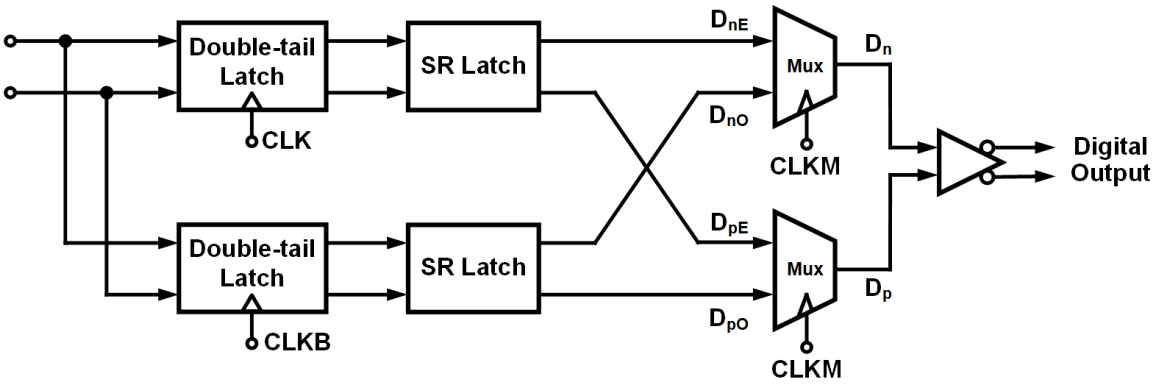


Figure 7.4: Half rate decision circuit including double-tail latches, SR-latches, 2:1 multiplexers and output buffers

Fig. 7.4 shows a practical implementation of the decision circuit. The input voltage is fed into two latches that are driven by a half-rate clock ($t_{CLK,Decision} = 1/2T_{CLK} = 200\ ps$). When the clock is high, the upper latch updates the value of the even path D_E. When the clock is disabled, the SR-latch stores the state of the

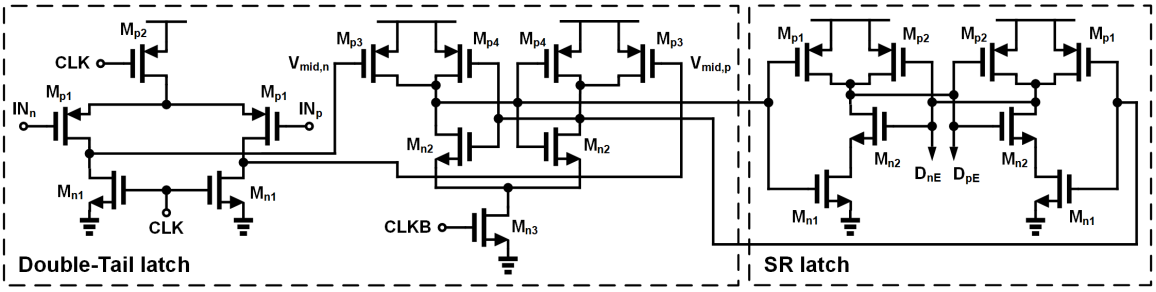


Figure 7.5: Schematic of a double-tail latch followed by a SR-latch

Table 7.4: Double-tail latch transitors' size

Name of component	Width size value (μm)
W_{n1}	5
W_{n2}	5
W_{n3}	15
W_{p1}	5
W_{p2}	2.5
W_{p3}	2.5
W_{p4}	2.5

upper dynamic latch, and the odd data path (D_O) becomes operational. Using this type of decision circuit schematic facilitates the equalization process in future works. Two multiplexers, driven by a delayed half-rate clock, are used to combine the two paths into a full-rate decision circuit. The buffers that follow the multiplexer drive the digital load.

The implementation of the high speed and gain latch, a double-tail latch, followed by a SR-latch is shown in Fig. 7.5. In the first phase of the double-tail latch operation, the clock signal is low, and the nodes V_{mis} are pre-charged to V_{DD} while the left-most differential pair is inactive. The crosscoupled inverters to the right are also disabled, and the differential output voltage is $V_O = 0\ V$. When the clock transitions to V_{DD}, the voltage nodes $V_{mid,p}$ and $V_{mid,n}$ are discharged at rates that are set by the differential input voltage. This allows the cross-coupled inverters to generate an output signal of $\pm V_{DD}$ [28]. Given that the output is reset to $0\ V$ when the clock is disabled, a SR-latch must be used at the output. Design variables of the double-tail latch circuit are shown in Table 7.4.

The transistors of the SR-latch are set such that the transistors directly connected to the inputs can drive the cross-coupled inverters into the desired state. Table 7.5

Table 7.5: SR latch transitors' size

Name of component	Width size value (μm)
W_{n1}	10
W_{n2}	10
W_{p1}	10
W_{p2}	10

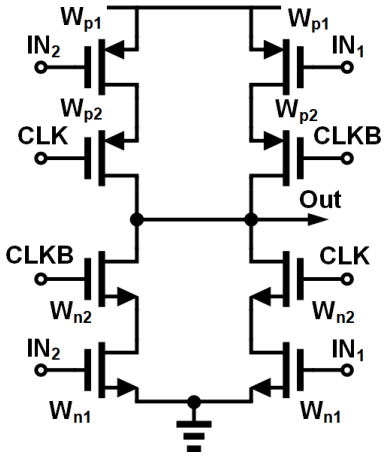


Figure 7.6: Schematic of a 2:1 multiplexer

shows the values of the SR-latch.

Fig. 7.6 shows the schematic of the 2:1 multiplexer [29]. Two multiplexers are used in the decision circuit to produce full-rate signals of D_n and D_p. The widths of the transistors are made large enough such that the rise and fall times are sufficiently fast relative to the bit-rate, while maintaining the clock feed-through at its minimum. To provide a shorter clock-to-output delay, the clock is placed closer to the multiplexer output. A clock edge is positioned midway between data transitions to ensure stability while the multiplexer is selecting the data. Inverters are placed at the outputs to mitigate the effects of the clock feed-through, and to drive the digital load of the receiver (including probes) [30].

7.4 Divider block

To drive the decision circuit at the half-rate, the input CLK signal must be divided by two. Therefore, a divider is used to generate a half-rate CLK signal. The block diagram of the divider is shown in Fig. 7.7 (a) [31] where two cross-coupled connected

Table 7.6: Mux transitors' size

Name of component	Width size value (μm)
W_{n1}	10
W_{n2}	10
W_{p1}	20
W_{p2}	20

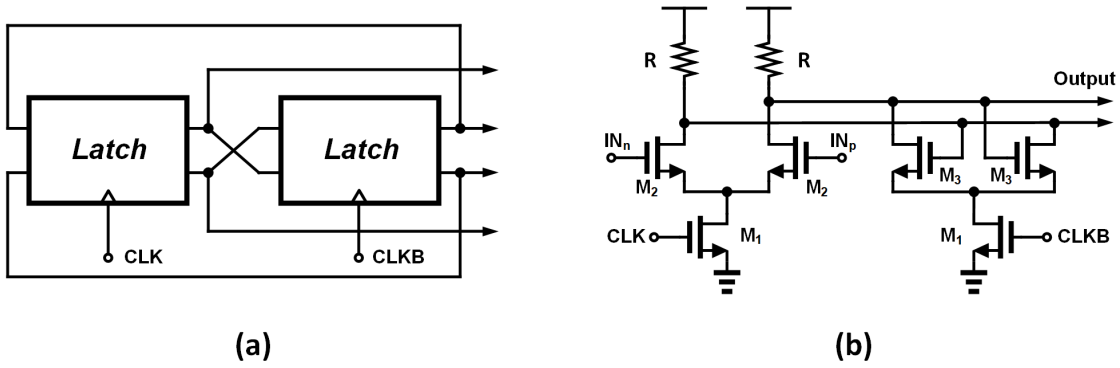


Figure 7.7: (a) Block digram of the divider to the half-rate (b) Schematic of the CML latch including the cross-coupled transistors to regenerate at the output

latches generate the half-rate CLK. In this system, CLK and $CLKB$ are the inputs and four signals at the frequency of $f_{CLK}/2$ are produced with the phase difference of $\frac{\pi}{2}$. We pick two generated signals as CLK and $CLKB$ signals of the double-tail latch, and two remaining signals are used as $CLKM$ and $CLKMB$ in the multiplexer circuit.

Fig. 7.7 (b) shows the schematic of the current-mode logic latch. Cross-coupled transistors are used at the output to regenerate the signal and increase the gain and speed of the divider. When the CLK is high, output tracks the input with some amplification. Once the clock goes low, the cross-coupled pair is activated and further amplifies the output, called the hold/regeneration mode. In the tracking operation mode, the time constant of the system determined by $\tau_{track} = RC_{out}$ but in the regeneration mode, the time constant is computed as $\tau_{regen} = (R||\frac{-1}{g_{m3}})C_{out} \approx \frac{-1}{g_{m5}}C_{out}$. Design parameters of the latch are presented in Table 7.7.

Table 7.7: Latch parameters design

Name of component	Value
W_1	15 μm
W_2	5 μm
W_3	15 μm
R	0.75 kΩ

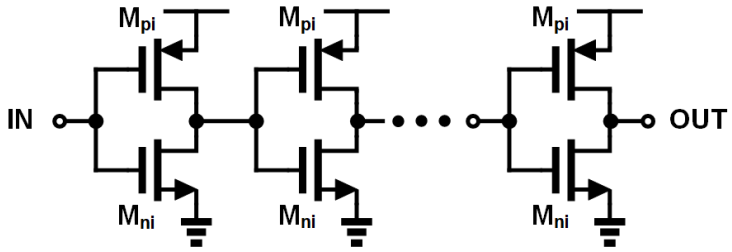


Figure 7.8: Schematic of a delay path including a number of series CMOS inverters to produce variable delays

7.5 Delay block

The delay block includes two separate and same delay paths connecting to the CLK and CLKB input signals. Fig. 7.8 shows each path that are designed by a series of CMOS inverters. It is determined by the number of inverters as to how much time is elapsed between the input and output. Furthermore, the size of transistors ($W_{ni} = W_{pi}$) regulates the value of rise/fall times. The rise/fall times of transistors are decreased as transistor size increases.

7.6 Chip simulation

In this section, simulation results of the proposed chip are provided. For all simulations using Cadence in 65 nm technology, $C_{in} = 200\ fF$ in each single inputs, $C_L = 50\ fF$ connected differentially across the analog and digital outputs, $R_L = 100\ \Omega$ is the resistance load at the differential analog output and $f_{bit} = 10\ Gb/s$ for random input data with peak-to-peak amplitude of 13.5 μA equals to the sensitivity of the front-end to achieve bit-error rate of $BER = 10^{-12}$. Design parameres of each block are given in previous sections, Tables 7.1, 7.2, 7.3, 7.4, 7.5, 7.6 and 7.7, where the transistors are in the minimum length (65 nm). The delay block includes two delay paths with four static CMOS inverters connected in series with the size of

$W_n = W_p = 20\ \mu m$ to generate CLK signals with rise/fall times of 15 ps or 0.15 UI. For all remaining CMOS inverters used in this design $W_n = W_p = 10\ \mu m$.

The power dissipation of the first supply voltage, V_{DD1} is equal to 9.8 mW. It includes the following power consumptions

- $P_{TIA+PA} = 9.8\ mW$ where $P_{TIA} = 4.7\ mW$ and $P_{PA} = 2.4\ mW$
- $P_{DCOC} = 2.7\ mW$

The supply voltage of V_{DD2} has a power consumption of 16.7 mW. The details of ech block dissipations are as

- $2 \times P_{Delay} = 2 \times 4.3\ mW = 8.6\ mW$
- $P_{Divider} = 4.3\ mW$ where $P_{CMLlatch} = 2 \times 2.15\ mW$
- $P_{Decision} = 2 \times 1.9\ mW = 3.8\ mW$ where $P_{DTlatch} = 0.85\ mW$, $P_{SRlatch} = 0.15\ mW$, $P_{Mux} = 0.45\ mW$ and $P_{Inv} = 0.85\ mW$

And finally, for the analog buffer, the power dissipation of the supply voltage has the value of 2.1 mW; therefore

- $P_{buffer} = 2.1\ mW$

Table 7.8 summarized the power dissipation of the proposed receiver chip. The overall value of the power dissipation is $P_{Chip} = 28.6\ mW$.

Table 7.8: Power consumption of the chip

Name of supply voltage	Power dissipation (mW)
V_{DD1}	9.8
V_{DD2}	16.7
V_{DD3}	2.1
Overall power consumption (P_{Chip})	28.6

Output eye diagrams of the TIA, post-amplifier, analog buffer and decision circuit blocks are shown in Fig. 7.9. The VEO gain of the shunt-feedback TIA is about 3 $k\Omega$, and the overall effective gain of the front-end is increased to about 10 $k\Omega$ using the Cherry-Hooper post-amplifier. Since the gain of the analog buffer for a resistance load of 100 Ω is 0.5 V/V, therefore the receiver has the overall analog VEO gain of

5 $k\Omega$. Fig. 7.10 shows the input bit-stream, shunt-feedback TIA output, Cherry-Hooper post-amplifier output, CML analog buffer output and full-rate digital output from the decision circuit. The digital output has the same pattern with a delay of $T_{bit} = 100\ ps$ compared to the input bit-stream. Two half-rate digital outputs and produced full-rate signal by multiplexers are shown in Fig. 7.11.

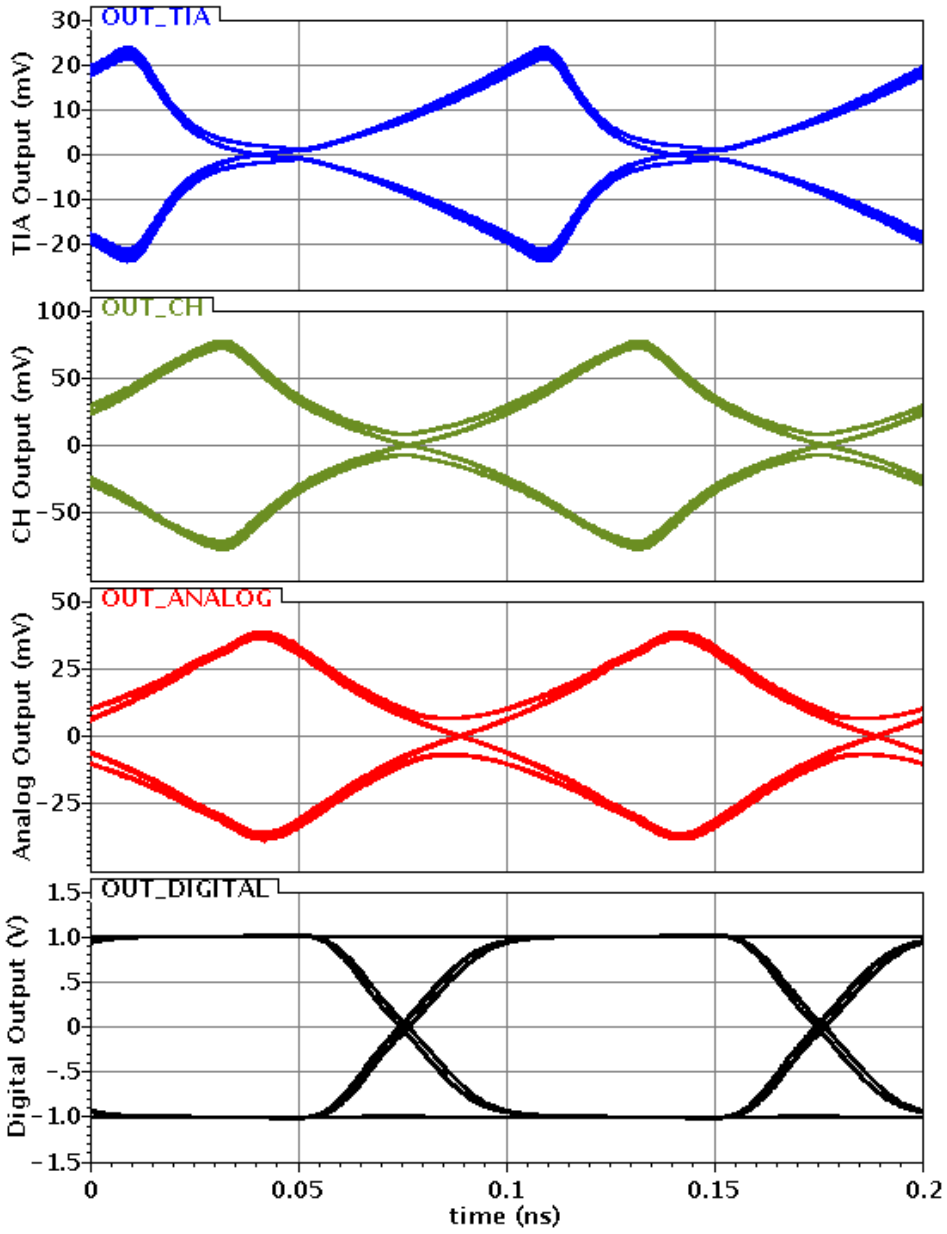


Figure 7.9: Output eye diagram of the shunt-feedback TIA, Cherry-Hooper post-amplifier, analog buffer and decision circuit

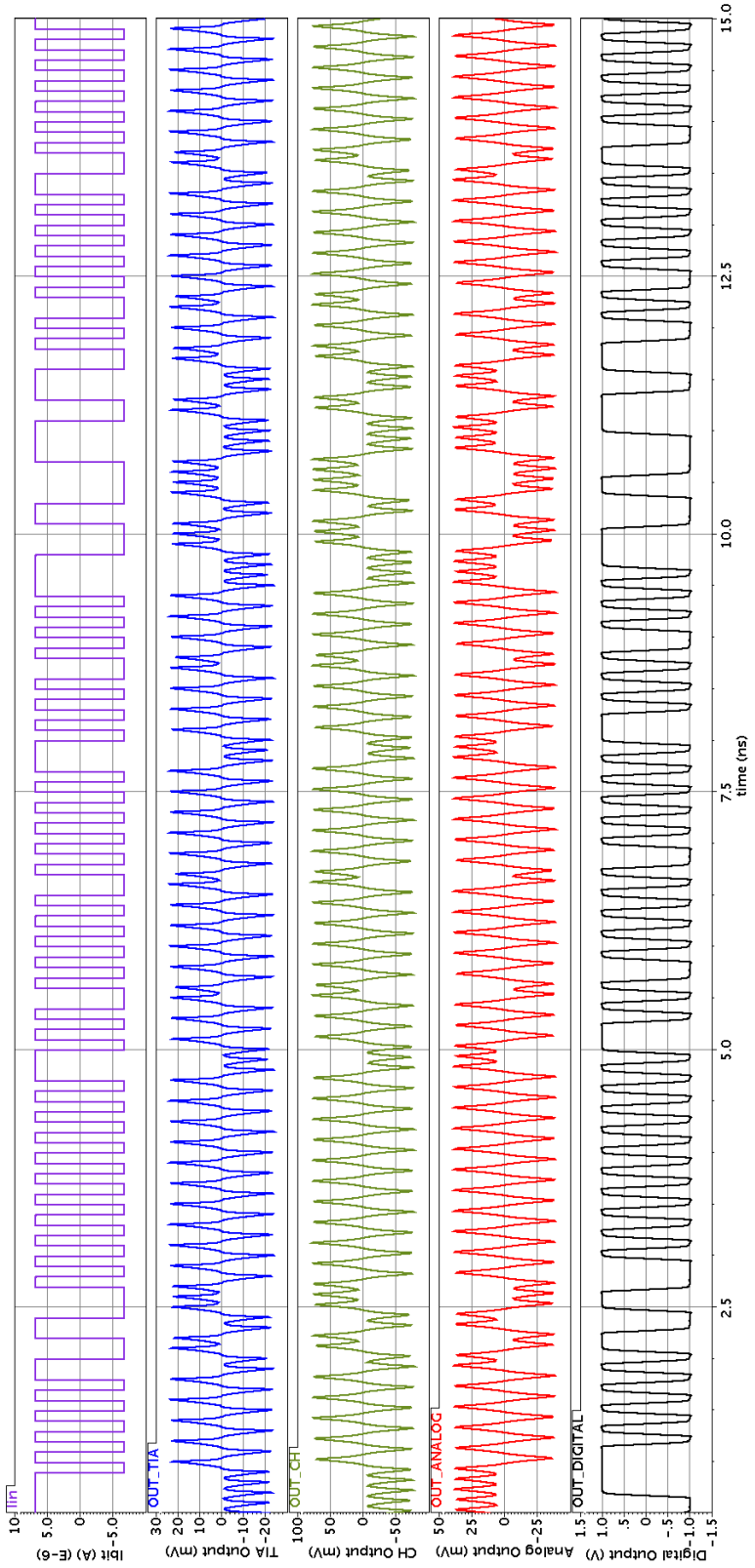


Figure 7.10: Transient simulation results including the input bit-stream, TIA output, post-amplifier output, analog buffer output and full-rate digital output

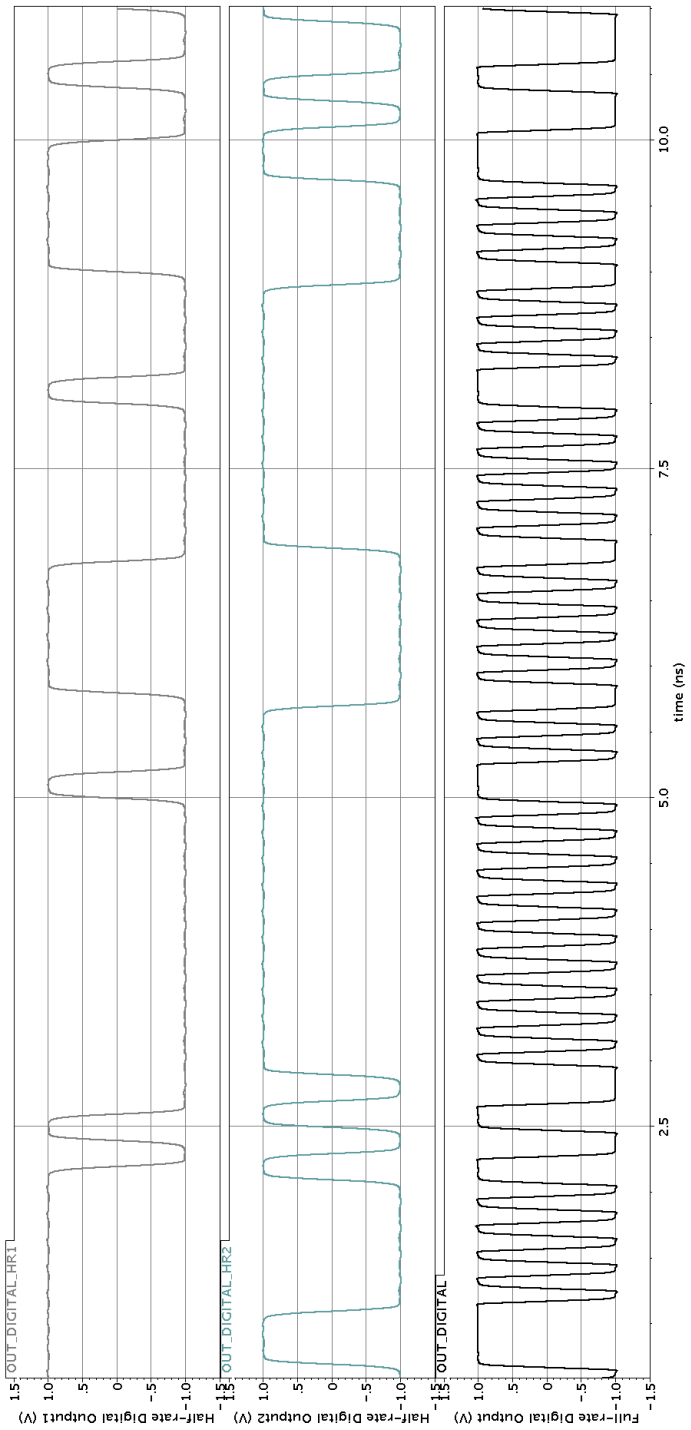


Figure 7.11: Transient simulation results including two half-rate and the full-rate digital outputs

Chapter 8

Conclusion

Circuit design for optical links is being pushed to its limits due to the increasing data throughput required by optical communications, as well as the development of new applications. In the course of this work, we have proposed the per-UI modulation of the damping factor of optical receiver front-ends between negative and positive values to take advantage of both low and high damping factor systems (high-speed and low ISI).

In Chapter 2, as a basis for this study, we reviewed the theoretical framework and literature.

In Chapter 3, we investigate design of simple shunt-feedback TIA and a shunt-feedback TIA with a cross-coupled inverter at the output which are omptimized for minimum input-referred noise current in a 65 nm technology.

In Chapter 4, switching between high and low values of the feedback resistor could increase the effective gain or VEO gain of the system, which in turn would improve the input-referred noise current and sensitivity. Modulating the feedback resistor allows the VEO gain to be raised, but it has a limitation as a result of the restricted minimum damping factor possible. A time-varying resistor is used at the output in order to change the damping factor synchronously with the incoming signal, leading to a to double the gain and a net improvement in receiver sensitivity. Finally, a rail-to-rail square wave was used to modulate the damping factor of the TIA. Through this modification, the complexity of generating a sine wave with the appropriate DC offset, amplitude, and phase is removed, and in place of it, a square wave must only be adjusted for phase. As well as better noise performance, this design provides better

VEO gain.

In Chapter 5, as a comparison of LPTV noise calculation with that of transient noise simulations, [11] presented a method in which the transfer function for any source in an LPTV system with a sampled output could be represented by an equivalent LTI. As a result, LPTV networks using adjoint networks can make straightforward noise calculations by determining equivalent LTI systems from multiple sources to the output.

In Chapter 6, a shunt-feedback TIA followed by a Cherry-Hooper PA with cross-coupled inverters at the outputs is designed as a reference design for minimum input-referred noise current in a 65 nm technology. The damping factors of the TIA and PA are changed synchronously with the incoming data by adding a time-varying resistor (a triode-region transistor with a square wave rail-to-rail bias voltage) across the outputs, giving rise to gains and Gain/Power ratios three times greater than before. Furthermore, this new design has better noise performance. In another simulation, it is shown that this system match the gain of the reference design while dissipating 40 % less power compared.

In Chapter 7, we designed and simulated the receiver's chip. The chip includes blocks of the modulated damping factor shunt-feedback TIA + Cherry-Hooper post-amplifier, the DC and offset compensation, the analog buffer and the decision circuit.

8.1 Future work

As a result of this research, several avenues for further exploration were identified:

1. The shown method in Chapter 5 using [11] proved that using the equivalent LTI system helps us to analyze the noise performance of the LPTV system. Further calculations and modelling are needed to computed the output noise voltage of the LPTV TIA and PA.

2. This system was designed and simulated at an input data rate of 10 Gb/s. Systems working at high data rates can benefit from damping factor modulation method.

3. The performance of the system is changed due to temperature variation. It needs to be determined the performance degradation of the LPTV system with

increasing the temperature and compared to the performance decreasing of LTI systems.

4. This LPTV system, due to having new types of the output eye diagram, needs a new clock-and-data recovery system. Therefore, one of the interesting works in the future could be design a compatible CDR chip to our designed LPTV frond-end.

Bibliography

[1] R. Essiambre and R. W. Tkach, "Capacity Trends and Limits of Optical Communication Networks," *Proceedings of the IEEE*, vol. 100, no. 5, pp. 1035-1055, May 2012.

[2] S. O. Kasap, Optoelectronics and Photonics: Principles and Practices. Englewood Cliffs, NJ: Prentice Hall, 2001.

[3] D. G. Goff, Fiber Optic Reference Guide, Boston: Focal Press, 1999.

[4] Mark A. Haidekker, Linear Feedback Controls. Elsevier, 2013.

[5] B. Razavi, Design of Integrated Circuits for Optical Communications. Hoboken, NJ, USA: Wiley, 2012.

[6] J. Proesel, C. Schow and A. Rylyakov, "25Gb/s 3.6pJ/b and 15Gb/s 1.37pJ/b VCSEL-based optical links in 90nm CMOS," *2012 IEEE International Solid-State Circuits Conference*, San Francisco, CA, USA, 2012, pp. 418-420.

[7] Cherry, E. M., and D. E. Hooper, "The design of wide-band transistor feedback amplifiers," *Proceedings of the Institution of Electrical Engineers*, Vol. 110. No. 2. IET Digital Library, 1963.

[8] P. Aminfar and G. Cowan, "Dynamic Damping in Transimpedance Amplifiers," *2020 IEEE International Symposium on Circuits and Systems (ISCAS)*, Seville, Spain, 2020, pp. 1-5.

[9] P. Aminfar and G. Cowan, "Square-Wave Modulated Damping in Transimpedance Amplifiers," *2020 IEEE 63rd International Midwest Symposium on Circuits and Systems (MWSCAS)*, Springfield, MA, USA, 2020, pp. 691-694.

[10] P. Aminfar and G. Cowan, "Multi-Stage Damping Factor Modulation in Optical Receiver Front-Ends," *Submitted to 2021 IEEE 64rd International Midwest Symposium on Circuits and Systems (MWSCAS)*, Springfield, MA, USA, 2021.

[11] S. Pavan and R. S. Rajan, "Interreciprocity in Linear Periodically Time-Varying Networks With Sampled Outputs," *IEEE Transactions on Circuits and Systems II: Express Briefs*, vol. 61, no. 9, pp. 686-690, Sept. 2014

[12] D. Abdelrahman and G. E. R. Cowan, "Noise Analysis and Design Considerations for Equalizer-Based Optical Receivers," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 66, no. 8, pp. 3201-3212, Aug. 2019.

[13] A. V. Oppenheim, A. S. Willsky, Signals and systems. Englewood Cliffs, N.J: Prentice-Hall, 2nd edition, 1997

[14] M. Chen, Y. Shih, C. Lin, H. Hung and J. Lee, "A Fully-Integrated 40-Gb/s Transceiver in 65-nm CMOS Technology," *IEEE Journal of Solid-State Circuits*, vol. 47, no. 3, pp. 627-640, March 2012.

[15] E. Säckinger, "The Transimpedance Limit," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 57, pp. 1848–1856, August 2010.

[16] Jieh-Tsorng Wu and B. A. Wooley, "A 100-MHz pipelined CMOS comparator," *IEEE J. Solid-State Circuits*, vol. 23, no. 6, pp. 1379-1385, Dec. 1988.

[17] P. P. Dash, "A variable bandwidth, power-scalable optical receiver front-end," Master's thesis, Concordia University, Sep. 2013. [Online]. Available: https://spectrum.library.concordia.ca/977824/.

[18] M. Atef, H. Chen, and H. Zimmermann, "10Gb/s inverter based cascode transimpedance amplifier in 40nm CMOS technology," *2013 IEEE 16th International Symposium on Design and Diagnostics of Electronic Circuits Systems (DDECS)*, Apr. 2013, pp. 72–75.

[19] E. Säckinger, Broadband Circuits for Optical Fiber Communication. Hoboken, NJ, USA: Wiley, 2005.

[20] B. Nauta and E. Seevinck, "Linear CMOS transconductance element for VHF filters," *Electronics Letters*, vol. 25, no. 7, pp. 448-450, Mar. 1989.

[21] S. Chu et al., "A 22 to 26.5 Gb/s Optical Receiver With All-Digital Clock and Data Recovery in a 65 nm CMOS Process," *IEEE J. Solid-State Circuits*, vol. 50, no. 11, pp. 2603-2612, Nov. 2015.

[22] Mark A. Haidekker, 3 - Solving differential equations in the Laplace domain, Linear Feedback Controls (Second Edition), Elsevier, 2020, Pages 25-49.

[23] F. Yuan and A. Opal, "Adjoint network of periodically switched linear circuits with applications to noise analysis," *IEEE Trans. Circuits Syst. I, Fundam. Theory Appl.*, vol. 48, no. 2, pp. 139–151, Feb. 2001.

[24] M. G. Ahmed et al., "A 12-Gb/s -16.8-dBm OMA Sensitivity 23-mW Optical Receiver in 65-nm CMOS," *IEEE Journal of Solid-State Circuits*, vol. 53, no. 2, pp. 445-457, Feb. 2018.

[25] J. Wang et al., "A Fully Integrated 25 Gb/s Low-Noise TIA+CDR Optical Receiver Designed in 40-nm-CMOS," *IEEE Transactions on Circuits and Systems II: Express Briefs*, vol. 66, no. 10, pp. 1698-1702, Oct. 2019.

[26] Razavi B., Design of analog CMOS integrated circuits. Tata McGraw-Hill Education; 2002 Oct 1.

[27] P. Heydari and R. Mohavavelu, "Design of ultra high-speed CMOS CML buffers and latches," *Proceedings of the 2003 International Symposium on Circuits and Systems*, 2003. ISCAS '03., 2003, pp. II-II.

[28] D. Schinkel, E. Mensink, E. Klumperink, E. van Tuijl and B. Nauta, "A Double-Tail Latch-Type Voltage Sense Amplifier with 18ps Setup+Hold Time," *2007 IEEE International Solid-State Circuits Conference. Digest of Technical Papers*, pp. 314-605, 2007.

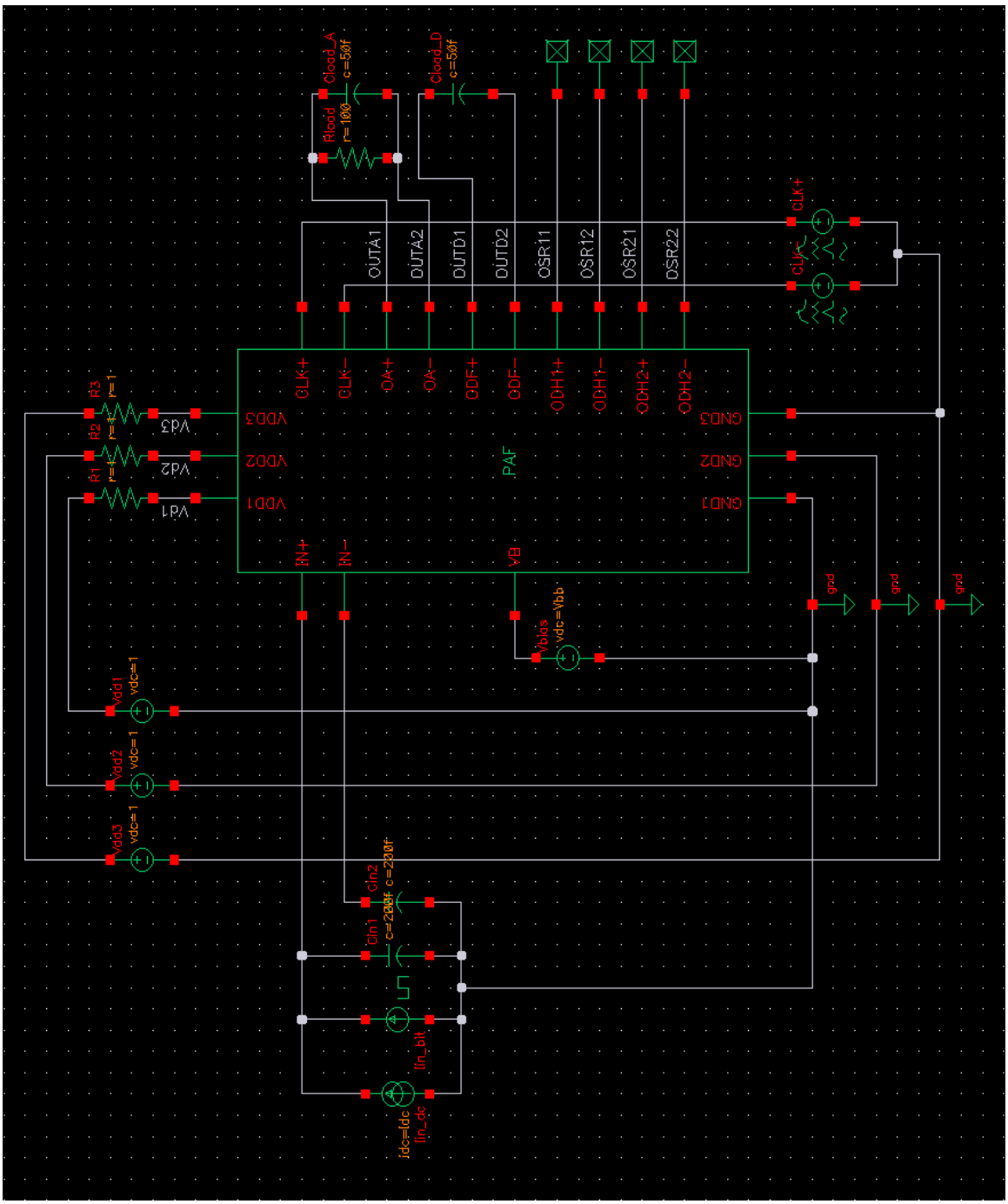
[29] Weste, Neil HE, and David Harris. CMOS VLSI design: a circuits and systems perspective. Pearson Education India, 2015.

[30] S. Shahramian and A. Chan Carusone, "A 0.41 pJ/Bit 10 Gb/s Hybrid 2 IIR and 1 Discrete-Time DFE Tap in 28 nm-LP CMOS," *IEEE Journal of Solid-State Circuits*, vol. 50, no. 7, pp. 1722-1735, July 2015.

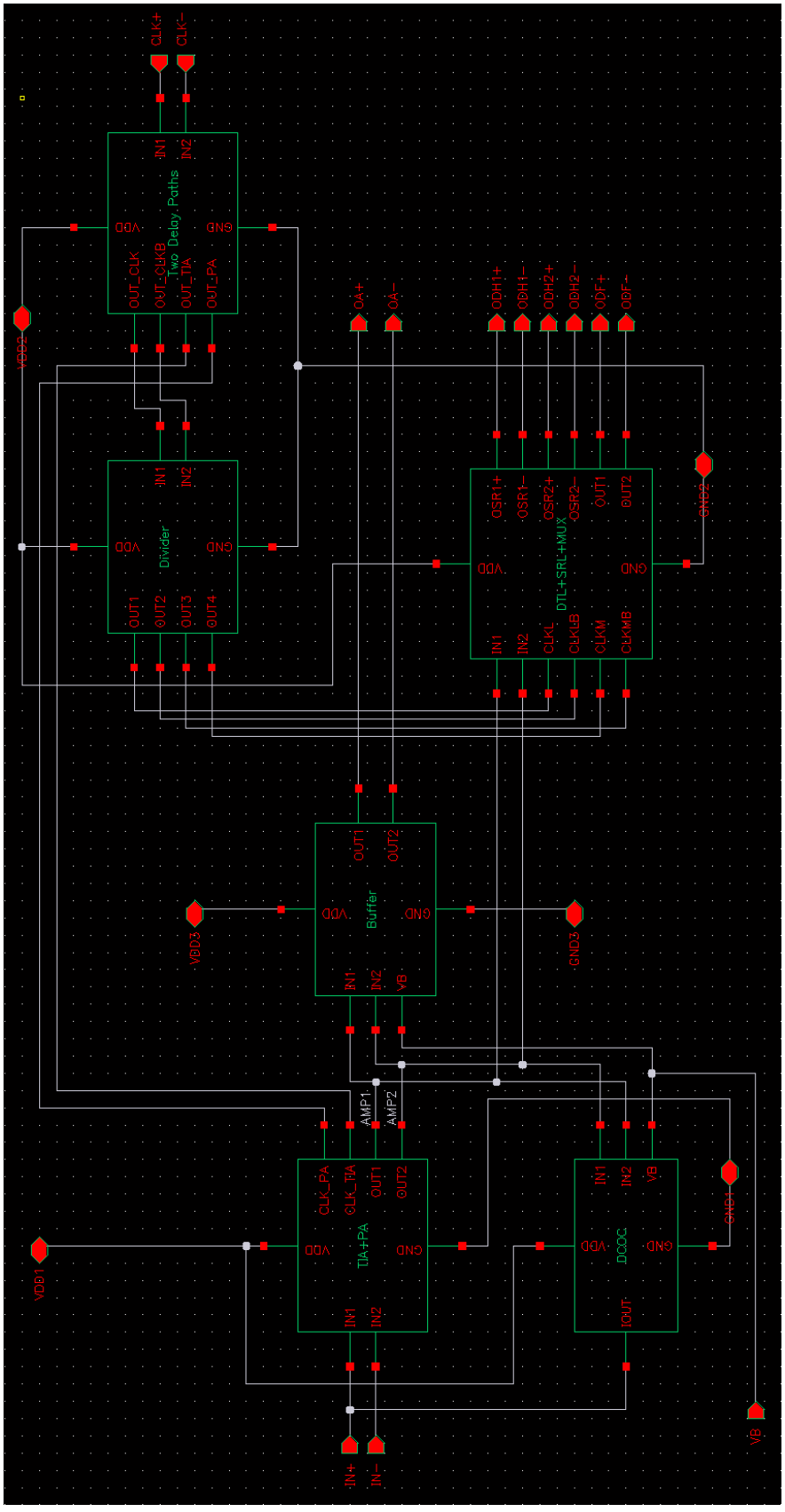
[31] A. Ghilioni, U. Decanis, E. Monaco, A. Mazzanti and F. Svelto, "A 6.5mW inductorless CMOS frequency divider-by-4 operating up to 70GHz," *2011 IEEE International Solid-State Circuits Conference*, 2011, pp. 282-284.

[32] M. Usama and T. Kwasniewski, "New CML latch structure for high speed prescaler design," *Canadian Conference on Electrical and Computer Engineering*, vol. 4, May 2004, pp. 1915-1918.

Appendix A
Test bench of the chip


Cload_A
c=50f
Cload_D
c=50f
Rload
r=100
OUTA1
OUTA2
OUTD1
OUTD2
OSR11
OSR12
OSR21
OSR22
CLK+
CLK-
R3
R2
R1
r=1
Vd3
Vd2
Vd1
VDD3
VDD2
VDD1
GND3
GND2
GND1
PAF
IN+
IN-
VB
Vbias
vdc=Vbb
gnd
Vdd1
Vdd2
Vdd3
vdc=1
Cin2
Cin1
c=200f
Iin_bit
Idc=Idc
Iin_dc

Appendix B
Block diagram of the chip


CLK+
CLK−
IN1
IN2
VDD
GND
OUT_CLK
OUT_CLKB
OUT_TIA
OUT_PA
Two Delay Paths
VDD2
OA+
OA−
ODH1+
ODH1−
ODH2+
ODH2−
ODF+
ODF−
Divider
OUT1
OUT2
OUT3
OUT4
OSR1+
OSR1−
OSR2+
OSR2−
DTL+SRL+MUX
CLKL
CLKLB
CLKM
CLKMB
GND2
VDD3
GND3
Buffer
VB
AMP1
AMP2
CLK_PA
CLK_TIA
TIA+PA
VDD1
DCOC
IOUT
GND1
IN+
IN−