INTEGRATED CIRCUITS AND SYSTEMS FOR A FULLY-FLEXIBLE WIRELESS AMBULATORY EEG MONITORING AND DIAGNOSTICS HEADBAND

ALIREZA DABBAGHIAN

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ABSTRACT

This thesis presents the design, development, and experimental characterization of wireless integrated circuits and systems built for ambulatory electroencephalography (EEG) monitoring and diagnostics. Two prototypes are presented.

The first one is a 3×4 mm^2 integrated circuit (IC), designed and fabricated in a 130nm CMOS technology, and integrates eight recording channels. A novel analog circuit is employed in each channel that detects and removes motion artifacts during amplification, resulting in a clean EEG prior to digitization. The idea prevents the amplifier saturation and removes the need for post processing of the digitized signals using artifact pattern recognition algorithms.

The second prototype is an integrated system in the form of a fully-flexible wearable wireless medical device. It integrates eight motion-resilient, active-electrode recording channels, with inter-digitated non-contact electrodes embedded into each of them, all implemented on a 4-layer polyimide flexible substrate, yielding the smallest form factor reported for a wearable EEG device. The flexible main board is connected to a 13×17 mm^2 rigid printed circuit board that hosts a low-power FPGA and a BLE 5.0 transceiver, which add diagnostic capability and wireless operation features to the device, respectively. The entire wearable solution with the battery weighs 9.2 grams.

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TABLE OF CONTENTS

Table of Contents

LIST OF TABLES

LIST OF FIGURES

Chapter 1

Introduction

1.1 Objective

Approximately 10% of patients admitted to the emergency departments (ED) present with altered mental status or seizures, with the most common cause being neurologic [1]–[6]. Due to the wide range of manifestation of such conditions and the lack of a specific diagnosis, many of these patients remain undiagnosed hours to days after admission, which leads to a disproportionately higher rate of death relative to other conditions [7]. For example, severe traumatic brain injury (TBI) has a mortality rate of over 40%. Studies show that up to 50% of these patients experience post-TBI non-convulsive (absence) seizures that could lead to an increase in the intracranial pressure and long-term damages to the neural system [8]. Conducting medical-grade electroencephalography (EEG) on

these patients allows for early detection of such neurological abnormalities and prevent further damages to the brain, consequently decreasing the alarming mortality rate.

Despite the clear motivation, a full conclusive EEG recording is not part of the standard tests conducted upon the admission of patients presenting with altered mental status. This is mainly because such a test requires (a) *Equipment*: data acquisition boxes, computers with EEG recording, analysis, and display software, and a large number (>20) of electrodes with connector cables; (b) *Setup*: careful placement of the electrode array on predefined locations of the scalp and applying an adhesive conductive gel to each electrode, all done by a trained technician; and (c) *Interpretation*: review and analysis of the entire recording by a trained technician under the supervision of an epilepsy specialist for detection of any abnormal activity or an indicator of a brain dysfunction. Such a demanding and time-consuming process has resulted in EEG monitoring to be excluded from the routine checks in the emergency departments. It has also resulted in a long wait time for the patient in the cases that an EEG test is prescribed [9].

Motivated by this, the development of small-form-factor wearable wireless devices has been investigated over the past decade. Such a solution is envisioned to enable EEG recording and analysis with medical-grade quality, while minimizing the time and staff/equipment resources required. A general top-level block diagram of such a device is shown in Figure 1.1. As shown, the system typically includes an array of recording (amplification and digitization) channels followed by a digital signal processing block for diagnostic purposes. Communications with the external (benchtop or hand-held) modules

is done through a wireless link that is used by the wearable device to transmit the recorded data and receive configuration commands.

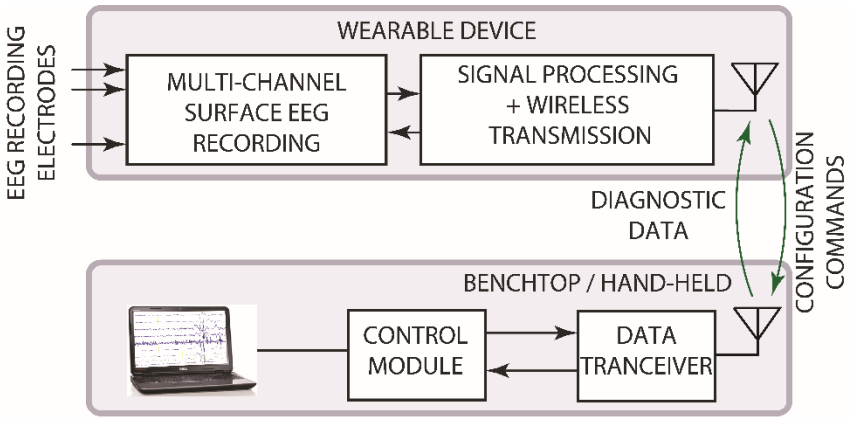


Figure 1.1 : Block diagram of a generic multi-channel wireless wearable EEG monitoring device.

Depending on their application, the wireless wearable devices for neuro-physiological monitoring and event detection can be divided into two main categories of "patient-specific" and "cross-patient" solutions. For an application such as the emergency room that was described above, the neurological event (e.g., seizure) detection must be done in a cross-patient manner where the algorithm does not require a long period of learning the specifications of each patient's brain neuronal activity. Authors in [10] have reported a seizure detection recurrent convolutional neural network (RCNN) algorithm capable of detecting seizures with 85% sensitivity and 0.8 false positives per hour. While such performance is certainly acceptable for a screening device in an emergency room, deep learning algorithms such as RCNN require substantial computational power (approximately an order of magnitude more than typical supervised learning algorithms

[10]), typically not available on a wearable device. Therefore, for the cross-patient diagnostic devices, raw EEG recordings must be communicated wirelessly to a mobile or stationary computer where the computationally expensive signal processing can be conducted.

The second category of applications is referred to ones that require a patient-specific solution. An example of this category are patients who are already diagnosed with epilepsy. A majority (near two-third) of these patients can be treated with pharmacological solutions. However, the optimal values for drug dosage and frequency of use is different from patient to patient and is currently decided based on an interview between the patient and the physician. Such a practice has the obvious shortcomings of (a) missing the seizures that are not sensed by the patient (e.g., happened during sleep), (b) missing the severity of absence seizures where there is no physical manifestation visible to the caregivers, and (c) inapplicability to younger patients during their infancy. A wearable device that could be worn by the patient to log the frequency and severity of their seizure episodes could improve the efficacy of this type of treatment significantly. Such a device is trained over a period of a few days to a couple weeks and after that can perform seizure detection with sensitivities as high as 95 to 100% [11]–[13].

For the approximately one-third of epileptic patients who cannot be treated with drugs, neurosurgery and implantable electrical neuro-stimulators are the only two available options. Patients who are considered to be candidates for surgery must undergo a pre-surgical monitoring test where they are connected to EEG recording equipment for many

hours. During this test, physicians hope to record at least one seizure to be able to judge the location of the seizure origin on the brain. In an effort to reduce the test time under a reasonable limit (e.g., one day), different methods such as sleep deprivation and photic stimulation are used that could artificially trigger seizures in cost of a significant amount of discomfort imposed on the patient. A wearable multi-channel EEG recording device capable of logging the frequency and duration of seizures with a reasonable spatial resolution allows the pre-surgical monitoring to be conducted outside of the hospital and with a natural pace as the patients go about their normal day-to-day activities.

1.2 Design consideration

1.2.1 Application-level

From the application-level point of view, using a wearable device while conducting everyday activities requires the solution to be minimally-obstructive. This includes having a small form factor, light weight, and reasonable aesthetics. Only with these criteria, several wearable EEG devices in the market that are too bulky and/or heavy are excluded from being considered for ambulatory EEG recording. Additionally, a basic requirement for medical-grade EEG recording is proper skin-electrode physical contact. Considering that several ambulatory EEG recording devices (e.g.,[14] and [15]) have the electrodes built into the device framework, and given that patients have different scalp size and curvature, lack of chassis flexibility in these devices results in major performance degradation to complete failure of the device in signal acquisition. Furthermore, the contact point of the device should be made of a material that does not have any harmful effect on the patient's

skin. Since ambulatory EEG is typically considered as an outpatient care solution, mounting (i.e., start-up) and use of the device should be a straightforward process without any need for technician intervention.

1.2.2 System-level

From the system-level point of view, a sufficient number of recording channels must be integrated onto the device to capture the brain neural activity with a reasonable spatial resolution. Multi-channel recording is also required for multi-variate algorithms that use signals from different locations on the brain to perform seizure detection. In addition, to add diagnostic capability to the solution, the wearable device should be equipped with a signal-processing unit that could be programmed with cross-patient or patient-specific diagnostic algorithms, depending on the application. Wireless communication is also an unavoidable feature that needs to be included in the system. Wireless link specifications such as the link throughput and being omni- or bi-directional are decided based on the application and the size of data that needs to be transmitted/received in real time, and whether or not certain aspects of the system needs to be reconfigured wirelessly. As it is discussed in details in [16], embedding signal processing on the device results in a significant reduction in decision-making latency and removes the need for a power-hungry high-throughput data transmitter that otherwise would be required to communicate raw EEG signals. However, it has the disadvantage of limited available computational power, which could lead to sacrificing seizure detection performance. Generally, unless the device is meant to be used for a short period (e.g., <1-to-2 hours), a significant portion of signal

processing (e.g., data compression, feature extraction and seizure detection) is conducted on an embedded processor, and only the signal processing results are communicated wirelessly. All the system-level modules (i.e., recording channels, signal processing, wireless transceiver) must be connected to each other using the least number of wires possible to realize a minimal form factor for the device. From a system-level point of view, this means using serializers/deserializers at the interface point of these modules to time-multiplex multi-bit data that is being communicated. Furthermore, to ensure that the solution is fully self-contained, all the necessary DC bias voltages and clock waveforms required for the operation of the integrated analog and digital circuits must be generated using on-device components such as digital-to-analog converters (DACs), voltage regulators, and crystal oscillators.

1.2.3 Circuit-level

From the circuit-level perspective, each recording channel should be able to amplify and digitize surface EEG signals with a typical amplitude range of 10µV to a few mV and frequency content of up to 300Hz. The sensing front-end circuit must have (a) a differential architecture, (b) an input-referred noise that does not add substantially (i.e., more than 10%) to the noise that already exists at the recording electrodes (10µVrms) [5], (c) input impedance that is orders of magnitude larger than the electrode-tissue interface impedance, (d) a reasonably high voltage gain, (e) a mechanism to avoid amplifier saturation due to the artifacts induced by the electrode physical motion, and (f) a mechanism for rejecting

large (up to 100s of mVs) DC offset between the recording and reference electrodes. The input signal dynamic range demands a minimum ADC resolution of 10 bits.

In addition to the above design specifications that are roughly the same for implantable EEG recording front ends, wearable devices have an important requirement that is mainly attributed to their large size where signals could travel up to 10cm between different modules. This makes the signals prone to various types of noise and interference from the environment and from neighbor components on the device. One effective way to avoid this is to employ a distributed (as opposed to centralized) architecture for the device where all the circuitry of a single recording channel (e.g., amplifier, filters, ADC, etc.) are placed right at the electrode contact locations (also known as active electrodes). Using this approach, weak surface EEG signals are first amplified and digitized locally before being routed along the device.

1.3 State-of-the-art

Table 1.1 summarizes some of the recently reported academic and commercial wireless monitoring headsets that aim to provide medical-grade EEG signals. Looking at these devices, it seems that the designs are either performance-oriented at the cost of sacrificing some of the application-level concerns (e.g., ease of use, comfort, lightweight, quick setup time, etc.), or user-oriented at the cost of reducing the system-level capabilities. For example, the device presented in [17] meets the channel count, noise, bandwidth, and wireless connectivity requirements. The device is also designed to be adjustable to different scalp shapes and sizes. However, the weight and bulkiness of the device makes its use

limited to in-lab tests and inappropriate for ambulatory EEG recording. Also the device does not feature a mechanism for removing artifacts due to the physical motions of the patient, which could significantly degrade the recording quality as it will be discussed in 2.3. An example of the other end of spectrum is the Muse headband [15]. While this solution features a small form factor and lightweight, it only has 4 recording channels and uses passive electrodes for recording and integrates all the active circuitry on one side of the device, causing significant susceptibility to different types of noise and interference sources. Overall, none of these devices is ideal to be used as a quickly-mountable medically-relevant ambulatory EEG monitoring and analysis headset for the applications described in the previous section.

Table 1.1: Summarizes some of the recently reported academic and commercial wireless monitoring headsets that aim to provide medical-grade EEG signals.

Specification	[14]	[18]	[17]	[17]	[15]
# of channels	8	5	6	30	4
Signal Processing	Yes	Yes	Yes	Yes	No
BW (Hz)	0.5-100	0.5-100	<262	<262	N/R
Wireless Tech	BT 2.1	BT 2.1	BT 4.0	BT 4.0	BT 2.1
Motion Artifact removal	Digital	Digital	No	No	No
Weight (grams)	200	N/R	110	610	61

1.3.1 Previous works in motion artifact removal

One of the most challenging problems in ambulatory bio-signal recording is motion artifact, specially in case of low amplitude signals like EEG. In order to overcome this obstacle, most of the works attenuate the effect of motion artifact in digital signal processing domain[19][20][21]. For example, in [20] authors used the information from a

multi-channel ECG recording front-end to calculate the motion artifact signal in digital backend and remove the effect of this artifact under the assumption that this motion artifact is an uncorrelated signal from the actual ECG. One of the main problems of removing motion artifact in digital domain is that the ADC require a large dynamic range to avoid saturation, since the ADC should be able to digitize the motion artifact signal which may have an order of magnitude higher amplitude than the target bio-signal.

In [22] the motion artifact signal is recorded by measuring the impedance of electrodes-tissue interface. As shown in Figure 1.2, the ETI block measures the impedance by injecting a current to the electrodes. Then the contaminated signals and measured impedance are fed to the digital back-end. The digital back-end calculates the motion artifact signal and converts the result to an analog signal using a digital to analog converter (DAC) and subtract it from the input signal. Subtracting the motion artifact before feeding the recorded signal to the ADC can relax the requirements on the ADC dynamic range but as it is shown in the Figure 1.2 adding DAC and ADC increases the design complexity and power consumption. Furthermore, in [23] it is mentioned that accuracy of this method is not sufficient at all frequencies.

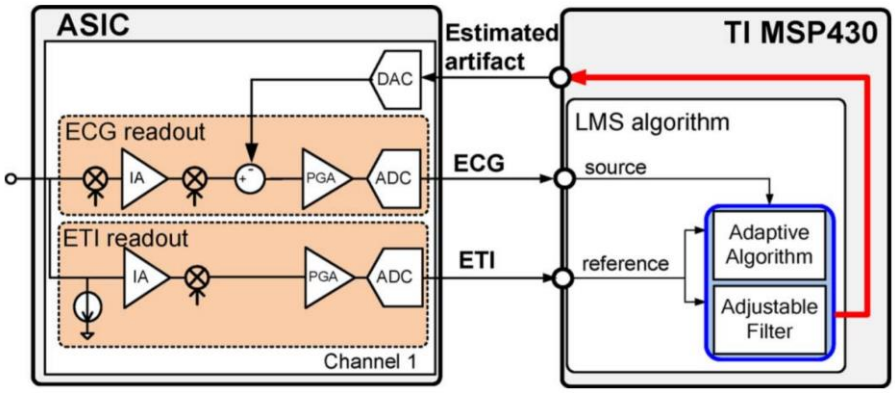


Figure 1.2: Conceptual representation of the motion artifact suppression method presented in [22]**.**

In other design presented in [24], authors tried to measure the impedance of electrodes-tissue interface without injecting extra current to the tissue. Figure 1.3 shows the schematic of the front-end design, where the two passes are supposed to have similar motion artifact duo to the special design of the electrodes. Two parallel RC with known different impedances are deliberately placed at the input stage of the buffers. This known unbalance in the input stage results in different gain and therefore, different voltage at the output of buffers. Based on these two output voltages, the digital back-end calculates the interface impedance and ECG signal. In this method, in order to decrease the effect of parasitic capacitance at the input of the buffers the impedance value of Zin_1 and Zin_2 should be less than C_P that results in attenuating the input signal. Another problem of this method is that for the low amplitude input signals the accuracy of this method decrease, which makes this approach inappropriate for the EEG recording systems.

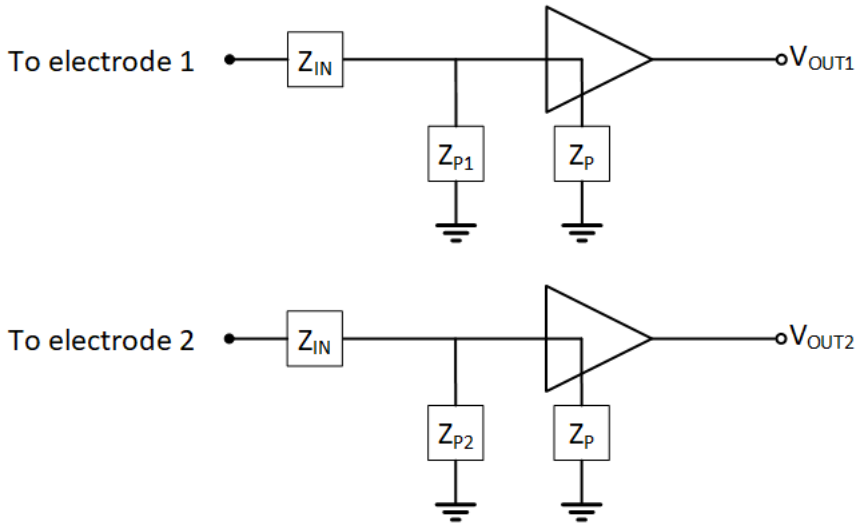


Figure 1.3: Conceptual representation of the motion artifact suppression method presented in [24]**.**

In our proposed method, we tried to record the motion artifact and compensate its effect in the recorded signal in the analog domain, which is suitable to record low amplitude signals like EEG and is needless of injecting any current to the tissue.

1.4 Technical gap

As we discussed, reported wireless EEG recording headsets are either too bulky that are not suitable for long-term EEG monitoring [17], [18] or could not meet the medical-grade EEG recording requirements [15]. In terms of physical properties of the EEG recording device, in order to have more comfortable devices, researchers tried to add some level of flexibility to the system by adding some flexible components such as, using flexible wire connection [25] or adding flexible electrodes [26]. However, there has not been any prototype reported to date where the entire system is fabricated on a fully flexible substrate.

Furthermore, several researches are focusing on addressing the effect of motion-induced artifacts on quality of recorded EEG. The majority of these works are focusing on solving the problem in the digital domain, which has shown some success but the problem is that with large artifacts the signal recording circuit might get saturated which does not allow any data to be recorded. There are also some efforts to solve the problem in the mixed-signal domain, but either they comes at the cost of increasing the complexity and power consumption of the recording channel [19], [22] or they present poor motion detection performance for low amplitude bio-signals such as EEG [20], [21].

We noticed that an important reason for the lack of a low power motion artifact detection and removal method that is suitable for EEG signals is actually the lack of information on how the electrode-tissue interface is actually affected by relative movement of electrode and skin.

In this work, we tried to fill these gaps by investigating the origin and effects of motion artifact, on EEG recording and electrode-skin interface. Then our goal was to design and fabricate a comfortable EEG recording headband, capable of tolerating motion artifact and practical for long term monitoring.

Based on the above, there is still a need for a light-weight, small form-factor ambulatory EEG recording device suitable for long term brain monitoring that can meet all the clinical-grade requirements while being capable of detecting and compensating the effect of motion-induced artifacts. In doing so, we present a novel analog-based circuit for detection and removal of motion-induced artifacts in the front-end circuit, without

negatively affecting the performance of the recording channel in terms of noise and power consumption. Prior to designing the proposed idea, we conducted a study on the motion-affected electrode-skin interface impedance, and we use the result in designing the recording channel architecture as well as the motion detection and removal circuitry.

1.5 Thesis organization

Chapter 2 presents characterization results of electrode-tissue interface impedance for dry EEG contact and non-contact recordings. The effect of random electrode motions on the recorded EEG signals as well as the noise contributions for both types of electrodes are studied. Using statistically-significant experimental measurement results, a model describing the motion-induced interface impedance variations of a dry electrode is developed. At the end of chapter, existing analog front-end circuits for surface EEG recording are reviewed, followed by a theoretical circuit analysis discussing the effect of electrode movements on the performance of these circuits.

Chapter 3 presents an 8-channel SoC designed, fabricated, and tested for recording surface EEG signals in the presence of motion artifacts. Each recording channel utilizes a novel mixed-signal (i.e., analog and digital) architecture capable of extraction and removal of motion-induced artifacts while amplifying the EEG signals. Various experimental tests have been conducted on the SoC to evaluate its performance in recording EEG signals contaminated by artifacts. The measurement results are presented and compared with the state of the art.

Chapter 4 presents a 9.2-gram fully-flexible wearable EEG recording system with 8 active-electrode active-shielded recording channels, a low-power digital signal processing backend, and a BLE 5.0 transceiver for wireless communications. The system-level schematic and physical design considerations are discussed and experimental measurement results are presented and compared with the state of the art.

Chapter 5 concludes the thesis and discusses possible future directions for this research work.

Chapter 2

Motion-Affected Electrode-Skin Interface Characterization in Surface EEG Recording

As mentioned in the previous chapter, EEG recording in hospitals is predominantly done by wet electrodes. These electrodes benefit from an adhesive conductive gel injected between the metallic plate and the skin to ensure a mechanically-stable and electrically-low-impedance interface. Use of such electrodes is not practical for ambulatory wearable EEG monitoring devices as they require post-recording wash-up, could cause discomfort and skin reactions in long term, and lead to a significant increase in the physical form factor of the device. Therefore, the majority of wearable EEG headsets (e.g., all devices presented in Table 1.1) use different variations of dry (i.e., gel-free) electrodes. Despite their benefits, a clear yet important problem using these electrodes is the mechanical instability of their contact with the skin due to the inexistence of an adhesive material, such as the gel used in wet electrodes.

This chapter presents a comparison between different types of dry electrodes (e.g., contact, non-contact, etc.) in terms of their electrical characterization such as impedance, noise and their response to motion. In addition, it provides an analytical explanation of how motion artifacts are generated, and presents a conceptual solution on how to translate the effect of motion to an electrical signal that could be used for artifact cancellation, the implementation of which will be described in later chapters.

2.1 Electrode-tissue electrical impedance model

Figure 2.1 shows the electrical models of electrode-tissue impedance for dry contact and non-contact electrodes. As shown, for contact electrodes, direct connection between the ionic solution (skin) and the electrode's metallic conductor results in polarization, which leads to a half-cell potential that could be in the order of hundreds of millivolts. In the case of a non-contact electrode, the skin is isolated from the recording front-end, typically by layers such as fabric, hair, and air (gap). While the polarization voltage removal is not a concern anymore, the extra layers form a very high-impedance electrode-tissue interface, which could result in a weaker signal at the input of the front-end amplifiers.

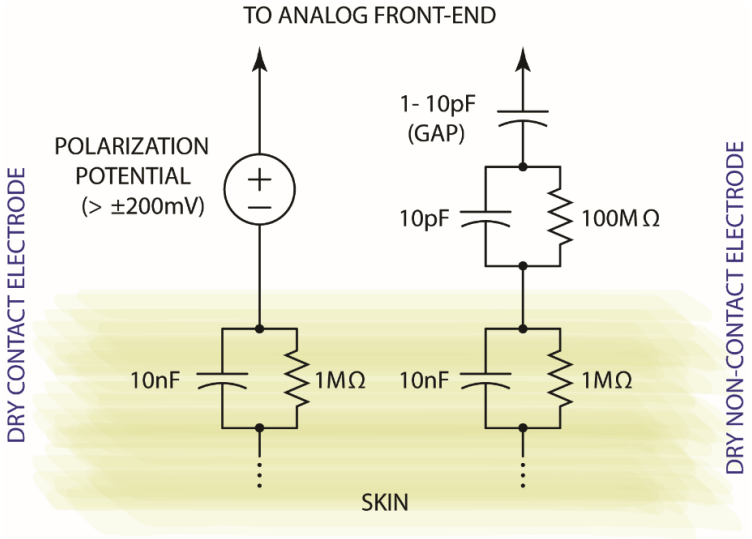


Figure 2.1 : Electrical models of electrode-tissue impedance for dry contact and non-contact electrodes.

Figure 2.1 also shows typical values for the resistors and capacitors in the presented electrical models. These numbers vary by the interface-insulating layer, as well as the electrode physical dimensions and material. For our experiments, we used a contact electrode with a surface diameter of 0.9cm and silver material.

Spatial resolution of EEG signals at the skin surface is about 1cm [27] so placing more than eight electrodes on the forehead does not give us any benefit in terms of resolution. We want the electrode to be as big as possible to experience as big capacitance as possible. Therefore, we tried to maximize the size of electrodes while eight of them could be placed on the forehead. Since fabricating the electrodes and analog circuitry on the same substrate, results in a small form-factor device, which is easily scalable, we decided to use standard FR4 for manufacturing the electrodes. Therefore, for non-contact

electrode, a custom design electrode was used with the diameter of 1.7cm, insulation layer and thickness of epoxy liquid and 0.9mil, respectively, and surface material of immersion gold.

It should be mentioned that any changes in the electrodes material or size of them that can change the range of interface capacitance is tolerable in our design by simply adjusting the value of some passive components.

Figure 2.2(a) shows the schematic of a simple circuit used for electrode-tissue impedance characterization. A test sinusoidal is applied to the skin by the first electrode, causing charges to flow through the electrode-tissue interface, while, the second electrode with the distance of 10 cm from the first electrode is attached to the skin. Current is integrated on the feedback capacitor, and the magnitude and the phase of the output sinusoidal are used to calculate the interface impedance. To verify the functionality and accuracy of this circuit for impedance measurement, a dummy test cell with a known impedance is used (Figure 2.2 (b)). Figure 2.2(c) shows that the measurement results using the proposed impedance characterization circuit are in a very good agreement with the known impedance of the dummy cell both for the real and imaginary parts.

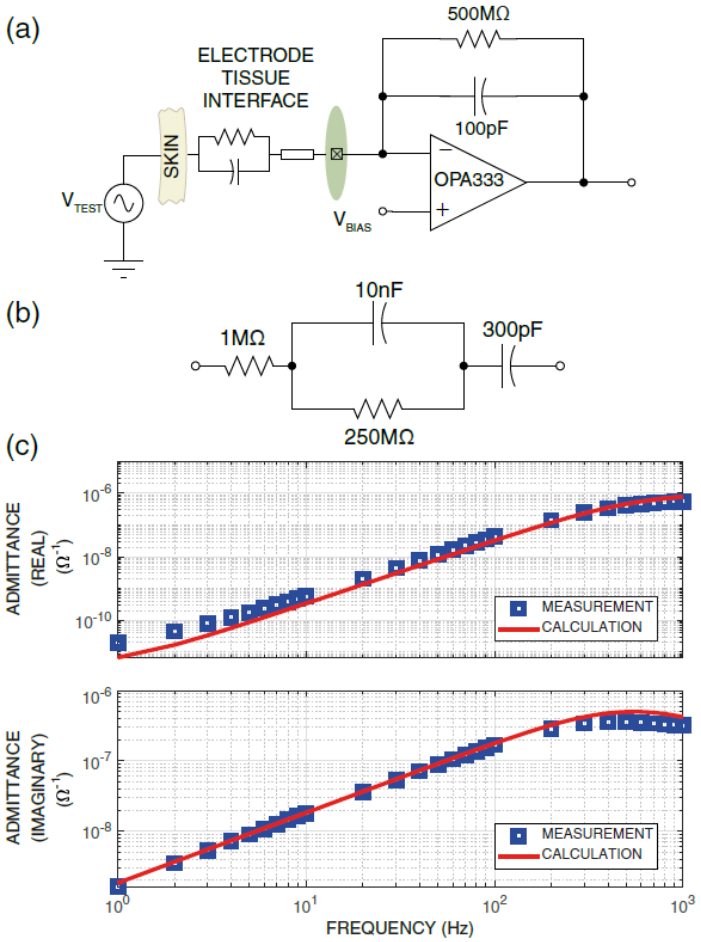


Figure 2.2 : (a) Schematic of the circuit used for electrode-tissue impedance measurement. (b) Dummy test cell used for characterization circuit validations. (c) Experimental test-cell characterization results in comparison with actual impedance values.

The circuit described above is used to characterize the actual impedance of the contact and non-contact electrodes used in this work. Figure 2.3 shows the magnitude and phase of the electrode-tissue interface admittance for the dry contact electrode when no

motion exists. The figure also shows what capacitance the interface admittance could be translated into.

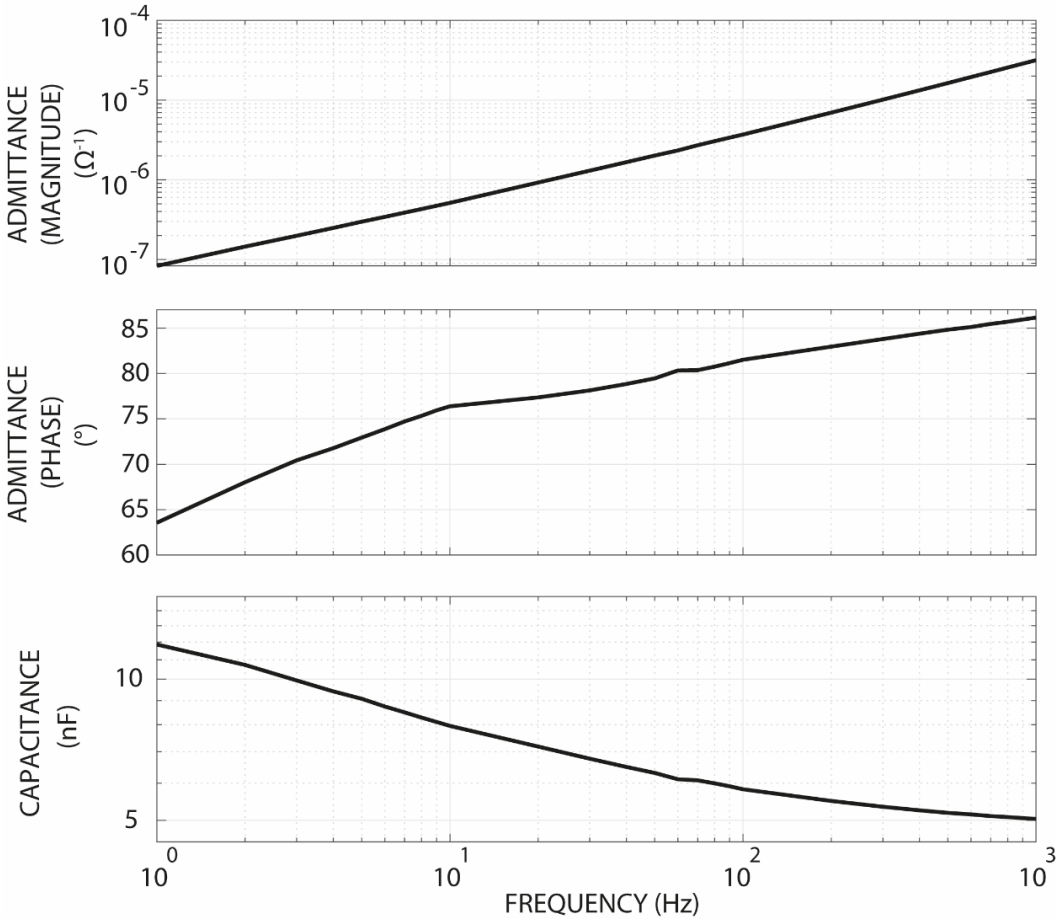


Figure 2.3 : The Admittance magnitude, phase, and equivalent capacitance of the electrode-tissue interface for the dry contact electrode.

As shown, the interface capacitance for the frequency range of 1 to 1000Hz varies from one to 11nF, which is in agreement with the typical values shown in the electrical model of Figure 2.1 . Figure 4 shows the similar results for the non-contact electrode. The interface capacitance is in the range of 10 to 200pF.

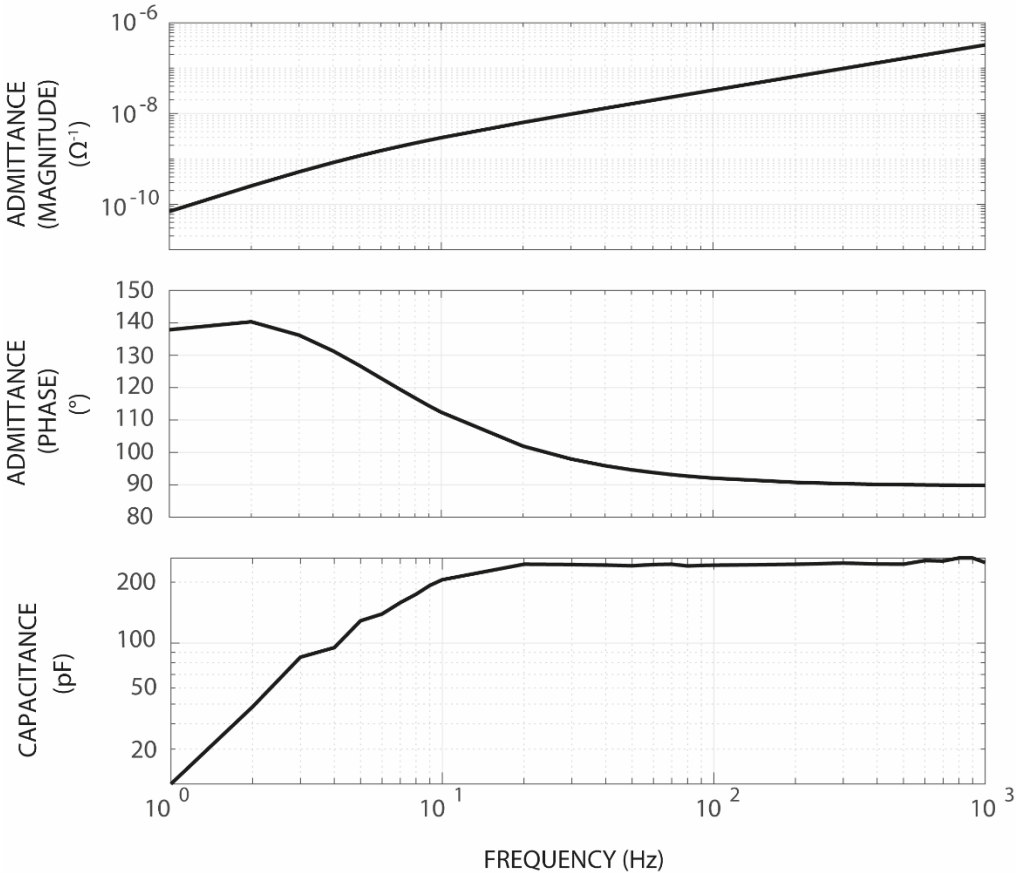


Figure 2.4 : Admittance magnitude, phase, and equivalent capacitance of the electrode-tissue interface for the dry non-contact electrode.

An electrode motion, which could occur due to the subject's random movements or respiration, results in a change in electrode-tissue interface impedance. For a dry electrode, these changes could be quite significant due to the lack of any adhesive material at the interface. Therefore, there is a very high possibility that a dry contact electrode loses its direct connection to the skin, leading to an additional capacitor (due to the gap) in the order of a 10-to-100pF in series with the rest of the model. This could increase the impedance seen by the analog front-end circuit by a factor of 1000, resulting in a large artifact in the

recorded EEG. On the other hand, an air gap and an insulating layer already exist for a non-contact electrode, resulting in motion-induced impedance variations at the same scale of the pre-motion interface impedance.

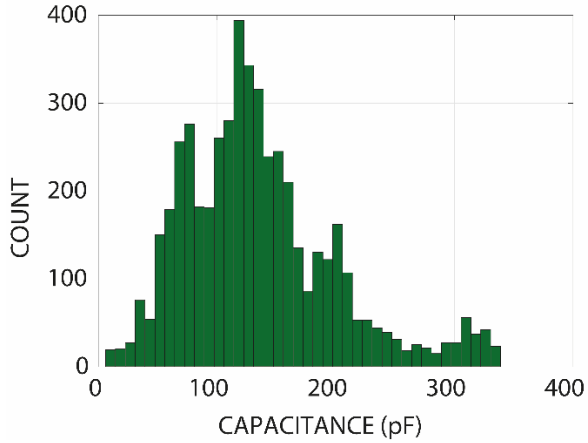


Figure 2.5 : Experimental results of 10,000 interface capacitance measurements of a non-contact electrode in the presence of various types of motions.

The custom-designed non-contact electrode was placed on the skin (with the insulating layer separating the electrode conductive material and the tissue) and the interface equivalent impedance was measured while an imitation of various facial gestures due to speaking, frowning, blinking, etc. that could result in a motion artifact were applied. Over the course of the experiment, 10,000 impedance measurements were conducted at 100Hz and the results are presented in Figure 2.5, which shows an average and standard deviation of 284pF and 122pF, respectively.

We tried to investigate the effect of motion artifact on electrode-tissue interface impedance. With the same setup shown in Figure 2.2(a) we applied a sine wave with the amplitude of 100mv(amplitude should be large enough to remove the effect of 60Hz noise)

and frequency of 100Hz(in this frequency our electrode is purely capacitive) through the first electrode. As described earlier, the second electrode is used as the input of the Op-Amp to record the value of the current generated by the sine wave. We tried to imitate any kind of movement that the electrode could experience due to the patients routine activities such as chowing, running and speaking, which is basically a combination of horizontal and vertical movements. We tried to cover the entire range and as we were moving the electrode, we were sampling the output of the Op-Amp with 1.33 kS/sec. This experiment has been conducted for 15 seconds, which resulted in 20000 data points. Figure 2.6 illustrates the translation of this data point to the capacitance value of the electrode- tissue interface.

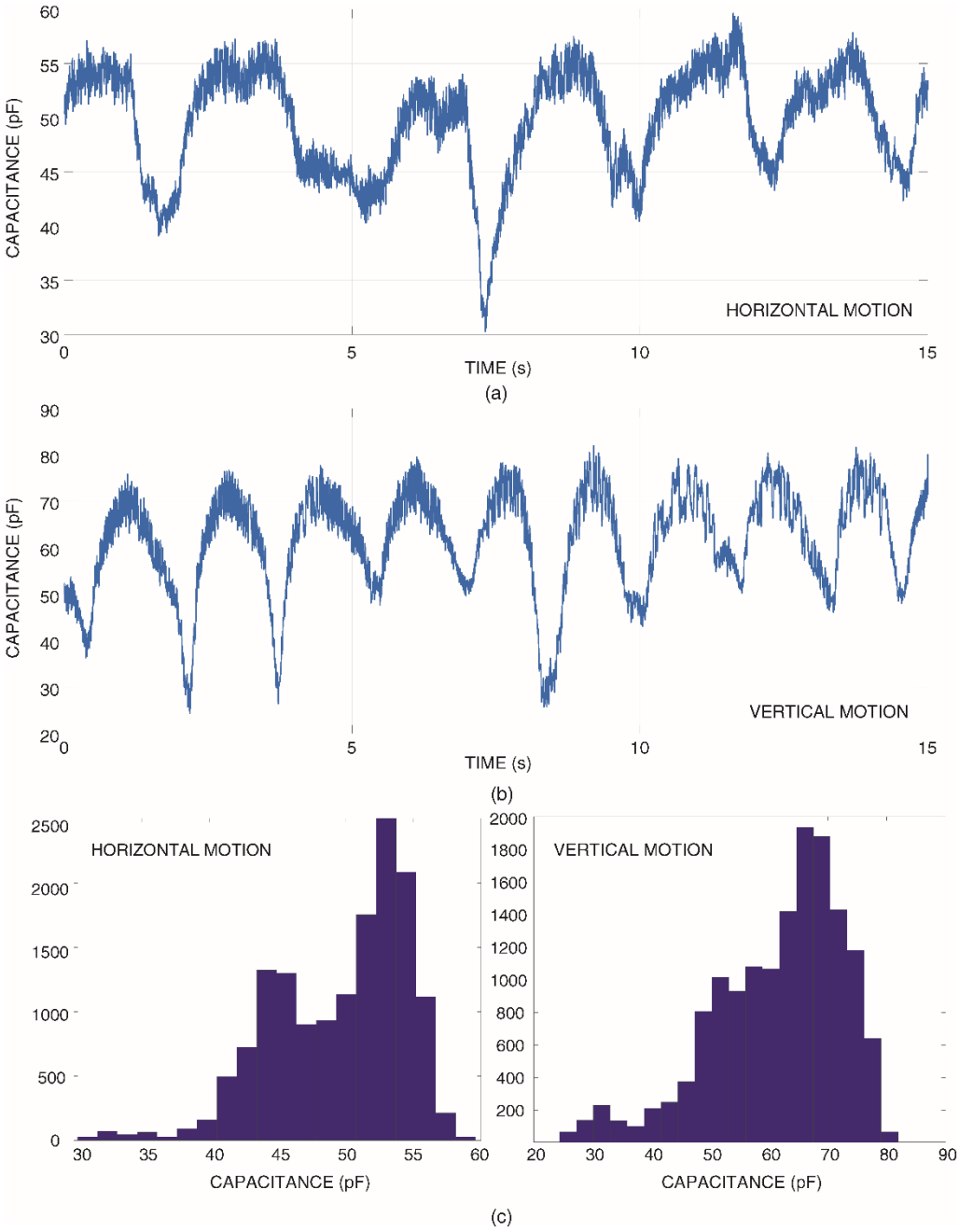


Figure 2.6 : Experimentally-measured electrode-skin capacitance variations due to (a) horizontal and (b) vertical movements of the electrode on the skin. (c) Distribution of the interface capacitance values during horizontal and vertical motions (20,000 measurements).

2.2 Electrode-tissue interface noise

Figure 2.7 shows a simplified electrical model of first stage of the electrode-tissue interface together with a simple voltage follower circuit. As it exhibits, a large input impedance as well as a unity gain, which leads to the amplifier not being saturated by the large motion artifacts [18], [28] We used this circuit to evaluate the effect of different components of the electrical model in the overall input-referred noise of the recording circuit. The input impedance of the voltage follower circuit is assumed infinite in our analysis, and finite (20GΩ) in the simulations.

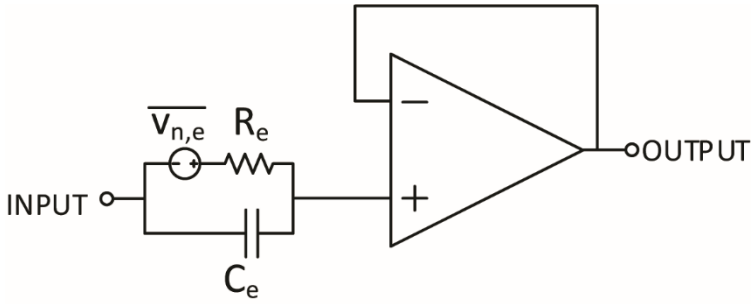


Figure 2.7 : Simplified electrical noise model of the electrode-tissue interface with a simple voltage follower circuit.

For the circuit shown in Figure 2.7, noise power spectral density (PSD) at the output is

$$S_{n,out}(f) = 4KTR_e \frac{1}{1 + (2\pi R_e C_e f)^2} \tag{2.1}$$

Which results in an integrated (over the neural bandwidth of interest) noise power of f_L (low cut-off frequency) and f_H(high cut-off frequency) that is,

$$p_{n,out} = \int_{f_L}^{f_H} 4KTR_e \frac{1}{1 + (2\pi R_e C_e f)^2} df \tag{2.2}$$

$$= \frac{2KT}{\pi C_e} \tan^{-1}(2\pi f_H . R_e C_e) - \tan^{-1}(2\pi f_L . R_e C_e)$$

This equation shows that, electrodes with either a very large or very small values for Re×Ce result in a very small integrated noise at the output. It should be noted that Eq. (2.2) only considers the resistive thermal noise generated at the interface and does not include other non-white noise sources such as what is discussed in [29]. The same is true about our noise simulations. We ignored other noise sources, simply because they either were too small compared to the thermal noise, or were similar for contact and non-contact electrodes, therefore, not impacting our comparative analysis. Figure 2.8 shows the simulated input-referred noise of the circuit shown in Figure 2.7, for an electrode with a capacitance of C_e=100pF and a resistance of R_e=20GΩ (nominal R_e and C_e values of a ~1 cm^2 dry electrode). For the simulations, the input node of the ideal opamp is biased through a 10 GΩ resistor. Compared to wet electrodes, the R_eC_e product is significantly increased, leading to a noise power spectral density that is an order of magnitude larger.

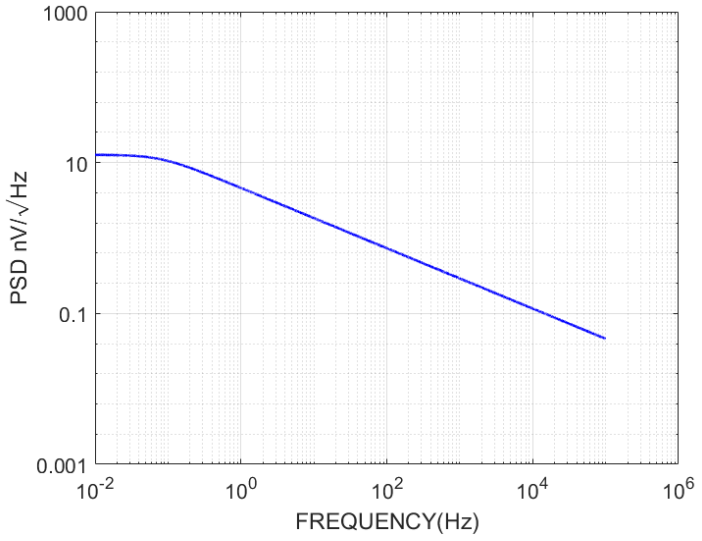


Figure 2.8 : Simulated input-referred noise of the circuit shown in Figure 2-6, for an electrode with a capacitance of Ce=100pF and a resistance of Re=20GΩ (nominal Re and Ce values of a ~1 cm^2 dry electrode).

Figure 2.9 shows the simulation result of input referred noise for electrodes with different $R_e \times C_e$. The figure confirms what was predicted by equation (2.2) and as it shows that wet electrode with (R_e=100kΩ, C_e=20nF) and near purely capacitive electrode (R_e=100kΩ, C_e=20nF) have the lowest input referred noise in EEG signal bandwidth (0.1Hz-1kHz).

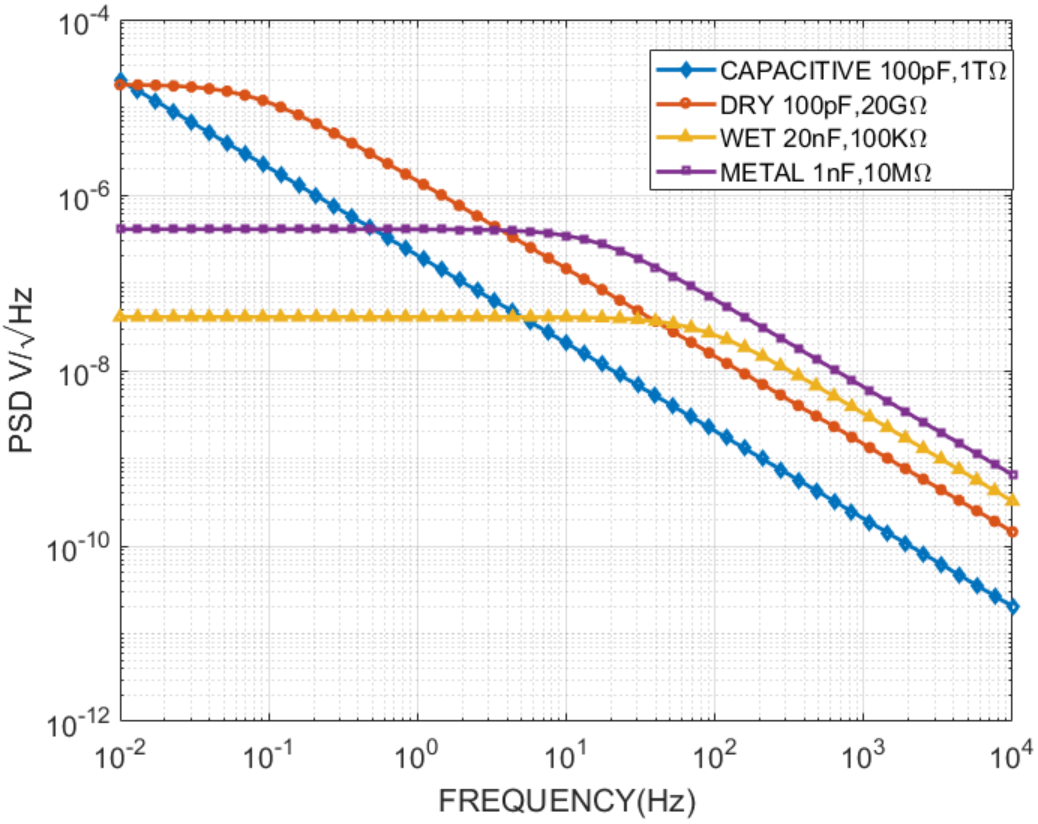


Figure 2.9 : Noise contribution of different types of electrodes to the noise power density of the input terminal of the recording front-end circuit.

2.3 Motion artifact

The characterized impedance variations at the electrode tissue interface demand for neural recording front-ends that can detect and compensate consequent artifacts induced by motion. For the typical EEG bandwidth of DC to 500Hz, the motion-induced 10-to-400pF range of variations in the interface capacitance results in hundreds of MΩ to a few GΩ variations in the impedance magnitude. This calls for an extremely high input impedance of the recording frontend amplifier in the order of TΩ. Figure 2.10 shows two of the most

common front-end architectures reported in the literature for dry-electrode EEG recording. To achieve the TΩ-range input impedance magnitudes, various impedance-boosting techniques have been reported in the literature [18],[28]. While the extremely high *Zin* ensures nearly no loss of AC signal even with a varying interface impedance (at the cost of additional power of impedance boosting module), it cannot prevent the large DC drifts caused by motion.

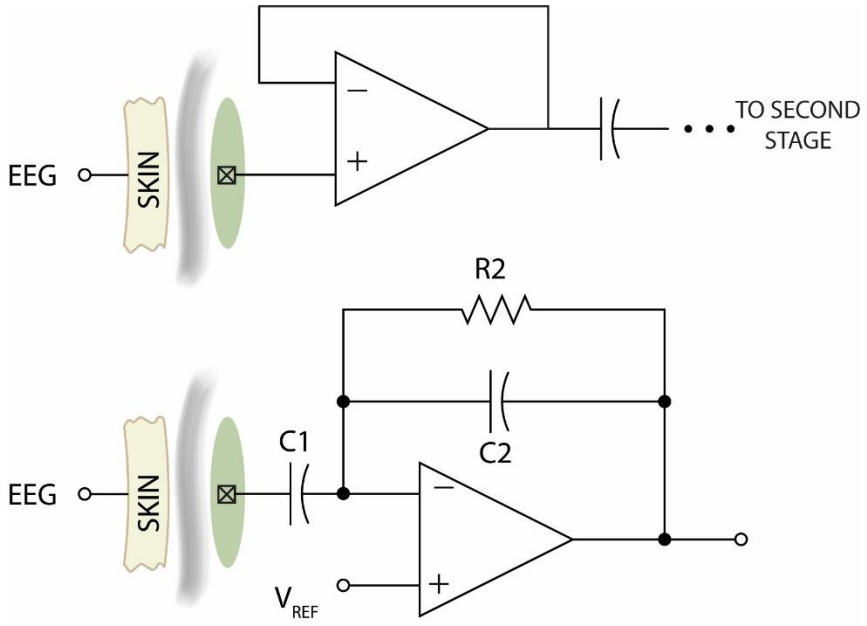


Figure 2.10 : Conventional analog front-end circuits used for EEG recording.

The source of such DC drifts could be explained by the current equation of a varying capacitor

$$i_C = C\frac{dV}{dt} + V\frac{dC}{dt} \tag{2.3}$$

Where V is the voltage across the capacitor. The second term of the Equation 1 ($V\frac{dC}{dt}$) means that the DC-decoupling property of capacitors is only valid as long as their capacitance is constant. In fact, a large DC voltage difference between the skin and the electrode could generate a current that is orders of magnitude larger than what is generated by the EEG signals ($C\frac{dV}{dt}$). This current is multiplied by the boosted input impedance of the front-end and appears as a large slow drift on top of the recorded signal. Therefore, not only the impedance boosting adds to the complexity and power consumption of the recording circuit, but also it becomes a disadvantage when there is an interface impedance variation due to the motion. Looking at the biopotential recordings reported in [22], [24], [30] such a slow drift is evident. Figure 2.11 shows the measurement results of our experiment, further confirming the above analysis.

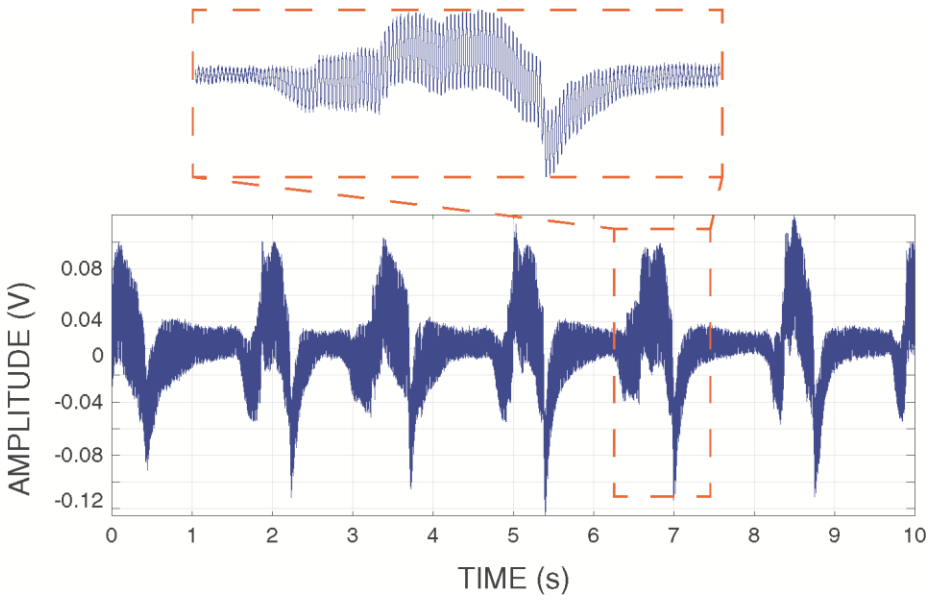


Figure 2.11 : Manifestation of motion artifacts as large DC drifts on top of the EEG recording.

Solving the above issue requires cancellation of the $V\frac{dC}{dt}$ term. Since the capacitance variations are unavoidable, the only way to do this is to ensure the same DC voltage for the electrode surface and the skin. This requires a front-end design that allows for control of the electrode DC voltage, hence, capacitively-coupled architecture may not be used. However, a modified version of this architecture, where the non-contact interface capacitance is used as the input capacitor could be employed, as shown in Figure 2.12.

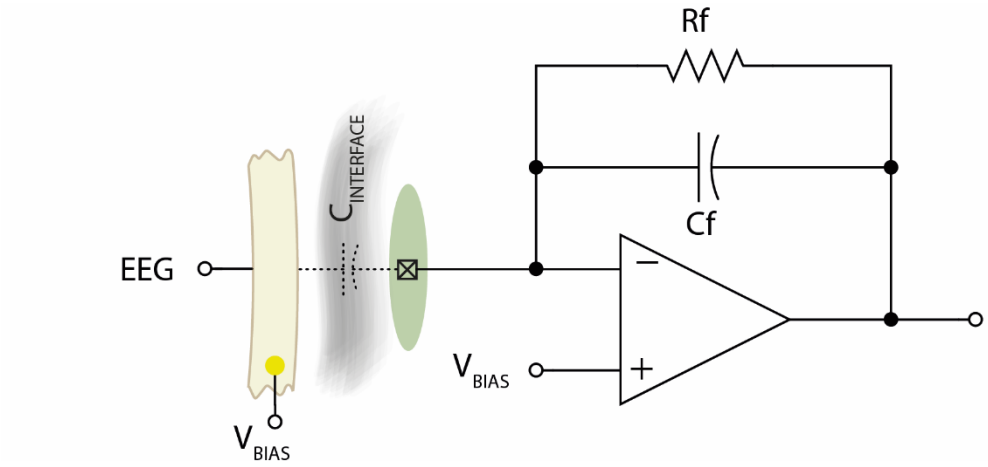


Figure 2.12 : A drift-less front-end circuit with artifact-modulated voltage gain for noncontact EEG recording.

This architecture allows for full control of the electrode DC potential as well as the skin, resulting in the full removal of the $V\frac{dC}{dt}$ term. Using this architecture, the front-end voltage gain is linearly dependent on the value of the interface capacitance. This means that the motion manifests itself as amplitude scaling instead of a large DC drift. Our experimental results shown in Figure 2.13 confirms such a behaviour.

The waveform shown in Figure 2.13 is a mixture of both EEG recordings (a.k.a, the signal of interest) and the motion-induced artifacts (in the form of voltage gain scaling). Based on these results, it could be imagined that if the scalings could be extracted from the EEG signal and applied inversely to their mixture, a relatively artifact-free amplified version of the EEG could be obtained. Such method does not rely on specific motion artifact patterns to be recognized and removed by a digital signal processing backend. It also avoids any amplifier output saturation. The details of solid-state circuit implementation of such circuit and various system and circuit-level considerations in its design are discussed in Chapter 4.

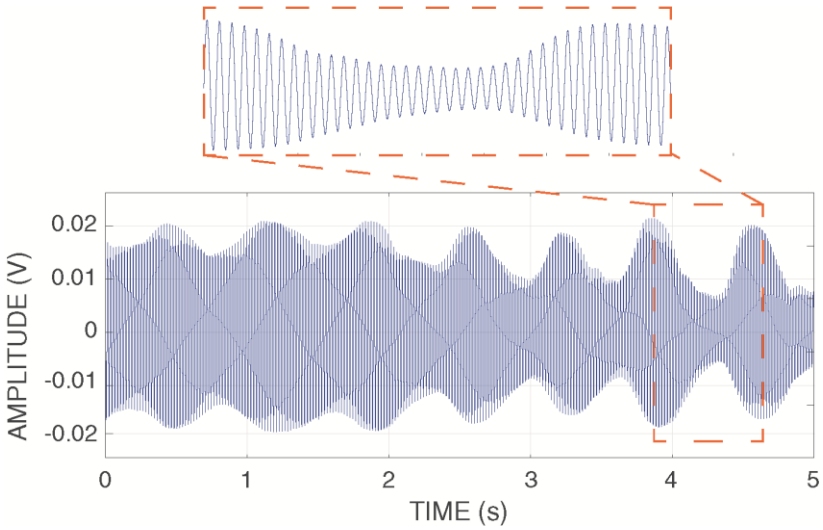


Figure 2.13 : Motion artifact manifestation in the recordings of the proposed analog front-end, showing gain scaling linearly proportional to the imitated motion.

Chapter 3

An 8-Channel 12 mm^2 EEG Recording IC with Mixed-Signal Motion Artifact Detection and Removal

In this chapter, we will present an 8-channel SoC with a novel channel architecture, capable of real-time detection and removal of motion artifacts. The VLSI circuit implementation and characterization results are presented. Compared to the state of the art, the most fundamental advantages of the presented system are (a) performing the motion detection and removal in the analog domain and before signal amplification, which prevents the risk of amplifier saturation, (b) being effective for any type of artifact, independent of their manifestation in the EEG signal (i.e., no need for digital pattern recognition), and (c) needless of injecting any current or voltage pulse into the skin for interface characterization.

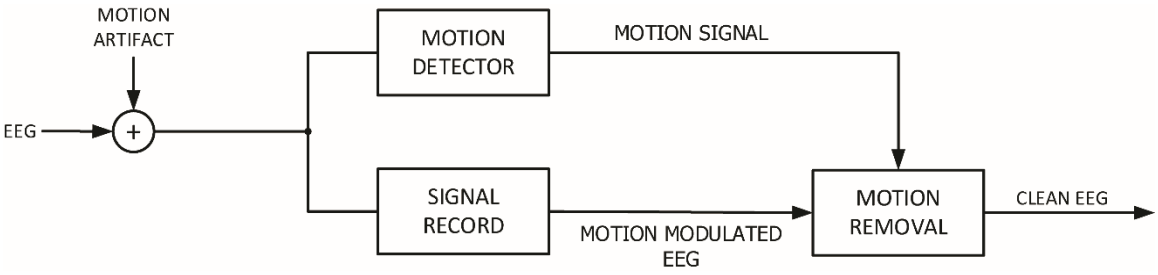


Figure 3.1: conceptual block diagram of the presented EEG recording channel architecture.

First, we will describe the system-level architecture and how motion is detected and removed conceptually and analytically. Next, individual modules employed in the presented design are described in details. A detailed noise analysis of the presented design together with its comparison with the conventional architectures is also presented. The chapter ends with presenting the on-chip physical design and implementation of the presented work, as well as experimental characterization results.

3.1 Channel architecture

Figure 3.1 shows the conceptual block diagram of the presented EEG recording channel architecture. As shown, the signal acquired at the electrode contains both neural activities and motion artifacts. As discussed in Chapter 2, the effect of motion is basically modulating of the amplitude of the EEG recordings by the physical motion magnitude. The presented architecture conducts motion removal in two stages. In the first stage, one of the two parallel paths (the upper one in Figure 3.1) extracts the effect of motion from the contaminated signal and outputs a waveform with a magnitude that is proportionate to the range/severity of physical motions. We will call this waveform the "motion signal", as

indicated in the figure. At the same time, the lower parallel path amplifies the signal acquired from the electrode with a small voltage gain that is proportionate to the motion range. The small gain assures that the amplifier's output won't be saturated, and the motion-affected variable gain will be equalized in the next stage.

In the second stage, the motion signal magnitude is used to set the voltage gain of the second amplification stage (motion removal) in an inverted manner (i.e., the higher the magnitude, the smaller the gain). By doing so, the first stage gain variations caused due to physical motions are fully compensated, and the output of the second stage amplifier (motion removal) will be a clean EEG signal that is amplified with a constant gain at all times, with or without physical motions.

It should be noted that all of the above must be implemented without a substantial increase in the power consumption or area of the recording channel, and the final design must meet the basic requirements of an EEG recording front-end circuit, which are low input-referred noise to achieve a high signal-to-noise ratio (SNR), high input impedance (to avoid signal loss and achieve high common-mode signal rejection), high voltage gain, and sufficient frequency bandwidth (typically, 300-to-500 Hz, depending on the application). The circuit-level implementation of the presented design is discussed in the next sections.

3.2 Recording Front-End Architecture

For recording bio-signals from electrodes with a large impedance (e.g., dry electrodes), there are generally two main approaches: (a) using an analog front end (AFE) with an extremely high input impedance to avoid signal attenuation at the input of the amplifier (voltage-follower amplifier) or (b) using an AFE with near zero input impedance to draw all the output current of the electrode (transimpedance amplifier). The main features of these two structures are compared in the following paragraphs and the suitable design for non-contact EEG recording in the presence of motion is concluded.

Figure 3.2 presents the circuit schematic for the voltage follower amplifier (buffered amplifier) and transimpedance amplifier. Reviewing the literature, different variations of the voltage follower circuit shown in Figure 3.2 (a) seem to be popular for surface EEG front-ends. This is mainly due to its extremely high input impedance compared to more conventional neural amplifiers such as the capacitively-coupled architecture proposed in [31]. The importance of the high input impedance of this circuit is because its output voltage is equal to Zin / (Zin+Zelec). Therefore, a very high input impedance guarantees that any large variations of the electrode-tissue interface impedance is not going to affect the amplitude of the voltage at the output of this circuit. The main issue with this configuration is that it requires an extremely large resistor to bias the input terminal of the OpAmp. The resistance is in parallel with the input impedance of the OpAmp, so it should large enough (e.g. > 100GOhm) to ensure that the input impedance of the front-end circuit remains very large. Implementation of such a large resistance on

the chip is impractical. Also, it cannot be implemented using a pseudo-resistor circuit such as the one proposed in [31] as we don't have control on the voltage of both sides of the resistor.

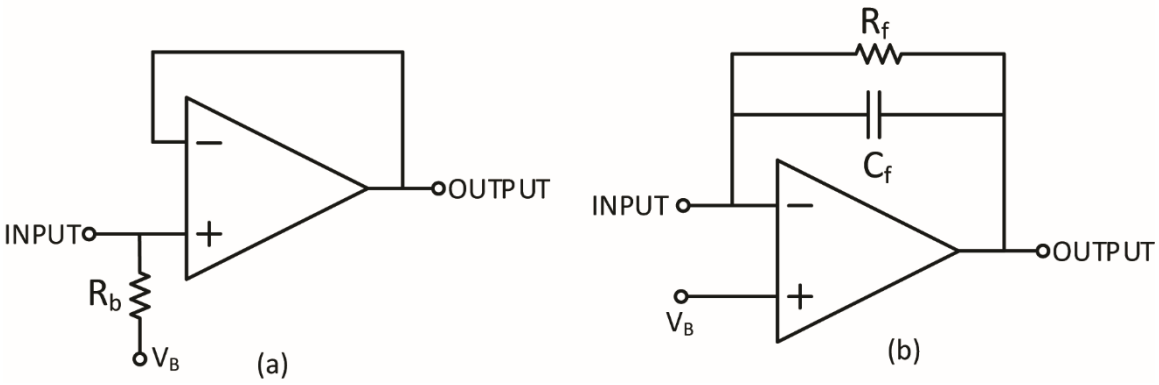


Figure 3.2 : Circuit schematic of (a) voltage follower amplifier, and (b) transimpedance amplifier.

The charge amplifier circuit (Figure 3.2 (b)), which was also discussed in the previous chapter (Figure 2.12) is a modification of the conventional capacitively-coupled neural amplifier (Figure 2.10(b)) that is considered to be the most popular front-end architecture in the literature. For a capacitively-coupled amplifier, the voltage gain is equal to the ratio of input capacitor to the feedback capacitor. Assuming that the electrode-tissue interface impedance for a non-contact electrode could be modeled as a simple capacitor (as discussed in Chapter 2), then the voltage gain of the circuit presented in Figure 3.2 (b) will be the ratio of the interface capacitance over the feedback capacitance. Additionally, since we know that the interface capacitance is linearly and directly proportional to the range of physical motions, then we can claim that the voltage gain of the charge amplifier presented in Figure 3.2 (b) is directly modulated by the physical motions.

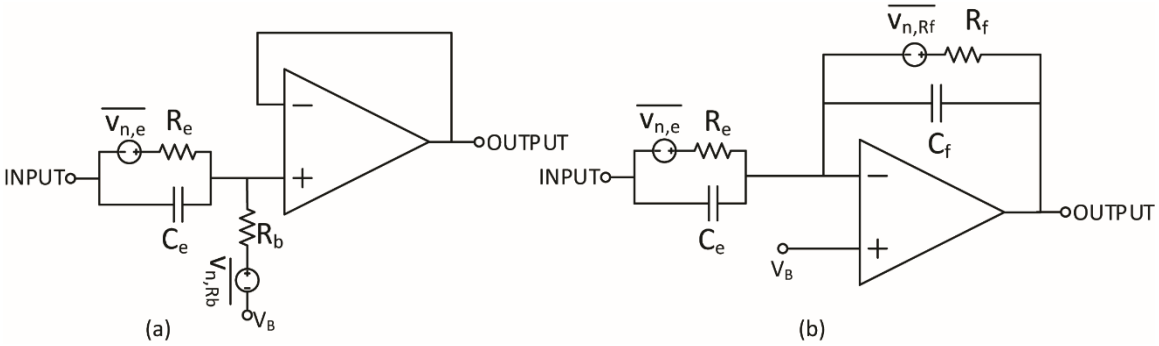


Figure 3.3 : Front-end noise model for (a) voltage follower amplifier, and (b) transimpedance amplifier.

3.2.1 Noise analysis

Noise analysis in these structures is divided in two different source of noise as presented in Figure 3.3. The first noise source we want to investigate is the noise generated by the electrode-tissue interface. As presented in section 2.2 the contribution of electrode-tissue interface noise in the power spectral density of the input-referred noise in buffered amplifier structure is calculated as,

$$S_{n,in}(f) = 4KTR_e \frac{1}{1 + (2\pi R_e C_e f)^2} \tag{3.1}$$

The contribution of the electrode-tissue interface noise in the output noise PSD for the case of the transimpedance amplifier structure is,

$$S_{n,out}(f) = \frac{4KT}{R_e.(2\pi C_f f)^2} \tag{3.2}$$

which makes its input-referred noise PSD equal to,

$$S_{n,in}(f) = \frac{4KT}{R_e.(2\pi C_f f)^2} \times \frac{\left(2\pi R_e C_f f\right)^2}{1+(2\pi R_e C_e f)^2} \tag{3.3}$$

$$= 4KTR_e \frac{1}{1+(2\pi R_e C_e f)^2}$$

Based on the above equations the electrode-tissue interface noise has the same contribution to the input-referred noise in both structures.

Second comparison is the noise of the biasing structures which means the feedback resistor in the transimpedance amplifier and the biasing resistor at the OpAmp's positive terminal of the buffered amplifier. Equation (3.4) illustrates the feedback resistor noise contribution to the input-referred noise PSD of the buffered amplifier structure.

$$S_{n,in}(s) = 4KTR_b \left|\frac{z_e}{z_e+R_b}\right|^2 \left|\frac{z_e+R_b}{R_b}\right|^2 \tag{3.4}$$

$$= \frac{4KT}{R_b}|z_e|^2$$

Also, equation (3.5) shows the biasing resistor noise contribution to the input-referred noise PSD of the charge amplifier structure.

$$S_{n,in}(s) = 4KTR_f \left|\frac{1}{1+R_f C_f}\right|^2 \left|\frac{1+R_f C_f}{R_f}\right|^2 |z_e|^2 \tag{3.5}$$

$$= \frac{4KT}{R_b}|z_e|^2$$

The input-referred noise PSD of the two structures are also is plotted in Figure 3.4, which also confirms that biasing resistor has the same noise contribution in both amplifier structures. Although, noise level for both structure is equal, transimpedance amplifier has a greater voltage gain that relaxes the design of next stage in terms of the noise requirement as the noise contribution of the next stages will be divided by the gain of the first stage. It should be mentioned that the OpAmp is the other source of noise but has a negligible effect in comparison with the other two sources (as shown in Figure 3.4), hence, it is not discussed.

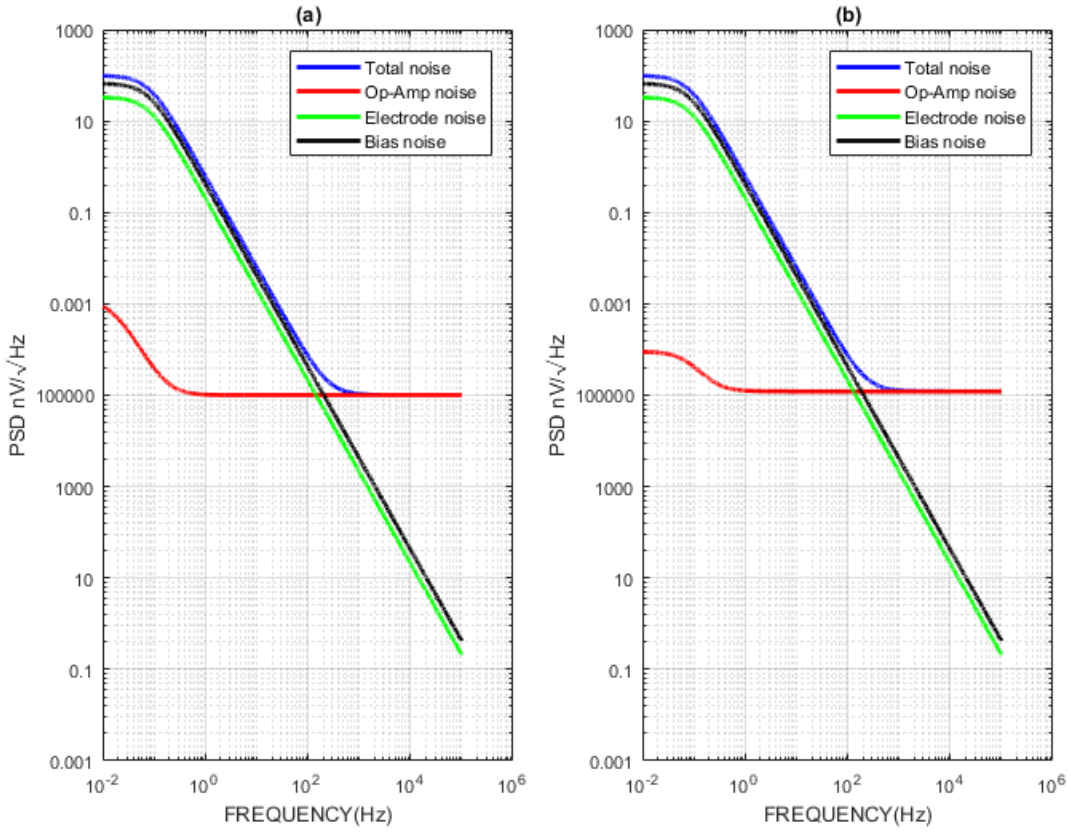


Figure 3.4 : Input referred noise for (a) voltage follower amplifier, (b) transimpedance amplifier

3.2.2 Front-End Implementation

Based on the above discussions, it seems that the charge amplifier is a good choice for the front-end stage as it exhibits a voltage gain that is linearly modulated by the motion while also having benefits in terms of noise performance.

Figure 3.5 presents transistor-level implementation of the OpAmp employed in the recording front-end that its block diagram was depicted in Figure 3.2 (b). Using the circuit presented in Chapter 2, we measured the electrode-skin interface capacitance variations to be in the range of 30 to 200pF. Therefore, to have a voltage gain that is greater than one, capacitance of feedback path is chosen to be 10p (although smaller values yield a higher gain, which increases the risk of output saturation). Considering the significant low-frequency components of the EEG signals, the amplifier should be designed in a way that it is operational down to sub-Hz frequencies. The lower frequency limit of the selected charge amplifier is set by the two passive components in the feedback path as $f_L = \frac{1}{2\pi C_f R_f}$. Given that the feedback capacitor was selected to be 10pF, a 1Hz high-pass pole requires the feedback resistor to be at least 160 GΩ. This is resulted in a huge resistor of 160 GΩ. To implement such a huge resistor structure pseudo-resistor with two NMOSs is used. This structure was based on what was first proposed in [31] and discussed in details in [32], [33]. As mentioned in [32], the actual resistance of such structure might go beyond the simulation results predicted by the foundry models. Therefore, the current drew from the negative input of OpAmp can change the DC operating point of the output, which in the

worst case it can result in output saturation. In order to solve this problem, the gate voltage of the NMOSs are connected to an adjustable DC input.

The high cut-off frequency of this structure can be determined by g_m of the input transistors the output capacitance. Therefore, so capacitor C_H is chosen in a way that high cut-off frequency becomes 200Hz.

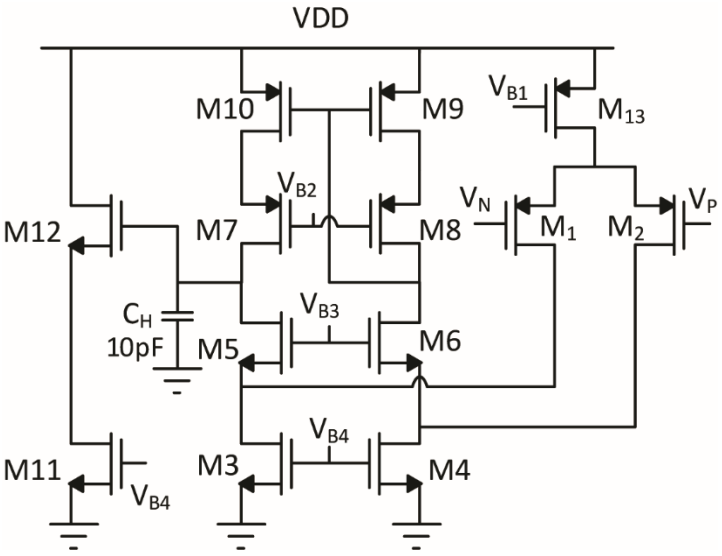


Figure 3.5 : Transistor-level implementation of the OpAmp used in the body of the presented recording front-end.

As presented in Figure 3.6, the post-layout simulation results for the magnitude and phase response of the OpAmp shown in Figure 3.5, confirming its voltage gain and 3-dB bandwidth. Table 3.1 reports the sizing information for the transistors of the OpAmp shown in Figure 3.5. Figure 3.7 illustrates the experimentally measured input referred noise for the first stage.

Table 3.1: Sizing information for the transistors of the OpAmp used in the body of the presented recording front-end.

Transistor	M_1	M_2	M_3	M_4	M_5	M_6	M_7
W/L	$\frac{4.2\mu}{900n}$	$\frac{4.2\mu}{900n}$	$\frac{1.8\mu}{900n}$	$\frac{1.8\mu}{900n}$	$\frac{1.8\mu}{900n}$	$\frac{1.8\mu}{900n}$	$\frac{4\mu}{900n}$
Transistor	M_8	M_9	M_{10}	M_{11}	M_{13}		
W/L	$\frac{4\mu}{900n}$	$\frac{2.4\mu}{900n}$	$\frac{2.4\mu}{900n}$	$\frac{1.35\mu}{350n}$	$\frac{4.8\mu}{900n}$		

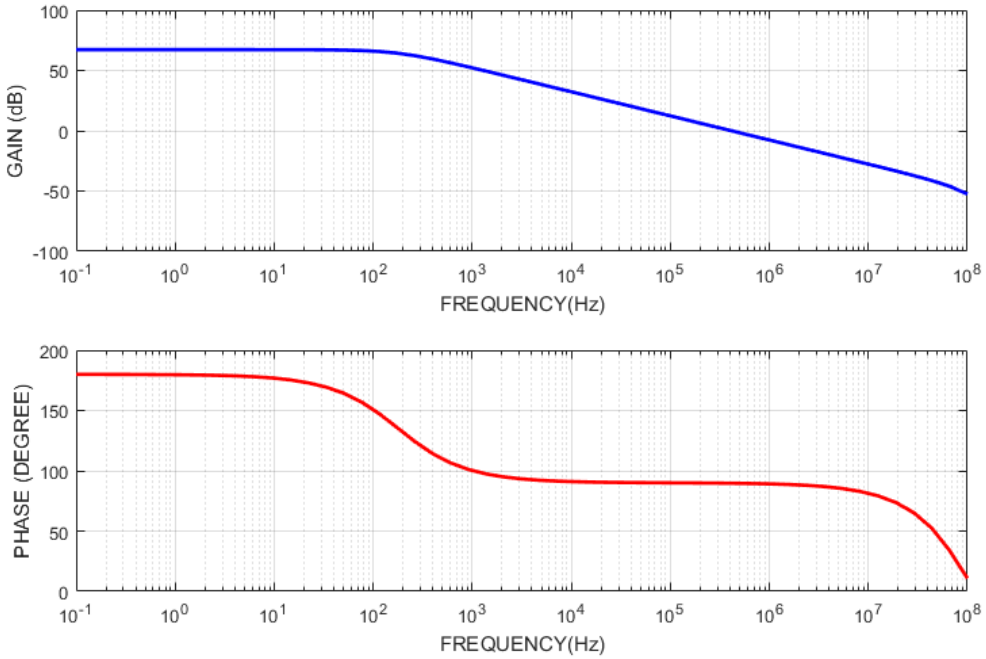


Figure 3.6: Simulation result for frequency response of the input stage of the recording channel.

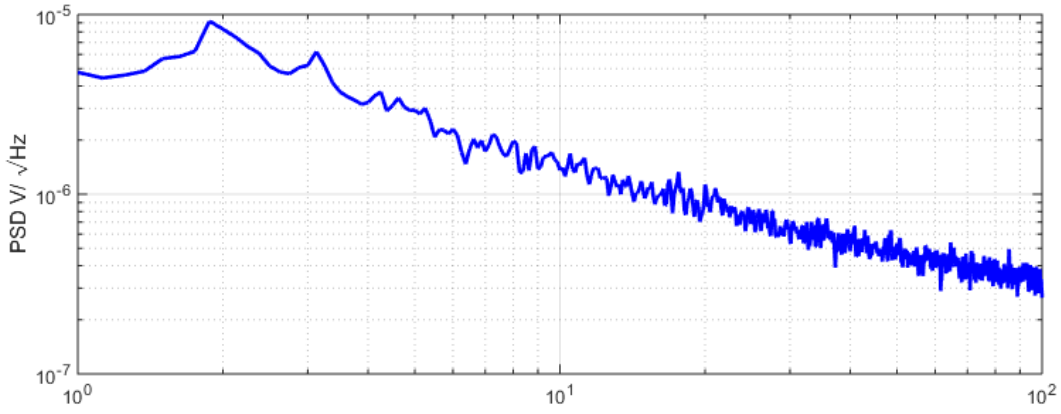


Figure 3.7: Experimentally measured input referred noise.

3.3 Motion extraction

Considering the linear relationship between the motion-induced amplitude scaling and the interface capacitance, the motion artifacts could be extracted using analog techniques. As shown in Figure 3.1, the first stage of our proposed channel architecture is by two parallel paths.

The only difference between the two paths is a large DC offset applied to the input terminal of one of them compared to the other one. Using this configuration, by biasing the skin DC voltage in the proximity of the electrode to be equal to the input DC bias of the lower path, the current of lower path will be equal to $C_{INTERFACE}\frac{dV_{EEG}}{dt}$ (that is, the second term of the current, $V\frac{dC}{dt}$ will be zero as we have made the voltage across the $C_{INTERFACE}$ to be equal to zero). Therefore, the lower path output voltage will be the integration of this

current, $V_{EEG}\frac{C_{INTERFACE}}{C_f}$ which will look like Figure 2.13. On the other hand, the upper path output voltage will be equal to $\frac{1}{C_f}\int V_{CTRL}\frac{dC_{INTERFACE}}{dt}+\frac{1}{C_f}\int C_{INTERFACE}\frac{dV_{EEG}}{dt}$.

Motion-induces artifacts frequency is typically in the range of below 1Hz to 10 Hz [34]. The amplitude and frequency of EEG signal is lower than 100µV and 300Hz respectively. Based on these ranges, we chose V_{CTRL} as 50mV that results in the second term of the above expression to be negligible compared to the first term, hence, making the result signal the representation of motion-induced artifact. It should be noted that this V_{CTRL} could be adjusted to address any effect of Op-Amp offset on the motion extraction.

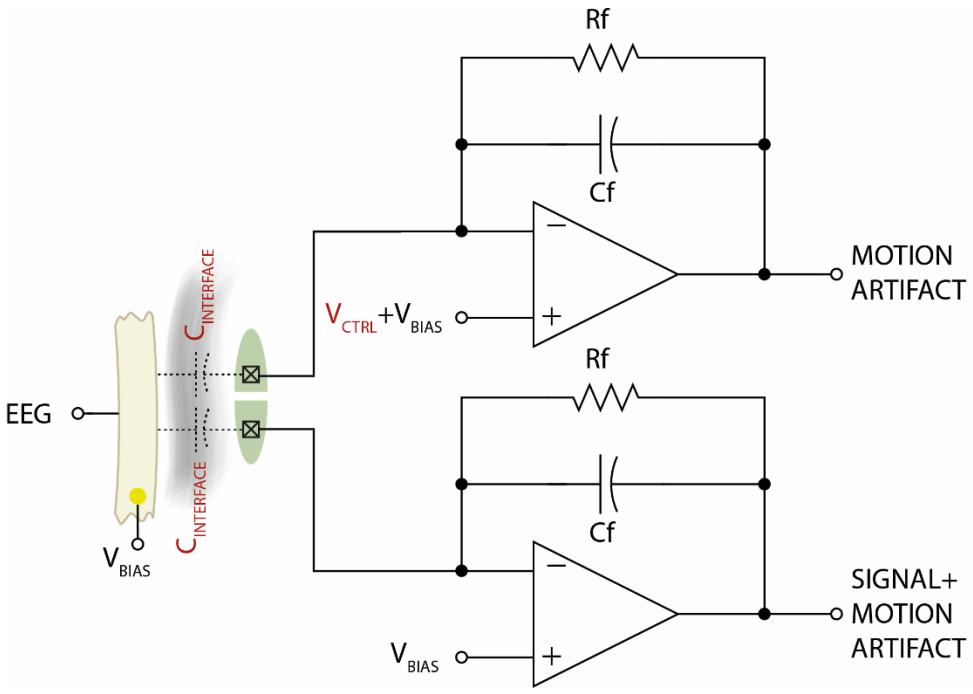


Figure 3.8 : Simplified circuit schematic of the first stage of the presented EEG recording channel architecture.

Once we perform the integration, the upper path (a.k.a. the motion detector) output voltage will be equal to $V_{CTRL}\frac{\Delta C_{INTERFACE}}{C_f}$, showing that it is proportional to the variations of the interface capacitance, therefore, representing the motions. The term $\Delta C_{INTERFACE}$shows that motion detector output is proportional to the variation of the electrode capacitor and not its absolute value. It is important because the absolute value of capacitance of the electrode determines the gain of first stage. For signal recording path, absolute value of voltage is not important because this structure blocks the DC of the V_{EEG} and just variation of signal is important.

In order to have absolute value of the capacitance of the electrode at motion detector output, initial value of the capacitance should be measured for a pre-determined period. To do this, we have designed the circuit shown in Figure 3.9, which is a modified version of the circuit shown in Figure 3.8 that is capable of recording absolute value of capacitance. Figure 3.9 (a) and (b) show two operating modes of this circuit. First, switch S_1 is closed, which sets the voltage of the non-inverting side of OpAmp to V_{BIAS}. In this stage feedback, capacitor is discharged. During the second mode of operation, feedback switch is opened, which charges the positive input terminal of the OpAmp to V_{CTRL} + V_{BIAS}. Therefore, a charge of $V_{CTRL}\frac{C_{INTERFACE}}{C_f}$ is transferred to the feedback capacitor, which makes the output voltage equal to $(V_{CTRL}+V_{BIAS})+V_{CTRL}\frac{C_{INTERFACE}}{C_f}$. The first term is a predetermined known voltage that can be easily removed. Figure 3.10 shows the relative error in

capacitance measurement by the motion detection stage for the entire range of possible values for the interface capacitance.

Based on the above description the proposed setup for measuring the interface capacitance could also account for any difference in electrode-tissue interface capacitance due to the system-to-system variation.

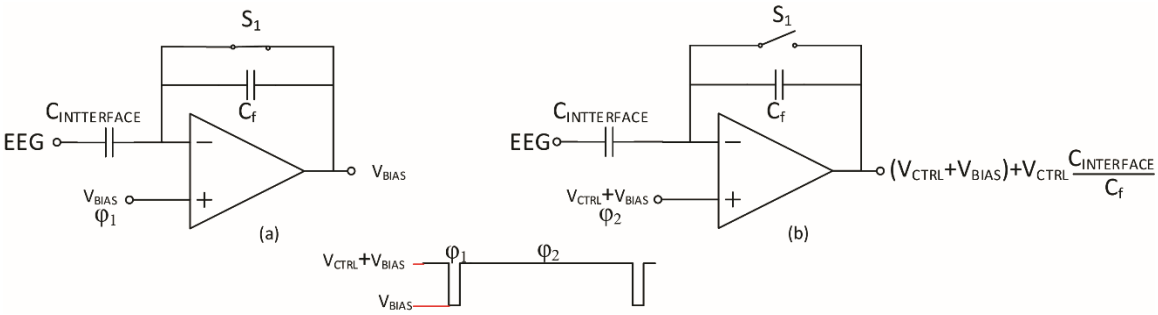


Figure 3.9 : Two operating modes of the motion detector circuit that is used in the body of the recording channel.

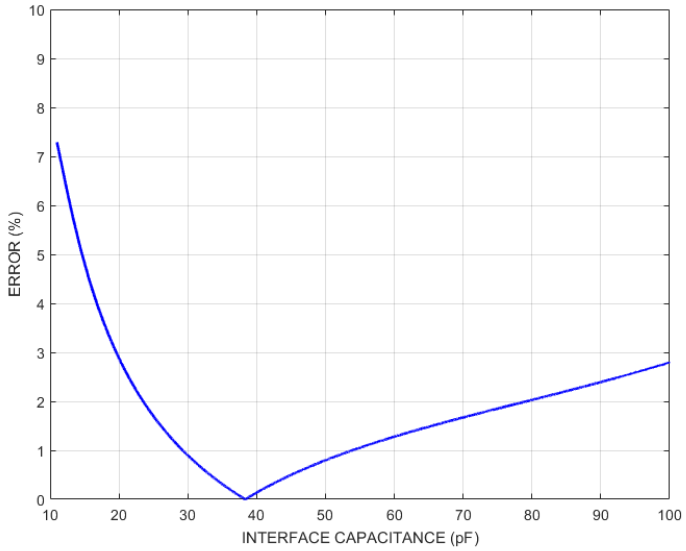


Figure 3.10: The relative error in capacitance measurement by the motion detection stage for the entire range of possible values for the interface capacitance.

3.4 Artifact removal

As mentioned, the second stage of the proposed recording channel architecture is responsible for motion artifact removal. As it was discussed in details in Chapter 2, and was illustrated in Figure 2.13 , the effect of motion on the output voltage of the charge amplifier circuit presented in the previous section will be in the form of amplitude variations proportional to physical motions.

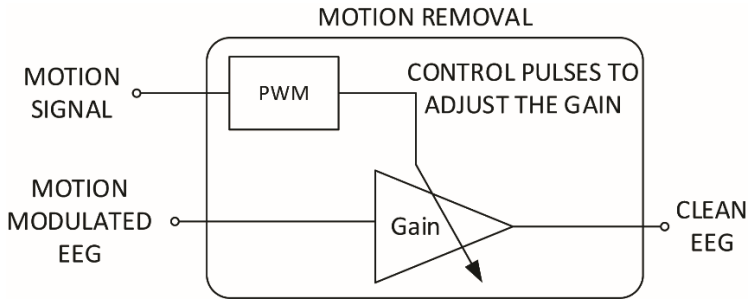


Figure 3.11 : A conceptual block diagram of the employed motion artifact removal circuit.

Here we try to compensate for these amplitude variations using the information extracted by the motion detector circuit described in the previous section. One of the choices to implement the voltage controlled variable gain was using a varactor. However, due to nonlinearity and capacitance variation range of the varactor which has been discussed in [35], varactor-based VCG was not a suitable solution in our application.

As it is shown in Figure 3.11 the magnitude of the "motion signal" is translated into pulse widths of a pulse train (i.e. pulse-width modulation), and next, the pulse-width modulated signal is used to control the gain of an amplification stage in an inverted fashion. Detailed implementation of these blocks are provided in the remaining of this section.

3.4.1 PWM block

Figure 3.12 shows the simplified picture of a sigma delta pulse width modulator (PWM) block. It generates pulses from zero to VDD with the duty cycle proportional to the amplitude of the motion signal.

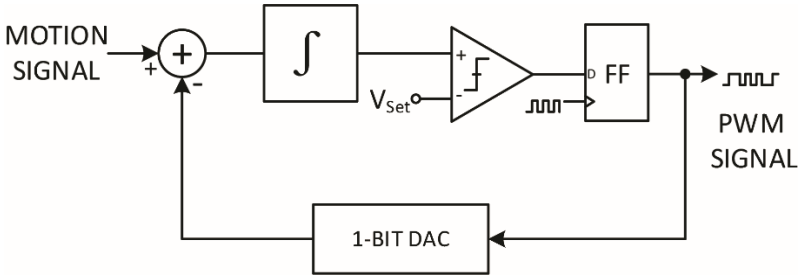


Figure 3.12 : Internal block diagram of the pulse width modulation circuit implemented in each recording channel.

The detailed implementation of the integrator and the 1-bit DAC of the PWM are shown in Figure 3.13. The delta sigma structure and OTA feedback force the inverting input terminal and the output voltages of the OTA to be close to V_{Set}. The 1-bit DAC is implemented with an NMOS ($\frac{20\times250n}{250n}$) and a PMOS ($\frac{30\times250n}{250n}$) that are connected to V_{P1} and V_{P2} respectively. V_{P1} and V_{P2} are the minimum and maximum voltage of motion detection output. Therefore, when PWM output (D) is zero, DAC output is V_{P2} and when PWM output is VDD, DAC output is V_{P1}. Nodal analysis at the inverting input of the OTA results in an equation that shows the relationship between the duty cycle of PWM output (D) and the input voltage of PWM, V_{in}.

$$DV_{P1} + (1 - D)V_{p2} + V_{in} = 2V_{Set} \tag{3.6}$$

$$D = \frac{V_{In} + V_{p2} - 2V_{Set}}{V_{p2} - V_{p1}}$$

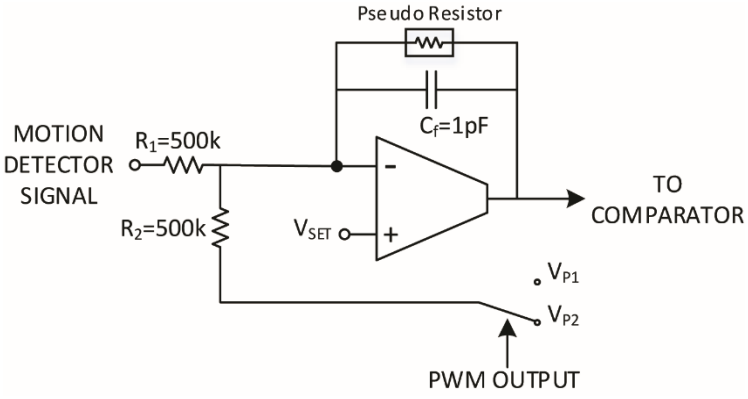


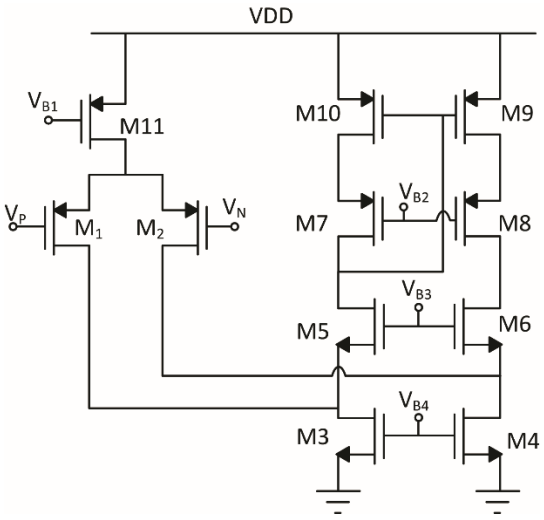
Figure 3.13 : Schematic of integrator and DAC.

As it was shown in the previous section, the motion detector output voltage is equal to $(V_{CTRL} + V_{BIAS}) + V_{CTRL}\frac{C_{INTERFACE}}{C_f}$. In order to have a linear relationship between duty cycle of the PWM signal and the gain of the first stage ($\frac{C_{INTERFACE}}{C_f}$), V_{Set} is chosen in a way that $2V_{Set} - V_{p2}$ is equal to $V_{CTRL} + V_{BIAS}$. If we replace these two terms in equation (3.6) we will have

$$D = \alpha \frac{C_{INTERFACE}}{C_f} \tag{3.7}$$

where α is the ratio of V_{CTRL} to the V_{P2}-V_{P1}.

The schematic of the OTA used in the circuit of Figure 3.13 along with the transistor sizing information, is shown in Figure 3.14.



Transistor	M_1	M_2	M_3	M_4	M_5	M_6	M_7	M_8	M_9	M_{10}	M_{11}
W/L	$\frac{4.2\mu}{900n}$	$\frac{4.2\mu}{900n}$	$\frac{1.8\mu}{900n}$	$\frac{1.8\mu}{900n}$	$\frac{1.8\mu}{900n}$	$\frac{1.8\mu}{900n}$	$\frac{4\mu}{900n}$	$\frac{4\mu}{900n}$	$\frac{2.4\mu}{900n}$	$\frac{2.4\mu}{900n}$	$\frac{4.8\mu}{900n}$

Figure 3.14 : Circuit schematic of OTA in integrator.

As shown in Figure 3.12 and Figure 2.11, the the integration of difference between the current input and digitized representation of the previous value of the input, this signal is compared to the voltage at negative input of comparator, V_{Set}. As the comparator output is reset in each clock period, a D-type flip flop (DFF) is used after the comparator to prevent propagation of this reset event to the next stage. The DFF clock is delayed by 100ns (frequency of clock is 1MHz), which allows enough time for the comparator to make a decision. A strong-arm comparator similar to [36] is used in this design and to ensure the symmetry of the design a dummy DFF is used at the floating output of the comparator.

Figure 3.15 shows the measurement result of the PWM block, confirming the linear relationship between the motion signal's magnitude and the pulse widths at the blocks output.

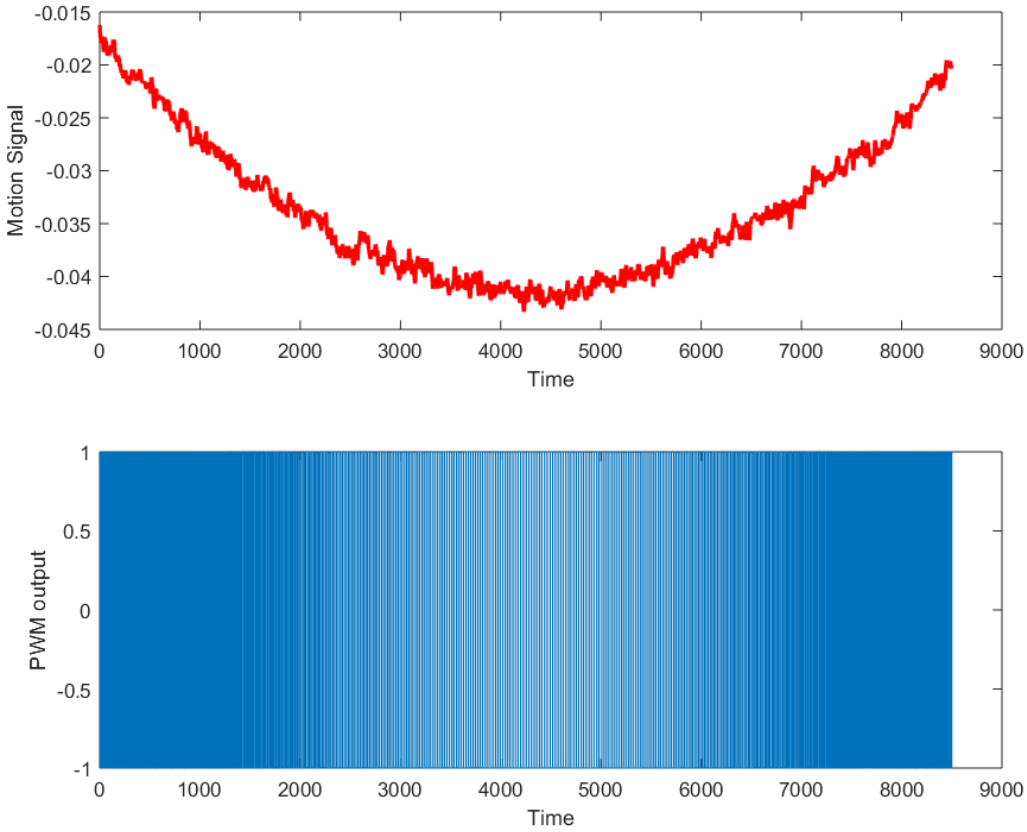


Figure 3.15: Output of the PWM block to the input signal from motion-extraction stage.

In order to check the linearity of the PWM block, we applied a ramp signal, between 0.7V to 0.8V, which is the designed full-scale range of the PWM block, which is controllable through two control voltages (V_{P1} and V_{P2}). Figure 3.16 illustrate the percentage of duty cycle for each level, which confirms the linearity of the PWM block.

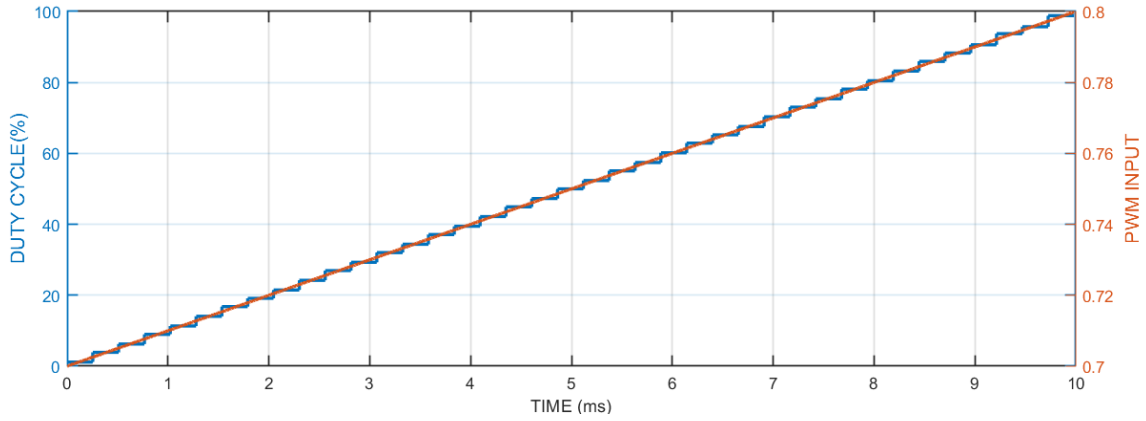


Figure 3.16: Simulation results for testing the PWM linearity.

3.4.2 PWM-Controlled Variable Gain Amplifier

As mentioned in the beginning of this chapter, the second stage amplification should have a variable gain, with variations that are exactly the inverse of the gain variations of the front-end charge amplifier. Figure 3.17 shows the detailed implementation of this second amplification stage that is realized as a voltage-controlled variable gain amplifier (VCG).

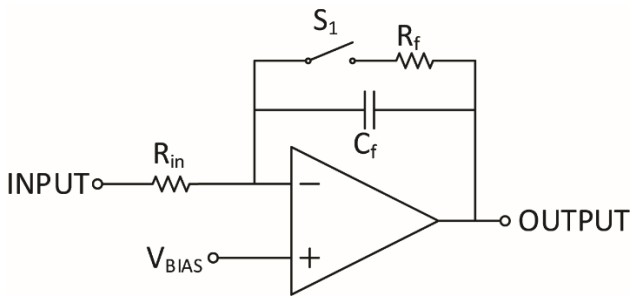


Figure 3.17: PWM-controlled variable gain amplifier.

As shown, the feedback path is formed by a resistor in series with a switch S_R. In [37] shown that equivalent resistor of switched resistor is equal to $\frac{R}{D}$,where D is the duty cycle

of the control pulse of the switch. In addition, the gain of this structure is ratio of feedback resistor to the input resistor $\frac{R_f}{D.R_{in}}$. Therefore, if we control the gain of VCG with the output signal of the PWM block, it will be equal to $\frac{C_f.R_f}{C_{INTERFACE}.R_{In}}$. Multiplying this gain expression by the first stage gain ($\frac{C_{INTERFACE}}{C_f}$) results in an overall channel gain expression equal to $\frac{R_f}{R_{in}}$, which is independent of the absolute value or variations of the interface capacitance, $C_{INTERFACE}$.

Additionally, to avoid saturating the OpAmp while the clocked-resistor's switch is open, a capacitor C_{fh} is paralleled with the switched resistor. The high cut off frequency of this structure is equal to $\frac{D}{2\pi R_f C_{fh}}$. Accordingly, the C_{fh} is chosen in a way that for D > 0.01 the cut-off frequency of the VCG is greater than the signal frequency bandwidth in order to prevent any attenuation of the neural signal. Figure 3.18 validates the functionality of the Voltage control gain block. In this setup, the input signal (blue waveform) is a sinusoidal waveform, modulated with a known signal (purple waveform) which is also fed to the PWM block. The VCG output (yellow waveform), controlled by the output of the PWM block, extract the clean sinusoidal input.

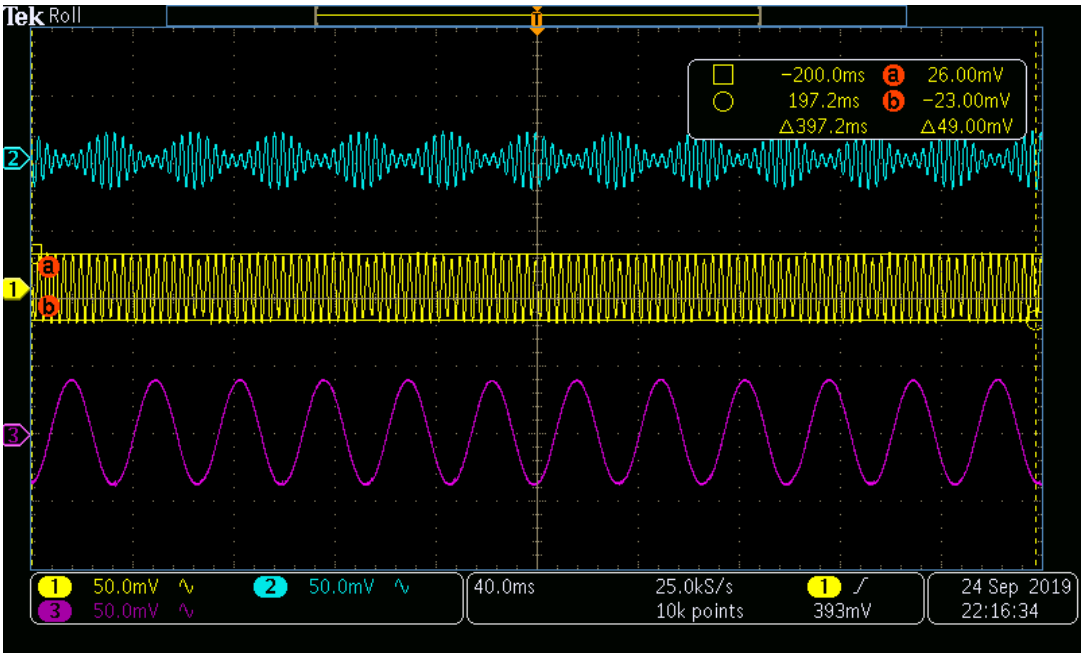


Figure 3.18: Measurement result validating the functionality of the PWM and VCG.

Figure 3.19 shows the power spectral density of modulated and cleaned signal, which confirms that the PWM-controlled variable gain amplifier can remove the extra tones resulted from motion. The signal that we fed to this block is a sinusoidal wave with frequency of 300 Hz (representing the input signal) which is modulated by another sinusoidal wave with frequency of 20 Hz (representing the motion artifact signal). The FFT plot of the input signal illustrate a tone at frequency of 300 Hz and two other tones at frequencies 280 Hz and 320 Hz, which are basically $f_{Input}+f_{Motion}$ and $f_{Input}-f_{Motion}$. The FFT plot of the output signal illustrates that the two extra tones are removed, which means we have extracted the input signal and removed the effect of motion artifact and power of the extra tones representing the motion-induced artifacts has been reduced by 41.5dB.

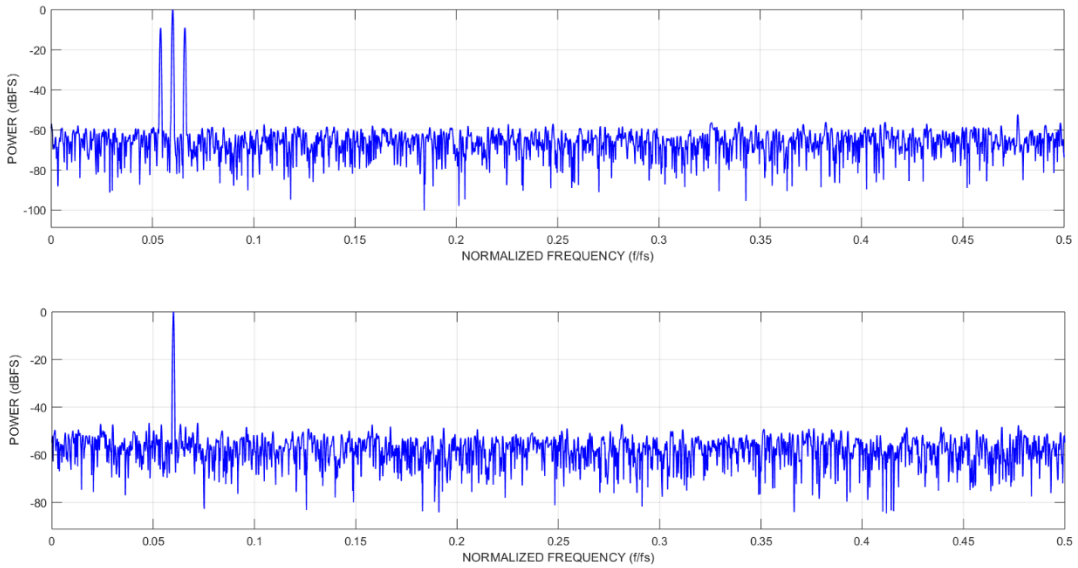


Figure 3.19: Power spectral density of (up) input and (down) output of the PWM-controlled variable gain amplifier.

3.4.3 Two-stage band-pass filter

The described switching job in the VCG block causes undesired interference with frequencies higher than the signal bandwidth. Therefore, a two-stage band-pass filter as it is shown in Figure 3.20 is included in the channel design. Figure 3.21 shows the schematic of the fully differential OTA and the common mode feedback (CMFB) circuitry used in both stages of the band-pass filter. Table 3.2 Reports the sizing information for the transistors in the fully differential amplifier and the CMFB circuitry. Simulation results showing the frequency response of the two-stage for this two-stage band-pass filter is shown in Figure 3.22.

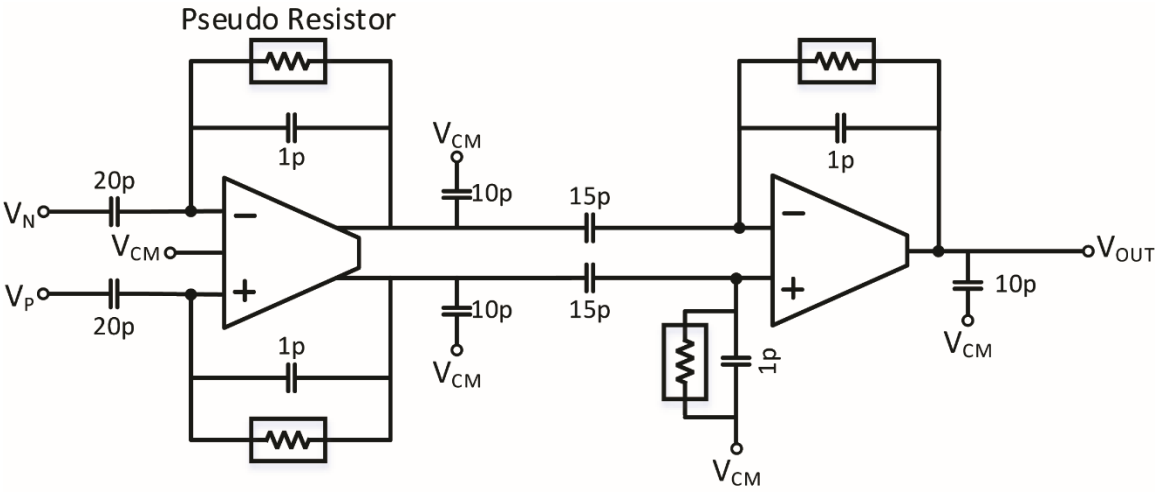


Figure 3.20: Two-stage band-pass filter used as the third and fourth stages of the presented channel architecture.

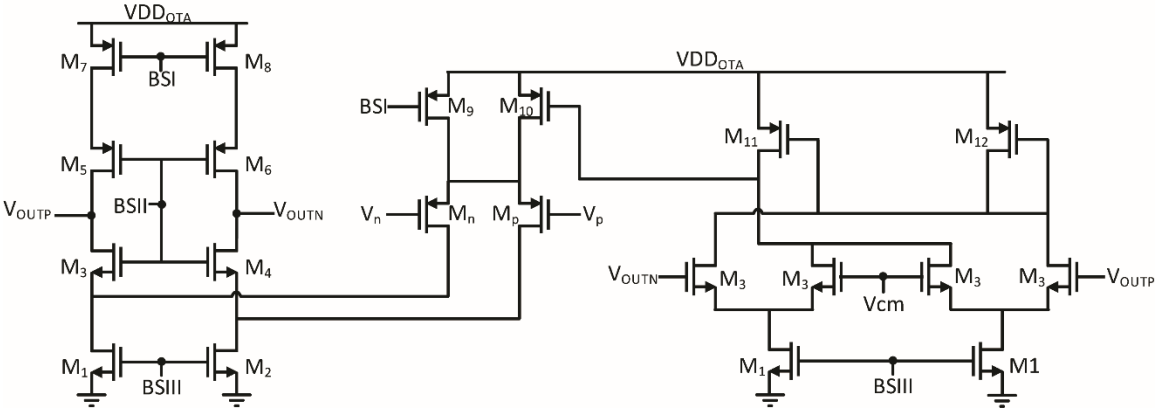


Figure 3.21: fully differential OTA and the common mode feedback circuitry used in both stages of the band-pass filter.

Table 3.2: Sizing of the transistors in the fully diffrential OTA.

Transistor	M_n	M_p	M_1	M_2	M_3	M_4	M_5
W/L	$\frac{4.2\mu}{900n}$	$\frac{4.2\mu}{900n}$	$\frac{1.8\mu}{900n}$	$\frac{1.8\mu}{900n}$	$\frac{1.8\mu}{900n}$	$\frac{1.8\mu}{900n}$	$\frac{4\mu}{900n}$

Transistor	M_6	M_7	M_8	M_9	M_{10}	M_{11}	M_{12}
W/L	$\frac{4\mu}{900n}$	$\frac{2.4\mu}{900n}$	$\frac{2.4\mu}{900n}$	$\frac{2.4\mu}{900n}$	$\frac{2.4\mu}{900n}$	$\frac{4.8\mu}{900n}$	$\frac{4.8\mu}{900n}$

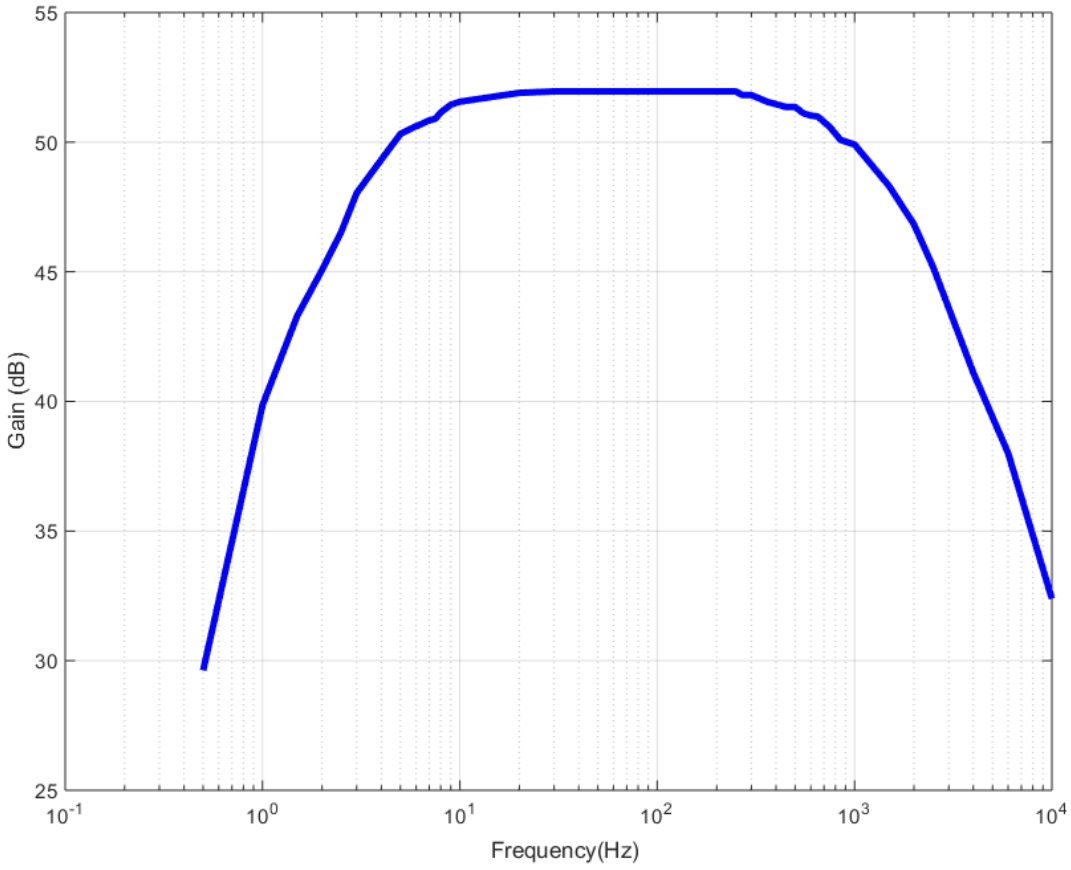


Figure 3.22: Experimentally measured frequency response of two-stage the low-pass filter.

3.5 Microchip Fabrication and Characterization

Figure 3.25 shows the full 4-stage schematic of the presented channel architecture. An 8-channel version of the presented EEG recording circuit was designed and fabricated using TSMC 130nm technology. The micrograph of the 3×4 mm^2 integrated circuit is shown in

Figure 3.23. Each recording channel is highlighted and the channel dimensions are annotated. Finally, Table 3.3 summarizes the overall specification of EEG recording SoC and Figure 3.24 illustrate the power and area breakdown of the EEG recording front-end.

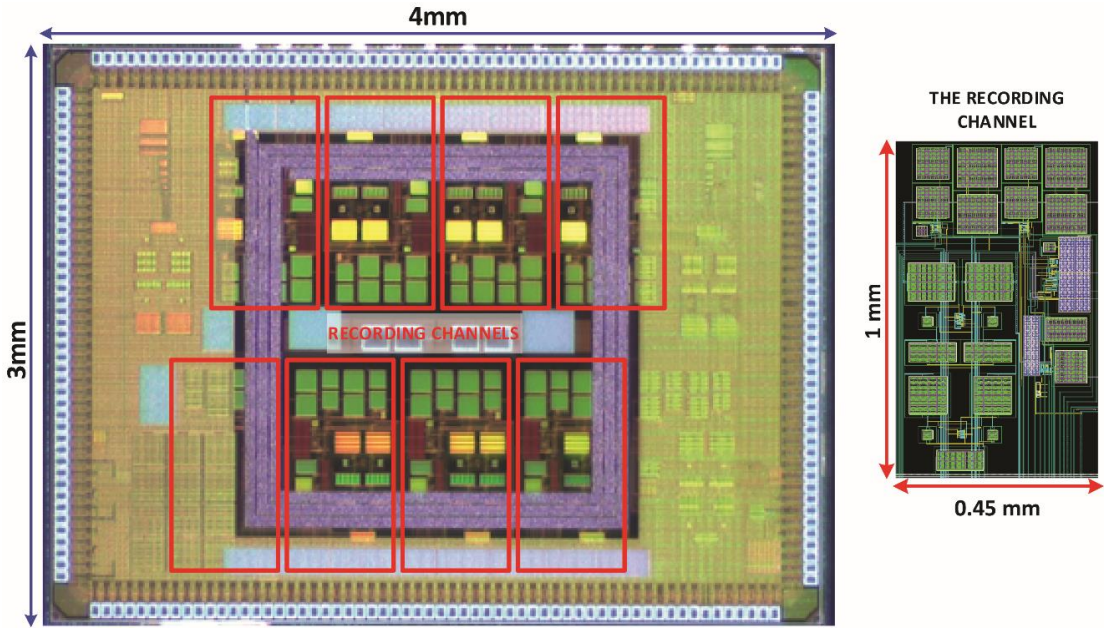


Figure 3.23: The chip micro-graph showing the placement of the eight recording channels and their dimensions.

Table 3.3: EEG recording SoC specification summary

Technology	130 nm	Gain	68.5dB
Supply	1.2 V	Bandwidth	3Hz-1kHz
Area	12 mm^2	Power/channel	55µW
# of channels	8	Area/channel	0.45mm^2
		Input referred noise	12.3 µVrms

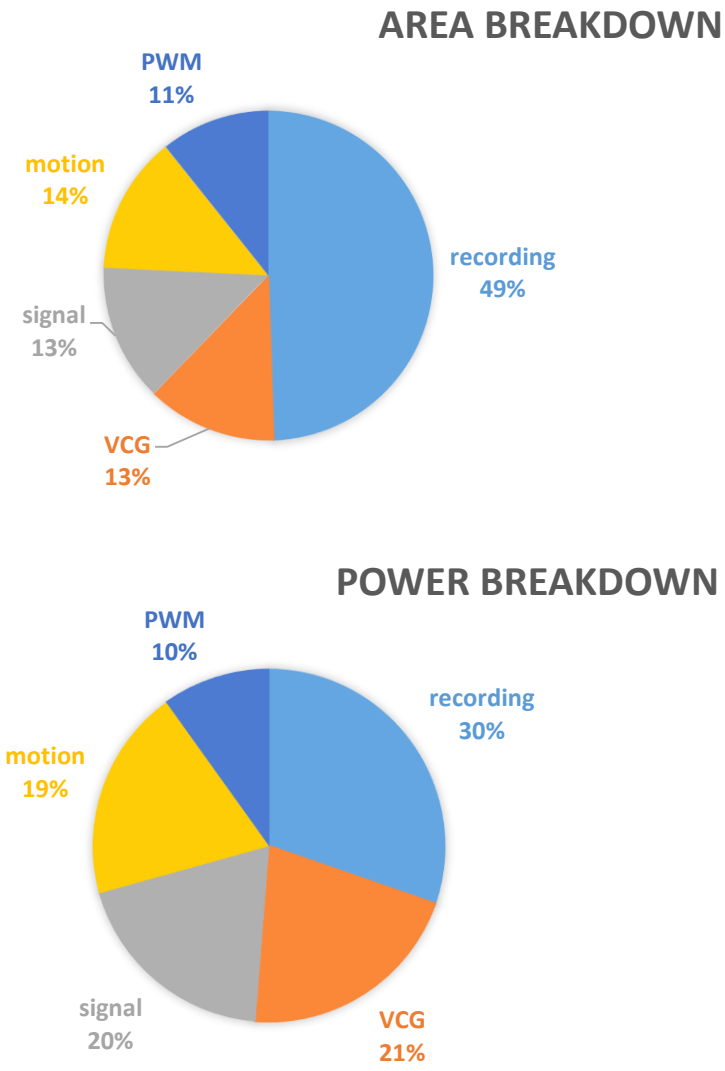


Figure 3.24: Area and power breakdown for the EEG recording front-end.

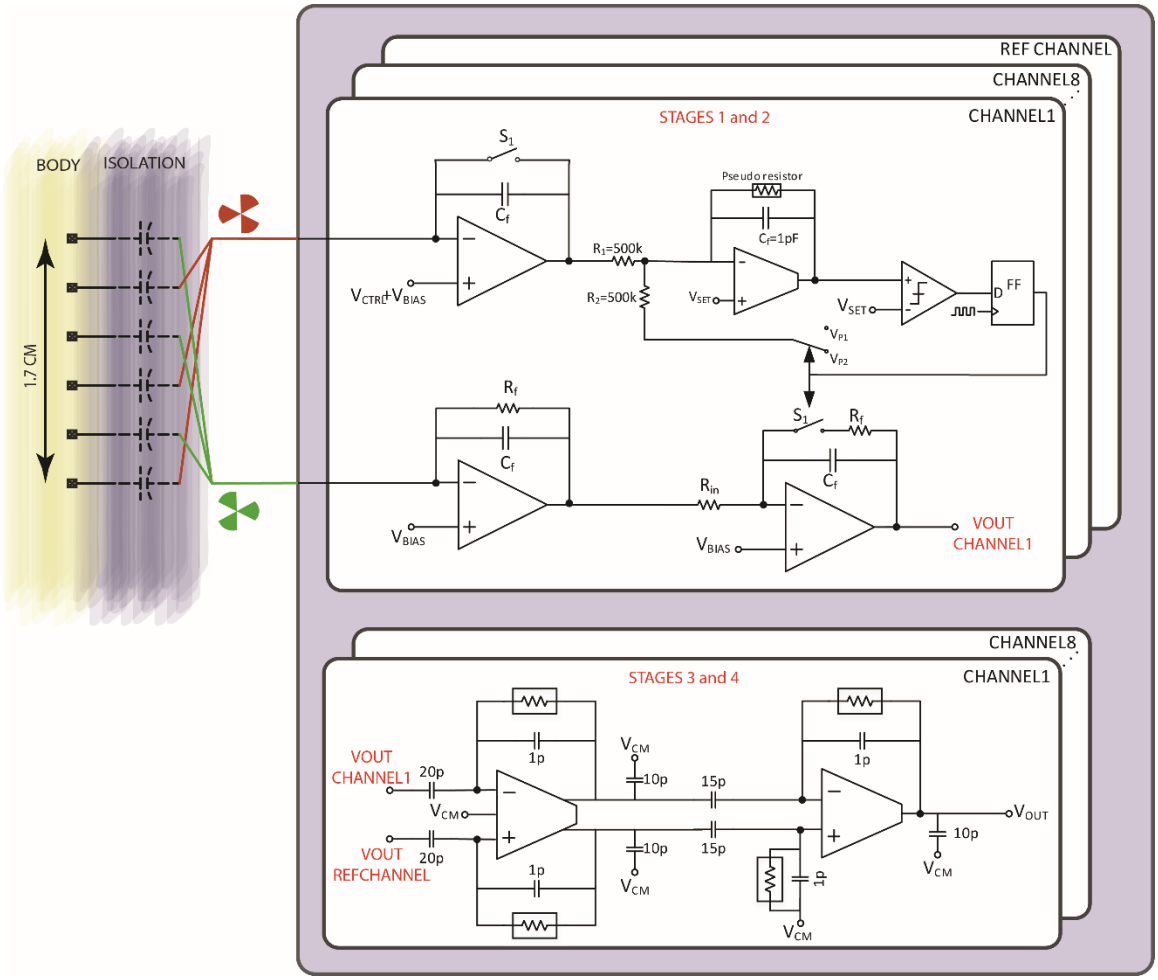


Figure 3.25: Block diagram of the 8-channel EEG recording SoC and the 4-stage circuit implementation of the proposed channel architecture.

3.6 Measurement setup

Figure 3.26 illustrate a 6-layer PCB board that has been design for characterizing the presented SoC. The board is designed using Altium Designer software. An FPGA (544-2464-ND, Altera CycloneIII) has been implemented on the chip to provide the required clock signals. The FPGA also allows further digital signal processing to implement feature extraction algorithms.

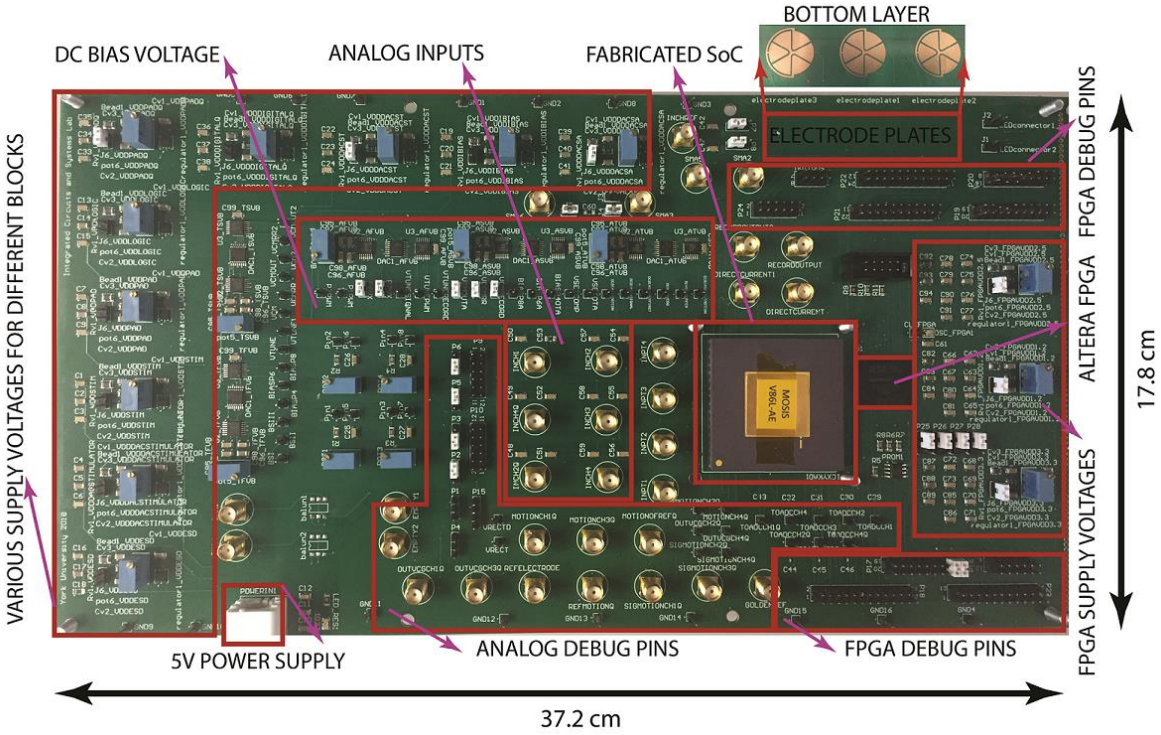


Figure 3.26: The PCB designed for characterizing the presented SoC.

Chapter 4

Discrete implementation

In this chapter, we present a fully-flexible wearable integrated system for ambulatory EEG recording with 8 actively-shielded recording channels, a low-power digital signal processing backend, and a BLE 5.0 transceiver for wireless communications. The system is planned to be a platform that hosts 8 of the ICs presented in Chapter 3. However, as an intermediate step, we first used off-the-shelf components to implement the exact channel architecture presented in Chapter 3, to form an early prototype that helps us validate system-level functionality of the wearable device. The discrete implementation is basically a proof of concept for the system-level and application level properties of our system, for example common-mode signal calculation, connection to the digital back-end board and wireless data transmission and we also wanted to make sure about the functionality of the flexible PCB substrate for the electrodes as well as the circuit connections . However, in the discrete implementation we are limited in terms of IC selection, which means we are

not able to have a customized design with smallest possible power and area consumption and an optimal noise performance, while an ASIC design would offer superior performance in terms of power consumption, noise level and switching performance.

Toward this goal, we developed a 9.2-gram fully-flexible wearable device that is capable of recording EEG signals from 8 channels in a differential manner, each equipped with an active electrode (amplifier + ADC), active shielding, and analog motion artifact detection and removal. The device uses non-contact dry electrodes for recording that are integrated together with the electronics on the same flexible substrate. A 1.18-gram $17\times13mm^2$ rigid digital backend board hosting a low-power FPGA connects to the main flexible substrate and adds signal processing capability to the device, making it a diagnostic tool as well. The digital backend board also hosts a low-energy Bluetooth 5.0 transmitter that communicates the digitized EEG recordings at up to two Mbps rate.

4.1 Design and implementation

4.1.1 Top-level architecture

Figure 4.1 shows a picture of the presented work on a head mannequin with pointers to the major blocks discussed in Figure 1.1. The picture illustrates the minimal form factor and adjustability to scalp shape.

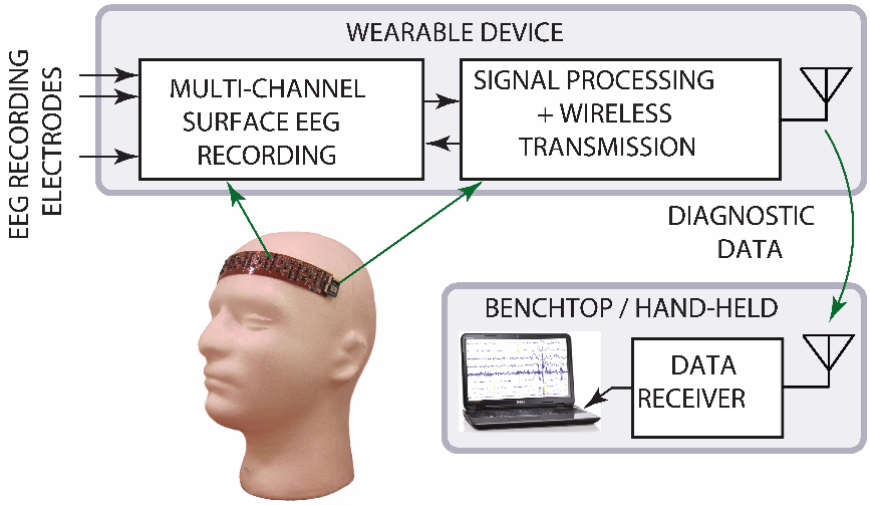


Figure 4.1: Block diagram of the wireless wearable EEG monitoring device with a picture of the presented work mounted on a head mannequin.

Figure 4.2 (a) shows the top-level block diagram of the presented system, as well as an actual picture of the complete wearable device and how different parts of it are connected to each other. As shown, the system is comprised of three main modules namely, the flexible recording board, the digital/wireless back-end board, and the battery. The front-end board is implemented using a 4-layer flexible polyimide printed circuit board (PCB). The board length is 204 mm, which is long enough to cover the frontal and front-temporal lobes of an adult scalp, and its width is 23.6mm, making it easily fitted into a typical fabric headband. The physical flexibility of the substrate (demonstrated in Figure 4.2(b)) allows for the device to perfectly take the shape of the patient scalp, making it patient- and age-universal (i.e., usable for infants, children, and adults).

Figure 4.2 (a) also shows a simplified top-level block diagram of the device. The flexible board hosts nine (8 recording plus 1 reference in the middle) channels. The channels are

implemented using off-the-shelf components that are populated on the top layer of the board. The bottom layer of the board is used to implement the dry EEG recording electrodes, which not only reduces the overall weight of the device but also makes the system self-contained and needless of wires connecting the electronic and the electrodes. More importantly, having the electrodes physically placed right under the front-end recording amplifiers (and on the same substrate) means that they could be connected through a via hole. This forms a perfect active electrode where almost no interference is

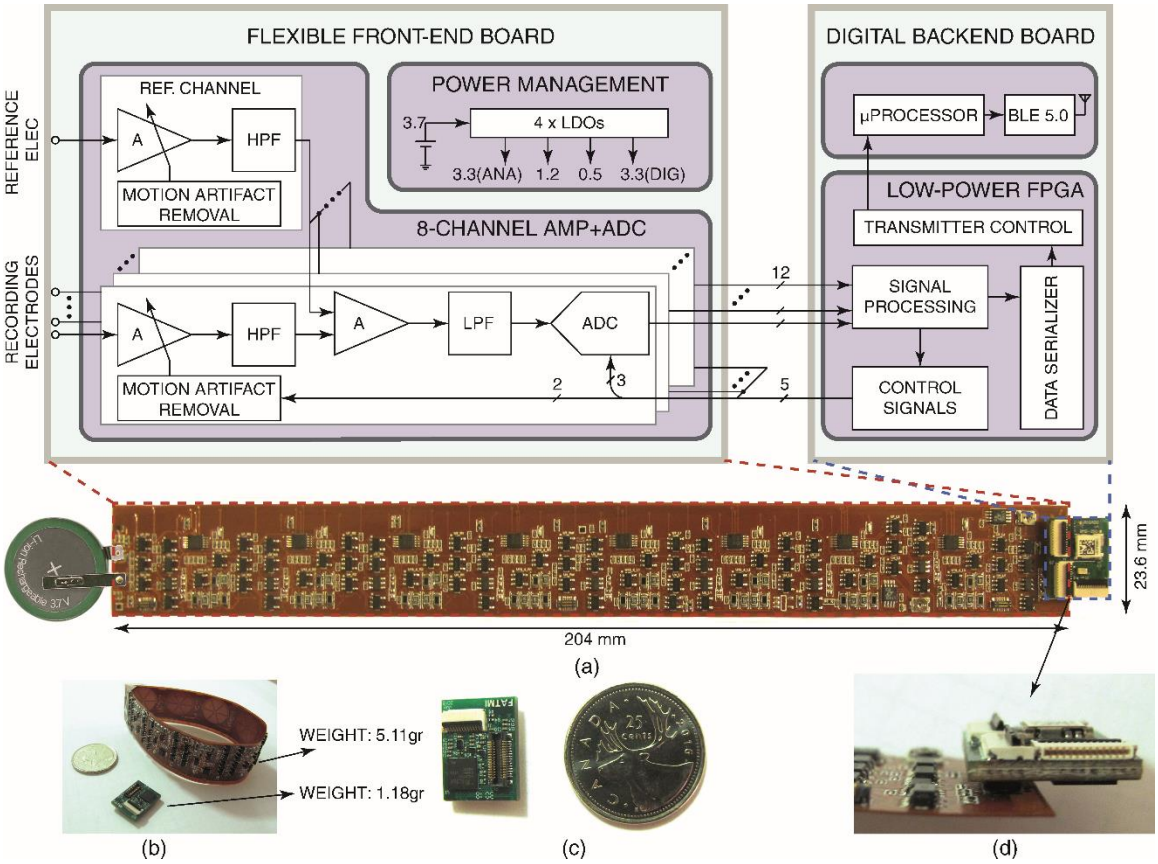


Figure 4.2 : (a) Top-level block diagram and pictures of the presented system showing its (b) weight and flexibility, (c) size relative to a 25-cent coin, and (d) mechanical/electrical connection of the front-end and backend boards.

coupled onto the EEG signal before amplification. Additionally, to avoid bio-compatibility issues associated with certain metallic electrodes, the electrodes are covered with a non-conductive material and the front-end is designed for non-contact recording based on the considerations described in [38].

Figure 4.2 (a) also depicts the block diagram of the circuit implemented on both boards. As shown, each channel contains multiple amplification and filtering stages and has dedicated modules for quantization and motion artifact removal. To compensate/remove the large motion-induced artifacts that appear on the recorded EEG due to the use of dry electrodes, we have employed a novel recording front-end architecture that (a) makes the signal's voltage gain directly proportional to the motion-induced skin-electrode interface capacitance variations, (b) intentionally adds difference between two parallel near-identical paths to separate the signal from the motion, and (c) uses the extracted motion to compensate for the signal gain variations due to the physical motion. The above-mentioned design is implemented in each channel, including the reference channel, and the resulted artifact-free signals in each channel are subtracted from the clean (i.e., artifact free) reference signal to achieve a common-mode-free spatially-significant EEG recording.

Each channel also hosts a dedicated 12-bit ADC with a serial output. The outputs are sent to the FPGA in the backend board through the vertical connectors. The top and bottom views of the backend board is shown in Figure 4.3. As shown, the board hosts a programmable FPGA, a Bluetooth low-energy (BLE) 5.0 transceiver module (microchip +

antenna), as well as various voltage regulators and crystal oscillators for DC bias voltage and clock frequency generation, respectively. The board also hosts various connectors for electrical/mechanical attachment to the flexible board; test/debugging purposes, and programming the FPGA.

The FPGA is used to collect and organize the data and send them to a microprocessor on a Bluetooth low-energy (BLE) transceiver module that allows for bidirectional communication with a desktop/handheld computer to send the recorded EEG signals and receive system reconfiguration commands. A control unit is also embedded into the FPGA that manages timing and mode-selection of the mixed-signal circuits on the main flexible board. This includes the reset and pulse-width modulation signal used for the motion artifact removal circuit (explained in section 3.4) as well as the timing signals for the ADCs operation.

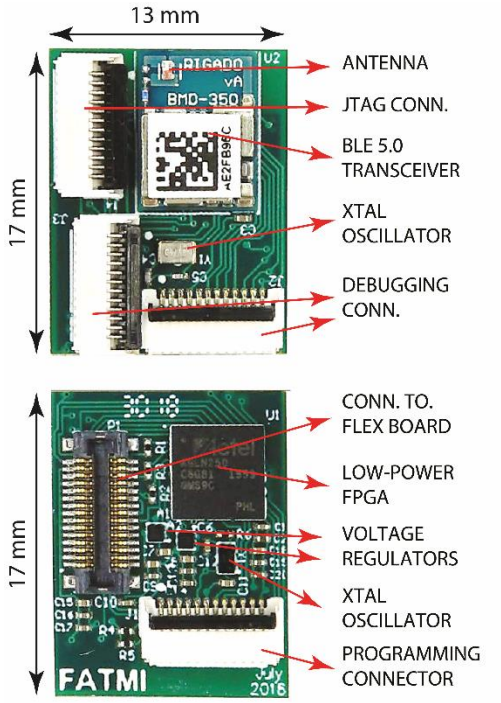


Figure 4.3 : Top and bottom view of the digital backend board.

Additionally, the FPGA is selected to have a reasonable number of logic elements (Microsemi Igloo Nano AGLN250) that allows for uploading an algorithm onto it for online processing of the EEG data for detection of a neurological event such as epilepsy seizures or sleep states [39],[40] and [41]. In fact, the main purpose of including an FPGA in this design is for diagnostic applications. Deterministic or data-driven algorithms for detection of various neurological events could be programmed on the FPGA, which results in a much smaller latency and better energy efficiency compared to the case where a power-hungry high-throughput transmitter is used to communicate raw EEG signals to a computer [16]. In [11] we have demonstrated successful implementation of a patient-specific epilepsy seizure detection algorithm in an energy efficient manner on this FPGA. Our

experimental results show a detection sensitivity and specificity of 92.5% and 80.1%, respectively, while consuming only 110µW.

To avoid the discrete electronic components at the top layer to induce noise on the recording electrodes at the bottom layer through capacitive coupling, an active shielding scheme is implemented using one of the middle layers. The low-impedance output of the recording amplifier which is a magnified replica of the recorded EEG signal is connected to a metal plate (same size and exactly on top of each electrode) implemented on the second-lowest layer of the flex PCB. The other internal later is used for routing and GND/VDD plane implementation. The flexible board weighs 5.11 grams.

A pair of vertical connectors (AXT420324 and AXT420124) shown in Figure 4.2(d) are used to connect the flexible board to the 17×13 mm^2 rigid backend mini-PCB. The vertical connectors between the two boards provide the means for (a) sending the serialized digital output of each channel to the backend digital board, (b) sending back the control and timing signals from the digital backend board to the quantization and motion artifact removal modules in each channel of the front-end flex board, (c) sharing the ground, vdd, and biasing voltages between the two boards, and (d) realizing a robust, yet miniature mechanical connection between the two boards. Table lists the major discrete components used in the making of the presented wearable device.

Table 4.1 : List of the major off-the shelf components used.

Component	*Company*	*Model*
Switch	Analog device Inc	ADG701LBRJZ
PWM	Linear Technology	LTC6992CS6-2xTRMPBF
Op Amp	Texas Instruments	OPA333AIDCKR
Op Amp	Texas Instruments	OPA378AIDCKR
Op Amp	Texas Instruments	OPA314AIDCKR
ADC	Texas Instruments	ADS1018IDGSR
Regulator-3.3	Analog device Inc	ADP121-ACBZ33R7
Regulator-1.2	Analog device Inc	ADP121-ACBZ12R7
Adj. regulator	Linear Technology	LT3020EMS8xPBF
BLE Tx	Rigado Inc	BMD-350-A-R
FPGA	Microsemi	AGLN250V2-CSG81
XTAL 32kHZ	ECS Inc	ECS-.327-6-12-C-TR
Oscillator 4MHz	SiTime	SIT8021AI-J4-XXS-4.0E
Vertical Connector	Panasonic	AXT430124
Vertical Connector	Panasonic	AXT430324
FFC Connector	Molex	5034801200

4.2 Circuit implementation

Detailed schematic of the circuit implemented on the flexible front-end board is depicted in Figure 4.4. As shown, each recording channel has two parallel path for sensing the surface EEG signals -- the "signal" path -- and for sensing the capacitance variations induced by a physical motion -- the "motion" path. Sensing amplifiers on both paths are

connected to two identical sections of an inter-digitated pie-shape electrode. The electrode is implemented using the bottom layer of the flexible PCB and is covered with a 0.9mil-thick liquid epoxy insulator to realize a non-contact interface. The inter-digitated design will make sure that both half electrodes will experience identical skin-electrode interface capacitance value as well as motion-induced capacitance variation.

The sensing front-end amplifiers design is a variation of a capacitive-feedback amplifier shown in Figure 2.12, where the input capacitance C1 is replaced with the electrode-skin interface capacitance (C_{ESI}). Both motion and signal paths are designed to have a direct control on the DC voltage at the input using OpAmps. For the motion path, an intentional large DC difference is applied across the C_{ESI}, causing the second term of Equation (2.3) to dominate the current flowing into this path. Periodic application of the DC voltage across C_{ESI} while the 100pF feedback capacitor is being reset at the same frequency results in the output of this stage (V_{motion}) to have a linear relationship with the absolute value of the interface capacitance.

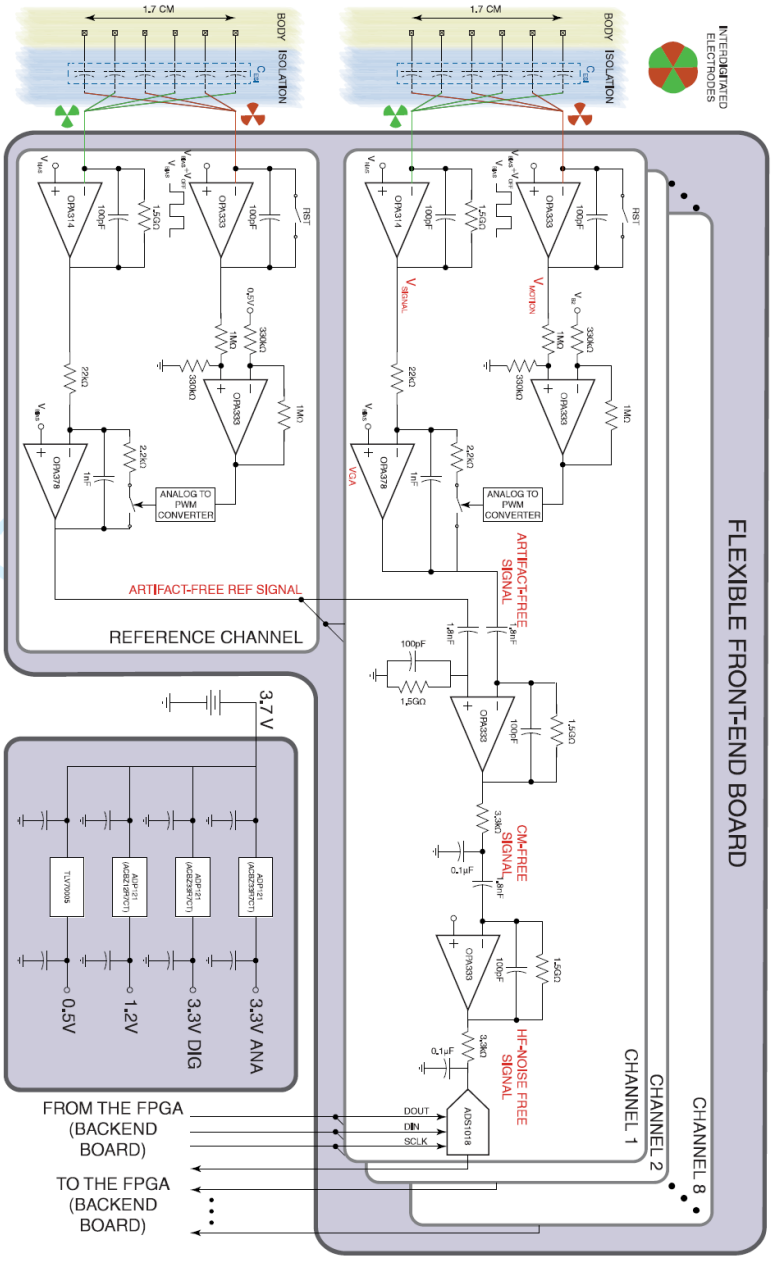


Figure 4.4 : Detailed circuit schematic of the active electrode used for EEG recording (amplification and quantization), the motion artifact detection and removal, and the interdigitated electrode design used for non-contact interfacing with the skin.

The circuit used in the signal path conducts somewhat the opposite of the motion path in the sense that it is designed to ensure that the current flowing into the sensing path is dominated by the first term of Equation (2.3) by enforcing the DC voltage across the C_{ESI} to zero. This way, the signal path first amplifying stage has a gain that is directly proportional to the interface capacitance value.

In the second stage of the motion path, V_{motion}, after being level shifted is fed to a voltage-controlled pulse-width modulator IC that sets the gain of a variable gain amplifier (VGA) stage using a duty-cycled resistor. By doing this, the motion-induced interface capacitance variations are sensed and inversely multiplied by the gain of the signal path. Therefore, after two stages of amplification, the overall gain of the signal path will be independent of the interface capacitance variations.

The performance of the circuit described above is heavily dependent of the symmetry of the two paths to ensure the same interface capacitance variations for them. We experimentally measured the output of the two paths to evaluate the symmetry of our design. Figure 4.5 shows the capacitance values sensed by two parallel paths. While the results are more than satisfactory for our application, the errors could be made even smaller by increasing the number of inter-digitated sections of the electrodes.

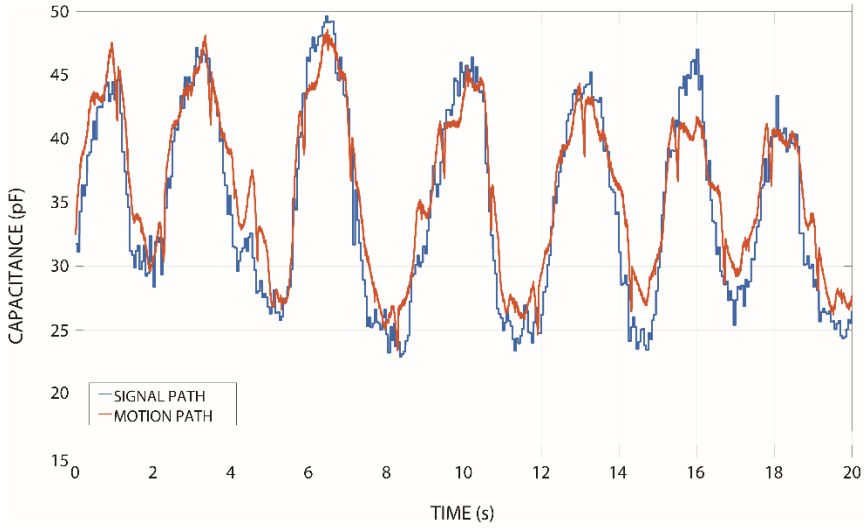


Figure 4.5 : Experimentally measured variable skin-electrode interface capacitance from two parallel paths of the presented active electrode.

The circuit described above is used for all the 8 recording channels as well as the reference channel. As shown in Figure 4.4, the artifact-free signal in each channel is subtracted from the artifact-free signal from the reference channel, essentially removing the common-mode component of the signal. The common-mode free output of this stage is low-pass filtered to remove the high-frequency noise coupled onto the signal, mainly due to the pulse-width modulation circuit. The analog output is then fed to a 12-bit ADC that is integrated in each channel/active electrode.

Figure 4.6 shows the magnified picture of top and bottom views of one of the active electrodes implemented on the flexible PCB with all the discrete components used. As shown the circular electrode implemented on the bottom layer of the PCB has 6 interdigitated sections, each of them shorted to two non-neighbour sections, constituting

two interdigitated electrodes. The presented design guarantees that the signals recorded by each of the parallel paths will record identical EEG signals and will experience identical motions, hence, exactly the same impedance variations.

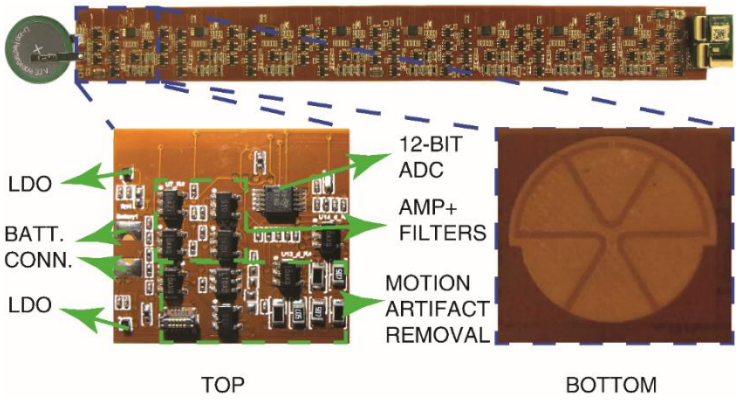


Figure 4.6 : Top and bottom view of one of the recording channels and the electrode implemented on the flex substrate.

4.3 Measurement results

The performance of different components of the system were validated experimentally in the lab. Figure 4.7(a) shows the measured voltage gain of the recording channel versus frequency confirming the full 300-Hz bandwidth of the circuit required for local field potential recording. Signals were fed to the device through an aluminium conductive plate that was separated from the electrodes by an insulating layer (both air and fabric were used). Figure 4.7(b) shows the input-referred noise of the recording front-end, which is well below the required level for LFP recording. Figure 4.7(c) shows the measured CMRR of >70dB confirming excellent rejection of common-mode input signals and interference. The BLE 5.0 digital transceiver was also tested showing error-free transmission throughput

of 1Mbps for up to 5m distance. The power consumption of each recording channel and the entire digital backend are measured to be 1.5mW and 14mW, respectively, and the whole device with a coin battery weighs 9.2 grams.

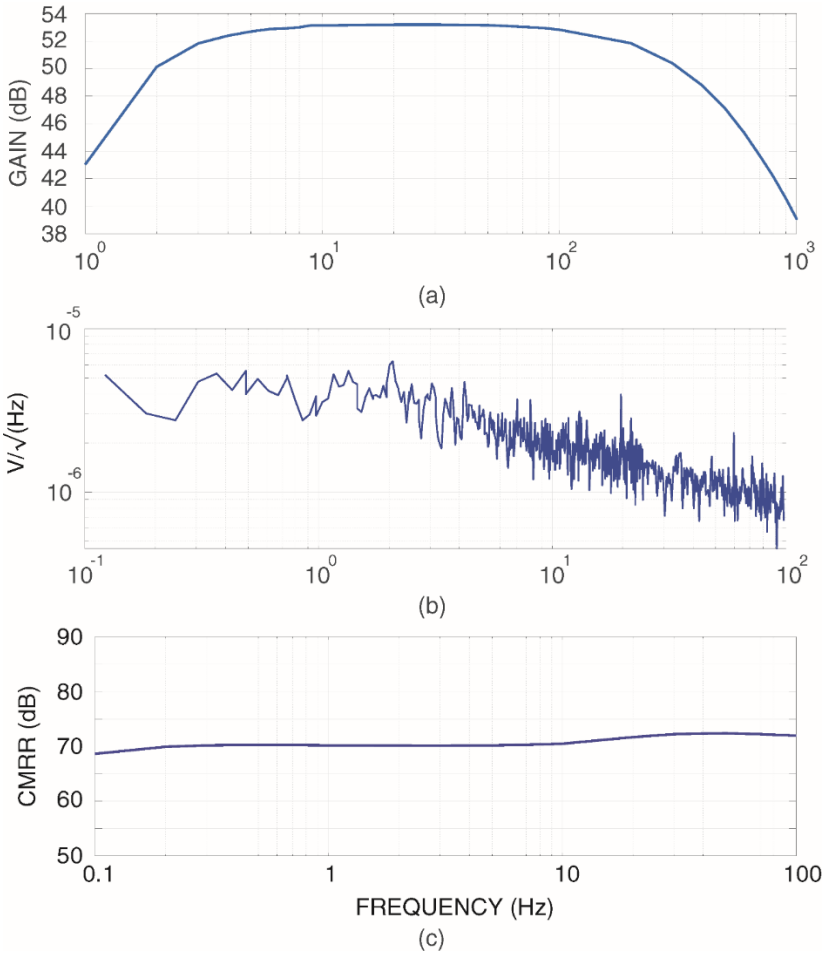


Figure 4.7 : Recording channel experimental measurement results: (a) gain bandwidth, (b) input-referred noise, and (c) CMRR.

Figure 4.8 (a) and (b) show sample recorded signals at the output of the first and second (i.e., motion artifact compensated) amplification stage in the "signal" path, respectively. The experiment is done by applying a sinusoidal signal into the living tissue

and recording the incident waves using the non-contact active electrodes described above, a few centimeters away. While recording for tens of seconds, various horizontal and vertical motions that could happen due to the patient's normal activities (e.g., speaking, frowning, breathing, talking, chewing) were applied to the electrode.

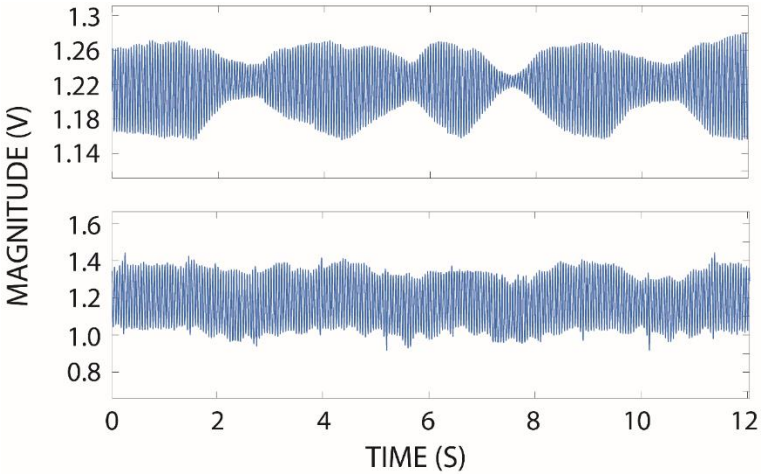


Figure 4.8 : Sample recordings of the presented circuit before and after analog motion artifact removal.

Figure 4.8(a) shows that while motions can generate large variations in the recorded signal, due to the use of presented novel recording architectures, the artifacts are manifested in the form of voltage gain variations rather than large DC drifts that have been observed using conventional recording circuits (Figure 2.6 (a), (b), [30] and [42]). Figure 4.8(b) shows the artifact-compensated signal at the output of the second stage of amplification. As shown, large voltage gain variations are compensated and the recorded signal is fairly artifact free.

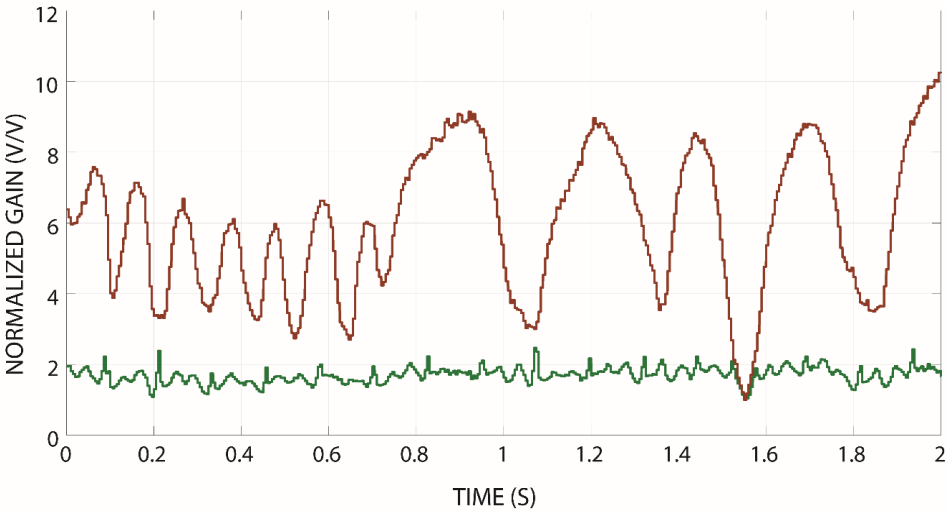


Figure 4.9 : Normalized voltage gain of the recording circuit with and without motion artifact removal (MAR).

Figure 4.9 presents the normalized voltage gain of the presented circuit for the first and second stages of amplification. The figure clearly illustrates the effectiveness of the presented analog motion artifact removal (MAR) in yielding a relatively constant gain for the EEG-recording active electrodes. Table 4.2 compares the presented work with the state of the art active electrodes in terms of system-level and circuit-level attributes.

Table 4.2 : State-of-the-art active electrodes designed for ambulatory surface EEG/ECG recording.

	[5]	*[1]*	*[2]*	*[3]*	*[4]*	*This work*
Motion detection	No	No	Yes	No	Yes	Yes
Method	-	-	Current	-	Current	Parallel
	-	-	injection	-	injection	recording
ETI Frequency	-	-	1KHz	-	1KHz	Same as EEG
Motion removal	No	No	Digital	No	Digital	Analog
Active shielding	Yes	-	-	No	-	Yes
No. of wires	-	4	6	4	5	4
Interface	Non-contact	contact	contact	contact	contact	Non-contact
VDD (V)	3.3	1.8	1.8	3	1.8	3.3
Power/ch (W)	600 µ	20 µ (Amp only)	82µ	360 µ (Amp only)	105 µ	1.3m
Channel Count	-	8	8	-	16	8
Voltage Gain (V/V)	1000	3,10,100	11,51,101	10	140,700,1200	260
Input Impedance (Ω)	-	100M	500M	100M	100M	Charge Amp
Bandwidth (Hz)	100	-	200	-	300	300
ADC	Yes	No	Yes	No	Yes	Yes
Resolution (bits)	16	-	12	-	12	12
Offset tolerance (mV)	R-to-R	R-to-R	- +250mV	-	-+350mV	R-to-R

*: No real wire as all the channels are on the same substrate.

R-to-R: Rail to Rail

Chapter 5
Conclusion and future works

5.1 Conclusion

Design, development, and experimental validation of integrated circuits and systems for ambulatory EEG monitoring and neurological disorder diagnostics were presented. A conclusive review and experimental analysis of the effect of physical motions on the signal quality acquired by various EEG electrodes were conducted prior to the design and development stage. Based on the review's outcome, a novel circuit architecture that employs inter-digitated dry non-contact electrodes together with mixed-signal circuit techniques for detection and removal of motion artifacts was designed and incorporated into both prototypes presented in this thesis.

The first prototype which is an integrated circuit designed and fabricated in a 130nm standard CMOS technology is an EEG recording system on a chip that integrates 8 channels, each equipped with the above-mentioned architecture capable of motion artifacts detection and removal. The IC was tested in the lab and the measurement results show an average voltage gain of 70 dB, power consumption of 55 μW per channel, integrated input referred noise of 10 μVrms (integrated over 1-200 Hz) and 3-dB frequency bandwidth of 3-1000 Hz. The IC's performance was also evaluated with motion-contaminated input signals and the measurement results were presented

The second prototype is a fully-flexible wearable EEG monitoring and diagnostic device. The system integrates 8 active-electrode recording and one reference channels, each equipped with the motion artifact detection and removal module described above, a dedicated ADC, and active shielding. The flexible substrate allows for the device to be indifferent to scalp shape and patient's age, making it a suitable solution for ambulatory EEG monitoring and analysis. Dry non-contact inter-digitated electrodes are also integrated on the main flexible substrate, allowing for quick setup time, comfortable use, and avoiding bio-compatibility issues. The system top-level architecture and circuit implementation were described in details. The device was validated experimentally and measurement results were presented.

5.2 Future directions

To validate the functionality of the presented novel architecture for the analog front-end at the system level, the chip presented in Chapter 3, should replace the off-the shelf components of the EEG recording headband. Using the integrated system instead of the discrete components will improve performance in terms of noise and power consumption. Also it will decrease the number of components and connection on the substrate, hence improving the physical features such as size, weight, and flexibility.

A natural next step for either prototypes presented in this thesis is clinical validation. Recording forehead EEG signals in a clinical setup will be the ultimate confirmation of the presented system's efficacy in ambulatory EEG monitoring.

Another direction would be investigating the efficacy of the presented systems as a diagnostic medical device. Our group has implemented a machine learning algorithm for patient-specific epilepsy seizure detection on the digital backend signal processing PCB presented in Chapter 4 of this thesis [11]. The algorithm uses only frontal-lobe EEG signals that the presented system in Chapter 4 is capable of recording. An experimental test showing both recording and signal processing done by the integrated system presented in this thesis will prove its diagnostic capabilities.

The proposed method can extract motion independently could be used for application that needs motion recording.

For the next generations of the ambulatory monitoring and diagnostic system, the prototype could be designed to be able to record signals from all over the scalp, instead of only from forehead. To improve detection accuracy and/or enable new applications, the next-generation device could also be turned into a multi-modal technology by integrating techniques such as functional near-infrared spectroscopy into it.

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