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Adoption of 2T2C ferroelectric memory cells for logic operation

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***Abstract*—A 2T2C ferroelectric memory cell consisting of a select transistor, a read transistor and two ferroelectric capacitors that can be operated either in FeRAM mode or in memristive ferroelectric tunnel junction mode is proposed. The two memory devices can be programmed individually. By performing a combined readout operation, the two stored bits of the memory cells can be combined to perform in-memory logic operation. Moreover, additional input logic signals that are applied as external readout voltage pulses can be used to perform logic operation together with the stored logic states of the ferroelectric capacitors. Electrical characterization results of the logic-in-memory (LiM) functionality is presented.**

Keywords—ferroelectrics, memristor, logic-in-memory, compute-in-memory, FeCAP, FTJ, FeRAM

I. INTRODUCTION

The discovery of ferroelectricity in HfO_2 films has led to an increased interest in ferroelectric memory devices, thanks to its unique properties as compared to classical ferroelectric materials (such as PZT). One of the biggest benefits of HfO_2 is its CMOS compatibility, which allows for easy integration with existing processes. For example, it was possible to implement the ferroelectric field-effect transistor (FeFET) using standard high-k metal gate (HKMG) technology [1]. These developments paved the way towards novel devices that would be able to overcome some of the limitations of existing memory technologies. Non-volatility and relatively high speed of ferroelectric memories makes them potential candidates for storage class memory (SCM) application. In addition, they are viewed as a platform for realization of logic-in-memory concepts. This is particularly important since the problem of the von-Neumann bottleneck is becoming the limiting factor in the performance of current electronic devices. It affects data throughput and increases power consumption. One way to overcome this issue is to perform logic operations directly in the memory device itself, thus eliminating the need for data transfer between logic and memory units. Several implementations adopting different memory devices were proposed, including FeFETs [2][3], ferroelectric capacitors (FeCAPs) [4] or magnetic tunnel junctions [5] etc. In this paper a 2T2C memory cell with HfO_2-based ferroelectric capacitors is demonstrated which is capable of performing logic operations between internally stored bits as well as with external voltage input. The main advantage of the proposed concept compared to other technologies is its potential for ultra-low power consumption and the adoption of small-scaled planar ferroelectric capacitors, eliminating the need for expensive 3D integration.

II. FERROELECTRIC CAPACITOR BASED MEMORIES

A. Ferroelectric random-access memory (FeRAM)

One of the earliest implementations of ferroelectric memories is the ferroelectric capacitor. It consists of a ferroelectric film sandwiched between two electrodes. Information is stored as a polarization direction of the ferroelectric layer. In order to write a bit, a voltage pulse is applied to the electrodes, such that the electric field inside the ferroelectric layer is larger than the coercive field. In this way the polarization can be set into one of the two states, thus writing either "0" or "1" into the cell. The read operation is performed by applying a switching pulse across the capacitor and sensing the displacement current which is dependent on the polarization direction. In a ferroelectric random-access memory array, a large number of FeCAPs are connected to the bit line (BL) via individual select transistors, thus forming the memory cells (Fig. 1a). The ferroelectric switching current charges up the bit line, which will be then sensed by a voltage sense amplifier. This means that the switched charge must be large enough in order to yield a sufficient voltage signal at the BL, thus posing a challenge for scaling down the size of the FeCAP.

B. 2T1C memory cell

In order to overcome scaling limitations of the FeRAM cell, it is possible to realize a gain cell by connecting one or more FeCAPs to the gate of an additional read-out transistor T3 (Fig. 1b) [6]. During readout the select transistor T1 will stay switched off, such that the effective capacitance that has to be charged by the polarization switching current will consist of only the small gate capacitance of the transistor T3 instead of the much larger bit line capacitance. Thus, the same amount of switched charge will result in a much larger voltage signal at the internal node n1 and consequently at the SL as compared to the conventional FeRAM. Several constraints have to be taken into account when designing such a cell. Firstly, in this cell the voltage across the FeCAP depends on the capacitive voltage divider ratio between the ferroelectric capacitor and gate capacitance of the read-out transistor T3. Thus, a suitable capacitance ratio has to be ensured that allows to switch the capacitor during readout while ensuring enough signal at n1 to be sensed at SL via the sense transistor T3. Second, the leakage currents through the ferroelectric capacitor and gate dielectric might shift the potential of the internal node, possibly leading to a loss of stored information. During write operation the select transistor T1 allows direct connection of the internal node n1 to the BL, such that the write signal can be applied to the FeCAP directly between BL and PL. This particular 2T1C cell can be operated in different regimes,

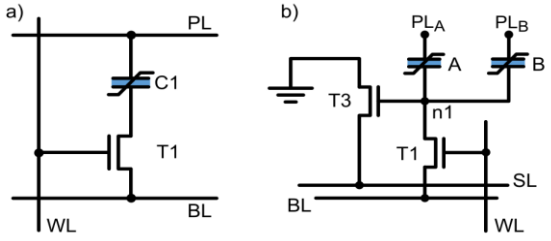

Fig. 1 Circuit diagram of a) FeRAM cell and b) 2T2C cell of this work.

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namely in a FeFET, FeRAM and a ferroelectric tunnel junction (FTJ) mode [6]. This work focuses on the FeCAP operation.

III. Experimental

A. Cell structure and device fabrication

The memory cell under investigation is based on the structure described in [6]. Here, the ferroelectric capacitor is realized adopting the gate capacitance of an integrated FeFET device. Source, drain and bulk contacts of each FeFET are connected together and the corresponding contact is referred to as a plate line (PL), while the gate electrode is connected to the internal node n1 in order to avoid undesirable influence by leakage currents originating from the S/D and bulk junctions. In most of the measurements, a 2T2C cell as shown in Fig. 1b was studied. However, the actual structure features four FeCAPs with their gate terminals connected to node n1. By grounding the plate lines of the other two FeCAPs of this 2T4C cell one can focus on the 2T2C part only. The logic-in-memory cells were fabricated using Globalfoundries' 28 nm HKMG FeFET process with 8 nm Si-doped HfO_2 as the ferroelectric and ~1 nm silicon oxide interfacial layer [7]. The size of the FeCAPs used here is W = L = 180 nm, while the read-out transistor T3 has dimensions W = 360 nm and L = 200 nm and select transistor T1 has W = 320 nm and L = 590 nm. The comparatively large size of select and readout transistors are given by the design rules for high voltage devices that are used in the test structures to ensure adequate reliability while operating the cells at voltages up to 4V that are mandatory to switch the polarization in the FeFET gate.

B. Electrical measurement setup

In order to set the polarization state of a FeCAP, a voltage of a given polarity has to be applied across the ferroelectric layer. This is done by applying a program pulse to the plate lines PL_A or PL_B voltage (V_{pr} = ± 4.0 V), while setting the bit line to ground and keeping the select transistor switched on through applying a positive voltage to the word line (WL). Positive plate line voltage corresponds to "0" and negative to "1". The read operation is schematically shown in Fig. 2. First the internal node n1 is pre-charged via the access transistor to V_{pc} = 0.4 V in order to reach the desired operating point of the read-out transistor T3 that determines the amount of current that can be sensed at the SL. Hereafter the select transistor is switched off via WL, such that the internal node n1 is floating. Then, a switching pulse with amplitude V_{switch} is applied to either plate line PL_A or PL_B. Depending on the stored

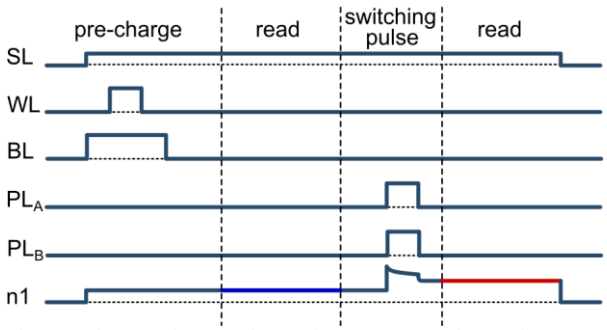

Fig. 2 Pulse waveform used to perform FeCAP read operation (not to scale)

polarization value of capacitor A or B, a charge corresponding to the induced polarization reversal will accumulate at node n1, thus raising the potential at the gate of read-out transistor T3. The signal is then read as an increase in drain current of the read-out transistor at the SL.

IV. Performing Logic-in-Memory Operations

A. Logic operation between 2 bits in 2T2C cell

The two FeCAPs can be addressed individually by applying write pulses to the corresponding plate lines PL_A or PL_B. This allows to set the stored bits independently and perform logic operations between them during a collective read operation. A result of such a combined measurement of two FeCAP devices is shown in Fig. 3b. Each of the two devices was set into either a Program or Erase state (which corresponds to logic "1" or "0", respectively). All 4 possible combinations were investigated, namely "00", "01", "10", "11", where the first bit corresponds to the value stored in device A and second bit in device B, respectively. The switching pulse was applied to both plate lines during the read operation, such that the polarization state of both devices influences the signal. From Fig. 3b one can see that when both FeCAPs are in Erase state ("00", blue line) there is no increase in current as compared to the pre-charge level. This is to be expected since in this configuration there will be no polarization reversal, and hence no switched charge that would increase the potential at the internal node n1. On the other hand, if both FeCAPs are in Program state ("11", red line) the resulting current is the highest. The other 2 states ("01" and "10") result in the current that is in between the "00" and "11" case. The obtained results allow to perform logic operations between the two bits e.g. by choosing a current threshold when reading the signal at the SL. For example, by setting a threshold in between "11" and "01"/"10" levels a logic AND operation is obtained. In case of setting a threshold between

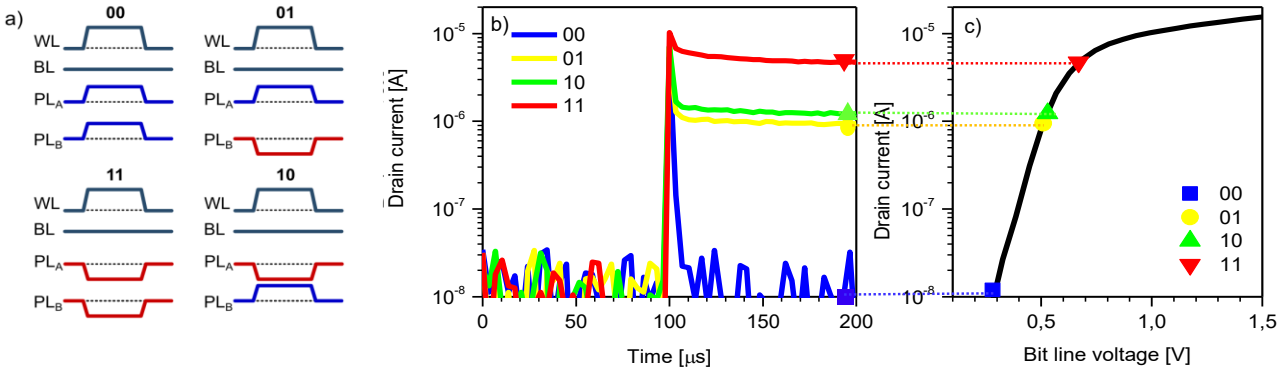

Fig. 3 a) Program pulses used to set the cell into logic states. b) Result of a FeCAP measurement depending on the internally stored value. A clear separation between "00", '01'/"10" and "11" states is observed. c) Id-Vg characteristics of a read-out transistor.

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"00" and "01"/"10" levels it is possible to perform the logic OR operation. The obtained result might be processed further outside of the array or might be directly written back to the capacitors A or B via the BL. In general the write back operation could be performed similarly as in conventional FeRAM, that is, after signal development via the SA that is connected to SL and transferring the signal directly or inverted to the BL. Fig. 3c shows the I_d-V_g characteristics of the read-out transistor T3. By using it one can deduce the voltage at the internal node n1 at a given current level. The results of this transformation are given in Table 1. When both devices are in erased state ("00") the voltage at node n1 V_{n1} is close to the pre-charge value (V_{pc} = 0.4 V). However, it is slightly lower due to the capacitive coupling between internal node and word line which leads to a slight decrease in voltage at node n1 during the falling edge of word line pulse. Programming either of two bits leads to an increase of about 240 mV as compared to a pre-charge voltage. The addition of one extra programmed FeCAP ("11") increases internal voltage by another 150 mV as compared to the "10" case. By optimizing V_{pc} and V_{switch} it is possible to adjust the value of V_{n1} after switching – either into the sub-threshold region of the I_d-V_g characteristics of T3 to attain a larger separation of current levels between the different logic states, or into the linear region of T3 to increase the read current at the SL.

TABLE I. VOLTAGE AT INTERNAL NODE V_{n1} AFTER SWITCHING

bit A	bit B	V_{n1}, mV
0	0	280
0	1	520
1	0	530
1	1	680

B. *Logic operation between 4 bits in 2T4C cell*

It is possible to extend the described approach even further and apply it to a larger number of FeCAP devices. For example, Fig. 4 shows the result obtained for four FeCAPs connected in parallel. Five distinct current levels are observed, that correspond to the number of FeCAPs set into Program state. The other combinations, that correspond to the same number of "1"s are expected to follow the same behavior (e.g. "1100" should be identical to "1010", if device to device variability is small). This allows to perform logic operations between more than two bits or use as a multilevel memory cell.

Important to note here is that the behavior of this memory cell is highly dependent on the capacitance ratios between the FeCAP and the gate capacitance of the read-out transistor. This is because during the switching pulse, voltage is applied across the capacitive voltage divider, and the potential at the internal node is determined by the capacitive voltage divider

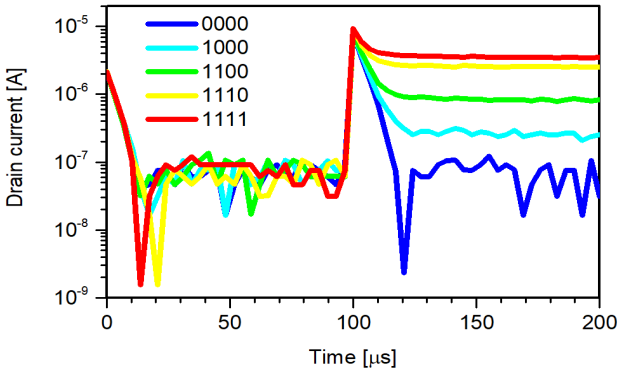

Fig. 4 FeCAP measurement of 4 FeCAPs connected in parallel depending on the stored value.

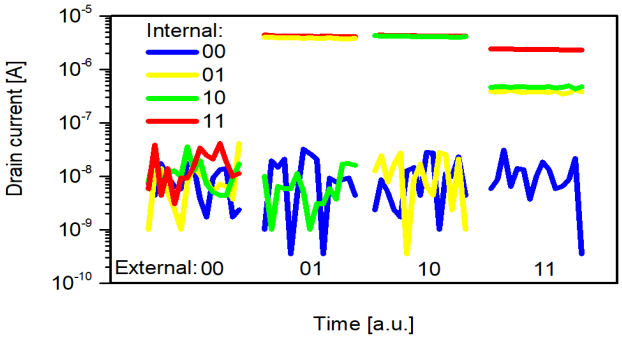

Fig. 5 Result of logic operation between internally stored values in 2 FeCAPs and external input (presence or absence of switching voltage at the corresponding plate line). The measured current levels at SL after applying the switching pulse are shown.

ratio. This in turn influences the voltage drop across the FeCAP, which determines whether the polarization will switch or not. In the case of using 4 FeCAP devices, as described above, the effective capacitance of the FeCAP part of this voltage divider is increased by a factor of 4 as compared to a single FeCAP. This leads to a smaller voltage drop across the FeCAPs and hence a smaller switching charge in sub-loop operation, which reduces the obtained signal. The effect can be compensated by applying a larger common read pulse voltage to the PLs or by applying consecutive read pulses to the individual PL of each capacitor.

C. *Logic operations with external input in 2T2C cell*

Another step towards performing logic-in-memory operations is to use the applied external PL read voltage as a second logic input signal. This way, the magnitude of a signal will depend on whether the switching voltage V_{switch} was applied to a particular bit or not, as demonstrated in Fig. 5. When V_{switch} = 0 V is applied to both FeCAPs – no signal will be detected, because neither of the devices received the switching voltage and hence no switched charge will be present. In contrast, if V_{switch} = 4.0 V is applied to device B, while device A is kept grounded which corresponds to the external input of "01", the signal will only depend on the value stored in the device B. This means that the current is high when the state of device B is "1" and it is low when the state is "0", no matter what the state of device A is. It is obvious that the logic AND operation is performed between the external input and the value stored inside the FeCAP. The results of other possible combinations of external input are presented in Fig. 5. The case of external "11" (both devices are selected) corresponds to the logic operation between stored values as was discussed in the section above. However, there is an interesting remark to be made. In this case, the current level corresponding to internal "11" state (red curve) is lower than the equivalent current level when only one of the two devices is selected. This is due to the different capacitive voltage divider ratios (larger ferroelectric capacitance when both devices are selected, hence lower voltage drop across FeCAP and hence less switched charge). This effect might also be beneficial in certain situations. For example, if the threshold for detecting the logic state at the SL is set such that it is above the internal value "11" level for external "11", but below the "11" level for external "01" and "10", then effectively the XOR gate for the external input is obtained. Moreover, in analogy to memristive devices that are connected in a similar way as the ferroelectric capacitors in this work [8], IMPLY logic operations might be performed by combining readout and write-back operation in a suitable way.

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D. Logic operations in FTJ operation mode

In addition to a FeCAP mode, this memory cell can be used with ferroelectric tunnel junctions (FTJ). FTJ operation is based on the tunneling electroresistance (TER) effect, which manifests itself as a polarization-dependent resistance of a stack consisting of a ferroelectric layer sandwiched between two (asymmetric) electrodes. It is analogous to the tunnel magnetoresistance effect observed in magnetic tunnel junction. The TER effect originates from the difference in effective tunnel barrier height, depending on the polarization direction. This is due to an asymmetric screening of polarization charges inside two different electrode materials [9]. From circuit theory perspective, the FTJ can be seen as a memristor, where the memristance of the device depends on the history of device operation in terms of applied voltage over time and gradual switching between different memristance states can be achieved [10]. However, in this study we use just digital values, thus switching the FTJ just between high resistance state (HRS) and low resistance state (LRS), respectively. Moreover, the restriction of using a very thin ferroelectric operating in the direct tunneling regime can be overcome by using a double layer tunneling junction as described in [11]. In the FeFET structure utilized here, the interface layer acts as the tunneling barrier. Write operation in FTJ mode is identical to that for the FeCAP. The first step of a read operation is also similar, starting by applying a pre-charge voltage to the bit line to set the operation point of the read-out transistor. It is then followed by an application of a negative bias voltage V_{bias} to the plate line, in order to reach a certain voltage drop across the ferroelectric layer which is necessary for tunneling to occur. In contrast to the FeCAP measurement, the access transistor is kept open during rising edge of PL pulse, which ensures that node n1 stays at the pre-charge voltage. After this the access transistor is closed and the drain current of a read-out transistor is recorded. Because of the polarization state dependent current flowing through the FTJ, the potential at node n1 will decrease over time. Finally, this will lead to a reduction of the voltage over the FTJ and the read current will decrease, eventually leading to a polarization state dependent saturation of the node voltage n1. The behavior and operation principle of this particular FTJ cell was investigated in detail previously [6]. The idea of performing logic-in-memory operations using FeCAPs can be directly extended towards the FTJs as well. Here, a cell consisting of two FTJs is analyzed and a logic operation between the values stored inside each individual FTJ is demonstrated in Fig. 6. Four measurements were performed, corresponding to different combinations of programmed/erased states of the two FTJs. As expected, in the case when both FTJ are set into Program state ("11", red curve) the current is decreasing faster than the signal for "00" state. When only one of the two FTJs is set into Program state while the other one is in Erase ("01" and "10", yellow and green curves respectively) the current level is located in between "00" and "11" curves. Thus, similar logic operations can be attained as were shown for the FeCAP case depicted in Fig. 3b. However, the benefit of FTJ operation is the non-destructive readout, which means, that the stored logic states will persist and do not have to be refreshed after readout.

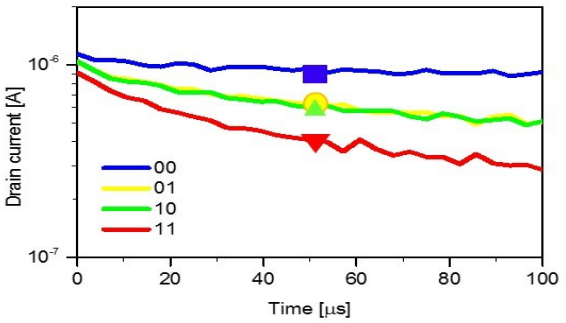

Fig. 6 FTJ measurement showing the possibility of LiM operation. A clear separation of the read currents by a factor of 2 can be observed after a signal development time of 50µ as indicated by the symbols.

V. Summary

A 2T2C / 2T4C memory cell is presented that can be realized in small scaled state-of-the-art CMOS technologies without the need for integration of a 3D capacitor. Besides pure memory operation, the cell allows to perform logic operations between multiple bits that are stored inside the cell as polarization state of individual FeCAPs. In addition, the ability to adopt variable read pulses as externally applied logic states leads to even greater flexibility in implementing logic-in-memory architectures. Finally, an outlook for FTJ based logic operation is given.

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