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A Physical Synthesis Flow for Early Technology Evaluation of Silicon Nanowire based Reconfigurable FETs

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***Abstract*—Silicon Nanowire (SiNW) based reconfigurable field-effect transistors (RFETs) provide an additional gate terminal called the program gate which gives the freedom of programming p-type or n-type functionality for the same device at runtime. This enables the circuit designers to pack more functionality per computational unit. This saves processing costs as only one device type is required, and no doping and associated lithography steps are needed for this technology. In this paper, we present a complete design flow including both logic and physical synthesis for circuits based on SiNW RFETs. We propose layouts of logic gates, *Liberty* and *LEF* (Library Exchange Format) files to enable further research in the domain of these novel, functionally enhanced transistors. We show that in the first of its kind comparison, for these fully symmetrical reconfigurable transistors, the area after placement and routing for SiNW based circuits is 17% more than that of CMOS for MCNC benchmarks. Further, we discuss areas of improvement for obtaining better area results from the SiNW based RFETs from a fabrication and technology point of view. The future use of self-aligned techniques to structure two independent gates within a smaller pitch holds the promise of substantial area reduction.**

I. Introduction

Silicon nanowire based functionality enhanced transistors also called reconfigurable transistors (RFETs) provide an alternative path to increase the number of functions offered by a particular logic gate. SiNW RFETs are a potential candidate to complement CMOS technology in selected applications because of their unique polarity control and equalized driving strength for p-type and n-type devices with equal footprint area. Reconfigurability in SiNW RFETs allows the freedom of choosing symmetrical p-type or n-type functionality from the same device as programmed at runtime through a dedicated program voltage. Such polymorphism is generally seen in circuits like FPGAs or CGRAs but at a coarser grain configuration level. This is also observed in ASICs but it comes at the cost of extra chip area which compensates the gains from scaling. SiNW RFETs offer similar polymorphism at smaller area overheads. Structurally, SiNW RFETs tend to demolish the pull-up and pull-down barrier by combining both of the functionalities.

In spite of its great promise, most of the work in this domain has been mainly at the logic level as discussed in [1], [2], [3] and [4]. While [1] demonstrated efficient and exemplary logic gates, [2] and [3] showed the potential of these RFETs in bigger circuits and SOC core components respectively. DeMarchi et al. in [5] explained device characterization for SiNW RFETs. Further, they provided a detailed explanation of device fabrication using a stacked nanowire approach. They also showed that XOR logic is an inherent function of the device itself. On the other hand, [6] demonstrated a novel layout technique to address the routing congestion arising from the extra gate terminal in the SiNW RFET. However, their approach was technology independent and they showed layouts for basic logic gates only.

None of these works has tried to demystify the entire design flow – logic synthesis up to physical synthesis for SiNW RFETs. Neither is there an evaluation of silicon nanowires through a parallel CMOS standard flow from a technology perspective. We have not considered vertically stacked nanowire FETs as mentioned in [5]. We have formalized a complete physical synthesis flow along with layouts for various logic gates. Then, using these logic gates, we ran the entire flow and compared area numbers for MCNC benchmark [19] circuits with the standard CMOS flow. We define both static and reconfigurable ready layouts of logic gates. For simplicity, we have exclusively used dual gate RFETs as our basic building blocks.

Contributions: Major contributions of the present work are–

- Based on the electrical characterization of SiNW RFETs, a table model was proposed based on the I-V properties of scaled silicon nanowire ribbons considering stressors to adjust symmetry [7]. We propose a 22 nm technology to pattern the minimal individual nanowire ribbon width and to define the half pitch between parallel arranged nanowire channels. The target technology in our paper is the fully symmetrical RFET as proposed in [8], adapted to an SOI platform.
- We propose for the first time the layouts for a set of logic gates based on SiNW RFETs. We also extend these layouts to demonstrate a reconfigurable ready layout for the MINORITY logic gate.
- We provide a physical synthesis flow along with a standard cell library under an open source license including *LEF* and *Liberty* files to facilitate further research from the technology point of view [9].

We studied various aspects by running the above flow with MCNC benchmarks to get the area numbers for SiNW based circuits and compared them to the standard CMOS flow. A detailed analysis in order to achieve better area numbers has been done from the manufacturing and fabrication point of view. This has been done to promote SiNW as a technology that can be co-integrated with CMOS, e.g. for selected applications employing inherent reconfigurability, such as hardware security circuits [10]. The present work has been organised in the following sections. Section II explains about silicon nanowire as technology and how its transfer characteristics have been used to formalize the layout and generate the *LEF* and *Liberty* files. Section III summarizes the experimental setup and provides a detailed analysis of the results of our experiments. This is followed by concluding remarks in Section IV.

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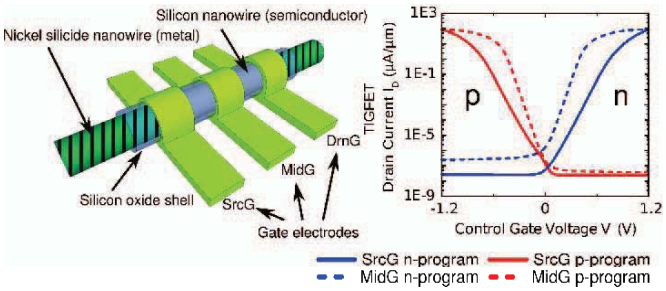
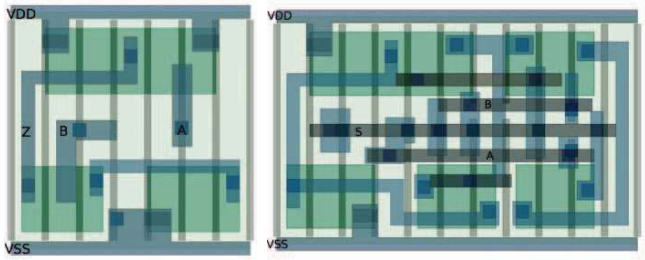


Fig. 1: Structure of SiNW RFET and Transfer Characteristics Showing Symmetrical *p* and *n* Functionality [2].



(a) Static NAND **(b)** Reconfigurable MINORITY

Fig. 2: Layouts of Logic Gates

II. Silicon Nanowire Reconfigurable Transistors: A Technology Perspective

A. Silicon Nanowire Ribbon Reconfigurable Transistors

Fig. 1 represents a 1-D dopant-free mono-crystalline nanowire structure made of silicon as shown in [2]. The nickel silicide metal contacts form Schottky junctions at the source and drain contacts. The gate overlapping with the source is called the control gate (CG). It controls the carrier flow. The gate overlapping with the drain is called the program gate (PG) and it selects the charge polarity. Transfer Characteristics in Fig. 1 represent fully symmetrical p-type and n-type functionality [8]. The device can be steered either with three or two gates. In the three gate configuration with the middle gate MidG as the control gate, the dashed transfer curves are obtained. The signal at the outer gates, DrnG and SrcG, control the p-type or n-type nature of the transistor. In the dual gate configuration, the middle gate is left out in the design and the solid transfer curves are obtained. In the latter, DrnG acts as the program gate selecting p-type or n-type configuration and SrcG acts as the control gate.

For this work, we propose an SOI based 22 nm technology to pattern the minimal width of individual nanowire ribbons and to define the half pitch between parallel arranged nanowires. These features can be achieved with a conventional 45 nm technology node and a spacer pattern transfer technology as commonly done for *fin* patterning in FinFETs. The top Si thickness is set to 6.0 nm and the effective gate oxide thickness (EOT) is set to 1.0 nm. To accommodate the two parallel gates per device, we chose the technologically simplest route with a gate pitch of $\sim$110 nm and an active channel length of $\sim$100 nm. This would imply a gate composition and patterning flow as similar as possible to the commonly employed MOSFET gates in CMOS. As only a single kind of transistor type would be needed and no doping would be required, at least one lithography step and four implantation steps with associated dopant activation anneals would be spared compared to a 45 nm CMOS technology. Nevertheless, we do note that the transistor cells for the RFETs can be defined in a much more compact way e.g. by self-alignment as previously shown in [5]. This would require an additional lithographic step compared to our approach but would allow in our case a channel length shrinkage from 100 nm to $\sim$48 nm or less. Since RFET devices exhibit Schottky junctions, they introduce an energy barrier even in the on-state, therefore drive currents are lower than in conventional MOSFETs for comparable dimensions. Accordingly, they are slower as compared to CMOS based devices but they have substantially lower static leakage power consumption. Germanium nanowires as implemented in RFETs [11] offer a similar structure but better electrical properties. Therefore, they are able to outperform previous polarity-controllable device concepts on other material systems in terms of minimized threshold voltages and higher normalized on-currents. The present work lays the foundation for emerging reconfigurable technologies with different channel materials.

B. Layouts for Logic Gates

Fig. 2 refers to the proposed layout for logic gates using SiNW dual gate RFETs exclusively. For gate level representation of these layouts, readers are advised to go through [12] as the authors have represented the gates in terms of RFETs. Multi-input gate FETs like TIGFETs and MIGFETs exhibit a higher potential for minimizing the transistor count and saving the overall area. However, in the present work, we have not considered multi-input gate FETs.

Layout for Static Functional Logic Gates: Fig. 2a shows the basic layout of a SiNW RFET based NAND logic gate predefined in a static manner by the interconnect design. The vertical brown lines in the layout are the gate terminals that are self-aligned to the Schottky contacts below. This particular layout is static in nature, i.e. the functionality is defined by the layout and reconfigurability at runtime is not used. One can notice in the NAND layout that the program gates are connected to V_{DD} or V_{SS} internally through vias. This obviously swells up the layout a bit but it does not create additional routing overhead.

Layout for Reconfigurable Logic Gate: The MINORITY gate layout, as shown in Fig. 2b is a reconfigurable ready layout. The dark brown horizontal lines are the input/output points. Depending upon the value of S, this layout of MINORITY gate can function as a NAND gate ($S = 0$) or a NOR gate ($S = 1$). This particular layout possesses more number of gate terminals. Such layouts can be extended for other logic gates to utilize the runtime reconfigurability provided by RFETs. The choice lies in the hand of the circuit designer to choose among the layouts whether to use them in a static design or a runtime reconfigurable design.

C. Table Model for Silicon Nanowire RFETs

The internal structure and material properties of the SiNW transistor is modelled in a TCAD simulator. To enable a realistic estimation of SiNW logic gate timing and area, *Liberty models* are required. To create this model, a SPICE simulation is executed for each table entry.

There is no direct link from TCAD simulations to transistor models for SPICE simulators. Usually, compact models are used which are based on equations. While this compact modelling is necessary for final technology development, in early evaluation stages a more simple table model might offer

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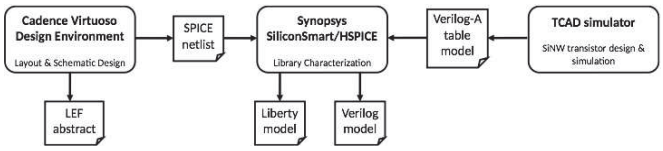

Fig. 3: Tool Flow for Library Characterization for Silicon Nanowires

a better compromise to link transistor design to electrical simulators. Therefore, we exported a table of current, voltage, and capacitances based on DC simulations inside the TCAD environment as a plain ASCII file. For the electrical transistor model, this table is read inside a Verilog-A module and thereby can be used by every analogue SPICE simulator supporting the required Verilog-A constructs. Although this approach cannot model dynamic charge distributions inside the transistor channel, we compared the simulation results of a small circuit in TCAD and SPICE and verified that the transient delay error between both simulations is within 20% and is thereby a valid approximation for early technology development. The parasitic capacitances for a typical transistor structure, upto Metal1, have been included in this model.

For library characterization, Synopsys SiliconSmart is used which integrates all required functionality if a cell netlist and transistor model files are provided. Based on the cell function, it generates all the timing and power arcs and a set of corresponding HSPICE simulations for each table entry. It then extracts the results and writes out a *Liberty* file and a matching *Verilog behaviour model*. Based on the SiNW technology status, there is currently only one operating condition characterized which is a typical one at a supply voltage of 1.8V. While these simulations provide timing and power numbers, the area of the SiNW logic cells needs to be extracted from real cell layouts. As shown in the previous section, these layouts follow advanced node design rules and the *LEF* layout abstract files for Place & Route are created by the Cadence Abstract Generator. These *LEF* files contain information like cell boundaries, metal blockages and pin locations. The area is written to the *Liberty* files. The schematics of the cells are exported as SPICE netlists and are used by the characterization tool. The complete library characterization flow is shown in Fig. 3.

III. Experiments and Results

The table model as explained in the previous section was used as a base model and the *LEF* and *Liberty* files were generated using the tool flow as shown in Fig. 3. We carried out the above process for a set of gates and ran the flow as shown in Fig. 4 on MCNC benchmarks [19] for logic gates based on SiNW RFETs as well as standard CMOS FETs for comparison.

A. Experimental Setup

For our experiments, we used an open source tool, *qflow* [13] as we needed a physical synthesis flow in which various tool optimizations can be controlled.

The qflow tool chain used is shown in Fig. 4. The tool uses other open source tools like Yosys [14], graywolf [16] and qrouter [17] for logic synthesis, placement and routing steps respectively. Yosys internally uses the ABC tool [15].

A *.par* file specific to SiNW RFETs based on the technology information from the *LEF* file was developed. This file is used by graywolf.

TABLE I: Area Results Post Place and Route

Benchmarks	Area CMOS (μm^2)	Area SiNW (μm^2)	% Overhead
b1	5.34	5.56	4.10
b9	49.55	60.6	22.31
C1355	151.36	202	29.35
C17	3.41	4.2	23.20
C1908	164.32	202	22.93
C432	82.27	89.3	8.54
cavlc	331.82	397	19.64
cm138a	14.07	17	20.84
cm150a	13.98	15.9	13.76
cm151a	7.57	8.68	14.69
cm152a	9.18	10.8	17.62
cm162a	19.41	22.7	16.96
cm163a	18.66	22.2	18.98
cm42a	12.91	15.6	20.85
cm82a	9.39	11.2	19.32
cm85a	18.77	21.4	14.00
ctrl	60.45	71.5	18.27
cu_synth	26.59	29.8	12.07
int2float	99.09	118	19.08
router	123.41	143	15.87
t481	336.36	401	19.22
tcon	18.77	21	11.86
x1	199.55	239	19.77
x2	22.95	26.8	16.75
z4ml	16.84	18.8	11.63
Average			~17%

For obtaining the final layout in the GDS2 format, the tool Klayout [18] is used to get the overview of the post-layout circuit.

For the experiments, we have used a CMOS based open source standard cell library for comparison. The open source library from *FreePDK45* [20] is based on 45 nm CMOS technology. We then use technology scaling as mentioned in [21] so as to have a fair comparison with 22 nm *SOI*-based silicon nanowire library. Both these libraries contain a basic set of logic gates as mentioned in [1]. Our standard cell library contains INV, NAND, NOR, XOR, MUX, BUF and MINORITY gates.

B. Benchmarks

Table I shows the area calculation using our physical synthesis flow. This area is the post place and route area for both CMOS and SiNW technology. We scale the CMOS area numbers for 22 nm technology node for a fair comparison with SiNW. The authors in [21] describe that for scaling from 45 nm technology node to 22 nm technology node, a scaling factor of 4.4 gives a good estimate. We ran experiments using our physical synthesis flow for MCNC benchmarks and found that SiNW based circuits occupy 17.43% more area as compared to their CMOS counterparts. Since an individual SiNW based transistor is bigger than a CMOS based transistor in a conventional gate patterning flow having a large gate pitch, the area for all the logic gates will increase with an increase in the number of RFETs in the logic gates. In the following sections, we explain the possibility of obtaining better area numbers using various techniques.

C. Parameters Which Affect The Area

The present work presents a complete feasibility study of the design route by taking into account a simplified technology flow for the gate patterning and manufacturing. Nevertheless, as stated in Section II-A, it is technically possible to substantially reduce the length of the transistor cells by the use of self-aligned techniques for double gate patterning in combination with an additional lithography step. This additional technological effort would bring a benefit in circuit size. The RFET could be realized with a total channel length of 48 nm, compared to the 100 nm used here. The electrical performance of such a scaled RFET device has already been verified by TCAD simulation and benchmarked in terms of inverter delay and power consumption in the work of [12]. The transistor cell length could be reduced from a total length of ~188 nm down to 92 nm. Consequently, the layouts of Fig. 2 will substantially reduce in size, although not by the same factor as the design

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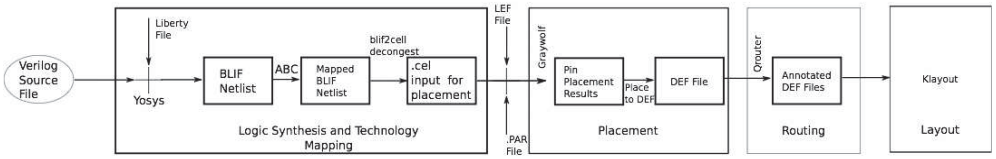

Fig. 4: Physical Synthesis Flow Through Qflow[13] Yosys [14] ABC[15] Graywolf[16] Qrouter[17] Klayout[18]

rules have to be met. Another opportunity to actively reduce the device area is vertical stacking of multiple nanowires ([22], [23]) as already demonstrated for polarity control devices with four stacked nanowires by de Marchi et al. [5]. This will lead to a substantial reduction of device width and accordingly to a reduced cell height of the layouts in Fig. 2. One can anticipate that reduction in nanowire channel length will have a positive impact in the reduction of capacitances and RC delay of the transistor [12]. For stacked nanowires, methods on controlling RC delays explored in [24] can be applied to RFET devices as well.

D. Use of Germanium Nanowires Channels

In terms of circuit speed and power consumption, a promising solution is to use germanium or silicon-germanium nanowire channels instead of silicon nanowires. Silicon germanium and pure germanium channels are conventionally used for p-FETs. Indeed it has been shown experimentally and by TCAD simulations [11], that the use of germanium nanowires for RFETs is feasible. Germanium brings benefits in performance and power consumption of RFETs both for p-type and n-type characteristics. The lower band gap of germanium together with the higher tunnelling probability is able to enhance the device drive currents by a factor of 10. The expense for taking this route is a higher static current, however the inherent blocking nature of the RFETs program gate is able to filter out a substantial level of source-drain leakage. The lower Ge bandgap also enables the reduction of the supply voltage of RFETs from 1.8V to $\sim$0.8V, thereby reducing dynamic power consumption of the transistors to less than one-fourth of the SiNW RFET value.

IV. Conclusion

In the present work, we demonstrated a physical synthesis flow for early technology evaluation for Silicon Nanowire reconfigurable FETs. We have designed both static as well as reconfigurable layout designs for some logic gates of which the NAND gate and the MINORITY gate are discussed. Further, we carried out an extensive evaluation for physical synthesis flow for MCNC benchmarks in terms of area and found that on an average the area of SiNW based logic circuits is 17% more than that of CMOS. This physical synthesis flow is made available online under open source license for technology evaluation of further progress in silicon nanowires. However, the flow presented in this work is not only limited to silicon nanowires but can also be applied to other future emerging technologies. We also discussed the possible approaches in which this difference in area can be reduced. We considered various techniques which can be employed for SiNW RFETs for denser packing of transistors. Further, with reduction in transistor cell size, capacitances and RC delay will be reduced. This will, in turn, improve the performance of SiNW RFETs. Additionally, we discussed other emerging nanowire based technologies which exhibit high performance and lower dynamic power consumption. Such technologies can be efficiently employed for reconfigurable-ready circuits. The greatest promise which the silicon nanowires hold is that they are compatible with the current silicon technology. We envisage that SiNW RFET based technology can complement CMOS for a wide variety of applications.

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