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Junction tuning by ferroelectric switching in silicon nanowire Schottky-barrier field effect transistors

V. Sessi^{1,2}, H. Mulaosmanovic³, R. Hentschel³, S. Pregl³, T. Mikolajick^{1,2,3}, and W. M. Weber^{2,3}

¹*Technische Universität Dresden, Dresden, Germany Email: violetta.sessi@tu-dresden.de,*

²*Center for Advancing Electronics Dresden, Dresden, Germany*

³*NamLab gGmbH, Dresden, Germany*

Abstract—We report on a novel silicon nanowire-based field effect transistor with integrated ferroelectric gate oxide. The concept allows tuning the carrier transport in a non-volatile approach by switching the polarization in the ferroelectric layer close to the source Schottky-junction. We interpret the results in terms of tuning the transmissibility of the Schottky-junction for charge carriers. The experimental results provide a first step towards the integration of memory-in-logic concepts with reconfigurable nanowire transistors.

I. INTRODUCTION

Silicon nanowires (SiNWs) are considered amongst the most promising building blocks for future electronic devices [1, 2], due to their ultimate scalability in a surround gate architecture and their compatibility with existing CMOS processes. Beyond CMOS scaling, the high sensitivity to external electric fields opens the path towards enhanced device functionality that is in the focus of current research.

One route to add new functionality is the integration of switching materials to the transistors and by this merging memory functionality into computing. Recently, it has been shown that a charge trapping layer can be added to a reconfigurable field-effect transistor (RFET) [3] and realize a nonvolatile memory function integrated into the computing device [4]. However, this solution requires quite high switching voltages. Here, we show that it is possible to introduce non-volatility in SiNW FETs by means of thin ferroelectric layers based on doped hafnium oxide HfO₂.

Ferroelectricity in doped HfO₂ was first reported in 2011 [5]. It is argued that this property is induced by the stabilization of a non-centrosymmetric orthorhombic phase upon annealing. Different from conventional ferroelectrics like Pb[Zr_xTi_{1-x}]O₃ which show several integration and scaling issues, HfO₂ is a high-k dielectric already in use in CMOS manufacturing. When doped with suitable dopants and/or a particular fabrication procedure is applied, the ferroelectric HfO₂ phase can be stabilized.

Very important for applications, HfO₂-based ferroelectrics show stable ferroelectricity with high coercive fields in the 1 MV/cm range for comparatively thin films of 5 nm – 30 nm thickness. This allows downscaling of devices and reduction of the gate-stack height. Compatibility with miniaturized metal-oxide-semiconductor FETs (MOSFETs) has been

established for laterally scaled ferroelectric FETs (FeFETs) having the channel length and width of 30 nm and 80 nm, respectively [6]. Recently, large FeFET memory arrays based on Si:HfO₂ have been successfully demonstrated [7, 8].

In this work we show first results of the integration of a HfO₂-based ferroelectric gate oxide in SiNW Schottky-barrier FETs (SiNW SB-FETs). Schottky contact geometries of SiNW SB-FETs provide sharp, exposed junctions whose transmissibilities can be modified by locally applied electric fields [9]. Here, we expose the injecting source junction to a Al:HfO₂ layer and observe non-volatile gating of the Schottky contact, which can be attributed to the remanent ferroelectric Al:HfO₂ polarization. The switchable ferroelectric unit functions as a non-volatile valve which either passes or blocks low energy holes. As a result, the SiNW SB-FET can be reversibly tuned by voltage pulses between two states with resistance differing by more than one order of magnitude.

II. RESULTS AND DISCUSSION

A. SiNW SB-FET with Pt contacts

For simplicity we build our device demonstrators with bottom-up grown SiNWs. The SiNWs are formed by the vapor-liquid-solid growth mechanism in a chemical vapor deposition (CVD) furnace, using synthesized catalytic gold nanoparticles with 20 nm average diameter. The gas precursor is mono-silane SiH₄ and the CVD process temperature and deposition time are T = 450 °C and t = 40 minutes, respectively. The resulting NWs are undoped and crystalline, with length of approx. 30 μm and average diameter 20 nm.

To provide multiple conduction channels a parallel arrangement of SiNWs is transferred to a degenerately p-doped Si/400 nm SiO₂ substrate by contact printing [10]. Gold nanoparticles are chemically etched by *Aqua Regia*. Next, a thermal oxide is grown on the NWs by rapid thermal oxidation (O₂ at 875°C, for 5 minutes), followed by a forming gas anneal. The resulting oxide shell is approx. 10 nm thick.

In this work we focus on p-type SiNW SB-FET. Thereto, the SiNWs are contacted by interdigitated Pt source (S) and drain (D) contact leads [Figs. 1 (a) and (b)] and annealed at T = 500 °C for 1 minute. Pt intrusion into the SiNWs and formation of the metallic Si_xPt_y segment visible in Fig. 1 (c) deliver abrupt and exposed Schottky-junctions (SJs). The

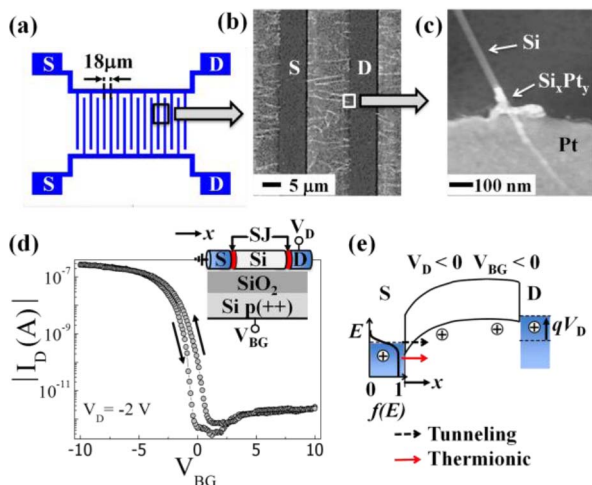


Fig. 1. SiNW SB-FET before Al:HfO₂ deposition. (a) Scheme of the interdigitated source (S) and drain (D) contacts. (b)-(c) Scanning electron micrograph (SEM) images showing (b) multiple NWs and (c) the interface region between Si and Si_xPt_y. (d) Drain current (I_D) versus back-gate voltage (V_{BG}) for one representative device. The arrows show the sweep direction. (e) Band diagram of the SiNW SB-FET.

residual intrinsic Si channel together with the two SJs defines a transistor with an active length of approx. 10 μm along the NW axis. More details on sample fabrication can be found in Refs. [11, 12].

In Fig. 1 (d) the absolute value of the drain current $|I_D|$ (in the following, I_D) of the SiNW SB-FET versus the back-gate voltage V_{BG} with an applied drain voltage $V_D = -2$ V is shown. The predominant p-type characteristics are due to the Pt contacts, as Pt has a high work function and its Fermi level aligns near the valence band of Si. Electron transport in these devices is only achieved for high values of V_{BG} . A sketch of the band diagram can be found in Fig. 1 (e). Transport of holes across the barrier occurs via both tunneling and thermionic emission processes. The former is the main contribution to I_D .

B. MIM structures

Several dopants are known to induce ferroelectricity in HfO₂. Examples are Si, Al, Y, Sr, La and Gd [13, 14]. Here we focus on Al doping, because of the availability as a standard ALD process.

Control structures made of planar metal-insulator-metal (MIM) capacitors processed on Si wafers are fabricated and characterized to determine the optimal Al concentration for integration in the NW FETs. Al:HfO₂ films are deposited by atomic layer deposition (ALD) with tetrakis(ethylmethylamino)hafnium (TEMAHf), and trimethylaluminum (TMA) as precursors. The oxidant is H₂O and the purge and carrier gas is N₂.

The Al concentration is varied by the cycle ratio of the metal precursors and ranges between 2 and 16 cationic percent (cat%). The thickness is kept constant for all samples by adjusting the number of TEMAHf:TMA supercycles.

TiN electrodes are deposited by reactive sputtering of Ti in N₂ plasma at room temperature. The obtained MIM stacks with 20 nm thickness are then annealed in a rapid thermal

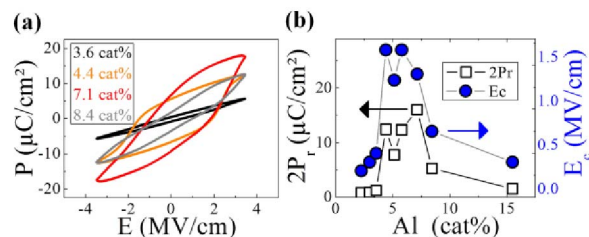


Fig. 2. MIM control structures with various Al:HfO₂ with different Al content. (a) Polarization (P) versus electric field (E) curves after 10^4 field cycles. (b) Double remanent polarization ($2P_r$) and coercive field (E_c) versus Al content, extracted from (a).

anneal chamber in N₂ atmosphere at 800 °C to promote the ferroelectric phase. Pt dots are finally deposited on the MIM stack and provide a hard mask to structure the TiN top electrode by an SC1 etch.

Polarization–voltage (P – V) measurements in Fig. 2 (a) are performed by an aixACt Systems TF Analyzer 3000. The curves are recorded after 10^4 wake-up cycles, at a frequency of 10 kHz. The extracted double remanent polarization $2P_r$ and coercive field E_c values are plotted in Fig. 2 (b) versus the Al concentration. From these results the optimal Al content delivering the highest $2P_r$ and E_c values is found to be between 4 cat% and 8 cat%. The reported values for $2P_r$ and E_c are comparable to what was found in previous works [15].

C. Polarization switching effects in SiNW SB-FETs

The Al content selected for the NW FETs is ca. 7.1 %, as given by 8 supercycles with (24:1) TEMAHf:TMA cycle ratio. The same layer thickness as in the MIM structures, i.e. 20 nm, is chosen for the ferroelectric gate. Meander-shape top gates source-gate (SG) and drain-gate (DG) are structured on the sample as in Fig. 3 (a), aligned to the underlying S and D contacts, respectively. The individual gates couple to the S and D junctions independently. Herewith it is possible to locate a specific ferroelectric polarization at a distinct device region.

The metal top gate is TiN/Pt (10 nm/ 20 nm). Annealing of the entire gate stack is performed at reduced thermal budget ($T = 600$ °C for 20 seconds, in N₂ atmosphere) compared to the MIM structures to avoid critical diffusion of Pt. Characterization of Al:HfO₂ directly on the NW device is shown in Figs. 3 (c)-(d). P - V measurements are performed in a shielded probe station equipped for pulsed and DC measurements. Field-cycling is performed by application of the voltage between the SG and the S, with the DG floating (see sketch in Fig. 3 (b)). The effect of wake-up cycles, also observed for the corresponding MIM structures (not shown), is visible in Fig. 3(c). After field cycling the two separated current peaks merge into a single peak and the hysteresis becomes wider, as expected for HfO₂-based ferroelectrics [16]. The normalization used in Fig. 3 (d) includes the overlap area between S and SG. Compared to the MIM structures the $2P_r$ is reduced, due to the lower annealing temperature [15]. Furthermore, the leakage increases.

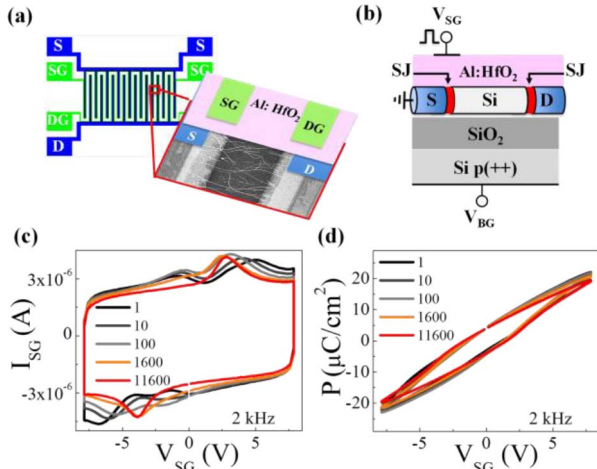


Fig. 3. SiNW SB-FET with Al:HfO₂ gate oxide. (a) Layout of the meander shape top gates SG and DG aligned to the S and D contacts, and SEM image of the area marked in red. (b) Measurement geometry. (c) SG Current (I_{SG}) versus applied SG voltage (V_{SG}). Each curve is recorded after the number of wake-up cycles indicated in the caption. (d) Polarization (P) versus applied V_{SG} , extracted from (b).

However, the current peaks shown in Fig. 3 (c) clearly demonstrate ferroelectric switching.

The transfer characteristics of a SiNW SB-FET with Al:HfO₂ gate oxide are measured according to the geometry and sequence sketched in Figs. 4 (a) and 4 (c). A pulsed voltage V_{SG} with amplitude of 7V is applied at the SG, as shown in Fig. 3 (a). DC-sensing is instead done by sweeping the V_{BG} in remanence, directly after applying the pulse at SG. In this way, we avoid a possible perturbation of the polarization state that could occur upon sweeping V_{SG} .

In Fig. 4 (c) the DC transfer characteristics of the SiNW SB FET versus V_{BG} with an applied drain voltage $V_D = -2$ V are shown after a positive (red, open circles) or a negative (blue, filled squares) pulse at SG. The different overlaying curves show repeated pulse/DC sensing sequences, as sketched on the top of Fig. 4 (c). When we compare the curves taken with different polarity we observe two effects: i) a sizeable shift of the threshold voltage towards more negative (positive) values after positive (negative) pulse, as

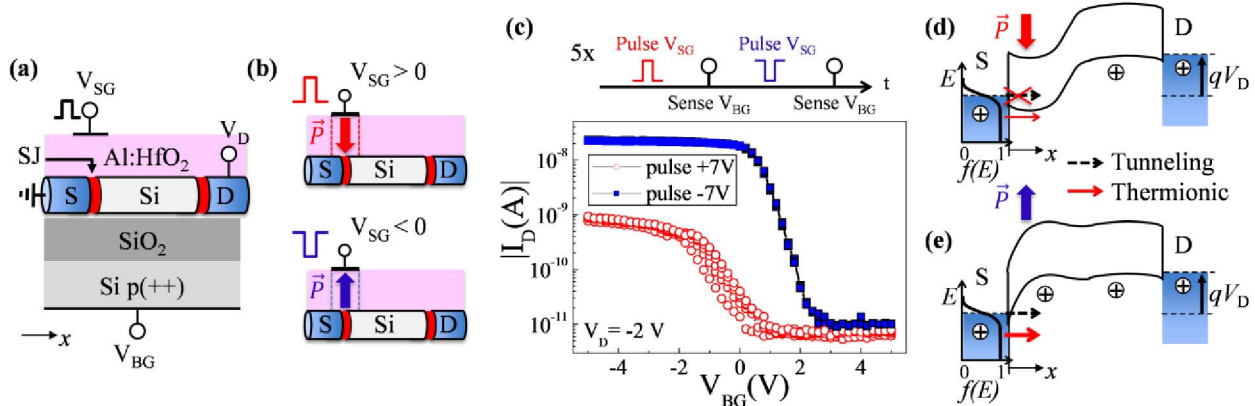


Fig. 4. Transfer characteristics of the SiNW SB-FET with Al:HfO₂ gate oxide. (a) Measurement geometry. (b) Generation of remanent polarization (P) near the SJ at the S contact, after positive or negative source-gate voltage pulses (V_{SG}). (c) Drain current (I_D) versus back gate voltage (V_{BG}) after positive (red circles) and negative (blue squares) V_{SG} pulses according to the sequence on top of the figure. For simplicity only the forward scans are reported. (d)-(e) Sketch of the SiNW SB-FET band diagram with $V_D < 0$ V and $V_{BG} < 0$ V, in presence of a remanent polarization near the SJ at the S contact.

expected for FETs with ferroelectric gate (see for example Ref. [17] for a p-MOSFET) and (ii) a strong reduction of the 'ON' I_D current after positive pulse, observed for both forward and backward (not shown) scan directions. The second effect is not reported for MOSFETs, and the origin has to be sought in the distinctive energy landscape of the SiNW SB-FET. As sketched in the band diagram of Fig. 1 (e), with $V_D < 0$ V and $V_{BG} < 0$ V the SB for holes at the S and D contacts is thinned. Holes can enter the Si channel from the S side via both thermionic and tunneling emission. The holes flow until they leave the channel from the D side. In the specific geometry of Fig. 4 (b), a pulse generates a remanent polarization P in the ferroelectric domains located near the SJ at the S contact. According to our interpretation this additional, local electric field alters the shape of the potential at the S side, enhancing (positive pulse) or decreasing (negative pulse) the SB, therefore effectively tuning the potential landscape of the SiNW SB-FET. As a result, blocking (positive pulse) or promoting (negative pulse) the tunneling and the thermionic emission current at the S contact is achieved, as schematically depicted in Fig. 4 (d)-(e). In the specific case, the ferroelectric unit functions as a non-volatile valve which either passes (Fig. 4 (e)) or blocks (Fig. 4 (d)) low energy holes.

The reported effect is also observed in the DC output characteristics of Fig. 5, recorded in the 'ON' state ($V_{BG} = -5$ V) after positive and negative V_{SG} pulses. After a negative V_{SG} pulse a non-linear output characteristics is observed, especially pronounced at low $|V_D|$. This behavior is typical for SB-FETs since the tunnel barrier width is decreased by V_D , with consequent non-linear enhancement of the tunneling current [11]. On the other hand after a positive V_{SG} pulse, I_D is found strongly reduced, over the entire V_D range. It appears that in this case the influence of V_D over the SBs is hindered, in connection with the diminished transmissibility of the SJ at the S contact (Fig. 4 (d)).

The device 'ON' resistance, including channel and contacts contributions, is extracted as

$$R = \left(\frac{dI_D}{dV_D} \right)^{-1} \Big|_{V_D=0 \text{ V}, V_{BG}=-5 \text{ V}} \quad (1)$$

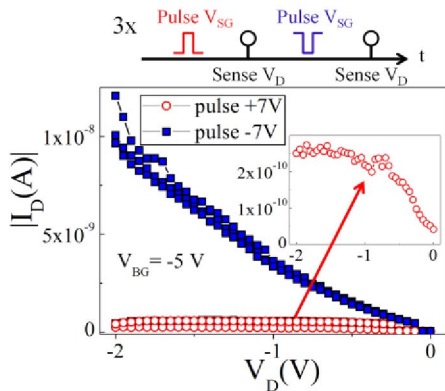


Fig. 5. Drain current (I_D) versus drain voltage (V_D) of the SiNW SB-FET with Al:HfO₂ gate oxide after positive (red circles) and negative (blue squares) V_{SG} pulses according to the scheme on top of the figure. Inset: magnification of the output characteristic after positive V_{SG} pulse.

The ratio r between R values calculated from (1) after positive and negative V_{SG} pulses can be used as an efficiency parameter for non-volatile tuning of the SJ transmissibility. In the device reported here we find $r = 20$.

Finally, charge trapping as a possible interpretation for the observed modification of the transistor characteristics after pulsing can be ruled out. In this case we would expect an opposite effect, e.g. a lowered I_D after negative voltage pulses, as consequence of holes being trapped. Such trapping is for example responsible for the hysteresis in the transfer characteristics of Fig. 1 (d).

III. CONCLUSION

In conclusion, we have presented a new type of device that combines a SiNW Schottky-barrier FET with a HfO₂-based ferroelectric gate stack. The Schottky junction at the source side provides a tuning knob for carrier transmissibility that can be accessed reversibly by a voltage pulse.

The achieved efficient non-volatile tuning of the Schottky-barrier properties via voltage pulses in this prototype can be of significant interest for the research community in the field of low power consumption architectures and non-volatile reconfigurability.

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